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A COMPUTERIZED DYNAMIC CHARACTERIZATION
FOR
MNOS MEMORY TRANSISTORS

by

FRANK ROBERT LIBSCH

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in the Department of

Computer Science and Electrical Engineering

Lehigh University

March, 1984

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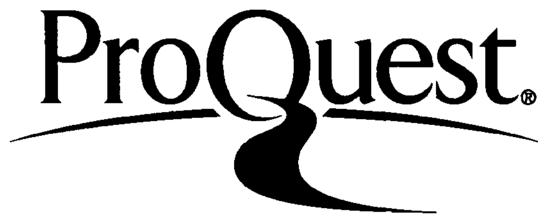

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April 4th, 1984

Date

Professor in Charge

Chairman of Department

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ABSTRACT

This thesis examines the MNOS memory transistor through three characterization measurements: (1) erase/write, (2) retention, and (3) endurance. Characterization measurements were taken by a real-time automated system using a desktop computer (HP-9836), a digitizing scope (Tektronix-7854) and a specially designed pulsing circuit driven with a 10-MHz on-board clock. The system offers flexible (program capability), accurate (100 nanoseconds delay time resolution), automated real-time measurements while minimizing MNOS read disturb factors. The data, theory, and procedure of each measurement is discussed within.

INTRODUCTION

Since their introduction in 1969, MNOS (metal-nitride-oxide-semiconductor) transistors have the potential for wide application in the electronics industry. One popular application of MNOS transistors is as memory elements (EEPROMS) that offer flexibility of random-access memory (RAM) and the nonvolatility of read-only memory (ROM). This application permits the nonvolatile storage--retain data after power is removed --in critical systems.

This thesis concentrates on three characterization measurements that will help us towards understanding and theoretically modeling the operation of the MNOS transistor. Each characterization measurement begins with a discussion of the device physics involved followed by experimental documentation. The last part of each chapter includes a discussion of the measurement techniques and their advantages.

Each characterization measurement is completely automated by the use of an HP9836 desktop computer, a Tektronix 7854 digitizing oscilloscope, and peripheral instruments. The schematic of the equipment in the Device Characterization Lab, Figure 0.1, and the software package developed, Figure 0.2, form the basis of this thesis.

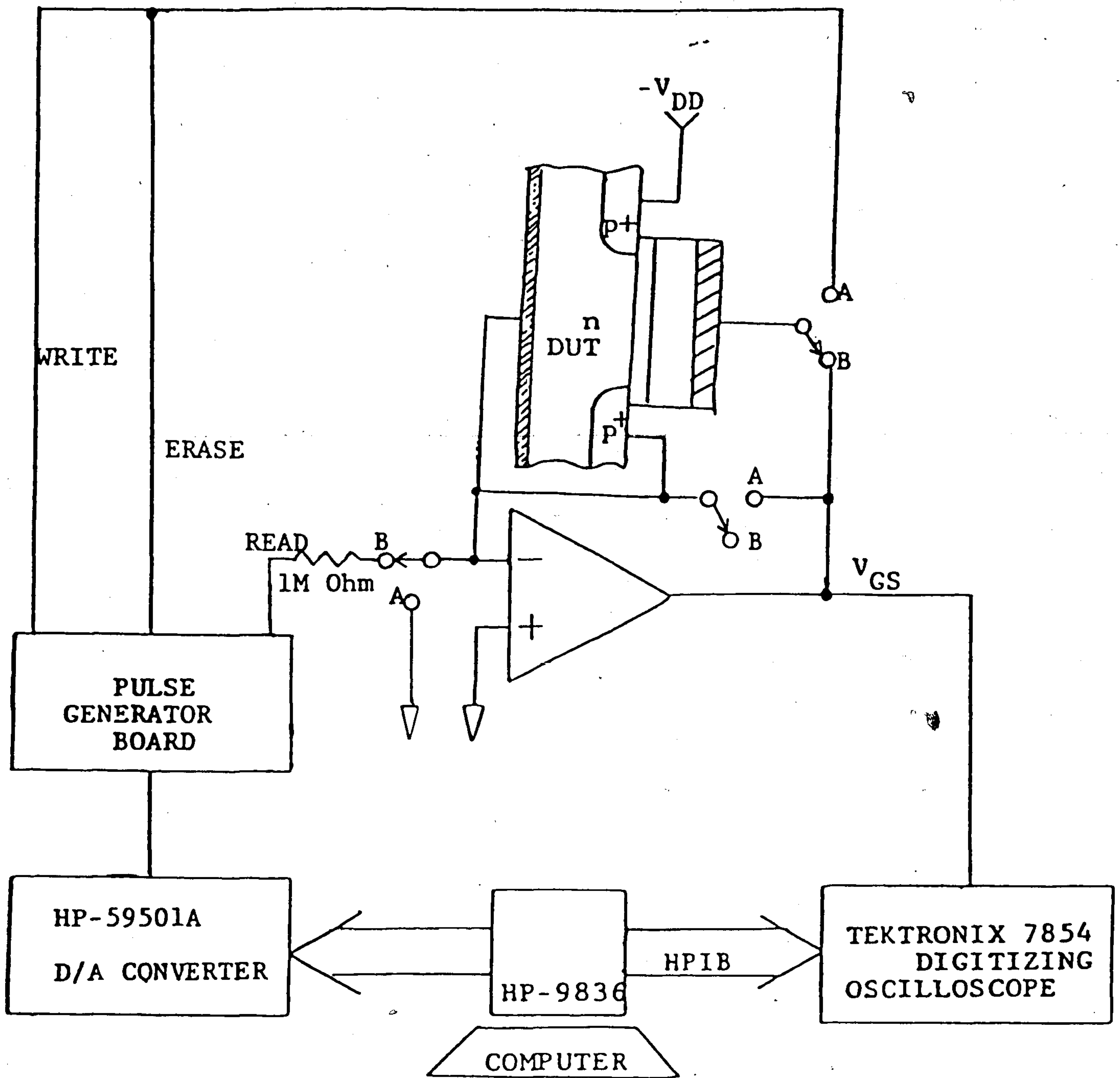


FIGURE 0.1
SCHEMATIC OF LABORATORY SET-UP IN DEVICE CHARACTERIZATION LAB

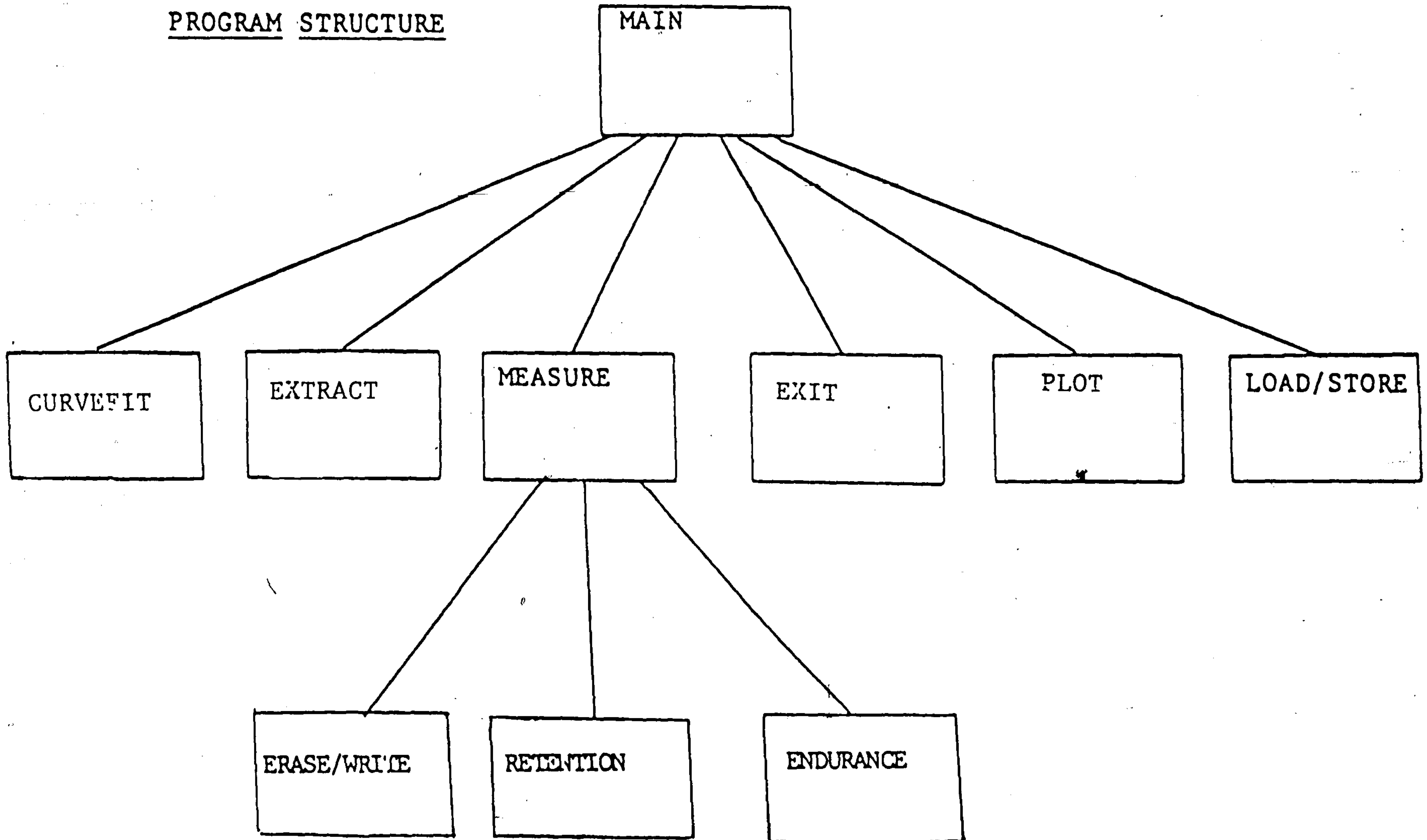


FIGURE 0.2 HP9836 CONTROL PROGRAM STRUCTURE

The first characterization measurement, erase/write characterization, is a test for erasing, writing, and reading the desired threshold voltage within the MNOS transistor (see Figure 0.3a). This is accomplished by programming the computer to apply a predetermined erase and write pulse to the gate of the MNOS device and immediately monitoring the resulting read pulse across the gate to source terminals. The write pulse amplitude curves are recorded with the write pulse width as a function of a change in the threshold voltage.

Chapter 2 is concerned with endurance of MNOS memory transistors (Figure 0.3b). Here the erase and write pulse width and amplitude are predetermined inputs, usually set to force saturation in both states, the high conduction state and the low conduction state of the MNOS device. The computer monitors the change in threshold voltage of the memory transistor after each erase/write cycle applied.

The third chapter deals with the retention of the MNOS device (Figure 0.3c). From the computer's point of view, this measurement is executed in an identical fashion to the endurance measurement program, except a software provision allows only one erase/write cycle. The user instructs the computer to record the threshold voltage for the programmed time duration.

All three measurements are dynamic: The threshold voltage decays with time. As a result, computer control is a must to record the results as an accurate function of time. The first two measurements can be taken in one sitting. The last measurement may take days. However, complete automation requires user's presence only in the setup phase (the first ten minutes).

FIGURE 0.2 MEASUREMENTS POSSIBLE WITH LABORATORY SETUP IN DEVICE CHARACTERIZATION LAB. a.) P-CHANNEL MNOST ERASE/WRITE CHARACTERISTICS, b.) MEMORY WINDOW VERSUS CYCLING(ENDURANCE) OF P-CHANNEL DSP-MNOST, AND c.) CHARGE RETENTION OF N- AND P-CHANNEL MNOS MEMORY TRANSISTORS.

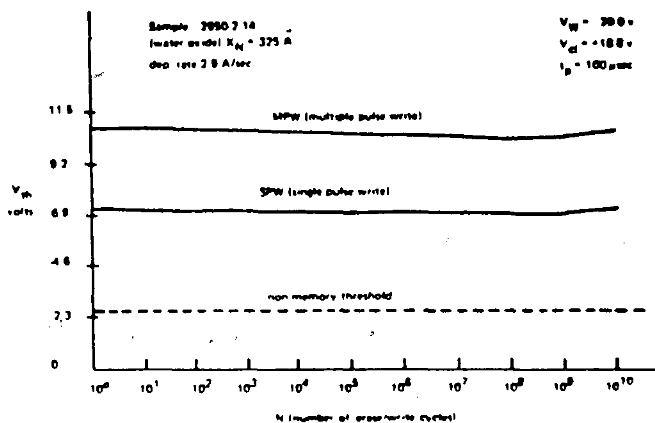


FIGURE 0.3c (REF 12)

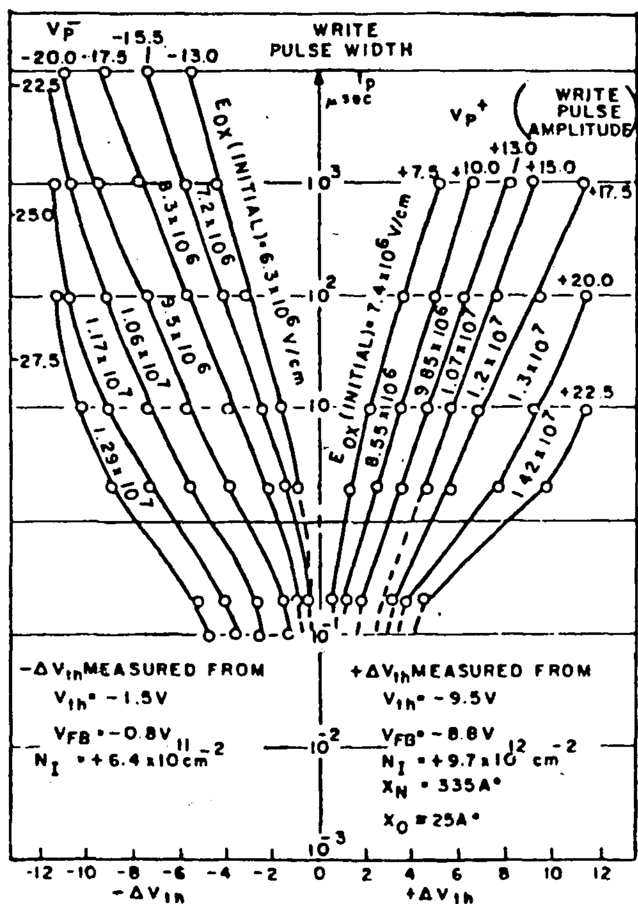


FIGURE 0.3a (REFERENCE 11)

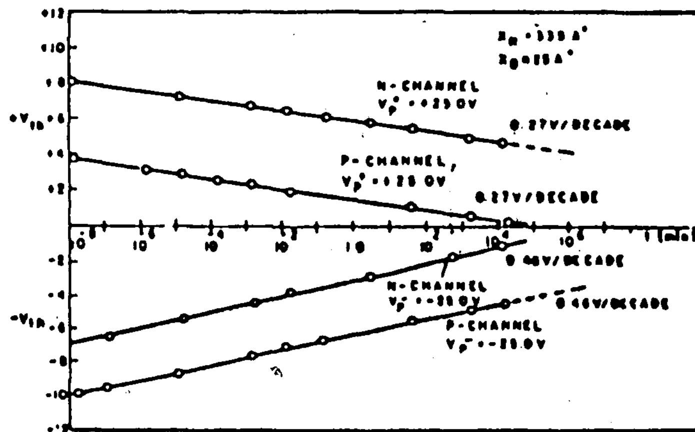


FIGURE 0.3b (REF 11)

TABLE 0.1

SYMBOL	UNITS	DEFINITION
C_G	F/cm^2	Total gate capacitance per unit area
C_{ox}	F/cm^2	Gate oxide capacitance per unit area
C_n	F/cm^2	Gate nitride capacitance per unit area
$\Delta V_{TH(SAT)}$	V	Threshold voltage change at saturation
ΔV_{TH}	V	Threshold voltage change
d_{ox}	cm	Gate oxide thickness
d_n	cm	Gate nitride thickness
E_a	V/cm	Switching field parameter
E_n	V/cm	Gate nitride electric field
E_{ox}	V/cm	Gate oxide electric field
ε	F/cm	Permittivity of free space
ε_{ox}	F/cm	Oxide permittivity
ε_n	F/cm	Nitride permittivity
ϕ_s	V	Surface potential
ϕ_{ms}	V	Contact potential between gate and silicon
I_{ds}	A	Total source-drain current
I_{sd}	A	Total drain-source current
J_n	A/cm^2	Gate nitride current density
J_{ox}	A/cm^2	Gate oxide current density
$J_{ox}(E_{oxo})$	A/cm^2	Gate oxide current density at initial oxide electric field
k_n	V/cm-sec	Nitride constant

SYMBOL	UNITS	DEFINITION
l	cm	Channel length
Q_i	A/cm^2-sec	Charge density in insulator or at its interface with silicon
T	K	Temperature
t	sec	Time
t_e	sec	Erase pulse width
t_p^+	sec	Switching time constant of positive gate voltage pulse
t_p^-	sec	Switching time constant of negative gate voltage pulse
t_{rd}	sec	Read delay time
t_s	sec	Switching time constant
t_r	sec	Read pulse width
t_w	sec	Write pulse width
μ	cm^2/V-sec	Channel mobility
V_d	V	Drain voltage
V_{ds}	V	Drain-source voltage
V_g	V	Gate voltage
V_{GE}	V	Erase pulse amplitude at gate
V_{GR}	V	Read pulse amplitude at gate
V_{GW}	V	Write pulse amplitude at gate
V_{HC}	V	High conductance threshold voltage
V_{LC}	V	Low conductance threshold voltage
V_{oa}^-	V	Op-amp negative voltage supply
V_{oa}^+	V	Op-amp positive voltage supply

SYMBOL	UNITS	DEFINITION
V_s	V	Source voltage
V_t	V	Threshold voltage
w	cm	Channel width

CHAPTER 1

ERASE/WRITE MEASUREMENTS

THEORY OF ERASE/WRITE MEASUREMENTS

The erase/write characteristics, in general, show the change in threshold voltage (V_t) for a given erase/write pulse width (t_e, t_w) and erase/write pulse amplitude (V_{GE}, V_{GW}). After application of an erase/write pulse, such effects as an initial time delay, a region of constant slope, and a final saturation of the threshold voltage is observed (see Figure 1.1). Parameters such as pulse reversal rate, pulse rise time, pulse length, pulse amplitude, absolute values of initial thresholds, reading between pulses, annealing at elevated temperature, presence of light, and temperature are some of the parameters responsible for the threshold shift observed in MNOSTs. These parameters along with the two methods for normalizing procedures in measuring erase/write characteristics will be discussed in this section.

The operation of a P-MNOST is depicted in Figure 1.2 preceded by a typical transfer characteristic curve in Figure 1.1. As the gate voltage is increasingly made more positive with respect to the substrate, the MNOST will progress from flatband condition to accumulation. The result is a net negative charge trapped in the nitride. The process by which the threshold is made more positive is termed erasing.

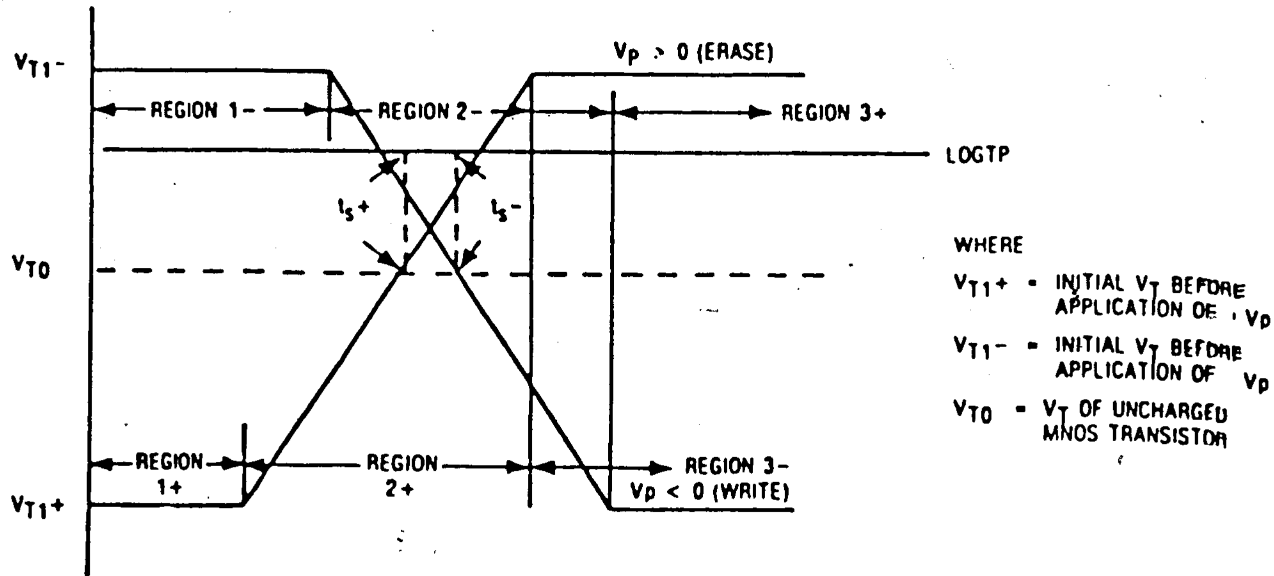
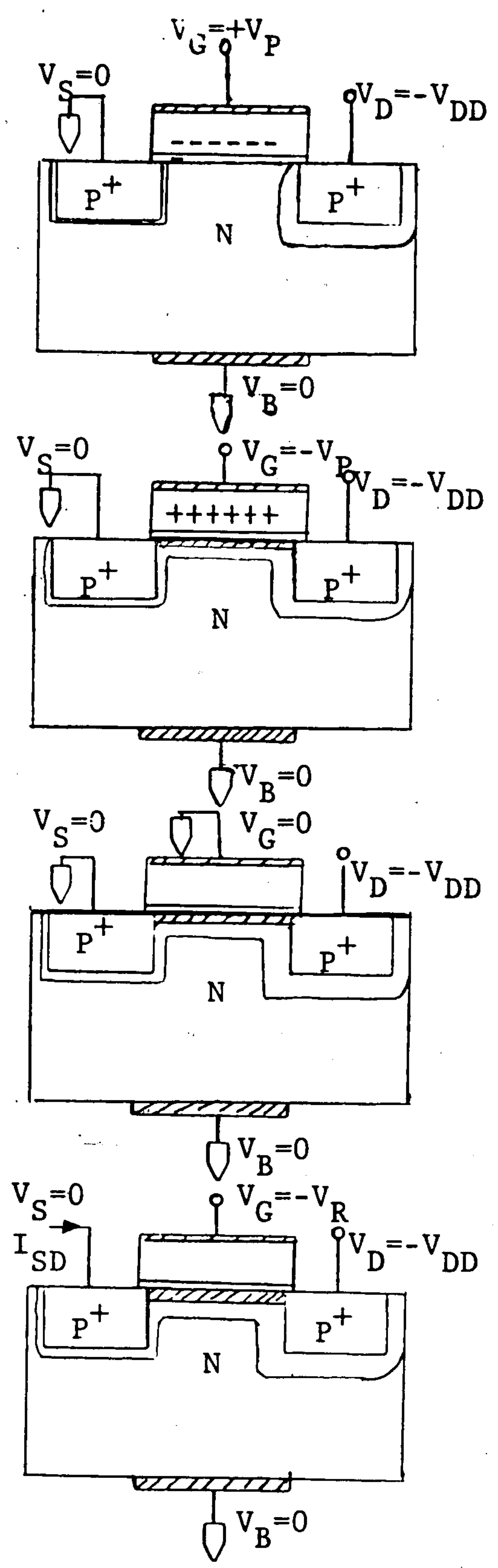


FIGURE 1.1
IDEALIZED SWITCHING CHARACTERISTICS OF MNOS MEMORY TRANSISTORS



ERASE

V_{TH} SHIFTS POS TO HC STATE

WRITE

V_{TH} SHIFTS NEG TO LC STATE

INHIBIT

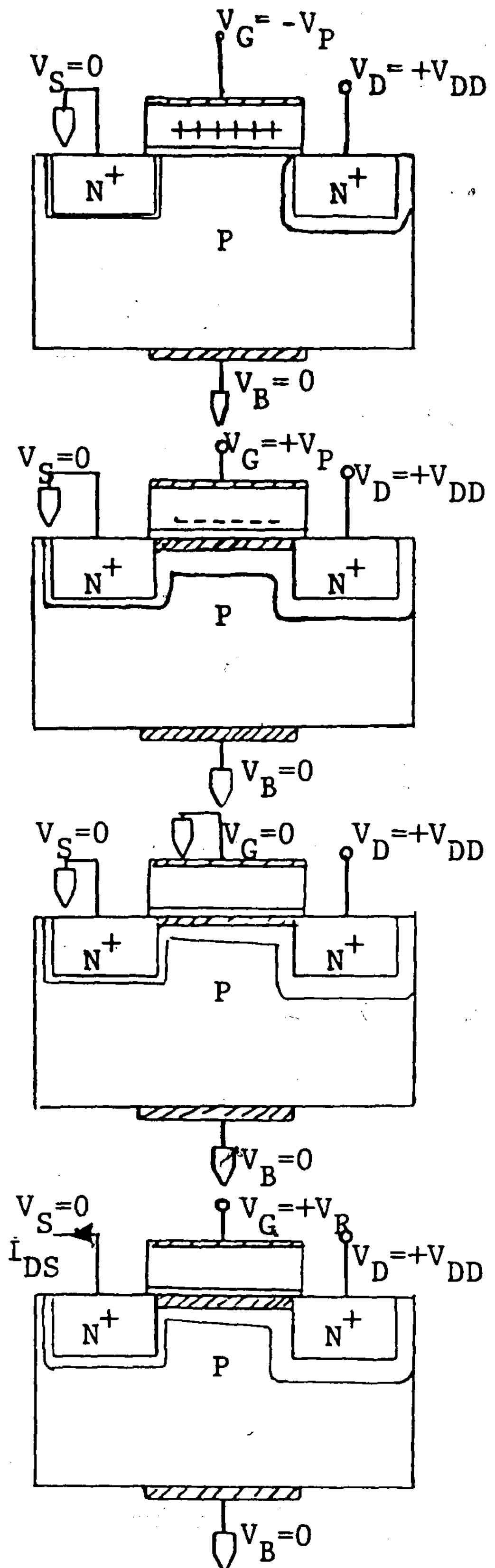
V_{TH} REMAINS THE SAME

READ

$V_T=V_{GS}$ AT $I_{SD}=10$ A

V_{GS} IS MEASURED FOR NDRO

FIGURE 1.2 MODES OF OPERATION FOR P-CHANNEL MNOS MEMORY TRANSISTOR.



ERASE

V_{TH} SHIFTS NEG TO HC STATE

WRITE

V_{TH} SHIFTS POS TO LC STATE

INHIBIT

V_{TH} REMAINS THE SAME

READ

$V_T \doteq V_{GS}$ AT I_{DS}=10 A, V_{GS} IS MEASURED FOR NDRO

FIGURE 1.3 MODES OF OPERATION FOR N-CHANNEL MNOS MEMORY TRANSISTOR.

Writing may be defined as the inverse process. Here an increasingly negative pulse applied to the gate will push the MNOST through depletion into inversion with the resulting threshold being more negative, thereby decreasing the conduction of the transistor. A net positive charge is now trapped in the nitride. A similar operation results for n-channel MNOST (see Figure 1.3). The dependence of the change in threshold (which is proportional to charge trapped in the nitride) as a function of erase/write pulse width and amplitude has been an active study by numerous investigators in the field.[2,4,6,7,9,10,12,13]

Direct-tunneling modes apply only to thin oxide (<50A) devices in which the oxide conduction current is much greater than the nitride conduction current. For the erase/write operations, White and Cricchi treated direct tunneling from a deep monoenergetic donor and acceptor trap at the oxide-nitride interface to the silicon conduction band (writing) and from the silicon valence band to the traps (erasing). They assumed nitride current density and the nitride electric field were independent of time. This is valid for a thin oxide MNOST where $d_n >> d_{ox}$ since the oxide current is considerably larger than the nitride conduction current. This threshold voltage change (see

Appendix E) for a MNOST is

$$\Delta V_t = \frac{d_{ox}}{(1+C_{ox}/C_n)^{-1}} \ln \left[1 + \frac{1-\exp(-t\ k_n/E_a)}{\left(\frac{J_n}{J_{ox}(E_{oxo})-J_n}\right)} \right] \quad (1.1)$$

More helpfully, ΔV_t may be written as

$$\Delta V_t = \frac{2.3\ d_{ox}}{(1+C_{ox}/C_n)^{-1}} \left\{ E_a^{+} \log \left[\frac{J_{ox}(E_{oxo})-J_n}{J_{ox}(E_{ox})} \frac{t_p^{+}}{t_s^{+}} \right] + E_a^{-} \log \left[\frac{J_{ox}(E_{ox})-J_n}{J_{ox}(E_{oxo})} \frac{t_p^{-}}{t_s^{-}} \right] \right\} \quad (1.2)$$

A consideration due to Brunn is that t_s^+ and t_s^- are functions of d_n, and that E_a^+, E_a^-, and C_n are weak functions of d_n. Therefore, there is also some dependence of V_t on variations in the nitride thickness in the MNOST.

The erase/write characteristics of MNOSTs may be divided into three regions as shown in Figure 1.1:

1. An initial region for small values of t_e, t_w, where virtually no shift of V_t is observed (see Eq. (E.15)).
2. V_t is logarithmically dependent on t_e, t_w (Eq. E.19).
3. V_t finally reaching saturation for large values of t_e, t_w (Eq. E.18).

The transition between region 1 and region 2 depends on the initial value of V_t. Compare the two different values (V_{t1}^-, V_{t1}^+) in Figure 1.1.

The slope of the erase/write charging characteristic of region 2 may be written as (see Appendix E)

$$\frac{\delta \Delta V_t}{\delta(\ln t)} = \frac{\varepsilon_{ox} E_a}{C_g} \qquad (1.3)$$

This constant is dependent on the MNOST structure and material properties only. The final transition between region 2 and region 3 depends on the saturation value of V_t which is proportional to V_{GE}, V_{GW}, t_e, t_w and properties of the gate insulator (Eq. (E.18)).

$$\Delta V_{t(sat)} = \frac{d_{ox} E_a}{(1+C_{ox}/C_n)^{-1}} \ln\left[\frac{J_{ox}(E_{oxo})}{J_n}\right] \qquad (1.4)$$

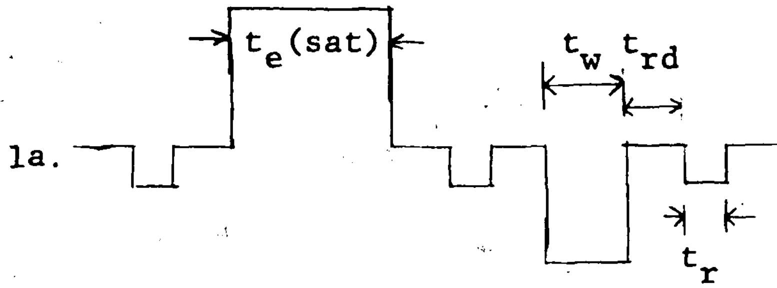
Obviously, from Figure 1.1, the final threshold voltage of the MNOST depends upon the initial threshold voltage state. For this reason it is important to introduce a technique for normalizing the threshold. The two methods for normalizing erase/write measurements are threshold saturation and threshold non-saturation.

Method one, threshold saturation, requires that the MNOST be pulsed into saturation of the opposite

state that characterization measurements are taken. For example, in Figure 1.4 waveform pattern 1a presupposes the user has knowledge of the saturation values $t_{e(sat)}$ and $V_{GE(sat)}$. Once $t_{e(sat)}$ and $V_{GE(sat)}$ are chosen, the user varies only t_w and V_{GW}. In this way, the characteristic relationship between V_t and t_w for each polarity of V_{GW} can be obtained. The result is a write characteristic plot. To generate an erase characteristic plot, the user proceeds in a like manner, but the waveform pattern 1b of Figure 1.4 is chosen. The data is plotted as V_{GW} (if waveform 1a was used) or V_{GE} (if waveform 1b) versus the logarithm of time. This method displays the worst case results between pulsing and V_t change.

The second method, threshold non-saturation, tends to portray a faster behavior: Measurements start with a reproducible intermediate threshold value rather than the saturated threshold value. A major advantage here is no preliminary knowledge of $t_{e(sat)}/t_{w(sat)}$ or $V_{GE(sat)}/V_{GW(sat)}$ is needed. For the write characteristic plot, waveform 2a in Figure 1.5 is used. t_e and V_{GE} are fixed while varying t_w for each polarity of V_{GW}. To generate the erase characteristic plot, waveform 2b is used and t_w and V_{GW} are fixed while varying t_e and V_{GE}. Again, the data is plotted as $V_{GW(2a)}$ or $V_{GE(2b)}$ versus the logarithm of time.

1a.



1b.

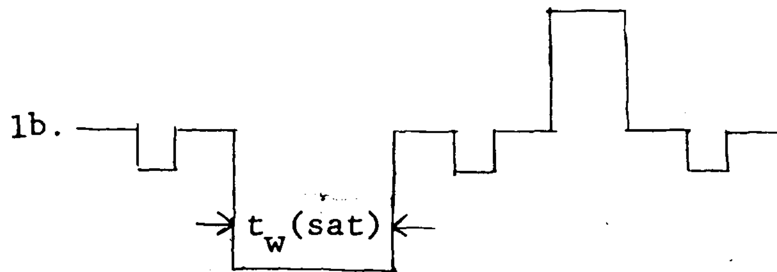
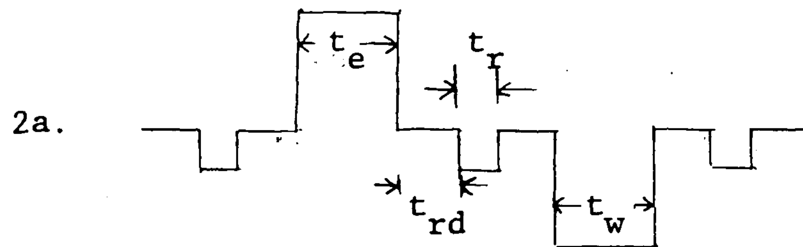


FIGURE 1.4 ERASE/WRITE WAVEFORM PATTERN OF DEVICE #3 FOR a.) WRITE AND b.) ERASE CHARACTERISTIC PLOT USING THRESHOLD SATURATION METHOD.

2a.



2b.

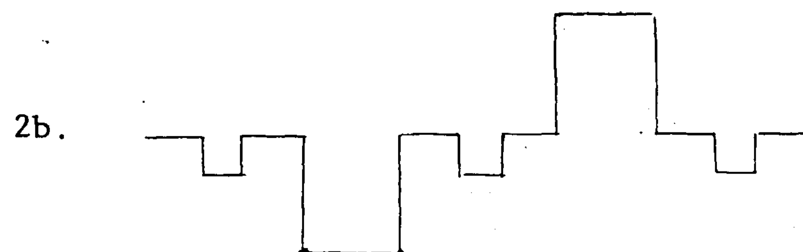
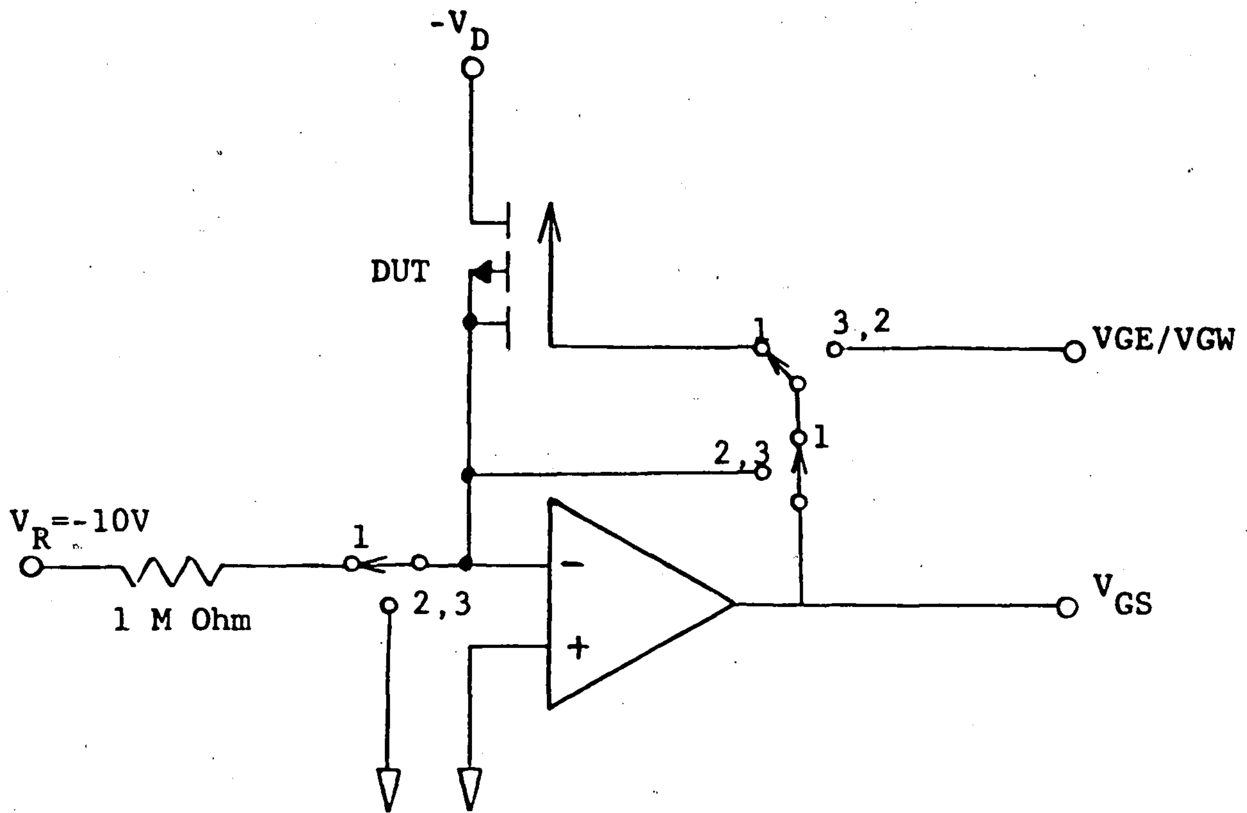


FIGURE 1.5 ERASE/WRITE WAVEFORM PATTERN OPTION FOR a.)WRITE AND b.) ERASE CHARACTERISTIC PLOT USING THRESHOLD NON-SATURATION METHOD.



SWITCH POSITIONS

1 = READ
2 = INHIBIT
3 = ERASE/WRITE

FIGURE 1.6 TOTAL SWITCHING CIRCUIT CONFIGUATION AROUND DUT.

ERASE/WRITE MEASUREMENT PROCEDURE

The erase/write measurement is performed in the characterization laboratory under the control of the HP9836 computer and loaded characterization program, and some peripheral instrumentation (see Figures 0.1 and 1.6). The erase/write MNOST characterization program is documented as Appendix D.

The start of the measurements requires that the DUT (device under test) be biased to the correct level, also the PGB (pulse generator board) be biased with the correct set of voltages as outlined in Appendix B. Once the user has pressed the MEASUREMENT and ERASE/WRITE HP9836 soft keys, and set V_{GE}, t_e, V_{GW}, t_w, t_{rd}, t_r on the PGB, the characterization program will instruct the PGB to generate a waveform pattern as shown in Figure 1.4. A very short time later (15 seconds), the user will EXTRACT and STORE, using a cursor, data points from a waveform displayed on the HP9836 CRT. This waveform, a function of time, will contain data points of value 0v, when the DUT was in the inhibit mode, or V_t when the DUT was being interrogated. This procedure will be performed numerous times: the only difference is possibly V_{GE} and t_e or V_{GW} and t_w must be changed on the PGB to generate a complete erase/write plot. The measurement completes when the user

initiates the EXIT software key in the measurement subroutine.

Preliminary information on the DUT may be helpful, and, depending on which one of the two erase/write methods chosen from the preceding section, may be a must. For example, erase/write method normalized by threshold voltage saturation requires advance knowledge on the HC and LC state thresholds and the V_{GE}/V_{GW} and t_e/t_w values needed to achieve these threshold voltages. Also, t_r is to be less than t_{rd}.

For the first set of erase/write measurements, a P-channel DSP MNOST (device #3) is chosen. The fabrication of this device is dwelled upon in great detail in Appendix C. The memory portion of the transistor has a nitride thickness of 500 A on top of the 25 A memory oxide. The gate electrode is aluminum. A microphotograph of the MNOST along with a dimension scale is given in Plate C.1. From the layout in Plate C.1, the MNOST has a total gate length of 18 μm and a width of 76 μm. The memory gate length is 5 μm.

Erase/write measurements were performed on this MNOST using the threshold voltage saturation (and threshold relaxation--see retention, Chapter 2) method in the LC state. $V_{GE(sat)} = -3.45v$ and $t_e = 1$ ms. Data points were recorded at t_w = .1 μs, 1.8 μs, 10 μs, 100 μs, and

1 ms for seven values of V_{GW} between -7.5v and -22.5v. The MNOST has a cycle history of 1000.

The fits for the curves are especially good and agree well with the analytic switching properties of MNOSTS presented in Appendix E. Using equation (E.17) or (2.1) with d_n = 500 Å, d_{ox} = 20 Å, ε_{ox} = 3.9, ε_n = 6.5, and for V_p = -22.5v with a slope of 4.2V/decade (see Fig. 1.7), the switching field parameter, E_a, is calculated to be 9.7V/cm. From the measurement data plotted in Figure 1.6, three distinct regions are observed for a given V_{GW}: (1) an initial time delay, (2) a region of constant slope, approximately 2.5V/decade, and (3) a saturation value at approximately -14v. Note the straight line voltage cutoff of -3.45v at the LC state because of the non-memory enhancement transistor portion of the DUT. The pulse train values for this MNOST are summarized in Figure 1.1.

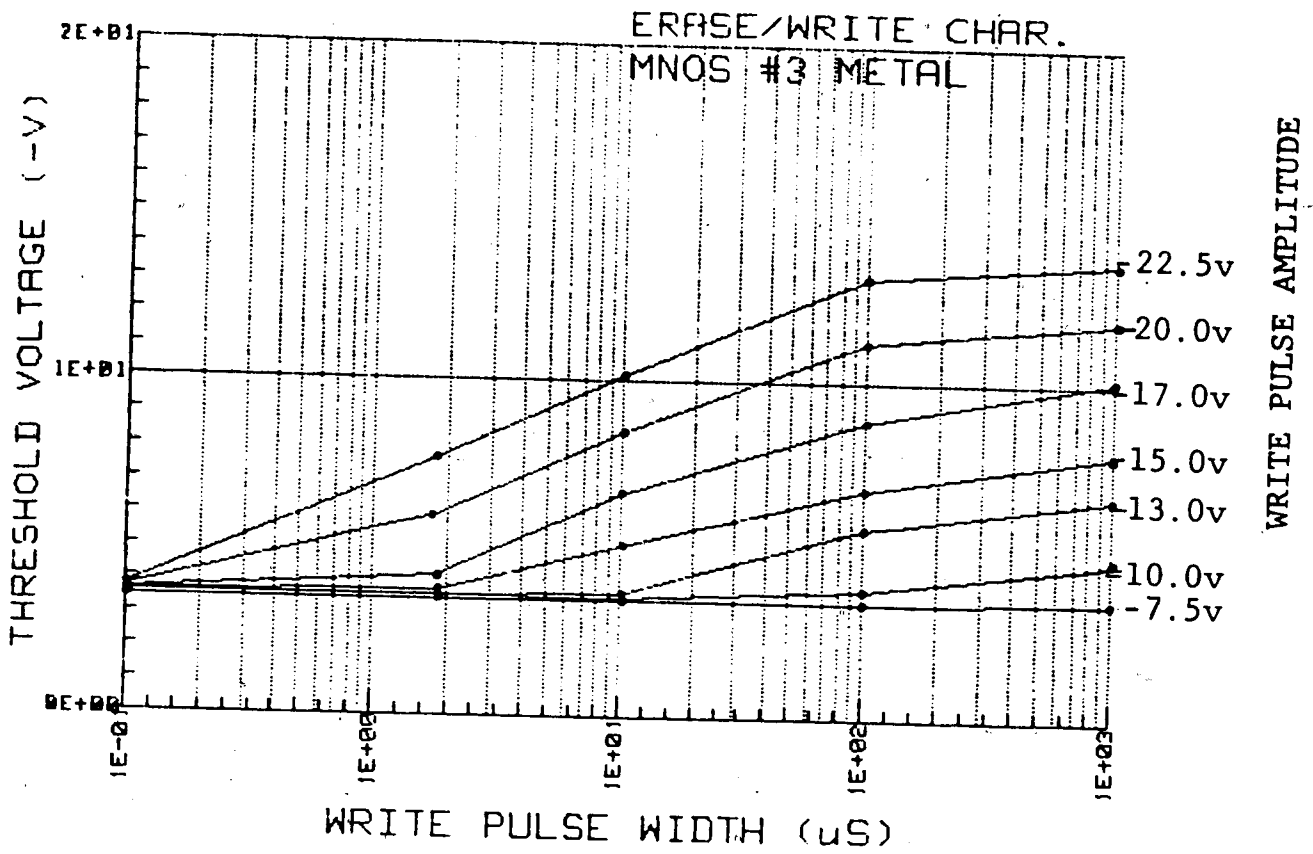


FIGURE 1.7
ERASE/WRITE MEASUREMENT DATA, DEVICE #3.

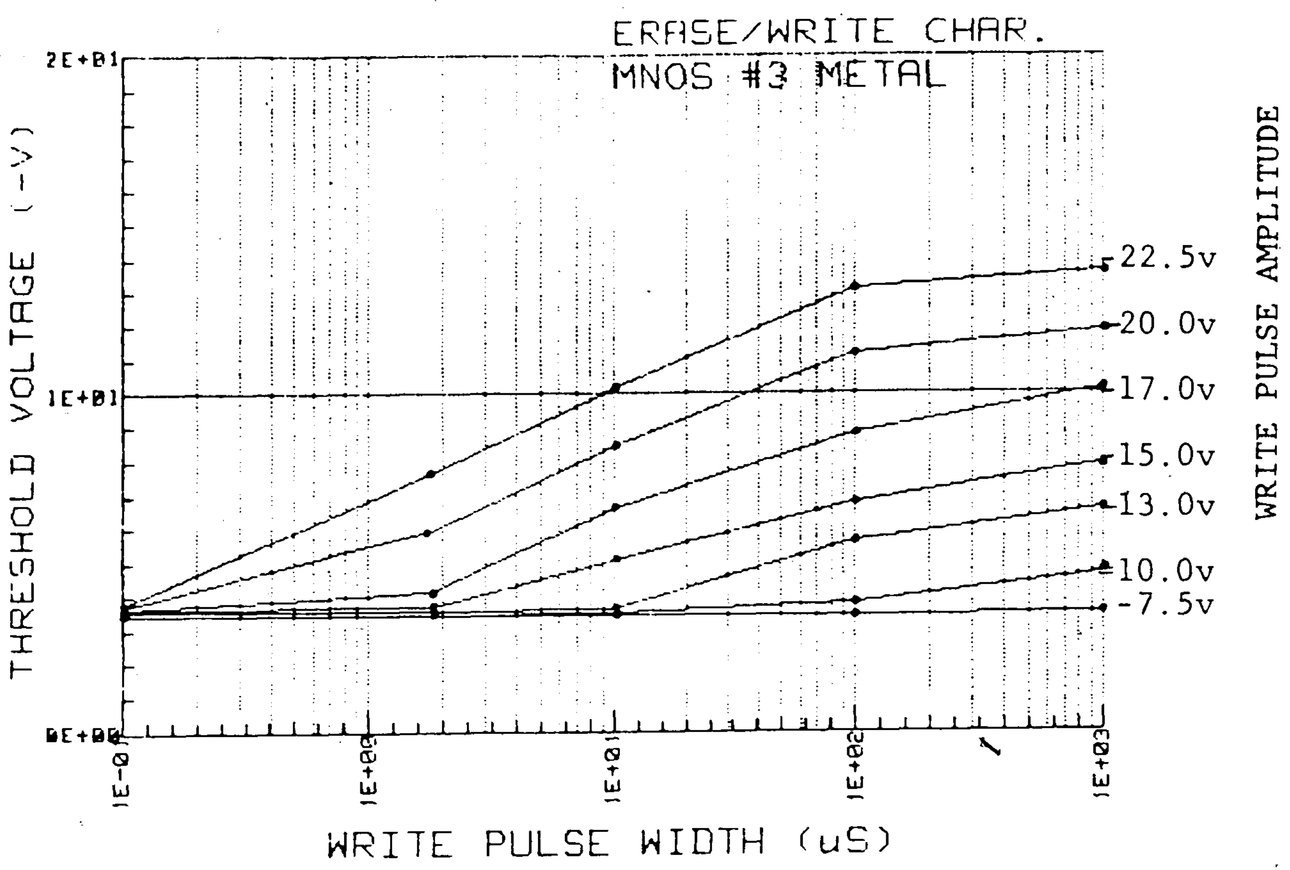


FIGURE 1.7
ERASE/WRITE MEASUREMENT DATA, DEVICE #3.

DISCUSSION OF ERASE/WRITE CHARACTERISTICS

The system setup is a compromise between automatic and manual control. This is due to the nature of the erase-write measurement itself. If V_{GE} and t_e or V_{GW} and t_w are built into the control program, this would detract from the user's flexibility in specifying these parameters. Also, since all MNOSTs do not have the same material properties and dimensions, V_{GE}, V_{GW}, t_e, and t_w may be different. Also, as demonstrated, in some devices such as the DSP MNOST only the writing characteristic is of interest since the erase characteristic is determined by the non-memory portion of the transistor.

Along with the initial setup and calibration described in Appendix B, the measurement data of Figure 1.7 was taken in one afternoon. The amount of data, if taken by conventional techniques, would probably have taken at least a week. This time savings alone, not mentioning the accuracy of the computerized data reading, is an extreme experimental advantage.

CHAPTER 2

RETENTION MEASUREMENTS

THEORY OF RETENTION MEASUREMENTS

Generally speaking, there are two main different types of tests for MNOSTs: A test for writing, reading, and erasing (erase/write characteristics--see Chapter 1), and a test for nonvolatility (retention). Nonvolatility testing is more difficult because retentivity of data stored in MNOSTs can be a fraction of a year to several hundred years. In short, it cannot be measured directly. As will be pointed out in this chapter, there are several methods for recording retention of a MNOST, namely, (1) threshold relaxation, (2) constant drain current, (3) constant gate voltage, and (4) accelerated retention technique. The accelerated retention technique is used in conjunction with any one of the three former techniques mentioned above. A brief background on retention is first presented.

When the MNOST is written into the low conduction (LC) state, the transistor will tend to relax with time toward an intermediate threshold value between the high conduction and low conduction states. The time span that the MNOST can maintain a distinguishable separation between the two states is called retention. To interpret meaningfully retention data, one must record the initial threshold and its decay of either state

(typically specified in volts per decade of time (1.1)) as a function of time. Like the erase/write characteristics, a retention curve may be divided into three regions as shown in Figure E.2.

Region 1 shows virtually no decay of the threshold window (eq. (E.15)); region 2 exhibits a decay of the threshold window logarithmically proportional to time (E.19); region 3 has the most accelerated decay rate of the threshold window (E.18). For thin oxide MNOSTs, region 1 is less than 1μs wide while region 3 starts at very large times, for all practicality, near infinity. The decay rate of region 2 depends on, for the most part, the material properties such as the oxide growth conditions and the silicon-nitride deposition conditions of the gate. However, erase/write pulse amplitude and cycling also alters the material properties of the gate which degrades the ability of the MNOST to retain charge. A reduction of the memory window results. Chapter 3 (endurance) will discuss the above influences of erase/write cycling on the MNOST.

From (E.17), this decay rate may be written as

$$\frac{\partial \Delta V_t}{\partial (\log t)} = \frac{2.3\varepsilon_{ox} E_a}{C_g} \tag{2.1}$$

where

$$E_a = \left. \frac{J_{ox}(E_{ox})}{\frac{\partial J_{ox}}{\partial |E_{ox}|}} \right|_{E_{ox}=E_{oxo}} \tag{2.2}$$

which is a function of the oxide current density exponentially dependent on the oxide field. Because of the exponential dependence on the oxide field, the read voltage used to interrogate the MNOST may actually soft erase the device (read disturb). Hence, retention of a MNOST is influenced by the method of reading out the information.

The first measurement describes the change of threshold voltage with time under zero bias. Because a pulse method is employed to switch the gate from zero bias to the threshold bias only when reading the MNOST, this method will have the lowest read disturb, and, hence, the longest retention time. The pulse train starting pattern is shown in Figure 2.1. Note that the first gate pulse is to achieve a starting reference threshold.

The constant current method is the second method. Here there is always a channel potential, usually $(V_G - V_T) = -2V$, so that a small amount of current may flow through the channel. The result is a constant interrogation. Likewise, the pulse train of Figure 2.1 is used for the constant current method, as well as the next method.

The constant gate voltage method is also in a state of constant interrogation. Since this constant gate

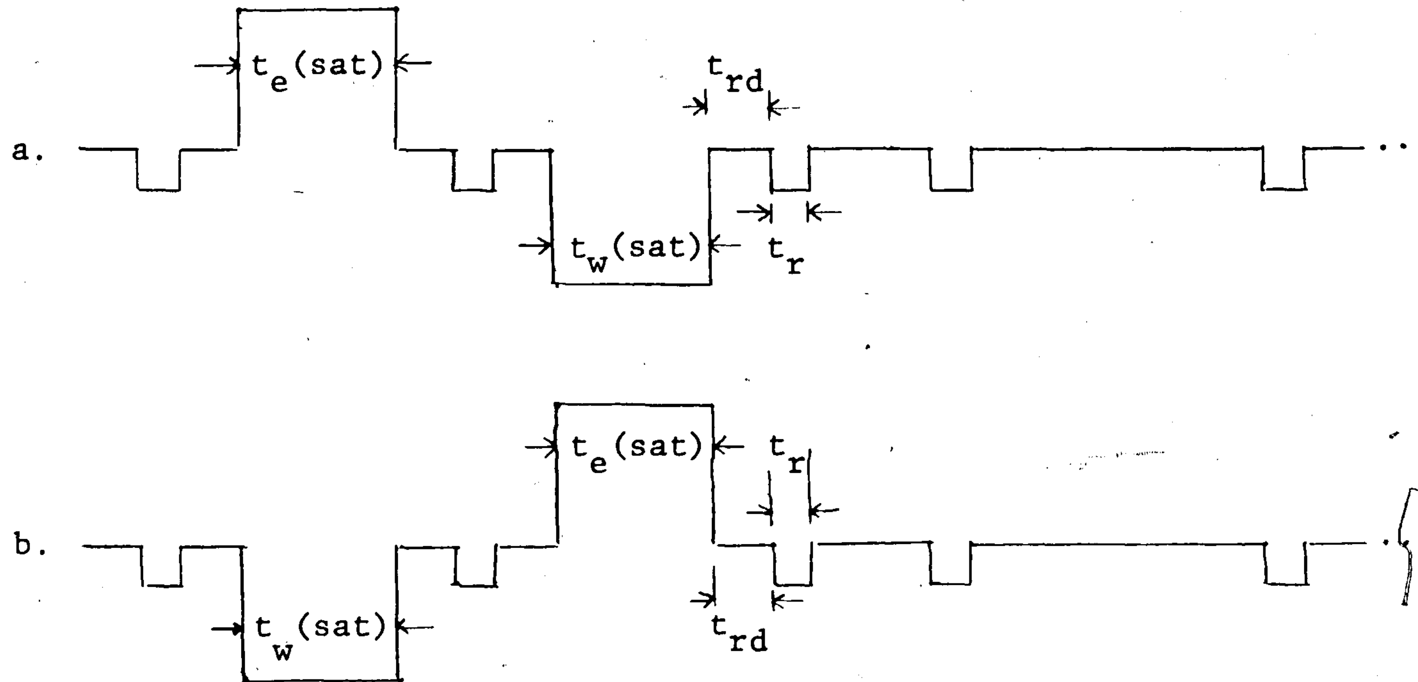


FIGURE 2.1 WAVEFORM PATTERN GENERATED FOR RETENTION STUDIES ON DEVICE #3.

voltage acts as a read disturb condition, this method results in the shortest retention times.

One must choose the method--threshold relaxation, constant current, of constant voltage--that simulates best the future use of that MNOST. However, some MNOSTs exhibit retention on the order of years. This impracticality in lengthy monitoring makes the accelerated method, when used with any of the above methods, a valid approximation. The acceleration method has three approaches.

(1) Approach one is based on the straight line extrapolation of retention measurements taken over hours or days. This is reasonable since (1.1) decays logarithmically with time. The uncertainty is in approximating where region 3 begins.

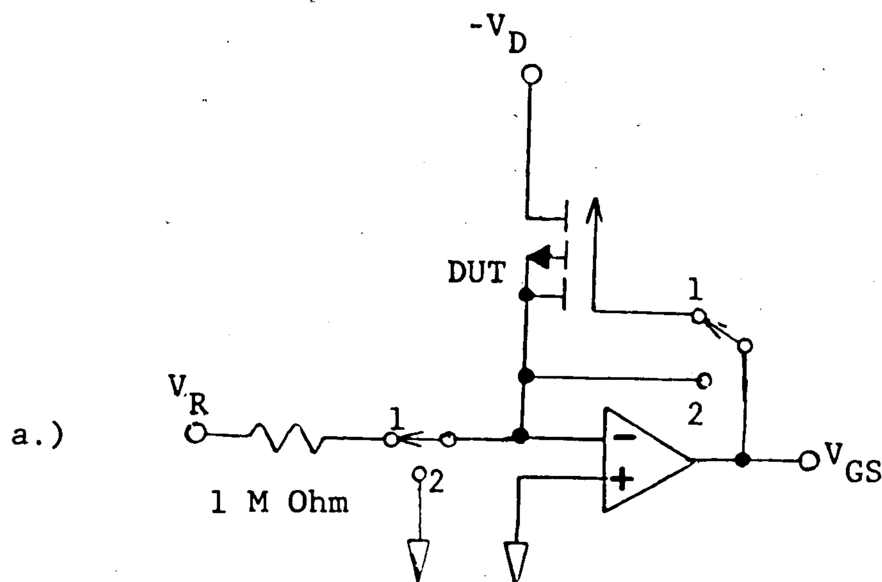
(2) The second approach records retention at elevated temperature. The approximation assumes that the charge lost from the deep traps is due to thermal activation.

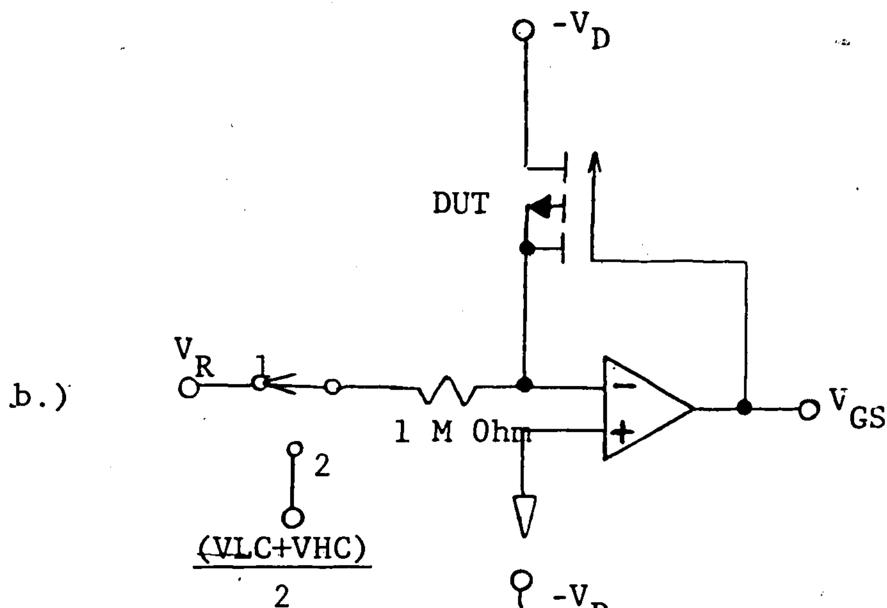
(3) The third approach accelerates threshold decay by increasing the read signal: Method one is pulsed at a larger voltage; method two now has a larger channel potential; and method three has a larger constant gate bias. In essence, the read disturb has been made more severe.

RETENTION MEASUREMENT PROCEDURE

For simplicity, the experimental setup used to perform the retention measurements (shown in Figure 0.1) is identical to the setup used for the erase/write measurements listed in Chapter 1. The only difference is in the selection of the retention subroutine option in the HP9836 control program. The retention MNOST characterization program is documented in Appendix D. Figure 2.2 shows a schematic representation of the electrical equivalence of the circuit configuration around the DUT under the erase, write, read, and inhibit modes when the retention subroutine softkey is pressed.

Once the DUT, PGB, Tektronix 7854 digitizing scope, HP9836 desktop computer, and the peripheral instrumentation is in place as outlined step by step in Appendix B, retention measurements may be started. After the user has set V_{GE}, t_e, V_{GW}, t_w, t_{rd}, t_r on the PGB, the user will press the MEASUREMENT and RETENTION softkeys from the HP9836. Finally, the user enters the time duration of the retention measurements. The HP9836 desktop will automatically take control at this point and the user need not be present. The HP9836 control program will instruct the PGB to generate the waveform in Figure 2.1. While the DUT is interrogated with the PGB waveform, the Tektronix 7854 is instructed by the





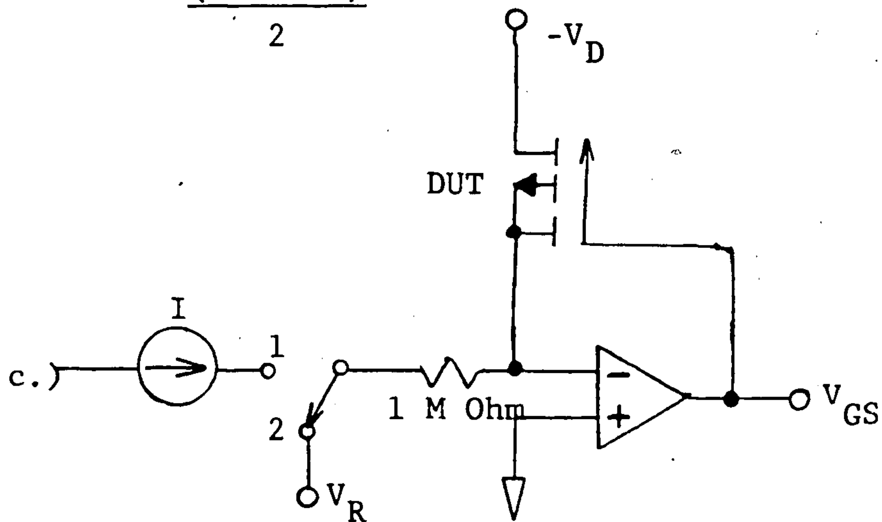
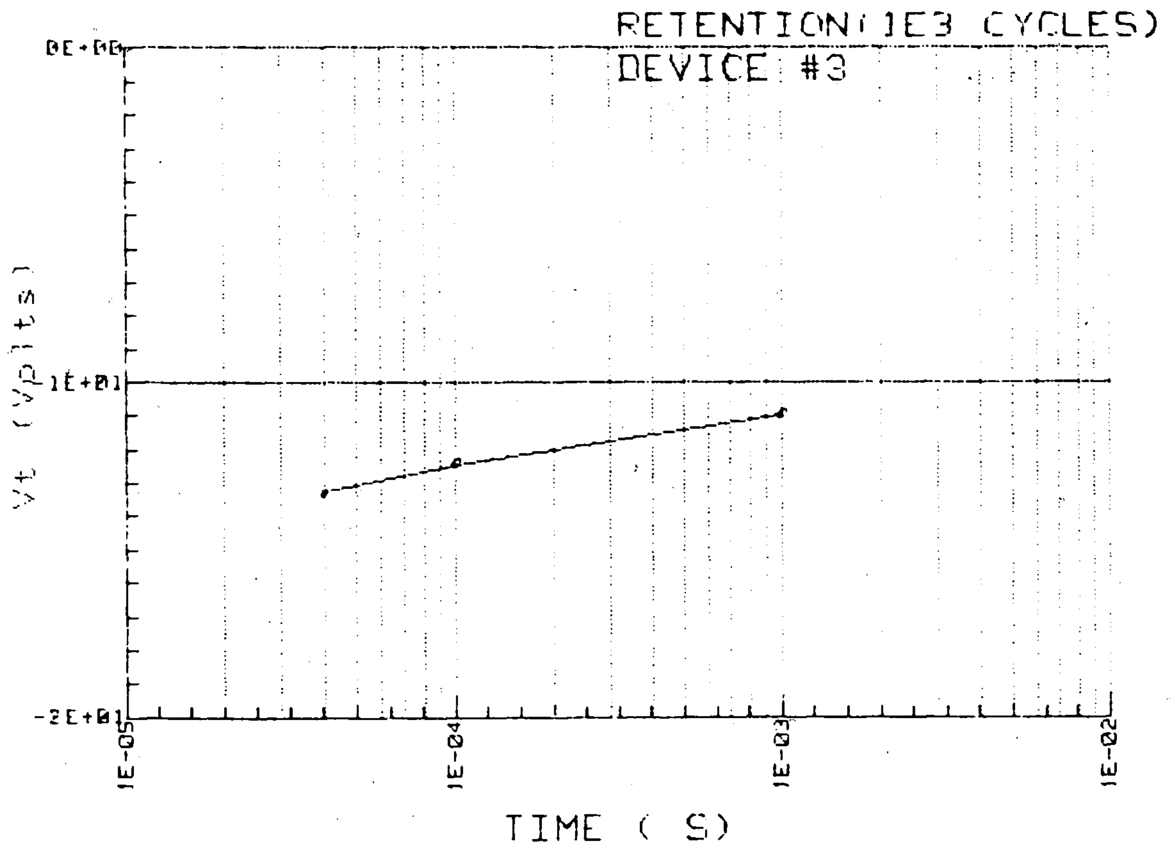


FIGURE 2.2 CIRCUIT CONFIGURATION AROUND DUT UNDER a.) ZERO BIAS, b.) CONSTANT GATE BIAS, and c.) CONSTANT CURRENT BIAS.

HP9836 software program to gather and store the threshold voltage changes logarithmically in time. When time permits, the Tektronix 7854 stored data is sent to the HP 9836. Any time after the time duration of the retention measurements specified by the user, the user will EXTRACT and STORE, using a cursor, data points from a waveform displayed on the HP9836 CRT. The data may be PLOTted or STOREd for future analysis. The measurements commensurate when the user presses the EXIT softkey.

Retention measurements were performed on the identical device as in Chapter 1 of this thesis, the p-channel DSP MNOST (Device #3). The measured log(t) versus V_T plot is shown in Figure 2.3 The drain bias ($-V_{DD}$) was set at -2.0 volts, with V_{GE}=22V, t_e = 1ms, V_{GW} = -22V, t_w = 1ms, t_{rd} = .5μs, and t_r = 8μs. The initial starting threshold voltage is -14V, which is the LC saturation threshold voltage of Device #3. Only the LC threshold shows a decay since the HC threshold is controlled by the non-memory portion of the MNOST. The experiment indicates a threshold window decreasing logarithmically with time at 1.38 dB/decade.

The most important parameter describing the switching speed for a negative pulse (V_{GW} = -22V) is the switching time constant t_s^-, which from equation (E.9) is



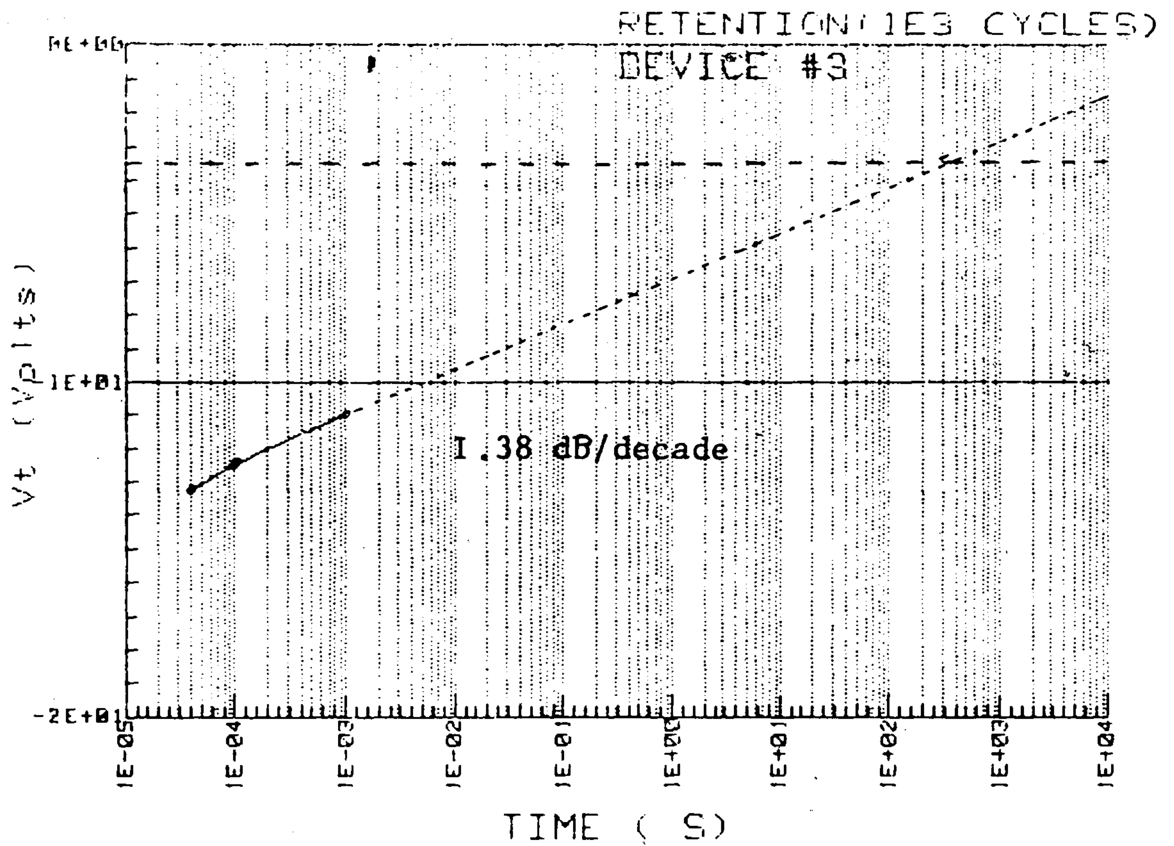
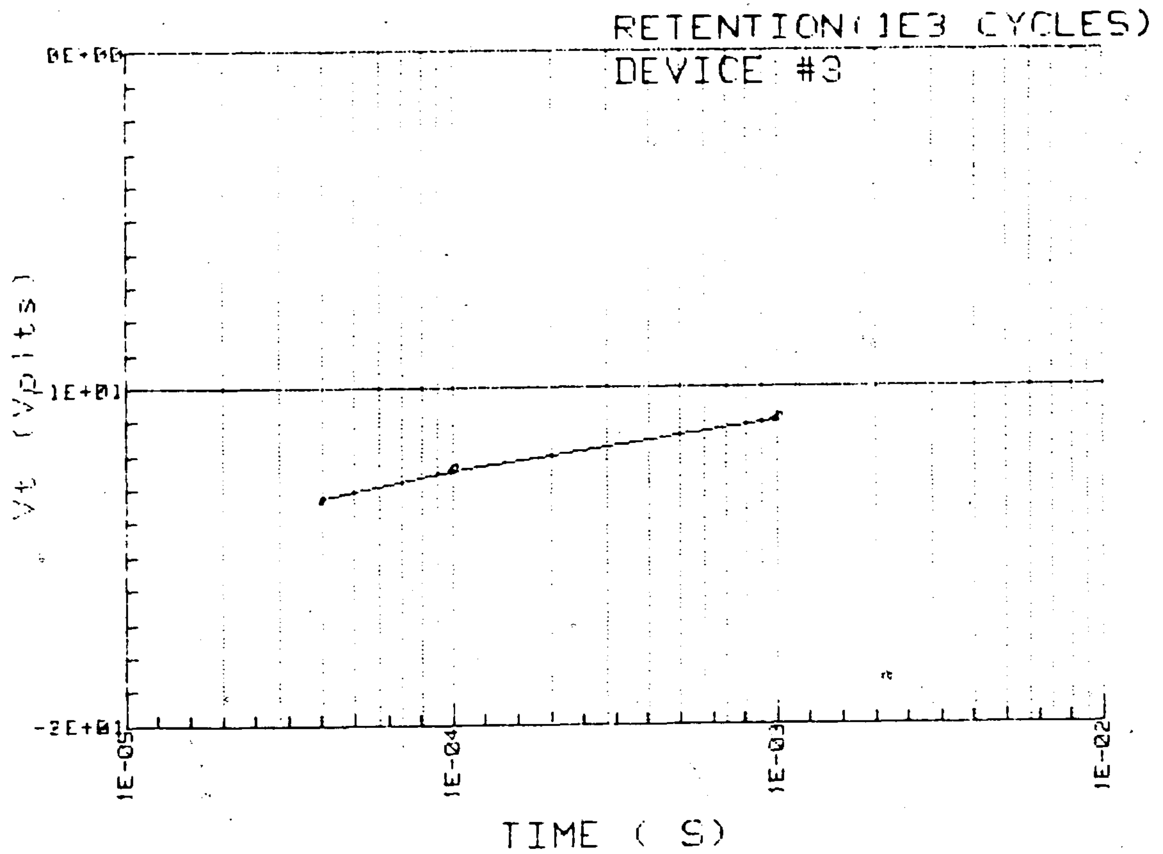


FIGURE 2.3 RETENTION MEASUREMENT DATA AFTER 1E3 CYCLES
(TOP PLOT IS AN ENLARGEMENT)



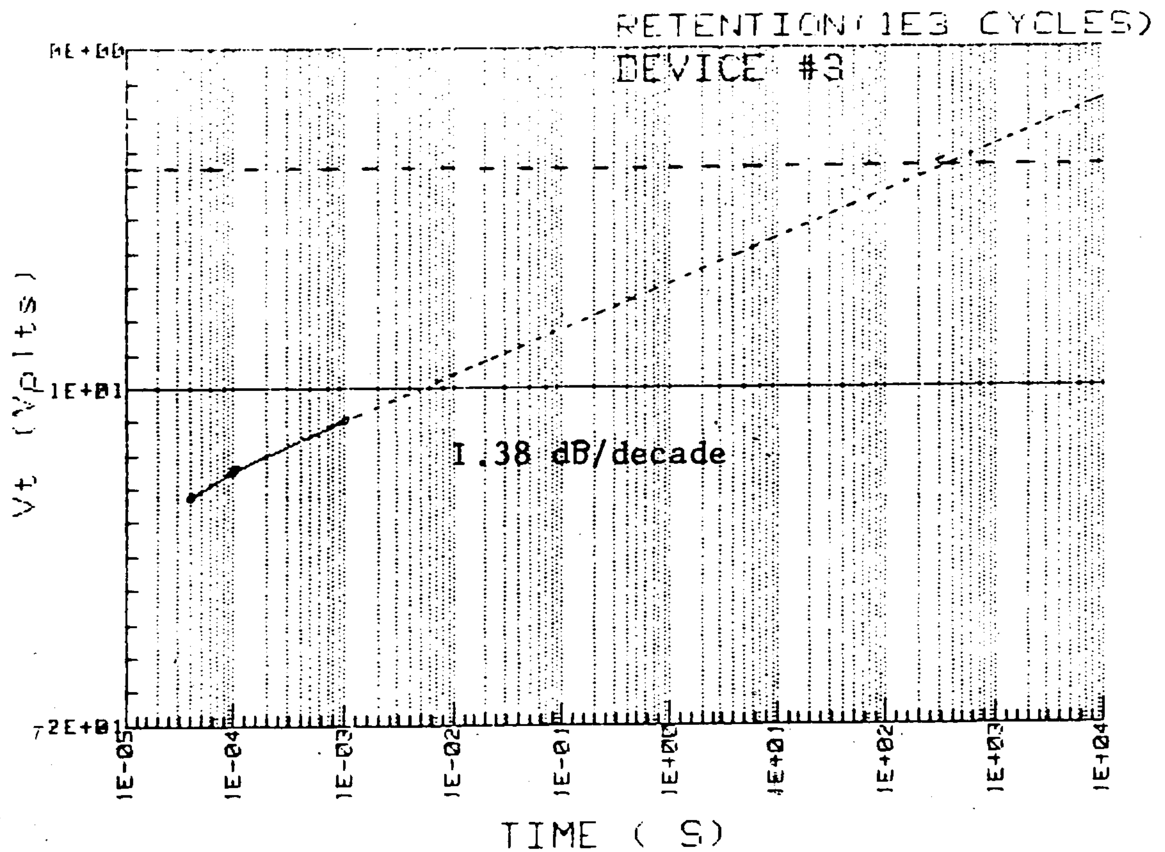


FIGURE 2.3 RETENTION MEASUREMENT DATA AFTER 1E3 CYCLES
(TOP PLOT IS AN ENLARGEMENT)

$$t_s^- = \left(\frac{C_n \varepsilon_{ox}}{C_g}\right) \frac{E_a^-}{J_{ox}(E_{oxo})} \qquad (2.3)$$

or

$$t_s^- = (C_n + C_{ox}) d_{ox} \left[\frac{\partial J_{ox}}{\partial |E_{ox}|}\right]^{-1}_{E_{ox}=E_{oxo}} \qquad (2.4)$$

From Appendix E, the switching time constant is seen to be a function of the oxide field and oxide thickness. For thin oxide devices, t_s^- is small and, hence, the transition point between regions 1 and 2 of the idealized switching characteristics (Figure E.2) may occur sooner. In fact, region 1 of the ideal waveform may be less than t_{rd} and unobservable. This is the case with Device #3, Figure 2.3. Also, region 3 has not been reached for Device #3.

The retention measurements of Device #3 are performed under zero bias (method one, page 25). Because of the limitation encountered in the speed of data transfer between the Tek7854 and the HP9836 (see next section --Retention Measurement Discussion), retention data is recorded only to lms. The straight line extrapolated acceleration technique of the short term data is shown by a dashed line in Figure 2.3 to predict the long-term retention characteristics. Although the logarithmic threshold voltage dependence upon time is evident, region 2 decays quicker than predicted (1.4V/decade). There are two

basic causes for this poor memory window: (1) There may be an increase in the Si-SiO interface-state density and/or an increase in the nitride conductivity caused by cycling in the early portion of the endurance cycle, or (2) there may be a logarithmic decrease some time immediately after lms that is then incorrectly modeled by the application of a straight line extrapolation. In application, the experimenter will decrease the uncertainty in threshold window estimating by the application of a longer retention time to the MNOST.

DISCUSSION OF RETENTION CHARACTERISTICS

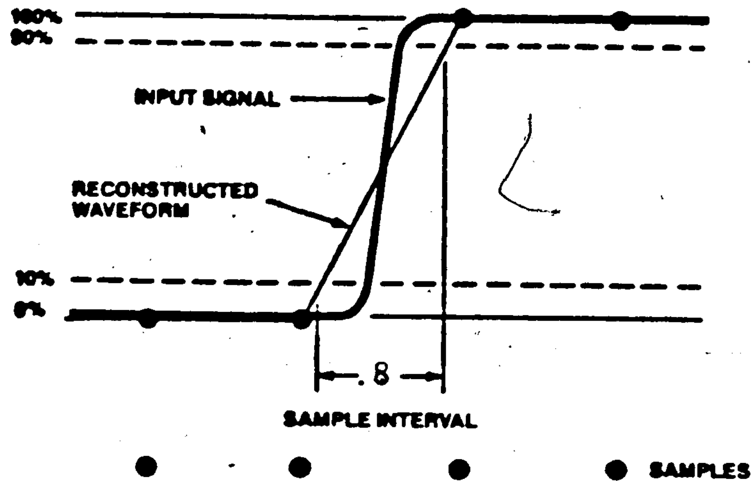
This software program package eliminates human error in recording data points as a function of time. For instance, if a single experimenter is taking data by hand, a read pulse would first be applied. Then the experimenter would look at the readout of the DVM and mark the threshold value and then look at the clock and mark the time. This data taking task is impossible by hand when recording values as a function of time in microseconds, milliseconds, and even seconds. Also, considerable error may result in marking time in minutes.

In contrast, when using the CDCS, the PGB is triggered by some start instruction through the D/A converter from the HP9836. The read pulse pace rate applied to the DUT is set by the PGB to occur logarithmically in time (1μs, 10μs, 100μs, 1ms, etc.). Capabilities of the Tektronix 7854 allow triggering by the read pulse. Hence, the threshold values of the DUT are recorded and at known time values (1μs, 10μs, 100μs, 1ms, etc.). Note that the user need not be present at all after the start instruction.

In the above data collection, the Tektronix 7854 is invaluable in the collection and processing of data. The Tektronix 7854 may not only act as a fast-in slow-out A/D converter, but also as a mathematical pre-

processor of acquired data. As the data is continuously acquired and stored by the scope, averaging, voltage offset subtraction, extrapolation between data points, etc., may be performed in real time on the data. Also, stored data may be loaded from a disk into the HP9836 and sent, by the user's instruction, to the Tektronix 7854 for mathematical massaging. The fitted data is then sent back to the HP9836 for disk storing or plotting. Extrapolation of the short term retention plot of Figure 2.3 is performed in this way.

Although better than by hand recording, limitations in the CDCS retention mode exist. First, the time value is only as accurate as the instrumentation. The Tektronix 7854 is limited to a digitinzing speed of 4μs for each data point in a non-repetitive waveform. This automatically establishes that the read pulse be greater than 4μs since the digitizing frequency is less than 250kHz for pulse interpolating. Note one advantage of pulse interpolating--it makes glitches more visible by connecting every data point and preventing a single dot far from the rest of the waveform from being overlooked. Also, positive rise time errors produced by the pulse interpolator display may be expressed as (see Figure 2.4)



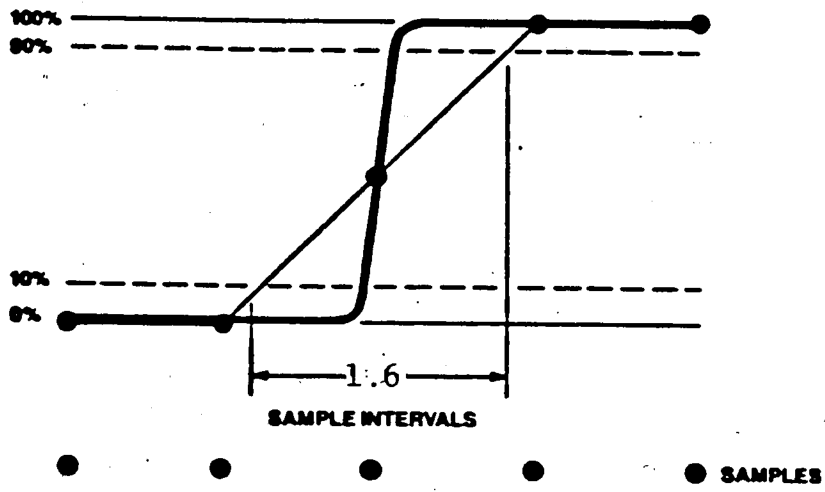


FIGURE 2.4 RISE TIME MEASUREMENT ERRORS. USING THE SAME INPUT STEP IN BOTH DRAWINGS. RISE TIME ERROR MAY BE AS SMALL AS .8 SAMPLE INTERVALS (TOP) TO AS LARGE AS 1.6 SAMPLE INTERVALS (BOTTOM).

$$1/(\text{digitizing freq})\times(.8) = \text{minimum positive rise time} \quad (2.5)$$

and

$$1/(\text{digitizing freq})\times(1.6) = \text{maximum positive rise time} \quad (2.6)$$

Using a maximum digitizing frequency of 250kHz yields a maximum positive rise time of 6.4μs. Therefore, to ensure accurate reading of the amplitude, the read pulse should be greater than 6.4μs.

Second, in the Tek78534 quickest non-repetitive waveform mode, one single-sweep acquired waveform of 512 data words (resolution of 9 bits) takes approximately 2 seconds to store in a Tek7854 memory location or 3 seconds to transfer over the IEEE-488 bus to the HP9836 and dump into a one-dimensional array. One feasible way may include the use of direct memory access (DMA) available to the HP9836 with a plug-in option board to the HP9836. This buffer may be set up using TRANSFER. The most important difference between using a TRANSFER and the regular methods of communication (OUTPUT and ENTER) is that a transfer can take place concurrently with continued program operation.

CHAPTER 3

ENDURANCE MEASUREMENTS

THEORY OF ENDURANCE MEASUREMENTS

A major limitation of MNOSTs are their electrical fatigue or endurance. Endurance is defined as the limit on the number of erase/write cycles that a MNOST may be exposed to before its electrical properties degrade beyond the user's defined limit. This section will briefly discuss the change in three electrical properties observed as the endurance limit is approached: (1) the reduction in the memory window size, (2) the reduction in retention, and (3) the change in the center voltage, $(V_{HC}-V_{LC})/2$. Often, the above three electrical properties will be used for the criteria in endurance measurements. Finally, three endurance techniques will be presented and discussed in this section.

Initially, the short term charge decay rate will be a function of the initial stored charge, $Si\text{-}SiO_2$ interface state density, and the negative exponent of the effective tunneling distance. From Appendix E, for $t \ll t_s$

$$\Delta V_t = \frac{d_{ox} E_a}{(1+C_{ox}/C_n)^{-1}} \ln\left[1 + t\left(\frac{C_g}{C_n \varepsilon_{ox}}\right)\left(\frac{J_{ox}(E_{oxo})-J_n}{E_a}\right)\right] \tag{3.1}$$

As may be deduced, the electrical field in the SiO_2-Si_3N_4 layer must be precisely controlled to prevent premature endurance limitation. The electric field,

with cycling, plays the dominant role in increasing the interface state density, thereby increasing the back-tunneling of charge stored near this SiO_2-Si_3N_4 interface. The result is a decrease in memory retention.

Finally, long term charge decay rate is a function of the nitride current and its variation under prolonged cycling. For $t \gg t_s$ the change in threshold is

$$\Delta V_t = \frac{d_{ox} E_a}{(1+C_{ox}/C_n)^{-1}} \ln \left[\frac{J_{ox}(E_{oxo})}{J_n} \right] \quad (3.2)$$

The first technique is destructive to the MNOST and utilizes the retention criteria. The object is to record retention using one of the three methods described in Chapter 2. The MNOST is cycled a predetermined number of times, usually 10E4 times, and another retention measurement is taken. This pattern is repeated but with increased cycling by a factor of ten from the previous, i.e. 10E4, 10E5, 10E6, etc. The retention plots should reveal a degradation of retention with increased cycling.

The soft erase threshold technique assumes that transistors having a thicker gate nitride will erase slower than thinner nitride transistors for a given pulse amplitude and width. Each MNOST is given a normal write followed by a reduced voltage, shortened

cycle erase. The threshold is measured to determine the shift from the high conductance state to the low conduction state. MNOSTs that have a greater threshold voltage shift (smaller $\Delta V_t = (V_{tHC} - V_{tLC})$) have thinner nitrides and thus lower endurance. As can be seen from (E.9) listed below

$$t_s = \left(\frac{\varepsilon_n \ \varepsilon_{ox}}{d_n \ C_g}\right) \frac{1}{J_{ox}(E_{oxo})} \cdot \left(\frac{\partial \ln J_{ox}}{\partial |E_{ox}|}\right)^{-1}_{E_{ox}=E_{oxo}} \quad (3.3)$$

the MNOSTs with the thicker nitrides will have larger switching time constants to obtain the same change in threshold as their counterparts.

The number of soft erases technique uses the same principle as the soft erase threshold technique above with the noted exceptions. A series of reduced voltage, cycle erase pulses instead of a single erase pulse are applied to the gate to measure nitride thickness variation. After each erase pulse a check is performed to determine if the MNOST has changed from the HC state to the LC state. MNOSTs with the fewest soft erase pulses needed to switch state, erase quicker and indicate a thinner nitride.

In essence, the latter two techniques seem to track nitride thickness. If nitride variation is tightly controlled, other process parameters become dominant in determining erase speed.

ENDURANCE MEASUREMENT PROCEDURE

Once the control program is loaded into the HP9836, the user specifies the endurance measurement subroutine via the soft keys. The endurance measurement subroutine (lines 510 to 850) is outlined in Appendix D. The experimental configuration is given in Figures 0.1 and 3.1. The data presented in Figure 3.2 is recorded via the first technique (destructive, page 45) using zero bias retention. Again for continuity and comparison, Device #3, DSP p-channel MNOST, is used.

The step-by-step outline of Appendix B is used to interface the DUT, PGB, Tektronix 7854 digitizing scope, HP9836 desktop computer, and the peripheral instrumentation. For the data in Figure 3.2, the endurance cycling pulse train of Figure 3.3 is used with V_{GE} = +22V, t_e = 1ms, V_{GW} = -22V, t_w = 1ms, t_{rd} = .5μs, and t_r = 8μs. The rise and fall times of the previous pulses are 200ns. At the HP9836 terminal, the softkey "ENDURANCE" is pressed. The HP9836 terminal displays "NUMBER OF CYCLES" and "10" was entered. At this point automation starts. The cycling pulse train set above is applied to Device #3. The first, second, fifth, and seventh output waveform (V_{GS}) for each decade (1, 10, 100, etc.) of cycling is captured by the Tektronix 7854 and sent to the HP9836 computer. For 10E4 cycles, measurement collection required approximately one hour.

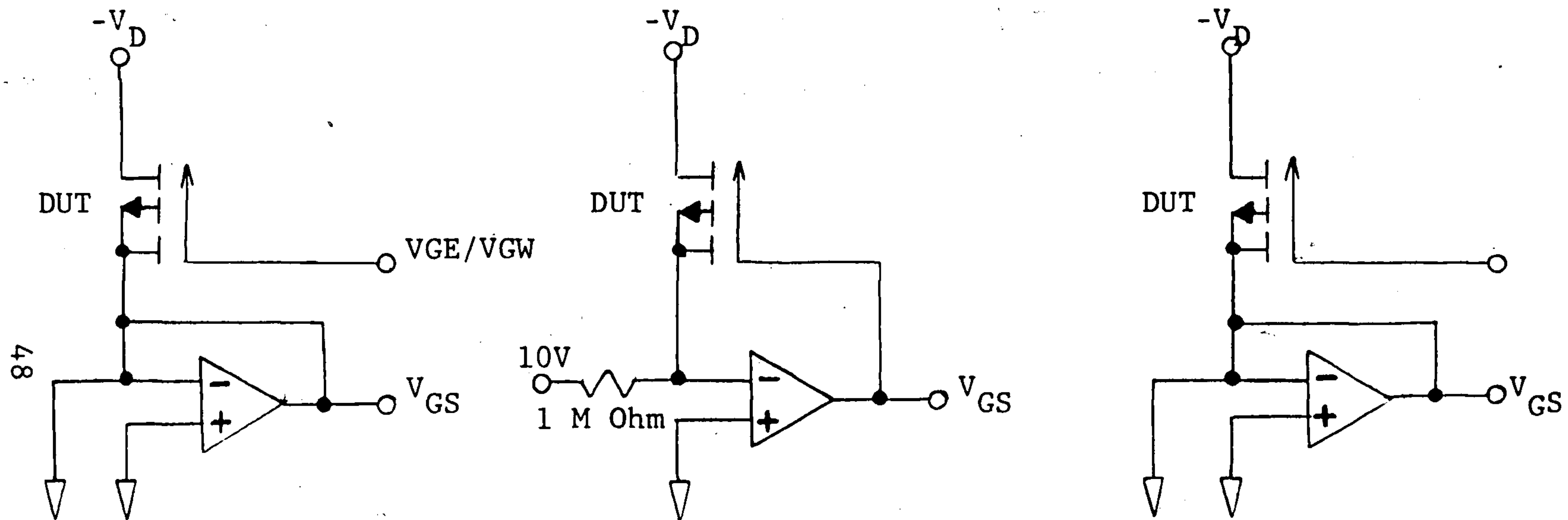


FIGURE 3.1 CIRCUIT CONFIGURATION AROUND DUT UNDER a.) WRITE/ERASE, b.) READ, AND c.) INHIBIT.

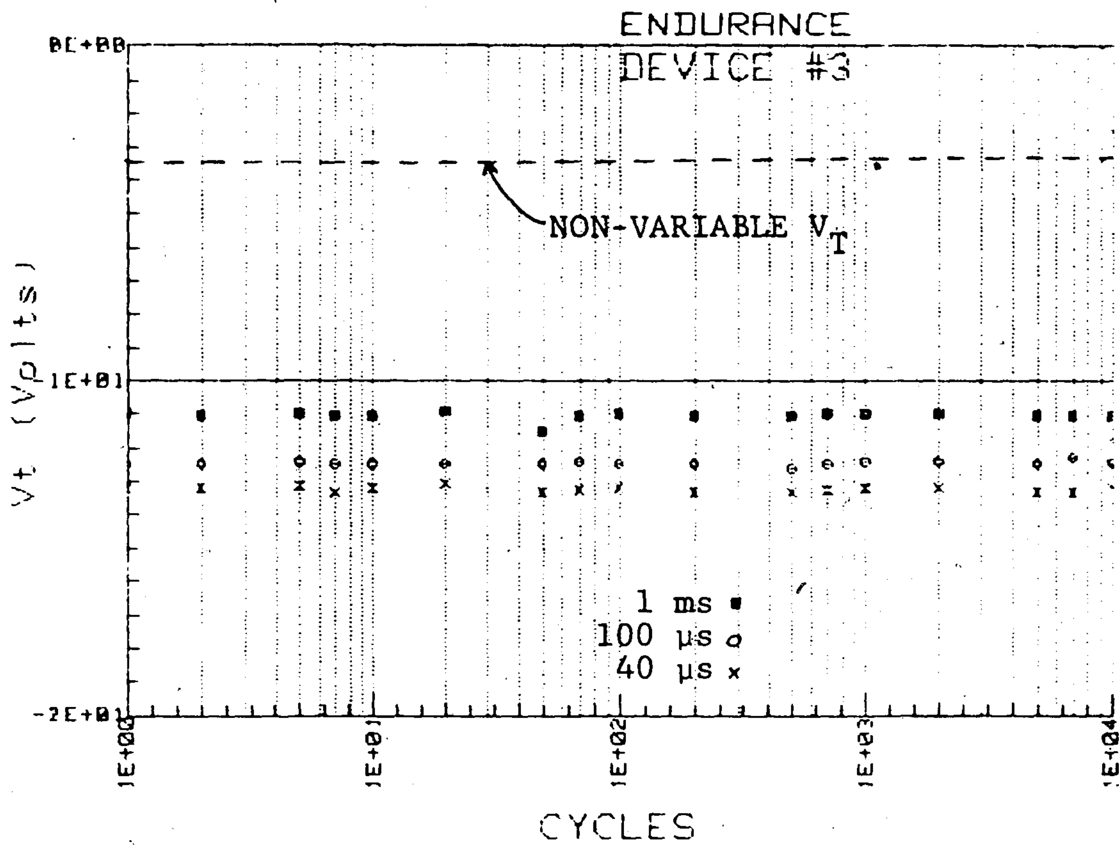


FIGURE 3.2 ENDURANCE MEASUREMENT DATA UPTO 1E4 CYCLES.

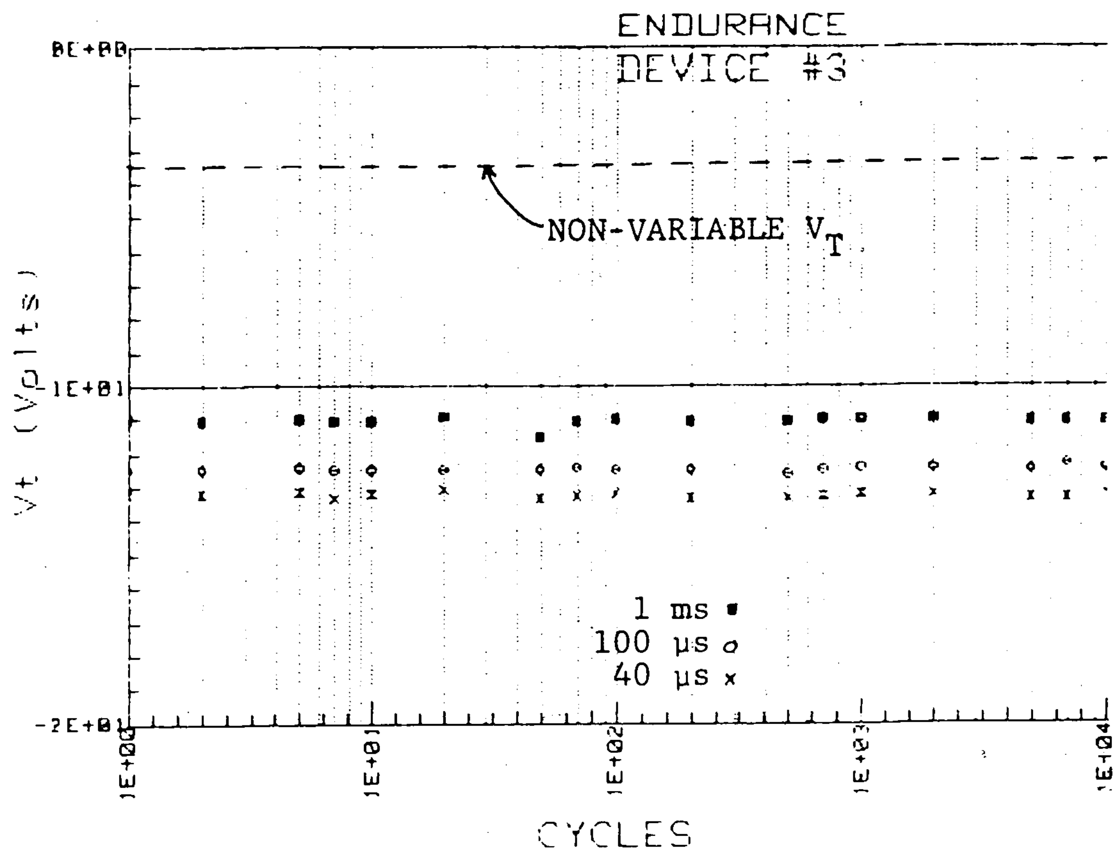


FIGURE 3.2 ENDURANCE MEASUREMENT DATA UPTO 1E4 CYCLES.

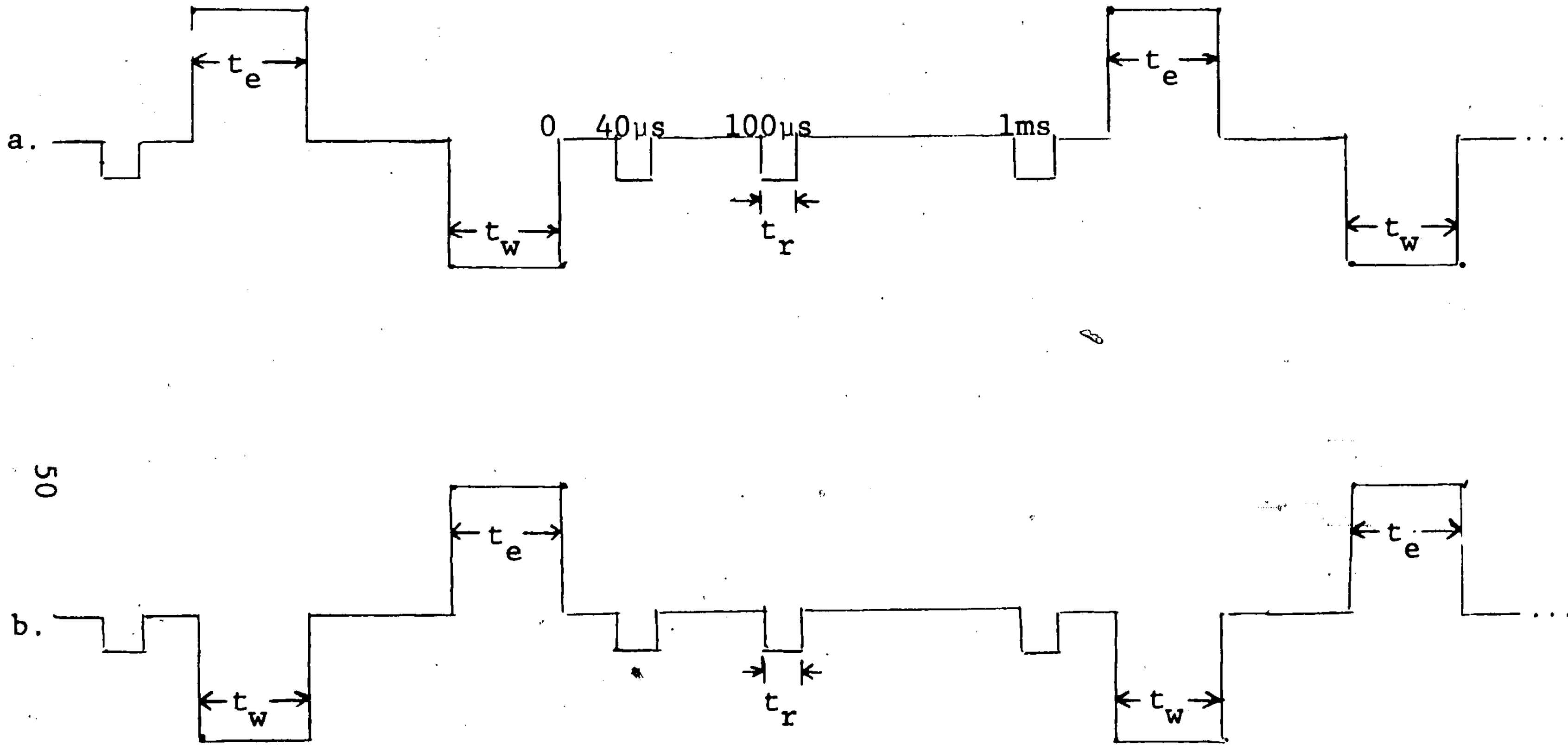
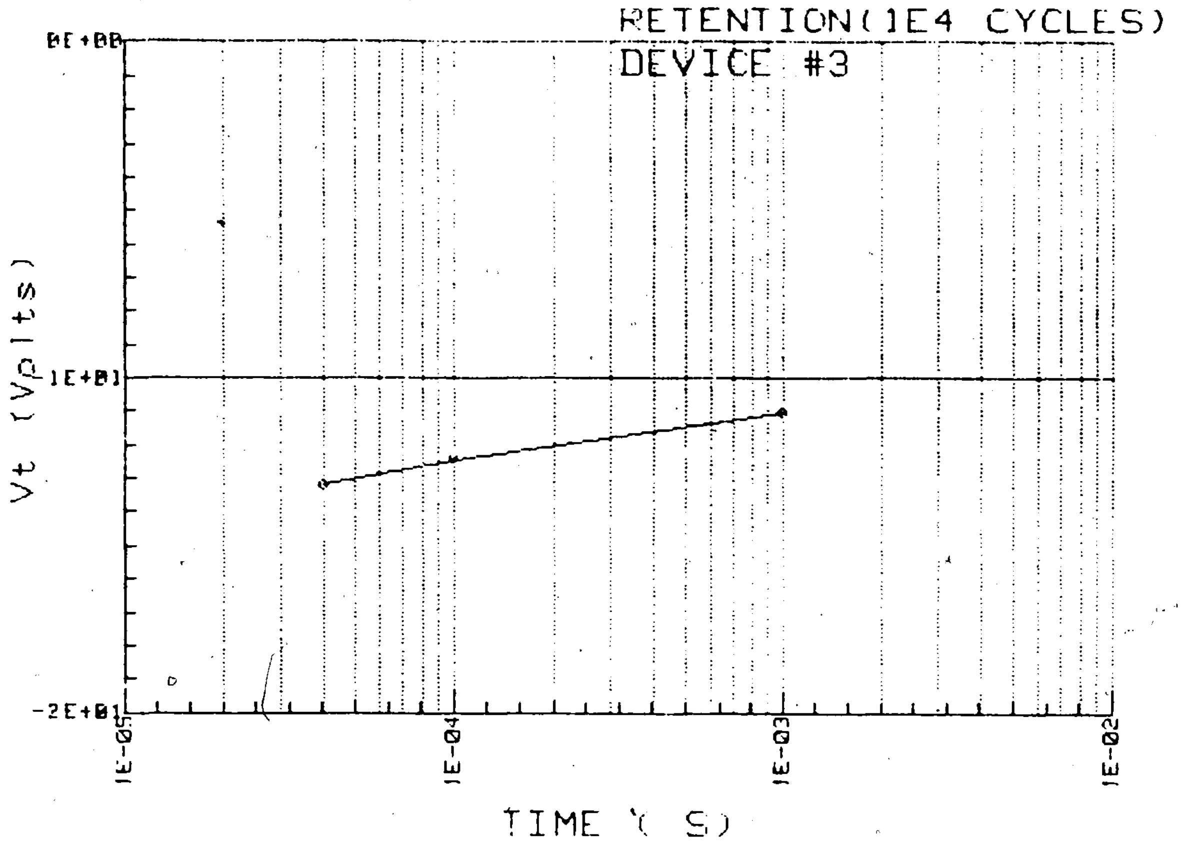


FIGURE 3.3 ACTUAL ENDURANCE PULSE TRAIN FOR DEVICE #3. THRESHOLD VOLTAGE RECORDING DONE FOR a.) LOW CONDUCTION- AND b.) HIGH CONDUCTION STATE.

Next, the user returned to the HP9836 computer to press the "EXTRACTION" softkey. Using the cursor displayed on the screen, the user extracted the threshold voltage values from the output waveforms. Upon completion, the "PLOT" softkey was pressed. The cycled number values of 1, 2, 5, 7, 10, 20, 50, 70, 100, etc., to 1000 were entered consecutively paired with the extraction threshold voltage values. This satisfies the two-dimensioned array in the plot subroutine (threshold voltage value, number of cycles) = (x,y)). The plot generated is shown in Figure 3.4.

For a comparison with the data in Figure 2.3, the zero biased retention measurement was performed after 10E4 cycles. The softkeys "END," "MEASURE," and "RETENTION" were consecutively pressed. 20 is entered via the HP9836 terminal after "NUMBER OF POINTS" is displayed on the screen. The HP9836 control program will instruct the PGB to generate the retention waveform in Figure 2.1. See Chapter 2.2 for retention procedure. After 56 hours, the experimenter returned to press the "EXTRACT" and "PLOT" softkeys. The threshold



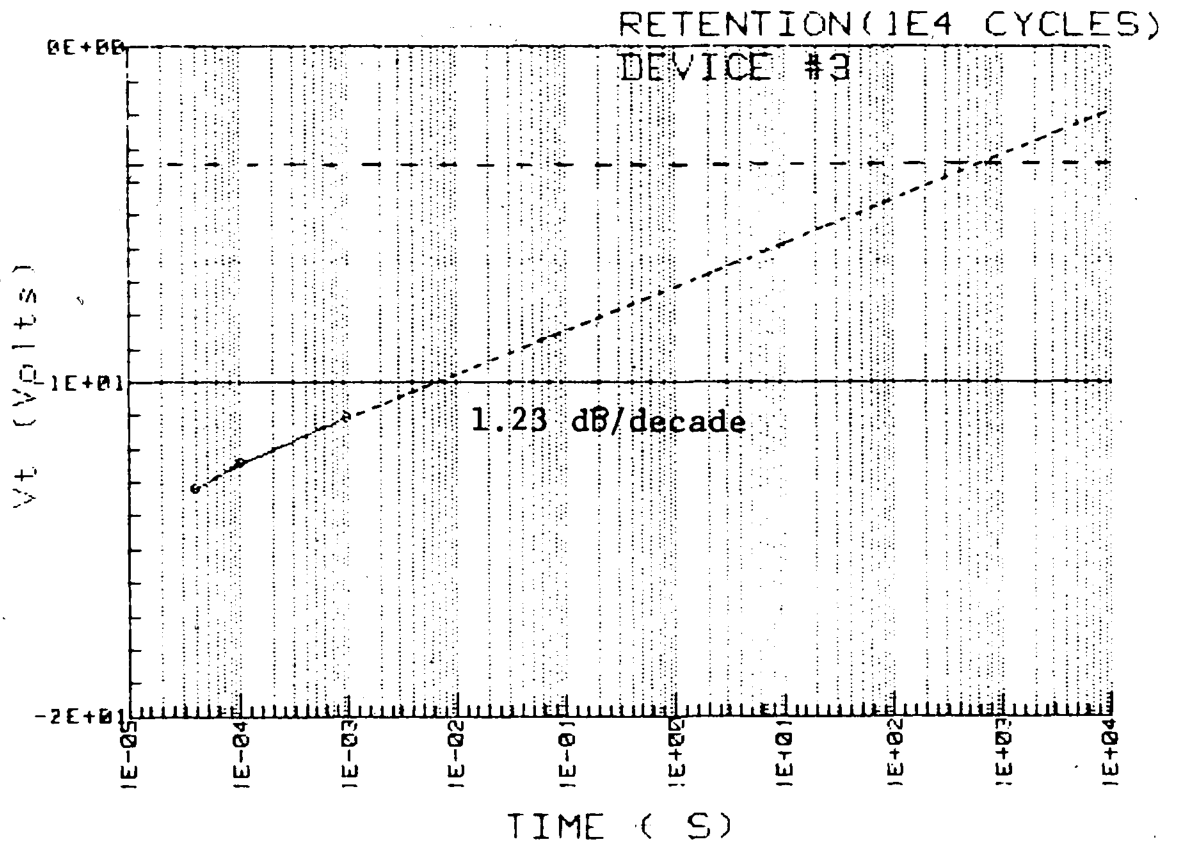
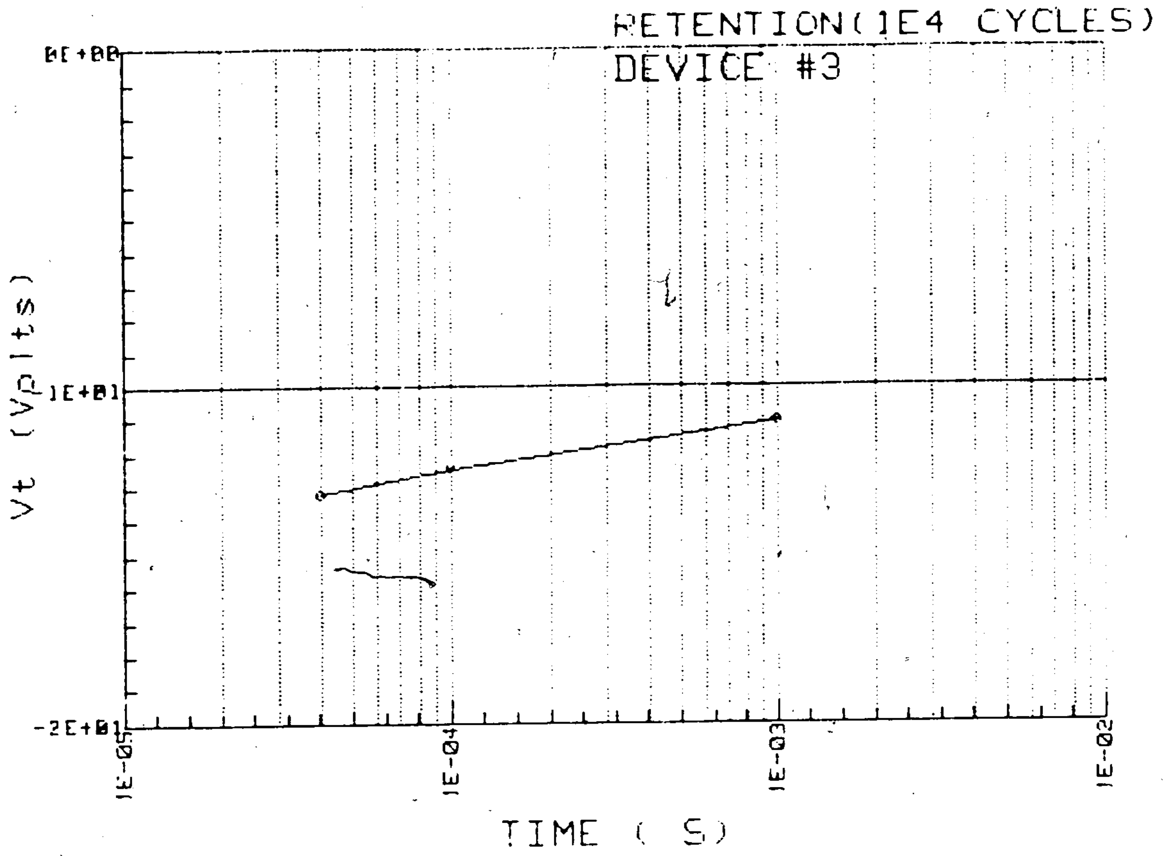


FIGURE 3.4 RETENTION MEASUREMENT DATA AFTER 1E4 CYCLES (TOP PLOT IS AN ENLARGEMENT)



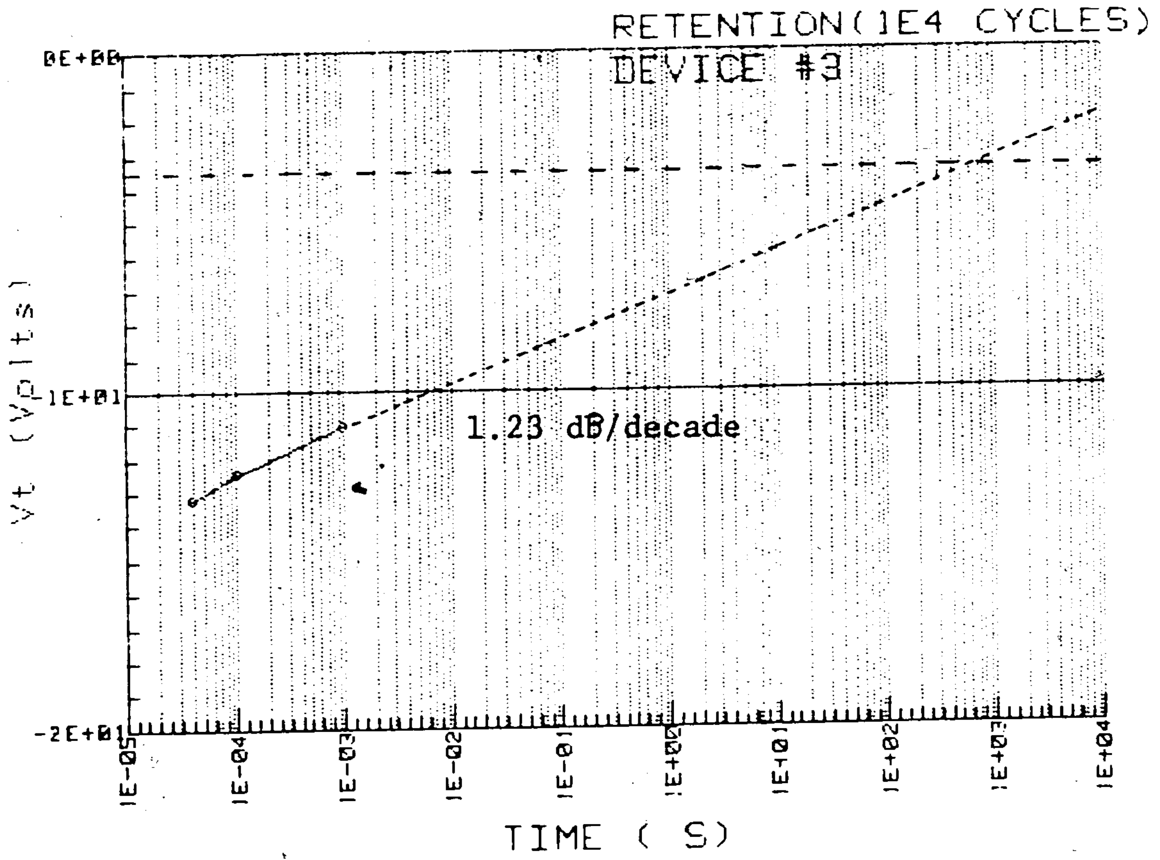


FIGURE 3.4 RETENTION MEASUREMENT DATA AFTER 1E4 CYCLES (TOP PLOT IS AN ENLARGEMENT)

voltage change versus the logarithm of time is plotted in Figure 3.4. The "LOAD" and "PLOT" softkey combination makes displaying more than one curve possible.

The above procedure for Device #3 was repeated for 10E5 cycles, followed by another zero bias retention measurement. Plots of the number of cycles versus threshold voltage and logarithm of time versus threshold voltage are given in Figures 3.5 and 3.6, respectively. The endurance experiments indicate a narrowing of the threshold voltage window (V_t/decade) with increased cycling. Also, reduction in retention as well as a change in the center voltage $(V_{HC}-V_{LC})/2$ is observed. Other researchers have observed similar effects. A possible explanation for the decrease in retentivity with cycling includes the increase in surface state and/or an increase in the nitride conductivity.

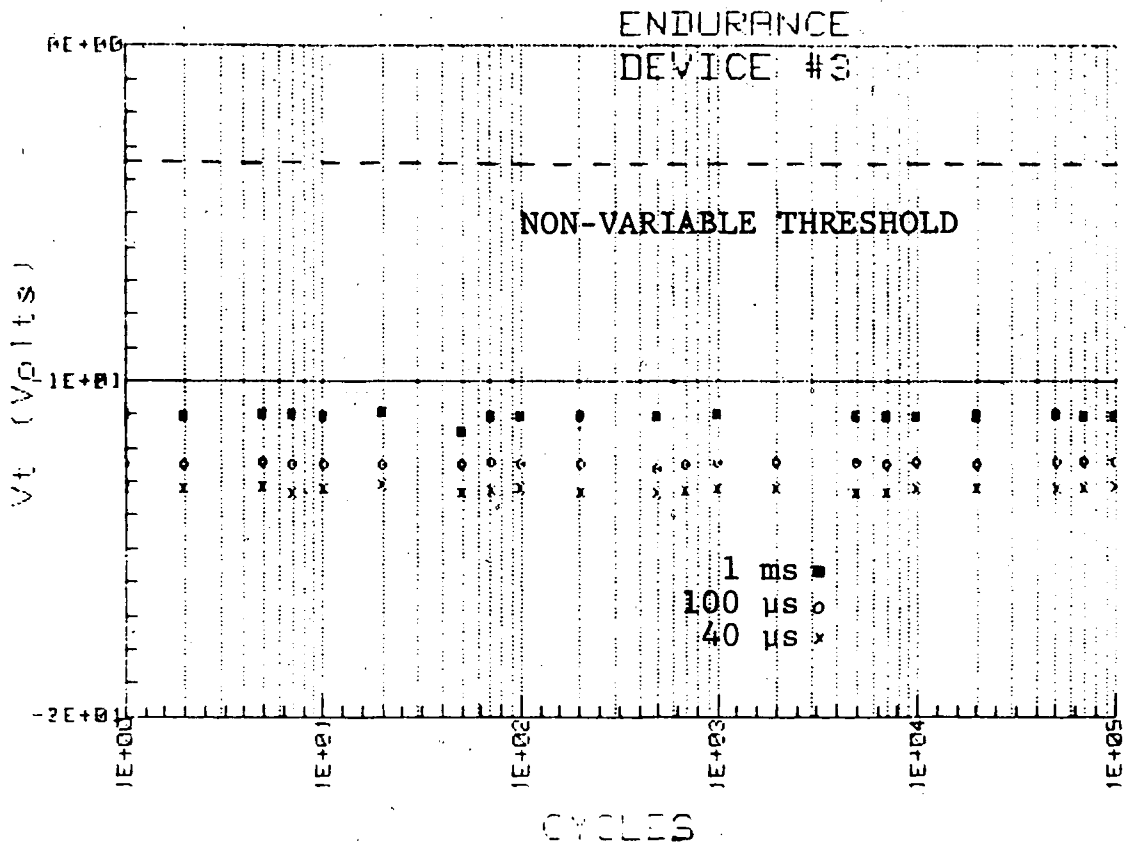


FIGURE 3.5 ENDURANCE MEASUREMENT DATA UPTP 1E5 CYCLES

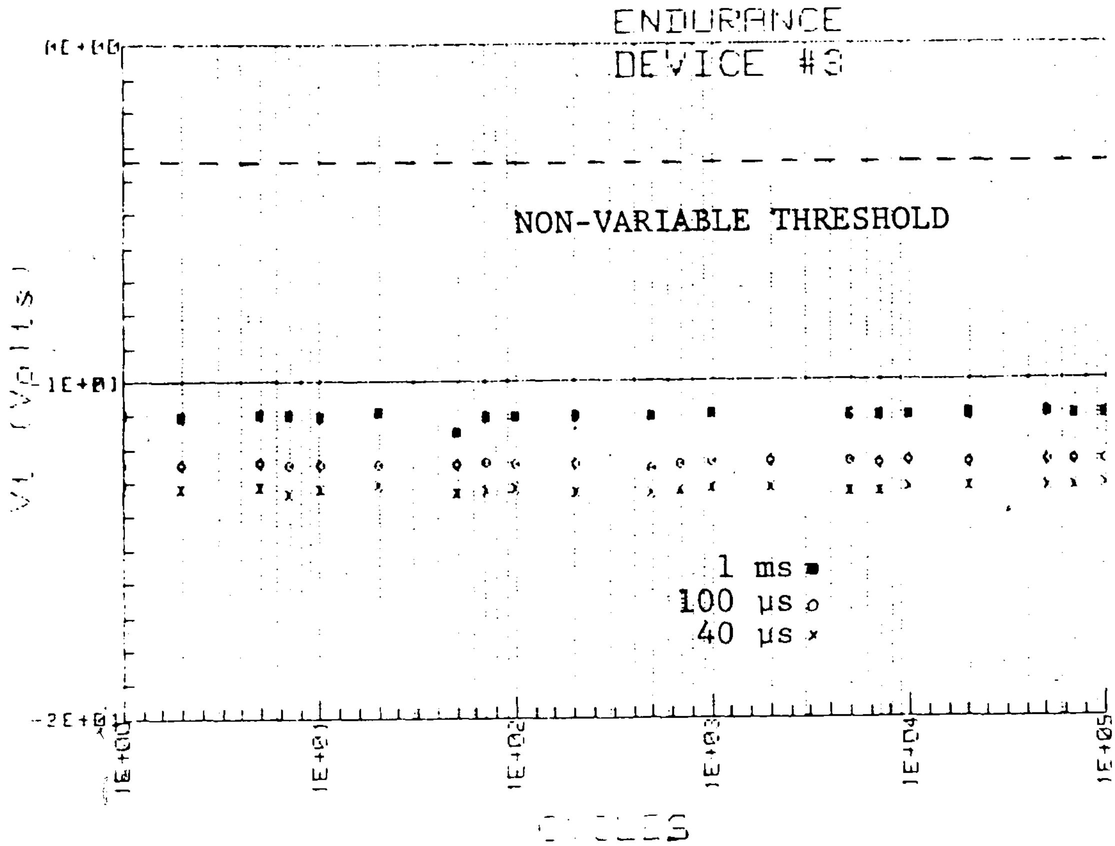
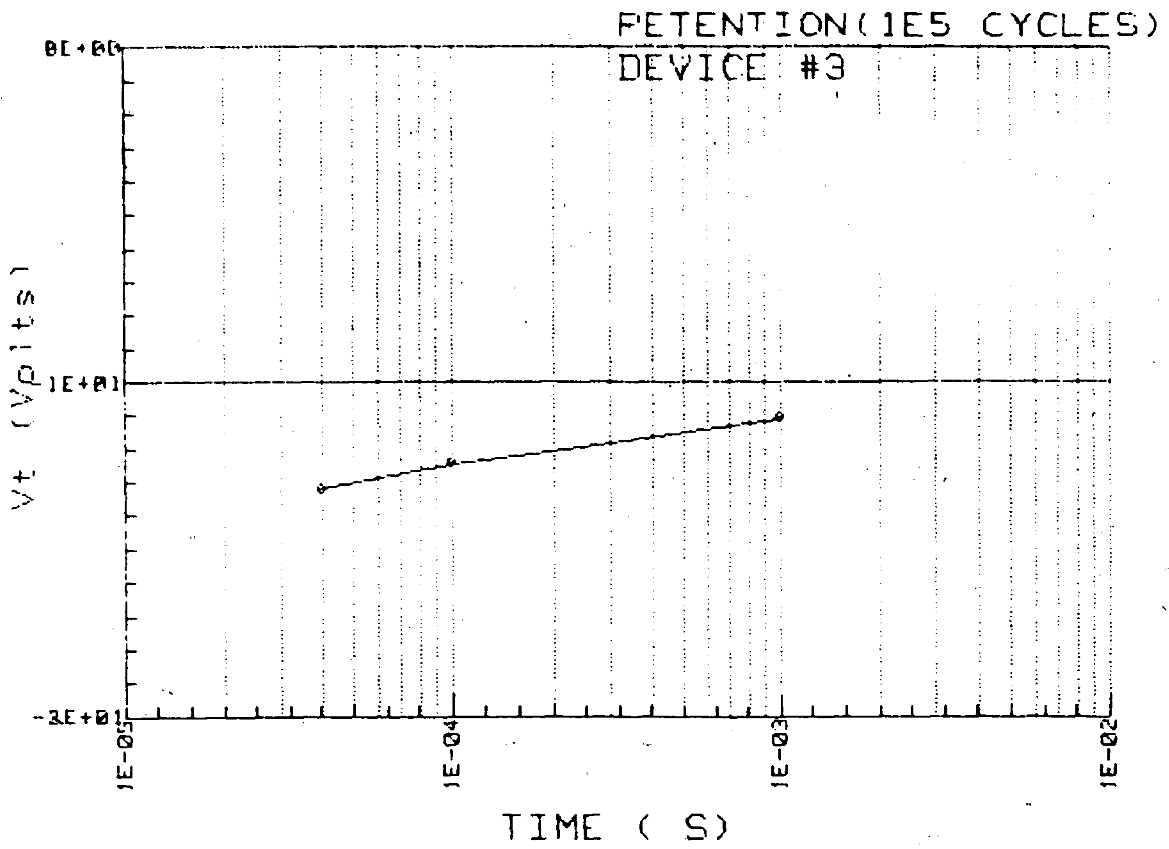


FIGURE 3.5 ENDURANCE MEASUREMENT DATA UPTP 1E5 CYCLES



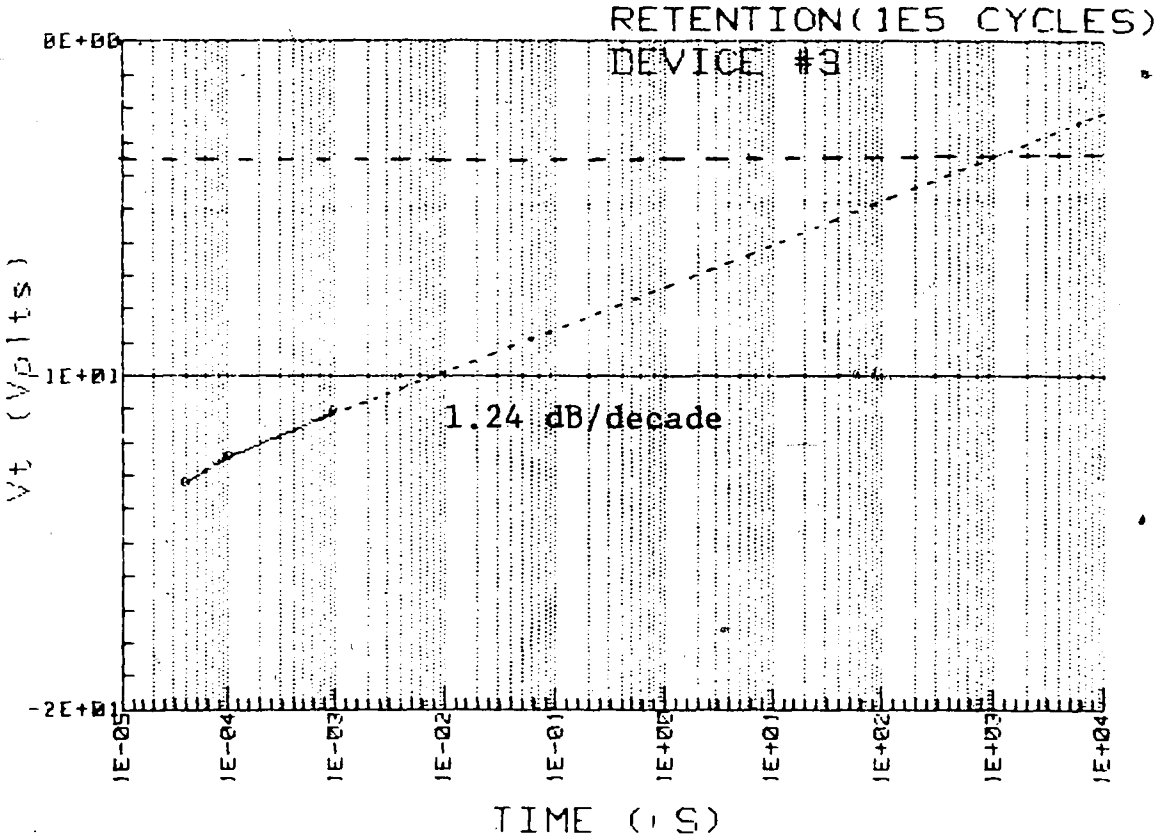
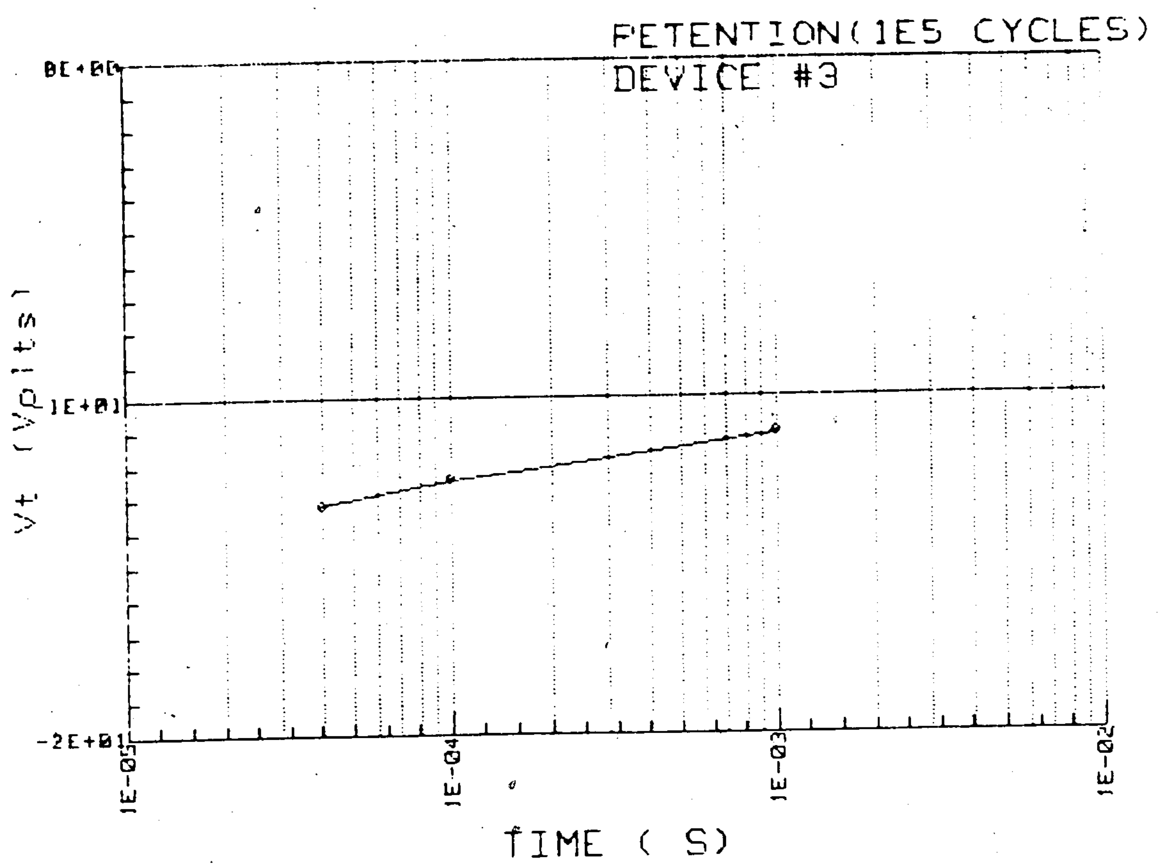


FIGURE 3.6 RETENTION MEASUREMENT DATA AFTER 1E5 CYCLES
(TOP PLOT IS AN ENLARGEMENT)



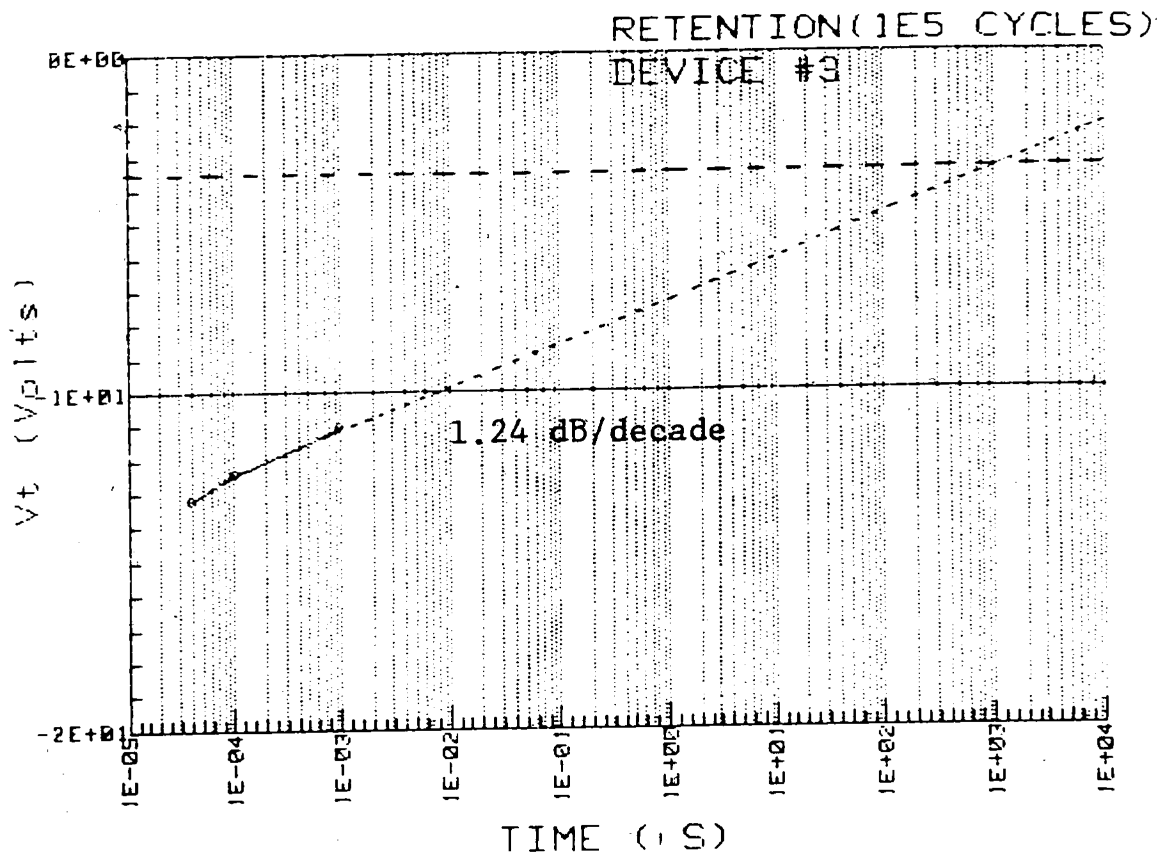


FIGURE 3.6 RETENTION MEASUREMENT DATA AFTER 1E5 CYCLES
(TOP PLOT IS AN ENLARGEMENT)

DISCUSSION OF ENDURANCE CHARACTERISTICS

The data in Figures 3.2 and 3.4 through 3.6 follow the measurement format of (1) cycling (endurance) the device (10E4) and plotting the number of cycles versus threshold voltage, (2) performing a retention measurement and plotting log(t) versus V_t, (4) again cycling Device #3 (10E5) and plotting the number of cycles versus V_t, and (4) performing a retention measurement and plotting log(t) versus V_t. Some other options include (1) continuation with the present pattern, i.e., cycling the device 10E6 and taking a zero bias retention measurement; (2) performing constant current or constant bias retention measurements between cycling measurements; or (3) performing acceleration retention measurements between cycling measurements. Automation provides flexibility, measurement accuracy, and time savings.

(1) Flexibility is demonstrated by the numerous options available to the experimenter. Through the softkeys the experimenter may specify the number of cycles for cycling, whether or not retention measurements are to be performed between cycling and which retention measurement (zero bias, constant current, or constant voltage), and even how the data is to be presented (paper plot or disk storage).

(2) The experimental results presented here were taken in approximately one week. However, out of that week's time, the experimenter was present at only the start-up and end phase of measurement taking, approximately 4 hours. Thus a significant time savings was realized by the experimenter.

(3) Also, computer automation makes possible recording the read pulse transient to 200ns resolution with a 1mV accuracy in the threshold voltage reading. The errors result from the risetime of the read pulse and the off-set voltage of the measuring op-amp in the PGB. All in all, an automated endurance measurement scheme is very advantageous.

CONCLUSION

Results

From the experiments presented in this thesis, the CDCS proved advantages in two of the three MNOST characterization measurements. A functional conclusion is summarized below for each of the three measurements.

(1) In erase/write measurements, the experimenter will input through the HP9836 keyboard V_{GE}, and V_{GW} (see Recommendations). The only manual adjustment is setting t_e and t_w, which requires trimming two variable resistors and looking at the pulse width on an oscilloscope crt. This gives the greatest flexibility to the experimenter. Also, accuracy of the Tek7854 is superior to manually reading a DVM display. Even measurement time savings is evident by comparing one afternoon to one week by conventional techniques for one complete erase/write characteristic. All in all, the erase/write measurement option of the CDCS is superior in every aspect to the conventional manual approach.

(2) Presently, for long retention recording, there is an undesirable two-second gap present starting after 2 ms. The advantage of the CDCS retention option is in the read-delay time (trd). trd may be as short as 100 nanoseconds. For the CDCS retention option to be

completely superior over conventional techniques, the two-second Tek7854 waveform storage time must be reduced. One way is by the use of a DMA (see Recommendations).

(3) The CDCS endurance option is advantageous below 10E5 cycles and disadvantageous above 10E5 cycles. There are several reasons for the above. First, software flexibility allows the experimenter to specify where the Tek7854 should acquire waveforms (t_r), but at the expense of additional measurement time. The PGB must be turned on and off by HP9836 software controlled 5V power supply for each cycle. The HP9836 BASIC code requires a finite time as does the 5V power supply (approximately 1 ms/cycle). In addition, the experimenter may specify the added accuracy of the Tek7854 AVG command (see Recommendations), but not without additional time storage for each averaged waveform. For a V_{GE} and V_{GW} equal to 1 ms without the AVG command, 10E5 erase/write cycles takes ten hours. Obviously, the experimenter is not present.

Recommendations

At the time of compilation of this work, the three measurement options are functioning as described within this work. However, alterations for improvement are constantly in development. Therefore, it is highly recommended that the author be consulted for the latest updates/changes in the CDCS. Among the changes being instituted are (1) the incorporation of six on-board voltage supplies (completed), (2) the presetting of the erase/write voltage amplitude (V_{GE}, V_{GW} through software), (3) the use of DMA in retention data TRANSFER, and (4) software development for taking advantage of the Tek7854 AVG and MEAN functions.

(1) The six on-board voltage supplies in the PGB obviously eliminate all but four periphery power supplies: (a) +7V for powering all of the digital portion of the PGB (see Figure A.3); (b) +5V PGB enable supply controlled by the HP9836, (c) a +25V and (d) a -25V supply for powering of the six on-board voltage supplies that generate variable V_{GW}, V_{GE}, V_R, V_{DD}, and a fixed +15V for the analog PGB circuitry. These on-board power supplies will also decrease the setup time.

(2) By having the experimenter enter V_{GE} and V_{GW} from the keyboard manual adjustment during the erase/ write measurement option will be eliminated.

(3) Replacing the present retention waveform storage in the Tek7854 memory locations by DMA storage in the HP9836, additional waveforms between two milliseconds and two seconds will be possible. Recall that the first retention waveform AQS command captures a 2 ms window (1 μs, 10 μs, 100 μs, and 1 ms tr's). Then this first waveform must be saved (storage equals two seconds in the Tek7854). Now the Tek7854 is ready for the second retention waveform (tr), but after a two-second gap! The DMA will decrease this two-second storage time to approximately 100 ms.

(4) Increased resolution and extending accuracy can be done, for instance, with the Tek 7854 AVG command. For example, the resolution of your measurement --meaning the smallest unit you can distinguish--may be as bad as 1 and 1/2 divisions and only as good as 1/2 division, depending on what part of the signal you were measuring. After averaging, represented by the line inside the noisy signal (Figure 4.1) your resolution would be closer to 1/5 or 1/10 of a division. Now with resolution increased, the accuracy of your Tek7854 has the same trigger each time the scope reads the signal. The noise surrounding the signal, however, is not related to time (independent of the trigger) but is random with an arithmetic mean (AVG) of zero.

For n averages of a waveform, the S/N ratio is improved by a factor of $\sqrt{n}$. For example, if accuracy is $\pm 10\%$ because of noise, S/N equals 10:1. Now an average of only four signals increases that to 20:1 ($10 \times \sqrt{4}$) or 5%. That is an increase by a factor of two! Additional advantages are the Tek7854's pre-triggering viewing, the expansion and repositioning of stored waveforms, and cursor measurements (rise and fall times, delay, pulse width, etc.).

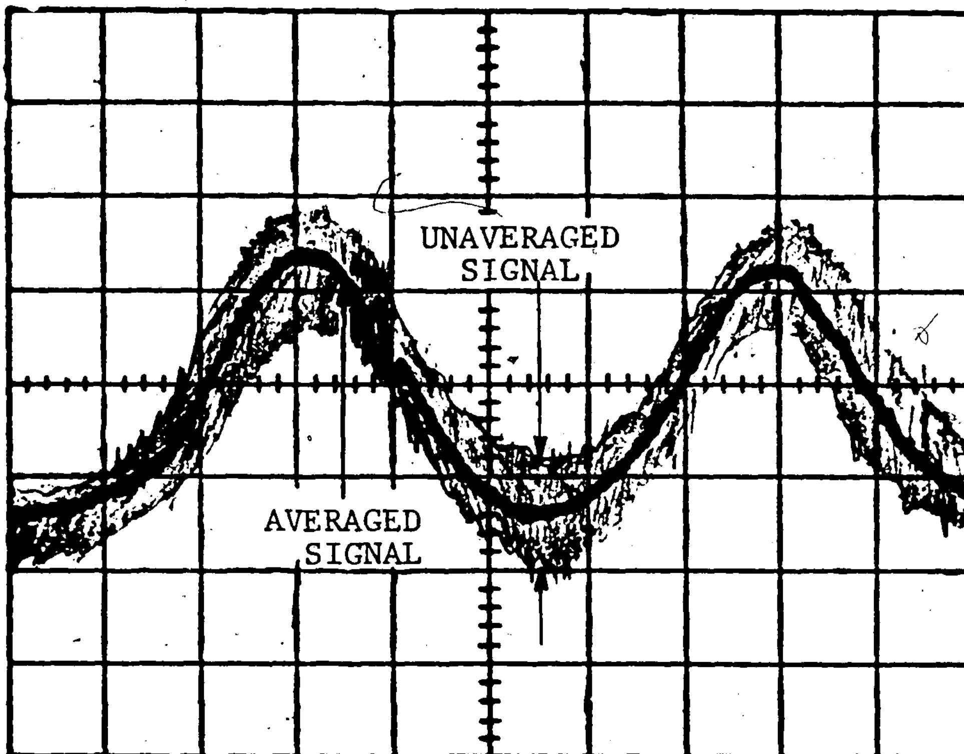


FIGURE 4.1 WAVEFORM RESOLUTION ERROR. UNAVERAGED SIGNAL RANGES FROM 1/2 DIVISIONS TO 1½ DIVISIONS. AVERAGED SIGNAL SHOWS IMPROVEMENT TO 1/10 OR 1/5 OF A DIVISION.

APPENDIX A

PULSE GENERATOR BOARD (PGB)

The function of the PGB is to (1) generate read, write and erase pulses, (2) provide a switching network to apply these read, write, and erase pulses in a pattern to a four-terminal MNOST, and (3) measure the threshold voltage of the MNOST.

The read, write, and erase pulses are generated by the digital portion of the PGB displayed by Figure A.3. When the experimentor starts measurements, the HP9836 instructs the D/A to send a +5V dc voltage from power supply 709 (HP-6505, right) to the PGB input jack labeled "enable." Counters, S-R latches, and the monostable multivibrators (oneshots) are reset and enabled. The voltage controlled oscillator with a 10-MHz crystal (U1) clocks the serially connected decade counters (U2-U14). The output of the decade counters is manipulated by nand gates to trigger the oneshots at 1 μs, 10 μs, 100 μs, and so on. The oneshots generate the digital (0 or 5V) pulses representing the read, write, and erase pulses. The S-R latches insure that the corresponding oneshots are turned off after the generation of their pulse.

The analog switching network shown in Figure A.2 uses the 0 or 5V digital read, write and erase pulses

generated by the oneshots to generate the corresponding analog read, write and erase pulse. Note: The analog DPDT switches used have a 40 volt peak-to-peak limit (or a maximum of +20V). However, a scheme using U62 and U29 as voltage supply switches for U31 allow the corresponding analog erase and write pulse (pins 3 and 4 of U31) to switch up to +25V. U63 (pin 13) provides the switching in of the analog read pulse to the B (bulk) and S (source) terminals of the DUT (MNOST).

When pin 6 of U63 is 0 volts (indicating a read), the inverting input of opamp#1 (U16, pin 2) is connected to the bulk (B) and source (S) of the MNOST (DUT). The opamp output (pin6) is connected to the gate (G).

TABLE A.1 PULSE GENERATOR BOARD PARTS LIST

PART NUMBER		FUNCTION
U1	(74S124)	Voltage Controlled Oscillator with 10MHz Crystal
U2-U14	(74LS162)	4-Bit Decade Counters
U15,U16	(TL081)	High Slew Rate Operational Amplifier
U17-U20		Red DIP Switches (1st Read/Write, 2nd Read/Erase, respectively)
U21,U22 U37,U38	(74LS30)	8-input Positive Nand Gate
U23,U26	(74LS00)	Quadruple 2-input Positive Nand Gate
U27	(74LS133)	13-input Positive Nand Gate
U28	(74LS10)	Triple 3-input Positive Nand Gate
U29,U31 U62,U63	(DG303A)	DPDT 40V Dual Analog Switches
U30,U32,U33 U48,U49	(74LS279)	Quad S-R Latches
U34-U36		13-22K Ohm Common Lead Resistor DIP
U40,U42,U44,U46 U50,U52,U54,U56 U58,U60,OS#1,OS#2		Dual 10K-50K Ohm Multiturn Potentiometers
U41,U43,U45 U51,U53,U55 U57,U59,U61	(74LS221)	Dual Monostable Multivibrators
U47	(LM340)	+5V Voltage Regulator with Heat Sink
R1,R2,R3		1M, 10K, 10K Ohm Metal Film Resistors

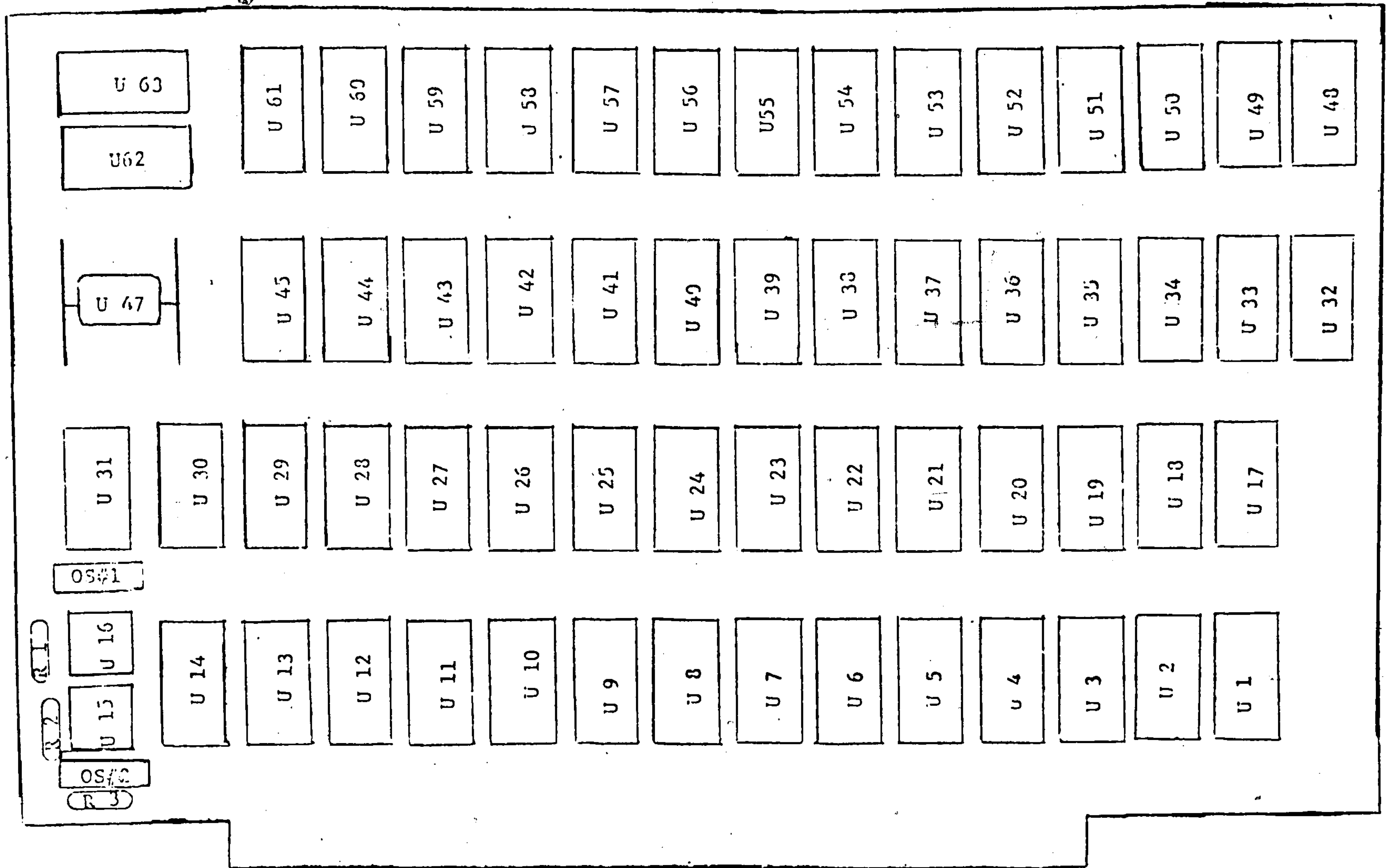


FIGURE A.1 PULSE GENERATOR BOARD LAYOUT

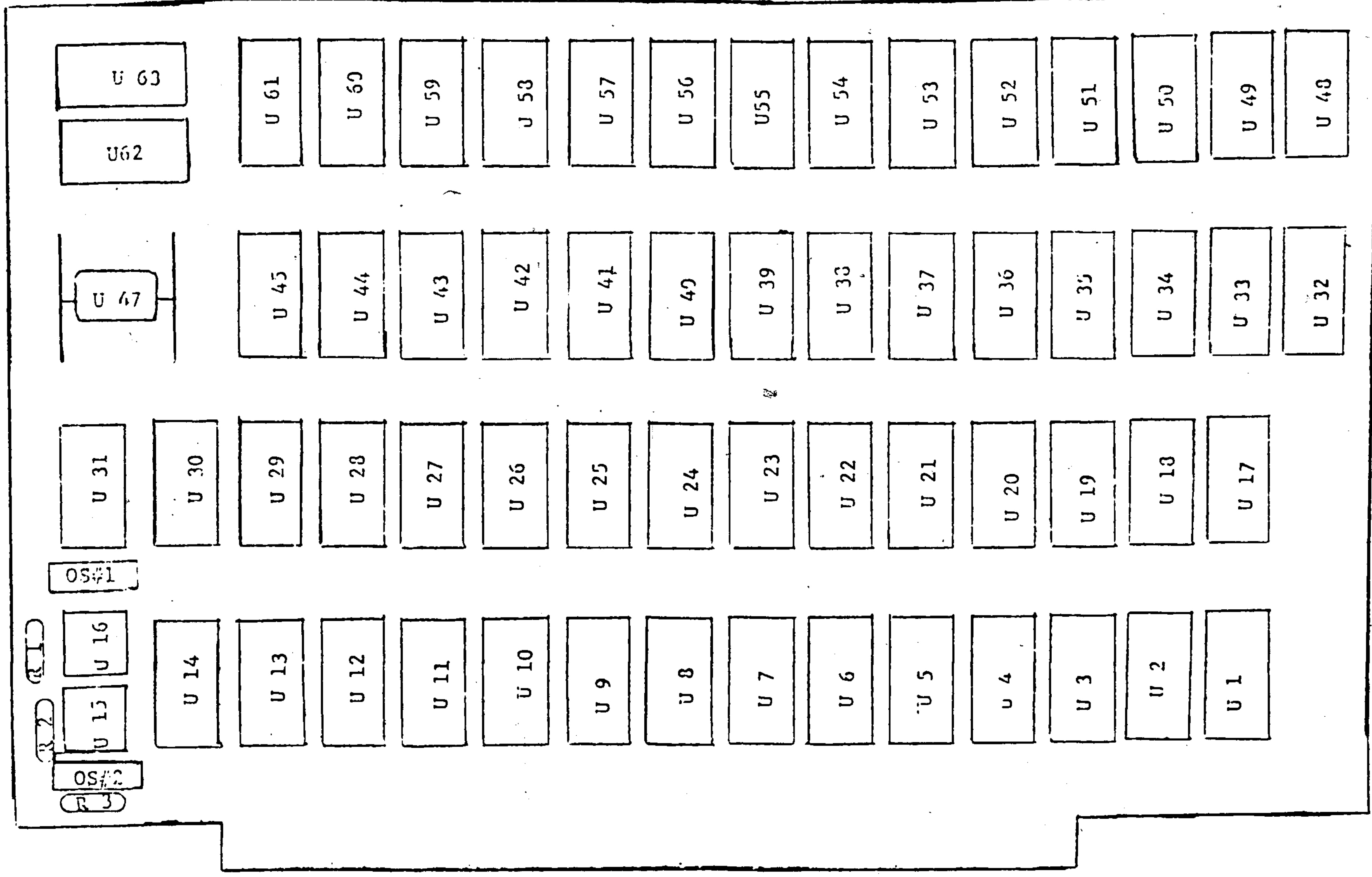


FIGURE A.1 PULSE GENERATOR BOARD LAYOUT

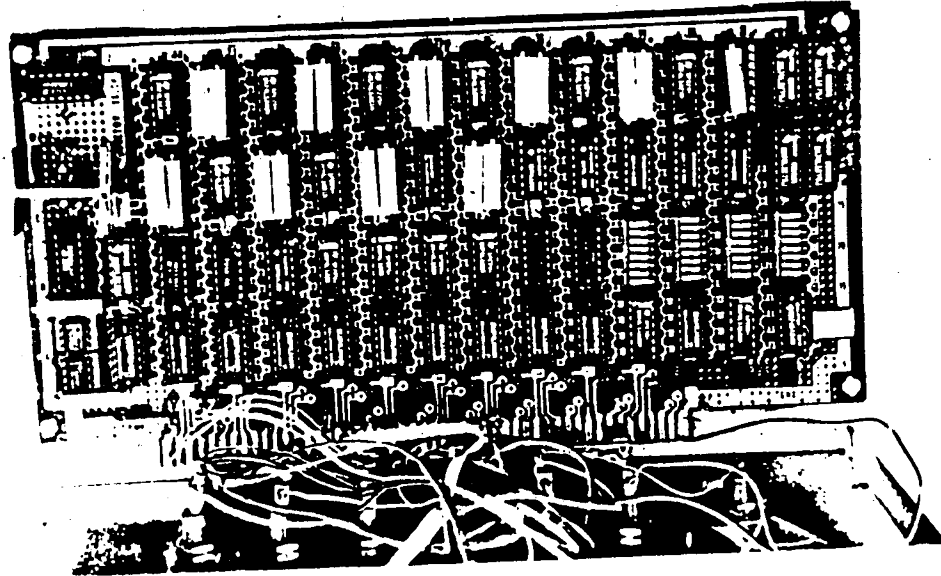


Plate A.1 PHOTOGRAPGH OF PULSE GENERATOR BOARD(PGB)

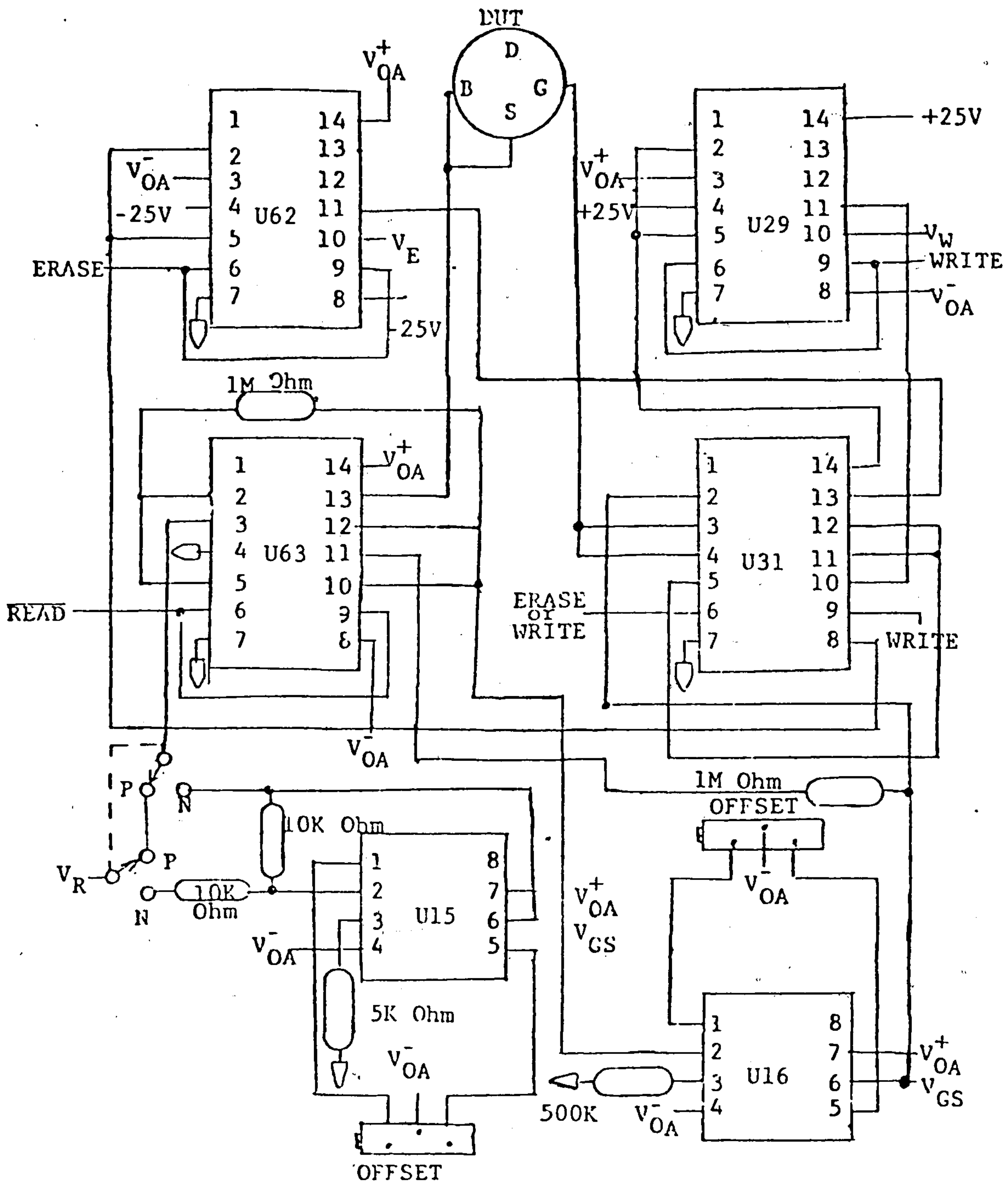


FIGURE A.2 LAYOUT SCHEMATIC OF ANALOG PORTION OF PGB.

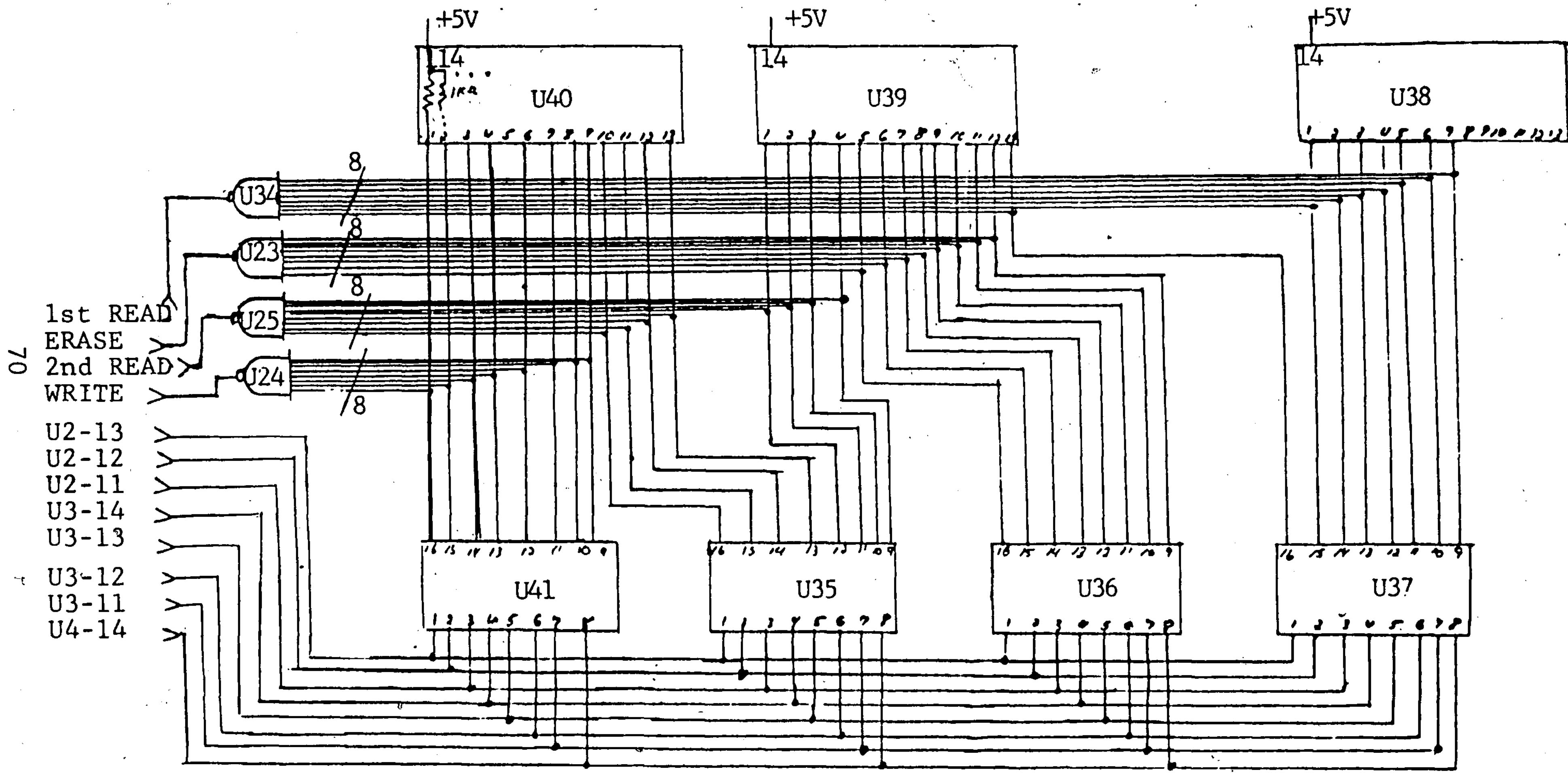
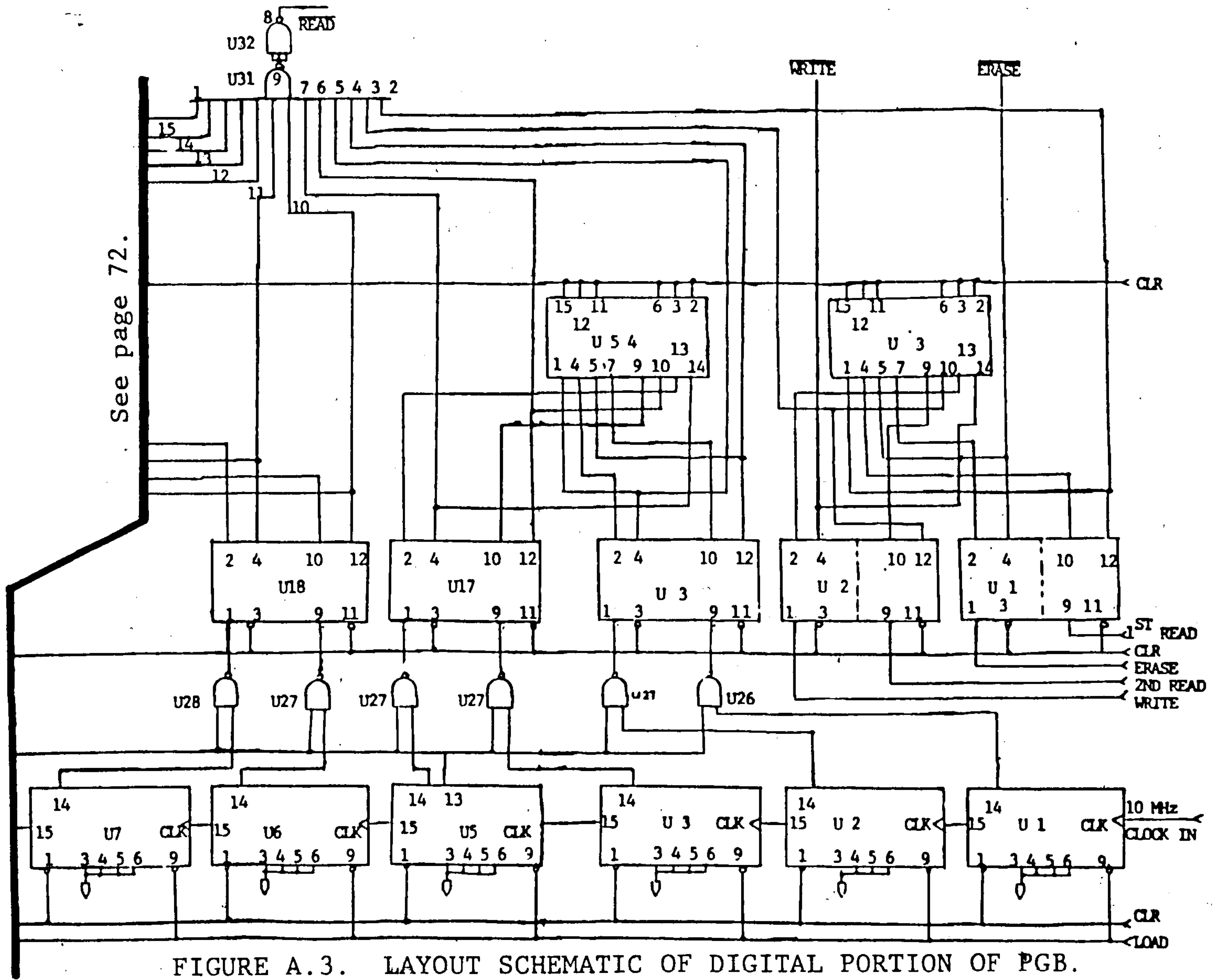


FIGURE A.3 LAYOUT SCHEMATIC OF DIGITAL PORTION OF PGB.



See page 72.

FIGURE A.3. LAYOUT SCHEMATIC OF DIGITAL PORTION OF PGB.

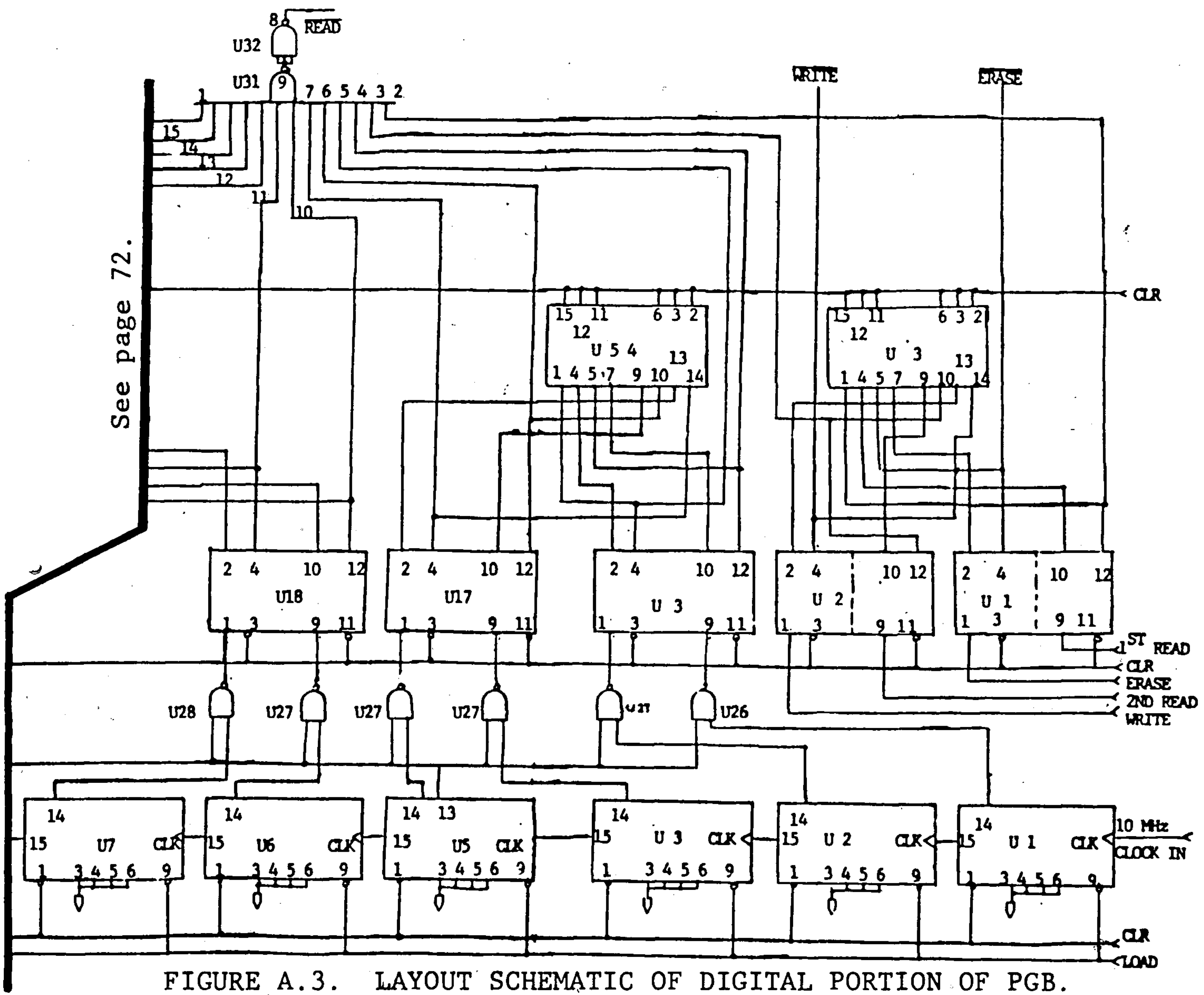
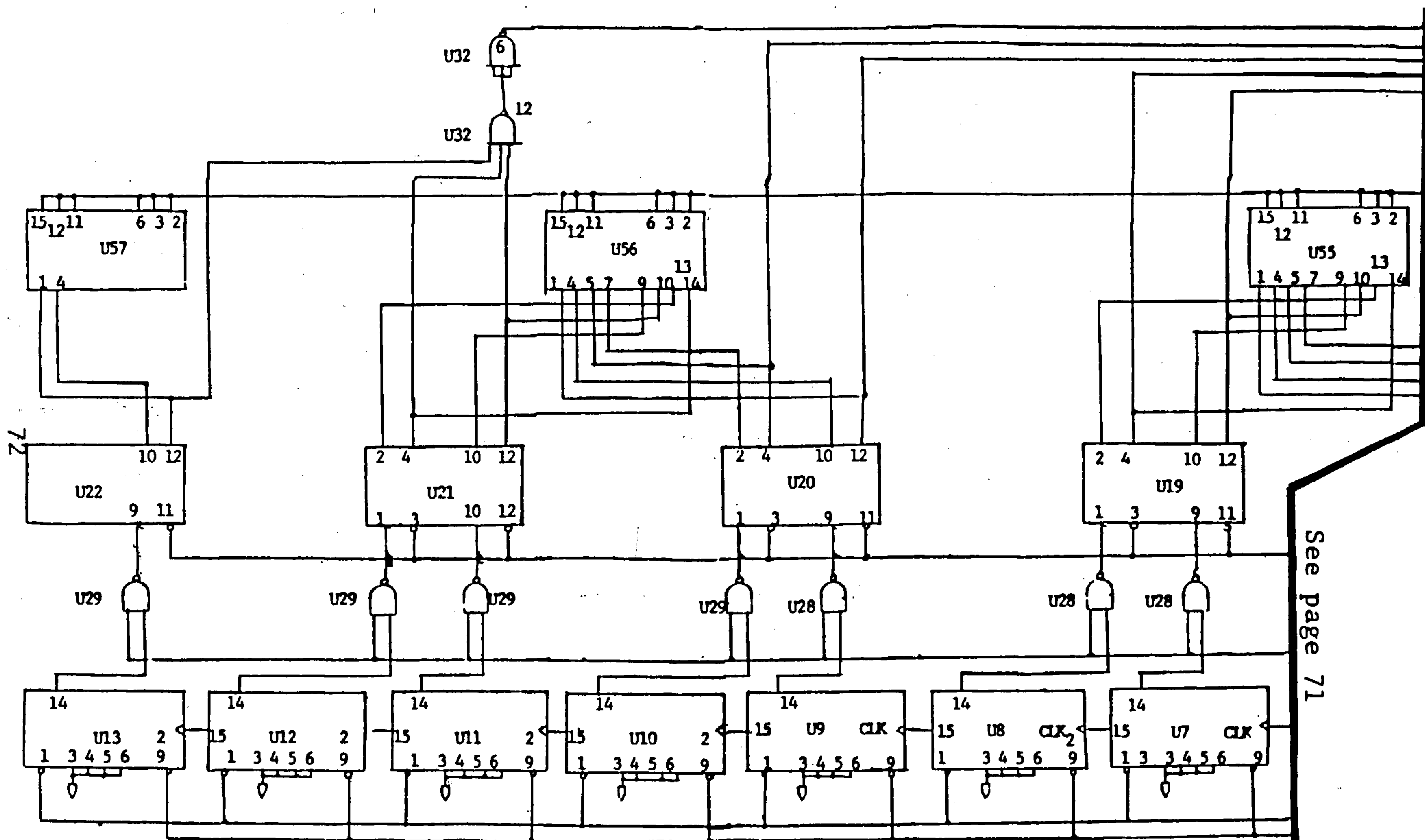
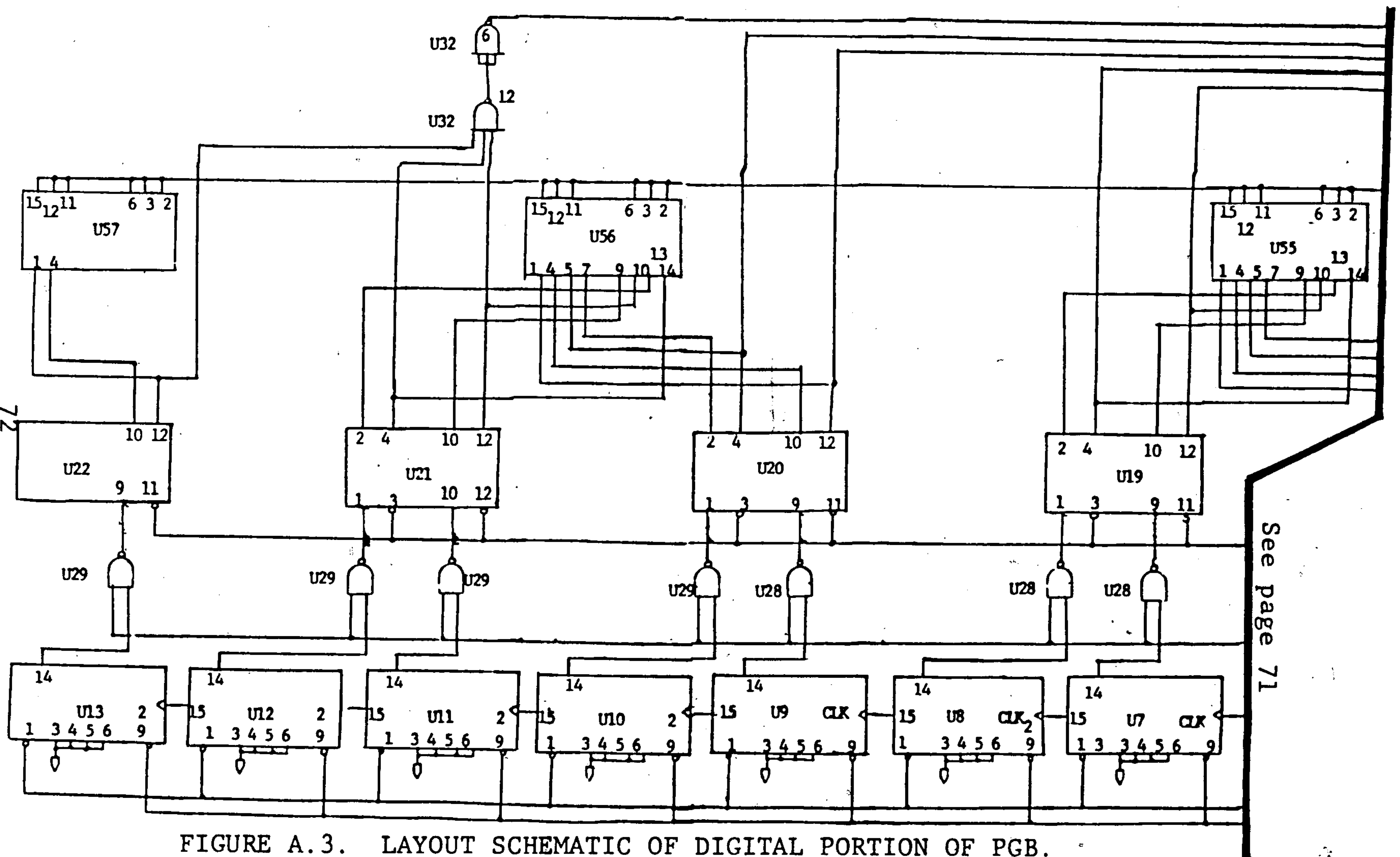


FIGURE A.3. LAYOUT SCHEMATIC OF DIGITAL PORTION OF PGB.



See page 71

FIGURE A.3. LAYOUT SCHEMATIC OF DIGITAL PORTION OF PGB.



See page 71

FIGURE A.3. LAYOUT SCHEMATIC OF DIGITAL PORTION OF PGB.

APPENDIX B

USER'S MANUAL FOR THE COMPUTERIZED DYNAMIC CHARACTERIZATION SYSTEM (CDCS)

The MNOST characterization program (Appendix D) and pulse generator board (PGB - Appendix A) were developed to take measurements on four-terminal P- and N-channel MNOSTs. The CDCS consists of the PGB, HP9836 desktop computer, Tek7854 digitizing scope, an HP59501A D/A converter with 0V to 5V power supply, and other power supplies for biasing the DUT and PGB. Integrated, the CDCS has three different measurement options: erase/write (Chapter 1), retention (Chapter 2), and endurance (Chapter 3). For a detailed description on the three different measurement options, see the chapters noted above. A summary of the CDCS MNOST measurement options is given in Figure B.1. Also, Plate B.1 shows a typical retention waveform pattern of the CDCS summarized in Figure B.1.

OUTLINE PROCEDURE FOR THE CDCS

I. Refer to Figure 0.1 for system diagram. The HP9836 computer is connected via the HPIB interface bus to the HP59501A D/A converter to control the HP6205B power supply (709).

II. Adjust HP59501A D/A full scale of 5V.

   A. Send from the HP9836 the command: "OUTPUT 709 USING "4Z";2000"

   B. Connect a DVM to the 709 power supply and adjust D/A to give 5V.

III. Adjust D/A zero.

   A. Send from the HP9836 the command: "OUTPUT 709 USING "4Z"; 2500"

   B. Connect and DVM to the 709 power supply and adjust D/A to give 0V.

IV. Connect PGB as shown in Figure . Connect power supplies including D/A controlled power supply (709) to labeled power supply inputs.

V. Op-amp offsets:

   A. Place top DPST switch to side labeled "P-channel."

   B. Hold down red normally opened switch labeled "O A OFFSET."

      1. Connect a DVM to jack on PGB labeled "VT" (output) and adjust trim po-

tentiometer on right side of PGB labeled "0 A OFFSET #1" to give 0V.

2. Place top DPST switch to side labeled "N-CHANNEL."

3. Leaving DVM connected from step 1, adjust trim pot on right side of PGB labeled 0 A OFFSET #2" to give 0V. See Figure A.1 for trim pot location.

C. Again, place top DPST switch to "N-CHANNEL" or "P-CHANNEL" for your DUT.

VI. Power up Tektronix 7854.

A. Connect X10 probe from channel one of Tektronix 7854 to PGB output jack "VT."

B. Choose appropriate Tektronix 7854 settings:

1. "VOLTS/DEV" of channel 1 usually at .5V

2. Select "TIME BASE B":

a. Set "TIME/DIV" knob to .2 msec.

b. Set "TRIGGERING" to:

i. "NORM"

ii. "COUPLING AC"

iii. "EXTERNAL TRIG" (plug "EXTERNAL TRIG" from PGB into scope.

VII. Set t_r, t_e, t_w V_{GE}, V_{GW} V_R on PGB (see Table B.2).

VIII. Load "MAIN" program from disk "MNOS PROGRAMS"

IX. Plate DUT into 4-terminal socket on PGB box.

A. The terminals are labeled

1. "G" = gate

2. "D" = drain

3. "S" = source

4. "B" = bulk.

B. Connect appropriate drain bias through the input jack "VD" on the PGB.

X. "RUN" program (refer to Figure D.1). Example follows:

A. "MEASURE" by pressing one of three softkeys:

1. "ENDURANCE" and enter "NUMBER OF CYCLES"

2. "RETENTION" and enter "NUMBER OF DATA POINTS"

3. "ERASE/WRITE" and press "BEGIN"

B. "EXTRACT" data from measurements just taken above. Move knob to move cursor.

C. "PLOT" latest set of EXTRACTED data.

D. "LOAD/STORE" data.

1. "CATALOG" input into "LEFT" or "RIGHT" disk drive.

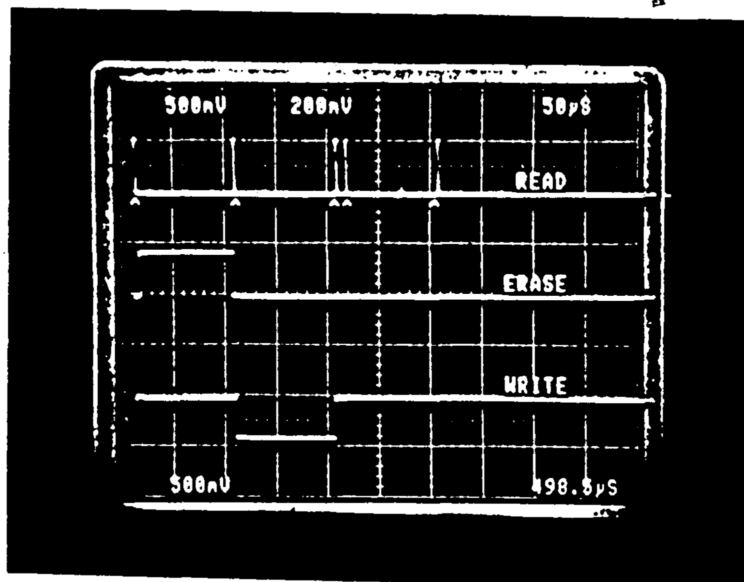
2. "STORE" by inputting "FILENAME."

3. "LOAD" by inputting "FILENAME," "WAVEFORM OR CURVE," "LEFT" or "RIGHT" hand drive.

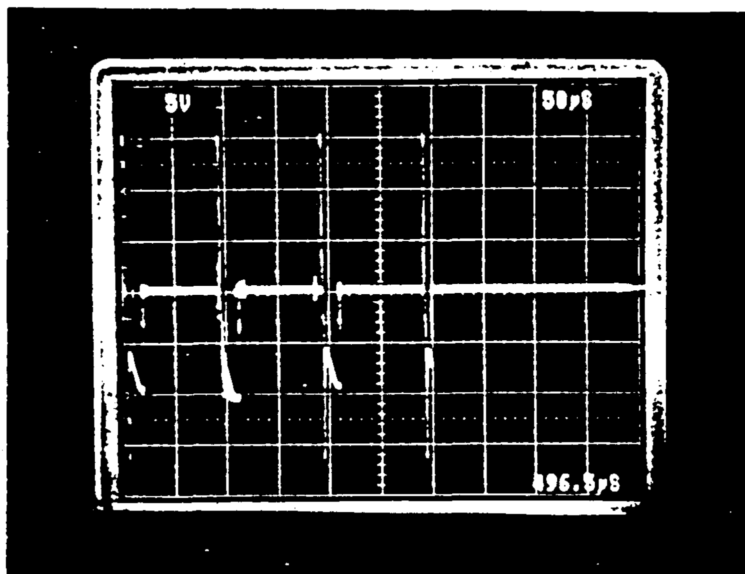
4. "EXIT."

OPTION	SET	WAVEFORM PATTERN GENERATED	MEASURED
ERASE/WRITE	$V_{GS}t_W$ $V_{GS}t_E$ t_{rd}, t_r	A.) (t_r, t_E, t_W) B.)	V_{TH}(TIME)
RETENTION	$V_{GS}t_W$ $V_{GS}t_E$ t_{rd}, t_r	A.) ... B.) ...	V_{TH}(# OF CYCLES)
ENDURANCE	$V_{GS}t_W$ $V_{GS}t_E$ t_{rd}, t_r	A.) ... B.) ...	$V_{TH}(V_{GS}t_w, V_{GS}t_E)$

FIGURE B.1 SUMMARY OF MNOS CHARACTERIZATION MEASUREMENT OPTIONS WITH PULSE GENERATOR BOARD(PGB).



(a.)



(b.)

PLATE B.1 PHOTOGRAGPH OF (a.)A TYPICAL PULSE TRAIN PATTERN GENERATED BY PGB FOR RETENTION MEASUREMENT AND (b.)V_{GS} OF A MNOST INTERROGATED BY CONSTANT CURRENT RETENTION METHOD.

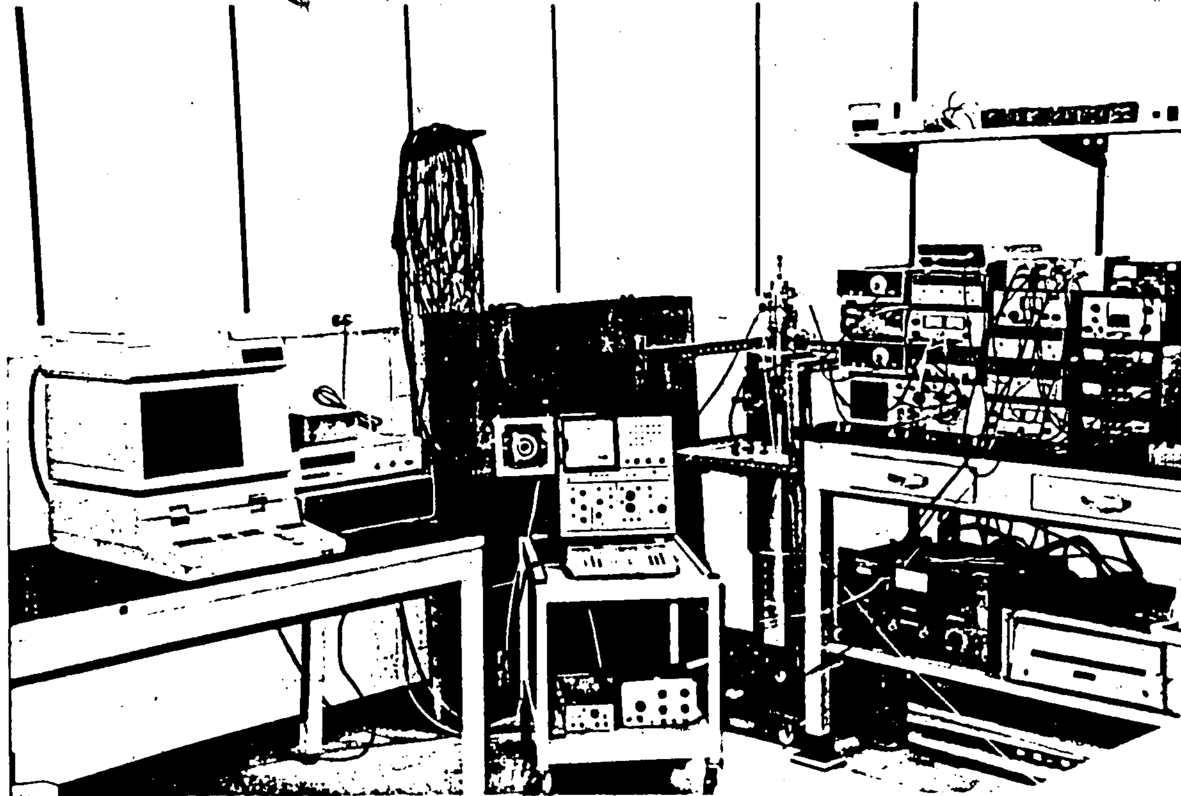


PLATE B.2 PHOTOGRAPH OF LABORATORY SET-UP IN DEVICE CHARACTERIZATION LAB.

APPENDIX C

DUT AND MNOST MICROELECTRONIC FABRICATION PROCESS

The dimensions of the p-channel DSP and n-channel MNOST measured in this work are shown in Figure C.1.

The DSP poly-gate process is listed in Table C.1 with a cross-section of the process shown in Figure C.5.

Also a photomicrograph of the poly and metal-gate DSP MNOST appears in Plates C.1 through C.3.

TABLE C.1 MNOS MEMORY TRANSISTOR PROCESS

LEVEL	STEPS
0	Incoming Inspection and Oxidation
	1. Clean and HF etch of 4-8 Ohm-cm N-type, 100 wafer.
	2. 6KA oxide (wet, 1100 C, 45 min) (dry, 1100 C, 5 min)
	3. Anneal (N, 700 C, 16 hrs)
1	N^+ Substrate Contact (P_s < 30 Ohm/Sq)
	1. Photoengraving 1 (etch oxide)
	2. Clean
	3. Deposition (Phos, 950 C, 5-14-1)
	4. Strip glass
	5. 6KA oxide (wet, 1100 C, 45 min) (dry, 1100 C, 5 min)
	6. Drive in (wet, 1000 C, 50 min) (dry, 1000 C, 5 min)
2	P^+ Source and Drain (P_s = 150 Ohm/Sq)
	1. Photoengraving 2 (etch oxide)
	2. Clean
	3. Deposition (B, 980 C, 3-18-2)
	4. Drive in (wet, 1000 C, 30 min) (dry, 1000 C, 60 min)
	5. 1KA non-memory fate oxide (HCl, 1000 C, O -90 min, N -30 min)
3	Memory Window
	1. Photoengraving 3 (etch oxide)
	2. Clean (pre-nitride)
	3. 25A memory gate oxide (HCl, 750 C)
	4. Deposition (Si_3N_4, 500A)
	5. Deposition (Poly, 3.5KA, 850 C, 5-60-1, P_s = 1000+10% Ohm/Sq)
	6. 2KA silox
4	Polysilicon Definition
	1. Photoengraving 4 (etch Silox, Poly)
	2. Clean (strip remaining Silox)

Level	Steps
5	Nitride Etch
	1. Photoengraving (plasma etch nitride) 2. Clean 3. 1KA oxide (wet, 1000 C, 15 min)
6	Metal-Poly Contact Windows
	1. Photoengraving (etch oxide) 2. 10KA Aluminum (electron bombardment)
7	Metal Mask
	1. Photoengraving 7 (etch aluminum) 2. 13KA Silox (passivation oxide) 3. 10KA Aluminum (electron bombardment) 4. Sinter (450 C, 25 min)

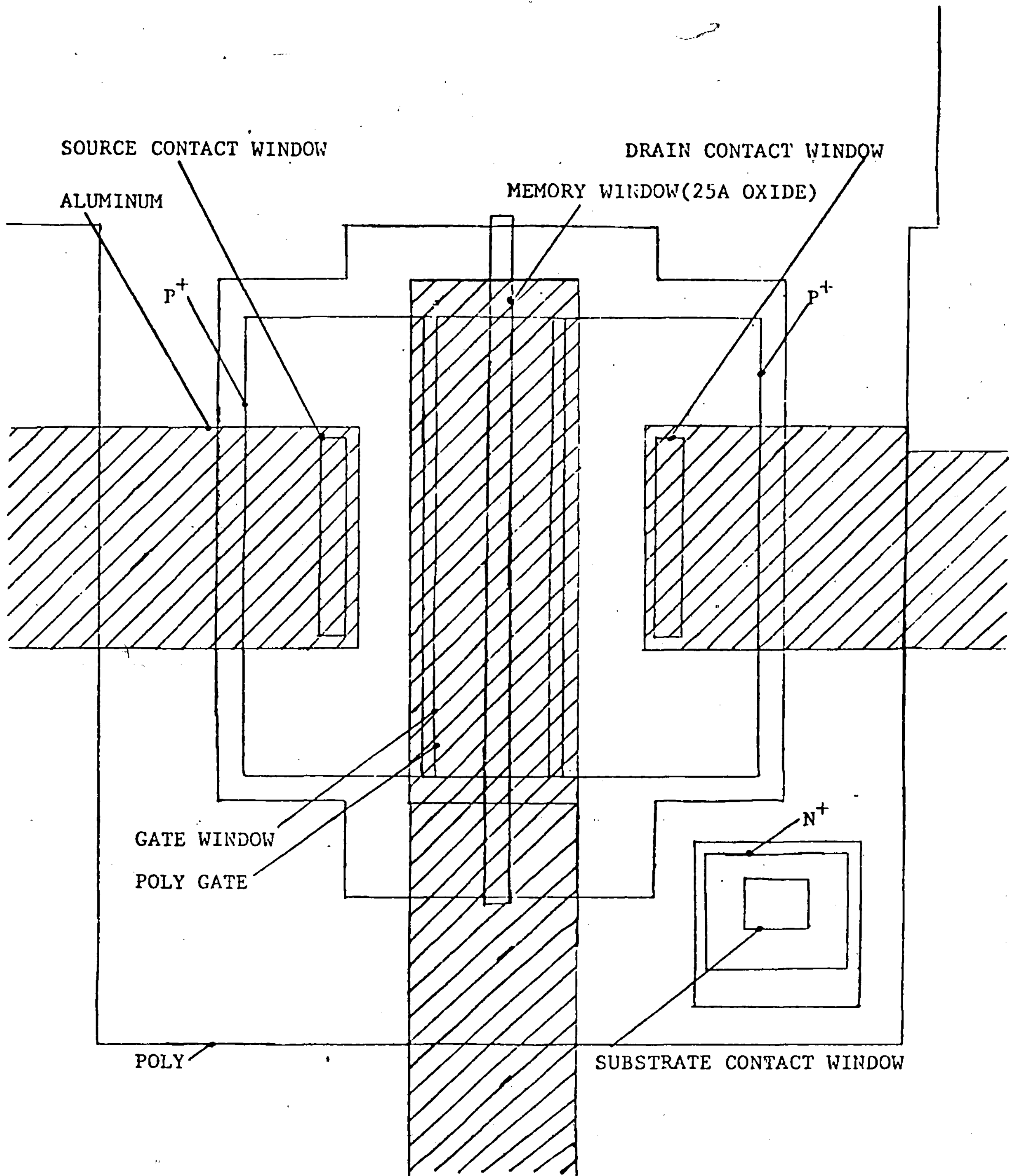


FIGURE C.1 DEVICE LAYOUT: P-CHANNEL DSP MNOST.

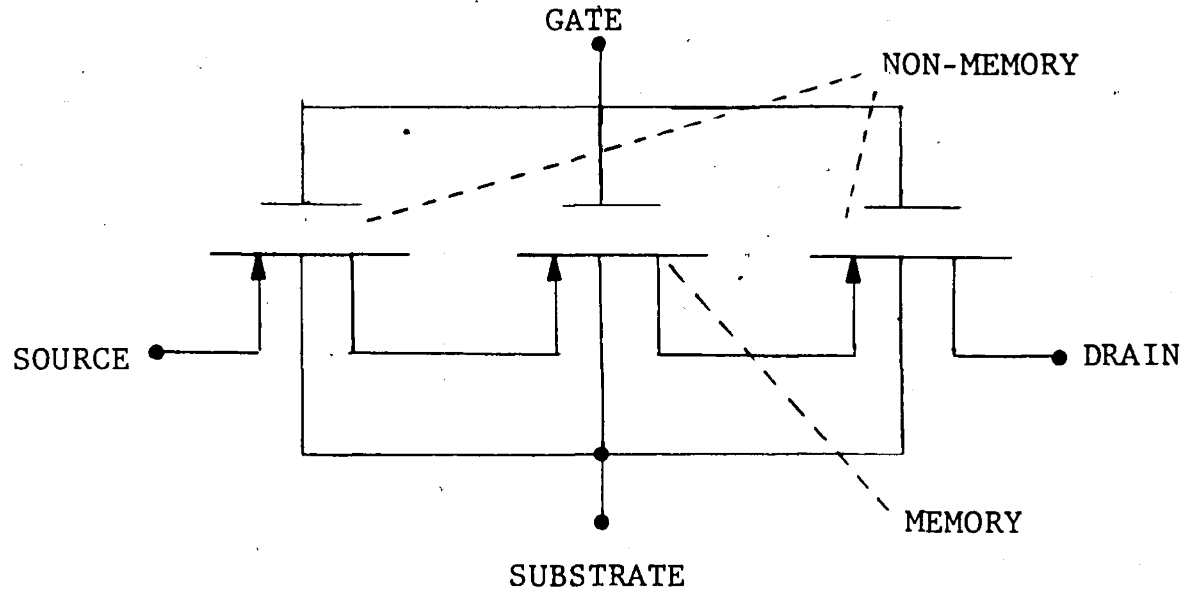


FIGURE C.2 EQUIVALENT CIRCUIT OF THE DRAIN-SOURCE PROTECTED (DSP) MNOST.

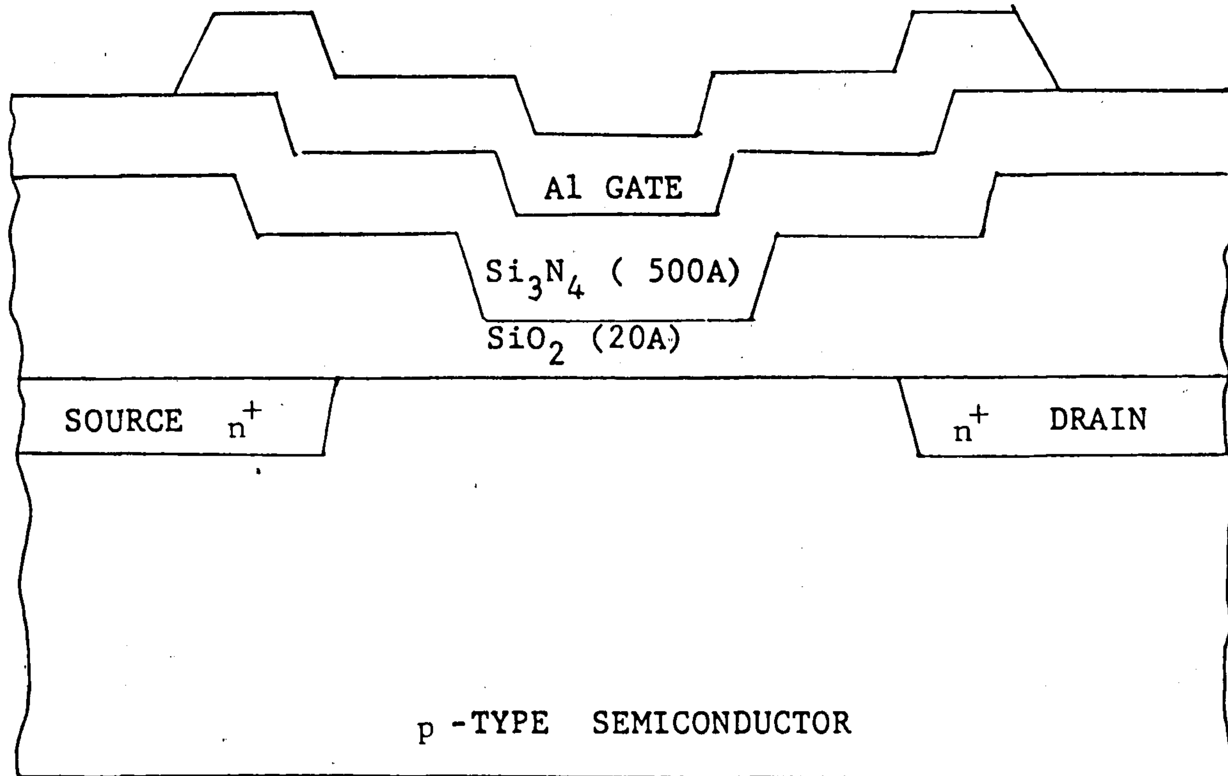


FIGURE C.3
CROSS SECTION OF N-CHANNEL MNOS MEMORY TRANSISTOR

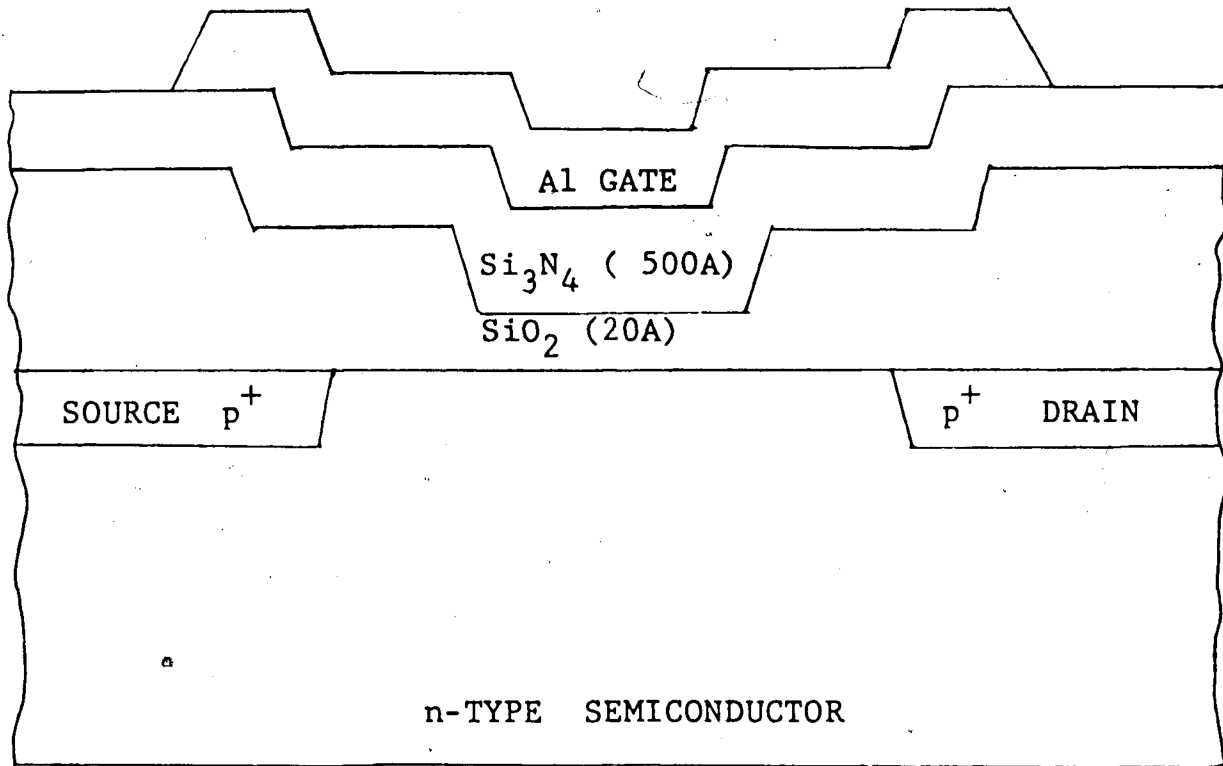


FIGURE C.4
CROSS SECTION OF P-CHANNEL MNOS MEMORY TRANSISTOR

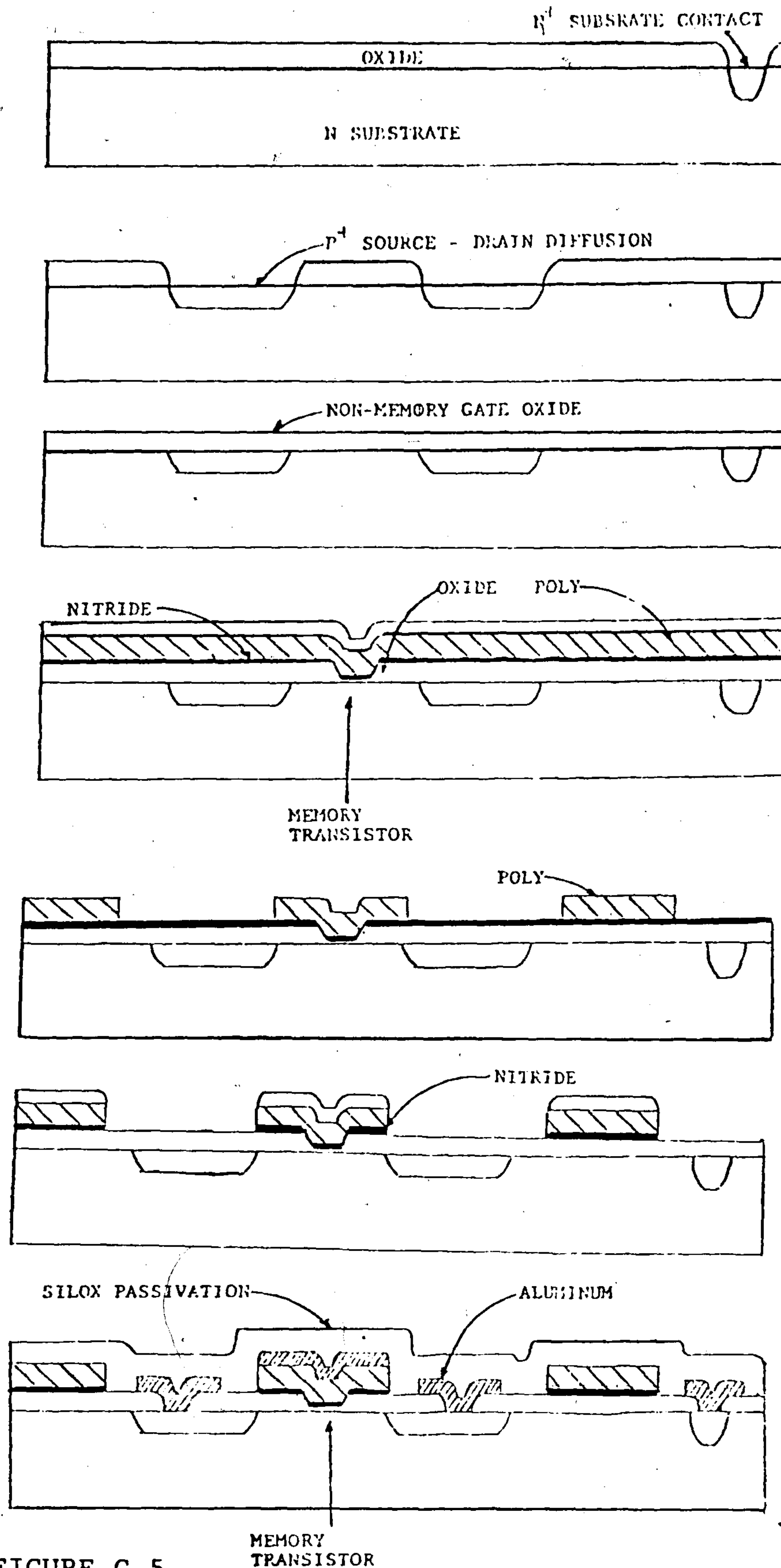
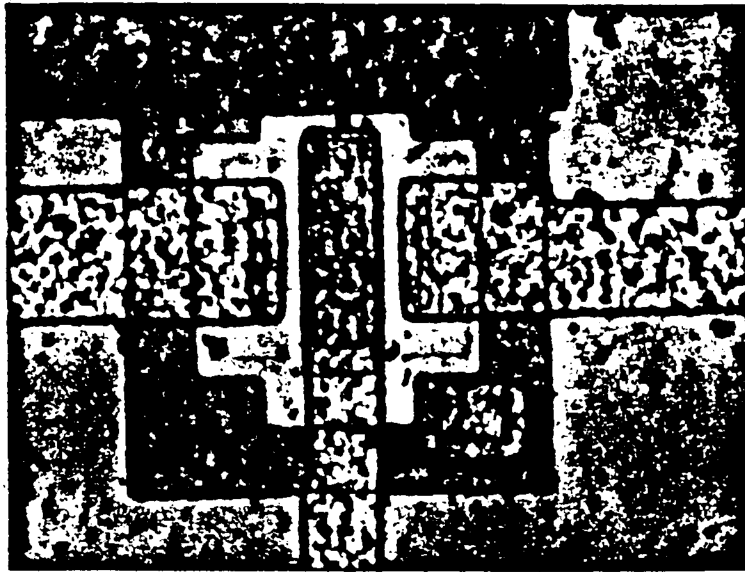


FIGURE C.5

MICROELECTRONIC FABRICATION PROCESS FOR MNOST



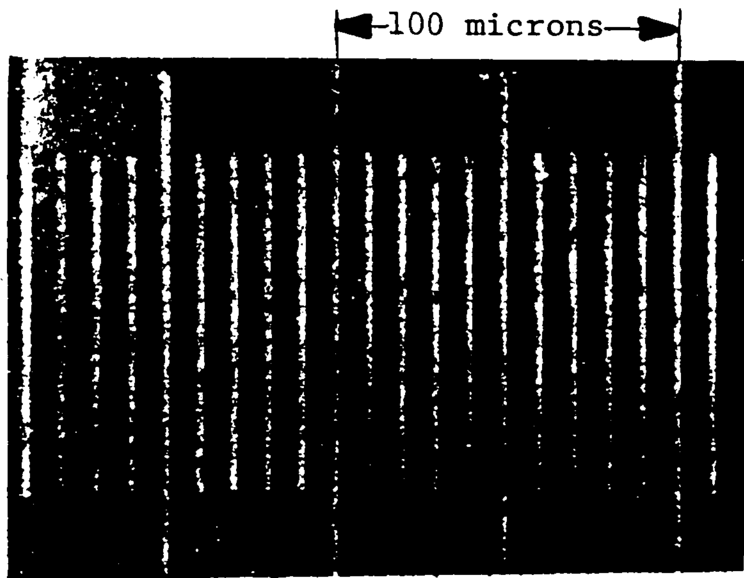
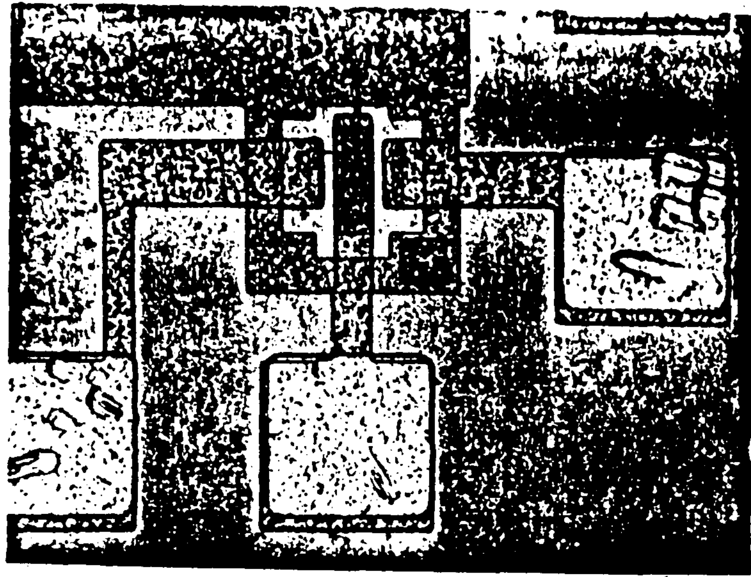


PLATE C.1 MICROPHOTOGRAPH OF METAL GATE(AL) P-CHANNEL DSP MNOST WITH SCALE.



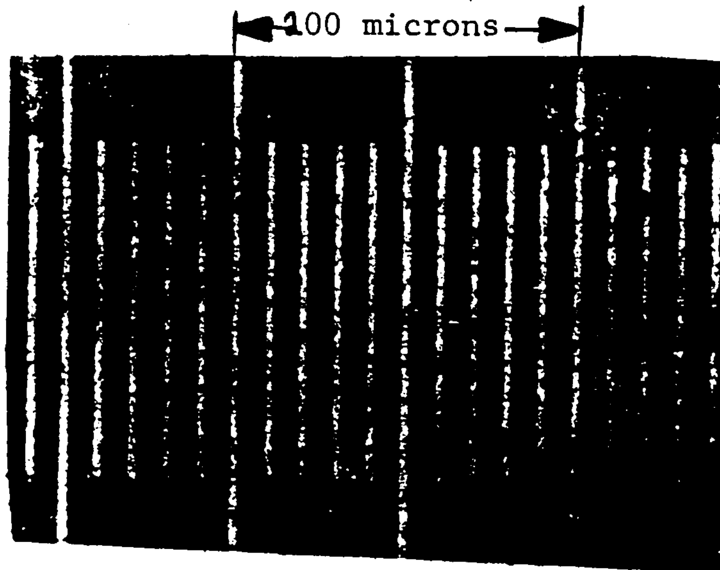
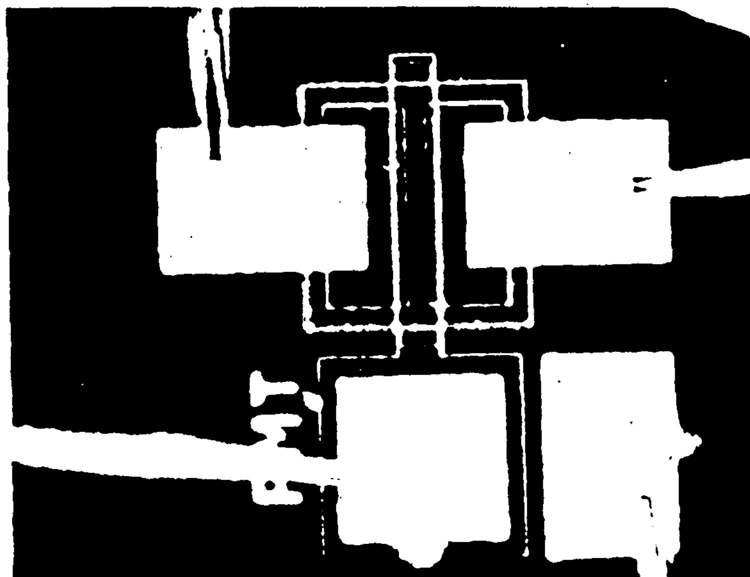


PLATE C.2 MICROPHOTOGRAPH OF P-CHANNEL DSP(POLY) MNOST WITH SCALE.



1000 microns

PLATE C.3 MICROPHOTOGRAGH OF METAL GATE(AL) N-CHANNEL MNOST WITH SCALE.

APPENDIX D

MNOS MEMORY TRANSISTOR CHARACTERIZATION
PROGRAM LISTING

This program is written to gather retention, endurance, and erase/write data from the MNOS Pulse Generator Board. The program is written in a structured manner so that the program functions are available to the user with use of the software keys. The functions available are EXTRACT, EXIT, PLOT, LOAD and STORE. See Figure D.1 for program structure setup.

The program uses a D/A, the Pulse Generator Board, and the Tektronix 7854 Digitizing Oscilloscope. The program controls the D/A to create an enable and a clear signal to the Pulse Generator Board as well as instructing the Tektronix 7854 Digitizing Oscilloscope to gather V_{gs} across the MNOS memory transistor.

Usually, a user, after calibration (see Appendix B), would run the MEASUREMENT subroutine and data will be collected. When data gathering is complete it may be graphed (PLOT) or STORED. Old data files can be retrieved with the LOAD key. For the convenience of the user a software key, CATALOG, is incorporated to assist in recalling the store data file names.

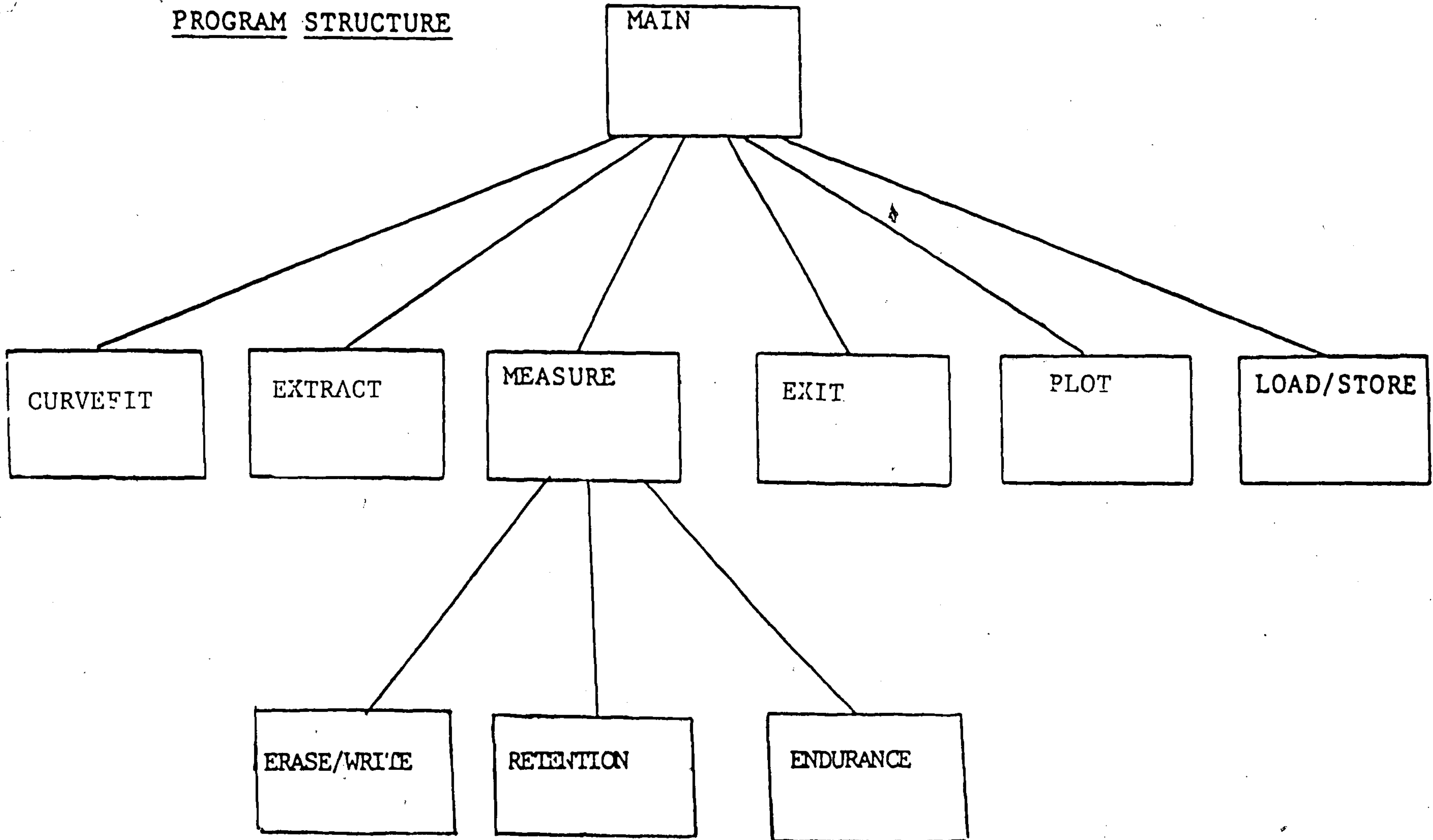


FIGURE D.1 HP9836 CONTROLL PROGRAM STRUCTURE

TABLE 0.1 VARIABLE DIRECTORY OF COMMON BLOCK

MNOS-DATA

VARIABLE	DESCRIPTION
PREAMBLE$	(STRING) 200 characters containing points/waveform, volts/division, time/division, offset voltage, etc., from the Tektronix 7854 Digitizing Oscilloscope.
HEADER$	(STRING) Six characters that are a carriage return and line feed received from the Tektronix 7854 Digitizing Oscilloscope.
WAVEFORM (20,512)	(REAL) Measured data containing the actual vertical ordinate value (in divisions) of each point of the waveform relative to the CRT graticle of the Tektronix 7854 Digitizing Oscilloscope.

POINTS

VARIABLE	DESCRIPTION
V_{GS} (20)	(REAL) The user "EXTRACTED" V_{GS} values from the array WAVEFORM (20,512) are stored here until the softkeys "PLOT" or "STORED" are pressed.
T (20)	(REAL) Same function as V_{GS} (20) above.
NPTS	(INTEGER) Variable set for the number of points contained in one waveform transfer from the Tektronix 7854 Digitizing Oscilloscope, i.e. 128, 256, 512, 1024.

TABLE D.2 SUMMARY OF PROGRAM LISTING

LINES		EXPLANATION
FROM	TO	
10	300	(MAIN) PROGRAM. Defines software keys and waits in idle loop until user specifies next subroutine to be executed.
330	500	(MEASURE) SUBROUTINE. Set up soft-keys and wait for user to specify from one of three measurements: (RETENTION), (ENDURANCE), (ERASE/WRITE).
510	850	(ENDURANCE) SUBROUTINE. User must specify "number of cycles" the device is to be cycled. V_{GS} is stored in WAVEFORM (20,512) every 1, 2, 5, and 7 measurements of a cycle.
860	1280	(RETENTION) SUBROUTINE. User must specify "number of cycles" the device is to be monitored in time. V_{GS} is stored in WAVEFORM (20,512) logarithmically each decade.
1290	1420	(ERASE/WRITE) SUBROUTINE. Records V_{GS} before and after V_w and V_e.
1450	3510	(PLOT) SUBPROGRAM. General plotting subprogram.
3540	4400	(EXTRACT) SUBPROGRAM. Lets user extract points from waveforms (WAVEFORM (20,512)) acquired by Tektronix 7854 Digitizing Oscilloscope by moving cursor knob on HP9836 keyboard.
4430	5100	(LOAD/STORE) SUBPROGRAM. Creates file, stores data, and closes file or opens file, loads previously taken data, and closes file.

```
10    !-----------------------------------------------------------------------
20    ! MNOS RETENTION, ENDURANCE, AND ERASE/WRITE CHARACTERISTICS MEASUREMENT
30    !-----------------------------------------------------------------------
40    !
50    !       DECLARATIONS
60    !
70    OPTION BASE 1
80    COM /Mnos_data/ Preamble$[200],Header$[6]
90    COM /Mnos_data/ Waveform(20,512)
100   COM /Mnos_data/ Devicetype(1)
110   COM /Mnos_data/ Comments$[30]
120   COM /Points/ Vgs(20),T(20),Npts
130   !
140   !       DEFINE KEY FUNCTIONS
150   !
160   ON KEY 0 LABEL "MEASURE" CALL Measure
170   ON KEY 2 LABEL "PLOT" CALL Mnos_plot
180   ON KEY 7 LABEL "LOAD/STORE" CALL Load_store
190   ON KEY 5 LABEL "EXTRACT" CALL Extract
200   ON KEY 9 LABEL "EXIT" GOTO Ending
210   !
220   !      SET MACHINE IN IDLE LOOP WHILE WAITING FOR KEY INTERRUPTS
230   !
240   LOOP
250      DISP "PRESS KEY"
260   END LOOP
270   !
280   !      EXIT PROGRAM
290 Ending:  !
300   END
310   !
320   !
330  SUB Measure    ! ACQUIRE DATA WITH 'SCOPE
340  OPTION BASE 1
350  INTEGER Stat
360 COM /Mnos_data/ Preamble$[200],Header$[6]
370  COM /Mnos_data/ Waveform(20,512)
380 COM /Mnos_data/ Devicetype(1)
390 COM /Mnos_data/ Comments$[30]
400  COM /Pulse/ Pulse_width,Amplitude
410  OFF KEY
420  ON KEY 0 LABEL "ENDURANCE",15 GOTO Endurance
430  ON KEY 1 LABEL "RETENTION",15 GOTO Retention
440  ON KEY 2 LABEL "ERASE/WRITE",15 GOTO Erase_write
450  ON KEY 9 LABEL "EXIT",15 GOTO Go_back
460  WHILE 1=1
470       DISP "PRESS KEY"
480  END WHILE
490 Go_back:  !RETURN TO MAIN PROGRAM
500  SUBEXIT
510 Endurance:  ! OBTAIN DATA FOR ENDURANCE CHARACTERISTICS
520 DISP "NUMBER OF CYCLES?";
530 INPUT Cycles
540  PRINT Cycles;" CYCLES"
550  ALLOCATE Temp(512)
560 INTEGER I,J,Flag
570 I=0
580 ON INTR 7 GOSUB Interrupt
590 ENABLE INTR 7:8
600 L1=0
610 L2=DROUND(LGT(2),12)
```

```
620 L5=DROUND(LGT(5),12)
630 L7=DROUND(LGT(7),12)
640  FOR Counter=1 TO Cycles
650      OUTPUT 709 USING "4Z":2000
660      Flag=0
670      Round=DROUND(LGT(Counter)-INT(LGT(Counter)),12)
680      IF Round=L1 OR Round=L2 OR Round=L5 OR Round=L7 THEN Flag=1
690      IF Flag=1 THEN OUTPUT 711;"AQS"
693      WAIT .2
700      OUTPUT 709 USING "4Z":2500
710      WAIT .5
720      OUTPUT 709 USING "4Z":2000
730      IF Flag=1 THEN
740           OUTPUT 711;"SENDX"
750           WAIT .5
760           ENTER 711;Preamble$,Header$,Temp(*)
770           I=I+1
780           Stat=SPOLL(711)
790           FOR J=1 TO 512
800                Waveform(I,J)=Temp(J)
810           NEXT J
820      END IF
830  NEXT Counter
840 DEALLOCATE Temp(*)
850 SUBEXIT
860 Retention:  ! TAKE DATA FOR RETENTION CHARACTERISTICS
870 DISP "NUMBER OF CYCLES?";
880 INPUT Cycles
890  ALLOCATE Temp(512)
900 ON INTR 7 GOSUB Interrupt
910 ENABLE INTR 7:8
920  I=0
930  OUTPUT 711;"AQS 1 >WFM AQS 2 >WFM AQS 3 >WFM AQS"
940  WAIT .5
950  OUTPUT 709 USING "4Z":2500
960  !  1000 SEC. ALLOTTED FOR TRANSFER OF FIRST 6 WAVEFORMS.
970 OUTPUT 711;"1 WFM SENDX"
980 GOSUB Accept
990 OUTPUT 711;"2 WFM SENDX"
1000 GOSUB Accept
1010 OUTPUT 711;"3 WFM SENDX"
1020 GOSUB Accept
1030 OUTPUT 711;"0 WFM SENDX"
1040 GOSUB Accept
1050 J=7
1060 WHILE J<=Cycles
1070      OUTPUT 711;"AQS SENDX"
1080      ENTER 711;Preamble$,Header$,Temp(*)
1090      Stat=SPOLL(711)
1100      I=I+1
1110      FOR K=1 TO 512
1120           Waveform(I,K)=Temp(K)
1130      NEXT K
1140      J=J+1
1150      PRINT I+4
1160 END WHILE
1170 OUTPUT 709 USING "4Z";2000
1180 DEALLOCATE Temp(*)
1190 SUBEXIT
1200 Accept: ! GET DATA AND TRANSFER INTO Waveform(*)
```

```
1210 ENTER 711:Preamble$,Header$,Temp(*)
1220 Stat=SPOLL(711)
1230 I=I+1
1240 PRINT I+4
1250 FOR J=1 TO 512
1260      Waveform(I,J)=Temp(J)
1270 NEXT J
1280 RETURN
1290 Erase_write: ! TAKE DATA FOR ERASE/WRITE CHARACTERISTICS
1300 DISP "PULSE WIDTH?";
1310 INPUT Pulse_width
1320 DISP "PULSE AMPLITUDE?";
1330 INPUT Amplitude
1340 DISP "SET THE PULSE WIDTH AND AMPLITUDE; PRESS KEY 0 TO BEGIN MEASUREMENTS.
"
1350 BEEP
1360 GOTO 1360
1370 SUBEXIT
1380 Interrupt:  !  HANDLE INTERRUPTS
1390 Stat=SPOLL(711)
1400 ENABLE INTR 7;8
1410 RETURN
1420 SUBEND
1430 !
1440 !
1450 SUB Mnos_plot
1460 OPTION BASE 1
1470 COM /Points/ Vgs(*),T(*),Npts
1480 IF Npts=0 THEN SUBEXIT
1490 ALLOCATE X(Npts),Y(Npts)
1500 FOR I=1 TO Npts
1510      X(I)=T(I)
1520      Y(I)=Vgs(I)
1530 NEXT I
1540 ALLOCATE Horiz(Npts),Verti(Npts)
1550 DIM Xlab$[20],Ylab$[20],Tit$[20],Dev$[20]
1560 INTEGER Axes_flag
1570 Axes_flag=1
1580 INPUT "X AXIS LABEL?",Xlab$
1590 INPUT "Y AXIS LABEL?",Ylab$
1600 INPUT "GRAPH TITLE?",Tit$
1610 INPUT "DEVICE NAME?",Dev$
1620 INPUT "X AXIS SCALE (LIN/LOG)?",X$
1630 IF X$<>"LIN" AND X$<>"LOG" THEN 1620
1640 INPUT "Y AXIS SCALE (LIN/LOG)?",Y$
1650 IF Y$<>"LIN" AND Y$<>"LOG" THEN 1640
1660 Line$="LINE"
1670 X1=X(1)
1680 X2=X(Npts)
1690 Y1=Y(1)
1700 Y2=Y(1)
1710 FOR I=1 TO Npts
1720      IF Y(I)>Y2 THEN Y2=Y(I)
1730      IF Y(I)<Y1 THEN Y1=Y(I)
1740 NEXT I
1750 GRAPHICS ON
1760 DEG
1770 Epsilon=1.E-13
1780 Typer:!
1790 IF X$="LIN" THEN
1800      IF X2<>0 THEN Mm=10^INT(LGT(ABS(X2)))
```

```
1810       IF X2=0 THEN Mm=0
1820       IF X1<>0 THEN Pp=10^INT(LGT(ABS(X1)))
1830       IF X1=0 THEN Pp=0
1840       IF Pp>Mm THEN Mm=Pp
1850       IF Mm=0 THEN Mm=1
1860       Xmin=INT(X1/Mm)*Mm
1870       Pp=INT(X2/Mm)*Mm
1880       Xmax=Pp+(ABS(X2/Pp-1)>Epsilon)*Mm
1890       IF Xmax=Xmin THEN Xmax=Xmin+1
1900       FOR J=1 TO Npts
1910        Horiz(J)=X(J)
1920        NEXT J
1930       END IF
1940 IF X$="LOG" THEN
1950       IF X1>0 THEN Xmin=INT(LGT(X1))
1960       IF X1<=0 THEN Xmin=INT(LGT(ABS(X2)/10))
1970       IF X2>0 THEN Mm=LGT(X2)
1980       IF X2<=0 THEN Mm=LGT(ABS(X2))
1990       Xmax=INT(Mm)+(ABS(Mm/INT(Mm)-1)>Epsilon)
2000       FOR J=1 TO Npts
2010        IF X(J)>0 THEN Horiz(J)=LGT(X(J))
2020        IF X(J)<=0 AND J>1 THEN Horiz(J)=Horiz(J-1)
2030        IF X(J)<=0 AND J=1 THEN Horiz(J)=Xmax
2040        NEXT J
2050       END IF
2060 IF Y$="LIN" THEN
2070       IF Y2<>0 THEN Mm=10^INT(LGT(ABS(Y2)))
2080       IF Y2=0 THEN Mm=0
2090       IF Y1<>0 THEN Pp=10^INT(LGT(ABS(Y1)))
2100       IF Y1=0 THEN Pp=0
2110       IF Pp>Mm THEN Mm=Pp
2120       IF Mm=0 THEN Mm=1
2130       Ymin=INT(Y1/Mm)*Mm
2140       Pp=INT(Y2/Mm)*Mm
2150       IF Y2=0 THEN
2160           Ymax=0
2170       ELSE
2180           Ymax=Pp+(ABS(Y2/Pp)-1>Epsilon)*Mm
2190       END IF
2200       IF Ymax=Ymin THEN Ymax=Ymin+1
2210       FOR J=1 TO Npts
2220        Verti(J)=Y(J)
2230        NEXT J
2240       END IF
2250 IF Y$="LOG" THEN
2260       IF Y1>0 THEN Ymin=INT(LGT(Y1))
2270       IF Y1<=0 THEN Ymin=INT(LGT(ABS(Y2)/10))
2280       IF Y2>0 THEN Mm=LGT(Y2)
2290       IF Y2<=0 THEN Mm=LGT(ABS(Y2))
2300       Ymax=INT(Mm)+(ABS(Mm/INT(Mm)-1)>Epsilon)
2310       FOR J=1 TO Npts
2320        IF Y(J)>0 THEN Verti(J)=LGT(Y(J))
2330        IF Y(J)<=0 AND J>1 THEN Verti(J)=Verti(J-1)
2340        IF Y(J)<=0 AND J=1 THEN Verti(J)=Ymax
2350        NEXT J
2360       END IF
2370 IF Axes_flag=0 THEN GOTO Plotpts
2380 GCLEAR
2390 Plotwindow:!_________________________
2400 Dx=(Xmax-Xmin)/8
2410 Dy=(Ymax-Ymin)/5
```

```
2420  Left=Xmin-Dx
2430  Right=Xmax+Dx/3
2440  Top=Ymax+Dy/3
2450  Bottom=Ymin-Dy
2460  WINDOW Left,Right,Bottom,Top
2470  CLIP Xmin,Xmax,Ymin,Ymax
2480 Drawaxes:!_______________________________
2490  Xtic=10^INT(LGT(ABS(Xmax-Xmin)))/10
2500  Ytic=10^INT(LGT(ABS(Ymax-Ymin)))/10
2510  LINE TYPE 1                                   ! DRAW AXES
2520  AXES Xtic,Ytic,Xmin,Ymin,10,10,5
2530  LINE TYPE 4                                   ! DRAW GRID
2540 IF X$="LIN" THEN
2550  Mm=Xtic*10
2560  FOR J=Xmin+Mm TO Xmax+Mm STEP Mm
2570   PENUP
2580   MOVE J,Ymin
2590   DRAW J,Ymax
2600   NEXT J
2610  END IF
2620 IF X$="LOG" THEN
2630  FOR I=Xmin TO Xmax
2640   FOR J=1 TO 9
2650    Over=LGT(J)+I
2660    MOVE Over,Ymin
2670    DRAW Over,Ymax
2680    NEXT J
2690   NEXT I
2700  END IF
2710 IF Y$="LIN" THEN
2720  Mm=Ytic*10
2730  FOR J=Ymin+Mm TO Ymax+Mm STEP Mm
2740   PENUP
2750   MOVE Xmin,J
2760   DRAW Xmax,J
2770   NEXT J
2780  END IF
2790 IF Y$="LOG" THEN
2800  FOR I=Ymin TO Ymax
2810   FOR J=1 TO 9
2820    Up=LGT(J)+I
2830    MOVE Xmin,Up
2840    DRAW Xmax,Up
2850    NEXT J
2860   NEXT I
2870  END IF
2880 Scaleaxes:!_______________________________
2890  CLIP OFF
2900  CSIZE 3
2910  LINE TYPE 1
2920  Mm=Xtic*10
2930  FOR J=Xmin TO Xmax+Mm STEP Mm
2940   MOVE J,Ymin
2950   LDIR 90
2960   LORG 8
2970   IF X$="LIN" THEN Mm=J
2980   IF X$="LOG" THEN Mm=10^J
2990   LABEL USING "MDE";Mm
3000   NEXT J
3010  Mm=Ytic*10
3020  FOR J=Ymin TO Ymax+Mm STEP Mm
```

```
3030   MOVE Xmin,J
3040   LDIR 0
3050   LORG 8
3060   IF Y$="LIN" THEN Mm=J
3070   IF Y$="LOG" THEN Mm=10^J
3080   LABEL USING "MDE";Mm
3090   NEXT J
3100 Titles:!_________________________________
3110  CSIZE 5
3120  MOVE (Xmax+Xmin)/2,Bottom
3130    LDIR 0
3140    LORG 4
3150    LABEL Xlab$
3160  MOVE Left,(Ymax+Ymin)/2
3170    LDIR 90
3180    LORG 6
3190    LABEL Ylab$
3200  MOVE (Xmax+Xmin)/2,Ymax
3210    LDIR 0
3220    LORG 1
3230    LABEL Tit$
3240  MOVE (Xmax+Xmin)/2,Ymax
3250    LDIR 0
3260    LORG 3
3270    LABEL Dev$
3280 Plotpts:!_________________________________
3290  CLIP ON
3300  LDIR 0
3310  LINE TYPE 1
3320  Plotflag=0
3330  PENUP
3340  FOR J=1 TO Npts
3350   IF Plotflag=1 AND Line$="LINE" THEN
3360       DRAW Horiz(J),Verti(J)
3370   END IF
3380   IF Plotflag=0 THEN
3390     Plotflag=1
3400     MOVE Horiz(J),Verti(J)
3410   END IF
3420   IF Line$<>"LINE" THEN
3430     MOVE Horiz(J),Verti(J)
3440       CSIZE 2
3450       LDIR 0
3460       LORG 5
3470       LABEL Line$
3480   END IF
3490   NEXT J
3500   DEALLOCATE X(*),Y(*),Horiz(*),Verti(*)
3510  SUBEND
3520  !
3530  !
3540  SUB Extract
3550  OPTION BASE 1
3560  COM /Mnos_data/ Preamble$[200],Header$[6]
3570  COM /Mnos_data/ Waveform(20,512)
3580  COM /Mnos_data/ Devicetype(1)
3590  COM /Mnos_data/ Comments$[30]
3600  COM /Points/ Vgs(20),T(20),Npts
3610  ALLOCATE Plotpts(512),Voltage(512)
3620  Wave=1
```

```
3630  Npts=0
3640  OFF KEY
3650  ON KEY 0 LABEL "LAST WAVEFORM",14 GOTO Decrease
3660  ON KEY 1 LABEL "NEXT WAVEFORM",14 GOTO Increase
3670  ON KEY 3 LABEL "STORE",14 GOSUB Keep
3680  ON KEY 9 LABEL "EXIT",14 GOTO Leave
3690  ON KEY 5 LABEL "SECTOR",14 GOTO Sector
3700  ON KNOB .1,15 GOSUB Nob
3710  N=POS(Preamble$,"YZERO")
3720  Offset=VAL(Preamble$[N+6,N+16])
3730  N=POS(Preamble$,"YMULT")
3740  Y_unit=VAL(Preamble$[N+6,N+16])
3750  GINIT
3760  GRAPHICS ON
3770  PRINT CHR$(12)
3780  Sector=0
3790 Graph: FOR I=1 TO 128
3800        Voltage(I+128*Sector)=Waveform(Wave,I+128*Sector)*Y_unit+Offset
3810        Plotpts(I+128*Sector)=(Waveform(Wave,I+128*Sector)+4)*12.5
3820  NEXT I
3830  GCLEAR
3840  MOVE 0,Plotpts(1+128*Sector)
3850  FOR I=2 TO 128
3860        Xplot=I
3870        Yplot=Plotpts(I+128*Sector)
3880        DRAW Xplot,Yplot
3890  NEXT I
3900  X=1
3910  Y=Plotpts(1+128*Sector)
3920  Oldx=1
3930  Oldy=Plotpts(1+128*Sector)
3940  GOSUB Cursor
3950  WHILE 1=1
3960        DISP "VOLTAGE=";Voltage(X+128*Sector),"  WAVEFORM #";Wave,"   SECTOR
#";Sector
3970  END WHILE
3980 Cursor:   !
3990  MOVE Oldx,Oldy+1
4000  PEN -1
4010  DRAW Oldx,Oldy+4
4020  Oldx=X
4030  Oldy=Y
4040  MOVE X,Y+1
4050  PEN 1
4060  DRAW X,Y+4
4070  RETURN
4080 Nob:     !
4090  Nobb=KNOBX
4100  IF Nobb>0 THEN
4110        X=X+1
4120     ELSE
4130        X=X-1
4140  END IF
4150  IF X<1 THEN X=1
4160  IF X>128 THEN X=128
4170  Y=Plotpts(X+128*Sector)
4180  GOSUB Cursor
4190  RETURN
4200 Increase:  X=1
4210  Wave=Wave+1
4220  IF Wave>20 THEN Wave=20
```

```
4230  Sector=0
4240  GOTO Graph
4250 Decrease:  X=1
4260  Wave=Wave-1
4270  IF Wave<1 THEN Wave=1
4280  Sector=0
4290  GOTO Graph
4300 Keep:  Npts=Npts+1
4310  Vgs(Npts)=Voltage(X+128*Sector)
4320  GRAPHICS OFF
4330  INPUT "TIME VALUE?",T(Npts)
4340  GRAPHICS ON
4350  RETURN
4360 Sector:   !
4370  Sector=(Sector+1) MOD 4
4380  GOTO Graph
4390 Leave:  DEALLOCATE Plotpts(*),Voltage(*)
4400  SUBEND
4410  !
4420  !
4430 SUB Load_store
4440 OPTION BASE 1
4450 COM /Mnos_data/ Preamble$[200],Header$[6]
4460 COM /Mnos_data/ Waveform(20,512)
4470 COM /Mnos_data/ Devicetype(1)
4480 COM /Mnos_data/ Comments$[30]
4490 COM /Points/ Vgs(20),T(20),Npts
4500 ALLOCATE Filename$[20],Msus$[20],Filetype$[10]
4510 OFF KEY
4520 ON KEY 0 LABEL "CATALOG",14 GOSUB Catalog
4530 ON KEY 5 LABEL "LOAD",14 GOSUB Load_data
4540 ON KEY 6 LABEL "STORE",14 GOSUB Store_data
4550 ON KEY 9 LABEL "EXIT",14 GOTO Leave
4560 LOOP
4570      DISP "PRESS KEY"
4580 END LOOP
4590 Catalog:DISP "LEFT OR RIGHT HAND DRIVE";
4600 INPUT Drive$
4610 IF Drive$[1;1]="L" THEN
4620      CAT ":INTERNAL,4,1"
4630    ELSE
4640      CAT ":INTERNAL,4,0"
4650 END IF
4660 RETURN
4670 Load_data:DISP "FILENAME";
4680 INPUT Filename$
4690 DISP "FILE TYPE (WAVEFORM OR CURVE)";
4700 INPUT Filetype$
4710 DISP "LEFT OR RIGHT HAND DRIVE";
4720 INPUT Drive$
4730 IF Drive$[1;1]="L" THEN
4740      Msus$=":INTERNAL,4,1"
4750    ELSE
4760      Msus$=":INTERNAL,4,0"
4770 END IF
4780 ASSIGN @File TO Filename$&Msus$;FORMAT OFF
4790 IF Filetype$[1;1]="W" THEN
4800      ENTER @File;Preamble$,Header$,Comments$,Devicetype(*),Waveform(*)
4810    ELSE
4820      ENTER @File;Comments$,Devicetype(*),Vgs(*),T(*),Npts
```

```
4830 END IF
4840 ASSIGN @File TO *
4850 RETURN
4860 Store_data:DISP "FILENAME";
4870 INPUT Filename$
4880 DISP "FILE TYPE (WAVEFORM OR CURVE)";
4890 INPUT Filetype$
4900 DISP "LEFT OR RIGHT HAND DRIVE";
4910 INPUT Drive$
4920 IF Drive$[1;1]="L" THEN
4930       Msus$=":INTERNAL,4.1"
4940    ELSE
4950       Msus$=":INTERNAL,4.0"
4960 END IF
4970 IF Filetype$[1;1]="W" THEN
4980       CREATE BDAT Filename$&Msus$,325
4990       ASSIGN @File TO Filename$&Msus$;FORMAT OFF
5000       OUTPUT @File;Preamble$,Header$,Comments$,Devicetype(*),Waveform(*)
5010       ASSIGN @File TO *
5020    ELSE
5030       CREATE BDAT Filename$&Msus$,2
5040       ASSIGN @File TO Filename$&Msus$;FORMAT OFF
5050       OUTPUT @File;Comments$,Devicetype(*),Vgs(*),T(*),Npts
5060       ASSIGN @File TO *
5070 END IF
5080 RETURN
5090 Leave:DEALLOCATE Filename$,Msus$,Filetype$
5100 SUBEND
```

APPENDIX E

ANALYTIC THEORY OF THE SWITCHING PROPERTIES OF MNOS MEMORY TRANSISTORS

MNOS transistors are physically similar to MOS transistors except the MNOS transistor contains an additional insulator, silicon-nitride, between the metal gate contact and the silicon-dioxide. See Figure E.1.

MNOS and MOS transistors also have identical electrical characteristics except one: For the MOS transistor, the threshold voltage is 'FIXED' at a set value during fabrication and cannot be altered by normal electrical means. In contrast, the threshold voltage of a MNOS transistor is 'VARIABLE' and can be readily changed by changing the amount of charge trapped at the silicon-nitride/silicon-dioxide interface. The MNOS drain current equation is, for the non-saturation region, $|V_{ds}|<|V_{gs} - V_t|$,

$$I_{ds} = \frac{\mu\varepsilon}{2}\left(\frac{w}{l}\right)\left[\frac{\varepsilon_n}{d_n} + \frac{\varepsilon_{ox}}{d_{ox}}\right]\left[2(V_{gs}-V_t)V_{ds}-V_{ds}^2\right] \tag{E.1}$$

and for the saturation region, $|V_{ds}|>|V_{gs}-V_t|$,

$$I_{ds} = \frac{\mu\varepsilon}{2}\left(\frac{w}{l}\right)\left[\frac{\varepsilon_n}{d_n} + \frac{\varepsilon_{ox}}{d_{ox}}\right](V_{gs}-V_t)^2 \tag{E.2}$$

The four modes of operation, ERASE, WRITE, READ, and INHIBIT are shown in Figures 1.2 and 1.3. The

amount of charge trapped, which is directly proportional to the threshold voltage, can be adjusted only by the application of a large potential (+25V) across the gate/channel junction. For a P-channel MNOS transistor, the write voltage (-25V) causes the low-conduction state corresponding to the logic 0 state, while the erase voltage (+25V) causes the high-conduction state corresponding to the logic 1 state. The idealized switching characteristics of MNOSTs is plotted in Figure E.2.

Using the terminology in Figure E.1, summation of potential gives

$$V_g = d_{ox} E_{ox} + d_n E_n + \phi_s + \phi_{ms} \tag{E.3}$$

where d_n and d_{ox} are the thickness of the nitride and oxide layers, respectively. Upon differentiation of (E.3) with a constant gate voltage, we have

$$\frac{\partial E_n}{\partial_t} = - \left(\frac{d_{ox}}{d_n}\right) \frac{\partial E_{ox}}{\partial_t} \tag{E.4}$$

Also, the current continuity equation yields

$$\varepsilon_{ox} \frac{\partial E_{ox}}{\partial t} + J_{ox} = \varepsilon_n \frac{\partial E_n}{\partial t} + J_n \tag{E.5}$$

Substitution of (E.5) into (E.4) gives

$$\varepsilon_{ox} \frac{\partial E_{ox}}{\partial t} \left(\frac{C_n}{C_g}\right) = J_n - J_{ox} = \frac{\partial Q_i}{\partial t} \tag{E.6}$$

where $C_n = \frac{\varepsilon_n}{d_n}$ and $C_g = \frac{C_{ox} C_n}{C_{ox}+C_n}$

ε_n and ε_{ox} are the dielectric permittivity of the nitride and oxide layers, respectively. Using the Taylor series to a first order approximation on the oxide current density yields the expression

$$\ln(J_{ox}) = \ln\left[J_{ox}(E_{oxo})\right] + \left[\left(\frac{\partial}{\partial E_{ox}} \ln(J_{ox})\right) \cdot (E_{ox}-E_{oxo})\right]_{J_{ox} = J_{ox}(E_{oxo})} \quad \text{(E.7a)}$$

or

$$J_{ox} = J_{ox}(E_{oxo}) \exp \left[\left(\frac{\partial}{\partial E_{ox}} \ln(J_{ox})\right) \cdot (E_{ox}-E_{oxo})\right]_{J_{ox}=J_{ox}(E_{oxo})} \quad \text{(E.7b)}$$

The above expression shows the oxide current density's exponential dependence on the electric field across the oxide.

Combining (E.6) and (E.7) gives

$$0 = \frac{\partial E_{ox}}{\partial t} + k_n + \frac{E_a}{t_s} \exp\left(\frac{E_{ox}-E_{oxo}}{E_a}\right) \quad \text{(E.8)}$$

having the solution

$$E_{ox}(t) = E_a \ln \left[1-(1+ \frac{E_a}{k_n t_s}) \exp(-tk_n/E_a)\right] + E_{oxo} \quad \text{(E.9)}$$

where

$$E_a = \frac{J_{ox}(E_{oxo})}{\left[\frac{\partial J_{ox}}{\partial (E_{ox})}\right]_{E_{ox}=E_{oxo}}}$$

is the switching field parameter dependent on E_{ox} and d_{ox},

$$t_s = \left[\frac{C_n \varepsilon_{ox}}{C_g} \frac{E_a}{J_{ox}(E_{oxo})}\right]$$

is the switching speed strongly dependent on E_{ox} through $J_{ox}(E_{ox})$, and

$$k_n = -\left(\frac{C_g}{C_n \varepsilon_{ox}}\right) J_n$$

is a constant dependent on the nitride insulator properties.

Now continuity of displacements gives

$$Q_i = \varepsilon_{ox} E_{ox} - \varepsilon_n E_n \tag{E.10}$$

Combining (E.10) and (E.3), and solving for the voltage across the oxide, obtaining

$$d_{ox} E_{ox} = V_{ox} = \frac{V_g - \phi_{ms} - \phi_s + Q_i/C_n}{(1 + C_{ox}/C_n)} \tag{E.11}$$

With the gate voltage constant, the change in the threshold voltage is defined as

$$\Delta V_t = -\left[\frac{Q_i(t) - Q_i(0)}{C_n}\right] \tag{E.12}$$

Equating (E.11), (E.12), and (E.9) yields

$$\Delta V_t = \frac{\varepsilon_{ox} E_a}{C_g} \ln\left[1 + \frac{1 - \exp(-tk_n/E_a)}{\dfrac{J_n}{J_{ox}(E_{oxo}) - J_n}}\right] \tag{E.13}$$

for $tk_n/E_a << 1$, we may expand the exponential function using McClauren Series as

$$\exp\left(\frac{-tk_n}{E_a}\right) = 1 - \left(\frac{tk_n}{E_a}\right) + \ldots \quad \text{(E.14)}$$

Therefore, the threshold change is

$$\Delta V_t = \left(\frac{\varepsilon_{ox} E_a}{C_g}\right) \ln\left[1 + \left(\frac{tk_n}{E_a}\right)\left(\frac{J_{ox}(E_{oxo}) - J_n}{J_n}\right)\right] \quad \text{(E.15)}$$

and for $t \quad t_s$

$$\Delta V_t = \left(\frac{\varepsilon_{ox} E_a}{C_g}\right) \ln\left[\frac{tk_n}{E_a} \; \frac{J_{ox}(E_{ox}) - J_n}{J_n}\right] \quad \text{(E.16)}$$

Differentiating (E.16) one obtains the slope of the switching characteristics below

$$\frac{\partial \Delta V_t}{\partial (\ln t)} = \frac{\varepsilon_{ox} E_a}{C_g} \quad \text{(E.17)}$$

For very large times, V_t reaches saturation (see Figure E.2) and (E.13) becomes

$$\Delta V_t(\text{sat}) = \left(\frac{\varepsilon_{ox} E_a}{C_g}\right) \ln\left[\frac{J_{ox}(E_{oxo})}{J_n}\right] \quad \text{(E.18)}$$

or, in general, the threshold window (E.16) may be written as

$$\Delta V_t = \frac{2.3\ \varepsilon_{ox}}{C_g}\left[(E_a^{+})\log\left(\frac{t_p^{+}}{t_s^{+}}\right) + (E_a^{-})\log\left(\frac{t_p^{-}}{t_s^{-}}\right)\right] \quad \text{(E.19)}$$

where the superscripts + and - refer to a positive V_G and a negative V_G, respectively.

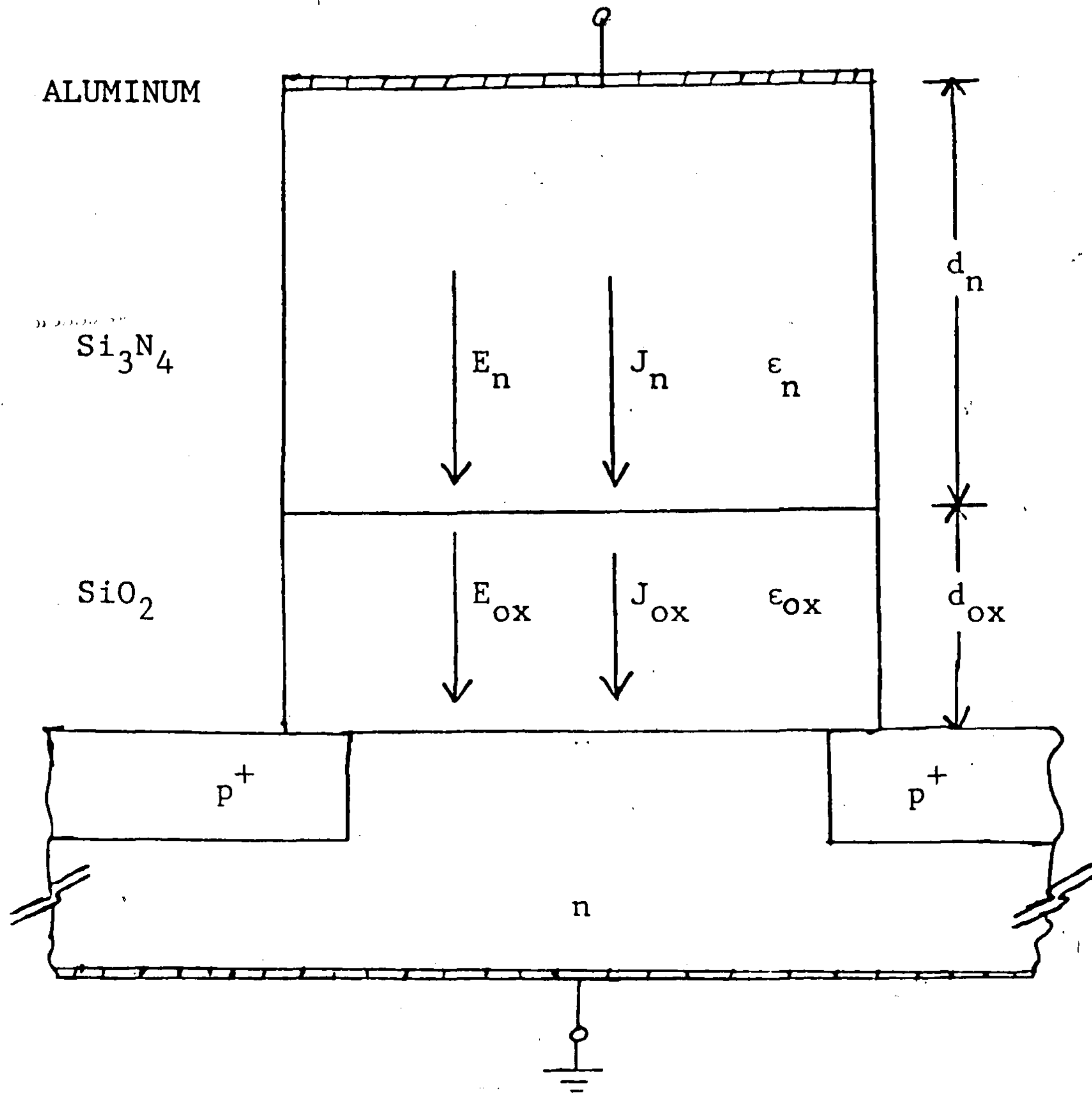


FIGURE E.1 DOUBLE INSULATOR SYSTEM OF MNOS MEMORY TRANSISTOR

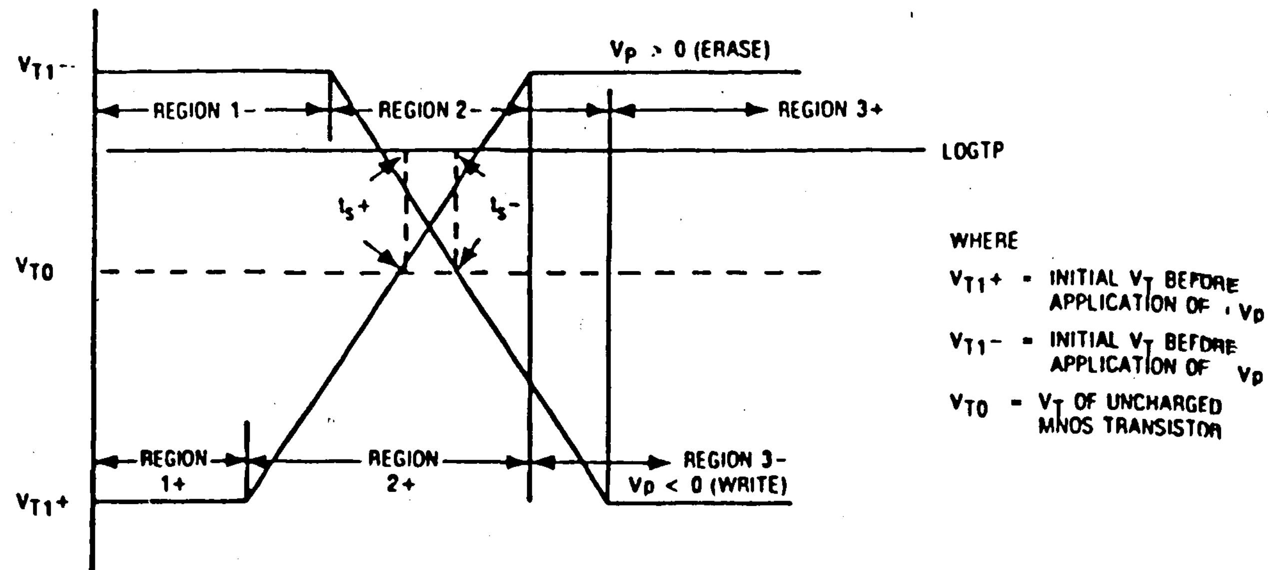


FIGURE E.2
IDEALIZED SWITCHING CHARACTERISTICS OF MNOS MEMORY TRANSISTORS

REFERENCES

1. Brown, W. D., "MNOS Technology--Will It Survive?" Solid State Technology, July, 1979, pp. 77-83.

2. Brunn, E., "The Influence of Nitride Thickness Variations on the Switching Speed of MNOS Memory Transistors," IEEE Trans. ED. vol. ED-25, No. 11, Nov., 1978, pp. 1328-1331.

3. Chang, J. J., "Nonvolatile Semiconductor Memory Devices," Proceedings of IEEE, vol. 64, no. 7, July 1976, pp. 1039-1059.

4. Cricchi, J. R., Blaha, F. C., and Fitzpatrick, M. D., "The Drain-Source Protected MNOS Memory Device and Memory Endurance," Int. Electron Dev. Mtg., Washington, DC, 1973, pp. 126-129.

5. Digital Storage Oscilloscope, The, Tektronix, 1982.

6. IEEE Standard Definitions, Symbols, and Characterization of Metal-Nitride-Oxide Field-Effect Transistors, IEEE Standard 581-1978.

7. Lampe, D. R., Fagan, J. L., Kub, F. C., White, M. H., Barth, D. A., Shutt, T. J., Charlge-Coupled Device (CCD) Boram Memory Techniques (Nonvolatile), Research and Development Technical Report, ECOM, 1974.

8. Libsch, F. R., 1984 (to be published).

9. Lundstrom, K. I., and Svensson, C. M., "Properties of MNOS Structures," IEEE Trans. ED, vol. ED-19, No. 6, June 1972, pp. 826-836.

10. Sze, S., Physics of Semiconductor Devices, 2nd ed., Wiley, 1981.

11. White, M. H., and Cricchi, J. R., "Characterization of Thin-oxide MNOS Memory Transistors," IEEE Trans. ED., vol. ED-19, no. 12, Dec. 1972, pp. 1280-1288.

12. White, M. H., Dzimianski, J. W., and Peckerar, M. C., "Endurance of Thin-oxide Nonvolatile MNOS Memory Transistors," IEEE Trans. ED, vol. ED-24, no. 5, 1977, pp. 577-580.

13. Wiker, R. L., Nondestructive Endurance Test Methodology for Nonvolatile Semiconductor Memories, Research and Development Technical Report, ERADCOM, August, 1982.

14. Wolfe, E. R., "Silicon Integrated Circuits," edited by Kahng, D., in Applied Solid State Science, Academic Press, 1981.

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