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**STRATEGIES FOR IMPLEMENTING
IN-PROCESS TESTING**

by

Ted D. Steigerwalt

A Thesis

Presented to the Graduate Committee

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1984

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ABSTRACT

This thesis deals with the placement of testing in the production line for electronic products. Described in this paper are the methodologies and strategies to be used in determining the need for testing at the various assembly levels. Both quality (instantaneous) and reliability (burn-in) testing are analyzed, along with their effects on the yield and costs of the product. A model has been developed which relates the yield and costs of the manufactured units to their incoming component quality and cost. The per unit cost equations of the model can be used to determine if a test facility should be added to or removed from a production line. Furthermore, additional cost equations are developed which aid in analyzing the effects of adding rework capabilities to a present test facility.

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1. INTRODUCTION

Many times in-process testing is performed on electronic devices without really knowing the effects that it may have on the cost and quality of the product. Test strategies are required which allow the test engineer to calculate these effects. The methodologies which can be used when determining the need for a given test facility will be described. A yield model, which was developed for integrated circuit chips, is extended to determine the product yield based on the quality and quantity of the component parts used in each sub-assembly. The cost of each sub-assembly must reflect the costs of any units which fail the testing, due to defective components, as determined by the yield.

A manufacturing production model will be developed which represents each stage of assembly and testing. The theory of the model can be extended as required in order to map the processing and testing steps of the particular production line which is to be investigated. The effects of including rework capabilities at a present testing facility are also analyzed. The per unit costs of a test station without rework capabilities is compared with the costs of a test station with rework

capabilities. Following are brief discussions on the efficiency of the test station based on the fault (test) coverage and sample testing.

Finally, product reliability is addressed with an Infant Mortality Model. Using the model which is based on the Weibull distribution the effects of product burn-in can be analyzed along with its cost effectiveness.

2. YIELD MODEL

In order to estimate the product quality and testing costs a yield model will be used. The yield is defined as the percentage of manufactured product which contains no defects. Wafer defects, according to Murphy (Ref. 11), can be divided into three categories. The categories contain area, line and point defects.

Area defects affect the entire wafer and include such defects as broken wafers, incorrect diffusions and mask misorientations. The number of broken wafers is assumed negligible. The remaining types of area defects are due to gross misadjustments of the production machinery and will affect the entire lot. Since the yield during these misadjustment periods will be very low, the situation will be corrected when it occurs in order to avoid large losses of product. One

can assume that these defects have been removed from the population. Chip failures caused by line defects are clustered and affect specific areas of the wafer. Line defects include such defects as wafer surface scratches, tweezer marks and defects due to improper handling. Assuming that care is taken when handling the wafers, the number of line defects becomes negligible. The point, or spot, defects are most critical to the yield model. These defects occur in highly localized regions of the wafer and are assumed to be randomly distributed throughout the wafer.

As shown in Sze (Ref. 15), the yield is dependent on the average defect density (D_0) and the chip area (A). The binomial distribution is used to distribute the n defects among N chips on a wafer. Approximating the binomial distribution with the Poisson distribution yields

$$P(x,u) = \frac{e^{-u} u^x}{x!} \text{ for } x=0,1,2,\dots$$

where X is the random variable for the number of defects on a chip. The average number of defects per chip (u) is equal to the defect density multiplied by the chip area. Thus, the probability of zero defects per chip is

$$P(0, u) = P(0, DoA) = e^{-DoA}$$

and the average yield is

$$Y = Y_0 \cdot Y_1 = Y_0 \int e^{-D \cdot A} f(D) dD$$

where $1 - Y_0$ is the fraction of chips which are failures due to processing (e.g. perimeter chips, test sites) and Y_1 is the percentage of the remaining chips which contain no defects. The calculation of yield is dependent on the defect probability density function ($f(D)$) chosen. Typically, this function is assumed bell shaped and can be approximated by a triangular function. Further refinements to the model (Ref. Sze) show that the gamma function is more appropriate because of the ability to fit the curve by varying the average defect density and the shape parameters. For simplification the signum function located at Do will be assumed. Therefore, the average yield equation becomes

$$Y = Y_0 \cdot e^{-DoA} = Y_0 \cdot e^{-u}$$

This equation can be used to estimate the yield at all assembly levels by assuming that the critical defects are randomly distributed throughout the population. By setting Y_0 equal to one, Y represents the effective

yield, or the ratio of good units to possible good units.

3. TESTING

Product testing can be categorized into two types. The first type, screen testing, is applied to 100% of the product. Devices which fail screen testing are removed from the population with the assumption that the remaining product consists of only good devices. The second type of test, the sampling test, is a predictive test. This test is performed only on a small sample of the product with the hopes of predicting the quality of the remaining product. Although sample testing does not remove all of the failures from the population, it is sometimes cost effective when used to determine the need for screen testing. The manufacturing process has many opportunities where testing can be implemented. It is important to develop a test strategy which produces an economic balance between quality and costs. The equations which will be used to determine the placement of product testing will first be developed for a single test and extended to the production environment where multiple tests can be performed .

SINGLE TEST YIELDS

Consider a production line with one screen test performed on the completed product. The manufactured devices will have an average of x defects per device. The incoming quality of the devices to the test station as predicted by the yield model is

$$Y_i = e^{-x}$$

which corresponds to a product quality level in percent defective of

$$PQL_i = 1 - Y_i = 1 - e^{-x}$$

This relationship between the PQL and the yield is shown in Figure 1. Ideally, the screen test should remove all of the defective devices from the population. However, since the fault coverage of the screen test is not 100% some of the bad devices will pass the test. Note also that some of the good devices will fail if the test limits are guardbanded (tightened beyond the specification). The effects of fault (test) coverage on the yield will be discussed later in this paper.

TESTING COSTS

The total production cost is equal to the sum of

the manufacturing and testing costs. For the purpose of this paper the manufacturing costs, which include fabrication, packaging and assembly costs are assumed constant. The testing costs can be further divided into capital expenses and operating expenses. The operating expenses include the wages of the equipment operators and maintenance personnel required to maintain the integrity of the system.

Assuming that the time to test good devices is equal to the time to test failures, then

$$t_{test} = t_t + t_h$$

where t_{test} = average time to test each device

t_t = actual time to conduct the test

t_h = handling time required to remove the device from the test position and insert a new device.

Note that the average test time for each device may be dependent on the test coverage. The quantity of good devices entering the test station will be equal to the quantity of good devices leaving the test station. Since some of the assembled devices will be removed during testing, the quantity of devices which must be tested will be larger than the quantity which leave the test station. Letting N_{in} represent the quantity of devices which must be tested

$$N_{in} \cdot Y_i = N_o \cdot Y_o$$

$$N_{in} = N_o \cdot Y_o / Y_i$$

where $N_{in}(N_o)$ = quantity of devices entering
(leaving) the test station

$Y_i(Y_o)$ = percentage of devices entering
(leaving) the test station which are
good.

The capacity of the test station is determined by dividing the available test time by the average time to test each device. The available test time must take into account the down time of the tester due to system failure as well as periodic maintenance and calibration.

$$\text{tester capacity} = \frac{(1 \text{ year}) \cdot (K)}{t_{\text{test}}}$$

where K = tester availability ($0 < k < 1$)

t_{test} = average time to test each device

Since the test station must also test the devices which fail, the capacity of the station in terms of passing devices must be reduced by the ratio Y_i/Y_o to yield an effective tester capacity.

The test system cost shall be divided equally over its life expectancy. This life expectancy is typically 5 years at which point the system becomes obsolete and

is in need of major reconfiguration. Assuming the test facility can be used on other product families, the cost to test each device is

$$\frac{\text{test cost}}{\text{device}} = \frac{(\text{system} + \text{maintenance} + \text{operator cost}) \text{ per year}}{\text{effective capacity per year}}$$

4. PRODUCTION MODEL

A model will be developed which relates the cost of in-process and final testing to the quality of the individual parts or components used in the electronic unit. The electronic unit is dependent on the system definition and can vary from a packaged integrated circuit chip to a complex system. Individual component parts include wafers, leadframes and packages for the devices and devices and circuit packs for the larger systems. By using the model one can analyze the economic effects of adding or removing in-process testing from the assembly line. Note that this model assumes that any testing done at the current level of assembly only tests for defects which are injected within the level. Therefore defects located one or more levels down will be transparent to the model and will be accounted for in the number of incoming defective components of the product. The manufacturing line can be viewed as a tree structure divided into

subsystems at each level of assembly or node. (Figure 2).

ANALYSIS OF ASSEMBLY LEVEL NODES

The costs and quality levels will be investigated at each node. The theory can be repeated to build a tree which represents the assembly process from the raw materials to the completed system. Testing is performed at various levels in order to attempt to separate the good devices from the failures.

Referring to Figure 3, N_{in} equals the total number of units which must be assembled in order to produce N_o units. Let n_i represent the number of the i th type of component which are required during assembly of each electronic unit at the node. The respective quality of these incoming parts is Q_i fractional defective. Therefore, the average number of defective component parts which will be assembled into the each unit is equal to the sum of the products of the quality and quantity of each type of incoming part used in the unit. This represents the average number of defects per unit due to the quality of the incoming components at the assembly step.

$$x_c = \sum_i n_i \cdot Q_i$$

At each assembly level a percentage of defects will be injected into each device by the manufacturing process. Adding the average number of defective components used in each unit to the average number of defects per unit injected by the assembly process yields the average defects per device.

$$x = x_m + x_c = x_m + \sum_i n_i \cdot Q_i$$

where x = average number of defects per unit

x_m = average number of defects injected by the manufacturing process per unit

x_c = average number of incoming defective components per unit

The quality of the outgoing units is equal to the yield. An estimate of the yield can be predicted using the yield model described earlier in this paper. Therefore, the quality in percent defective as a function of the quality of the incoming component parts and manufacturing defects is estimated using the Poisson approximation of the binomial distribution as

$$Q = 1 - Y$$

$$Y = e^{-x} = e^{-(x_m + x_c)} = e^{-(x_m + \sum_i n_i \cdot Q_i)}$$

Using this representation for yield, the relationships for the costs and quantities of the assembled units can

be derived for each node. If no testing is implemented at the particular node, then the equations above can be used as an estimate of the outgoing quality level at that node.

Since none of the units are removed from the population the number of units produced and assembled at the node will include both the good devices and the failures. Therefore,

$$N_o = N_i$$

The per unit cost to produce these N_o devices is equal to the sum of the incoming component costs and the assembly costs per device. Thus,

$$C_t = \underbrace{\sum_i n_i \cdot c_i}_{cc} + c_m$$

where C_t = total cost per unit

cc = component parts cost per unit

c_m = assembly cost per unit

c_i = cost of the i th component

SINGLE TEST STATION

The next step in developing the model is to consider a test station at the node. This station effectively separates the good devices from the

defective ones as shown in Figure 4.

The assumption has been made that those devices which fail the test will be considered junk and will be removed from the population. Assuming that the test coverage at the test station is 100 percent, the yield equation determines the proportion of units which will pass the test. Less coverage would be more realistic and will be investigated later in this paper. Analogously, the quality equation determines the quantity of units which will fail the testing. Therefore, the quantity of good units produced ($PQ_{Lo}=0$) is

$$N_o = N_{in} \cdot Y = N_{in} \cdot e^{-(x_m + \sum_1 n_i \cdot Q_i)}$$

and the quantity of junk units is

$$N_j = N_{in} \cdot Q = N_{in} \cdot (1 - Y) = N_{in} \cdot (1 - e^{-(x_m + \sum_1 n_i \cdot Q_i)})$$

The cost to produce N_o units now will include testing costs (ct per unit) as well as the assembly costs (cm per unit) for the N_{in} units. Note that the costs of testing the failures now must be absorbed in the cost of the good units since the junk devices are removed from production. The costs of assembly and testing is linearly dependent on the quantity of product which must pass through the test station. The

cost per unit to assemble the devices becomes

$$\begin{aligned}C_t &= \left(\sum_1 n_i \cdot c_i + c_m + c_t \right) N_{in}/N_o \\&= \left(\sum_1 n_i \cdot c_i + c_m + c_t \right) / Y \\&= \left(\sum_1 n_i \cdot c_i + c_m + c_t \right) / e^{-(x_m + \sum_1 n_i \cdot Q_i)}\end{aligned}$$

for a single test station and no reworking of the failed devices.

SINGLE TEST STATION WITH REWORK

Developing the model still further, consider a node where the defective units can be reworked. Assume that the efficiency of the rework is 100 percent, that is all defective units can be replaced and the assembly defects are correctable without replacement of any components. Following the rework the units shall be retested once. Those units which pass the retest will be added to the good unit population while the failures will be considered junk. Note that the retest will be the same test as was conducted in the initial unit testing. Figure 5 shows the product flow diagram that now exists.

The quantity of units which were considered junk in the single test station scheme will now pass through the rework station and be retested. Replacement parts,

which have the same percent defective as the component parts used in the initial assembly process, are used to replace those components which were defective in the failed devices. The percentage of devices which pass the retest after reworking are again estimated using the yield model. The quantity of component parts which must be replaced is equal to the quantity of defects which were used in the initial assembly. Multiplying the quantity of replacement parts required by the fractional defective for each type of component used yields the average number of incoming defects per reworkable unit.

$$\begin{aligned}
 x_c' &= \underbrace{N_{in} \cdot \sum_i n_i \cdot Q_i \cdot Q_i}_{\text{quantity of defective components}} / N_{in}' \\
 &= \sum_i n_i \cdot Q_i^2 / \{1 - e^{-(x_m + \sum_i n_i \cdot Q_i)}\}
 \end{aligned}$$

where $N_{in}' = N_{in} \cdot (1 - Y)$

During reworking some additional defects which will be injected. The sum of the defective replacement parts and the rework defects yield the average defects per reworkable unit.

$$x' = x_c' + x_m' = x_m' + \sum_i n_i \cdot Q_i^2 / \{1 - e^{-(x_m + \sum_i n_i \cdot Q_i)}\}$$

where x' = average number of defects per reworked unit

xm' = average number of defects injected by the rework process per reworked unit

xc' = average number of defective components per reworked unit

The yield of the reworked units is

$$y' = e^{-\{xm' + \sum_i n_i \cdot Q_i^2 / (1 - e^{-(xm + \sum_i n_i \cdot Q_i)})\}}$$

The quantity of good units ($PQ_{Lo}=0$) leaving the node is equal to the sum of the units which passed the initial testing plus the units which passed the rework testing. The remaining units (units which failed both the initial and rework testing) will be considered junk at this point.

$$N_o = N_{in} \cdot Y + N_{in}' \cdot Y' \quad (\text{good product})$$

$$= N_{in} \cdot [Y + (1-Y) \cdot Y']$$

$$N_j = N_{in} \cdot (1-Y) + N_{in}' \cdot (1-Y') \quad (\text{junk product})$$

$$= N_{in} \cdot (1-Y) + N_{in} \cdot (1-Y) \cdot (1-Y')$$

$$= N_{in} \cdot (1-Y) \cdot (2-Y')$$

Included in the cost of the N_o units are the costs of initial assembly and testing of N_{in} devices plus the

costs of reworking and retesting of the failed devices along with the costs of the components used in the assembly and rework. Thus the cost per unit would be

$$C_t = \frac{(\sum n_i \cdot c_i + c_m + c_t + \sum n_i \cdot Q_i \cdot c_i) N_{in} + (c_m' + c_t') \cdot N_{in} \cdot (1-Y)}{N_o}$$

$$= \frac{\sum n_i \cdot c_i + c_m + c_t + \sum n_i \cdot Q_i \cdot c_i + (c_m' + c_t') \cdot (1-Y)}{Y + (1-Y) \cdot Y'}$$

where c_m = assembly costs per unit

c_m' = rework costs per unit

c_t = testing costs per unit

c_t' = retesting costs per unit

c_i = cost of the i th component

USING THE MODEL

Many times the decision must be made whether or not to add or remove a test station from a current production line. Using the model which has been developed a good engineering estimate of the outcome can be made. In order to use the model one must draft a picture of the production line in a tree format which defines the manufacturing and testing flow of the product. The nodes must be chosen such that the quality of the components entering each node is known, presumably by prior testing of the components. The

node referring to the test station must be defined. When considering the addition of a test station a node must be added along the path between two nodes where the addition is desired. The strategy for determination of the test system need is as follows.

1. A test facility addition should be investigated on paths where the quantity of one incoming component is much lower than the quantity of the remaining incoming components. The possible benefit is to minimize the quantity of units which must be scrapped due to the defects caused by a normally weak component. This is extremely beneficial if the costs of the components with the better quality are much larger than the lower quality component costs.

2. A test facility removal shall be considered if the yield is very high at the particular node and minimal rework is performed. The philosophy here is that the removal of defective units at a higher assembly level could cost less to the production line. Also, if the number of defectives entering the current test station

is low, the number of defective units which enter the next may be low enough to warrant removal of the test facility from the line.

Estimation of the benefits of having a rework facility attached to a present test station is accomplished by comparing the cost per unit functions for the two configurations. The breakover point is determined by equating the two cost functions. Therefore,

$$C_t \text{ (without rework)} = C_t \text{ (with rework)}$$

$$\frac{\sum n_i \cdot c_i + c_m + c_t}{Y} = \frac{(\sum n_i \cdot c_i + c_m + c_t) + \sum n_i \cdot Q_i \cdot c_i + (c_m' + c_t') \cdot (1-Y)}{Y + (1-Y)Y'}$$

$$\frac{\sum n_i \cdot c_i + c_m + c_t}{Y} = \frac{\sum n_i \cdot Q_i \cdot c_i / (1-Y) + c_m' + c_t'}{Y'}$$

$$\frac{\text{per unit assembly costs}}{\text{initial test yield}} = \frac{\text{per unit rework costs}}{\text{retest yield}}$$

As the ratio of the assembly costs to initial test station yield becomes larger than the ratio of rework costs to retest yield the per unit cost of a test station without rework becomes larger than the test facility with rework capabilities. Thus, by comparing these two ratios with each other one can determine which scheme would be more cost effective.

TEST COVERAGE

As alluded to earlier in this paper, realistically the test coverage is not 100 percent. Therefore, there are some defects which will go undetected to the next process step or be incorporated into the finished product. The test coverage (E) will be defined as the percentage of defects which are detected. Since some of the defects are undetected at the test station there will be a variance between the observed yield (Yo) and the actual yield (Ya).

$$Y_o > Y_a$$

Some of the units which pass the testing will actually be defective. The ratio of defective units to the total number of units produced is equal to the product quality level (PQLo) in percent defective. The PQLo from a particular test station is computed using the following equations.

$$\begin{aligned} \text{PQLo} &= \frac{\text{defective units}}{\text{total units}} \\ &= \frac{Y_o - Y_a}{Y_o} = 1 - Y_a/Y_o \\ &= 1 - e^{-x}(1 - E) \end{aligned}$$

where x = average number of defects per unit assembled

E = test set coverage

As the test coverage (E) is varied from zero to 100 percent the PQLo varies between PQLi and zero. The sign of the exponent will always be negative provided $E \neq 0$. Therefore, as the defect density is varied from zero to infinity the PQLo will vary between zero and one. Note that the equation for PQLo is only dependent on the quality of the incoming components and the defects injected by the manufacturing process and does not take into account the human factors involved which may cause product to enter the population without being tested. The effect of test coverage is seen mostly at the last assembly level before product shipment.

5. SAMPLE TESTING

The product quality of conformance is a measure of how well the "quality characteristics of a product corresponds to those really needed to secure the results intended by the designer" (Ref. 6). The three alternatives for testing the product are no inspection, sampling inspection and 100% inspection (product screening). The object is to find an economic balance between the product quality and the inspection costs which are incurred. By choosing the type of inspection and the quantity of devices to be sampled one can

minimize the overall product costs and still meet the quality objectives. The product costs which are incurred include the production costs, acceptance costs and unsatisfactory-product costs. The production costs are the costs required to manufacture the device. In order to assess the quality of the manufactured product, testing and inspection must be performed and this accounts for the acceptance costs. Some of the product which is accepted will contain defective product which will account for the unsatisfactory product costs since this product cannot be used. These unsatisfactory product costs will include the down time and the cost to repair the system or board where the device is inserted.

The most economical approach to take when the PQL is consistently low and does not fluctuate is not to sample the product. Under these conditions the costs required to screen the product are larger than the potential unsatisfactory-product cost savings. When the PQL is consistently high and steady then the most economical approach would be to test 100% of the product and remove that product identified as defective.

Note that sampling inspection can not separate good lots from bad lots when the quality is consistent.

However, sampling inspection has the ability to remove freak lots from the populations which are not consistent in quality. Sampling inspection is warranted when the PQL is normally low enough that no inspection would be the most economical, and occasionally high enough that a 100% inspection is the most economical.

In order to determine which type of sampling best fits one's needs an initial quality level must be assumed. As the quality of the product is improved and become more consistent, alternative sampling plans must be considered which sample less of the product. Every time a different sampling plan is implemented the manufacturing costs, acceptance costs and unsatisfactory-product costs must be reevaluated. The final results should yield a better quality product at the lowest possible cost.

Suppose the quality of the devices is better than required. Ideally, the most economical approach would be to sample no product and realize a savings equal to the testing costs. Realistically, all of the product will not have the same number of defects and variations will be seen due to the fluctuations in the manufacturing process. Thus, some sampling of the product should be done to assure that the product with

the higher number of defects is not shipped. Also, sampling will flag any drifts in the calibration of the manufacturing equipment which might be detrimental to the overall PQL.

A sampling plan can be defined by choosing the sample size and the acceptance number. The acceptance number is the maximum allowable number of defective devices which will be accepted in the sample. Sampled lots which exceed this acceptance number are rejected from shipment and must be either reworked or junked. As the quality of the product becomes worse a larger proportion of the product will be rejected. The probability of accepting a lot is determined by the Operating Characteristic (OC) curve for the chosen sampling plan.

CALCULATION OF THE OC CURVE

The probability of accepting a given lot can be calculated using the Hypergeometric, Binomial or Poisson distributions. Assuming a Poisson distribution, which is widely accepted in the industry, the probability of acceptance is

$$P(\text{accept}) = F(c; np) = \sum_{k=0}^c e^{-np} np^k / k!$$

where c = acceptance number

n = sample size

p = % defective product in the lot

Values for these probabilities have been tabulated and can be found in Poisson Distribution Tables.

As the sample size is increased the curve becomes steeper allowing a greater separation between the good and defective product. Increasing the acceptance number will shift the curve to the right. See Figure 6. Inherent in all sampling plans is the producer's risk. This is the probability of rejecting a lot when its quality is acceptable.

6. RELIABILITY AND INFANT MORTALITY

Shown in Figure 7 is the bathtub curve which is commonly used in the electronics industry when representing product reliability. This curve shows the failure rates of a population of manufactured units as a function of time. The curve can be divided into three periods. The decreasing failure rate which occurs during the infant mortality period is caused by "weak" units among the population which tend to fail early in their lifetimes. These failures are typically caused by manufacturing defects which pass the instantaneous test of the factory, which was described earlier, but fail when the product is put into

operation in the field. Following the infant mortality period is the "steady state" period. During this period of time the failure rate remains relatively constant. The failures which occur during the steady state period are usually random in nature since failures due to a single cause would be more likely to occur at about the same period of time. As time is increased the wearout period is entered. This period is characterized by an increasing failure rate. At this point the number of units which are still functioning decreases rapidly. The wearout period is of little concern to electronic product manufacturers since this period of time is beyond the useful life of the units.

The infant mortality period is of most concern to the product user. This period typically lasts for the first ten thousand hours of operation. The manufacturer can attempt to remove the weak units through burn-in in order to increase their reliability.

The effects can be described using the Weibull Model of the infant mortality period. The advantage of using the Weibull Distribution is that it can be made to fit most distributions of product by choosing the parameters. The Weibull Failure Rate Function (See Figure 8) is

$$\lambda_{inst} = \lambda_1 \cdot t^{-\alpha}$$

where λ_1 = instantaneous failure rate after 1 hour of operation

t = operating time

α = shape parameter for Weibull Model

Integrating this equation from zero to 10,000 hours yields the percent of units which are expected to fail during during that time period, the infant mortality period.

Many electronic equipment suppliers choose to approach the problem of infant mortality with burn-in. By increasing the temperature at which the units are operated, the effective operating time elapsed can be accelerated. The degree of acceleration is predicted using the Arrhenius Temperature Acceleration Model defined by the following equation (Ref. 14).

$$A = t_n/t_{bi} = e^{\frac{E_a}{k} \left[\frac{1}{T_n} - \frac{1}{T_{bi}} \right]}$$

where t_n = operating time at normal operating temperature

t_{bi} = operating time at burn-in temperature

T_n = absolute operating temperature

T_{bi} = absolute burn in temperature

E_a = activation energy in electron volts

k = Boltzman constant

By conducting the burn-in test at elevated

temperature, failures occurring during the infant mortality period can be realized in a shorter period of time. This increases the availability of the test system for testing of additional product.

The cost of the test facility can be divided equally over its life expectancy of 5 years as before. The cost to test each unit will be determined by the number of devices which can be tested in one year, testing capacity. The maximum test time available is determined by its availability (K). Taking into account the acceleration factor and integrating from zero to the burn-in time yields the percent defective which will be detected.

$$\begin{aligned} \text{percent detected} &= \int_0^{t_{bi}} \lambda_1 \cdot (A t)^{-\alpha} dt \\ &= A \frac{1-\alpha \cdot \lambda_1 \cdot t^{1-\alpha}}{1-\alpha} \Bigg|_0^{t_{bi}} \end{aligned}$$

Multiplying the percent detected by the number of units tested yields the number of failed units which will be prevented from entering the field. The cost of performing the burn-in must be compared with the savings which is realized by not having to repair these failures in the field. This field repair cost will not include the cost of the units. Using the Weibull distribution one can determine the failures which are

not removed and which will occur during the remaining infant mortality period, up to the ten thousand hours of operation. Multiplying this number by the repair costs for each failure in the field represents the potential savings which can be realized. Using this technique it can be determined if the implementation of burn-in on a particular product line is cost effective.

7. SUMMARY

A production testing model has been presented which relates the manufacturing cost for an electronic product to the quantity and quality of the incoming components used in the unit. The model can be used to strategically place product testing within the production line through careful analysis of the economic effects. The basis for the model is a yield model developed for integrated circuits. Quality data of incoming components are estimated by quality control and assurance organizations. The primary result of the model is a cost estimate as a function of incoming component quality and testing parameters. The model assumes that all defective components will be randomly distributed throughout the population of completed product. The yield of the product is exponential with respect to the average number of defects which are

injected into the assembly process by defective components and processing errors.

The production line can be mapped into a tree format with assembly and testing conducted at the nodes. Yield equations have been developed for three testing configurations which can occur at each node.

- 1) No testing
- 2) Testing without rework capabilities
- 3) Testing with rework capabilities

A comparison of the defect configurations can be made using the manufacturing cost equations for each good unit produced. The cost of the defective units are added to the good unit costs. In order to determine the need for rework a comparison of the assembly costs/initial test yield and the rework costs/retest yield must be made. The outgoing quality of the product is a function of the test coverage, or effectiveness.

Burn-in is widely accepted in the electronics industry as an effective method of addressing component reliability. In order to estimate the cost effectiveness, the Weibull Failure Rate Model is used to predict the quantity of defective product which is

removed by burn-in. Comparing the cost to remove these failures through burn-in with the repair costs incurred if the product had entered the field yields the benefits of the burn-in.

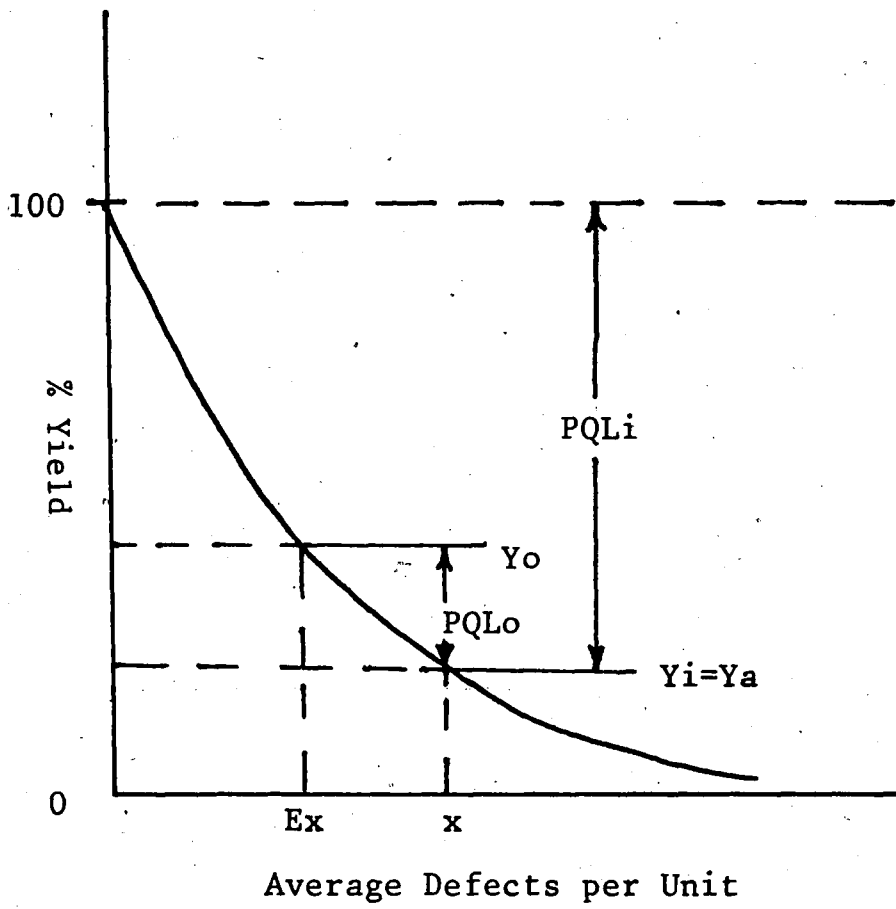


Figure 1. Relationship between the product quality levels and yields.

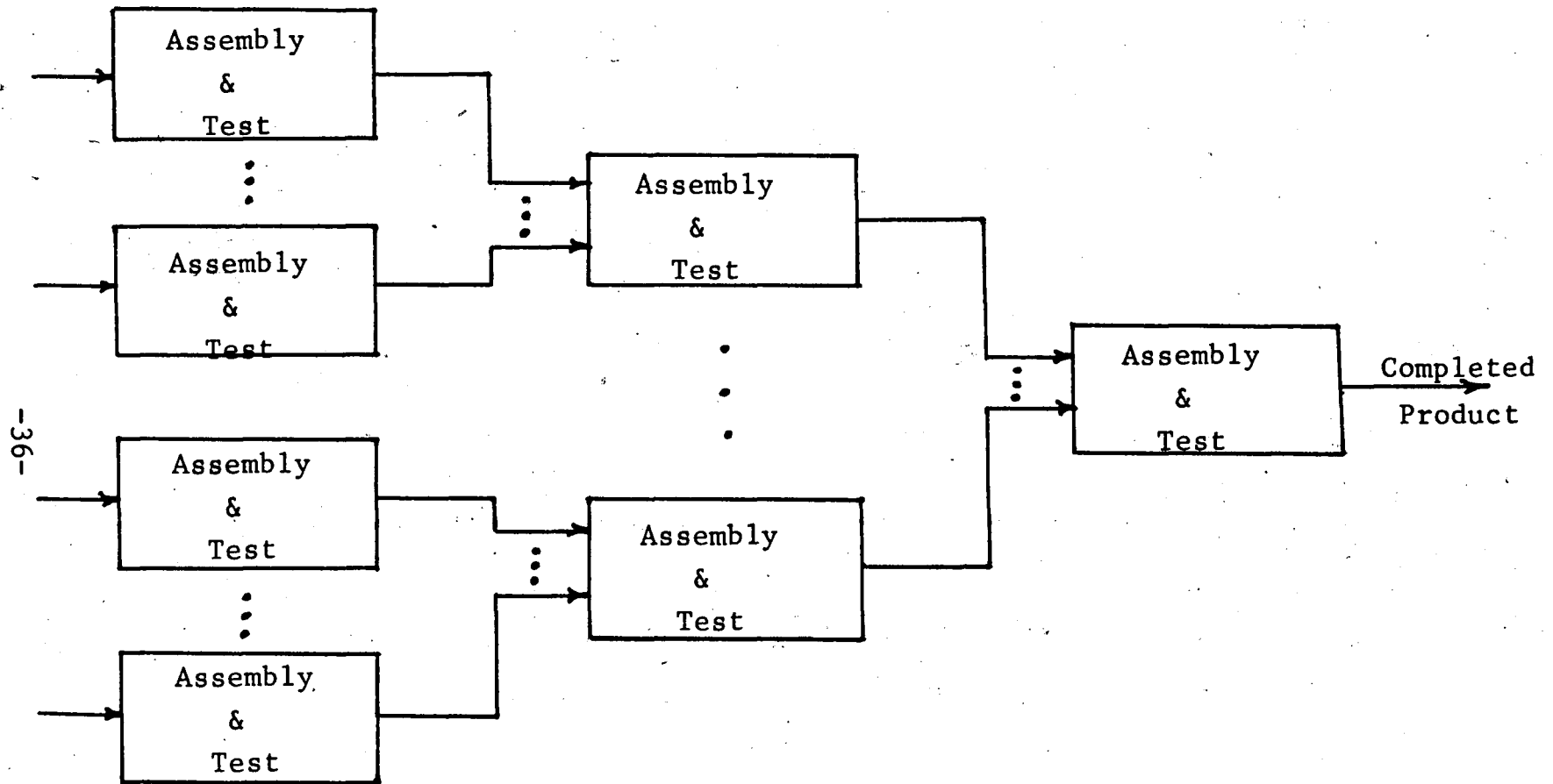


Figure 2. Tree structure used for production model.
Nodes represent various assembly levels.

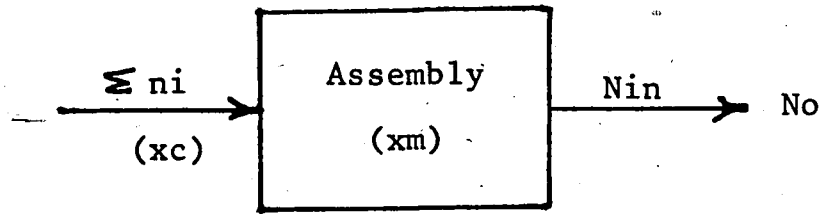


Figure 3. Representation of an assembly level node with no testing.

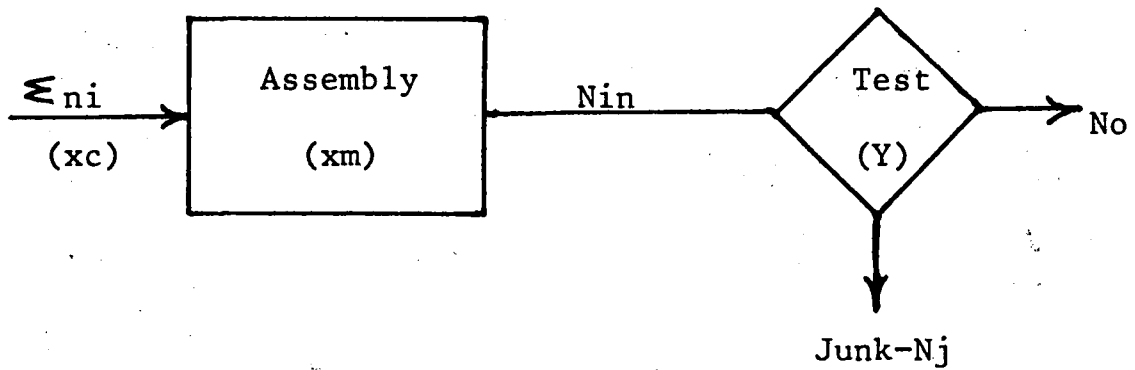


Figure 4. Representation of an assembly level node with testing and no rework capabilities.

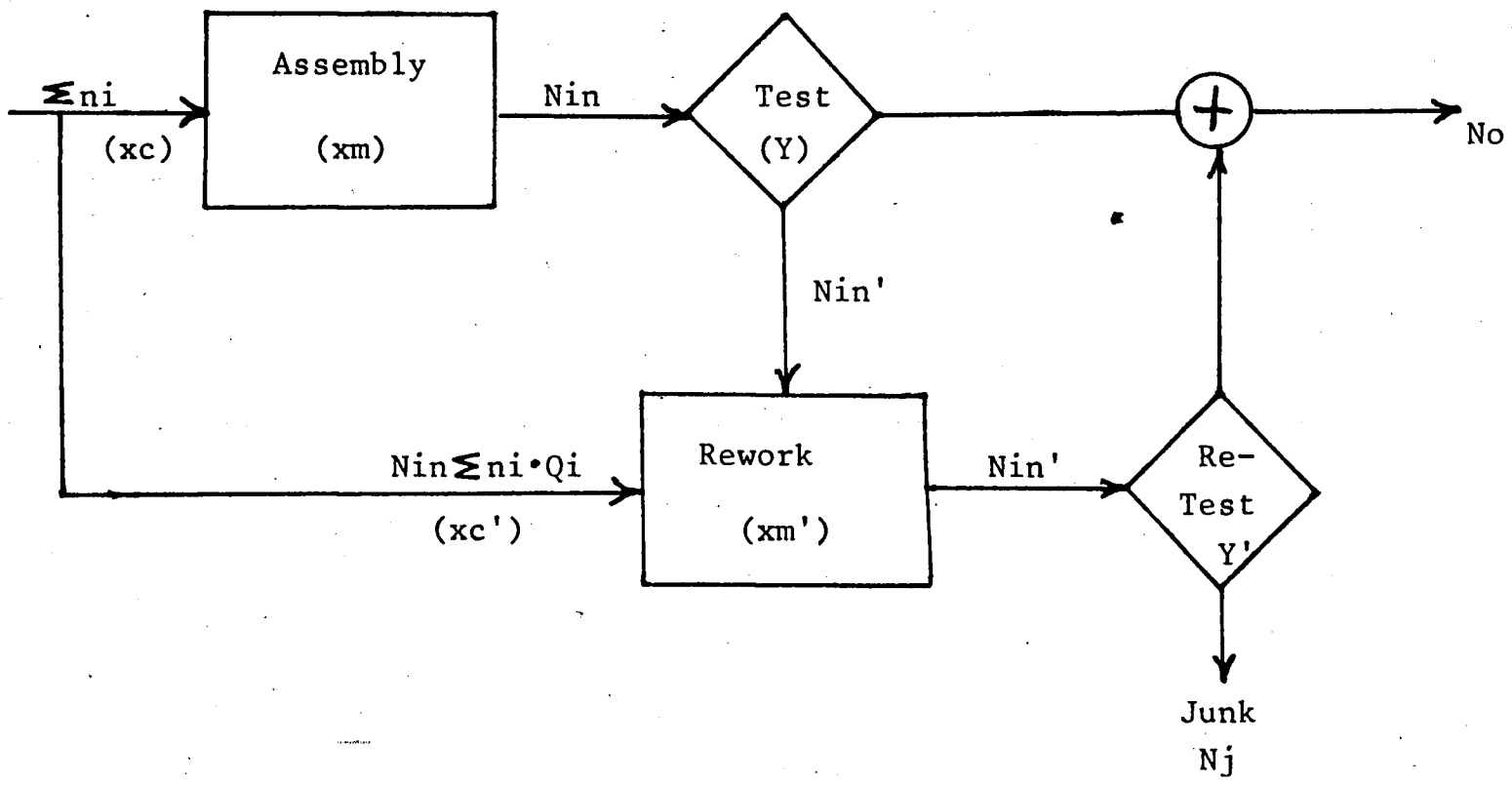


Figure 5. Representation of an assembly level node with rework capabilities.

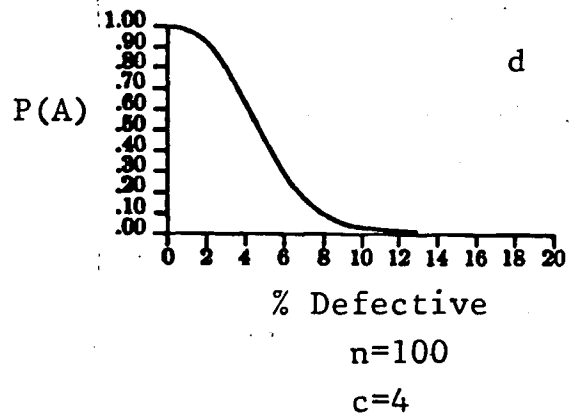
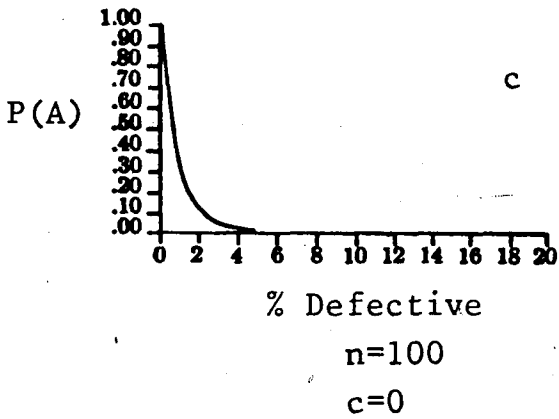
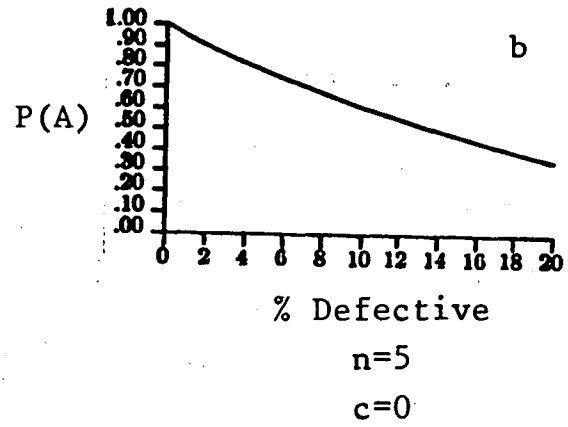
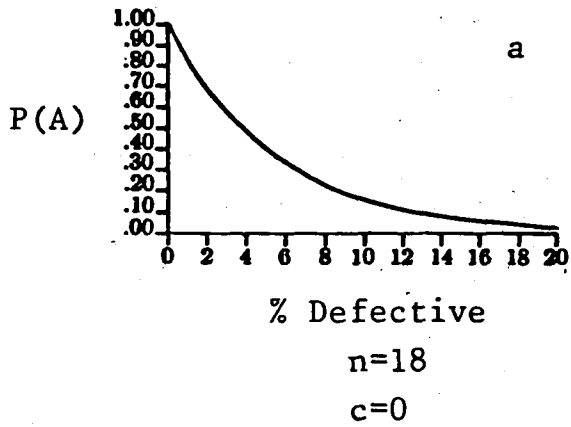


Figure 6. Typical OC curves for sampling.
 Sample size is varied in a and b while
 the acceptance number is varied in c and d.
 (Ref. 16)

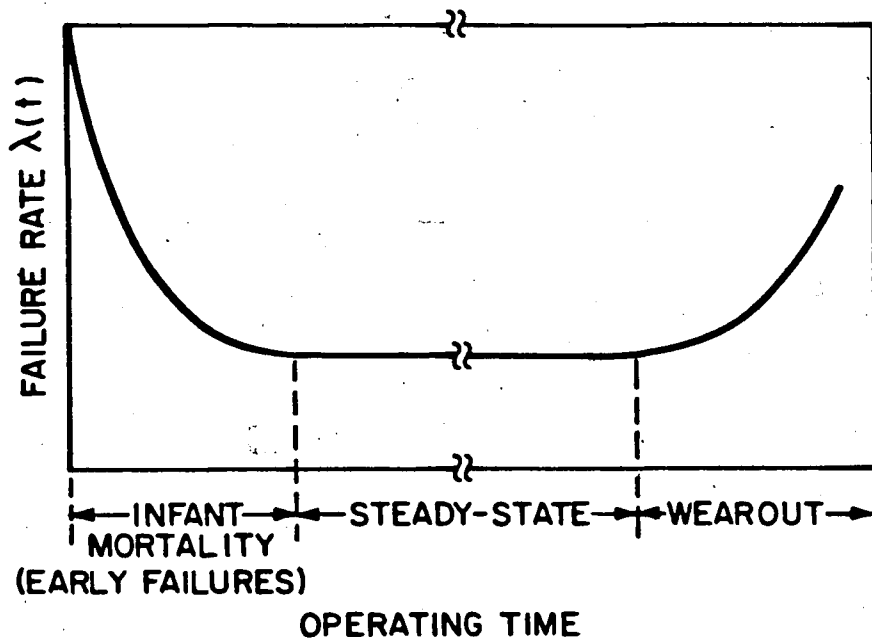


Figure 7. Failure rate curve for electronic product reliability. (Ref. 14)

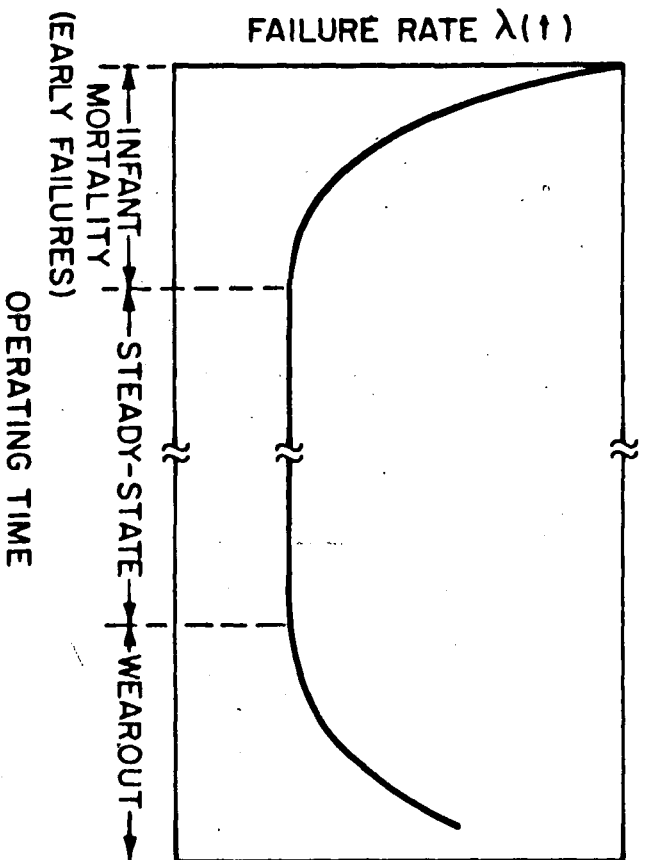


Figure 7. Failure rate curve for electronic product reliability. (Ref. 14)

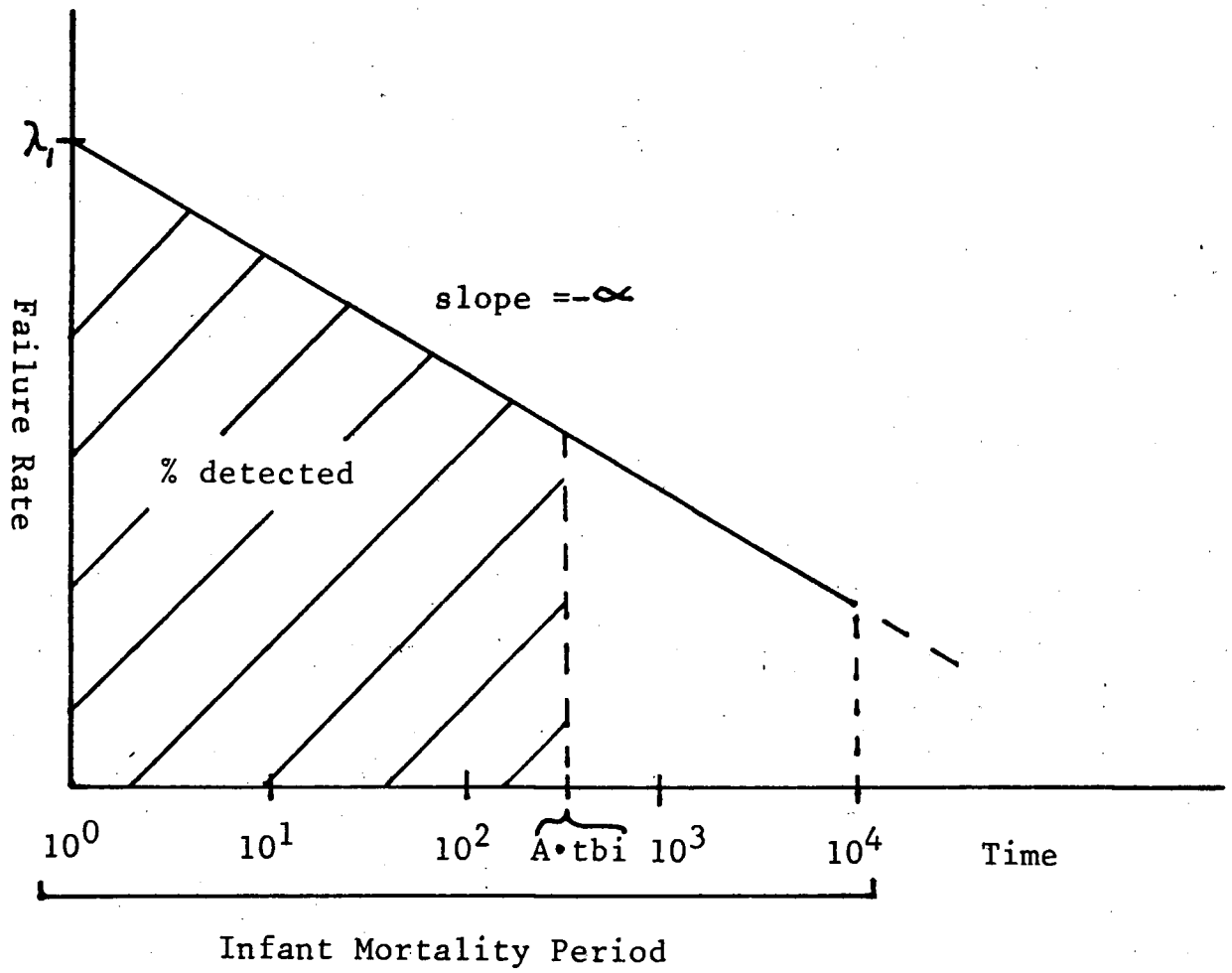


Figure 8. Weibull Failure Rate model for the Infant Mortality Period.

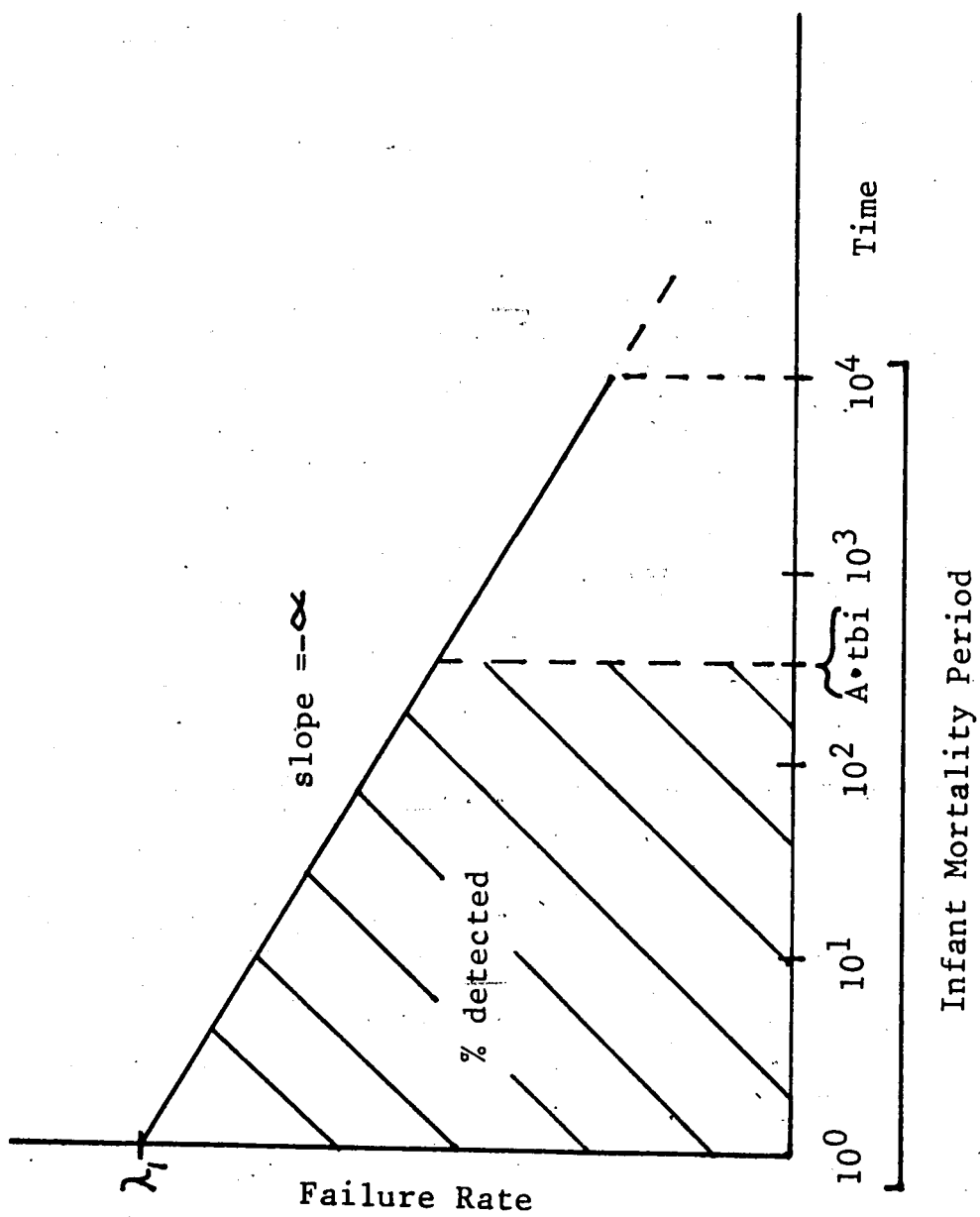


Figure 8. Weibull Failure Rate model for the Infant Mortality Period.

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VITA

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