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PROTECTION OF
MOS INTEGRATED CIRCUITS
FROM ELECTROSTATIC DISCHARGE

by

Jack K. Keller

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1976

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This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

May 4, 1976
(date)

Professor in Charge

Chairman of Department

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Abstract

Although the problem of static electric protection of MOS integrated circuits is by no means new, very little definitive information is available in the literature on this topic. While many models have been proposed for testing protection techniques, justification for their usage is frequently questionable.

One of the primary purposes of this paper is to present a realistic model of the human body for static electric protection purposes. A circuit consisting of a 150 picofarad capacitor, a 20K ohm series resistor, and an ordinary high voltage relay was tested and found to closely simulate the human body. In choosing this model, several other approaches were discarded because of lack of correlation to the actual problem.

The protection requirements are examined and electrical, technological, and circuit layout requirements are indicated. Failure mechanisms which commonly occur are found to be oxide damage, pn junction destruction, and metal shorts.

Various protection schemes are examined both as proposed in the literature and as used by several manufacturers. The resistor, diode, field plate diode, thick field MOS transistor, punch through, gated punch through, and spark gap devices are described. Using the elec-

trostatic equivalent circuit described, samples of the above protection schemes were tested and evaluated.

Results of these tests indicate that the gated punch through device, with proper modification and proper design, is most effective and versatile for static electric protection of MOS integrated circuits. Circuits presently protected in this manner typically survive discharges from persons charged to two to three kilovolts.

I. INTRODUCTION

Because MOS devices have input lines insulated from circuitry by a dielectric material which is destroyed by input voltages on the order of one hundred volts, they must be protected from large voltages appearing on these lines. Once the circuit is placed in its final operating system, it is (or can be) protected by external circuitry. However, during manufacture, testing, and assembly of these devices, they are unavoidably handled by human operators--who will inevitably carry a static electric charge. This charge can cause permanent damage to the device, and, as a result, the device must contain means to protect itself against possible static discharge from human beings.

Various protective circuits have been proposed in the literature (7,13,16-18) and many different types have been implemented in various manufacturer's circuits. However, available information on the effectiveness of these schemes is very scarce. Moreover, the static environment which these networks must protect against is either poorly defined or is not defined at all. A justifiable model of the human body's interaction with these circuits is not readily available. It will therefore be the purpose of this paper to provide the necessary information for accurate testing and protection of an integrated circuit

with respect to exposure to statically charged human handlers.

In defining the problem, an accurate model of the human body will be developed and tested. Consideration of resistance, body capacitance, and the actual nature of discharge into the circuit will be made. Conclusions will be drawn regarding the voltage levels, energy delivered, and the times during which discharge occurs. In order to provide a basis for understanding the requirements of the protection devices, mechanisms of destruction and technological restrictions will be indicated.

Using the human electrostatic model, and its consequent realization as an equivalent circuit, the various protection schemes proposed in the literature will be examined and their effectiveness will be tested using commercially available products. The results of these experiments will indicate the most effective methods for integrated circuit static electric protection, the proper methods of implementing them where speed or area requirements are critical, and are intended to provide the basis for development of even more effective schemes for future use.

II. BODY MODEL

1. PURPOSE

Measurement of the effectiveness of gate protection circuits requires the development of an accurate model of human charge storage and discharge characteristics. The model is necessary so that various integrated circuit protection schemes can be tested and evaluated easily and quickly. It is extremely important that the model be highly correlated to actual human characteristics, so that any results obtained can be directly related to actual usage conditions. Also, the model must be such that measurements exhibit a high degree of reproducability over time and between different setups. While integrated circuits may also be damaged by "self discharge" (such as by being dropped onto a grounded surface when statically charged), the capacitance of such circuits is small compared to that of the human body, and therefore the energy delivered by human discharge is far greater. This generally justifies its use as a sufficient and necessary test for a particular protection scheme.

2. GENERALIZED MODEL

Various models of the human body have been proposed in the literature. While each description varies in its

exact details, it is generally agreed (see Appendix A for references) that the best network for modeling the human body is that of a charged capacitor, a series resistor, and a relay-type switch as shown in figure 1 (see page 11). In order to test this model, specific values of components must be determined. Because of the widely varying and conflicting details available in the literature and the resulting need for a justification of the model finally chosen, actual measurements of human capacitive and resitive parameters are necessary.

A. CAPACITANCE

Human body capacitance was measured using a Keithley model 616 Digital electrometer. The technique used was to charge a person to 100 volts and then discharge the subject through the meter, while measuring the charge, in coulombs, delivered. Capacitance was then calculated using the expression:

$$C = dQ/dV$$

The results of a series of experiments involving body capacitance measurements of various subjects both insulated from and standing directly on ground can be found in Table 1. These results agree very closely with values calculated (1,2,3) assuming that the body capacitance can be modeled in terms of two components.

TABLE I

Measurements of Human Capacitance and Resistance

Subject	Body Cap'. C1 (pf) Meas.	Calc.	Foot Cap. C2 (pf) Meas.	Calc.	Wrist/Wrist Resist. (K ohm) Dry	Wet
A	106	96	74	47	28	3.2
B	119	100	941*	545	50	2.2
C	113	122	219	79	50	3.5
D	111	122	71	110	35.5	--
E	105	105	425*	514	40	--
F	109	96	75	90	19	--
G	112	95	76	78	55.8	--
H	125	103	356*	554	29.5	4.7
I	120	98	1070*	974	22	3.9
J	108	101	95	94	12.7	3.6

*Subject wore shoes with thin leather soles (k=20)

The first component (C1) is that due to the body's isolation from the ground. It can be assumed that the body is similar to a sphere of the same surface area isolated from a ground plane. Hence this component of capacitance can be given (4) by:

$$C1 = Q/V = 4\pi\varepsilon_o H/(10\times10^{-12} \times10\times10^{-2}) = 1.1H$$

where H=the subject's height in centimeters. Measurements of this component, as recorded in Table 1, were made by insulating the subject from the floor by a non-conductive material of at least one foot in thickness.

The second component (C2) is due to the parallel plate capacitive effect of the body being in contact with a ground plate through the soles of the shoes. Values for C2 in Table 1 were derived by measuring total body capacitance of a person standing on a metal plate, and subtracting the value of C1 previously determined. This component can be expressed as:

$$C2 = k\varepsilon_o A/(t\times10\times10^{-12} \times10\times10^{-2}) = 0.089kA/t$$

where A=area (in square centimeters) of both shoe soles in contact with the floor, t=thickness of subject's shoe soles in centimeters, and k=dielectric constant of material comprising the shoe soles (5). If the sole and heel vary in thickness or composition, the formula must be modified accordingly.

If it is assumed that an average person is 175 centimeters tall, wears rubber soled shoes (K=o.6) that have a total bottom area of 360 square centimeters and are one centimeter thick, then,

$$C1 = 1.1x175/2 = 95.7 \text{ pf}$$

$$C2 = 0.089xo.6x360/1 = 211.5 \text{ pf}$$

or the total body capacitance is:

$$Cb = C1 + C2 = 307 \text{ pf}$$

If we assume that the flooring material used in the handling environment is non-conductive, a more typical value may be 100 to 200 picofarads. For the purposes of testing, a value of 150 picofarads was chosed which represents an upper limit of C1 only.

B. RESISTANCE

The second component examined in the search for an accurate human model was that of body series resistance. Data from the literature as tabulated in Appendix A indicate that previously published values of this parameter range from zero to 10K ohms. Methods of measurement range from direct DC bridge measurements to computation from human discharge waveforms. While the latter has the advantage that its dynamic nature more closely matches actual discharge conditions, it suffers from the disadvan-

tage that other unknown parameters (such as switch characteristics, rise time, etc.) also enter into the calculations, affecting the result substantially. Conversely, the DC measurements are direct, but are not as closely related to the actual problem.

Table 1 (page 7) gives the wrist to wrist resistance values of several subjects, measured using a laboratory-grade volt-ohm-meter. Measurements were taken by having the subjects first hold large, dry copper electrodes, and secondly by having them hold electrolyte-impregnated electrodes. The vast difference in these readings probably explains the variety of published values in Appendix A. Similarly, the magnitude of these values seem to indicate that those measurements were taken using electrolyte-impregnated body contacts. This does not seem reasonable, however, since few people will handle integrated circuits with such contacts. Most problems in the field will surely be traceable to touch by a person with dry or, at worst, moderately moist finger tips. Hence, while individual values vary greatly for different conditions (humidity, skin conditions, etc.), a series resistance of about 20K ohms was chosen for future experiments.

C. VOLTAGE USED

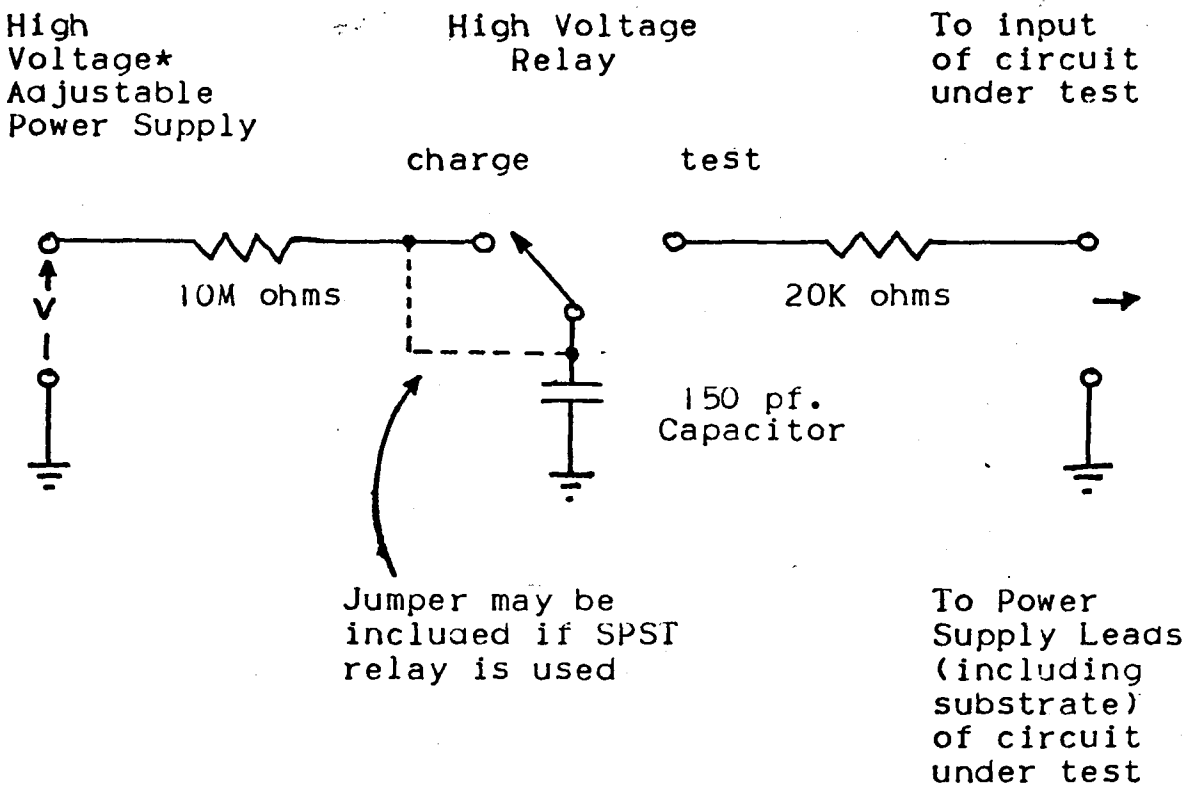
Just as with other parameters previously discussed, published ideas on the voltage to which a person can be charged to under various conditions varies greatly (from one to 30 kilovolts...see Appendix A). These values were verified using a Sweeney Model 1127 Static Meter. For example, it was found that in low humidity situations several tens of kilovolts can be generated and maintained on the human body by simply walking across a rug. Even friction of loose clothing rubbing against the body can develop substantial voltages, depending on the nature of the fabric (6).

Since the purpose of an MOS integrated circuit protection device is to isolate input circuitry from static electric voltages of these magnitudes, test procedures should ideally stress inputs to within this range. As of this writing, however, no protective networks have been found effective to voltage levels greater than five kilovolts. In actuality, however, two to three kilovolts may represent an upper limit on human static voltage levels in over 90% of all cases (7). Therefore, protection schemes should be tested to at least this range, and greater only as changes in technology occur. In any case, protective schemes which fail below about one kilovolt must be regarded as inadequate.

D. HUMAN SWITCH CHARACTERISTICS

The final part of the human body model to be investigated is the switching mechanism which takes place when the body discharges into an integrated circuit. Several published testing techniques indicate use of high speed mercury-wetted relays (7,8,9). However, such switches often suffer from substantial leakage when "off"; that is, much charge may be dissipated from the capacitor before the relay is energized (see figure 1).

Clearly, the switch used in the model should, as closely as possible, reproduce the effects which occur when a human touches a circuit package directly. Extensive examination of waveforms of human static electric discharge into an integrated circuit have indicated that the human switch "bounces" several times before making final contact. Discharge measurements were made into a five picofarad capacitor to simulate the input impedance of an integrated circuit. Figures 2 through 5 are oscilloscope photographs of these waveforms for the case where a human touches the lead directly, where a human touches the lead with a metal object, and the corresponding waveforms of equivalent discharge by a high speed vaccuum switch and a high voltage relay. In each case, a photograph of the initial pulse is included indicating circuit speed requirements. Note that the high voltage



*V > 0 for P type substrate

V < 0 for N type substrate

Figure 1. Equivalent Circuit for Human Static Electric Discharge

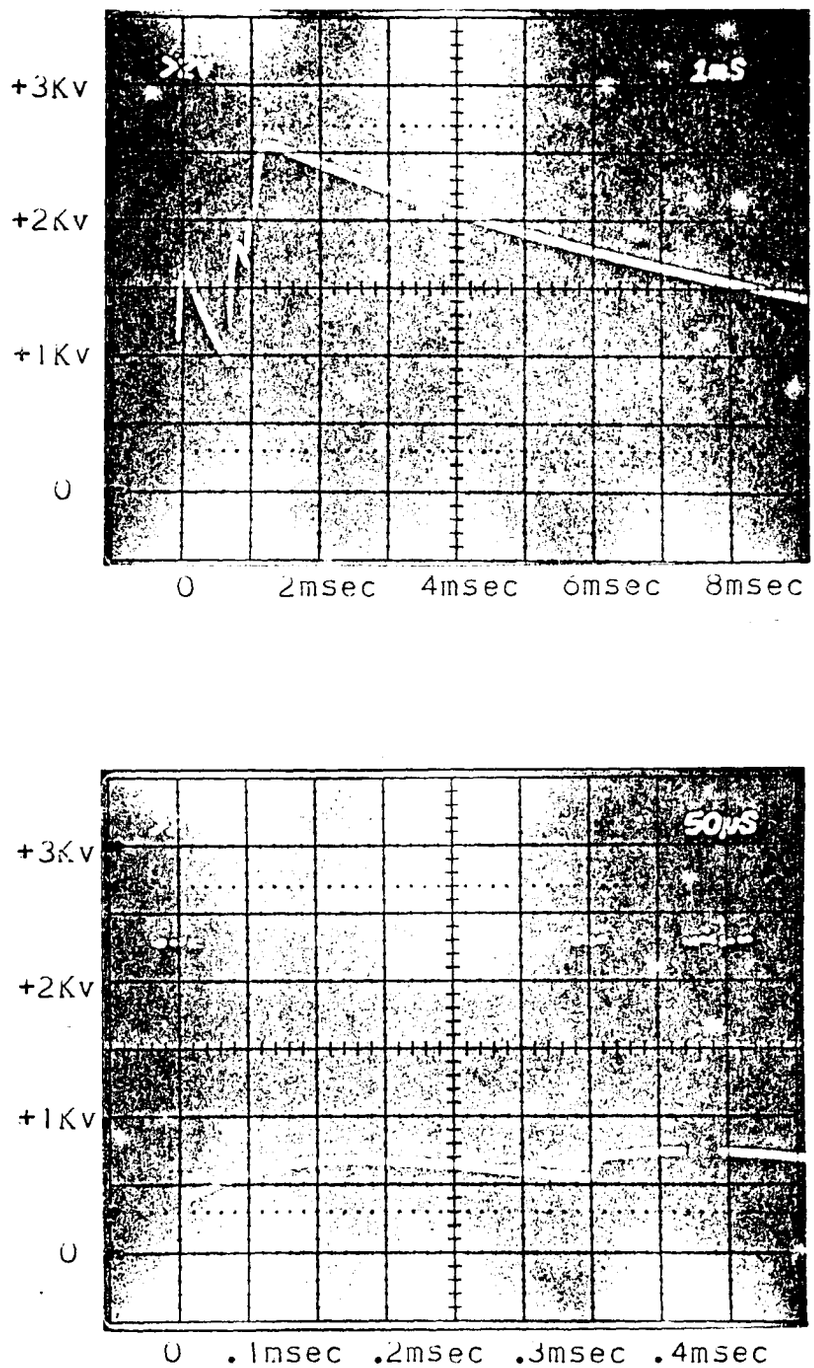
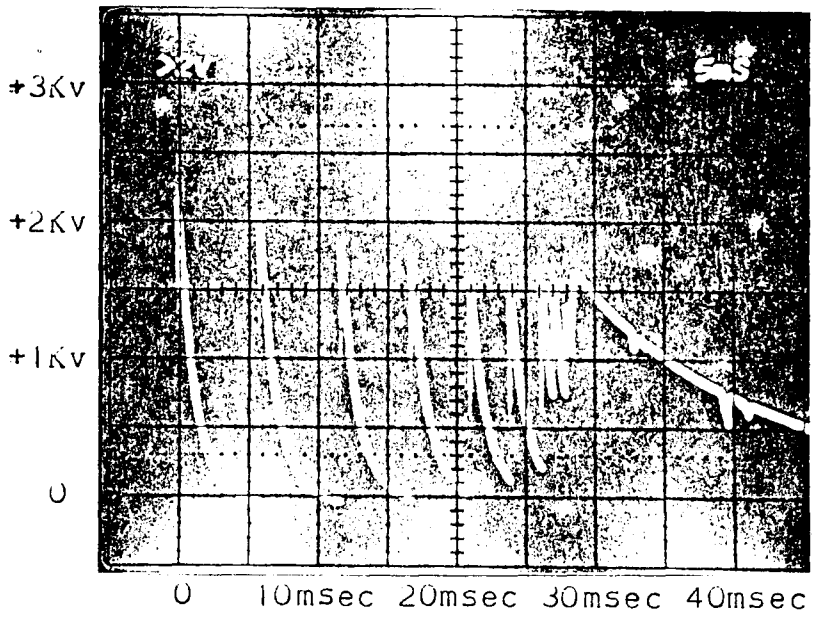


Figure 2 Waveforms of static discharge of human (charged to three kilovolts) touching integrated circuit lead directly



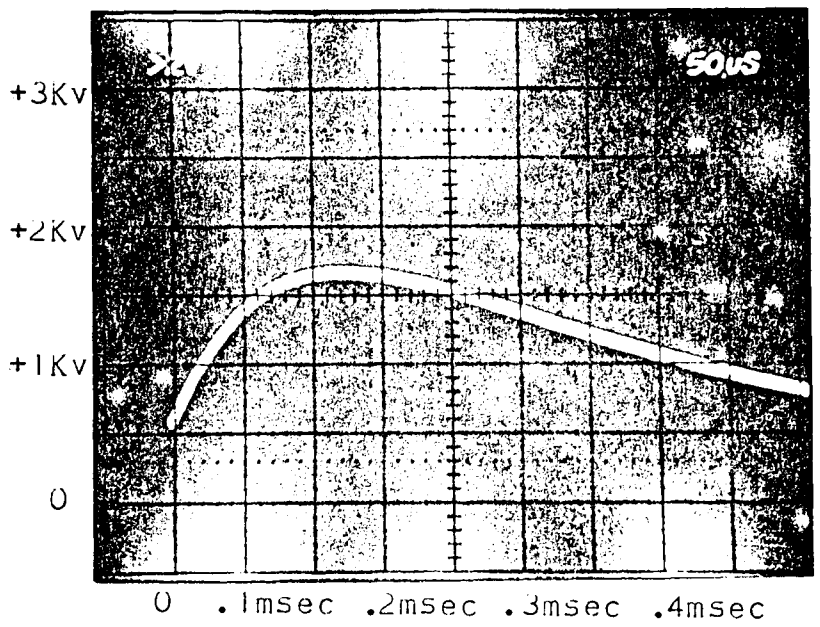


Figure 3 Waveforms of static discharge of human (charged to three kilovolts) touching integrated circuit lead with a metal object

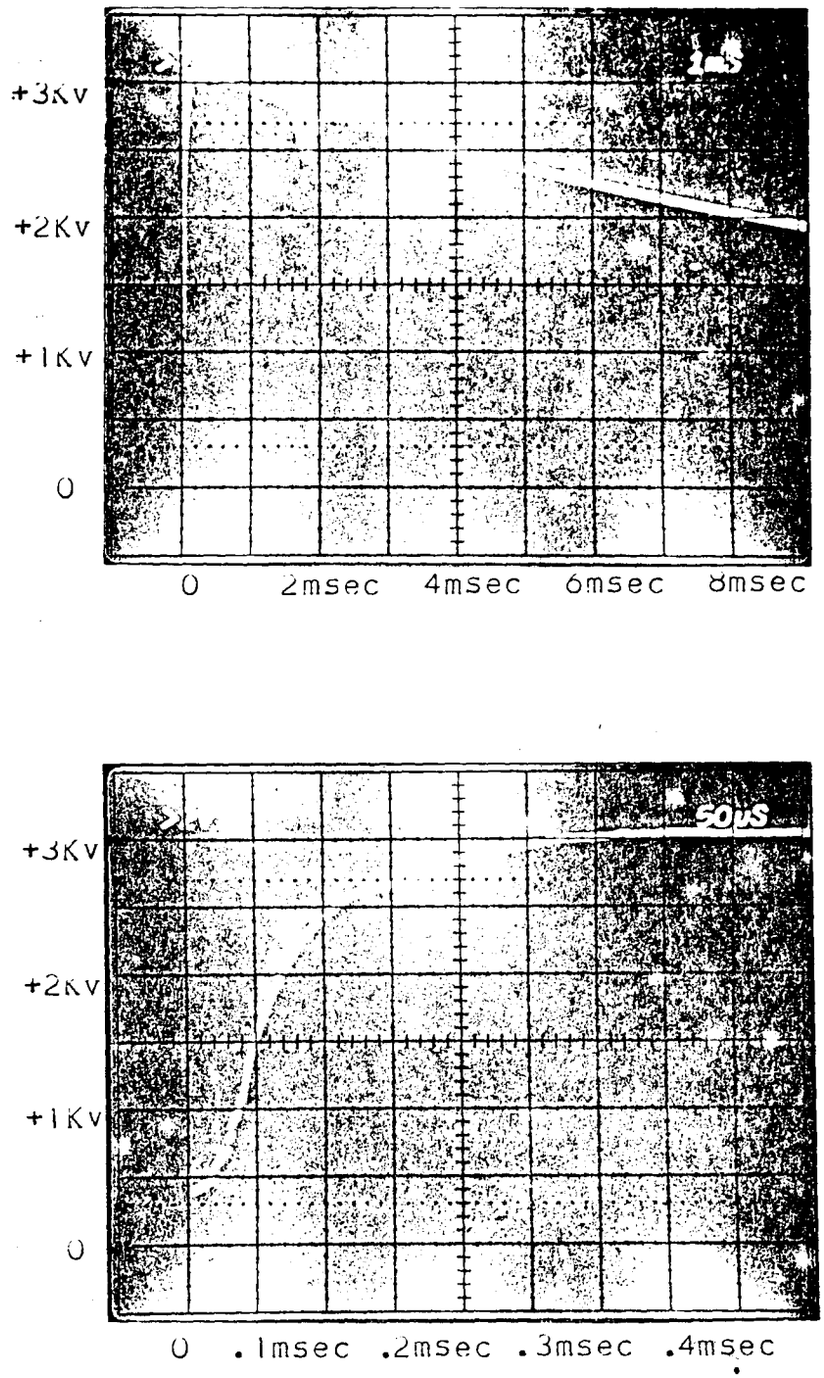


Figure 4 Waveforms of static discharge of human equivalent circuit using a high-speed relay

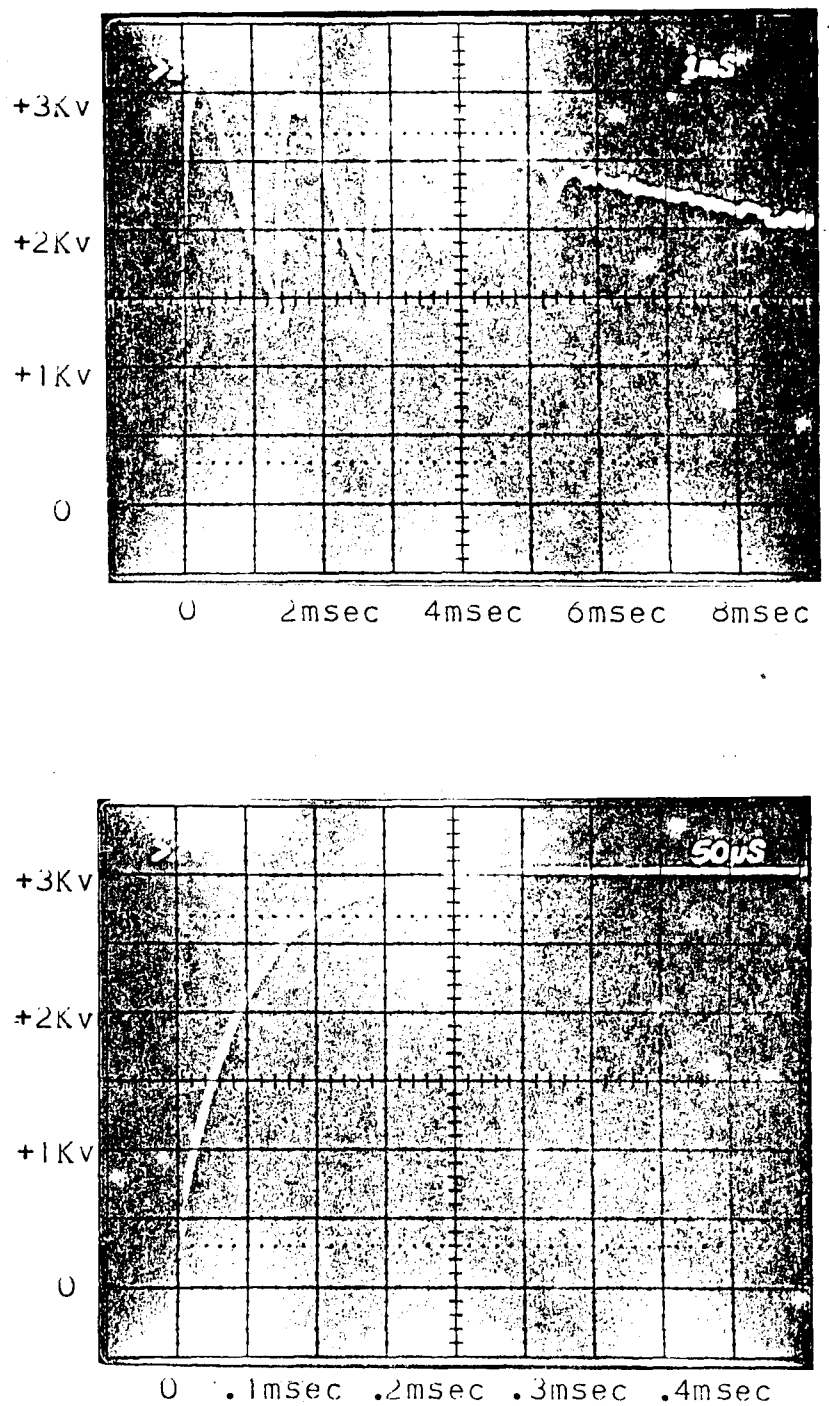


Figure 5 Waveforms of static discharge of human equivalent circuit using ordinary high voltage relay

relay more closely resembles the human discharge than does the high speed vaccuum switch. In all photographs, the slow discharge is due to the high input impedance of the measuring circuitry. These figures also show that the extent of the "bouncing" which occurs ranges from one millisecond to almost 30 milliseconds if the circuit is touched with a metal object held in the hand. These extremely long times may be somewhat justified by considering the rough and shaky nature of the human hand. If the impedance of the protection circuitry is small, clearly all charge would be dissipated in the first bounce.

As a result of these experiments, it seems that the use of high speed or mercury wetted switches are not indicated. Even the rise time of the initial pulse delivered to the circuit by a human is on the order of that of conventional high-voltage mechanical relays. The use of a series resistor in the model does not effect rise time but merely serves to limit current flow when the relay has closed. Since the latter generally suffer from contact bounce problems too, they seem the logical choice for human circuit modeling and have therefore been chosen for it.

One other factor deserves mentioning here. The voltages described thus far are sufficient to cause ioniza-

tion of the air resulting in the formation of an electrical arc. The characteristics of such an arc include negative resistance (10). When high voltage discharge is made into low impedance (<10K ohm) integrated circuits, the negative resistance of the arc is sufficient to temporarily cause current flow in the opposite direction from that forced by the charged capacitor. Appendix B further describes this phenomenon which has been observed in the laboratory during contact bounce.

3. TESTING of the MODEL

The completed model of the body is shown in figure 1. In order to test its validity, the inputs of several readily available four-input NAND MOS integrated circuits were stressed using successively higher voltages until failure occurred. Failure was indicated by a change in input characteristic as measured by a curve tracer. Almost all failures were catastrophic short circuits; hence, there was little difficulty in determining the voltage at which it occured. The results of the comparison between destruction by actual human touch and the human model as determined by the experiment are shown in Table 2. A close correlation of the model to actual direct human destruction is noted. Since destruction occurs at about 40% higher voltages for the model than for static

TABLE 2

Comparison of Actual Human Body

and Electrical Model Destructive Voltages

Circuit	Direct Human Discharge	Equiv. Circuit
1	1500	1200
2	1550	1450
3	1180	1270
4	1500	1300
5	1670	2000
6	1750	1250
7	2500	1500
8	2670	1170
9	2430	1430
10	3300	1670
Averages	2000±680	1420±250

Note: Above voltages are averages for each circuit and have been normalized for human destruction with a hand-held metal ooject at one kilovolt.

discharge with a hand-held metal object, the test voltages used should be derated for direct correlation to the problem of human interaction. Hence, if a circuit is tested to one kilovolt using the model in figure 1, it will be effective to only about 700 volts in protecting against stress with a hand-held metal object. In comparison, direct discharge by human contact will cause failure at voltages which are about 40% higher than those used in the model. Comparison of the waveforms in figures 2 through 5 support these experimental conclusions.

III. REQUIREMENTS OF A PROTECTION SCHEME

1. ELECTRICAL

The characteristics of a protection scheme must meet certain specific electrical criteria if it is to be effective. These criteria involve initial reponse time, subsequent restressings, maximum sustainable voltage, and total energy dissipation.

If the input capacitance of a typical integrated circuit is taken to be about five picofarads, then little voltage is lost by the 150 picofarad human source in charging up the integrated circuit to its voltage. Assuming a human series resistance of 20K ohm, the protective circuit must then react in:

$$t = RC = (5 \times 10^{-12}) \times (20 \times 10^{3}) = 100 \text{ nanoseconds}$$

Note that if a lower limit of 1K ohm is used as human source resistance, this time is cut by a factor of 20 to five nanoseconds. Hence, the protection scheme must be fast.

It has previously been mentioned that typical static electric discharges may take the form of a series of rapidly recurring pulses due to a form of human contact bounce. This problem must also be considered in designing an effective scheme.

Once contact bounce has stopped, the protection network must then be able to withstand the continued discharge of the human through substrate or power supply lines. Using 150 picofarads, charged to two kilovolts, the energy removed would be on the order of:

$$1/2CV = 1/2(150\times10^{-12})\times(2\times10^{3}) = 4\times10^{-4} \text{ joules}$$

Considerations of circuit over-heating and subsequent destruction at this and higher voltages common in working environments must be made (see reference 11).

2. MECHANISMS OF DESTRUCTION AND CIRCUIT LIMITATIONS

Of equal importance in the design of an effective gate-protection scheme as the protection requirements discussed above, are the mechanisms by which failure occurs. Although each proposed network will surely fail for different specific reasons, certain important generalizations can be made regarding the nature of these failures.

The commonly used gate dielectric material for MOS integrated circuits is thermally-grown silicon dioxide having a breakdown voltage on the order of 8x10 volts/centimeter (11,12). Hence, for commonly used gate oxide thicknesses of about 1000 angstroms, 80 volts may be sufficient to destroy this gate insulation material and render the circuit useless. Klein (11) has shown that

this breakdown is most likely to occur at flaws in the dielectric and occurs at lower voltages when thermal instabilities are present. Careful processing can reduce this problem significantly. Using silicon nitride as a gate dielectric instead of silicon dioxide allows somewhat higher breakdown voltages (13). This material, however, must also be protected for certain common voltage levels.

In addition to oxide destruction, or as a consequence of it, junction leakage may be increased by static stress causing a circuit to fail specifications even though it is functionally operational. These effects are similar to the melt transition caused by second breakdown of a p-n junction (14). Freeman and Beall (15) have also observed damage due to "microdiffusion" of dopants caused by high density breakdown currents.

Other mechanisms which may be responsible for circuit failures due to static electric overstress, although rarely seen, include actual metal destruction. This catastrophic failure is usually a result of severe overheating of the device or unexpected on-circuit electrical arcing. Internal protection against these extremes is difficult and might be better accomplished by external controls.

3. TECHNOLOGICAL RESTRICTIONS

Technology plays an important role in protection requirements. Protective networks should be designed using already present processing steps. A more complicated process to provide basic input protection may not be economical. Since the choice of processing technology (CMOS, PMOS, NMOS, SiGate, etc.) is based on circuitry performance requirements, protective schemes must be available as part of each process. The use of low substrate resistivity material using epitaxial processing, if available, will significantly improve current carrying capability of any protective scheme. In addition, circuit speed or size requirements may restrict usage of certain networks, forcing custom modifications of protection devices where necessary.

In general, any protective device used should be fabricated utilizing existing technology, should be of minimal size. and should not adversely affect circuit speed.

IV. PROTECTIVE SCHEMES

In the previous sections, the problem of input protection was explained, electrical and technological restrictions were defined, and possible destructive mechanisms were identified. A protective network remains to be described which will be effective in protecting the very circuitry out of which it is, itself, fabricated. Various attempts to solve this paradoxical problem have been made in the past several years and are described below.

1. RESISTOR

Perhaps the simplest of all protective networks, yet the basis of even the most complex, is the input resistor as shown in figure 10. The purpose of this device is to limit current flow into the active circuitry (16). When fabricated from non-diffused material (such as polysilicon), so that no parasitic diode results, it is of little value. To be effective, it must be combined with a device which will prevent the gate voltages from reaching destructive levels. While the resistor may be small in area requirements, it may adversely affect circuit speeds due to the "RC" time delay constant.

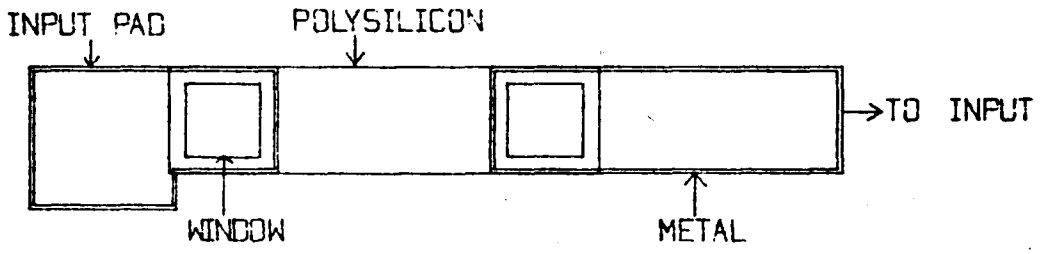


Figure 6 Circuit layout of resistor input protection network

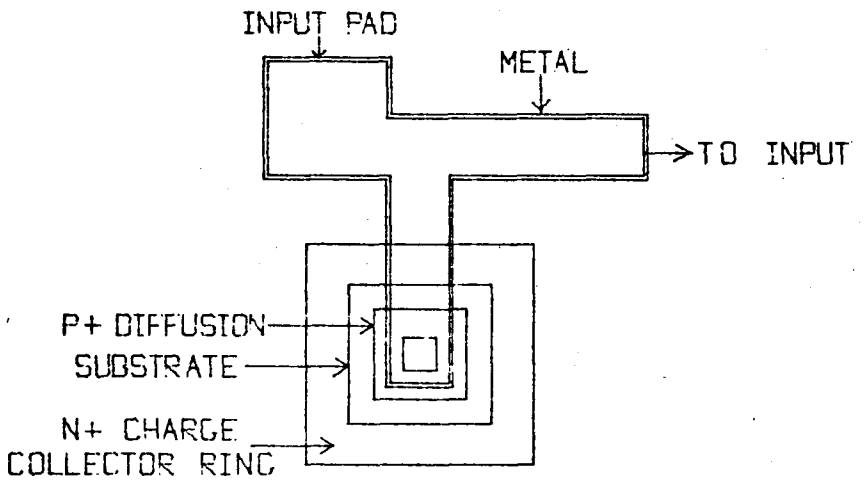


Figure 7 Circuit layout of diode input protection network

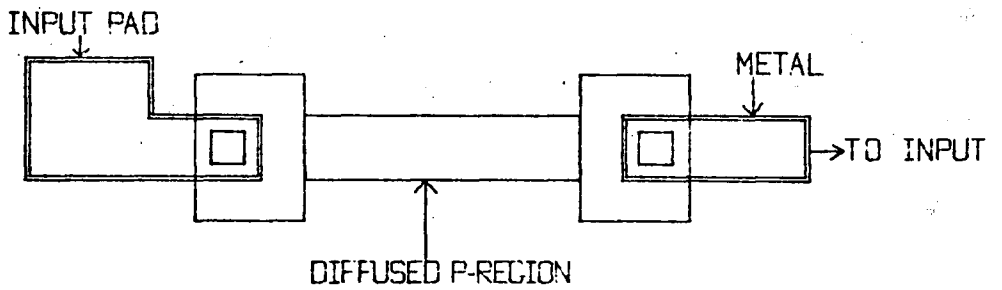


Figure 8 Circuit layout of resistor/diode combination protection network

2. DIODE

Another common protective device is the input diode (shown in figure 11). In the forward direction, the diode forms an excellent low-impedance current path. During normal operation, the diode is reverse biased and subsequently has little effect on the operation of the circuitry. Fabrication must be such, however, that the reverse breakdown voltage of the diode is less than that of the gate oxide. This device combines the advantage of small size with minimal increase in delay time. When used alone, however, it is itself easily destroyedeby excess currents and hence is not very effective.

3. RESISTOR/DIODE COMBINATION

By combining the previous two schemes, as shown in figure 8, a much more effective network is obtained. The resistor is used to limit current flow while the diode, whose reverse breakdown voltage is less than the breakdown voltage of the gate oxide, protects the latter from destruction. This idea has been found to be most effective if the resistor is diffused, so that, in effect, it also becomes a diode. The benefit in delay time resulting from the use of a deposited polysilicon input resistor in no way compensates for the loss in protective capability due to the absence of the associated diode. The value of

the input resistor used depends on the breakdown impedance of th diode. If the diode has a resistance to substrate (Rs) of 25 ohms under these conditions, and protection is desired to five kilovolts (Vprot) when the breakdown voltage (Vbd) across the diode is limited to 50 volts, then the value of the input resistor (Rin) can be found by voltage division:

$$Rin = (Vprot - Vbd) \times Rs / Vbd$$

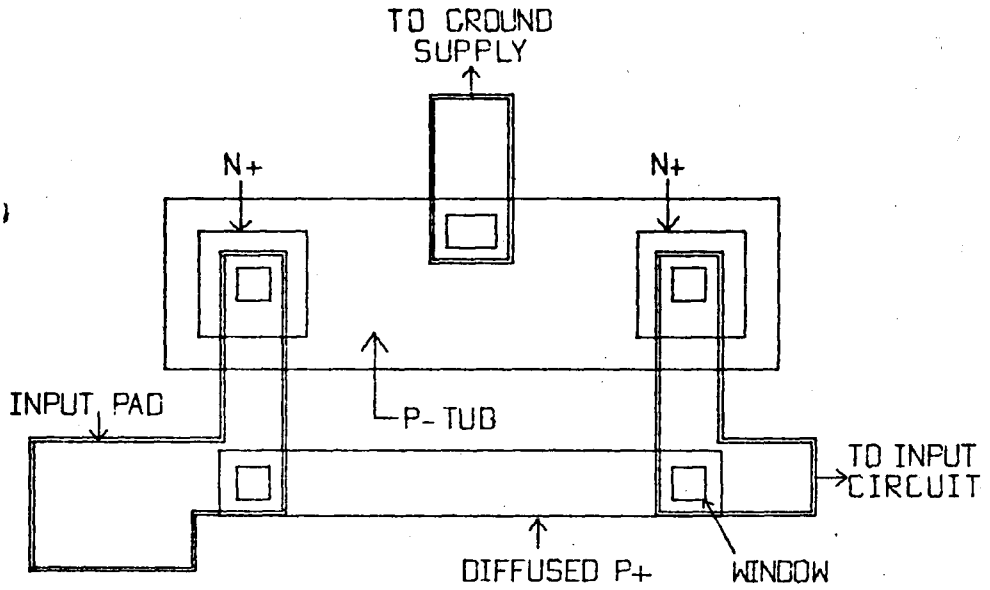
$$Rin = (5Kv - 50) \times (25) / 50$$

$$Rin = 2.5K \text{ ohm}$$

Further discussion of this scheme is given by Lenzinger (13).

When the technology used allows back to back diodes (such as with CMOS processes), as shown in figure 9, the current handling capability is greatly increased since protection is accomplished in both directions through the use of forward biased diodes. Results in Appendix E show that this technique is very effective, but is limited in its applications. Speed and area requirements for this network are moderate, making it a desirable, although not ideal, solution.

Circuit Layout



Schematic

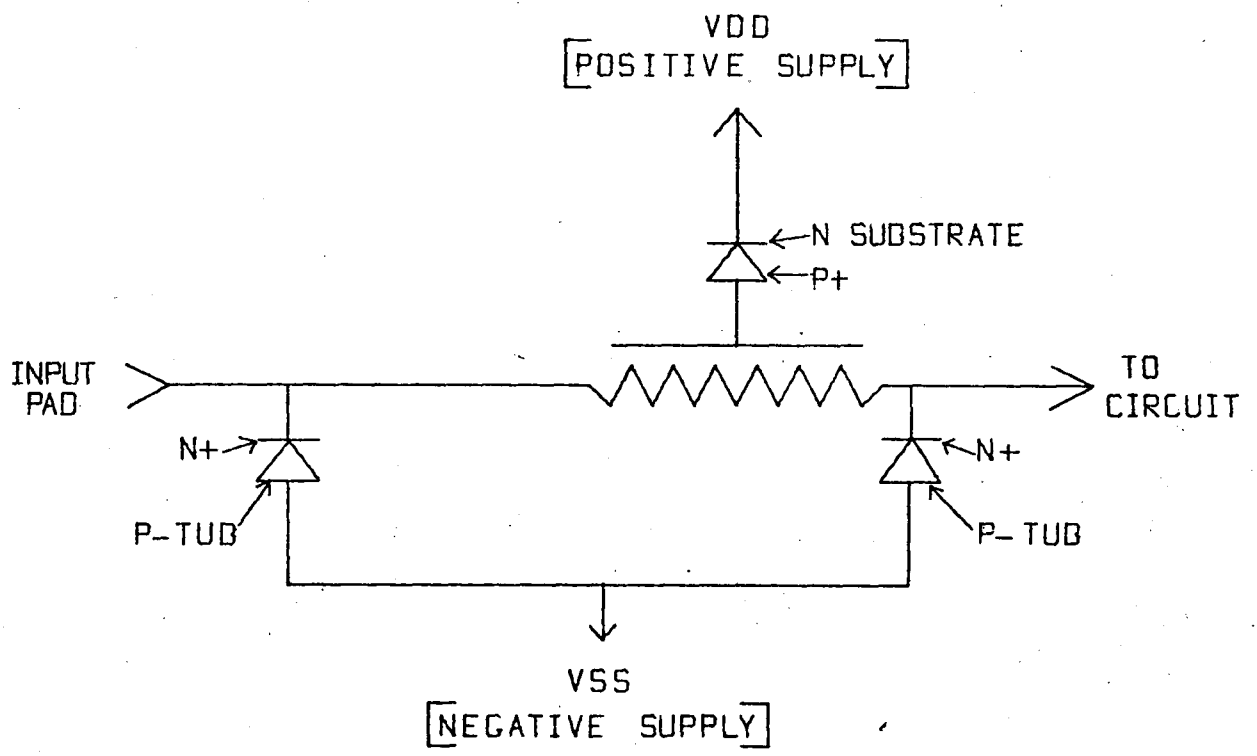


Figure 9 Complementary dual diode protection network

4. FIELD PLATE DIODE

As previously mentioned, in order to provide proper protection using a resistor/diode network, the diode reverse breakdown voltage must be less that that of the MOS gate oxide. One method of lowering the breakdown of a diode made from the source and drain diffusion, which should typically be 90 volts, is by use of a field-aided breakdown design (17). The idea, as shown in figure 10, is to coat the p-n junction with a thin oxide layer and to overlay it with a metal electrode attached to the substrate. The appropriate breakdown value can be obtained by varying the thickness of the dielectric under the electrode. Using the same dielectric as the gate of MOS devices, a value of about 40 volts is generally achieved. Although this device is simple, since the reduction in breakdown voltage occurs in such a small region, the series resistance of the device is high. In addition, the breakdown is prone to "walkout" when stressed, which raises the breakdown voltage of the diode and decreases the protective capability against further stress. Experimentally, "walkout" is easily observed as a slow increase in breakdown voltage while the reverse "IV" characteristic is being observed. Results shown in Appendix E indicate that this protective technique, used alone, is not sufficient to provide adequate protection.

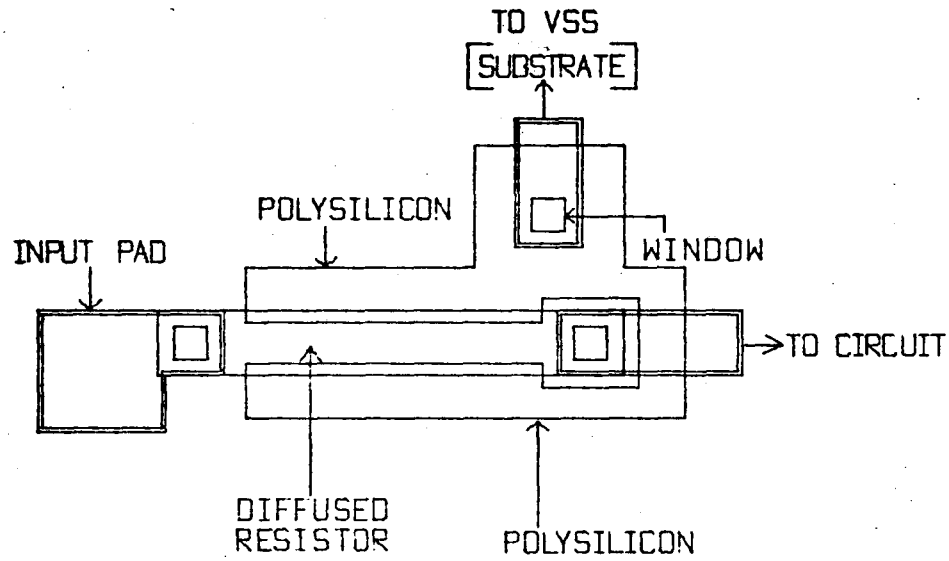


Figure 10 Circuit layout of Field plate diode protection device

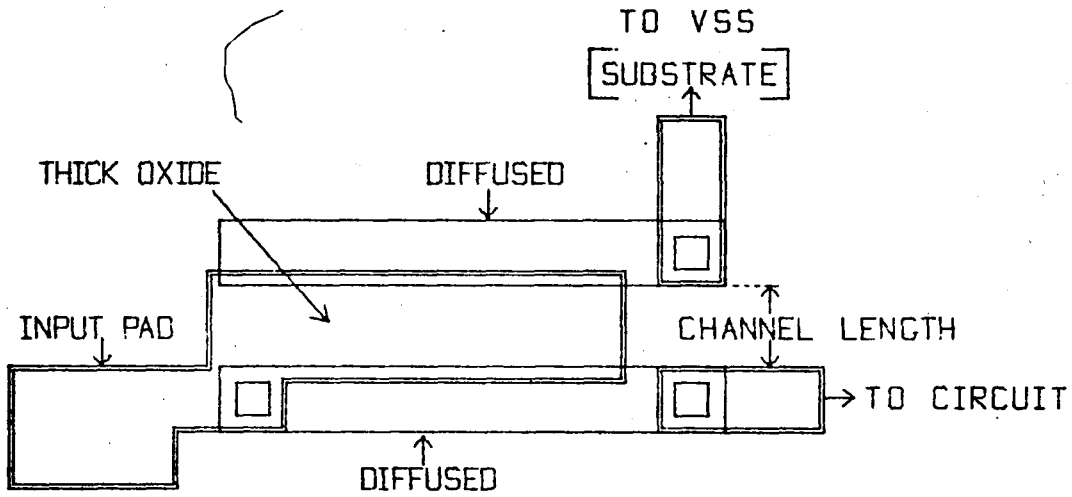


Figure 11 Circuit layout of thick oxide MOS transistor protection network

5. THICK-OXIDE MOS TRANSISTOR

A rarely used structure, shown in figure 11, is the thick oxide MOS diode. This device is simply an MOS transistor whose gate, covered with thick oxide (e. g. 5000 angstroms), is tied electrically to the input. When an input voltage is high enough to induce a channel in the silicon under the thick oxide, the device will conduct to the substrate. The disadvantages of this network are its low "on" resistance, and high threshold voltage (100 volts). Protection afforded by this device is poor. Note should be made of the fact that, in this device, adjacent diffusions are too far apart to allow effective punch-through protection as described next.

6. PUNCH-THROUGH DIODE

A popular and effective protection device is the punch-through diode (16,17,18). In this device, under stress, current flows from one diffused area to another adjacent diffused area of the same conductivity type, which is held electrically at substrate potential. It is similar in appearance to the thick MOS transistor shown in figure 11 except that the channel length is much smaller. Punch-through occurs when the input diffused region is reverse biased greatly enough so that its depletion region

extends to the other nearby diffused region. Sze provides an equation to permit calculation of the approximate voltage at which this effect occurs (19). For substrate doping (Nd) of $1x10^{15}$ /cubic centimeter, and channel length (L) of ten microns:

$$Vpt = L^2 qNd/2Es$$

$$Vpt = 75.2 \text{ volts}$$

This technique is especially effective if the diffused regions are strapped with metal (i. e. covered and connected to the metal by windows) to avoid resistive drop along them, and if the source diffusion is tied to the substrate bonding pad by a direct metal connection. In addition, experiments have shown that the use of a small resistor (about 1K ohm) in series with this device and the MOS circuitry provides greatly improved protection. While consuming little area, the scheme may, however, introduce appreciable capacitive delay.

7. GATED PUNCH-THROUGH DEVICE

One of the most commonly used, most versatile, and most effective gate protection techniques is the gated punch-through device (16,18) as shown in figure 12. It is basically a combination of many of the best features of previously-described devices. Incorporated in it are a

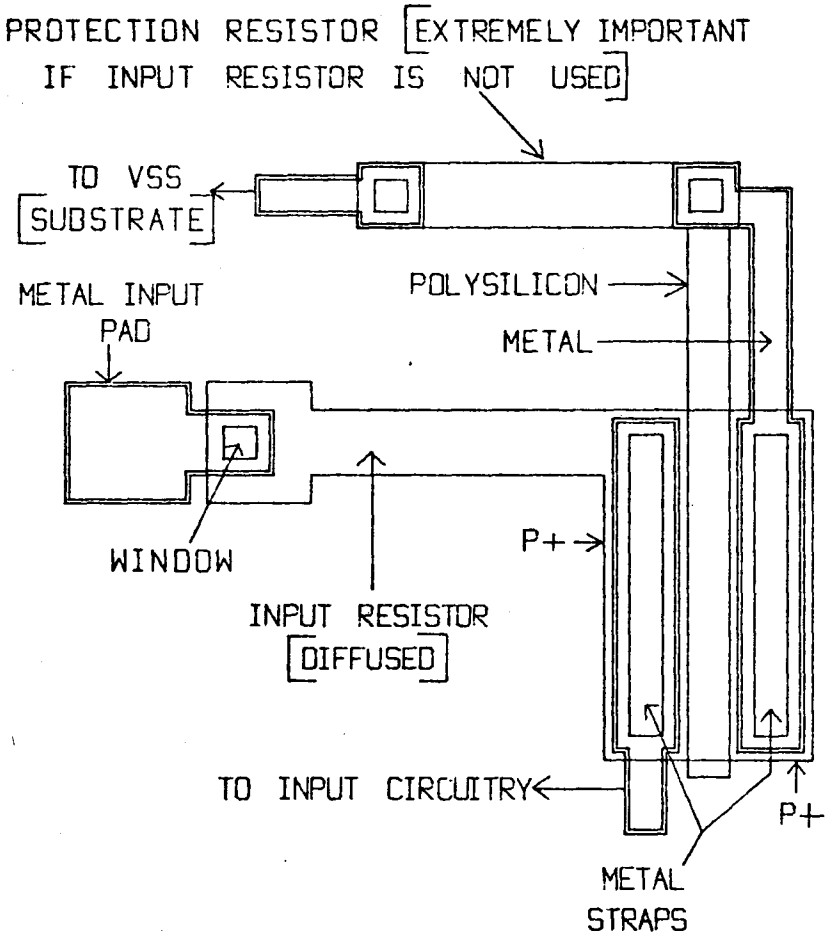


Figure 12 Circuit layout of gated punch through protection network

diffused input resistor, gate-enhanced p-n junction region, and a punch through device. The junction breakdown voltage is lowered by overlaying a polysilicon gate, which is itself protected by a small (500 to 1K ohm) resistor before being tied to substrate. Closely spaced diffusions, cut by the polysilicon gate, form the punch-through device. These diffusions are strapped with metal to prevent resistive voltage drop. If the delay time of the input resistor cannot be tolerated, it may be eliminated. However, in this case it is necessary to include a current limiting resistor between the source diffusion and substrate to prevent destruction of the network. The input pad should still include the initial large diffused region. This area acts as a diode, causing minor additional delay (usually tolerable), but providing substantial protection in the forward-bias region.

8. SPARK GAP DEVICE

Lindholm and Plachy (7), and Coule (16) describe a protection technique using two closely spaced metal pads forming a spark-gap as shown in figure 13. Placement of the device should be before any input or additional protection circuitry. It may be implemented by locating bonding pads close to a substrate metalization encircling the integrated circuit chip. To prevent metal to metal

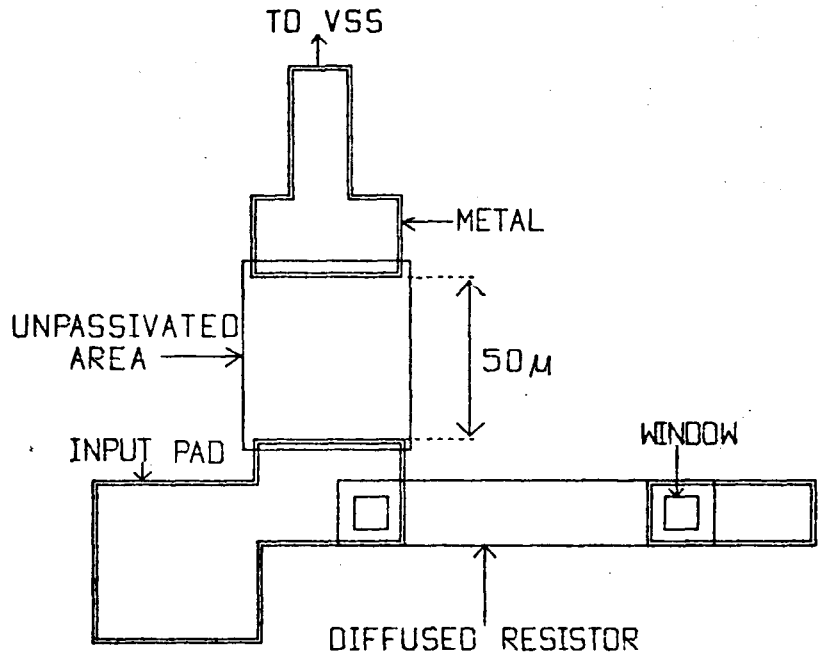


Figure 13 Circuit layout of Spark Gap Device

shorts, the distance between metal here should be at least 50 microns (7). This device must be used in conjunction with a field plate diode, punch-through device, or similar network since it is effective only above 300 to 400 volts. To allow this voltage to develop, it must therefore be separated from the additional circuitry by a resistor.

A requirement for implementation of this device, which may make it unsuitable for many applications, is that it requires a cavity package. That is, the area between the input and substrate ring must be left unpassivated so that the impedance of the gaseous discharge is kept minimal. The use of certain hydrocarbon-base compounds as encapsulants (such as RTV) should be avoided since they may "carbonize" and form a conductive path (short). Also, no other diffusions or metalization should be as close to the input as the spark gap device.

Although this device may be effective initially, repetitive sparking will cause metal erosion and eventual failure. Coule (16) indicates that a combination protective scheme including the spark gap device should be effective to stress voltages greater the five kilovolts. Although such structures appeared to be have been included on some of the integrated circuits tested, none withstood voltages to this level (see Table 3).

9. OTHER TECHNIQUES

Various other protection schemes have been developed, but most are not applicable except to specific circuits. The inclusion of zener diodes, having substantial reverse breakdown current carrying capabilities, is effective, but relies on special process steps for implementation. Such process techniques are not normally a part of MOS integrated circuit fabrication and therefore are uneconomical to include.

V. GENERAL LAYOUT COMMENTS AND TEST PROCDURES

Table 3 lists the results of static electric tests of protection schemes. The devices listed therein were tested using the circuit of figure 1. Starting at -100 volts (assuming N-type substrate material), the capacitor was discharged, at least five times into an input of the integrated circuit, whose power supply leads were all grounded. A curve tracer was then used to test the result of each discharge by examining the circuit's "IV" characteristic. The experiment was then repeated, increasing the negative voltage at 100 volt intervals until the input characteristic was altered so as to make the circuit unusable. Failure was easy to recognize since an overwhelming majority were severely catastrophic short circuits. While ideally the circuit should be functionally tested after each experiment, the time involved in this procedure is prohibitive. It was found in all cases that testing N-type substrate circuits with negative pulses was most destructive, and conversely for tests with positive pulses of P-type substrate circuits.

It should be noted that for devices using field-plate diodes "walkout" was observed, as previously described. Inputs were generally able to survive higher stress voltages if they were tested starting at a relatively small voltage and increasing that voltage until destruction oc-

curred, rather than stressing an untested input initially at some high voltage. Hence, data in Table 3 may be high by 100 to 300 volts. The voltage by which successive tests were incremented was chosen small enough to give good resolution, yet large enough to minimize this effect. Also, in some cases, a normal input characteristic could be restored by a second discharge after the first discharge "destroyed" the input. When this occured, only the final value was recorded, at which point the device was irreversibly damaged.

Some input lines on certain circuits seemed to survive better than others even though they included identical protective circuitry. These inputs were carefully visually inspected and the following layout procedures seem to be responsible for the desirable results:

1. The input network must be protected by a series resistor, even if the input, itself, is taken directly from the bonding pad. The resistor must be large enough to prevent destruction of the network for input voltages in excess of ten kilovolts. Input resistors as best included as long, thin diffused regions if the associated time delay can be tolerated.

2. Non-protected devices, diffusions, and metal lines should be kept away from the protective circuitry and bonding pad areas.

TABLE 3

Test Results of Various

Manufacturer's Protection Networks

Manufacturer	Product	Protection Device	Destruct Volt*
RCA	3031	Dual Zeners	+1750±360
Fairchild	3814	Gated Punch Through (Vss resistor)	−1530±150
Intel	1702	Gated Punch Through (input resistor)	−1480±270
Mostek	4102	Punch Through (input resistor)	+1430±220
Intersil	7511	Gated Punch Through	−1310±550
Mostek	50250	Punch Through (no resistor)	−1170±170
RCA	4001	Dual Diode with diffused resistor	−1160±120
Intel	2101	Gated Punch Through (input resistor, no metal straps)	+1150±530
National	5740	Field Plate Diode	−940±250
National	1101	Field Plate Diode	−620±190
Intersil	7780	Gated Punch Through (small input resistor)	−580±90
Fairchild	3701	Diffused resistor	−460±70
Fairchild	3814	Gated Punch Through (no input resistor)	−450±100
Motorola	14001	Diode	−180±40

*Voltage at which input destruction occurred

3. Where protective circuits must be positioned at some distance from the input pad, at least the input diffused resistor should be included as closely as possible to the input pad. Metal lines to this circuitry must be kept away from other lines or diffusions, especially from power supply lines.

4. If a diode protection scheme is used, diffusions should be liberal in size. Regions of low resistivity near such diffusions, to act as charge collectors, are not nearly as important as a large emitter diode diffusion to substrate (see figure 7).

5. For effective implementation of a gated punch through device, care must be taken to prevent resistive voltage drop along the width of the channel. This may be accomplished by including metal straps and windows over the tops of diffusions.

VI. CONCLUSION

A model of the human body for static electric stress-testing of MOS integrated circuits has been developed and verified by direct tests. The human body was found to be adequately represented for these purposes by a capacitor of about 150 picofarads, a series resistance of about 20K ohms, and an ordinary high voltage relay which purposely exhibits "bounce". Voltages at which circuitry was destroyed were found to be highly correlated between this model and actual human static discharge. The voltage level on the capacitor in the model should be increased by approximately 40% to accurately simulate protection against a charged human touching a circuit with a metal object. Conversely, protection against direct human contact will be simulated to 40% higher voltages than those used in the model. While voltages of up to 30 kilovolts can easily be developed on the human body, the common maximum under normal conditions is two to three kilovolts.

The mechanisms of integrated circuit failure due to static electric over-stress have been identified as oxide breakdown, p-n junction destruction, and metal shorts. It was found that static destruction, in virtually all cases, caused a short circuit to substrate to occur on the input lead being tested. In some cases, a "destroyed" input lead could be restored by restressing that lead. The

phenomenon of "walkout" was observed especially where field plate diode protection was used.

Various protection schemes have been described and tested. These include the input resistor, diode, resistor/diode combination, dual diode, field-plate diode, thick oxide MOS transistor, punch-through device, gated punch through device, and the spark gap. Several devices which consume much area, especially those including diodes with surrounding low resistivity charge collector regions, were found very ineffective. A simple diffused resistor of 1K to 2K ohms provides more protection in much less space.

The most versatile and effective network is a gated punch-through device. Modifications to this device allow it to be used for both moderate protection or high speed applications by changing the nature of the input resistor. The most effective device for situations where area is extremely limited is simply a punch-through device with a series resistor. However, this circuit introduces appreciably more capacitive delay time than the gated puch-through device. The inclusion of a spark gap, where possible, may extend the present protective limit of these circuits from two to three kilovolts to well beyond five kilovolts.

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APPENDIX A

Human Body Models

Source	Ref#	Res	Cap	Volt	Energy	RC
Frank. Inst'.	1	5K	500	20	100	2500
Linholm & Plachy	7	0	250	15	28	0
RCA ST6418	8	560	100	4	0.8	56
Mines Report	9	-	100-300	10	5-20	-
Lenzlinger	13	1.5K	100	10	5	150
Freeman & Beall	15	2K	150	5-20	1.9-30	300
Coule	16	1K	200	5	2.5	200
Mavor	17	-	100	-	-	-
Stephenson	20	1.5K	100	1.5	0.1	150
Hamiter	21	-	200	5	2.5	-
Bendix, Inc'.	22	100	218	3	1	22
Speakman	23	10K	60	10	3	600
Motorola	24	-	300	15	34	-
Petrick	25	25-60	200	30	90	5-12

Abbreviations:

Res = body resistance in ohms

Cap = body capacitance in picofarads

Volt = maximum voltage body may typically charge to

Energy = millijoules of energy delivered

RC = time delay constant of discharge in nanoseconds

APPENDIX B

Negative Resistance Characterisic of Electrical Arcs

During contact bounce, a positive voltage (Vout) of about 10 to 30% of Vstress (where Vstress = -2 kilovolts) was observed across the device under test when its impedance (Rd) was less than about 10K ohm. The magnitude of Vout was proportional to 1/Rd near these conditions. If the arc developed across the switch is represented by a negative resistance, -Ra, then:

$$Vout = IRd$$

$$I = Vstress/(Rd + Rs - Ra)$$

$$\text{so, } Vout = Vstress/(Rd + Rs - Ra)$$

if Rd + Rs < Ra, Vout varies as -Vstress, as observed!

Vita

Jack K. Keller was born in Allentown, Pennsylvania on January 24, 1952 to Mary A. and Wilmer F. Keller. He graduated from Emmaus High School, Emmaus, Pennsylvania in June, 1970. He entered Lehigh University in September, 1970 and received the degree of Bachelor of Science in Electrical Engineering in May, 1974. Since June, 1974, he has been employed by Bell Telephone Laboratories in Allentown, Pennsylvania, where he was a participant in the Graduate Studies Program at Lehigh University.