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A MODEL FOR AN OXIDE ISOLATED SCHOTTKY CLAMPED UP-TRANSISTOR

by

William A. Possanza

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

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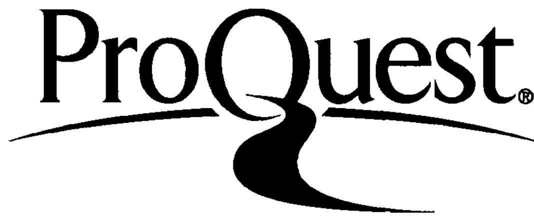

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August 7, 1981

Date

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ABSTRACT

A composite model of an oxide-isolated, Schottky clamped, npn up-transistor is developed as an aid in designing digital bipolar integrated circuits. The composite model is formed by combining a model for a Schottky diode with a model for an up-transistor. Charge-control models for both the Schottky diode and the up-transistor are given along with the equations and parameters governing their operation. The transistor model includes two PNP transistors added to account for parasitic effects associated with the substrate.

Values for parameters used in both the individual diode and transistor models were obtained from electrical measurements made on actual devices. DC characterization is accomplished by performing saturation measurements on the up-transistor, and current-voltage measurements on both the up-transistor and the diode. To characterize the up-transistor's ac response, storage time measurements were performed. A description of how the measurements are made is given in detail.

The accuracy of each model was verified by comparing computer simulations of the dc tests with the actual measurements. The accuracy of the up-transistor's model for ac was checked by simulating its storage time response.

In order to compensate for structural and dimensional differences, the individual models for the diode and the tran-

sistor are modified in order to fit the combined model for the clamped up-transistor. For example, the Schottky diode's series resistance was increased from 42 to 2000 ohms and the saturation current decreased from 2.97 E-12 Amps to 1.36 E-13 Amps. For the up-transistor, the intrinsic base resistance of a parasitic PNP was increased from 9 to 30 Kohms. The accuracy of the combined model is verified in the same manner as the individual models - the predicted values of the computer simulated model are compared with readings on actual devices. The final results show the composite model's agreement with measured data to be quite good.

I. INTRODUCTION

Transistor logic circuits can be classified as either saturating or nonsaturating logic. In saturating logic circuits, the transistor is operated from cutoff to saturation. Although less power is typically required than for nonsaturating logic circuits, the speed is restricted by the storage time of the saturated transistor. To reduce storage time delays in saturating logic, Schottky barrier diodes are used to prevent the transistor's base-collector junction from becoming deeply forward biased. To accomplish this, a Schottky barrier diode with its anode to the transistor's base is connected in parallel to the transistor's base-collector junction. Since the base-collector forward bias voltage is clamped at the threshold voltage of the diode (typically 0.3 - 0.4 volts smaller than that of the transistor's collector-base diode) excess minority charge in the base and collector regions is reduced. Transistors having such a feature are referred to as Schottky clamped transistors.(1)

Recent developments in bipolar technology have led to the fabrication of transistors that operate in the inverse or upward injection mode which exhibit the speed and performance of conventional downward injection transistors.(2) By optimizing the active transistor's profile for upward operation, and utilizing dielectric isolation instead of conventional junction isolation to reduce parasitic capacitance, an "up-transistor"

with high gain and high f_T is obtainable. Such a transistor is very useful in I^2L applications where it is necessary to operate in an upward injection mode. In this paper a model will be developed to predict the operation of such a transistor clamped by a Schottky barrier diode. Information concerning the structure of an oxide-isolated, Schottky clamped, up-transistor is given first. Models are then developed for an oxide isolated Schottky diode and an oxide isolated up-transistor separately. Next, measurements are made on a fabricated device from which parameters used in the models are extracted. Simulations using the models and their parameters are then made and compared to the measurements. Finally, a composite model is developed for a Schottky clamped up-transistor (upshot) device using the individual models for the diode and the transistor. Simulations of the composite model are made and its accuracy tested against measurements made on an upshot device.

II. THE SCHOTTKY CLAMPED UP-TRANSISTOR (UPSHOT)

The upshot transistor to be modeled is composed of two elements, a Schottky diode and an up-transistor as shown in Figure 1. The up-transistor is fabricated in a single step relying on differential diffusion rates.[2] Antimony and boron are successively and selectively implanted into a p-type substrate onto which n-type epi is grown. As the epi is deposited the boron outdiffuses faster than the antimony to form the base. The antimony forms the emitter; the undiffused epi becomes the collector. Contact is made to the base region by diffusing a highly doped p-type layer (P^+ in Figure 1) through the epi. To isolate this structure from other devices and to form an emitter contact region, selective areas of silicon are removed and silicon dioxide grown in its place. Diffusion of an N^+ layer in the emitter and collector regions to ensure ohmic contact completes the fabrication of the up-transistor.

The Schottky diode is formed during metallization. By extending platinum silicide (PtSi) over the epi region when making contact to the P^+ base region, two contacts are formed simultaneously, an ohmic contact to the P^+ extrinsic base, and a rectifying contact to the collector epi region. When metal is then deposited over the PtSi to contact the base, contact to the collector is then made through a Schottky diode. Because the upshot transistor consists of two devices integrated into one, as

indicated by the circuit symbol in Figure 1, separate models will be developed.

III. THEORY AND STRUCTURE OF A SCHOTTKY BARRIER DIODE

A Schottky barrier diode (SBD) is a metal-semiconductor diode formed when a metal (PtSi) is brought in contact with a lightly doped (n-type) semiconductor. At thermal equilibrium, the Fermi levels in the two materials must be coincident. In the case of an ideal contact (no surface states) negative charge will flow from the semiconductor to the metal for this to occur. Thus, the conduction and valence bands in the semiconductor become bent at the interface (Figure 2a). It is this bending effect of the bands at the surface that sets up a barrier height ϕ_{Bo} for electrons in the metal, and a contact potential V_{bi} for electrons in the semiconductor.

In the case of the diode to be modeled where the work function of the metal is greater than the work function of the semiconductor, a space charge layer will be formed at the interface. This space charge layer is maintained by the electrons in the metal at the interface, and a distributed positive charge of ionized donors in the semiconductor. If a negative voltage is then applied to the semiconductor, the barrier height for electrons going from the metal to the semiconductor will remain unchanged, whereas the contact potential for electrons going from the semiconductor to the metal will be lowered (Figure 2b). Therefore, for small changes in negative voltages a large flux of electrons will be injected from

the semiconductor into the metal, hence a large current will flow. If a positive voltage were to be applied to the semiconductor it would increase the contact potential for electrons in the semiconductor, while still leaving the barrier height the same (Figure 2c). Under this condition only a small number of electrons in the semiconductor would be injected into the metal, hence a small current flows. It is this changing of the contact potential while the barrier height remains essentially constant that gives this device its rectifying characteristic.

Since electrons are injected into the metal from the semiconductor under forward bias low level injection conditions (-V applied), the diode operates as a majority carrier device. As a consequence the storage time (τ_D) of minority carriers is eliminated and an inherently fast response is obtained. Typical storage times are on the order of tenths of a nanosecond.

The Schottky diode to be modeled is a unguarded diode as opposed to a guarded one. The difference between them is that a guarded diode has an extra p guard ring layer diffused around its periphery to reduce electrode "sharp-edge" effects.[3] Electrode "sharp-edge" effects result from high fields at the edges of the metal which give rise to excess leakage current and a low breakdown voltage. To avoid "sharp-edge" effects on the clamped up-transistor without the use of a p guard ring, the metal edges

of the diode are extended over the isolating oxide.

The unguarded Schottky diode modeled is structured as shown in Figure 3. It is fabricated by first diffusing a highly doped N^+ layer into a p-type substrate. An epitaxial N^- layer is then grown across the entire region, during which the N^+ layer diffuses upward into the epi. Through a series of photoresist and etching steps two regions are defined in the epi layer over the N^+ buried layer. One region will serve as an ohmic contact to the N^- side of the diode, and the other is where the Schottky diode is to be formed. In order to isolate these two regions from each other, and other circuit elements, a thick layer of silicon dioxide is grown in the areas that were etched out. An ohmic contact to the N^- side of the diode is ensured by diffusing a highly doped N^+ layer into the one epi region. In the other epi region the diode is formed by sintering a thin layer of platinum that was sputtered onto the silicon surface. This forms a layer of platinum silicide (metal) on the lightly doped epi. Finally, metal is sputtered on the PtSi to serve as a contact to the "p-side" of the diode, and on the N^+ layer to contact the "n-side" of the diode.

The unguarded Schottky diode formed can be represented by the circuit element shown in Figure 3 where the labels A and B relate the terminal connections on the structure to the appropriate terminals on the circuit.

IV. CIRCUIT MODELING OF A SCHOTTKY DIODE

A circuit model will be developed for an unguarded Schottky diode by first deriving the equations for the parameters governing the operation of the diode. A composite model of the diode is then formulated, and I-V and C-V measurements made on a fabricated device. From the measurements and the model, a computer simulation is made. The results of the computer simulation are then compared with the electrical measurements in order to determine the model's accuracy.

For a Schottky diode three main properties must be considered to model the diode effectively. They are, current flow, capacitive effects, and minority storage time. For deriving the equations governing current flow and minority storage time an approach presented by Sze(4) is used, and for capacitance effects a treatment by van der Ziel is used.(5)

A. Current Flow

Current transport theory in a Schottky diode can be described by differing approaches. The one to be used is the thermionic emission theory.(4) In using this theory two assumptions are made; (1) electron collisions within the depletion region are neglected and, (2) the barrier height $q\phi_{Bn}$ is much larger than kT.

Start by taking the equation for the electron current

density due to thermionic emission of electrons from the semiconductor to the metal:

$$J(s\rightarrow m) = qn(kT/2\pi m^{*})^{1/2} \exp(-m^{*} v_{ox}^{2}/2kT), \qquad (4.1)$$

where v_{ox} is the minimum velocity in x-direction to surmount the barrier and is given by

$$v_{ox}^{2} = 2q/m^{*} (V_{bi} - V_{D}). \qquad (4.2)$$

V_{bi} and V_{D} are the built-in potential and junction voltage, respectively (Figure 4). The electron density n in equation (4.1) can be expressed as

$$n = 2(2\pi m^{*} kT/h^{2})^{3/2} \exp(-qV_{n}/kT) \qquad (4.3)$$

where

$$V_{n} = E_{C} - E_{F}. \qquad (4.4)$$

Substituting equations (4.3) and (4.2) into (4.1) and using the relationship for the barrier height at low electric fields

$$\phi_{Bn} = \phi_{Bo} = V_n + V_{bi}, \tag{4.5}$$

equation (4.1) can be rewritten as

$$J(s \rightarrow m) = A^* T^2 \exp(-q\phi_{Bn}/kT)\exp(qV_D/kT) \tag{4.6}$$

where

$$A^* = 4\pi q m^* k^2 h^{-3} . \tag{4.7}$$

Under an applied voltage, the barrier height remains unchanged for electrons moving from the metal to the semiconductor. As a result, in thermal equilibrium when $V_D = 0$, the following expression must hold:

$$J(s \rightarrow m) = J(m \rightarrow s). \tag{4.8}$$

Therefore, the corresponding current density for electrons going from the metal to the semiconductor is obtained by setting $V_D = 0$ in equation (4.6):

$$J(m \rightarrow s) = -A^* T^2 \exp(-q\phi_{Bn}/kT). \tag{4.9}$$

The total current density is given by the sum of equations (4.6) and (4.9)

$$J_D = K_s[\exp(qV_D/kT)-1] \qquad (4.10)$$

where

$$K_s = A^* T^2 \exp(-q\phi_{Bn}/kT). \qquad (4.11)$$

Noting the fact that at high electric fields

$$q\phi_{Bo} = q\phi_{Bn} + q\Delta\phi, \qquad (4.12)$$

equation (4.12) can be rearranged and substituted for ϕ_{Bn} in equation (4.11):

$$J_D = A^{**} T^2 \exp(-q\phi_{Bo}/kT)\ [\exp kT^{-1}(q\Delta\phi + qV_D)], \qquad (4.13)$$

where the condition $V \geq 3kT/q$ was used to neglect the -1 term. In equation (4.12) $q\Delta\phi$ accounts for barrier lowering due to image force and electric field effects. Also, the Richardson constant A^* (120 $Amp/cm^2/{}^oK^2$) in equation (4.11) was replaced by A^{**} (effective Richardson constant) in equation (4.13). This was done to include the effects of electron optical-phonon scattering

and quantum mechanical reflection at the interface.

Since A^{**} and $q\Delta\phi$ are functions of the applied voltage, the forward J-V characteristics (for $V \geq 3kT/q$) cannot be represented by the simplified expression

$$J \sim \exp(qV_D/kT) \tag{4.14}$$

but rather by

$$J \sim \exp(qV_D/nkT), \tag{4.15}$$

where n takes into account the dependence of A^{**} and $\Delta\phi$ with voltage.

As a result, equation (4.13) can be replaced by the following simplified equation:

$$J_D = J_s\,[\exp(qV_D/nkT)-1]. \tag{4.16}$$

J_s is the extrapolated current density at zero voltage. Multiplying equation (4.16) by the diode area A_d yields the diode current as a function of voltage:

$$I_D = A_d J_s[\exp(qV_D/nkT)-1]. \tag{4.17}$$

In considering the current flow through the diode, the series resistance of the diode must also be included. This is because at high currents the $I_D R$ drop becomes larger than the junction voltage drop. As a result, the applied voltage (V) is no longer equal to the junction voltage (V_D). To account for this a series resistance R_s must be included.

B. Capacitance Effects

Due to the transfer of electrons from the semiconductor to the metal, a space charge layer as described in Section III is created and band bending occurs. When the applied voltage across the diode is varied the amount that the bands bend at the surface will also vary. As the bending of the bands increases or decreases, so too will the amount of ionized donor charge. The result is an incremental change in charge for an incremental change in voltage, or in other words, capacitance effects.

The voltage distribution in the space charge layer can be described by Poisson's equation:

$$d^2\Psi/dx^2 = -\rho/\epsilon\epsilon_o. \qquad (4.18)$$

The space-charge density ρ due to ionized donors, can be expressed as

$$\rho = +q[N_d - n]. \qquad (4.19)$$

Due to the fact that the net space charge is zero for $X \geq W$ (W is the depletion width), it follows that the region of interest is between X = 0 (interface) and X = W. Therefore using the depletion approximation,

$$\rho = qN_d \;, \; 0 \leq x \leq W \tag{4.20}$$

$$\rho = 0 \;, \; x \geq W \tag{4.21}$$

the potential in the space charge layer can now be solved for using the following boundary conditions:

$$\Psi = 0 \;, \; x = 0 \tag{4.22}$$

$$\Psi = V_{bi} - V_D \;, \; x = W \tag{4.23}$$

$$d\Psi/dx = 0 \;, \; x = W. \tag{4.24}$$

Substituting (4.20) into (4.18) and integrating once, using the initial condition (4.24) at X = W, you get

$$d\Psi/dx = -qN_d/\varepsilon\varepsilon_o \,(x - W) \;, \; 0 \leq x \leq W. \tag{4.25}$$

Integrating once more and applying the condition (4.22) yields

$$\Psi(x) = -qN_d/\varepsilon\varepsilon_o \, [(1/2)x^2 - xW] \, , \; 0 \leq x \leq W. \qquad (4.26)$$

Applying the condition (4.23) at $X = W$ yields the following relation for the thickness W of the space charge region,

$$V_{bi} - V_D = +(qN_d/2\varepsilon\varepsilon_o)W^2 \qquad (4.27)$$

where

$$W = [(2\varepsilon\varepsilon_o/qN_d)(V_{bi} - V_D)]^{1/2}. \qquad (4.28)$$

Since the space charge layer acts as a capacitor, the total charge Q_D per unit area of the metal is

$$Q_D = -qN_dW = -[2\varepsilon\varepsilon_o qN_d(V_{bi} - V_D)]^{1/2}. \qquad (4.29)$$

The small-signal capacitance per unit area (C_D) is defined as the rate of change of Q_D with junction voltage V_D:

$$C_D = dQ_D/dV_D = (q\varepsilon\varepsilon_o N_d)^{1/2}[2(V_{bi} - V_D)]^{-1/2}. \qquad (4.30)$$

C. Storage Time

Under low-injection, low forward bias conditions the Schottky diode operates as a majority carrier device, and the minority current is dominated by its diffusion term which is negligible. However, by increasing the forward bias voltage sufficiently a bulk electric field is produced that results in a significant minority carrier drift component. For further increases in bias, the drift component will eventually dominate the minority carrier current and increase as the square of the forward current.(6) This results in a build-up of minority charge in the quasi-neutral region (epi). The storage effects of this charge must then be taken into consideration in order for the diode to be modeled completely.

The minority storage time is defined to be the charge of minority carriers stored in the quasi-neutral region per unit current density. For a high current limit(4) τ_D is given by

$$\tau_D = (qn_i^2 L_p / N_d J_s). \qquad (4.31)$$

The above equation is based on the assumption that the minority carriers flowing through the epi region recombine at the epi buried-layer interface. Since it is the high current limit it gives a worse case storage time, and device response.

D. Composite Model

A composite model of a Schottky diode can be structured from the parameters governing the diode's operation. The capacitance effects and minority charge storage are modeled by a single capacitor whose charge Q_D is given by the following expression:

$$Q_D = \tau_D I_D + CJO \int_{V=0}^{V_D} [1 - V/V_{bi}]^{-m_d} \, dV. \qquad (4.32)$$

The first term in equation (4.32) is a relationship which takes into account the minority storage effects, and the second term a model for the depletion space charge capacitance as proposed by Poon and Gummel.[7] The depletion model is characterized by three parameters: the zero bias depletion capacitance, CJO, the depletion potential, V_{bi}, and the grading coefficient, m_d. Current flow in the junction of the diode is modeled by a voltage dependent current source whose relationship is given by equation (4.17):

$$I_D = A_d J_s \, [\exp(qV_D/nkT)-1]. \qquad (4.33)$$

Since V_D is the junction voltage it is referenced across the

current source. Both the current source and space charge capacitance are physical properties within the same region, therefore the two are in parallel. The model bears this out (Figure 5). To complete the model, a series resistance R_s is added to include the effect of the epi region. Shown also in Figure 5 is the circuit element for reference.

V. MEASUREMENTS OF A SCHOTTKY DIODE

The next step in modeling an unguarded Schottky diode was accomplished by measuring its I-V and C-V characteristics. In the following sections, a brief description of how the measurements were made, along with the procedures used for determination of the diode's parameters are given. Measurements of the I-V characteristics were performed at three different temperatures; 25^oC, 50^oC, and 75^oC. The C-V measurements were performed at room temperature. The resulting parameters derived from this data are listed in Table I. For the case of the storage time, a calculated value rather than measured value was used. This was accomplished using equation (4.31) along with known values for L_p and N_d characteristic of the N^- epi region.

A. I-V

The current voltage characteristics were determined by using the test circuit shown in Figure 6. Since the reverse leakage through the diode for voltages of interest (0 to -10V) is negligible, only the forward bias case was measured. Measurements were made by applying negative voltages to the substrate, and grounding the p-side of the diode. Voltages ranging from 0 to -1V, in increments of -0.025 V, were applied to the diode using a Lomac power supply (PS2). Current through the diode was measured by two Keithley 445 picoammeters (PAM 2 & 4), while the voltage drop across the diode was recorded by a Fluke

8502A (DDM3) digital voltmeter. The temperature of the diode was controlled by a Temptronix thermo-chuck.

The results of the I-V measurements are shown in Figure 7 for the various temperatures. From the I-V plot at 25°C; I_s, R_s, and n were determined. The saturation current and n were derived by fitting equation (4.17) to data points taken from the linear low voltage region of Figure 7. I_s was found by extrapolating the value for current at zero bias, and n from the slope of the data. The series resistance R_s was derived from a consideration of the current roll off at the higher forward bias. In this region, the applied voltage is dropped largely across the epi region.

B. C-V

Measurements of capacitance as a function of voltage were made using a Boonton 76A Automatic Capacitance Bridge. Data were taken by applying a positive voltage ranging from 0 to 5V, to the semiconductor side of the diode at the same time a small ac signal was applied to the metal. The small signal capacitance data (CD) versus voltage (V) is shown in Figure 8. By fitting the depletion capacitance equation proposed by Poon and Gummel to the data

$$C_D = CJO\,[\,1 - V/V_{bi}]^{-m_d}, \qquad (5.1)$$

values for CJO, V_{bi}, and m_d can be obtained. For the fit (C1) shown in Figure 8 the values listed in Table I were extracted.

VI. SBD - COMPUTER SIMULATIONS

To test dc accuracy of the model and the derived parameters, computer simulations of the I-V characteristics were made. The software program used for the simulations was ADVICE.[8] ADVICE is a circuit simulation program that contains dc and ac analyses capabilities. Simulations were performed at the same temperatures at which data had been obtained. The results of the circuit simulations are shown in Figure 7. The agreement between data and simulation was very good for each temperature tested over 6 decades of current. Due to the fast switching response of the diode, ac measurements and simulations were deferred until a study of the clamped up-transistor was made.

VII. CIRCUIT MODELING OF AN UP (NPN) TRANSISTOR

The transistor to be modeled in this section is structured as shown in Figure 9. This transistor except for slight dimensional differences in the buried layer, contact window, and isolation regions is identical to the upshot device described in Section II. These differences account for the fact that an upshot device has a SBD located between the collector and base contact regions, whereas the up device does not. As in the case of the upshot, the buried N^+ layer forms the emitter of the transistor, the P up diffused region - the base, and the lightly doped N^- epi on top - the collector. The doping profile of this structure is also the same as that of the upshot.

In modeling this device, the same approach outlined in Section IV for a SBD is used. Equations governing the operation of the transistor are given from which a composite model is formulated. Parameters used in the equations are then extracted from measurements made on a fabricated device. Finally the accuracy of the model is tested by comparing the measured characteristics to those simulated on a computer.

Before a charge control model of the up (NPN) transistor can be formulated a consideration of the structure of the device must be undertaken. Since the up-transistor is fabricated into a p-type substrate the device to be modeled becomes more complicated. The device is no longer a single NPN transistor,

but will be modeled as three transistors, the primary transistor (NPN) plus two parasitic PNP transistors due to the substrate. One PNP is formed by the up base, the buried layer, and the substrate (PNP2 in Figure 9). The second is formed by the P^+ base contact, the buried layer and the substrate (PNP1 in Figure 9). When a forward bias is applied to the emitter-base junction of the NPN, the two PNP transistors turn on. As a result, when the NPN is operated in the upward mode, base current from this transistor will be shunted to the substrate. Therefore, in addition to the charge control model for the NPN, a model for the PNP's is needed as well.

To facilitate the modeling of both the NPN and PNP structures, equations similar to the Gummel-Poon[9] model of a transistor are used. With the exception of polarity, the modeling of an NPN or PNP transistor is identical. The equations governing the transistor based on the Gummel-Poon model can be separated into three areas, (1) resistive effects, (2) current flow, and (3) charge storage. The polarity in the following analysis assumes a NPN transistor.

A. Resistive Effects

In describing the resistive effects in a transistor, the emitter, base, and collector regions must be considered. The collector resistance RC in the up-transistor is due to the metal contact (labeled C in Figure 9), and the N^+ layer diffused into

the epi (assuming the N^- region is totally depleted). This resistance is bias independent, and can be represented by a single passive resistor. The emitter resistance RE, which is also bias independent, is due to the metal contact (labeled E), the N^+ diffused layer, N^- epi region, and the lateral resistance of the buried-layer under the oxide isolation region. A passive resistive element is also used to model this resistance.

The base resistance, RB, which is due to the metal contact (labeled B), the P^+ region, and the lateral resistance associated with the up diffused base region, is more complicated. It can be divided into two components, an extrinsic component, RBX, and a zero bias intrinsic component at low injection levels, RBI. In order to account for high level injection and the modulation of the resistivity of the active base region, RBI is modified by Q (normalized base charge). The total base resistance is then expressed as,

$$RB = RBX + RBI/Q. \qquad (7.1)$$

B. Current Flow

Current flow in a transistor (neglecting resistive and capacitance effects) can be broken up into three main parts, I_n, I_{be}, and I_{bc}. I_n is the emitter-to-collector electron current which would flow in an ideal transistor. I_{be} and I_{bc}, are the

base-emitter and base-collector recombination currents. These currents as shown in Figure 10 are related to the intrinsic currents of a transistor by the following expressions,

$$I_c' = I_n - I_{bc} \tag{7.2}$$

$$I_b' = I_{be} + I_{bc} \tag{7.3}$$

$$I_e' = -I_n - I_{be} \tag{7.4}$$

where the primes denote the fact that these are junction rather than terminal currents.

The ideal electron current, I_n, can be derived from a detailed analysis of current flow in the base region of the transistor. To simplify the analysis only the results of a derivation performed by Getreu(10) based on the Gummel-Poon(9) model are given. The electron current as derived by Getreu is,

$$I_n = (I_s/Q)[\exp(qV_{be}/kT) - \exp(qV_{bc}/kT)] \tag{7.5}$$

where I_s (transport saturation current) and Q (normalized base charge) are defined as,

$$I_s = (qD_n n_i^2 A)\left[\int_{x_{EO}}^{x_{CO}} N_A(x)\, dx\right]^{-1} \tag{7.6}$$

and

$$Q = (Q_b/Q_{bo}). \tag{7.7}$$

In equation (7.6), $N_A(x)$ is the base doping profile, and A is the one-dimensional cross-sectional area of the base. The limits of integration x_{EO} and x_{CO} are taken from the base side of the emitter-base space charge layer to the base side of the collector-base space charge layer. The parameter I_s can be determined from measured data at low level since it is constant for a given device. The lower case subscripts on V_{be} and V_{bc} denote the fact that these are junction, not terminal voltages. Q in equation (7.5) takes into account the effects of high level injection and base width modulation. Q_b and Q_{bo} in equation (7.7) are defined as the total base charge (due to holes) at a given bias and the total base charge at zero bias, respectively. The normalized base charge Q is described in further detail in the next section.

The remaining two currents I_{be}, and I_{bc}, are identical in principle, but differ in that the former governs the base-emit-

ter junction, and the latter the base-collector junction. The emitter-base recombination current is given by[9]

$$I_{be} = I_1[\exp(qV_{be}/kT)-1] + I_2[\exp(qV_{be}/n_E kT)-1] \qquad (7.8)$$

where I_1 and I_2 are defined to be the ideal and non-ideal base-emitter saturation currents. The first term in equation (7.8) is the standard expression for current flow through a p-n junction. The second, or non-ideal term, accounts for the drop off of gain at low currents in the forward mode of operation. Included in the expression is n_E, the base-emitter emission coefficient (typical values 1-2).

The base-collector recombination current is similar to I_{be} and is given by,

$$I_{bc} = I_3[\exp(qV_{bc}/kT)-1] + I_4[\exp(qV_{bc}/n_C kT)-1] \qquad (7.9)$$

where I_3 and I_4 are the ideal and non-ideal base-collector saturation currents. The terms in this equation are similar to those in equation (7.8) with the exception that the non-ideal term here causes fall off of gain at low currents in the reverse mode of operation. The emission coefficient for the base-collector junction is n_C. Taking the equations for I_n, I_{be}, and I_{bc} and substituting them into equations (7.2) and (7.3)

yields,

$$I_c' = I_s/Q[\exp(qV_{be}/kT) - \exp(qV_{bc}/kT)] - I_3[\exp(qV_{bc}/kT)-1] - I_4[\exp(qV_{bc}/n_C kT)-1] \tag{7.10}$$

for the intrinsic collector current, and

$$I_b' = I_1[\exp(qV_{be}/kT)-1] + I_2[\exp(qV_{be}/n_E kT)-1] + I_3[\exp(qV_{bc}/kT)-1] + I_4[\exp(qV_{bc}/n_C kT)-1] \tag{7.11}$$

for the intrinsic base current. Equations (7.10) and (7.11) can be represented by two voltage dependent current sources.

C. Charge Storage

In the up-transistor being modeled there are three areas where the effects of charge storage must be considered. They are, (1) the base-emitter, (2) base-collector, and (3) the emitter-substrate junctions. Due to the structure of this transistor there are no base-substrate charge storage effects. Charge stored due to a junction can be divided into two types - depletion layer and diffusion charge. Since the substrate is always held at a constant negative potential during the operation of the transistor, the emitter-substrate junction is always reverse biased. The charge stored in this junction is a depletion charge, and because of the constant bias is modeled by

a bias independent capacitor (C_{es}).

In considering the base-emitter and base-collector storage effects, both depletion and diffusion charges have to be included. The total charge associated with each junction can be expressed as,

$$q_{be} = q_{je} + q_{de} \tag{7.12}$$

for the base-emitter junction and,

$$q_{bc} = q_{jc} + q_{dc} \tag{7.13}$$

for the base-collector junction. Depletion charge storage is accounted for by q_{je} and q_{jc}, whereas q_{de} and q_{dc} account for diffusion effects. The depletion charges can be represented by the model proposed by Gummel and Poon[7],

$$q_{je} = CJE \int_{V=0}^{V_{be}} [1 - V/PE]^{-m_e} \, dV \tag{7.14}$$

and

$$q_{jc} = CJC \int_{V=0}^{V_{bc}} [1 - V/PC]^{-m_c} \, dV \tag{7.15}$$

where CJE, CJC, PE, PC, m_e and m_c have the same physical significance as CJO, V_{bi}, and m_d explained earlier in the modeling of a SBD.

The diffusion charges q_{de} and q_{de} are given by

$$q_{de} = \tau_{FO}(I_s/Q)[\exp(qV_{be}/kT)-1] \qquad (7.16)$$

and

$$q_{dc} = \tau_{RO}(I_s/Q)[\exp(qV_{bc}/kT)-1]. \qquad (7.17)$$

In equations (7.16) and (7.17) τ_{FO} and τ_{RO} are the zero bias forward and reverse base transit times. As a result, the total charges q_{be} and q_{bc} are modeled as two non-linear capacitors.

Having completed the analysis of charge storage effects, the normalized base charge Q as defined by equation (7.7) can now be related to measurable parameters. In this equation Q_b (the total base charge) is the sum of the zero bias base charge Q_{bo}, and the total base-emitter and base-collector junction charges:

$$Q_b = Q_{bo} + q_{je} + q_{jc} + q_{de} + q_{dc}. \qquad (7.18)$$

Using equation (7.18), the normalized base charge becomes

$$Q = 1 + Q_{bo}^{-1}[q_{je} + q_{jc} + q_{de} + q_{dc}]. \tag{7.19}$$

Four additional definitions are made:

$$V_{BO} = (Q_{bo}/CJE) \tag{7.20}$$

$$V_{AO} = (Q_{bo}/CJC) \tag{7.21}$$

$$I_{KF} = (Q_{bo}/\tau_{FO}) \tag{7.22}$$

$$I_{KR} = (Q_{bo}/\tau_{RO}) \tag{7.23}$$

where equations (7.20) and (7.21) are the zero bias Early voltages, and equations (7.22) and (7.23) the intercept currents for high level injection. With the above definitions and equations (7.14) through (7.17), the normalized base charge equation (7.19) can be determined.

D. Composite Model

Using the equations presented in the previous sections a model of the up NPN transistor can be made (Figure 11). Each of the three effects, resistive, current flow, and charge storage are accounted for. Since the actual device consists of two parasitic PNP's in addition to the NPN (Figure 9), the model

shown in Figure 11 must be modified. To do this an assumption is made that all of the charge storage effects, q_{bc}, q_{be}, and C_{es} are associated with the NPN transistor, and can be eliminated from the models of PNP1 and PNP2. Certain additional circuit elements can also be eliminated from the models of the PNP's because their effects are included in the model of the NPN. They are the external resistances RBX, RC, and RE. The last parameter in the modeling of the PNP's to be taken into account before a composite model can be made is RBI. From a consideration of the structure in Figure 9, the intrinsic base resistance can be removed from the model of PNP2. This is because since the base of PNP2 serves also as the emitter of the NPN, intrinsic base resistance effects are eliminated. In the model of PNP1, RBI is included because the presence of the buried-layer between PNP2 and PNP1 behaves as an intrinsic resistance to the base current of PNP1. The final charge control model of the oxide isolated up-transistor is shown in Figure 12.

VIII. MEASUREMENTS OF AN UP-TRANSISTOR

In order to characterize the performance of the up-transistor and derive the parameters for its model, several dc and ac measurements were made. For the dc analysis, current-voltage, gain, and saturation measurements were made in both the upward (forward) and downward (reverse) injection modes. AC characterization was made by performing capacitance-voltage, transit time, and storage time measurements. Model parameters for the composite up-transistor were extracted from the current-voltage, capacitance-voltage, and transit time measurements. The remaining measurements, gain, saturation, and storage time, were made in order to test the accuracy of the model, and not for the determination of any parameters. In the following sections, a description of how these measurements were made is given, along with the methods used for extracting the model parameters.

A. I-V

Current-voltage measurements on the up-transistor were made in the upward and downward injection modes by biasing the transistor in the active region. The test circuit used for measuring the forward and reverse characteristics is shown in Figure 13. Data for each mode of operation were taken at 31°C. In both cases, the emitter, collector, and substrate were each connected to a power supply through a picoammeter. Voltage

readings were made on the emitter-base junction by the digital voltmeter DMM3. The test equipment used was the same type as that described earlier in the section on current measurements of a Schottky barrier diode. For measurements made in the upward direction, the base-collector and emitter-substrate junctions were reverse biased by applying a constant 2 V (PS1) and 5 V (PS3), respectively. The base-emitter junction was then forward biased (PS2) from 0.5 V t0 1.0 V, in increments of 20 mV. Three terminal current readings, I_C through PAM1, I_B through PAM2, and I_S (substrate current) through PAM3 were made at each voltage increment. Since the parasitic PNP's turn on in the forward injection mode, I_S is the total current flowing through these transistors. The results of the current versus voltage measurements in the upward mode are shown in Figure 14. Measurements in the downward active mode were made in a similar manner, except that the base-collector junction was forward biased, and the base-emitter junction reverse biased. In this direction, only two terminal currents, I_E through PAM4, and I_B through PAM2 were measured. I_S, the substrate current, in the downward mode is negligible because the substrate is inactive in this direction. Measurements for downward injection are shown in Figure 15.

Gain versus current, for each mode of operation, was calculated from the data presented in Figures 14 and 15 by using

the following expressions;

$$\beta_F = (I_C/I_B) \tag{8.1}$$

for upward injection and,

$$\beta_R = (I_E/I_B) \tag{8.2}$$

for downward injection. The results are shown in Figures 16 and 17.

Values for the parameters governing the dc operation of the composite model were determined through the use of a parameter extraction program called PAREX.[11] PAREX is an algorithm whereby dc parameters based on the Gummel-Poon model are determined from the current-voltage characteristics of a bipolar transistor. By inputing data from the forward and reverse (Figures 14 and 15) low current regions of operation into PAREX, the following parameters were extracted;[11,12] V_{AO}, V_{BO}, n_E, n_C, I_3, and I_4 for the NPN transistor model and, I_1, I_2, and I_S for the NPN and PNP models. The remainder of the modeling parameters were determined from the high current region of operation.[12] This included; I_{KF}, I_{KR}, RC, RE, and RBI of the NPN transistor, and RBI and I_{KF} of PNP1. The final extracted values for the dc parameters are listed in Table II.

B. Saturation

Since the up-transistor operates into the saturation region for digital logic, its performance in this mode had to be characterized. Saturation measurements in both the forward and reverse directions were made at ambient temperature (25°C). The test circuit used for these measurements is shown in Figure 13. The device was connected to the test circuit in the same manner described earlier for making current-voltage measurements. In order to perform saturation measurements, two interrelated bias conditions were controlled and a third was measured. For upward injection, the degree of saturation (V_{CE}) and the base current (I_B) at which it occurs, were controlled, and the collector current I_C was measured. To achieve these conditions the base-emitter voltage (PS2) and base-collector voltage (PS1) were adjusted to maintain a constant I_B as the collector-emitter voltage (V_{CE}) varied from 20 mV to 600 mV, in increments of 20 mV. Then for a fixed base current, I_C was measured as a function of V_{CE} for upward injection. Repeating this procedure for various base currents resulted in the data shown in Figure 18. Downward injection saturation measurements were made in the same fashion, except the emitter current (I_E) was measured as a function of the emitter-collector voltage (V_{EC}). The results for downward injection are shown in Figure 19.

C. C-V

Depletion capacitance measurements on the up-transistor were made on the emitter-substrate, base-emitter, and base-collector junctions. Measurements were performed on the base-emitter and base-collector junctions using a Boonton 76A Automatic Capacitance Bridge. For the emitter-substrate capacitance measurements, a capacitance meter (Princeton Applied Research - 410) rather than a bridge was used. A capacitance meter was needed because measurements had to be made with respect to ground, a condition which is unallowable for the bridge. Measurements on the junction capacitances were made at 31°C. In each case data were taken by applying a positive voltage from 0 to 5 volts to the n-side of the junction at the same time an ac signal was applied to the p-side. Capacitance data versus voltage for the base-emitter junction are shown in Figure 20, and for the base-collector junction in Figure 21. By fitting the depletion capacitance equation (5.1) to the data for the base-emitter (line C1 in Figure 20) the following model parameters were determined, CJE, PE, and m_e. Similarly, by using the same approach for the base-collector junction a best fit of equation (5.1) to the data (line C1 in Figure 21) yields CJC, PC, and m_c. The extracted values for these parameters are listed in Table II. Although the emitter-substrate junction has the same capacitance versus voltage relationship (Figure 22) it was

not necessary to fit this data to equation (5.1). The reason is that because the emitter-substrate junction is always sufficiently reversed bias its capacitance remains approximately constant. Therefore, only a single capacitance value is needed to model this junction. The value listed in Table II is based on the fact that the substrate was held at a constant -5 volts.

D. Transit Times

The zero bias transit time for upward injection (τ_{FO}) was determined from measurements made on the up-transistor's unity-gain bandwidth (f_T). The unity gain bandwidth is defined to be that frequency at which the small signal common-emitter current gain becomes equal to one. Values for f_T, in upward injection, were obtained by utilizing a test circuit and procedure similar to the one outlined in a thesis presented by C. E. Williams.[13] From this data, a plot of $1/f_T$ as a function of $1/I_c$ was made (Figure 23). By fitting a straight line to the low current region and extrapolating to $1/I_c = 0$, an intercept value ($1/f_A$) can be obtained. From this intercept ($1/f_A$) the following expression can then be used to find τ_{FO}.

$$\tau_{FO} = (1/2\pi)(1/f_A) - C_{jc}(V_{BC})\ RC \qquad (8.3)$$

In the above equation, $C_{jc}(V_{BC})$ takes into account the effect of the base-collector depletion capacitance on f_T. Since this term

is small regardless of the reverse bias applied to V_{BC}, the forward transit time can be found directly from the intercept value $1/f_A$. For the data shown in Figure 23, τ_{FO} was found to be 590 psec. For the reverse transit time a similar procedure can be applied from which an extrapolated value for $1/f_A$ of 3.323 nsec, or τ_{RO} of 529 psec was obtained.

E. Storage Time

To test the ac response of the up-transistor, storage time measurements were performed by switching the transistor from saturation ("on") into cutoff ("off"). Storage time (t_s) is defined as the time it takes the collector current to diminish to 90% of its full value, once the base current is cut off. The base current is said to be cut off when it has been reduced to 90% of its full value. Measurements were made using the biasing circuit shown in Figure 24 at 25°C. The transistor was switched "on" and "off" by the voltage pulse generator V_{in}. The base current in the "on" state was determined by R_1 and the V_{BE} drop of the transistor:

$$I_B = (V_{in} - V_{BE})/R_1. \qquad (8.4)$$

The collector current, in this state, was limited by the load resistance R_L. To ensure saturation in the "on" condition the

following expression was satisfied;

$$\beta I_B \geq I_C \tag{8.5}$$

where I_B and I_c are the base and collector terminal currents. Storage time measurements were then made by monitoring the delay between input and output currents when the input pulse went low. By changing the amplitude of the pulse, hence base current drive, the degree to which the transistor was saturated could be varied. Measured results for storage time as a function of I_B are shown in Figure 25. As expected, longer delay times were measured for increasing values of base current.

IX. UP-TRANSISTOR - COMPUTER SIMULATIONS

The composite model for the up-transistor (Figure 12) was tested for its dc and ac accuracy by simulating its performance on a computer. The software program used was ADVICE.[11] The Gummel-Poon parameters used in the simulations were those extracted from the measurements, and listed in Table II. Computer simulations of the measurements were made by utilizing the composite model in an equivalent ADVICE circuit that matched the test circuit for that case. Simulations of the model were performed at the same temperatures at which measurements were made. For comparison purposes, the results of the model's simulations are shown in the same graphs as the measured data. From Figures 14 through 19 it can be noted that the simulated dc performance of the up-transistor's model agrees very well to the measurements made for that test. The ac accuracy of the model, as shown in figure 25, is also quite good.

X. CIRCUIT MODELING OF AN UPSHOT TRANSISTOR

The model for the upshot transistor is developed by modifying and combining the model for the Schottky diode (Figure 5) with the model for the up-transistor (Figure 12) developed separately in preceding sections. In integrating the diode and the up-transistor together slight dimensional and structural changes were required. To account for this, critical parameter values were recalculated wherever possible.

For the diode new values for I_s and R_s were calculated. Scaling of the diode's area led to a value of I_s = 1.361E-13 Amps. Because the epi-region is pinched off by the up diffused base, the series resistance, R_s, was calculated to be 1500 ohms for the structure shown in Figure 1.

The additional space between the N^+ collector and the P^+ base contact required to add the clamping diode necessitated a larger buried-layer for the upshot transistor than for an up-transistor. This factor changes the value of RBI of PNP1. However, because of dependence on other parameters, RBI could not be calculated directly so the value determined for RBI in the up-transistor model was used as a first approximation. Values for all other parameters on the upshot transistor are assumed the same as the values used for the individual diode and up-transistor models as listed in Tables I and II.

Figure 26 shows the resulting model for an upshot transistor. It was simplified by replacing the charge control representation for the NPN and two PNP's with their circuit element symbols. The N^- side of the diode was connected to the intrinsic, rather than extrinsic collector terminal, because the diode's current combines with the intrinsic collector current before it flows out through the collector contact (RC). Since RC is small (1 ohm) for an upshot device this connection was not critical.

XI. MEASUREMENTS OF AN UPSHOT TRANSISTOR

DC characterization of the upshot transistor was accom-current-voltage and saturation measurements at ambient temperature (25°). Current-voltage measurements were made in the upward and downward injection modes by utilizing the same procedure outlined earlier in Section VIII for the up-transistor. The results of these measurements are shown in Figures 27 and 28 for upward and downward injection, respectively. From these data, forward (upward) and reverse (downward) gain calculations were made and plotted in Figures 29 and 30. Since operation of the upshot device in the downward saturated mode is not applicable, saturation measurements were made only in the upward mode. Data for upward saturation was also taken using the same procedure described for the up-transistor. Figure 31 shows the upshot's upward saturation characteristics.

By comparing the upshot's dc electrical characteristics to the up-transistor's some interesting similarities and dissimilarities can be noted. Since the Schottky diode on the upshot is inactive when making upward current-voltage measurements, the two transistors exhibit similar characteristics. This is expected since their structures are almost identical, except for the diode. For downward injection, the current-voltage characteristics differ for I_B (terminal base current), and are the same for I_E (terminal emitter current). I_B is different

because now the Schottky diode is active, and the current through it is a function of V_{BC}. I_E's are similar because although the diode is active the emitter terminal current is governed by the intrinsic base current (current flowing into the transistor) which is unaffected by the presence of the diode. Because the current through the diode is orders of magnitude larger than the current flowing into the transistor, I_B is dominated by the diode. I_B versus V_{BC} for the upshot is then nothing more than the current-voltage characteristics of the upshot's diode. This is important in the next section when the composite model is simulated on the computer. The similarities and non-similarities in gain for both modes of injection are a direct result of the current-voltage characteristics. Except for the clamping effect of V_{CE} on the upshot transistor, the upward saturation characteristics are similar for the two transistors (Figures 18 and 31).

AC measurements on the upshot transistor could not be completed at this time since the necessary equipment needed for making good quality small-signal measurements was unavailable. For this same reason ac measurements on the SBD which were deferred until this time were also postponed to be completed at a future date.

XII. COMPUTER SIMULATIONS - UPSHOT TRANSISTOR

Computer simulations of the upshot transistor were made using the model shown in Figure 26 and the parameters as described in the previous sections. The dc accuracy of the model was tested by first simulating the upward and downward current-voltage characteristics at 25°C and comparing them to those of the device. From these simulations some discrepancies were found between the model and the device. For upward injection, the simulated terminal base (I_B) and substrate (I_S) currents were greater than their measured values for voltages of V_{BE} greater than 0.85 V. In downward injection, the simulated base current was greater than those of the device for all values of V_{BC}; although the slope of I_B at low voltages was correct. To compensate for these discrepancies, adjustments to the calculated critical parameters I_s, R_s, and RBI, described in Section X, were needed.

For upward injection, simulated values for I_B and I_S were found to differ from their measured values by the same amounts; despite the fact that I_C agreed. Since the substrate is active in this mode and I_C agreed with the data, the increase in I_B was determined to be the result of an increase in I_S. To decrease the amount of current shunted through the substrate, RBI (intrinsic base resistance of PNP1) was increased. By using a reiterative procedure to best fit I_B and I_S to the data, a final

value for RBI of 30 Kohms was ascertained. The final simulated results for current versus voltage in the upward mode are shown in Figure 27 along with measured data.

To improve the model's simulation in the downward mode, I_s (saturation current) and R_s (series resistance) of the Schottky diode had to be adjusted. Since the diode is on in the downward mode, the transistor's terminal base current (I_B) is controlled by the diode, for reasons given in Section XI. At low values of V_{BC}, I_B is determined by diode parameters n and I_s. Because the slope of the simulated terminal base current was correct, only I_s had to be changed. To lower I_B, I_s was decreased until a best fit value of 1.225E-13 Amps was obtained. The discrepancy between calculated and actual I_s can easily be accounted for by variations in the diode's area. For values of V_{BC} greater than 0.6 V, I_B is governed by R_s. To fit I_B in this region, R_s was increased causing the slope of I_B to decrease. For the data measured a best fit value of 2000 ohms was determined. The final simulated results for downward injection are shown in Figure 28.

Gain calculations for both modes were made from the final simulated current characteristics and plotted in Figures 29 and 30. From Figures 27 through 30 ,it can be noted that the model agrees very well with the actual device. Finally, simulations were made of the model in the upward saturation mode at 25°C.

The results are shown in Figure 31. Here too the model is in good agreement with the data.

XIII. CONCLUSION

A model for an oxide isolated Schottky clamped, up-transistor (upshot) has been presented. It was obtained by merging together models developed separately for an oxide isolated Schottky diode and an oxide isolated up-transistor. Charge-control models for the diode and the transistor were developed from a consideration of the equations governing their operation. Parameters used in the models were obtained from measurements made on actual devices. In the case of the Schottky diode, model parameters were extracted directly from the measured data. Because of the complexity of the up-transistor's structure, its parameters were extracted using a computer algorithm called PAREX.[11] The model and corresponding parameter values for each device were then tested by simulating the electrical measurements and comparing the results with the measured data. Models developed for the Schottky diode and the up-transistor were shown to be accurate in their dc response. Good ac data for the diode could not be obtained because of the diode's inherently fast switching response. AC characterization of the up-transistor was achieved by comparing measured and simulated values for storage time. The agreement was quite good.

A composite model for the upshot transistor was developed by combining the two individual models after modifying the

critical parameters I_s (saturation current of the diode), R_s (series resistance of the diode), and RBI (intrinsic base resistance of PNP1). Because of structural and dimensional differences between the upshot and the discrete devices, new values for the critical parameters were calculated based on geometrical estimates. The remainder of the upshot's parameters were identical to the individual models. The model was tested by simulating dc electrical measurements made on a fabricated upshot device. Due to discrepancies between measured and simulated data, adjustments to the calculated cricital parameters were necessary. Final values for I_s, R_s and RBI were determined by fitting the model's simulated output to the measured data. In all cases, the changes made to these parameters could be attributed to variations in dimension and structure. For final values of RBI = 30 Kohms, I_s = 1.36E-13 Amps, R_s = 2000 ohms, and the remaining parameters as listed in Tables I and II, the composite model developed for the upshot transistor worked very well in simulating the actual device's dc response. AC characterization of the upshot transistor was deferred to a later time when the necessary equipment needed for making good ac measurements would be available.

TABLE I

EXTRACTED PARAMETERS
FOR AN OXIDE ISOLATED
SCHOTTKY BARRIER DIODE

Parameter	Value	Units
I_s	2.973E-12	AMPS
n	1.0627	-
R_s	42	OHMS
V_{bi}	0.7	VOLTS
m_d	0.3354	-
CJO	6.644E-16	FARADS/μm^2
τ_D*	0.138E-9	SECONDS
A_d	24.5	μm^2

*Parameter was calculated

TABLE II

EXTRACTED PARAMETERS FOR THE COMPOSITE MODEL OF AN OXIDE ISOLATED UP-TRANSISTOR

A. DC MODEL PARAMETERS

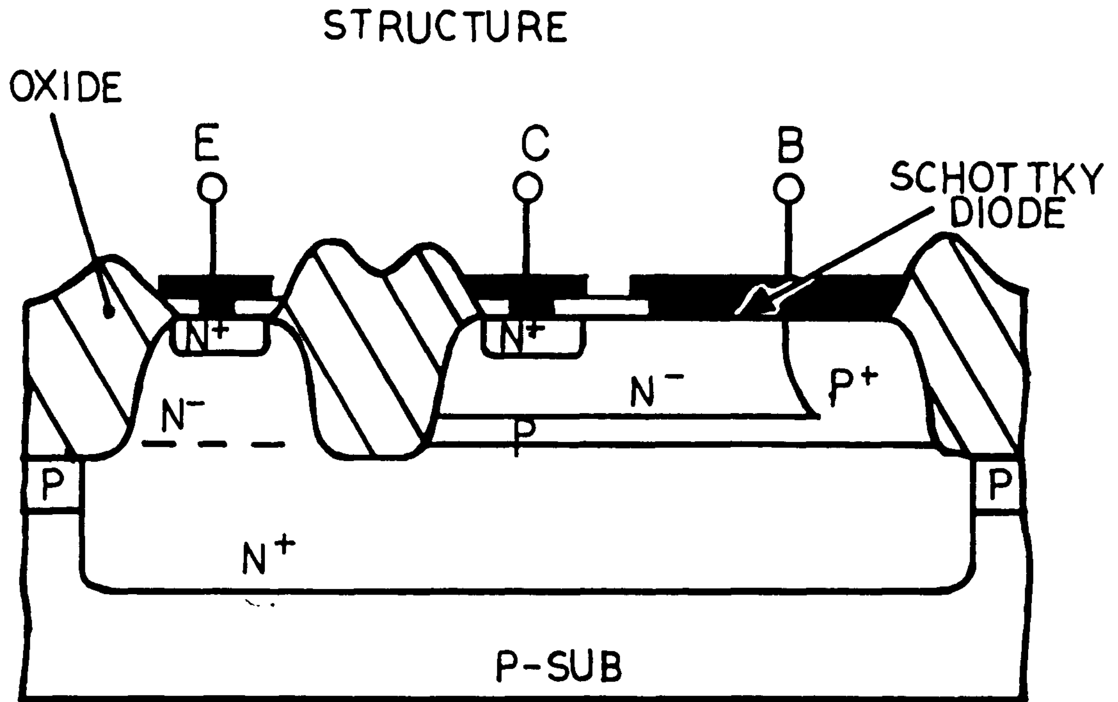
	PARAMETER	VALUE	UNITS
NPN:	RBI	15.58E+3	OHMS
	RE	95	OHMS
	RC	1	OHM
	I_s	1.1308E-16	AMPS
	I_1	7.826E-20	AMPS
	I_2	1.988E-17	AMPS
	n_E	1.327	-
	I_3	1.802E-19	AMPS
	I_4	5.583E-16	AMPS
	n_C	1.565	-
	V_{AO}	1.725E+1	VOLTS
	V_{BO}	5.787	VOLTS
	I_{KF}	1.099E-12	AMPS
	I_{KR}	4.649E-4	AMPS
PNP1:	I_s	4.41E-19	AMPS
	RBI	9.98E+3	OHMS
	I_1	7.815E-20	AMPS
	I_2	1.98E-17	AMPS
	I_{KF}	5.98E-5	AMPS
PNP2:	I_s	1.56E-19	AMPS
	I_1	7.826E-20	AMPS

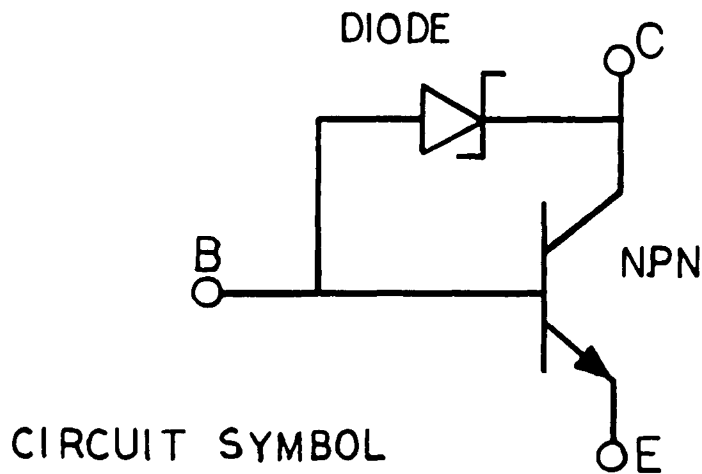
TABLE II (CONT'D.)

	PARAMETER	VALUE	UNITS
PNP2:	I_2	1.98E-17	AMPS

B. AC MODEL PARAMETERS

	PARAMETER	VALUE	UNITS
NPN:	PE	0.75	VOLTS
	m_e	0.3682	-
	CJE	6.898E-16	FARADS/μm^2
	PC	0.7	VOLTS
	m_c	0.3449	-
	CJC	1.615E-16	FARADS/μm^2
	τ_{FO}	590E-12	SECONDS
	τ_{RO}	529E-12	SECONDS
	C_{es}	2.618×10^{-16}	FARADS/μm^2

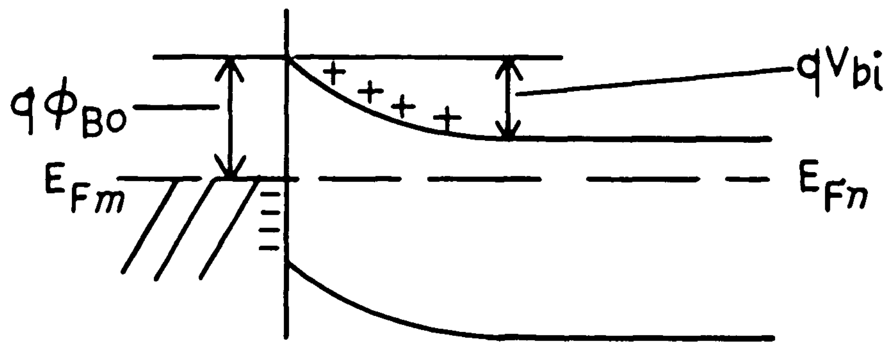




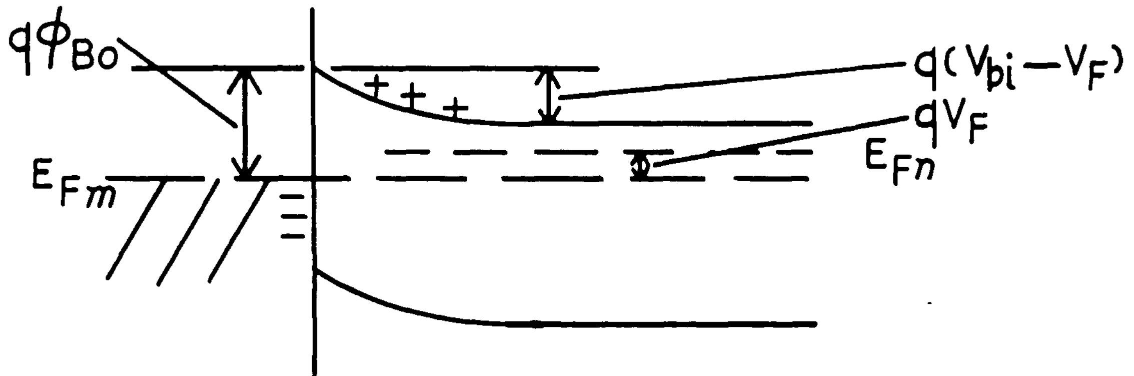
STRUCTURE AND SYMBOL OF AN OXIDE ISOLATED SCHOTTKY CLAMPED UP-TRANSISTOR (UPSHOT)

FIGURE 1

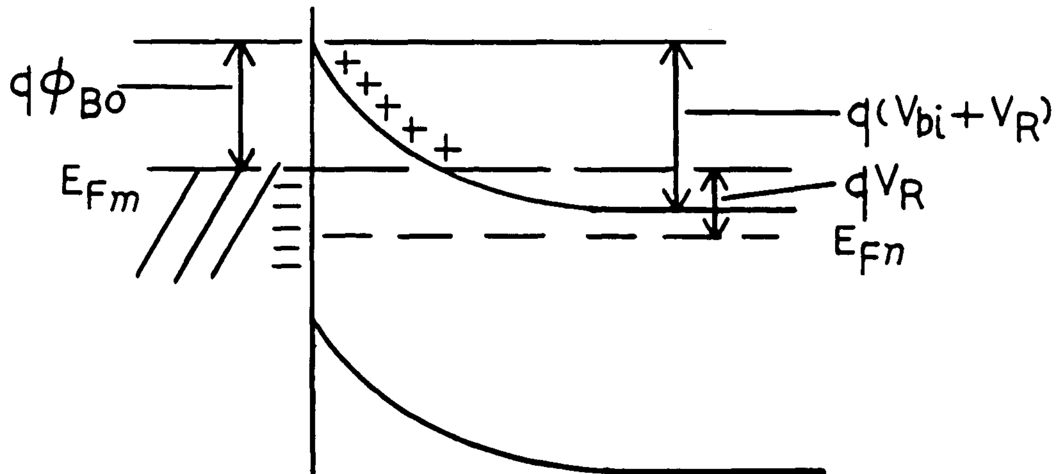
a) EQUILIBRIUM



b) FORWARD BIAS



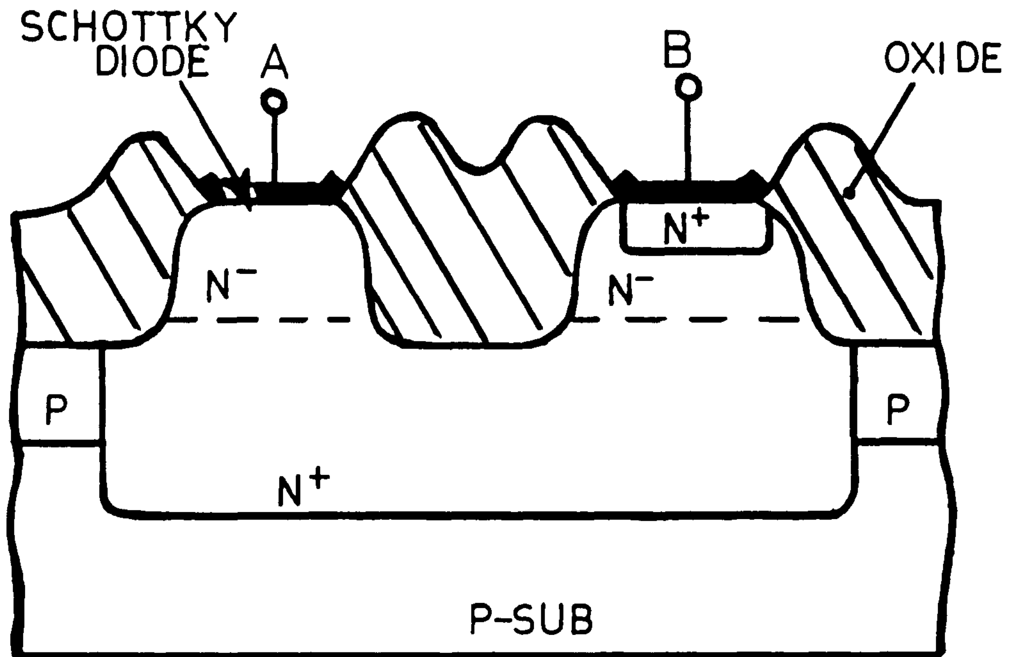
c) REVERSE BIAS



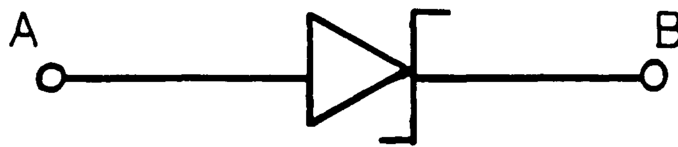
ENERGY BAND DIAGRAMS FOR A SBD UNDER DIFFERENT BIAS CONDITIONS

FIGURE 2

STRUCTURE

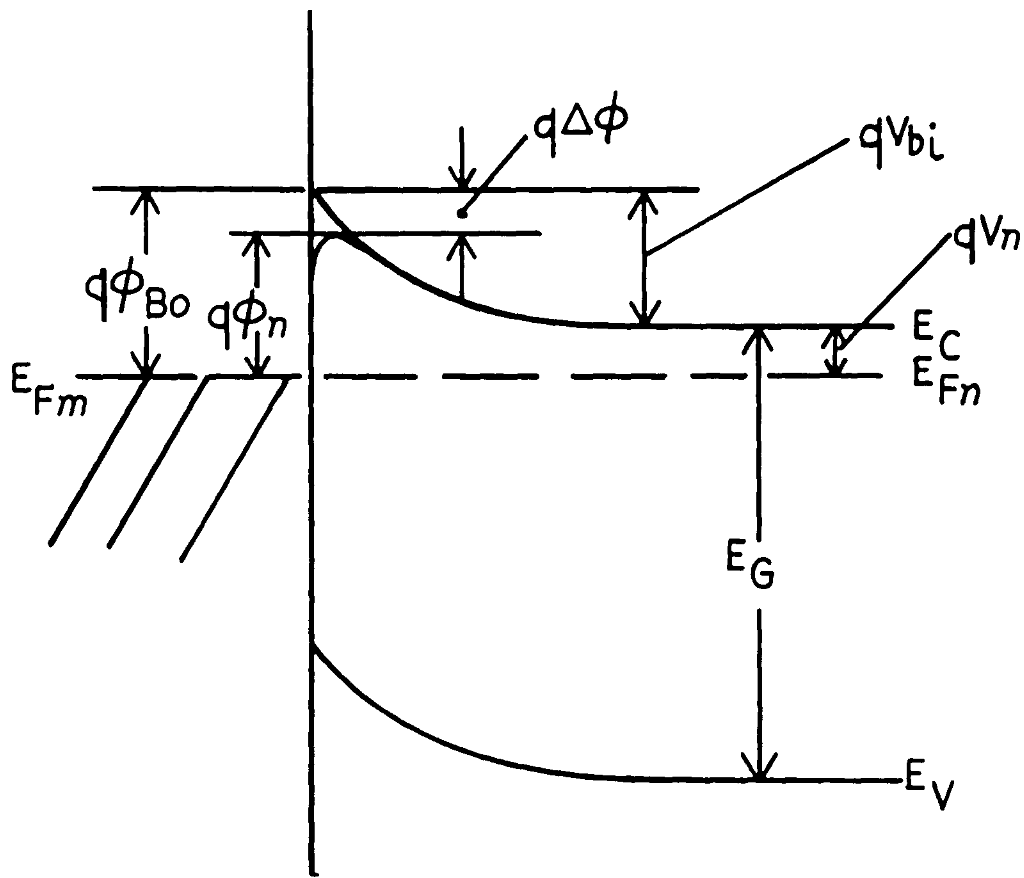


SYMBOL



STRUCTURE AND SYMBOL
OF AN OXIDE ISOLATED
SCHOTTKY BARRIER DIODE

FIGURE 3

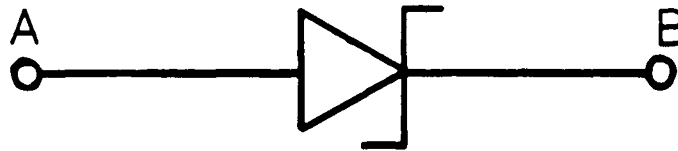


EQUILIBRIUM

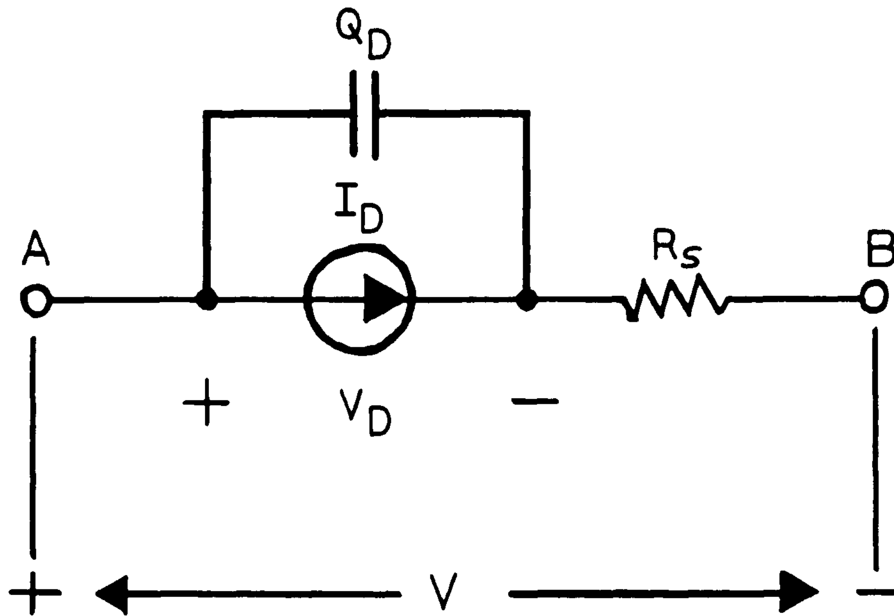
DETAILED ENERGY BAND DIAGRAM
OF A SCHOTTKY DIODE

FIGURE 4

SYMBOL

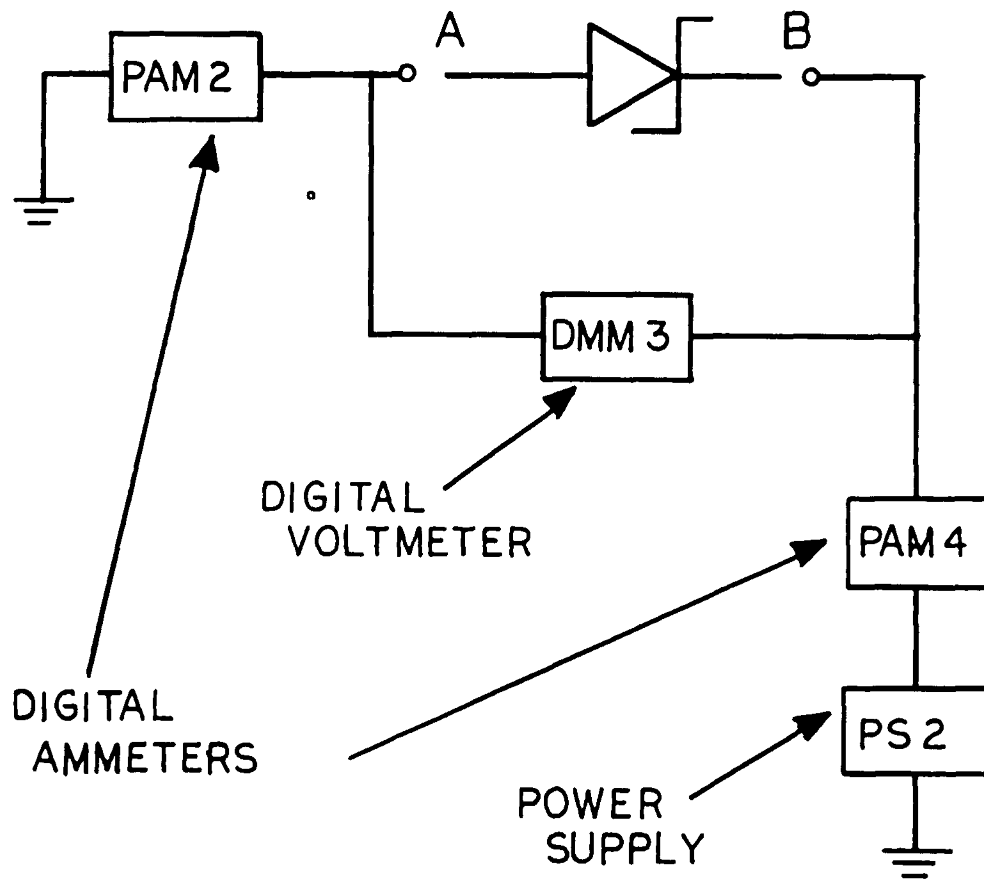


MODEL

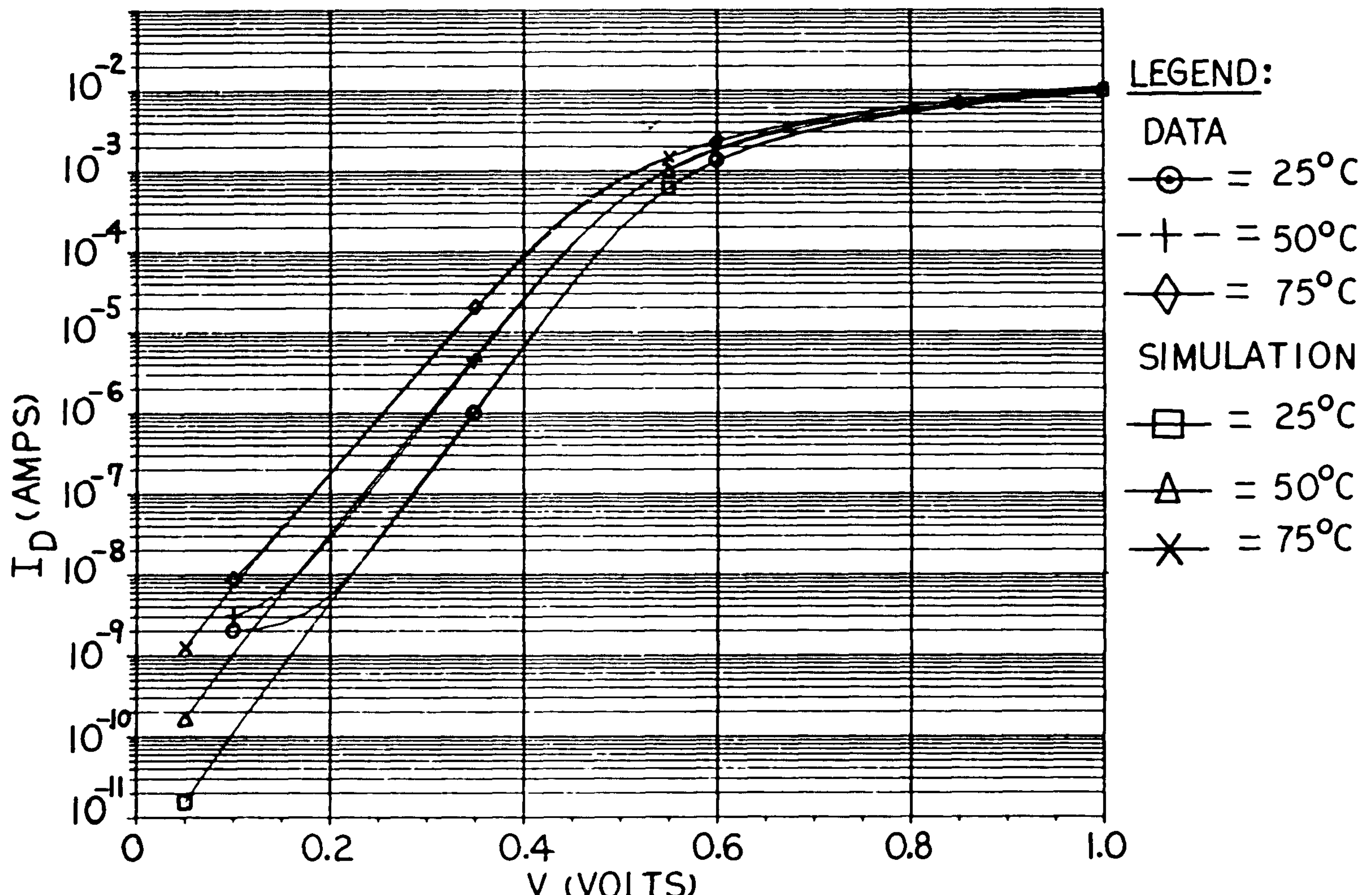


MODEL AND SYMBOL
OF AN OXIDE ISOLATED
SCHOTTKY BARRIER DIODE

FIGURE 5

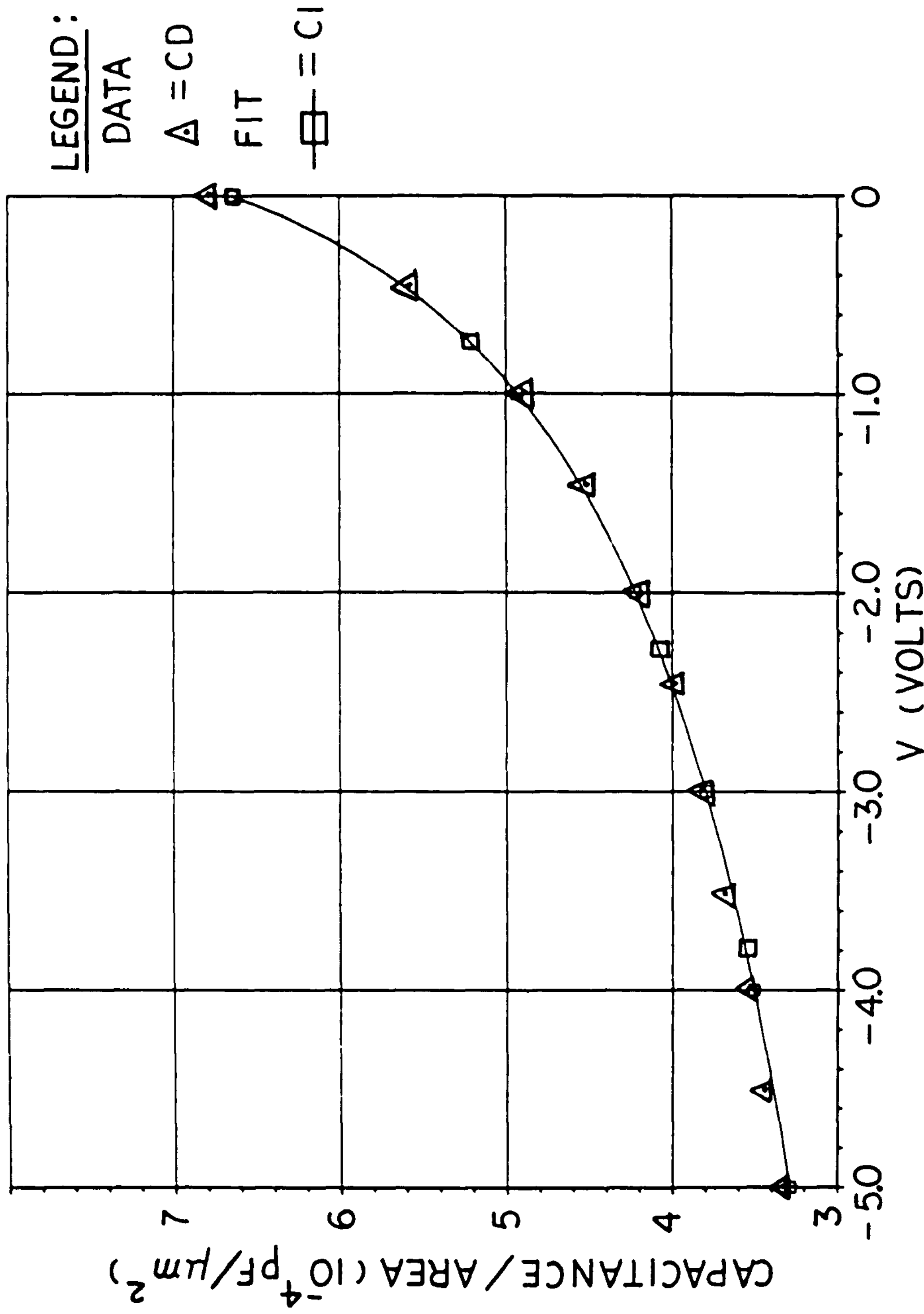


TEST CIRCUIT USED FOR
I-V MEASUREMENTS OF
A SCHOTTKY DIODE
FIGURE 6



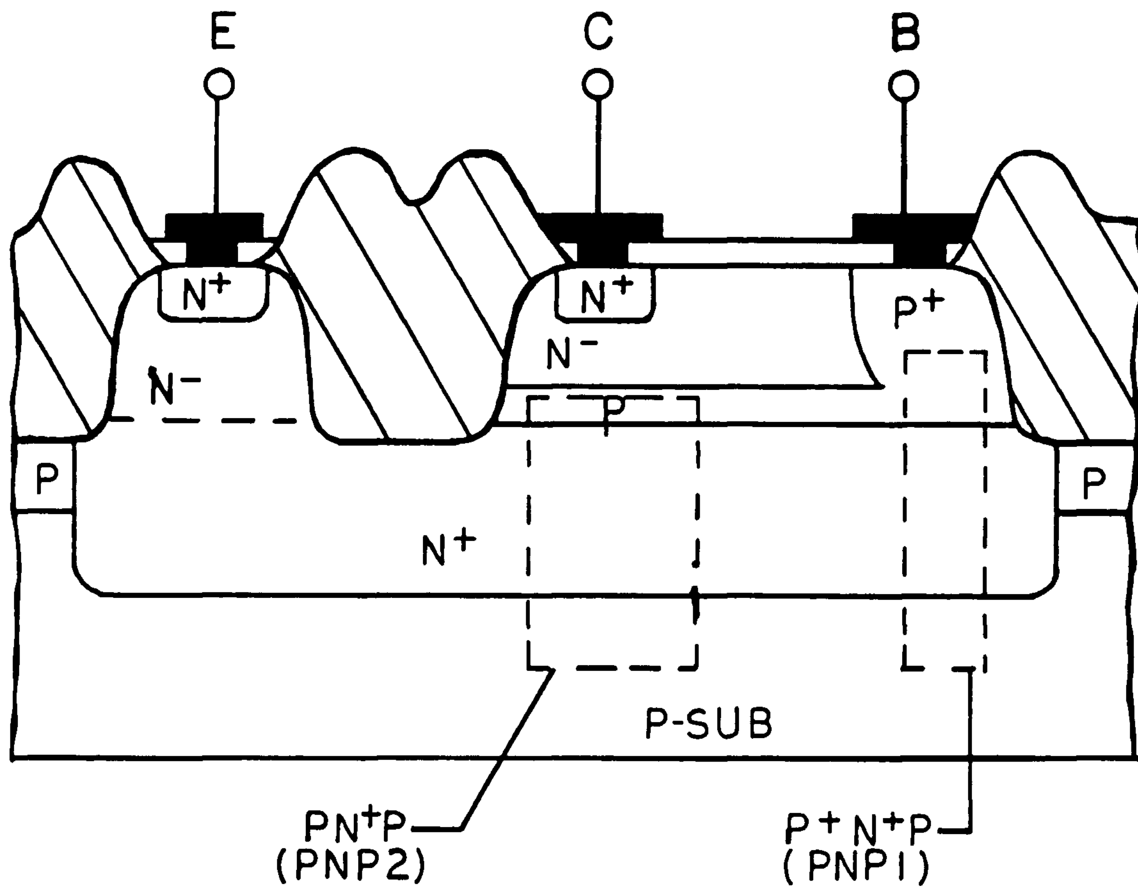
SCHOTTKY BARRIER DIODE — I-V CHARACTERISTICS

FIGURE 7



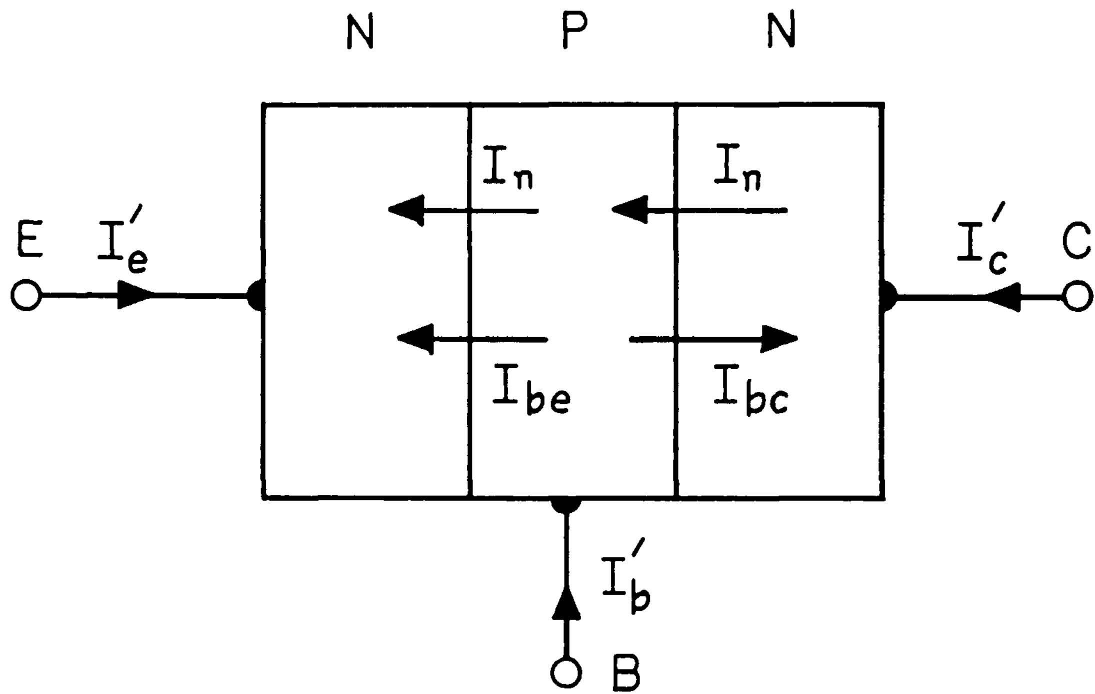
SCHOTTKY BARRIER DIODE — JUNCTION CAPACITANCE

FIGURE 8



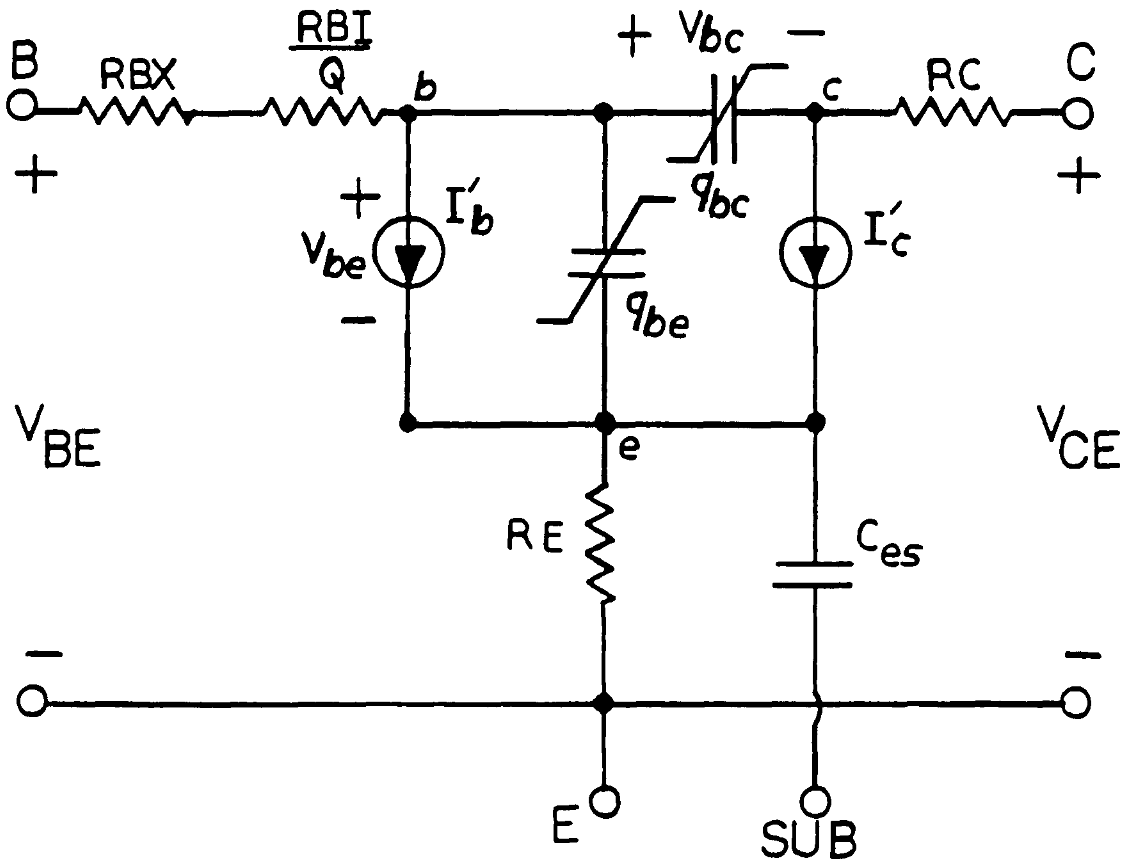
STRUCTURE OF AN OXIDE ISOLATED UP (NPN) TRANSISTOR

FIGURE 9



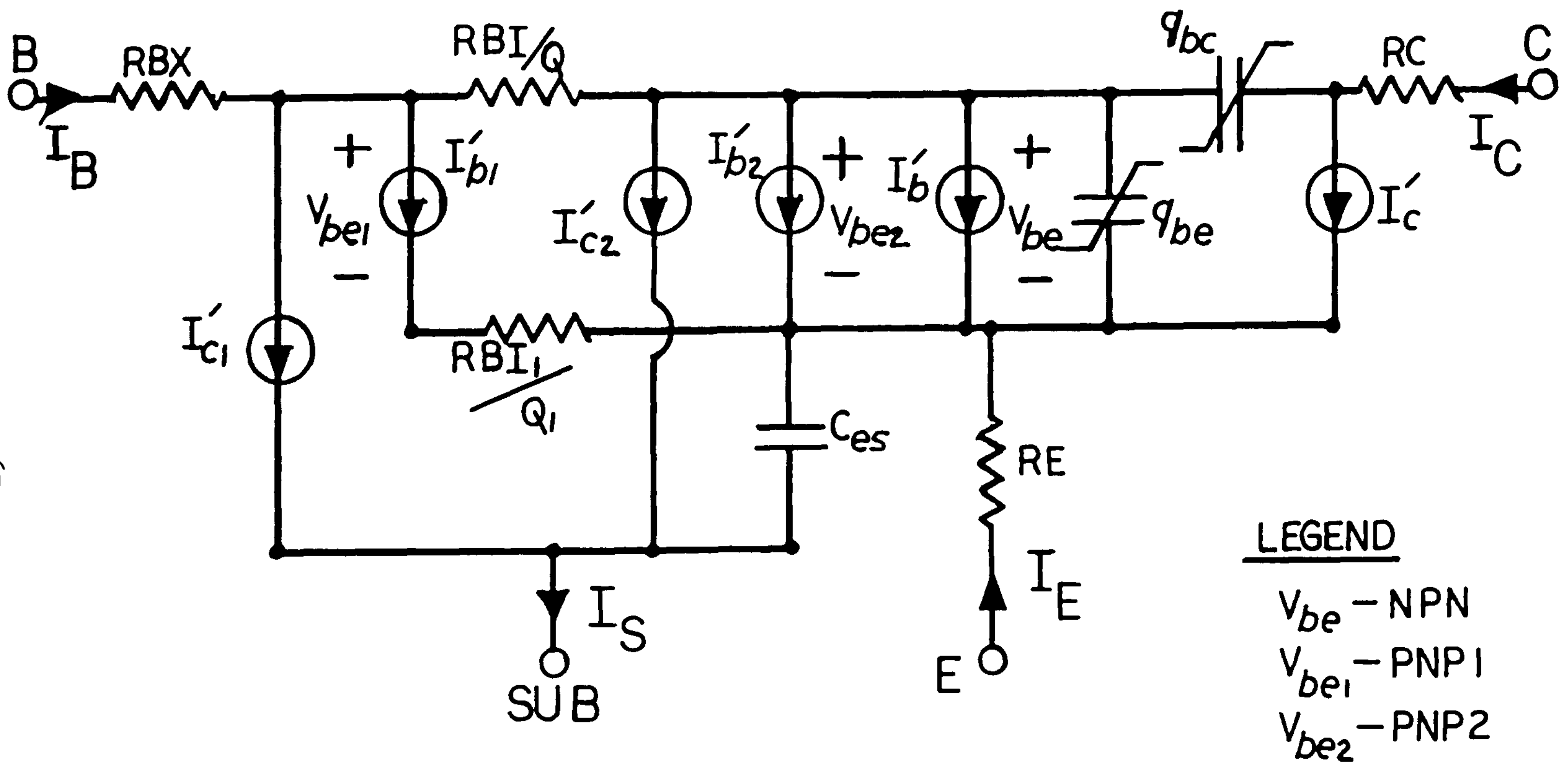
INTRINSIC JUNCTION CURRENTS FOR AN NPN TRANSISTOR

FIGURE 10



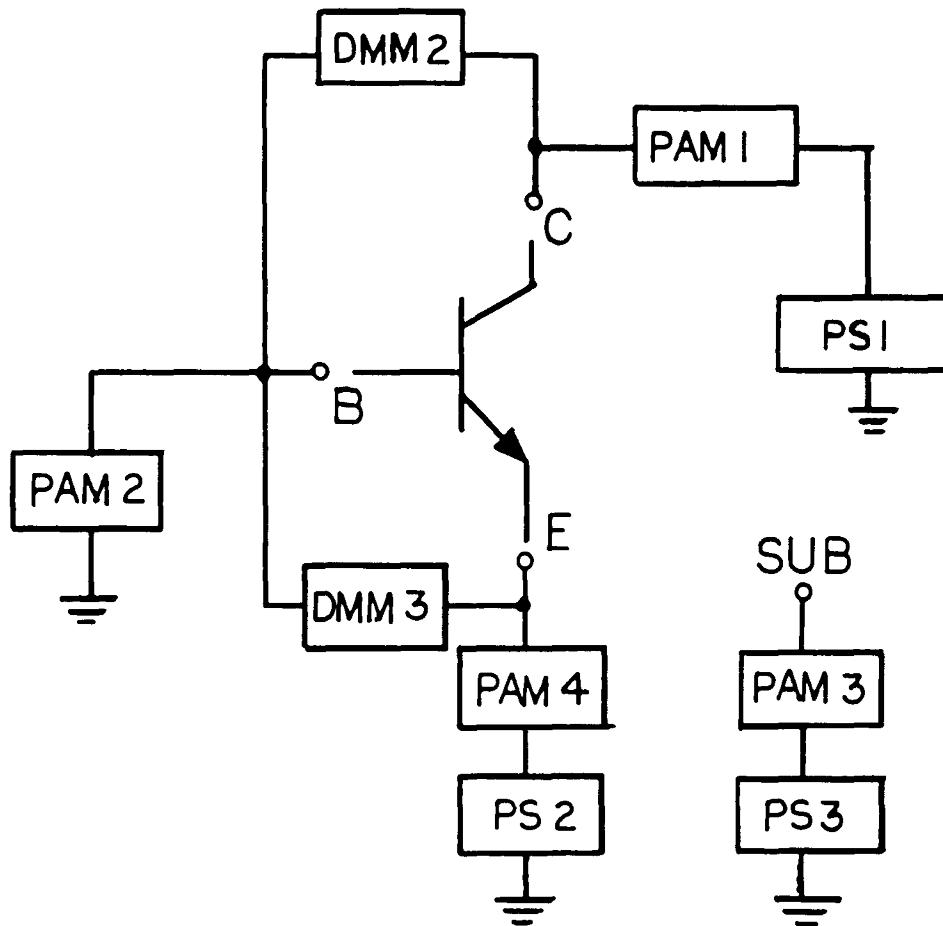
CIRCUIT MODEL OF AN
NPN UP-TRANSISTOR

FIGURE 11



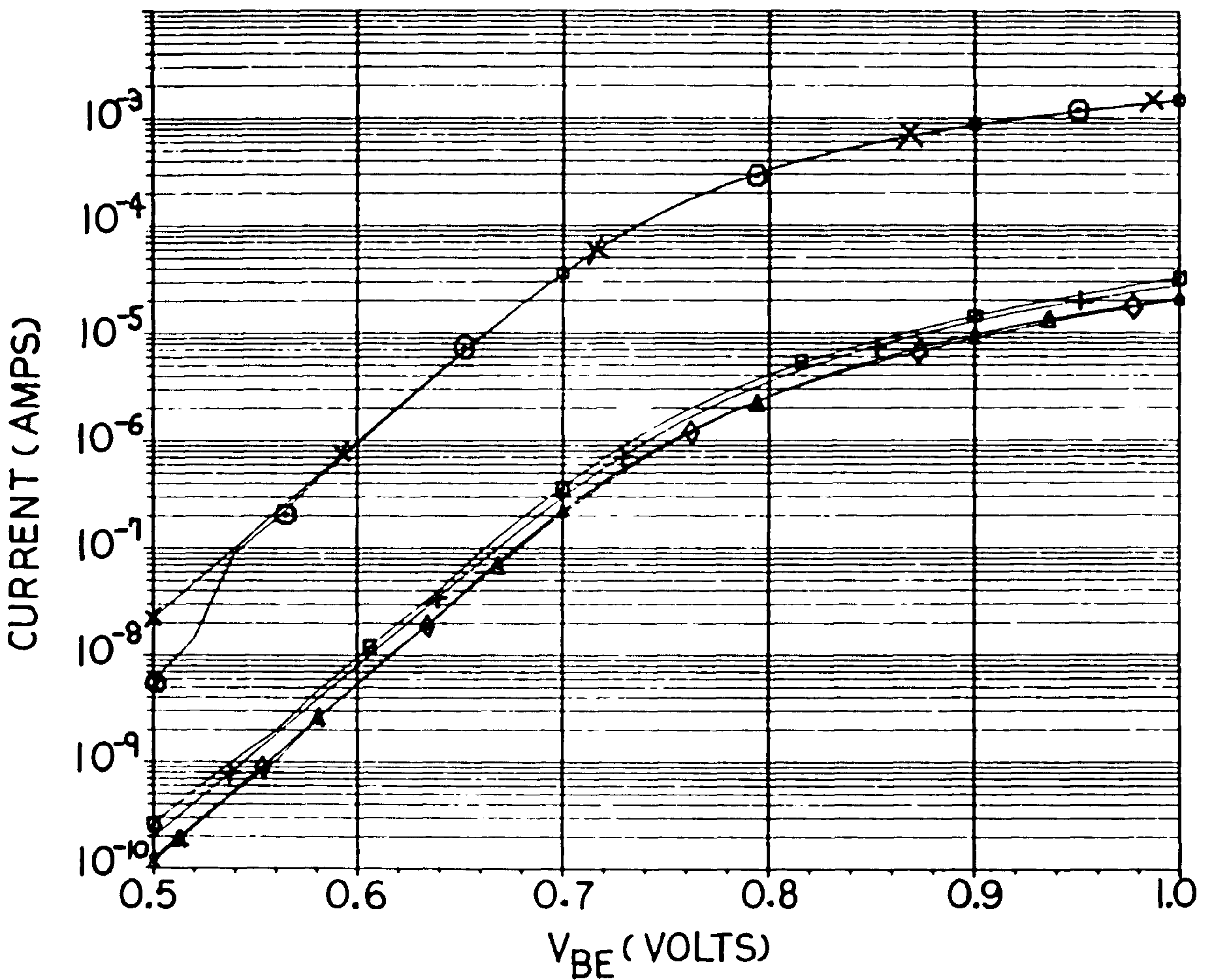
COMPOSITE CIRCUIT MODEL OF AN OXIDE ISOLATED UP-TRANSISTOR

FIGURE 12



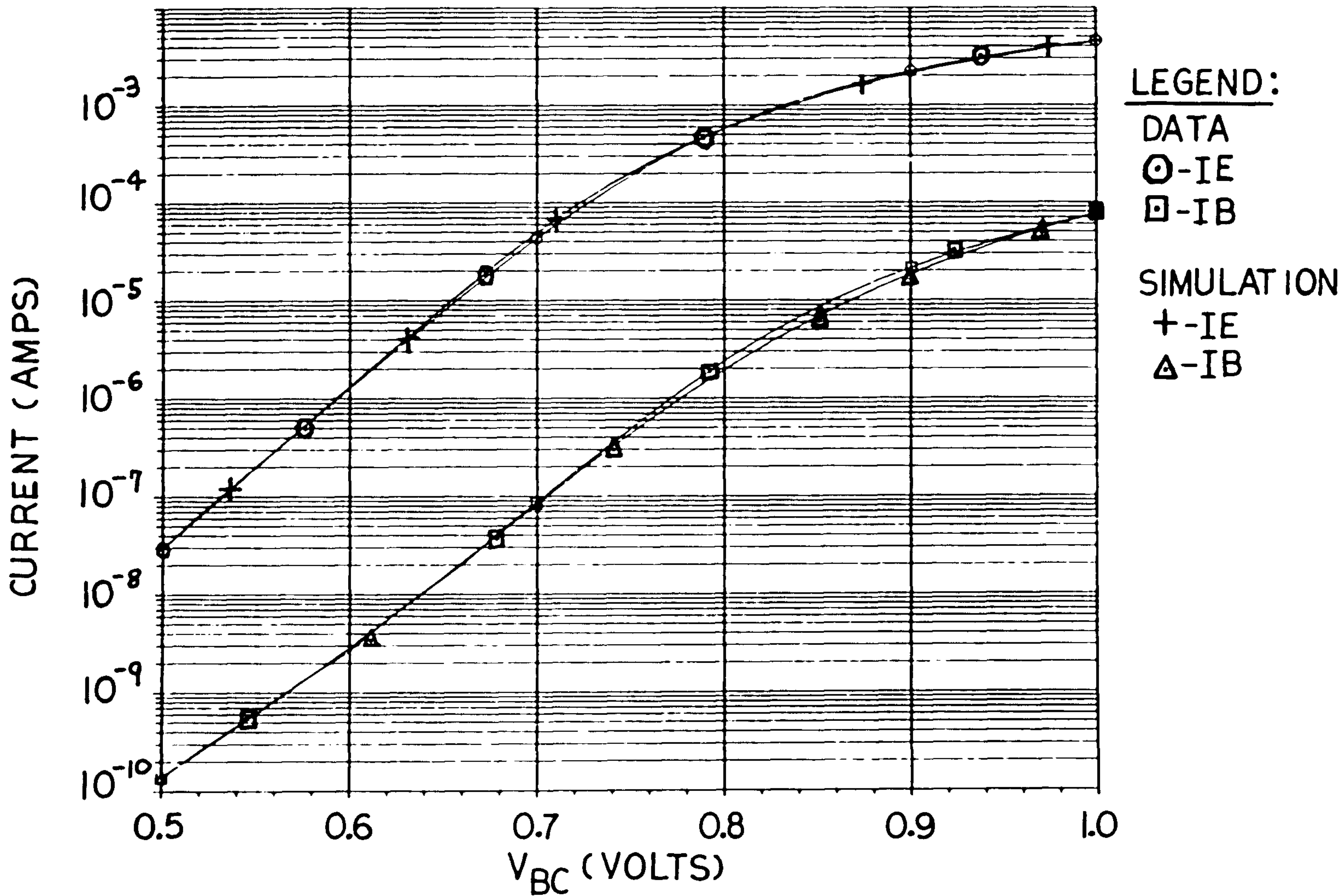
TEST CIRCUIT FOR
CURRENT-VOLTAGE AND SATURATION
MEASUREMENTS

FIGURE 13



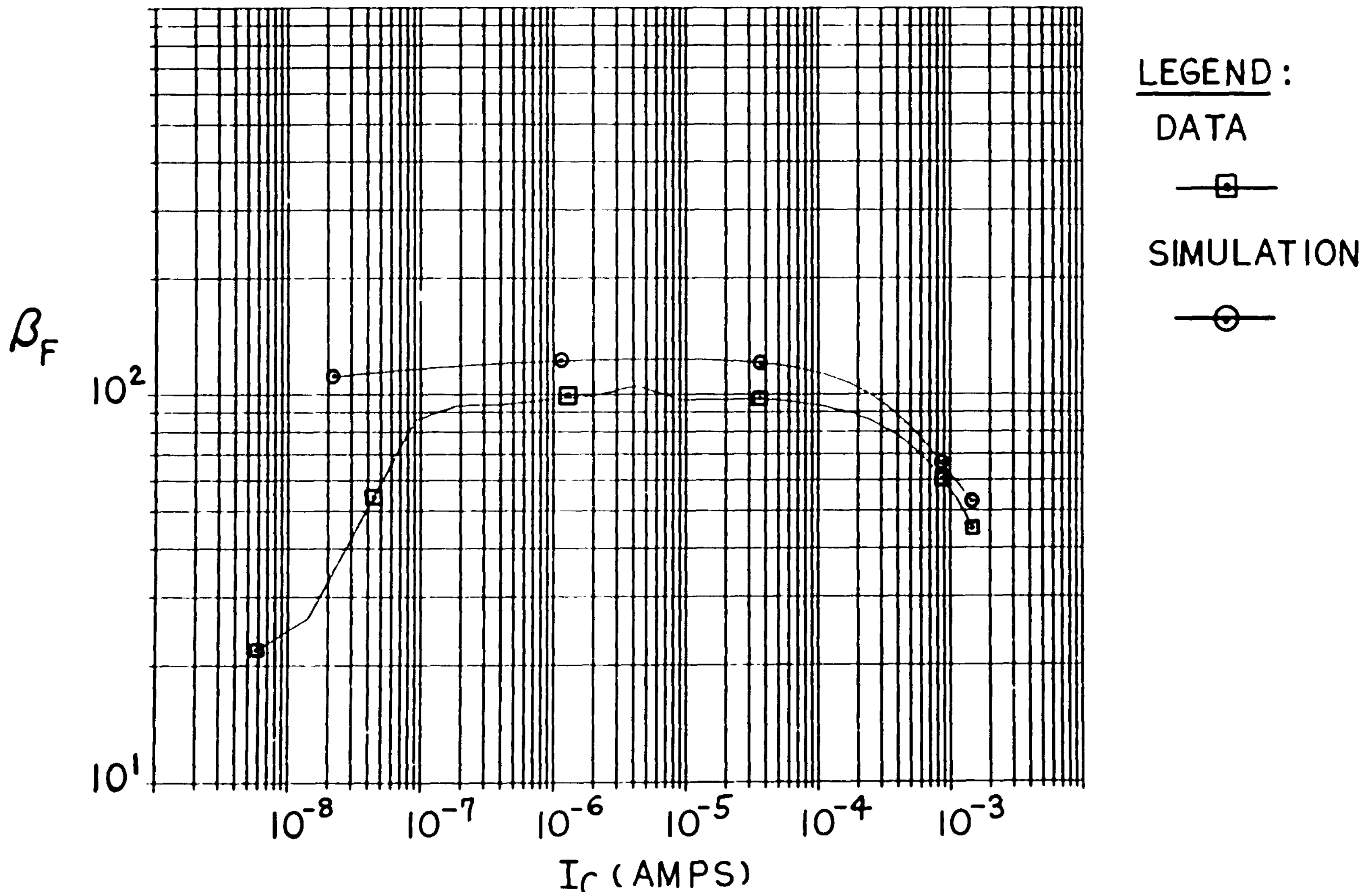
UP-TRANSISTOR I-V CHARACTERISTICS—UPWARD INJECTION

FIGURE 14



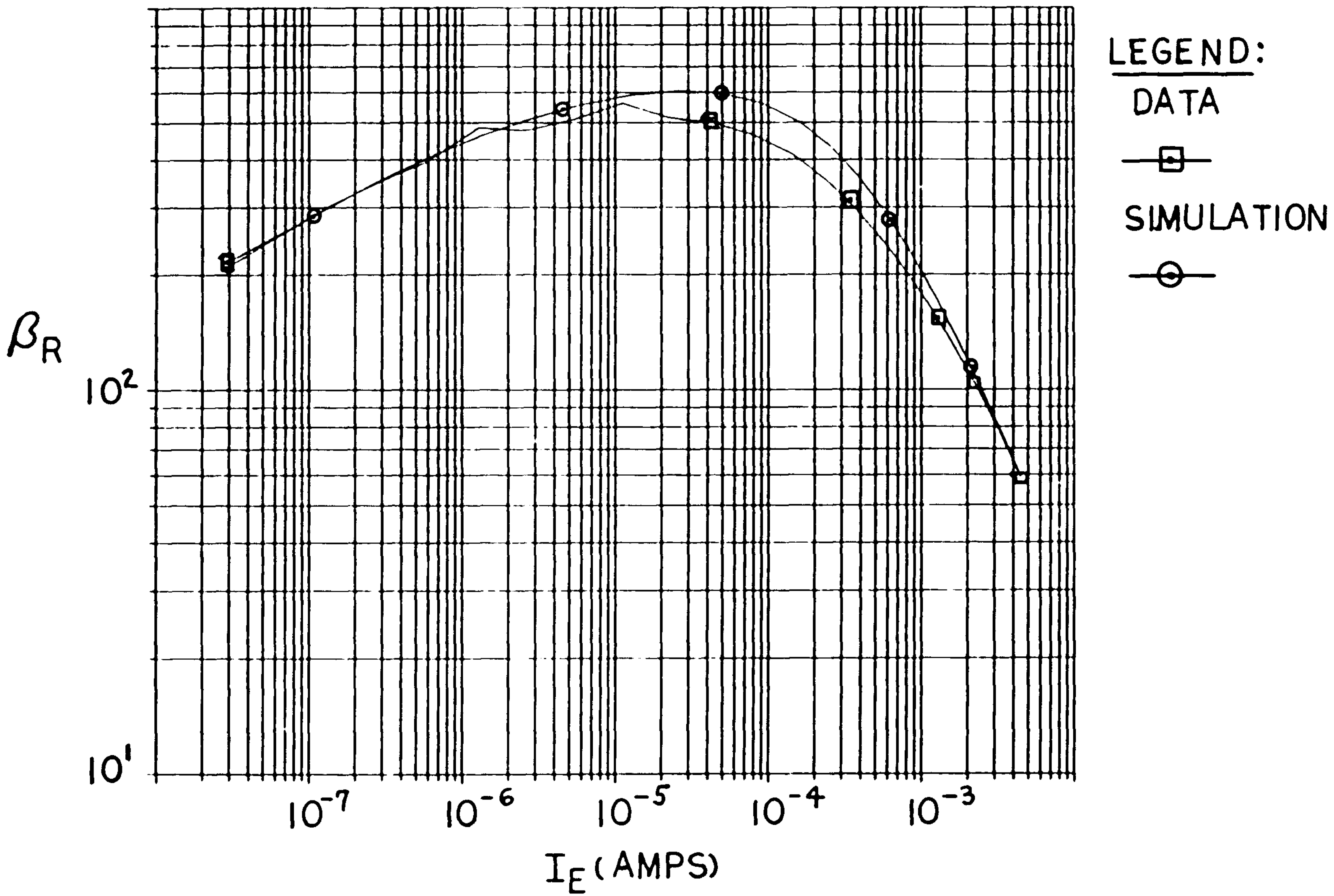
UP-TRANSISTOR I-V CHARACTERISTICS—DOWNWARD INJECTION

FIGURE 15

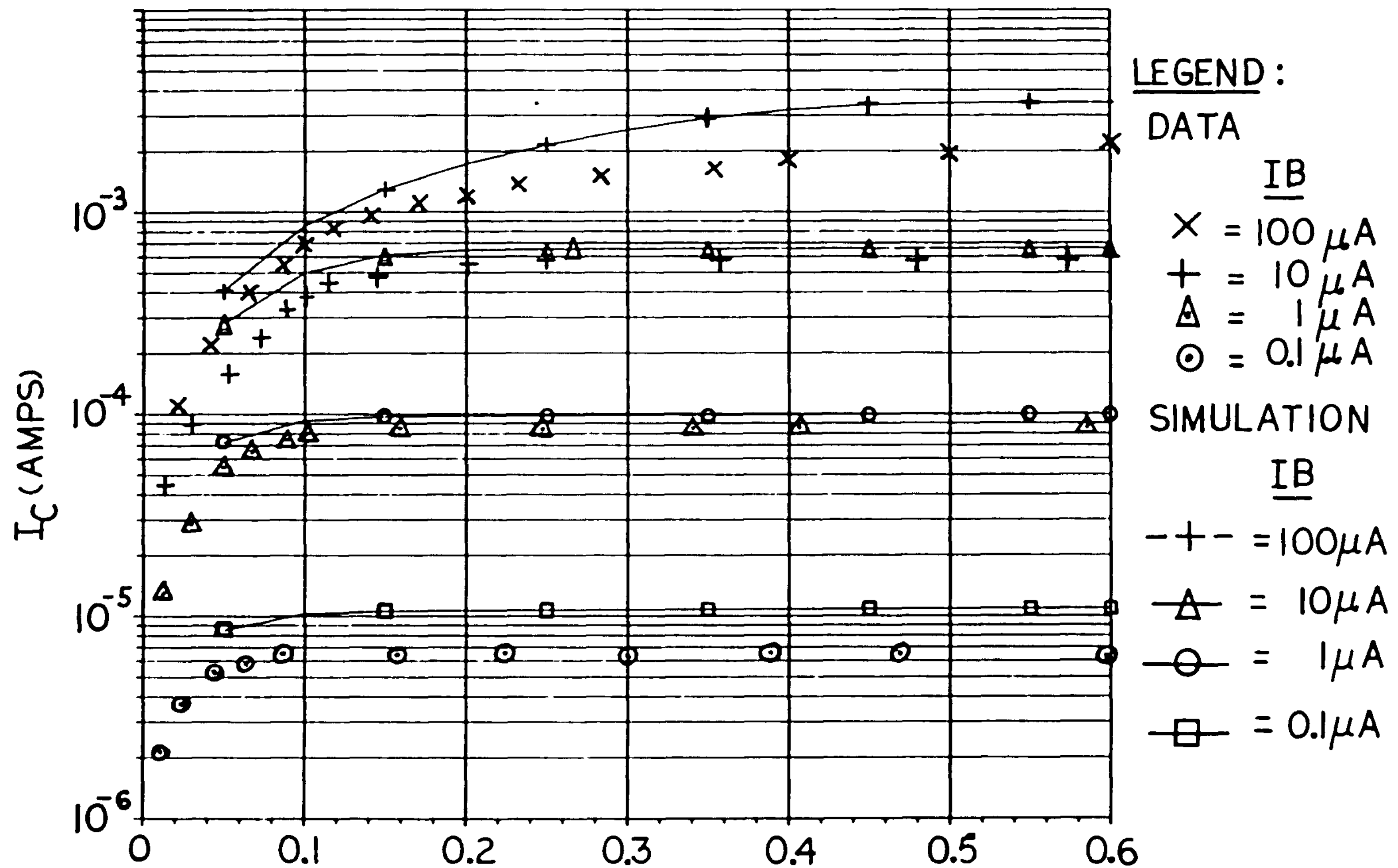


UP-TRANSISTOR—GAIN—UPWARD INJECTION

FIGURE 16

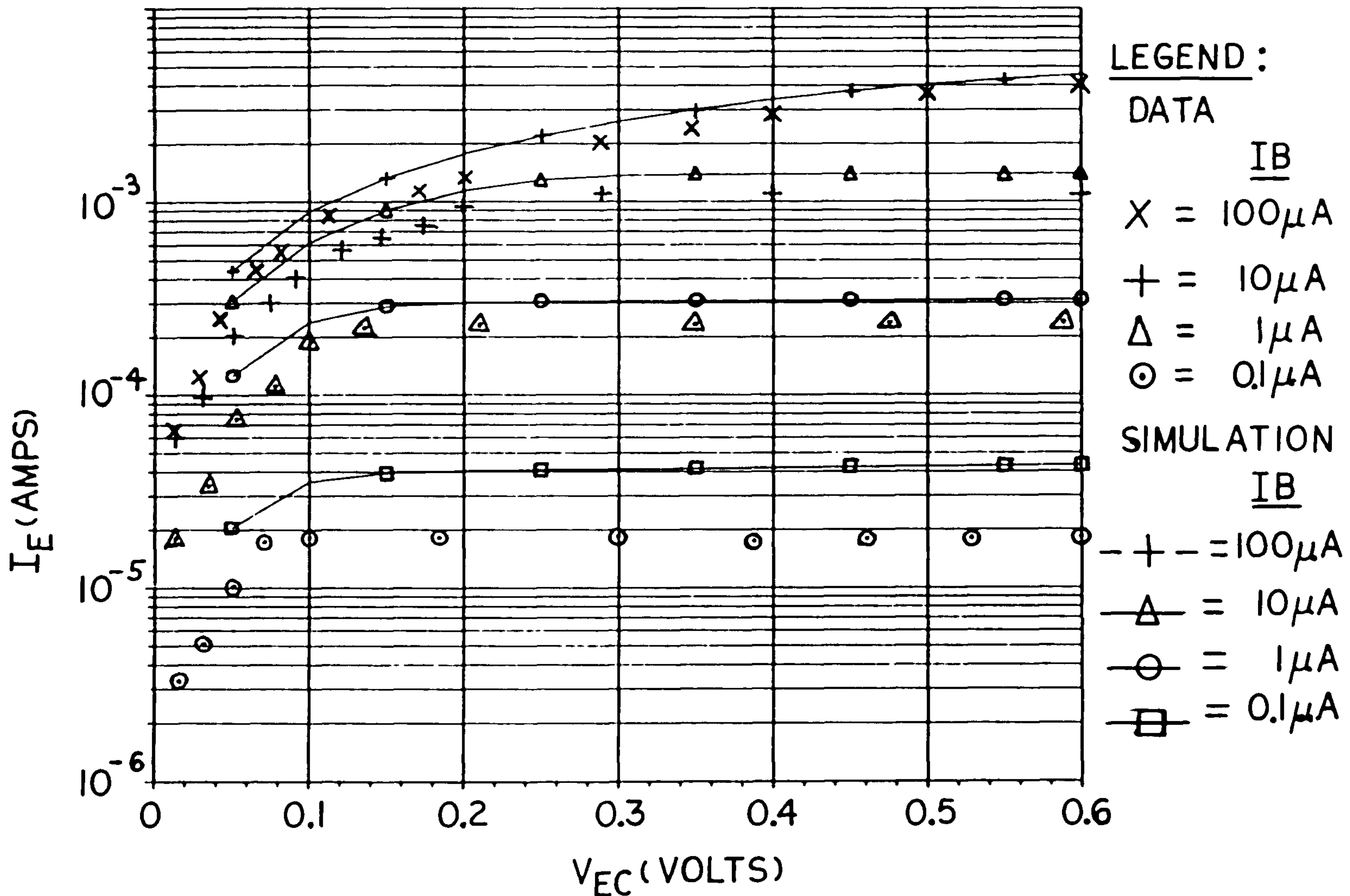


UP-TRANSISTOR — GAIN—DOWNWARD INJECTION
FIGURE 17



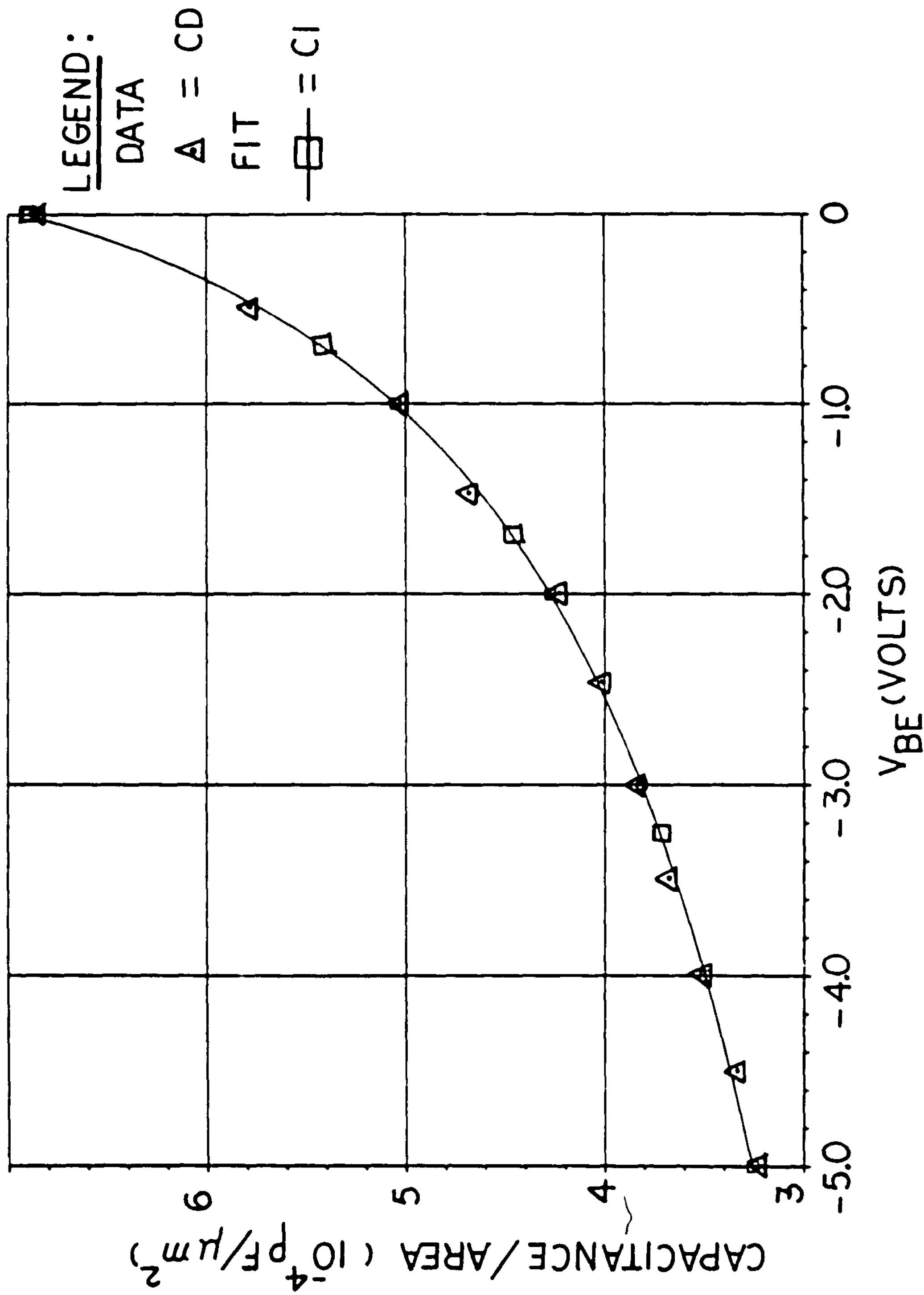
UP-TRANSISTOR — SATURATION CURVES—UPWARD INJECTION

FIGURE 18

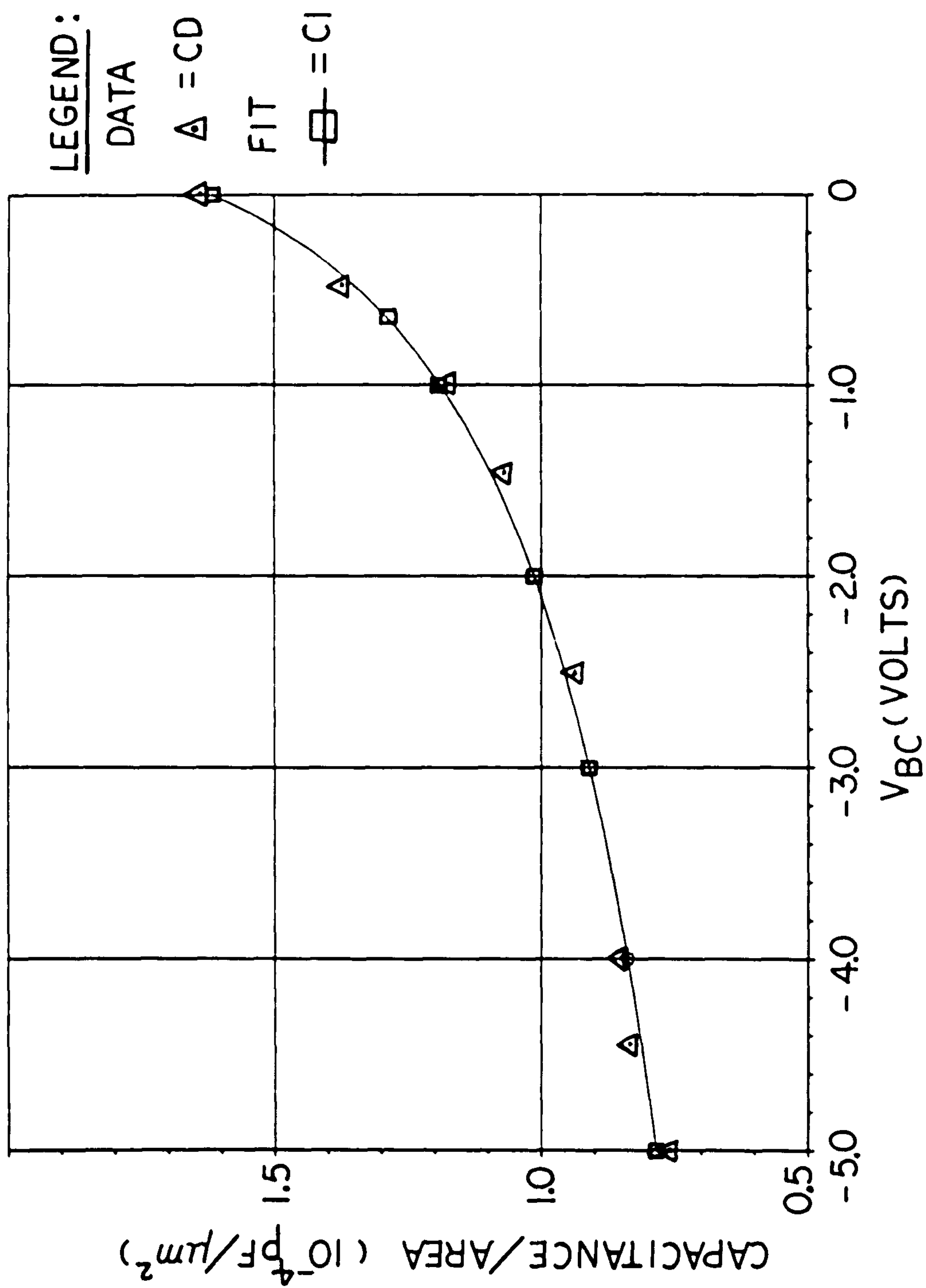


UP-TRANSISTOR — SATURATION CURVES — DOWNWARD INJECTION

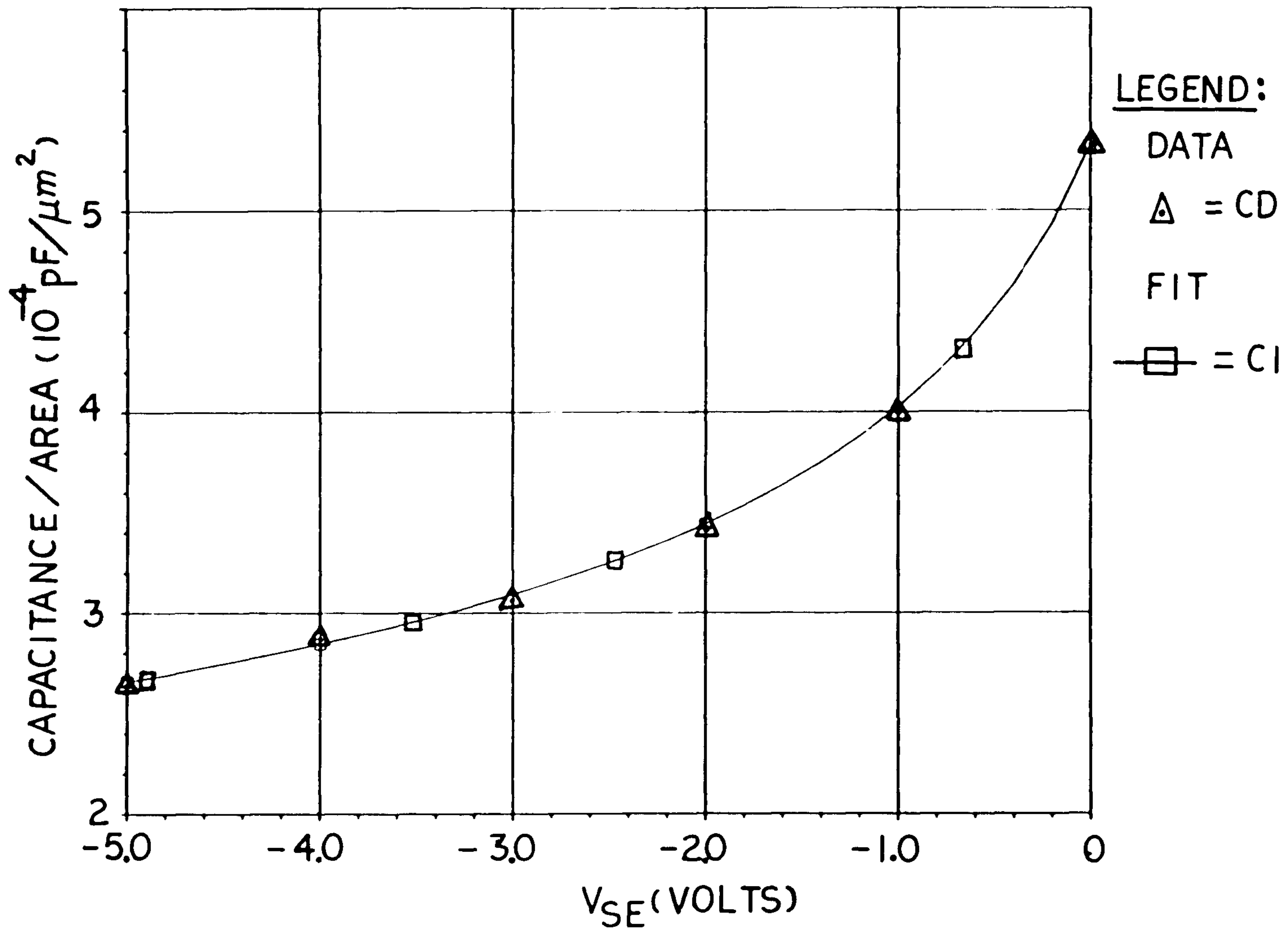
FIGURE 19



UP-TRANSISTOR — BASE-EMITTER JUNCTION CAPACITANCE
FIGURE 20

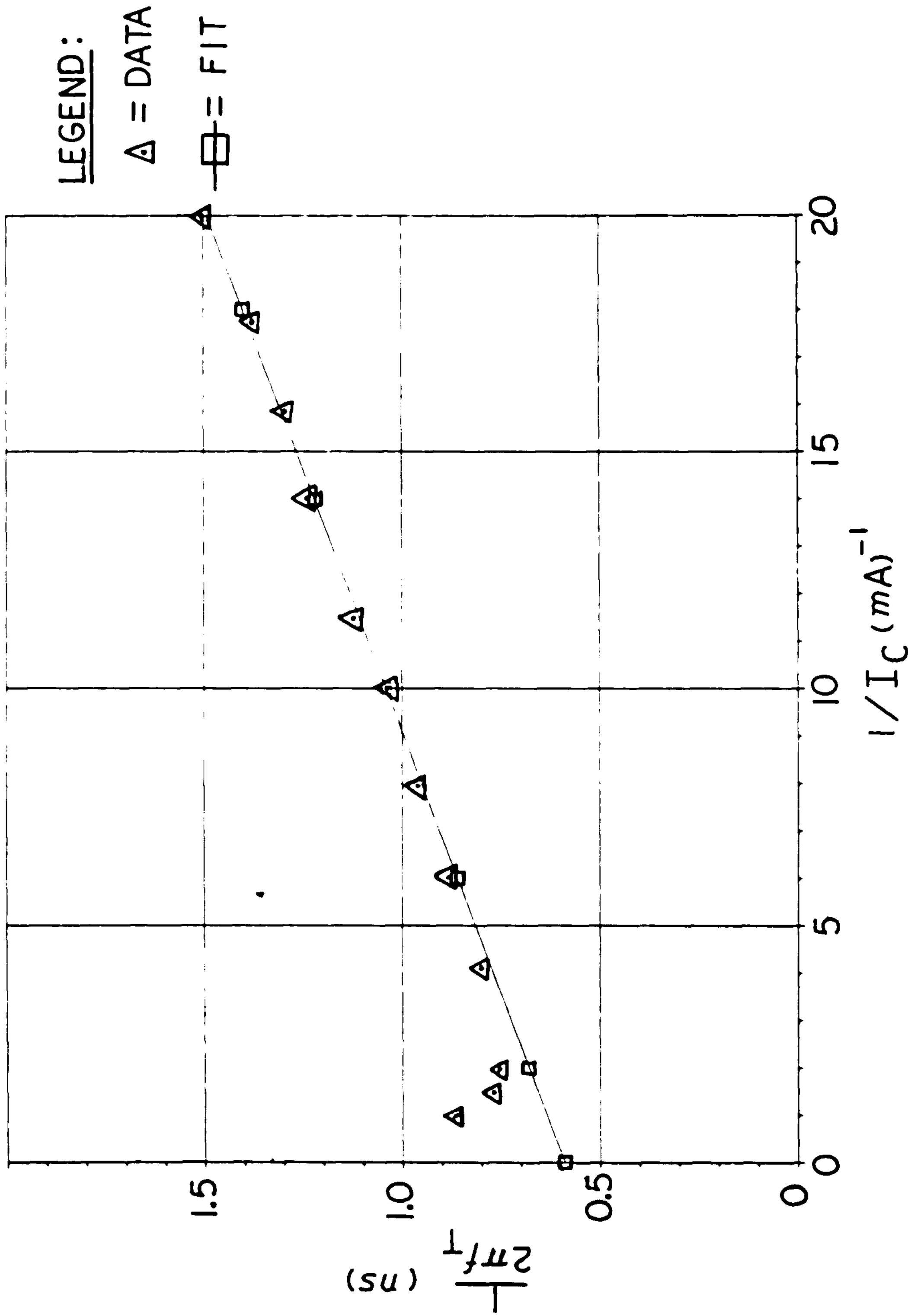


UP-TRANSISTOR—BASE-COLLECTOR JUNCTION CAPACITANCE
FIGURE 21



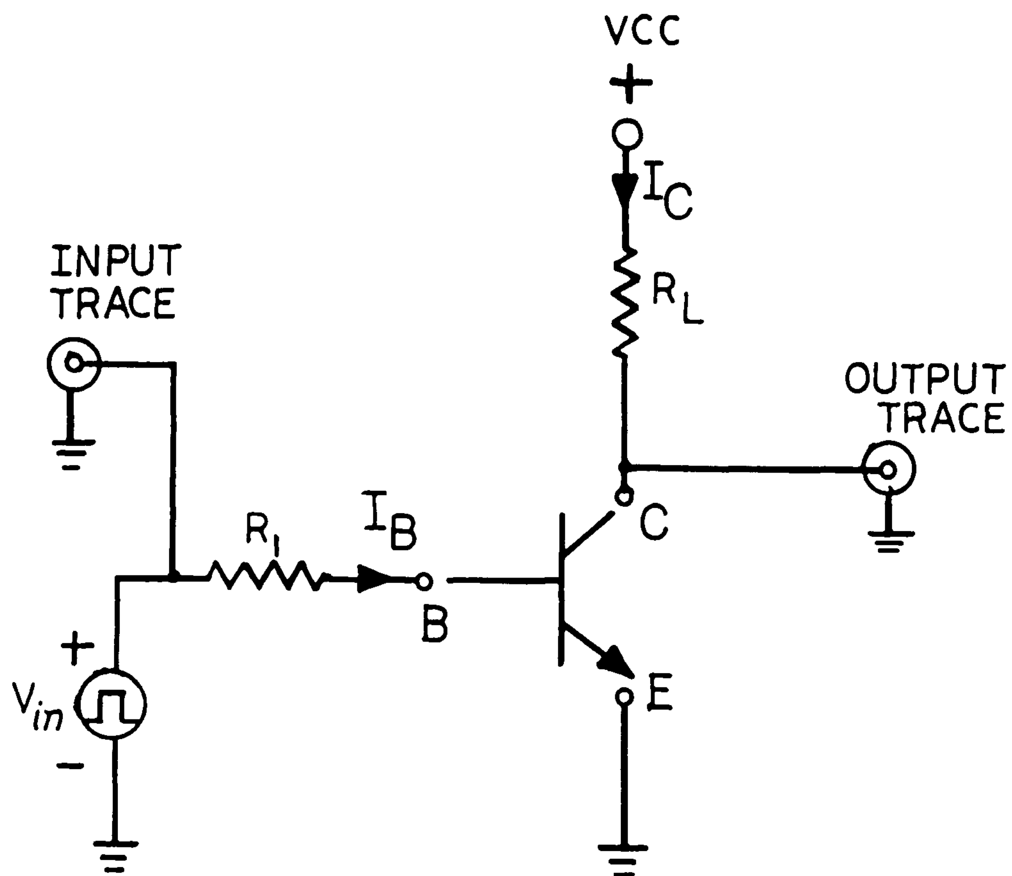
UP-TRANSISTOR — EMITTER-SUBSTRATE JUNCTION CAPACITANCE

FIGURE 22



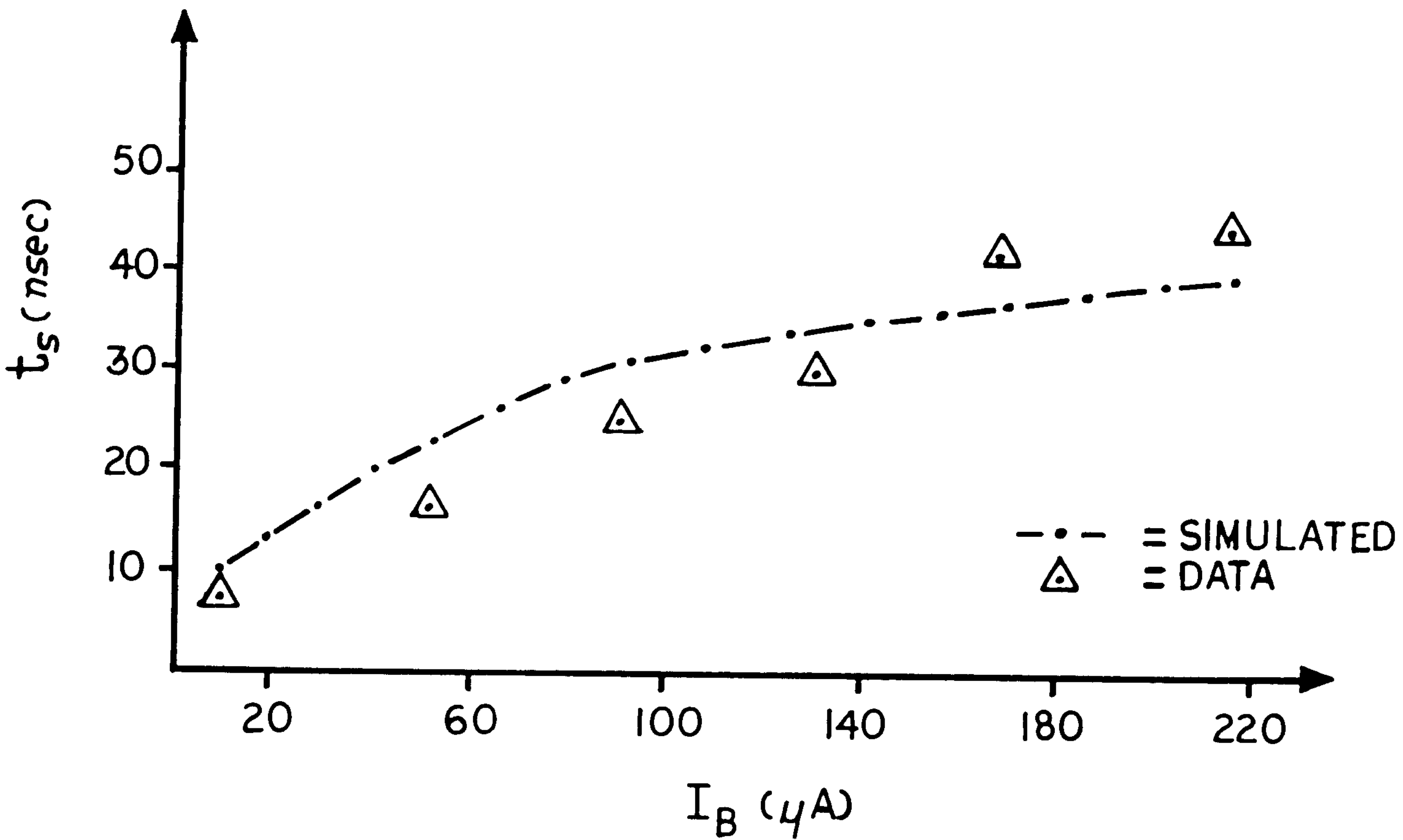
UP-TRANSISTOR — $1/2\pi f_T$ VS $1/I_C$ — UPWARD INJECTION

FIGURE 23

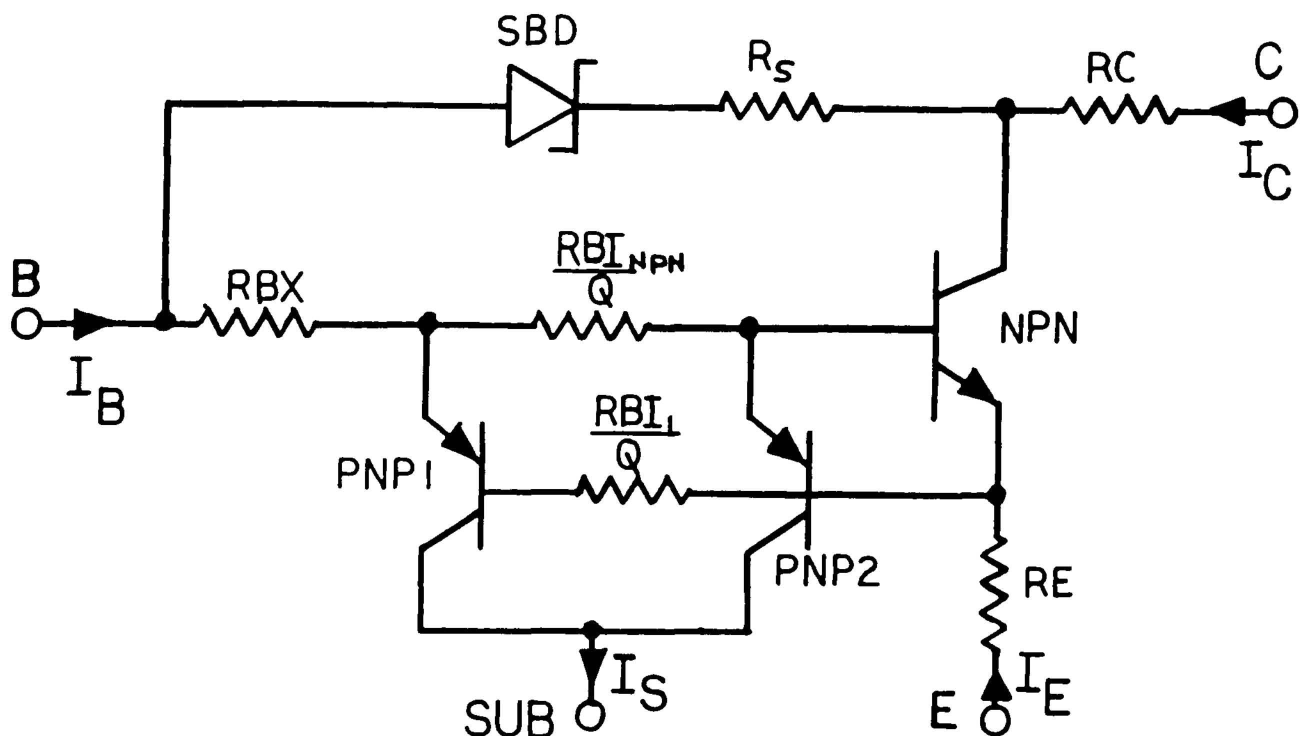


TEST CIRCUIT FOR
STORAGE TIME
MEASUREMENTS

FIGURE 24

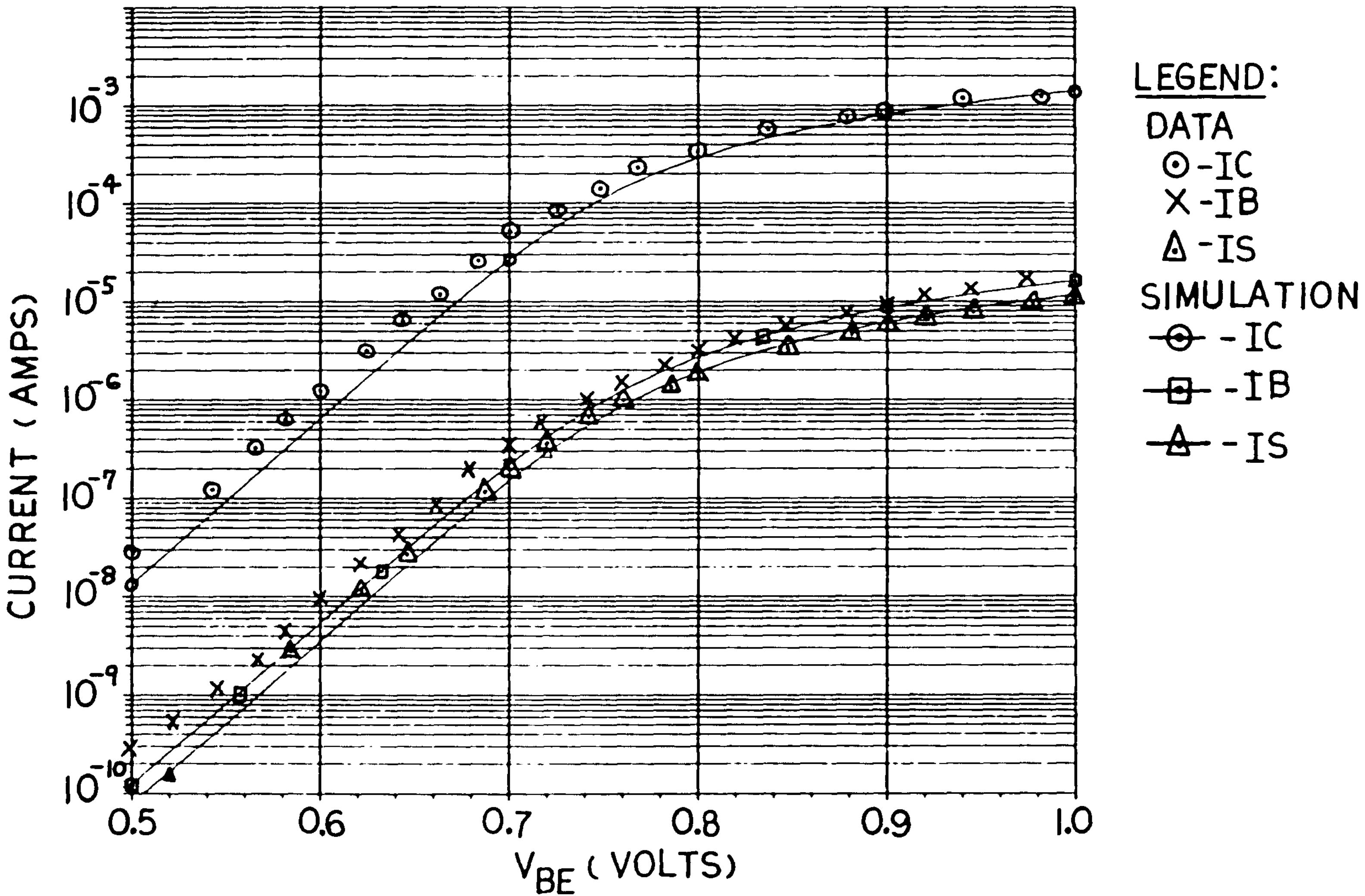


STORAGE TIME DATA
FOR AN UP-TRANSISTOR
FIGURE 25



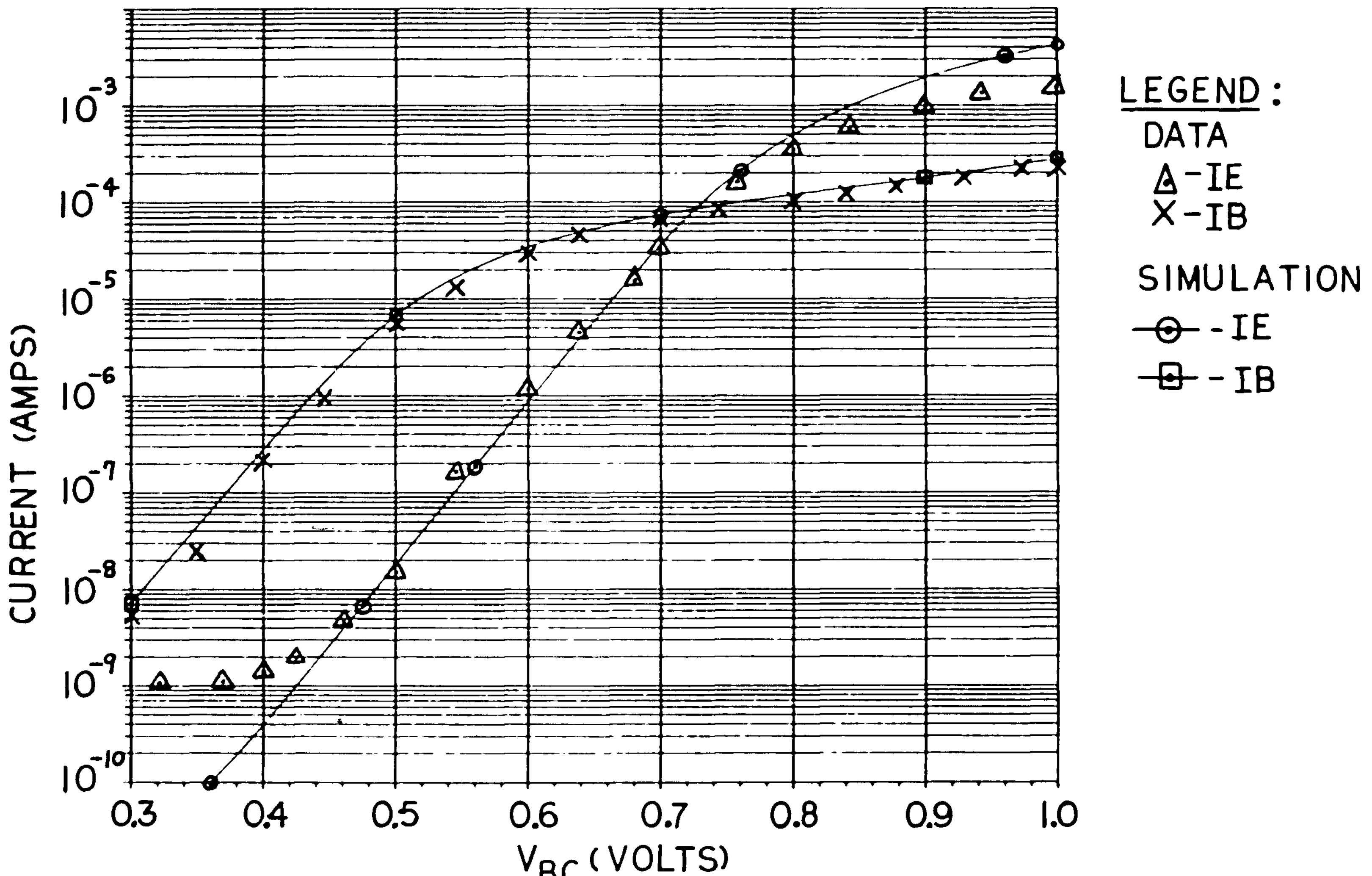
COMPOSITE CIRCUIT MODEL
OXIDE ISOLATED SCHOTTKY CLAMPED UP-TRANSISTOR

FIGURE 26



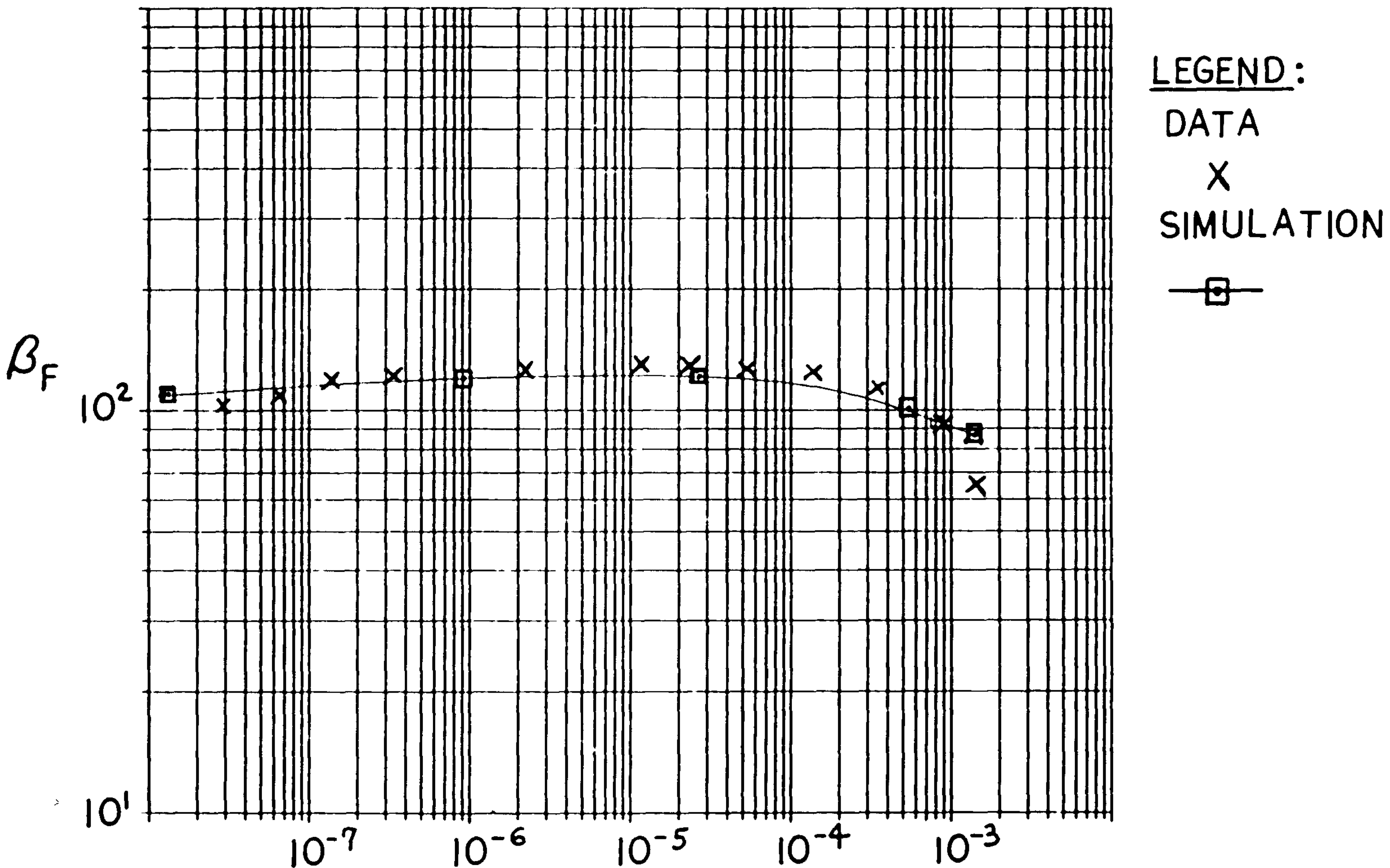
UPSHOT I-V CHARACTERISTICS—UPWARD INJECTION

FIGURE 27



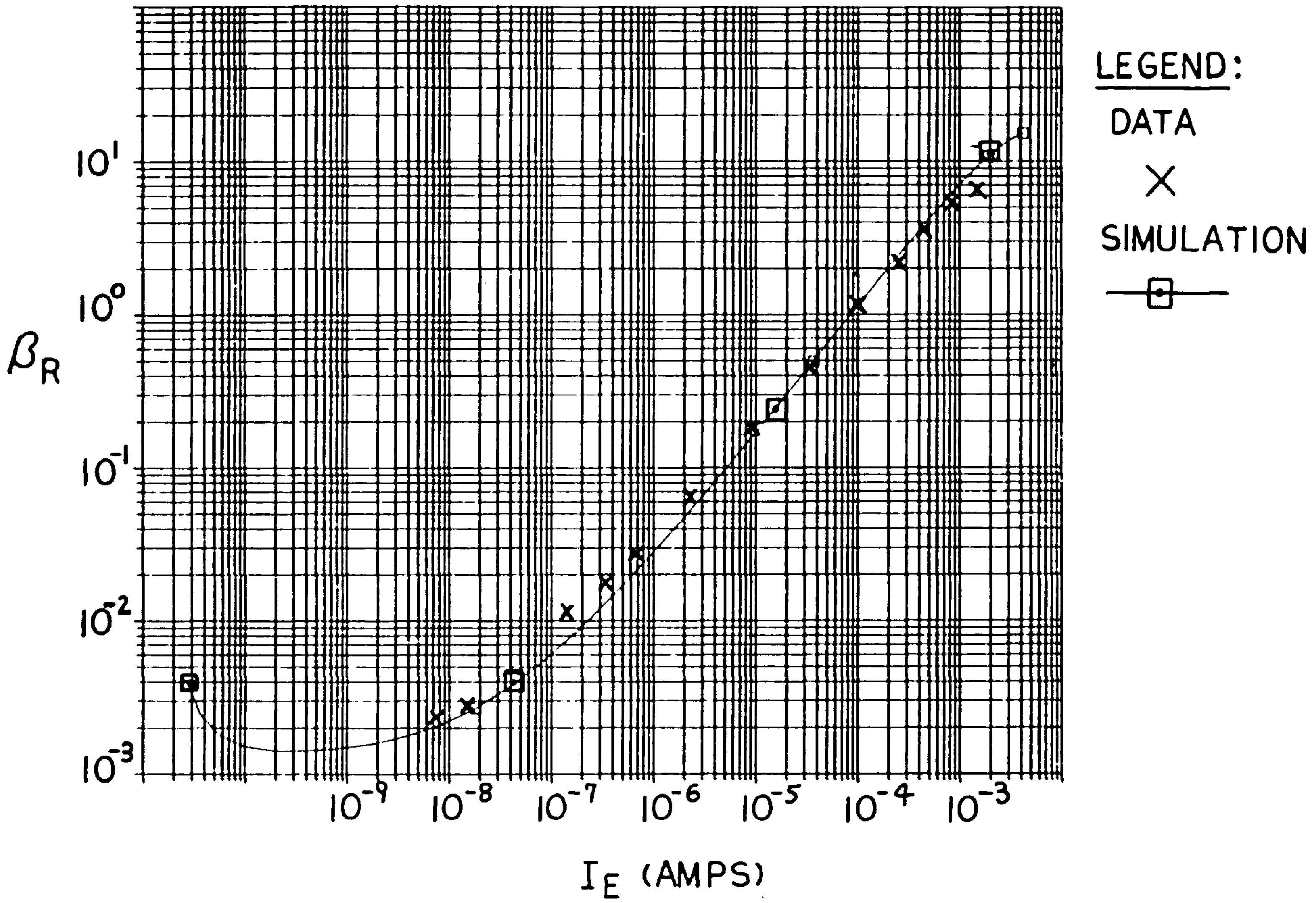
UPSHOT I-V CHARACTERISTICS—DOWNWARD INJECTION

FIGURE 28



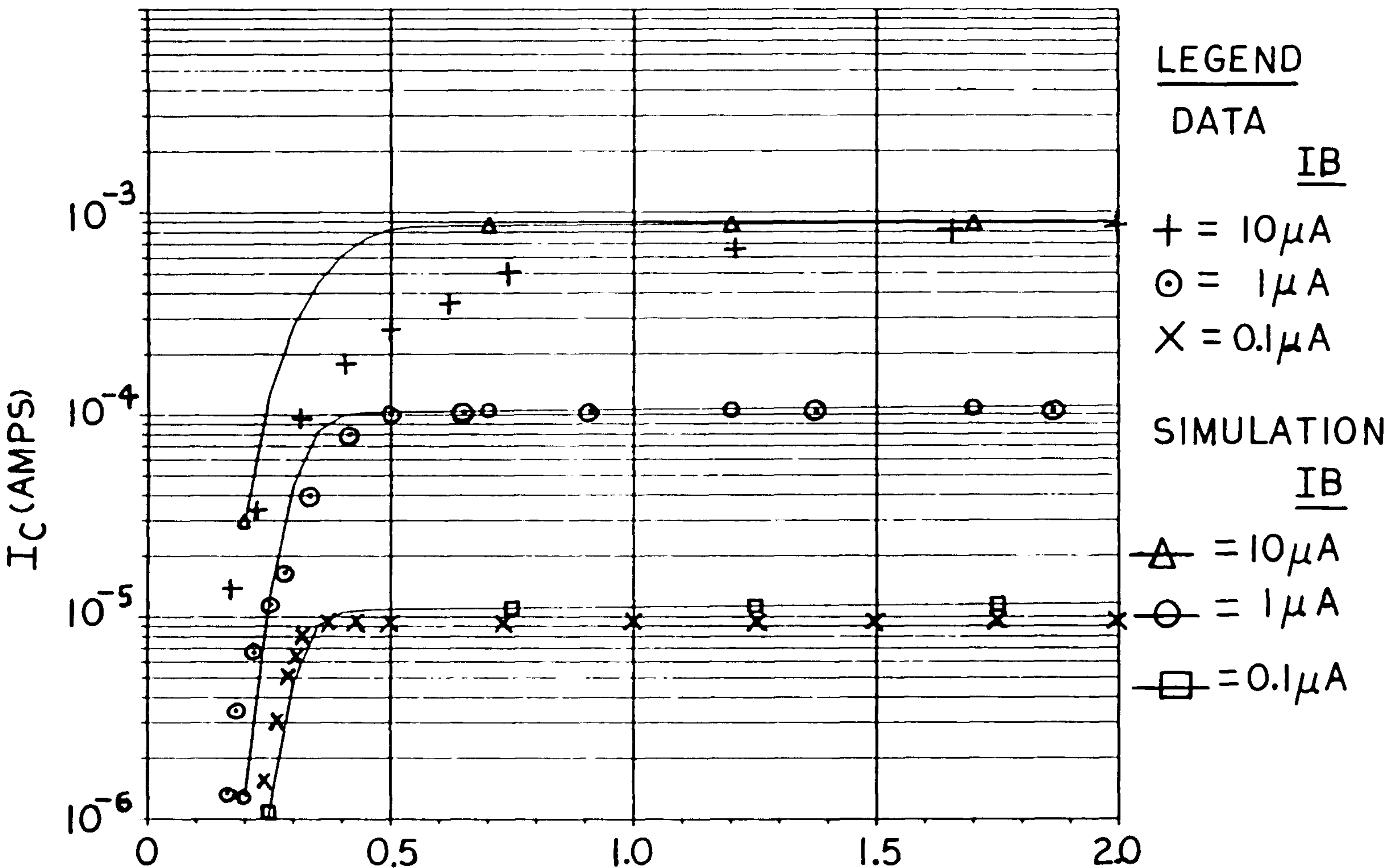
UPSHOT—GAIN—UPWARD INJECTION

FIGURE 29



UPSHOT—GAIN—DOWNWARD INJECTION

FIGURE 30



UPSHOT — SATURATION CURVES — UPWARD INJECTION

FIGURE 31

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VITA

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