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A Comparison of the CFSIM and CSIM IGFET Models.

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A Comparison of the CFSIM and CSIM IGFET Models

by

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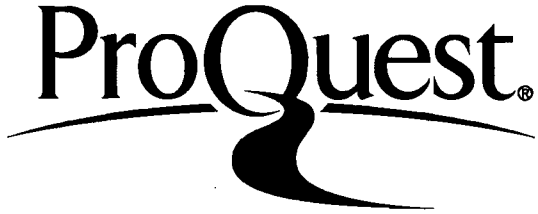

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LIST OF SYMBOLS

β	Gain of a device (A/V^2)
β_0	Gain of a large square device (A/V^2)
ϵ_0	Permittivity of free space ($8.85 \times 10^{-14} F/cm$)
k_{Si}	Dielectric constant of silicon (11.9)
k_{SiO_2}	Dielectric constant of silicon dioxide (3.9)
I_{DS}	Drain-to-source current
L	Coded channel length
L'	Electrical channel length
N_{SUB}	Substrate doping
Φ	Surface potential
t_{ox}	Gate oxide thickness
V_{BS}	Backgate-to-source voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{TH}	Threshold voltage
W	Coded channel width
W'	Electrical channel width

ABSTRACT

The evolution of Very Large Scale Integration (VLSI) has significantly changed the characteristics of MOS devices. This continuing evolution requires the transistor models used in computer aided design to adapt, or new models to be developed incorporating these changes. The Compact Short-Channel IGFET Model (CSIM), derived from the principles of semiconductor physics, is continually modified as new understandings in devices physics come to light. The Curve-Fitting Short-Channel IGFET Model (CFSIM) makes use of empirical curve fitting to characterize state of the art VLSI devices. The intent of this dissertation is to compare the accuracy of these two models for enhancement N-channel MOS devices, over a wide range of DC biasing conditions and device geometries.

Forty-eight transistors, located on the same 256K Dynamic RAM test chip, with geometries combining gate widths and lengths of 1 to 100 microns, were studied. Data was extracted from each device over the biasing range a transistor might experience during the operation of a 5v Dynamic RAM (i.e., back gate biasing of -2.0 to -6.0 volts, gate to source biases of 0.0 to 7.0 volts, and drain to source biases from 0.0 to 7.0 volts). Both CSIM and CFSIM model parameters were generated from this data.

The % RMS Deviation between experimental data extracted from each transistor and the predictions of each model for each transistor was determined using data points covering the aforementioned biasing range. Using the % RMS Deviations, variations in modeling accuracy as a function of device geometry can be observed. The Mean % RMS Deviation for each model, the average of the % RMS Deviations, was calculated for CSIM and for CFSIM, to be used as figure of merit.

Both CSIM and CFSIM performed within engineering accuracy, maintaining a Mean % RMS Deviation over the devices studied of less than five percent. CSIM modeled the devices with a Mean % RMS Deviation of 1.38%, while CFSIM fit the devices with a Mean % RMS Deviation of 3.75%. Both models display a modest degradation in accuracy as channel length falls below 2.25 microns.

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I. Introduction

The evolution of Very Large Scale Integration (VLSI), has significantly changed the characteristics of MOS devices. This continuing evolution requires the transistor models used in computer aided design to adapt, or new models to be developed incorporating these changes. Greater accuracy and economy in execution is required of these up-to-date models so that larger, more complex circuits can be reliably and rapidly simulated. To provide the circuit designer with a usable model and to facilitate the extraction of model parameters, simplicity in mathematical formulation is also required of the new models. Empirical curve fitting schemes and models of device physics have become sufficiently accurate and practical so that both were viable for use in the design of Large Scale Integrated circuits (LSI). The ability of these two alternative modeling techniques to describe VLSI transistor characteristics are tested and compared in this dissertation.

Physical models of the MOS transistor have been adapted to reflect new understandings in device physics. As gate oxide thickness decreased and the power supply standard remained constant, the increased electric field normal to the conducting channel began to exhibit a significant effect on carrier mobility[1]. This field tends to move the channel toward the Si-SiO_2 interface, where increased scattering results in decreased mobility. The depletion region widths about the drain and source became a significant fraction of channel length as horizontal geometries decreased, affecting gain and threshold voltage[2]. The finite output conductance of an IGFET operating in saturation became important as device density increased and speed-power products were required to decrease[3]. With the addition of new model parameters and multiplicative factors the physical models of the MOS transistor could accurately simulate the new generation of devices. The Compact Short-Channel IGFET Model (CSIM),[4] a model derived from the principles of semiconductor physics, has adapted to changes in device behavior by modeling these changes in terms of the device physics.

Curve fitting is an alternative approach to physical modeling. An empirical curve fitting model can provide an accurate, practical model of device characteristics. For example, the square law model of the Junction Field Effect Transistor in pinch-off:

$$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2 \quad (1)$$

where I_{DSS} and V_P are curve fit parameters with physical significance, is simple, practical, and quite accurate[5]. The Curve Fitting Short-Channel IGFET Model (CFSIM), provides a curve fitting alternative to physical modeling[6].

The CSIM model with its model parameters, and the CFSIM model with its curve fitting parameters are described within this dissertation. The CSIM and CFSIM model parameters were generated for forty-eight devices processed in a 256K Dynamic RAM technology. Device geometries combined gate lengths and widths of 1 to 100 microns. Model parameters were generated from device data covering the biasing range a transistor might experience during the operation of a 5 volt Dynamic RAM (i.e., back gate biasing of -2.0 to -6.0 volts, gate to source biases of 0.0 to 7.0 volts, and drain to source biases of 0.0 to 7.0 volts). The % RMS Deviation between experimental data extracted from each transistor and the predictions of each model for each transistor was determined using data points covering the aforementioned biasing range. Using the % RMS Deviations, variations in modeling accuracy as a function of device geometry can be observed. The Mean % RMS Deviation for each model, the average of the % RMS Deviations, was calculated for CSIM and for CFSIM, to be used as a figure of merit.

Though both models fit the device data with a Mean % RMS Deviation of less than five percent, the Compact Short-Channel IGFET Model displayed a Mean % RMS Deviation of less than half that of the Curve Fitting Short-Channel IGFET Model. Both models exhibit a modest degradation in accuracy as channel lengths fall below 2.25 microns.

II. The Compact Short-Channel IGFET Model

The Compact Short-Channel IGFET Model (CSIM) was developed out of the need for an accurate, practical model of simple mathematical formulation[7]. Being an extension of a first order model, if the CSIM model parameters which describe second order effects are set to their default values, the CSIM equations reduce to the classic equations:

$$I_{DS} = \beta[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \tag{2}$$

$$\text{for } 0 < V_{DS} \leqslant (V_{GS} - V_{TH})$$

and

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{3}$$

$$\text{for } V_{DS} > (V_{GS} - V_{TH}) > 0^{[8]}$$

The CSIM model has been adapted to the changes in device behavior brought about by technological advances made since its release in 1976. Changes in formulation have improved the model's accuracy in the biasing region about threshold, improved the accuracy with which the effect of substrate bias on output conduction is modeled, and explicitly incorporated the effect of drain bias on threshold voltage[9]. Despite these additions the CSIM model has maintained its practicality and economy of execution.

The DC CSIM model simulates device characteristics for IGFET operation in both the triode or linear region and the saturation region. It is assumed for gate voltages below threshold, the cut-off region, that current flow is negligible, and because devices are not normally operated in the breakdown region, it also is not modeled.

A complete DC description of an IGFET requires fourteen experimentally determined CSIM model parameters, four to define the geometry of the device and ten to characterize the D.C. device behavior. Threshold voltage is defined by CSIM to be:

$$V_{TH} = V_{TH0} - \eta^* V_{DS} \tag{4}$$

where

$$V_{TH0} = V_{T0} + K_1 \left(\sqrt{\Phi - V_{BS}} - \sqrt{\Phi} \right) \tag{4a}$$

$$\eta^* = \frac{\eta}{1 + \frac{GDC}{\sqrt{\Phi - V_{BS}}}} \tag{5}$$

and

V_{TO} Zero-bias threshold voltage;

Φ The Surface Potential;

K_1 Threshold voltage substrate bias dependent parameter;

η Threshold voltage drain bias dependent parameter;

GDC Threshold voltage substrate bias effect modulated by drain bias.

The term η^* models threshold voltage lowering due to applied V_{DS}. The degree of V_{DS} dependence is modulated by substrate bias. This modelation is modeled by parameter GDC.

The CSIM equations for drain-current are:

I. The Cutoff Region [$V_{GS} \leqslant V_{TH}$];

$$I_{DS} = 0 \tag{6}$$

II. The Triode Region [$V_{GS} > V_{TH}$ and $0 < V_{DS} < V_{DSAT}$];

$$I_{DS} = \frac{\beta}{1 - \Delta L/L} (V_{GS} - V_{TH} - \frac{V_{DS}}{2a}) V_{DS} \tag{7}$$

The Saturation Drain Voltage, V_{DSAT}, defined as

$$V_{DSAT} = \frac{V_{GS} - V_{TH0}}{a - \eta^*} \tag{8}$$

is decreased due to carrier velocity saturation modeled by the parameter a;

$$a = a_o[1 + \mu_1 (V_{GS} - V_{TH0})] \tag{9}$$

and increased by the threshold voltage lowering due to applied drain voltage modeled by η^*.

The reduction of surface mobility due to vertical gate fields is modeled by reducing the gain coefficient β as V_{GS} increases;

$$\beta = \frac{\beta_o}{1 + \mu_o(V_{GS} - V_{TH})} \tag{10}$$

The channel shortening factor $\Delta L/L$ is modeled by the parameters ADG and BGS, representing the extent to which the vertical gate field fringes into the depletion region near the drain, and is drain and backgate bias dependent[10].

III. The Saturation Region [$V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{DSAT}$];

$$I_{DS} = \frac{\beta}{2a} \frac{(V_{GS} - V_{TH})^2}{(1 - \Delta L/L)} \tag{11}$$

The use of the CSIM model is facilitated by the availability of packaged routines which automate the measurement of device data, the extraction of model parameters from the device data, and the generation of model files.

III. The Curve Fitting Short-Channel IGFET Model

The Curve Fitting Short-Channel IGFET Model (CFSIM) was developed as an alternative to the CSIM model. Both the triode and saturation regions of transistor operation are modeled by CFSIM. Subthreshold conduction and breakdown, considered to define the limits of device operation, are not modeled.

The CFSIM model has shown itself to be adaptable to changes in device characteristics brought about by technological advances. The reformulations within CFSIM made since its development in 1977 have improved the modeling of threshold voltage by taking into account modulation of the substrate bias effects by drain voltage, improved the modeling of channel mobility modulation by the gate electric field normal to the channel, increased the biasing region over which the model is accurate, and improved the modeling of drain conductance in the saturation region[10].

With the gate voltage held at a constant value above threshold, the drain current vs. drain voltage characteristic of an IGFET is, to a good approximation, independent of substrate bias; that is, substrate bias manifests itself primarily as a shift in threshold voltage[11]. Using this approximation, the CFSIM curve fitting scheme models threshold voltage and drain current vs. drain voltage characteristics independently.

The definition of threshold voltage used by the CFSIM model is that gate voltage which, under drain and substrate biasing, allows a predetermined amount of current to flow in the device. This "threshold current" can be chosen either empirically or extracted from device characteristics. The empirically chosen threshold current would be sufficiently small so that at a gate bias one-half volt below the threshold voltage essentially zero current would flow through the device. A threshold current can be extracted from device characteristics by applying an extrapolated threshold voltage to the gate of a device, forcing the substrate and drain to the potentials used to extract the threshold voltage and measuring the drain current. The threshold voltage may be determined by extrapolating the linear saturation region drain current vs. gate voltage characteristics to the gate voltage axis and subtracting one-half the applied drain voltage (See Figure 1). The latter definition of the threshold

current, and therefore threshold voltage, will be used in this dissertation.

A complete D.C. description of an IGFET requires a total of sixteen CFSIM curve fitting parameters, four to define the device geometry and the remaining twelve to curve fit the D.C. behavior. The CFSIM threshold voltage model is:

$$V_{TH} = V_{TO} + (K_1 - K_{12} V_{DS})\sqrt{|V_{BS}| + \Phi} - K_2 V_{DS} \tag{12}$$

where

V_{TO} Zero-bias threshold voltage;

K_1 Threshold voltage substrate bias curve fitting parameter;

K_2 Threshold voltage drain bias curve fitting parameter;

K_{12} Threshold voltage substrate bias effect modulated by drain bias.

The CFSIM equations for drain current are:

I. The Cutoff Region [$V_{GS} < V_T$];

$$I_{DS} = 0 \tag{13}$$

II. The Saturation Region [$V_{GS} > V_T$ and $V_{DS} > V_{DSAT}$];

$$I_{DS} = I_O + SV_{DS} \tag{14}$$

I_O is the current axis intercept of the extrapolated linear saturation region I_{DS} vs. V_{DS} characteristics (See Figure 2). I_O is modeled by three curve fitting parameters A_1, B_1, and n, and is dependent upon the value of gate voltage above threshold:

$$I_0 = \left\{\frac{B_1}{n\left(\frac{A_1}{1+1/n}\right)^{(n-1)}}\right\}(V_{GS} - V_{TH})^n \tag{15}$$

$$\text{for } (V_{GS} - V_{TH}) \leq A_1/(1-(1/n))$$

and

$$I_O = B_1(V_{GS} - V_{TH} - A_1) \tag{16}$$

$$\text{for } (V_{GS} - V_{TH}) > A_I/(1-(1/n))$$

$(A_I/(1-1/n))$ represents the transition to the region of operation in which carrier velocity saturates.

S is the slope of the linear saturation region I_{DS} vs. V_{DS} characteristics (See Figure 2). S is modeled by two curve fitting parameters A_S and B_S, and is I_O dependent:

$$S = (I_O/A_S)^{B_S} \tag{17}$$

V_{DSAT} is defined as that drain voltage at which the nonlinear triode region and the linear saturation region characteristics meet. V_{DSAT} is modeled by three curve fitting parameters m, β_o, and μ_o, and is bias dependent:

$$V_{DSAT} = \frac{m\, I_O}{\beta(V_{GS} - V_{TH})} \tag{18}$$

where

$$\beta = \frac{\beta_o}{1 + \mu_o(V_{GS} + V_{TH})} \tag{19}$$

III. The Triode Region [$V_{GS} > V_T$ and $V_{DS} \leqslant V_{DSAT}$];

$$I_{DS} = (I_o + SV_{DS})\ \{1 - (1 - \frac{V_{DS}}{V_{DSAT}})^m\} \tag{20}$$

Note that the non-linear characteristics of the triode region are imposed upon the extension of the linear saturation region characteristics into the triode region by a non-linear multiplicative factor that approaches zero as V_{DS} decreases and approaches unity as V_{DS} approaches V_{DSAT}.

Though CFSIM is an empirical model of device characteristics there are CFSIM model parameters that have physical significance, β and V_{DSAT} for example, with bias dependence very similar to that derived from semiconductor physics.

As with the CSIM model, the extraction of CFSIM model parameters is facilitated by the availability of packaged routines which automate the data extraction and model file generating process.

IV. Investigational Procedure

The purpose of this study is to determine which model, CSIM or CFSIM, most accurately describes modern VLSI devices over a practical range of biases and device dimensions. To achieve this end forty-eight devices located on a 256K Dynamic RAM test chip were characterized. Measurements made on this test chip revealed nominal gate oxide thickness, nominal effective channel doping, and slightly longer than nominal channel lengths. The coded, or mask, dimensions of these devices combine gate lengths of 100.0, 5.0, 3.0, 2.75, 1.75, and 1.25 microns with coded channel widths of 100.0, 3.0, 2.25, 2.0, 1.5, and 1.0 microns. The operating range covers the biasing a device might experience during the operation of a 5 volt Dynamic RAM (i.e., substrate biases of -2.0 to -6.0 volts, gate to source biases of 0.0 to 7.0 volts, and drain to source voltages of 0.0 to 7.0 volts).

For each device CFSIM and CSIM model parameters were generated and the % RMS Deviation of data points distributed over the biasing range was determined. The % RMS Deviation is defined as:

$$\%\text{RMS Dev.} = \left[\sum\left(\frac{\text{Measured } I_{DS} - \text{Modeled } I_{DS}}{\text{Measured } I_{DS}}\right)^2\right]^{1/2} \text{X } 100\% \qquad (21)$$

The results were analyzed to determine which model provides greater overall accuracy as well as to determine model accuracy variations with device geometry.

The measurement of device characteristics was performed on a Keithley LPT System 2, a computer controlled test set capable of making interconnections between device nodes, power supplies and a digital multimeter; making measurements; and manipulating data. Running MOSPAR, a Fortran program written for the Keithley, device data files are created and formated for each device probed. These files contain device identification, processing parameters, threshold and current-voltage characteristics. Once all the device data files to be used in this study were generated, they were edited into a single block and transmitted to a larger, more versatile Honeywell computer where the individual device data files were reconfigured and stored. CFSIM model

parameters and a model file were generated for each device by a Fortran routine, CFSIMS. To generate CSIM models the device data files were structured to be compatible with the CSIM model parameter extraction routine MOSPAC. The MOSPAC compatible data files are generated by using another FORTRAN program MOSDAT to restructure the MOSPAR generated data files. Both MOSPAC and CFSIMS generate the % RMS Deviation for each device over all data points used to extract the model parameters, providing the data for this model comparison (See Figure 3).

The extraction of the gate oxide thickness and effective channel doping, valid for the entire test chip, is performed by MOSPAR prior to the measurement of device characteristics. The junction depth, approximately 0.4 microns, was provided as an input parameter to MOSPAR.

Gate oxide thickness, tox, is determined by biasing a large MOS capacitor (325 x 355 microns), which has gate oxide as its dielectric, into accumulation so that a measurement of the gate capacitance will correspond to oxide capacitance. Negative ten volts was applied to the polysilicon gate, assuring the MOS structure is biased into accumulation. Using the measured capacitance and the parallel plate capacitance formula

$$C_{ox} = (\epsilon_o k_{SiO_2} \text{Area})/t_{ox} \tag{22}$$

the gate oxide thickness t_{ox}, was determined to be 487 Angstroms.

To determine the effective substrate doping, a large square device (100 x 100 microns) was probed. The slope of the extrapolated threshold voltage plotted as a function of

$$\sqrt{V_{BS} + \Phi} - \sqrt{\Phi} \tag{23}$$

for sufficiently large substrate biases is related to the effective substrate doping by the classical long channel equation:[12]

$$N_{SUB} = \left[\frac{(\text{Slope})\epsilon_o k_{SiO_2}}{t_{ox}}\right]^2 \frac{1}{2\epsilon_o k_{Si} q} \tag{24}$$

Using the extrapolated threshold voltage at substrate biases of -3.0, -6.0, and -9.0, with a drain voltage of 0.2 volts, the slope was determined using a least square fit. Using the gate oxide thickness previously determined and the calculated slope, the effective doping was found to be 2.96 x

$10^{16}/cm^3$. (See Figure 4)

Threshold measurements are made next by MOSPAR. The threshold current is measured with a substrate bias of -2.5 volts and 0.1 volts on the drain (See pg. 8 for a description of the threshold extrapolation method). Using this threshold current, twenty-five threshold voltages were measured at five substrate biases (-2.0, -3.0, -4.0, -6.0, and -8.0 volts) combined with five drain voltages (1.0, 2.0, 3.0, 5.0, and 7.0 volts). MOSPAR performs a four-parameter least square fit on the twenty-five threshold voltages to determine the four CFSIM threshold voltage parameters (V_{TO}, K1, K2, and K12). V_{TO}, the extrapolated zero bias threshold voltage, is then adjusted so the calculated threshold voltage corresponds to the extrapolated threshold voltage used to determine the threshold current.

The separate modeling of the threshold voltage and drain current characteristics by CFSIM requires that a drain current curve be extracted for a constant value of V_{GS} - V_{TH}. This requires that the threshold voltage be calculated at each drain voltage point measured and that the threshold be added to the value of V_{GS} - V_{TH} to determine the gate to source voltage to be applied. Drain current versus drain voltage points were measured for increasing values of V_{GS} - V_{TH} (0.7, 1.4, 2.1, 2.8, 3.5, 4.2, 4.9, 5.6, and 6.3 volts), while cycling through three values of substrate bias (-2.0, -4.0, and -6.0). Fifty drain current vs. drain voltage points are measured at each gate and substrate bias. Each resulting drain current versus drain voltage curve is analyzed in three segments. The gain of the linear portion of the triode region is calculated. This gain and a single linear triode region data point are stored in the data file. In the saturation region the slope S, and zero drain voltage intercept I_O, are calculated. The slope, zero drain voltage intercept, and a single saturation region data point are stored. In the transition region between the linear triode and saturation regions, three points, appropriately spaced to describe the curvature of the region, are stored (See Figure 5). Thus, for each of the nine combinations of V_{GS} - V_{TH} and V_{BS}, five data points plus the linear region gain and the saturation region slope and intercept are stored. MOSPAR then formats and stores the device geometry, process parameters, threshold measurements and parameters, and the drain current-voltage characteristics on a floppy disk.

Once the data has been extracted for each device, a string of editing commands gathers and stores the individual device data files in a single file. This single file is transmitted via a telephone link to a larger Honeywell computer, where an editor routine reconfigures the individual device data files.

CFSIM Model Parameter Extraction

The extraction of CFSIM model parameters requires that the carrier saturation velocity, the scattering limited velocity with which an electron can travel in the channel, be determined. The slope of an I_O versus V_{GS} - V_{TH} curve for a wide, short channel device (L' $\leqslant$ 2.25 microns), divided by the parallel plate component of the gate oxide capacitance per unit length of gate for this device, defines the carrier saturation velocity. Using a 100 micron long device, the slope of I_O versus V_{GS} - V_{TH} was calculated, using a least square fit, to be 3.79mA/V. Using the gate oxide thickness determined by MOSPAR, the gate capacitance per unit length for this device was found to be 7.09 x 10^{-10}F/cm, resulting in a carrier saturation velocity of 5.30 x 10^6cm/sec (See Figure 6).

The difference between electrical channel dimensions and the coded gate dimensions was determined by plotting the linear region gain against the coded gate dimensions. Defining the gain of a large square device (100 x 100 microns) as β_o, the quotient of the linear region gain of a device, β, by β_o is the ratio of electrical channel width to length;

$$\beta/\beta_o = W'/L' \tag{25}$$

A plot of coded gate width divided by β/β_o versus coded gate length for devices of a constant, wide width will intercept the coded gate length axis at -DL, the difference between the electrical channel length and the coded gate length (See Figure 7). Similarly, a plot of the product of coded gate length and β/β_o against the coded gate width for devices of a constant, long length will intercept the coded gate width axis at -DW, the difference between the electrical channel width and the coded gate width (See Figure 8). DW and DL were determined to be 0.13 and -0.53 microns respectively. The value of DW and DL, together with the carrier saturation velocity are stored in a parameter file accessed during the extraction of CFSIM model parameters and the generation of CFSIM model

files.

Using the individual device data files and the aforementioned parameter file, CFSIMS extracts CFSIM model parameters. Data from the appropriate segments of the current-voltage curves under the various biases is used to fit each model parameter. CFSIMS then calculates the % RMS Deviation over all the data points used to extract the model parameters.

CSIM Model Parameter Extraction

To extract CSIM model parameters, the device data must be manipulated and the files formatted to be compatible with the CSIM model extraction routine MOSPAC. The program MOSDAT is used to extract from a data file the twenty-five threshold measurements and the forty-five drain current measurements for each transistor. Recombining the modeling of threshold and drain current characteristics, MOSDAT uses the CFSIM threshold voltage parameters to calculate the threshold voltage at each of the forty-five data points and adds the threshold voltage to the value of V_{GS} - V_{TH}. The output of MOSDAT is a file containing the tabulation of V_{BS}, V_{DS}, and threshold voltage; and V_{BS}, V_{GS}, V_{DS}, and drain current. Using this "raw" data, MOSPAC extracts parameters for a first-order effects model to be used as the starting point in an interactive process of extractions in an effort to reduce the % RMS Deviation of the model over the entire biasing range to a minimum.

The % RMS Deviation provides a figure of merit with which the overall accuracy of the CSIM and CFSIM models will be compared and any variations in accuracy with geometry can be observed. For the purpose of comparison, the same data use in the CFSIM parameter extractions will be used for the CSIM parameter extractions. This requires the discarding of complete drain current vs. drain voltage curves, as is done by CFSIMS, when sport data points are found. A Mean % RMS Deviation will be calculated for the CSIM models and for the CFSIM models. The model with the smaller Mean % RMS Deviation has attained the greater overall accuracy.

V. Results

The % RMS Deviations of each device for the CSIM model are shown in Table 1, and for the CFSIM model in Table 2. The measured, CSIM modeled and CFSIM modeled drain-current characteristics for four devices (combining the maximum width and length of 100 microns with the minimum width and length used in the design of the 256K Dynamic RAM, 2 and 2.25 microns respectively) are depicted in Figures 9, 10, 11, and 12.

CSIM % RMS Deviation Analysis

The Mean % RMS Deviation for the CSIM model, for the forty-seven devices modeled in this study, is 1.38% (See Table 1). From the average deviation of devices with a constant length it is apparent that the CSIM model suffers a modest decrease in accuracy for devices with channel lengths shorter than 2.25 microns. No variation in accuracy with channel width is observed.

CFSIM % RMS Deviation Analysis

The Mean % RMS Deviation for the CFSIM model, for the forty-seven devices modeled in this study, is 3.75% (See Table 2). Though the data in Table 2 shows no apparent geometry variation, the average deviation for devices of constant length shows a degradation in accuracy when channel lengths become smaller than 2.25 microns. There is no apparent variation with channel width.

VI. Conclusions

Inadequacies in CSIM and CFSIM and the methods of parameter extraction are made evident by the data presented in Figures 9 through 12. The attempt to optimize the modeling of short and narrow channel devices leads to problems in modeling a long, wide device, as shown in Figure 9. The onset of breakdown within the modeled biasing range, as has happened for the short channel device of Figure 10, causes problems for both models. An erroneous data point in each of two high gate voltage, drain current vs. drain voltage curves of the 2 microns wide, 100 microns long device, Figure 11, required that both curves be removed from the data from which the model parameters were extracted. The effect of the loss of the complete curves because of two bad data points is obviously extreme, and in the case of CSIM unnecessary.

Figure 12 displays both models at their best. While both CSIM and CFSIM fit this 2 micron wide, 2.25 micron long device well, the more accurate global fit of CSIM is evident.

Though both CSIM and CFSIM performed well, for the forty-seven devices modeled the Mean % RMS Deviation of the CSIM, 1.38%, is but 37% of the Mean % RMS Deviation of CFSIM, 3.75%. The better fit of CSIM can be attributed to the interactive parameter extraction technique used by MOSPAC. While MOSPAC attempts to reduce the % RMS Deviation to a minimum, CFSIMS fits the model parameters to a portion of the device characteristics without an attempt at % RMS Deviation minimization.

CSIM should be used for modeling requiring high accuracy. When less accuracy is needed, CFSIM may be used.

References

[1] Sabnis, A. G. and Clemens, J T., "Characterization of the Electron Mobility in the Inverted <100> Si Surface", I.E.E.E. Technical Digest, International Device Meeting, 1979, pg. 18.

[2] Lis, S. and Nagel, L. W., "Small Signal MOSFET Models for Analog Circuit Design", I.E.E.E. Journal of Solid State Circuits, Vol. SC - 17, No. 6, pg. 996, December 1982.

[3] Lis, S. and Nagle, L. W., Ibid., pg. 997

[4] Johnston, R. L. and Poon, H. C., "A Compact Short - Channel IGFET Model (CSIM)", Bell Telephone Laboratories, April 1976. Unpublished.

[5] Gray, P. R. and Meyer, R. G, Analysis and Design for Analog Circuit Design. John Wiley and Sons, 1977, pg. 51.

[6] Jones, J. R., Rosenzweig, W. and Serpiello, J. W., "Simple Short - Channel MOS Transistor Model", Bell Telephone Laboratories, March 1977. Unpublished.

[7] Lis, S. and Nagel, L. W., Ibid., pg. 983-998.

[8] Liu and Nagel, Ibid., pg. 987.

[9] Liu and Nagel, Ibid., pg. 984.

[10] Liu and Nagel, Ibid., pg. 987.

[11] Kamins, T. I. and Muller, R. S., Device Electronics for Integrated Circuits. John Wiley and Sons, 1977, pgs. 352-354.

[12] Rosenzweig, W. and Weiner, A. S., "Revised CFSIM MOS Transistor Model (IM)", Bell Telephone Laboratories, January 1983. Unpublished.

[13] Jones, Rosenzweig and Serpiello, Ibid., pg. 3.

[14] Kamins and Muller, Ibid., pg. 361.

Bibliography

Cong, L., "CSIM Model Update". Bell Telephone Laboratories, August 14, 1981.

Cong, L. and Poon, H. C., "MOSPAC User's Guide". Bell Telephone Laboratories, April 15, 1980.

Gray, P. R. and Meyer, R. G., Analysis and Design of Analog Integrated Circuits. John Wiley and Sons, 1977.

Hamilton, D. J., Lindholm, F. A. and Marshak, A. H. Principals and Applications of Semiconductor Device Modeling. Hold, Rinehart, and Winston, New York, 1971.

Herskowitz, G. J. and Schilling, R. B. Semiconductor Device Modeling for Computer Aided Design. McGraw Hill Book Company, New York, 1972.

Jindal, R. P. and Bayruns, R. J., "A New Fine Line MOS Process File for Circuit Simulation". Bell Telephone Laboratories, July 15, 1981.

Liu S. and Nagel, L. W., "Small Signal MOSFET Models for Analog Circuit Design", I.E.E.E. Journal of Solid State Circuits, Vol. SC-17, No. 6, pgs. 983-998, December 1982.

Logan, J. "Characterization and Modeling for Statistical Design", Bell System Technical Journal Vol. 50, (April 1971): 1105-1147.

Montgomery, J. C., "A Comparison of Threshold Voltage Models for NMOS Transistors Including Short-Channel and Narrow Width Effects". Bell Telephone Laboratories, February 27, 1981.

Muller, R. S. and Kamins, T. I. Device Electronics of Integrated Circuits. John Wiley and Sons, 1977.

Poon, H. C. and Johnston, R. L., "A Compact Short-Channel IGFET Model (CSIM)". Bell Telephone Laboratories, April 30, 1976.

Rosenzweig, W. and Dumbri, A. C., "CFSIM MOS Transistor Model Update". Bell Telephone Laboratories, July 13, 1978.

Rosenzweig, W., et. al., "Simple Short-Channel MOS Transistor Model". Bell Telephone Laboratories, March 8, 1977.

Sabnis, A. G. and Clemens, J. T., "Characterization of the Electron Mobility in the Inverted <100> Si Surface", I.E.E.E. Technical Digest, International Device Meeting, 1979.

Weiner, A. S., and Rosenzweig, W., "Revised CFSIM MOS Transistor Model (IM)". Bell Telephone Laboratories, January 29, 1982.

TABLE 1

CSIM

% RMS Deviation of I-V Model and % Deviation of Threshold Model

		Lot #343		Wafer #7	Test Site #2			
	Gate Length (μm)	100	3	2.25	2	1.5	1	$\bar{x}$
Gate Width (μm)	100	1.19[2] 0.52	1.09[2] 0.69	1.18 0.74	1.19[2] 0.76	1.31[2] 0.77	1.26 0.95	1.20 0.74
	5	0.77[1] 0.42	0.92 0.66	0.75[1] 0.73	0.86[1] 0.76	1.13[2] 0.81	1.76[3] 0.88	0.91 0.71
	3	0.83[1] 0.38	1.03[1] 0.62	1.48 0.71	1.44 0.72	1.56 0.80	1.49 0.89	1.31 0.69
	2.75	1.09[3] 0.39	1.29[2] 0.62	1.43[1] 0.71	1.29 0.69	1.32 0.80	1.60 0.88	1.34 0.68
	2.25	0.82[1] 0.39	*	1.03 0.69	1.25[2] 0.72	1.18[2] 0.77	1.35 0.86	1.25 0.69
	2	1.41 0.41	2.02[2] 0.63	1.63[1] 0.67	1.73[1] 0.70	1.88 0.76	1.03 0.85	1.72 0.67
	1.75	1.55 0.44	2.31[1] 0.60	1.48 0.69	2.03 0.72	1.28 0.74	1.53 0.82	1.70 0.67
	1.25	1.70[3] 3.84	2.82[1] 0.82	0.77 0.98	0.88 0.78	1.30 0.72	2.34 0.80	1.64 0.82
	$\bar{x}$	1.17 0.42	1.64 0.66	1.29 0.74	1.33 0.73	1.37 0.77	1.50 0.77	1.38 0.71

* Errors in the transmission of the data from floppy disk to the Honeywell computer rendered this file inaccessible.

1 To eliminate sport data points a single V_{GS}-V_{TH} curve was excluded from the model parameter extraction.

2 To eliminate sport data points two V_{GS}-V_{TH} curves were excluded from the model parameter extraction.

3 To eliminate sport data points three V_{GS}-V_{TH} curves were excluded from the model parameters extraction.

TABLE 2

CFSIM

% RMS Deviation of I-V Model and % Deviation of Threshold Model

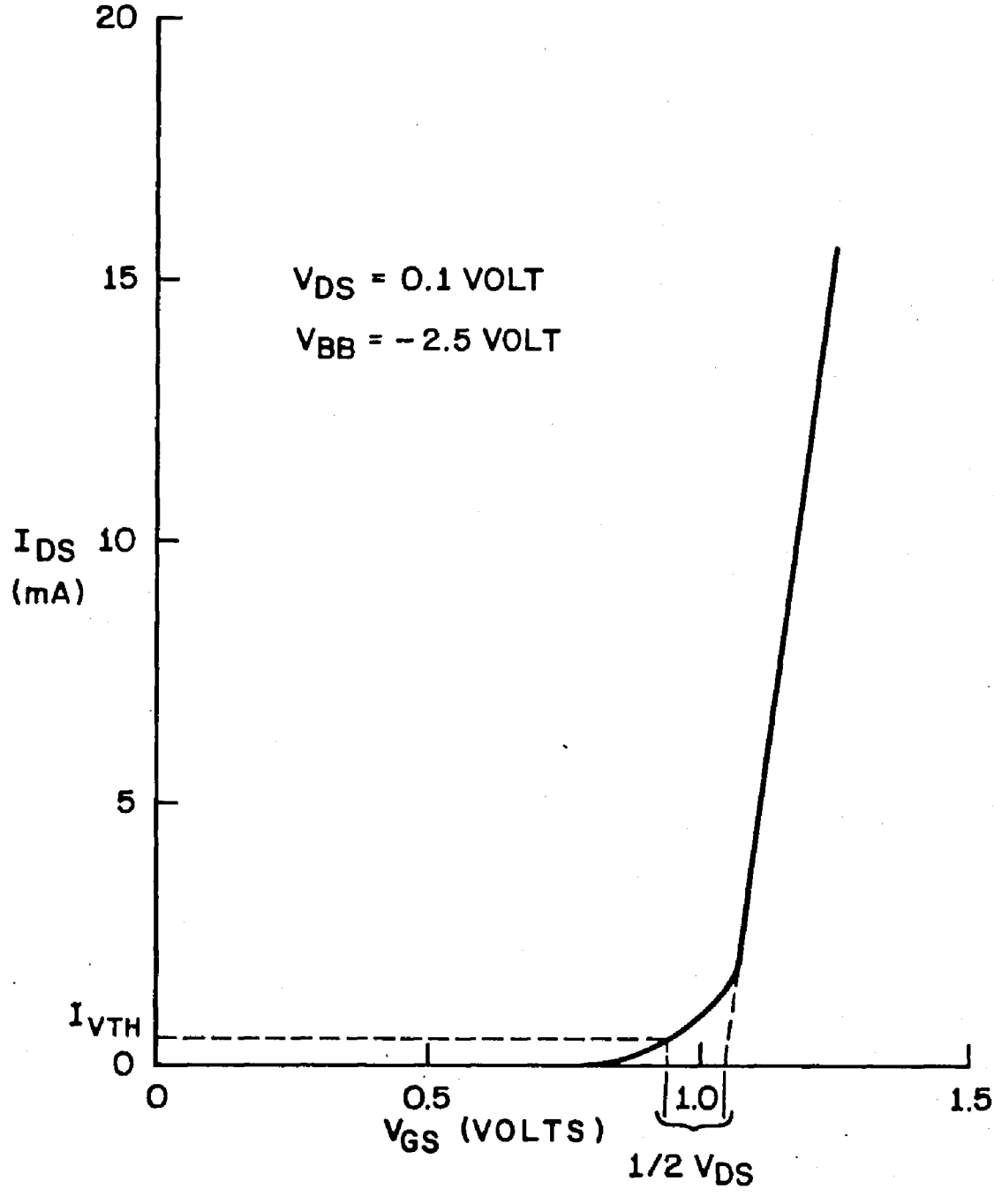
	Gate Length (μm)	Lot #343 Wafer #7 Test Site #2 100	3	2.25	2	1.5	1	$\bar{x}$
	100	3.31[2]	4.59[2]	4.35[2]	3.98[2]	4.23[2]	2.58	3.84
		0.29	0.60	0.80	0.95	0.98	1.60	0.87
	5	3.25[2]	2.75	2.60[2]	2.71[1]	2.30[2]	1.86[3]	2.58
		0.42	0.50	0.76	0.85	1.01	1.35	0.82
	3	3.75[2]	3.29[1]	4.04	4.30	3.33	2.30	3.50
		0.42	0.45	0.58	0.61	0.82	1.21	0.68
Gate Width (μm)	2.75	4.34[3]	3.43[2]	3.15[1]	3.58	4.22	4.04	3.79
		0.36	0.45	0.59	0.59	0.84	1.21	0.67
	2.25	3.94[1]	*	3.73	4.39[2]	2.85[2]	3.08	3.60
		0.33	0.48	0.64	0.59	0.65	0.92	0.60
	2	4.49	4.38[2]	4.02[1]	3.89[1]	4.04	4.98	4.30
		0.42	0.80	0.61	0.66	0.79	0.95	0.71
	1.75	4.52	4.27[2]	4.34	3.81	3.92	4.41[2]	4.22
		0.51	0.78	0.72	0.82	0.73	0.76	0.72
	1.25	3.03[3]	3.79[1]	4.34	4.71	4.45[1]	4.56	4.15
		2.05	1.33	1.70	1.14	1.58	1.05	1.48
	$\bar{x}$	3.83	3.79	3.82	3.92	3.67	3.48	3.75
		0.60	0.67	0.80	0.78	0.93	1.13	0.82

* Errors in the transmission of the data from floppy disk to the Honeywell computer rendered this file inaccessible.

1 To eliminate sport data points a single V_{GS}-V_{TH} curve was excluded from the model parameter extraction.

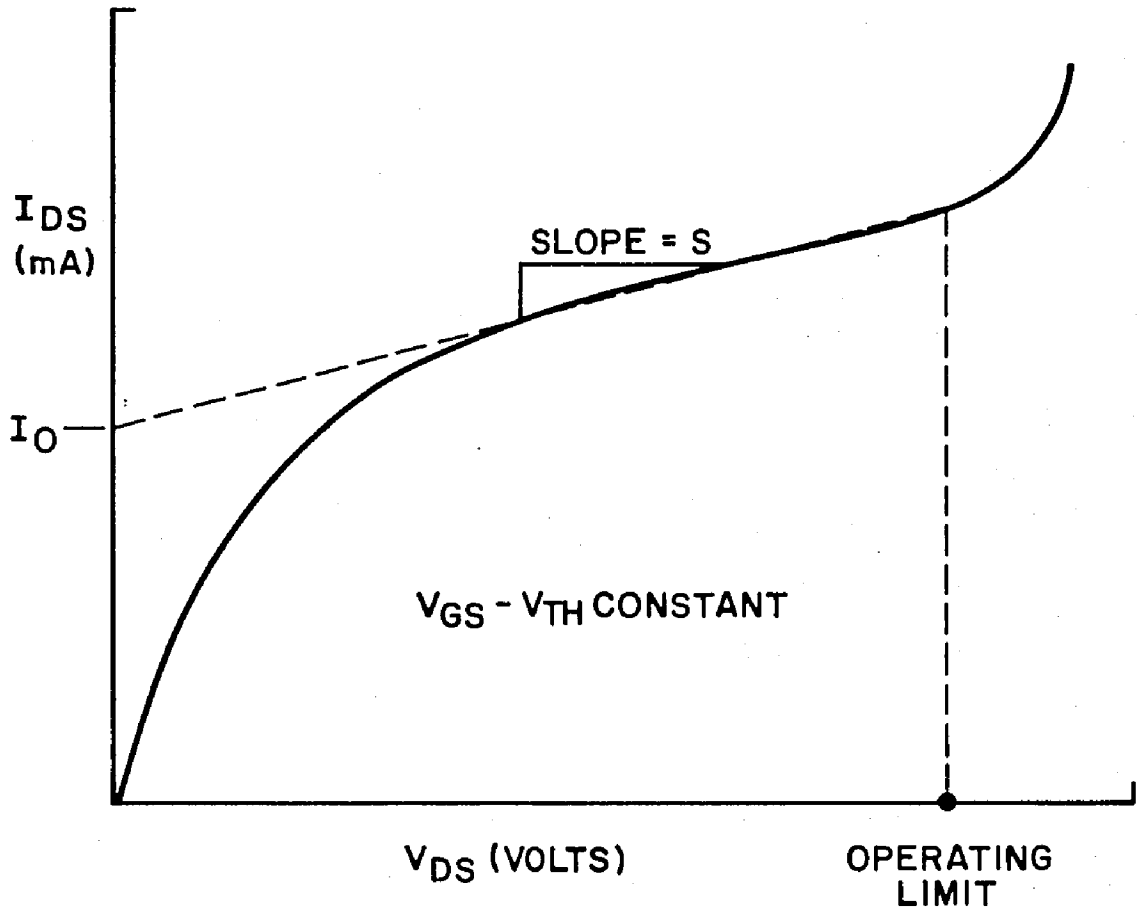
2 To eliminate sport data points two V_{GS}-V_{TH} curves were excluded from the model parameter extraction.

3 To eliminate sport data points three V_{GS}-V_{TH} curves were excluded from the model parameter extraction.



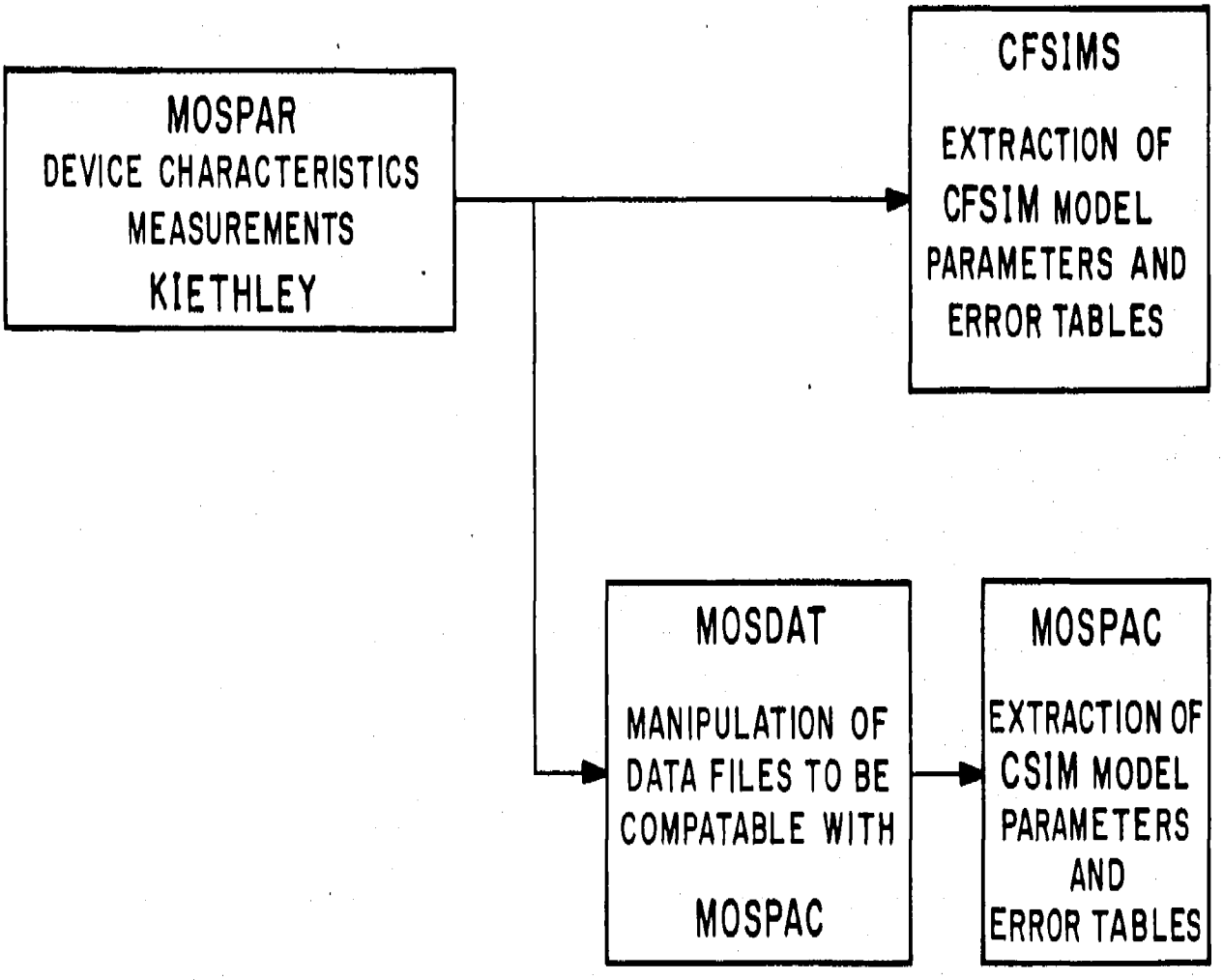
THRESHOLD CURRENT MEASUREMENT

FIGURE 1



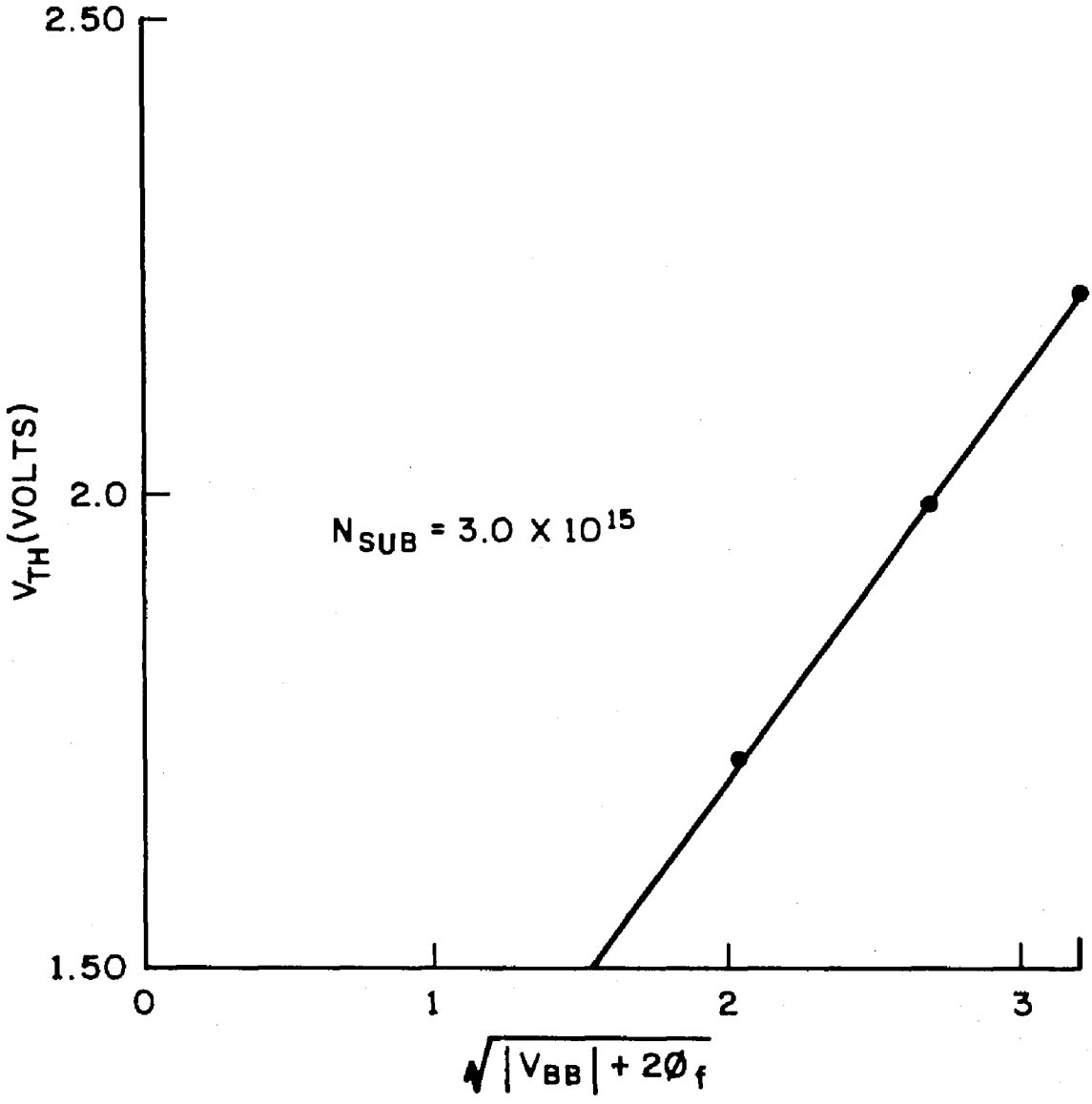
DRAIN CURRENT VS DRAIN VOLTAGE
FOR A CONSTANT $V_{GS}-V_{TH}$

FIGURE 2



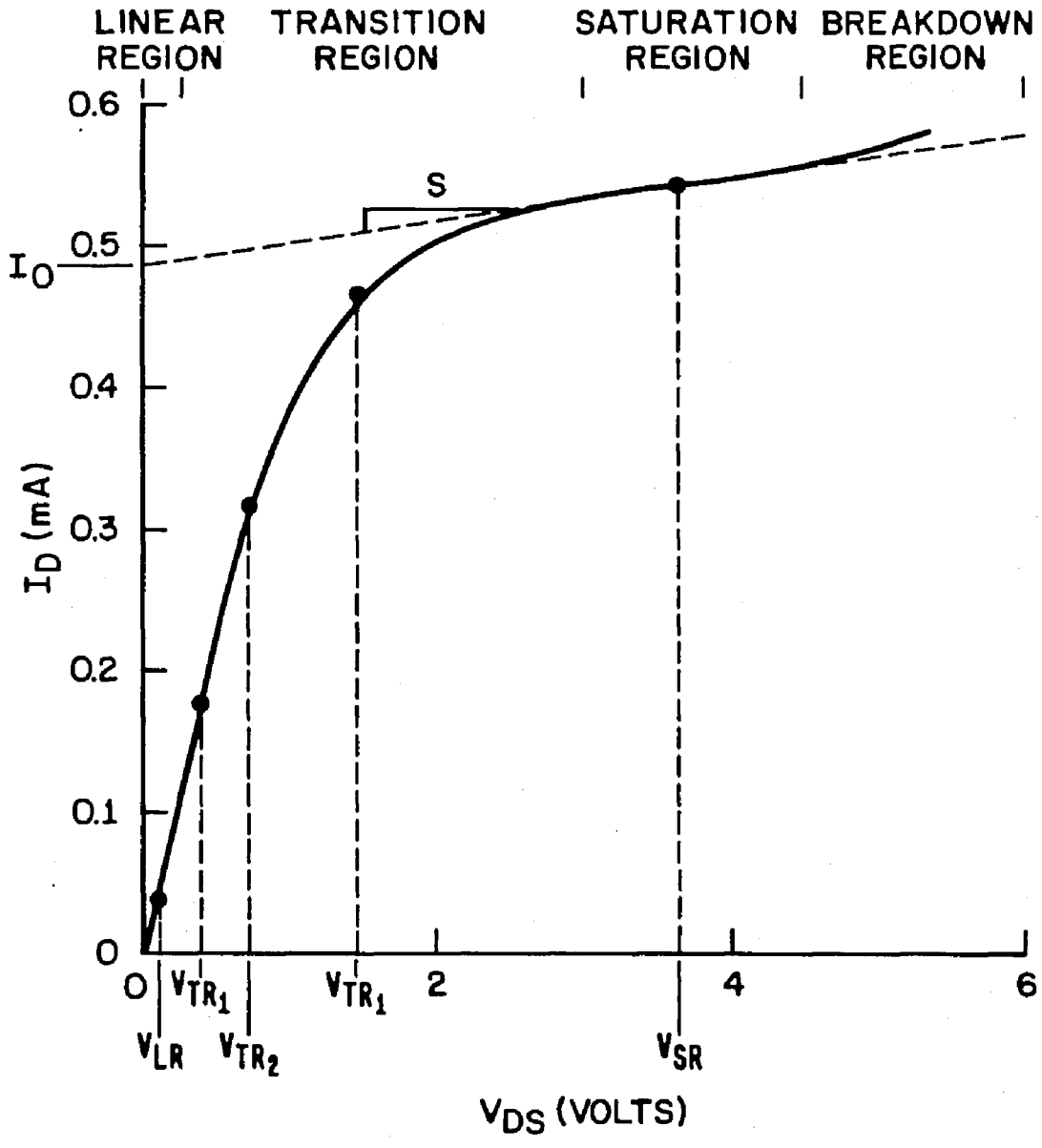
SCHEMATIC OF MODEL GENERATION PROCEDURE

FIGURE 3



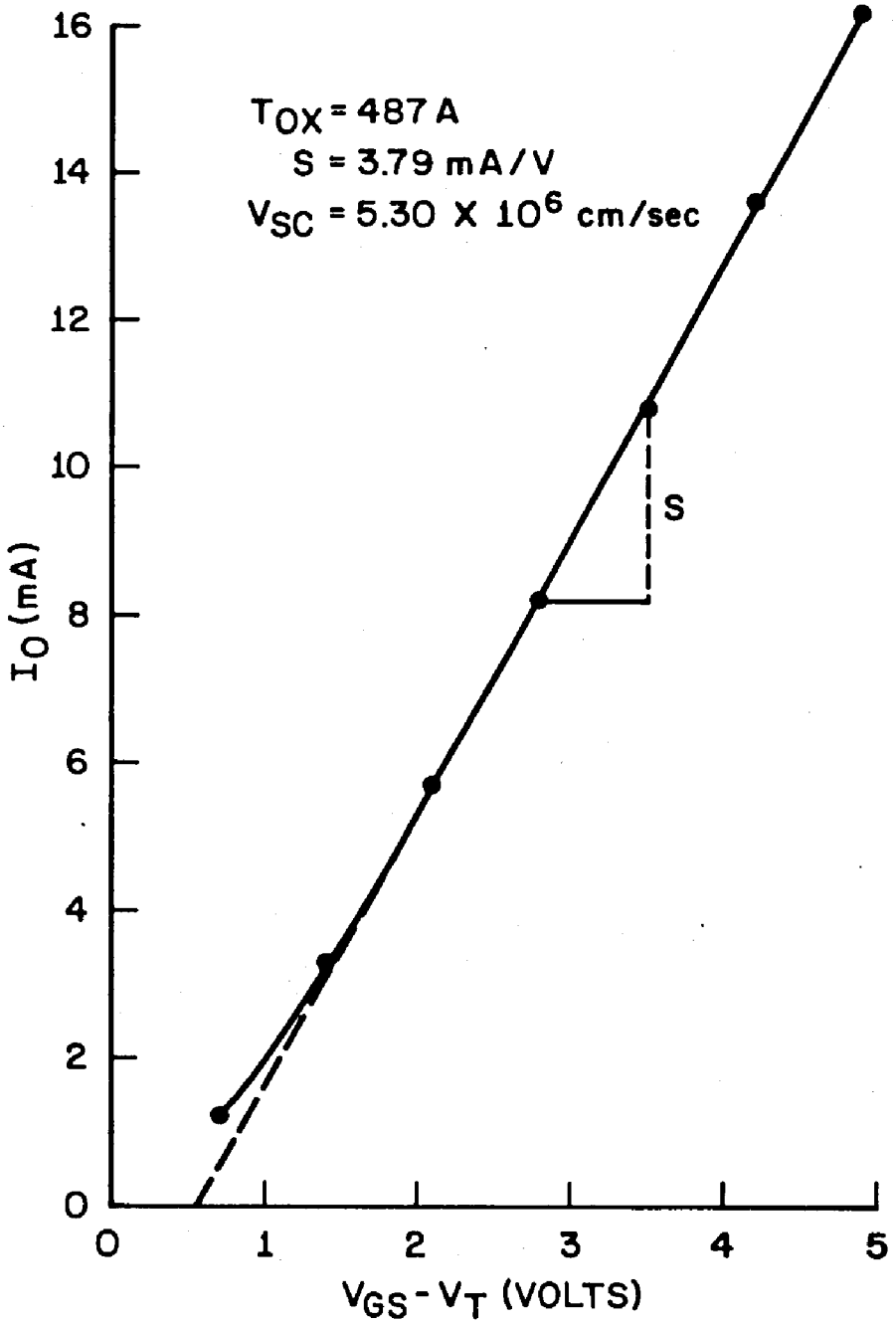
SUBSTRATE DOPING MEASUREMENT

FIGURE 4



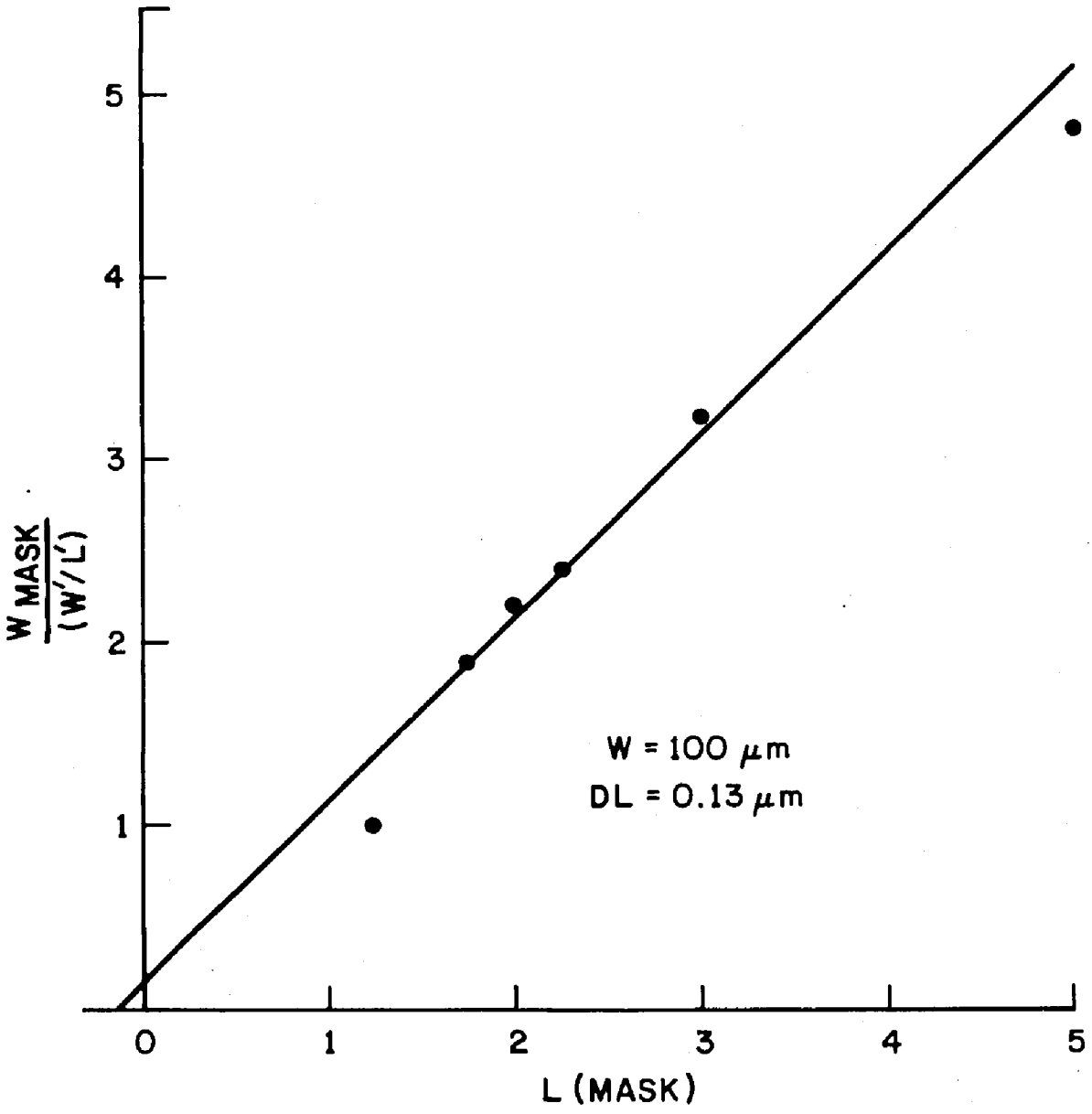
DRAIN CURRENT VS VOLTAGE CURVE

FIGURE 5



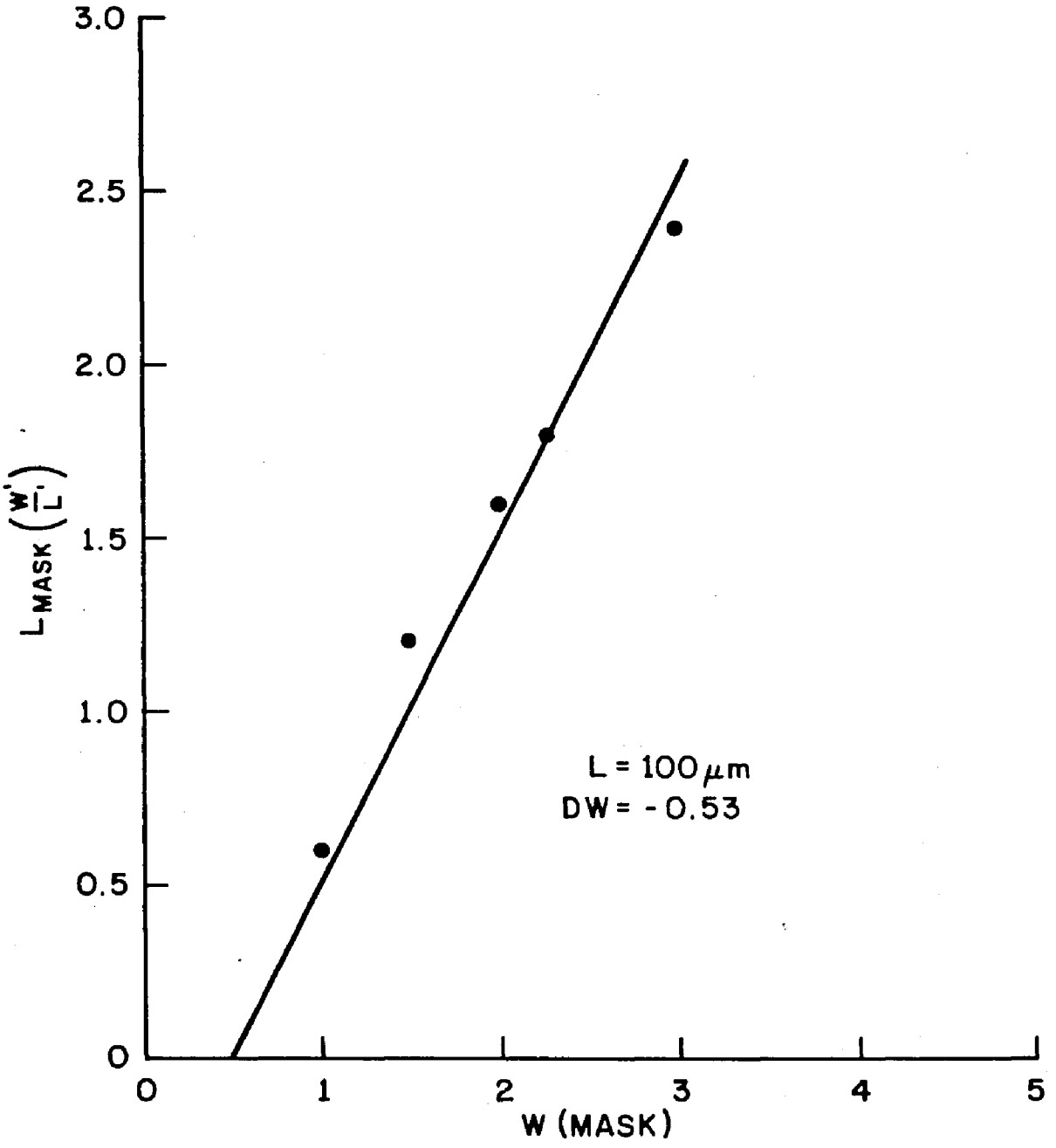
V_{SC} DETERMINATION

FIGURE 6



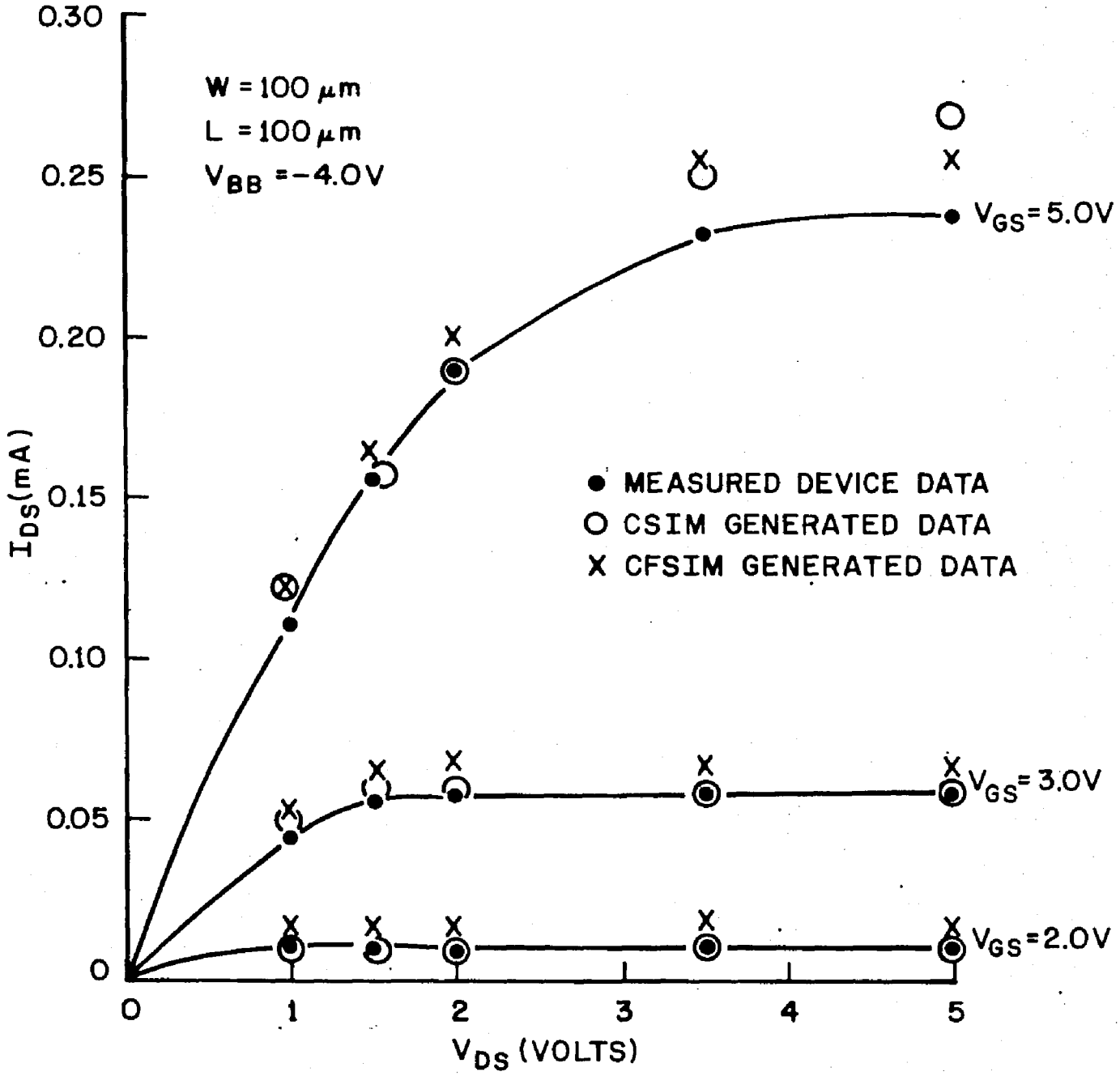
DL DETERMINATION

FIGURE 7



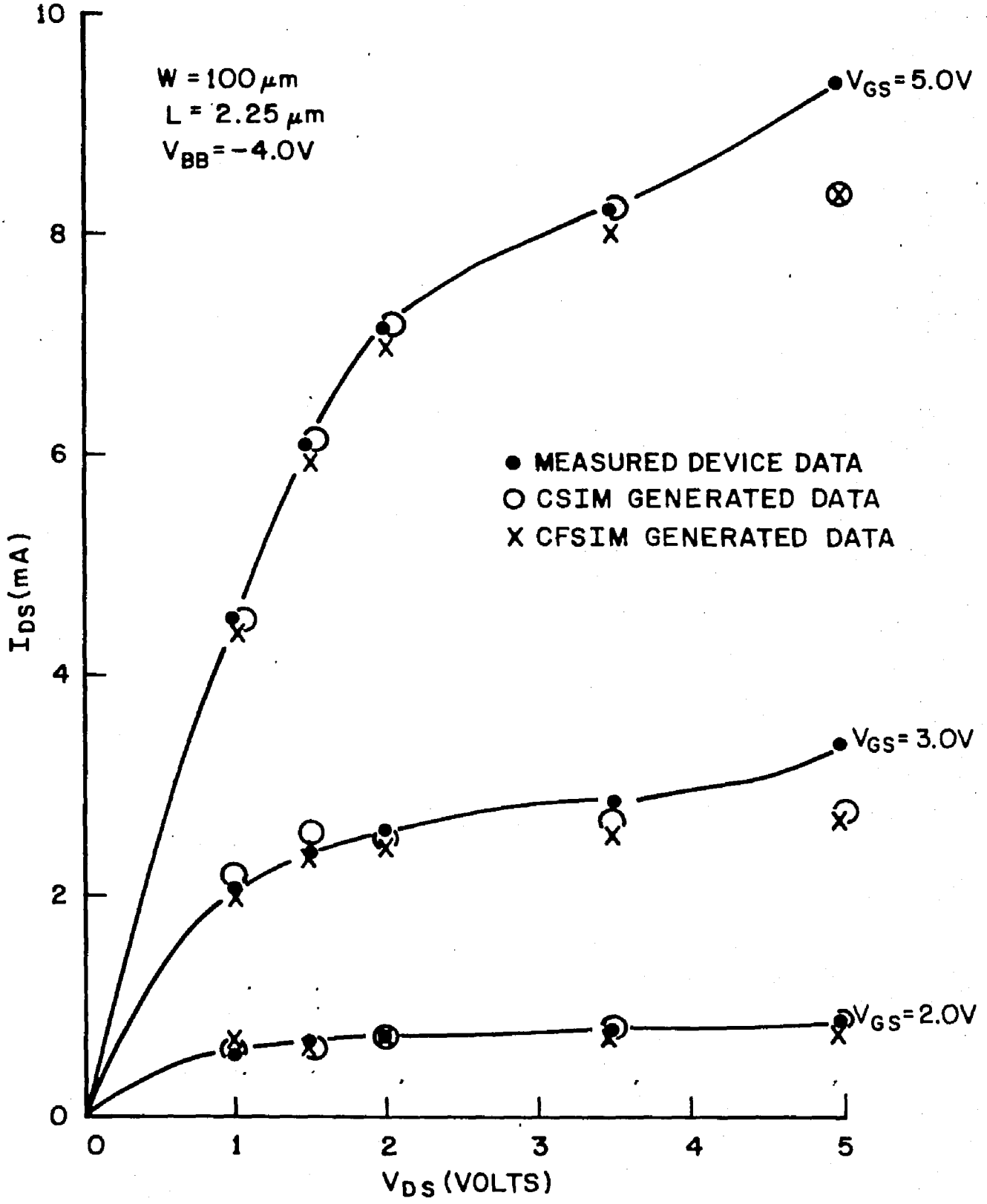
DW DETERMINATION

FIGURE 8



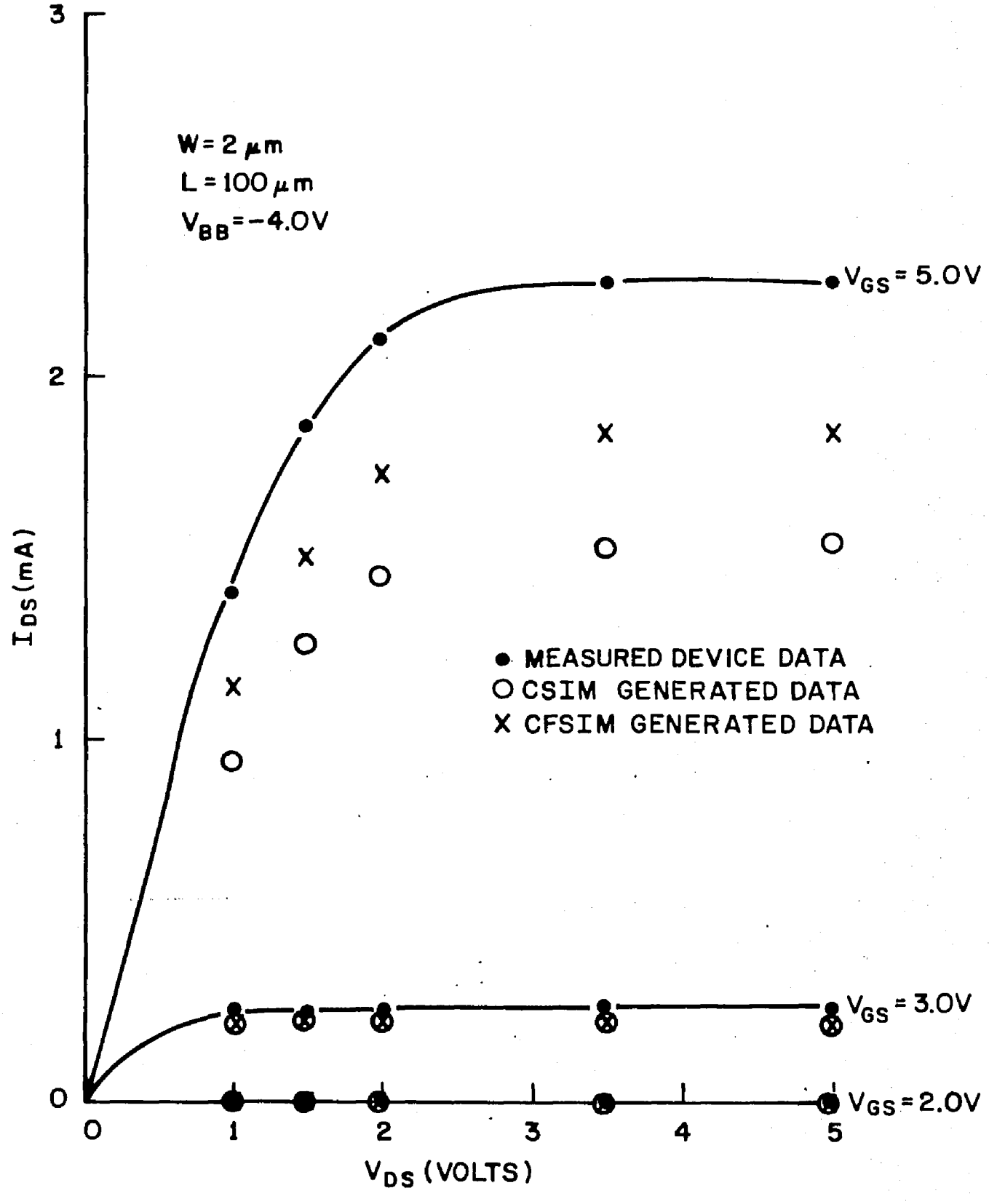
DRAIN-CURRENT CHARACTERISTICS
FOR A WIDE, LONG CHANNEL TRANSISTOR

FIGURE 9



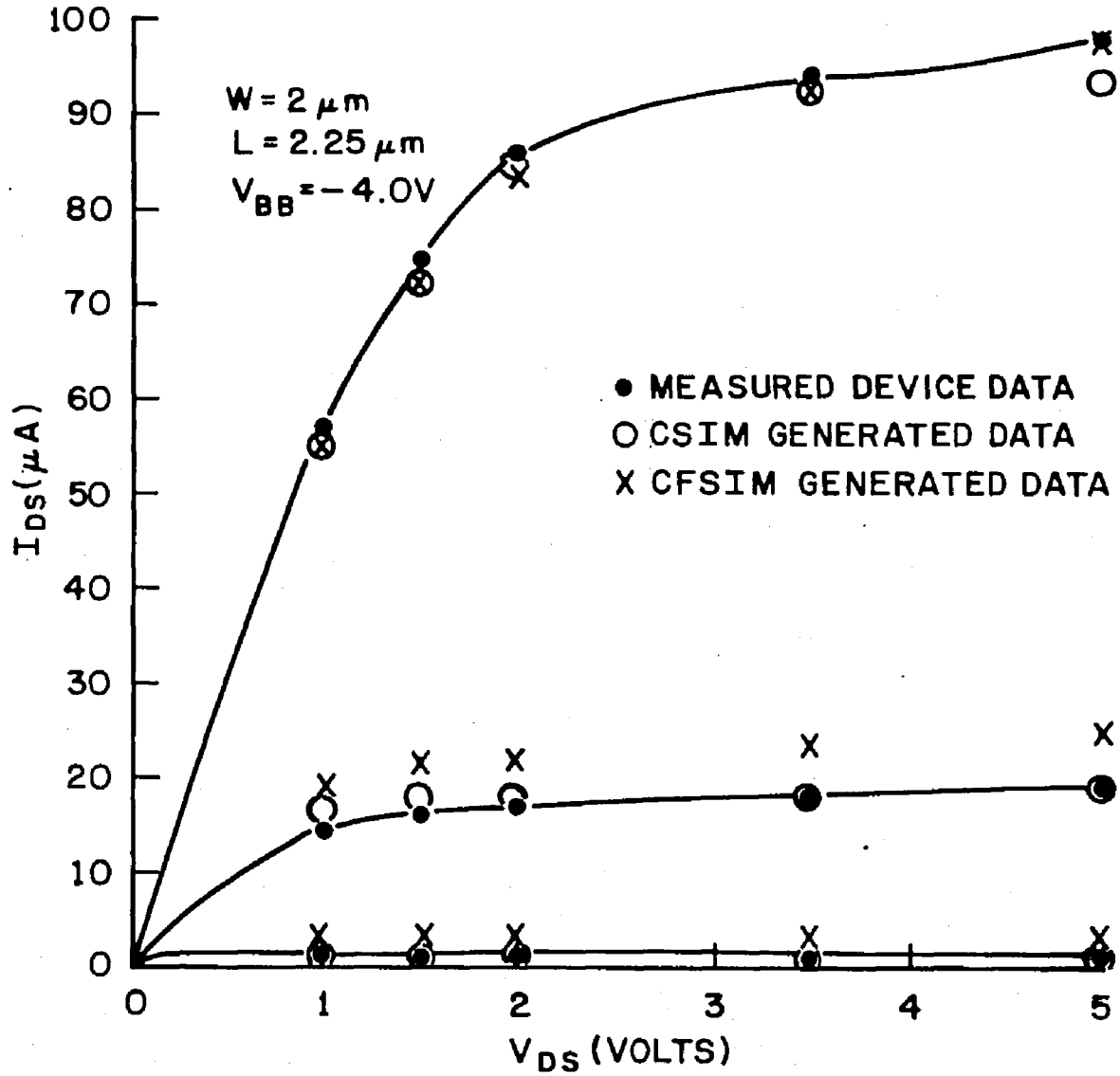
DRAIN-CURRENT CHARACTERISTICS
FOR A WIDE, SHORT CHANNEL TRANSISTOR

FIGURE 10



DRAIN-CURRENT CHARACTERISTICS
FOR A NARROW, LONG CHANNEL TRANSISTOR

FIGURE 11



DRAIN-CURRENT CHARACTERISTICS
FOR A NARROW, SHORT CHANNEL TRANSISTOR

FIGURE 12

JONATHAN EDWARD LACHMAN

Jonathan Edward Lachman was born to Lewis and Roberta on July 29, 1959, in Brooklyn, New York. He received his primary education within the New York City School System and graduated from Baldwin Senior High School, Baldwin, New York, with honors in June of 1976.

While attending the State University of New York at Stony Brook Jonathan was inducted into Tau Beta Pi, and graduated with honors with a Bachelors Degree in Electrical Engineering in May of 1980.

Jonathan has been working on a Masters Degree at Lehigh University while employed by Bell Laboratories. He has recently joined the employment of Western Electric Allentown.