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An RF phase measurement subsystem for CW-Lidar.

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AN RF PHASE MEASUREMENT SUBSYSTEM FOR CW-LIDAR

by

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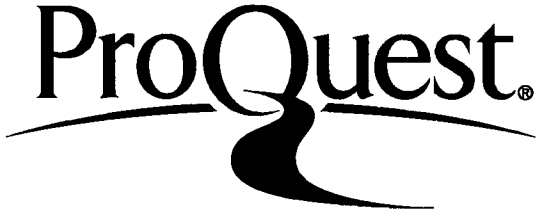

CERTIFICATE OF APPROVAL

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

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Abstract

A fast and accurate 420 Khz phase measuring circuit has been developed and is documented. The circuit is part of a laser based continuous wave modulated optical distance measuring system (CW-Lidar). Using a crosscorrelation scheme, the circuit extracts the phase angle information from a 420 Khz sine wave obscured by noise. To minimize integration time, the undesired high frequency components resulting from the crosscorrelation operation are eliminated by harmonic cancellation instead of low pass filtering. The circuit then converts the phase angle information to target distance based on the wavelength of the modulating signal. The target distance is displayed digitally.

The relations between the signal to noise ratio of the noisy received signal, the accuracy of the resulting distance measurement, and the integration time involved are derived and discussed. System error is evaluated. Methods to improve system performance are investigated.

1. Introduction

A light detection and ranging system (Lidar) using amplitude modulation of the light carrier can make distance measurements to a target in the same manner as conventional radar. For certain applications it is better to give the carrier a continuous sinusoidal AM modulation rather than pulsing it. This results in a higher resolution of small distance changes. However, information about absolute distance is lost. Such a system, using light as the carrier, is most properly called a continuous wave Lidar (CW-Lidar).

A CW Lidar system, of which the phase detector, as described in this paper, is a part, has been constructed by Eberhardt and co-workers[1,2] and is outlined in Figure 1. The operation of the system is as follows. A helium-neon laser beam (A) is directed by a lens (B) through a $LiTaO_3$ crystal which is a part of a microwave resonant cavity (C). A sinusoidal signal of approximately 3.82 Ghz is generated by a microwave oscillator (P), amplified (Q), and applied to the cavity (C), resulting in the AM modulation of the laser beam intensity by the microwave signal. A fraction of the modulated light from this modulating cavity is then split from the main beam (D) to serve as the reference signal. The main beam is focussed into a collimator (F) which is adjusted to expand the beam and refocus it at the target (I).

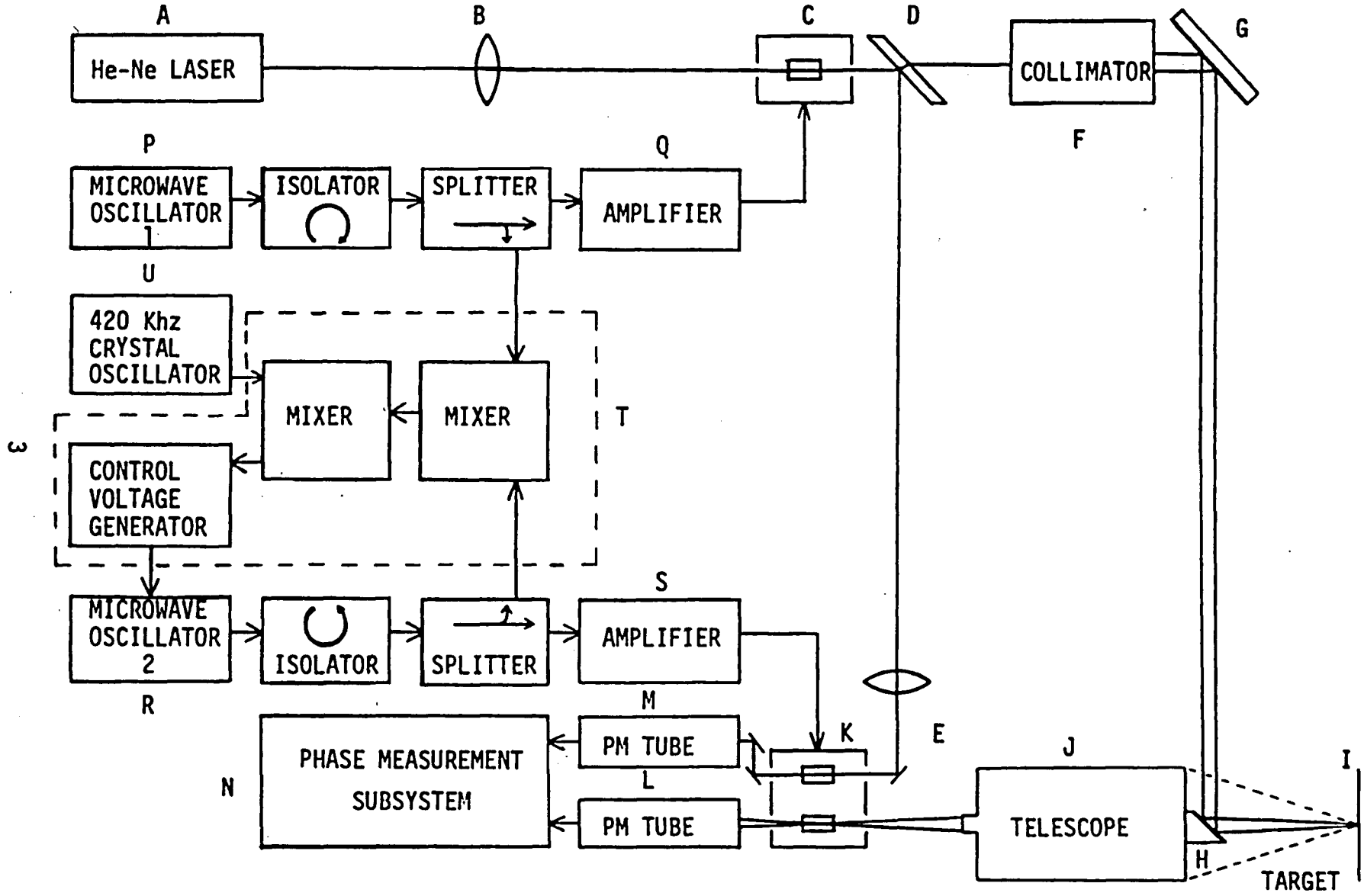


FIGURE 1 Diagram of the continuous wave Lidar system.

The expanded beam is guided by one mirror (G) to a second mirror (H) attached to a telescope (J) at the center of its objective lens. The beam is launched to the target from this second mirror. Light reflected from the target is gathered by the telescope and is focussed through a second $LiTaO_3$ crystal which is a part of a second microwave resonant cavity (K). A second microwave signal is generated by another oscillator (R), amplified (S), and applied to this second cavity (K). The difference frequency between the two microwave oscillators (P and R) is phase locked (T) to a 420 Khz crystal oscillator (U) so that the microwave frequencies remain exactly 420 Khz apart. Therefore, the resulting light signals emerging from this second crystal include a component at the 420 Khz difference frequency which has the same phase as the reflected microwave signal. This 420 Khz component is detected by a photomultiplier tube (L) and constitutes the received signal.

The fraction of light that was split off as a reference signal (D) is directed (E) through another $LiTaO_3$ crystal which is also a part of the demodulating cavity (K). The light signals emerging from this crystal include a component again at the 420 Khz difference frequency which has the same phase as the reference signal. This 420 Khz component is detected by a second photomultiplier tube (M) and constitutes the reference signal. A subsystem (N) accurately measures the phase difference between the received

and reference signals. This subsystem then converts that phase measurement to a corresponding distance measurement and displays the measurement to complete the Lidar system. The design and development of this subsystem is the subject of this paper. A functional block diagram of the subsystem appears in Figure 28.

2. System Overview

2.1 Optimum Phase Detection

To determine and ultimately display the relative target distance measured by the Lidar system, the phase difference between the reference and received sinusoidal intermediate frequency signals must be measured. Due to the presence of quantum noise in the received signal, as well as receiver noise, the detector chosen should be capable of optimally extracting the phase angle of the 420 Khz sinewave in the shortest possible time. It can be shown[3] that the optimum detector for such a condition is one in which the noisy received signal is simultaneously compared to reference sinusoids with all the possible phase angles. The reference sinusoid making the closest approximation to the received signal then indicates the received signal's phase angle.

One way to implement such a detector would be to crosscorrelate the received signal with a reference sinusoid of the same frequency. Crosscorrelation involves shifting one waveform in time with respect to a second waveform and provides a measure of the similarity between the two waveforms as a function of the time shift performed.[4] Since a time shift for a sinusoidal signal can be also interpreted as a phase shift, correlation in this case would provide a measure of the similarity between the received signal and the reference signal as a function of the phase shift between them, which is exactly what an optimum detector is required

to do.

For periodic signals, the expression for the crosscorrelation function is given by

$$\bar{X}_{12}(\tau) = \frac{1}{T} \int_{-T/2}^{T/2} f_1(t)\, f_2(t-\tau)\, dt ,$$

where $f_1(t)$ and $f_2(t)$ are the functions to be crosscorrelated and T is the period of $f_1(t)$ and $f_2(t)$. To find the crosscorrelation function between the received and reference signals, the expressions for the received and reference signals must be substituted into the above equation for evaluation. The reference signal is written in the form $b \cos(\omega t+\gamma)$. The received signal is of the form $a \cos(\omega t+\theta) + n(t)$, where $n(t)$ represents a noise component. By replacing the reference signal's phase angle γ by $(\theta-\phi)$, the single variable ϕ now represents the phase difference between the two signals, which is the ultimate information to be obtained. Replacing ϕ by $\omega\tau$ transforms the phase difference ϕ to a proportional time delay τ, required by the crosscorrelation process. By substituting the expressions $a \cos(\omega t+\phi) + n(t)$ and $b \cos(\omega(t-\tau)+\phi)$ for $f_1(t)$ and $f_2(t)$ and evaluating the integral (as performed in the appendix), the function $\frac{ab}{2} \cos\phi$ is obtained as the crosscorrelation function. This function does indeed provide a measure of the phase angle between the two signals, and can be further processed to evaluate ϕ.

2.2 Crosscorrelating Detector Schemes

Upon implementing a detector using just the above crosscorrelation function, the following difficulties arise. First, the inverse cosine function required to recover ϕ has a periodicity in only 180°. Hence, there will be ambiguities over half of the possible 360° interval available from the crosscorrelation process. Also, another type of ambiguity results for a crosscorrelation function value of zero. This can indicate either a 90° phase difference or no correlation at all, which would be the case if the received signal disappeared. To overcome these ambiguities, a second signal can be derived by crosscorrelating the received signal with a quadrature version of the reference signal. The resulting function would be proportional to $\sin\phi$. These two output signals will allow a full 360° resolution of the angle ϕ.

Another difficulty lies in the fact that the amplitude of the received signal, a, can vary, depending on the reflectivity of the target. These amplitude variations will affect the value of the crosscorrelation function just as changes in ϕ do. Therefore, amplitude variations must somehow be distinguished from phase changes so that errors do not result when computing ϕ from the function value.

Figure 2 shows a block diagram of a phase detector using crosscorrelation to produce two outputs proportional to $\sin\phi$ and $\cos\phi$.

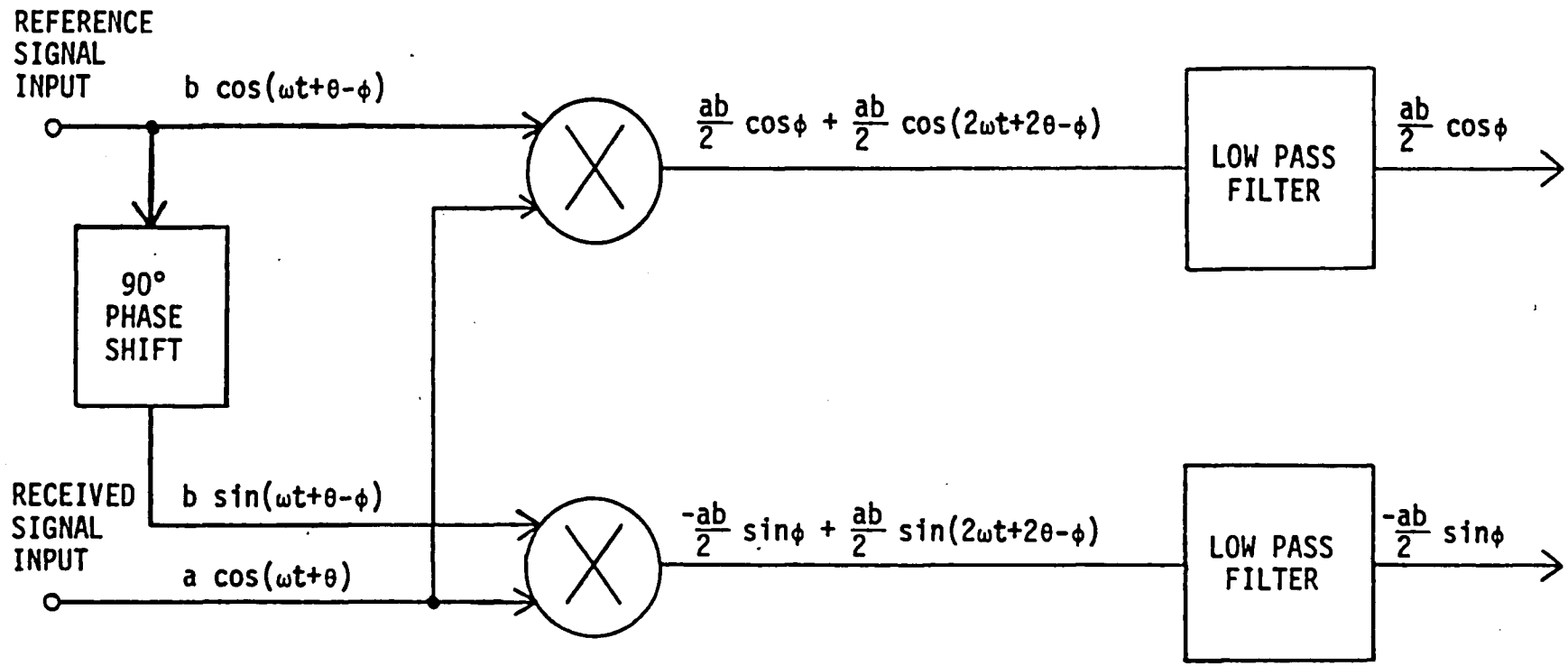


FIGURE 2 Simple phase detector using crosscorrelation and low pass filters.

This phase detector first generates a quadrature version of the reference signal by introducing a 90° phase shift in that signal. The incoming received signal is then multiplied separately by both the original reference signal and the quadrature reference signal. The low pass filters eliminate the $2\omega t$ terms and the final outputs are then the two desired functions proportional to $\sin\phi$ and $\cos\phi$.

This scheme can be modified as shown in Figure 3 to replace the low pass filters by harmonic cancellation of the $2\omega t$ terms. This scheme requires one additional signal, a quadrature version of the received signal, two additional multiplications, and two summations. Four products are formed by multiplying together each possible combination of a reference signal and a received signal. By summing the two products containing the $\frac{ab}{2}\cos\phi$ term and subtracting the two products containing the $\frac{ab}{2}\sin\phi$ term the higher frequency components at 2ω add to zero in both cases, leaving only the signals proportional to $\sin\phi$ and $\cos\phi$. This harmonic cancellation process gives the same result as low pass filtering the 2ω frequency component. In this second scheme, low pass filtering still is optional. It would improve the mean square deviation of the angle reading but would increase the time necessary for one measurement.

In either approach, further averaging of the $ab\cos\phi$ and $ab\sin\phi$ information over an interval can be handled in a digital

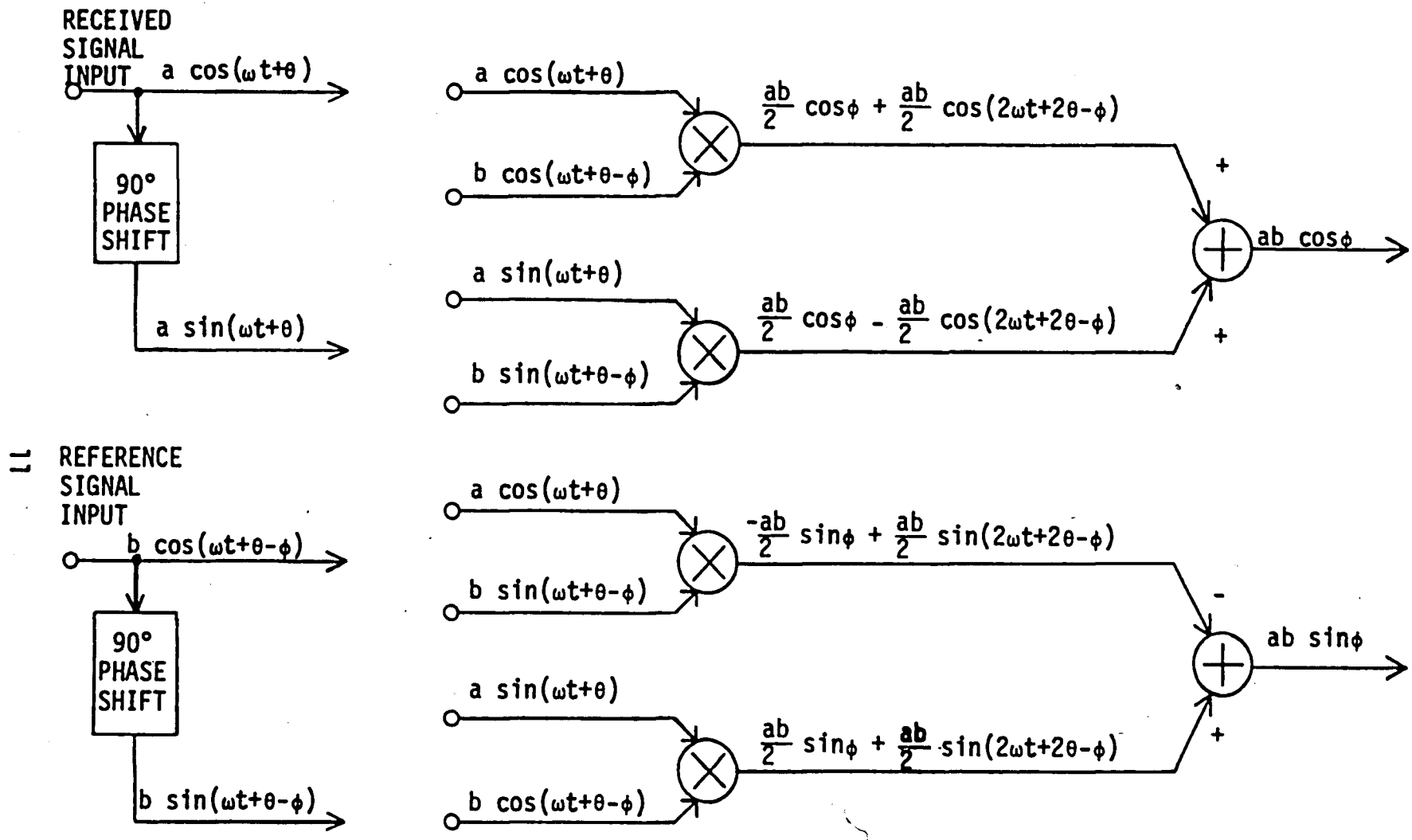


FIGURE 3 Phase detector using crosscorrelation and harmonic cancellation.

manner. In both approaches a step change in ϕ results in a transient. In the first scheme the transient occurs at the low pass filters. In the second scheme the transient occurs at the 90° phase shifter. At this time, no conclusions have been drawn as to which approach would handle such a step change in ϕ in the best manner. The harmonic cancellation approach was the approach chosen to construct the detector.

2.3 Elimination of Initial Amplitude Dependences

The next step in the phase measurement operation is to retrieve the phase angle ϕ from the sine and cosine information provided by the crosscorrelation. However, before implementing the inverse sine and cosine functions, the dependence of the crosscorrelation functions on the amplitude, a, of the received signal should be eliminated. Changes in a or b could be falsely interpreted as a change in ϕ. Since both of the correlation signals proportional to $\cos\phi$ and $\sin\phi$ have the same amplitude, forming a ratio of the two signals will eliminate the dependences on a and b. This operation will create a new trigonometric function, either the tangent or the cotangent of the angle ϕ depending on how the ratio is formed.

Although forming a ratio solves the problem associated with initial amplitudes, it creates a new problem when implementing the

new inverse function. The old functions, sine and cosine, have ranges from minus one to plus one inclusive. The tangent and cotangent functions each have ranges which span from minus infinity to plus infinity, an interval which will be much harder to work with. However, since the tangent and cotangent functions are reciprocals of each other, one of the two always lies between minus one and plus one inclusive. Therefore, if both functions are formed simultaneously by doing two separate divisions, one quotient will always be in that convenient minus one to plus one range, and that quotient can be used to determine ϕ. Note also that when one quotient is ± 1, the other must also be ± 1 so that at and only at the very endpoints of the minus one to plus one range either quotient could be used to determine ϕ.

A block diagram for the implementation of these divisions is shown in Figure 4. Since a simple analog divider will not remain stable when allowed to operate over all four quadrants, the divisions will be limited to two quadrants by taking the absolute value of the denominator signal before dividing. This will insure two quadrant operations because the denominator can never be negative. Therefore, strictly speaking, the functions formed by the two divisions are really $\frac{\sin\phi}{|\cos\phi|}$ and $\frac{\cos\phi}{|\sin\phi|}$. Graphs of these two functions also appear in Figure 4. From these curves it can be seen that both of these functions are periodic in 360° intervals

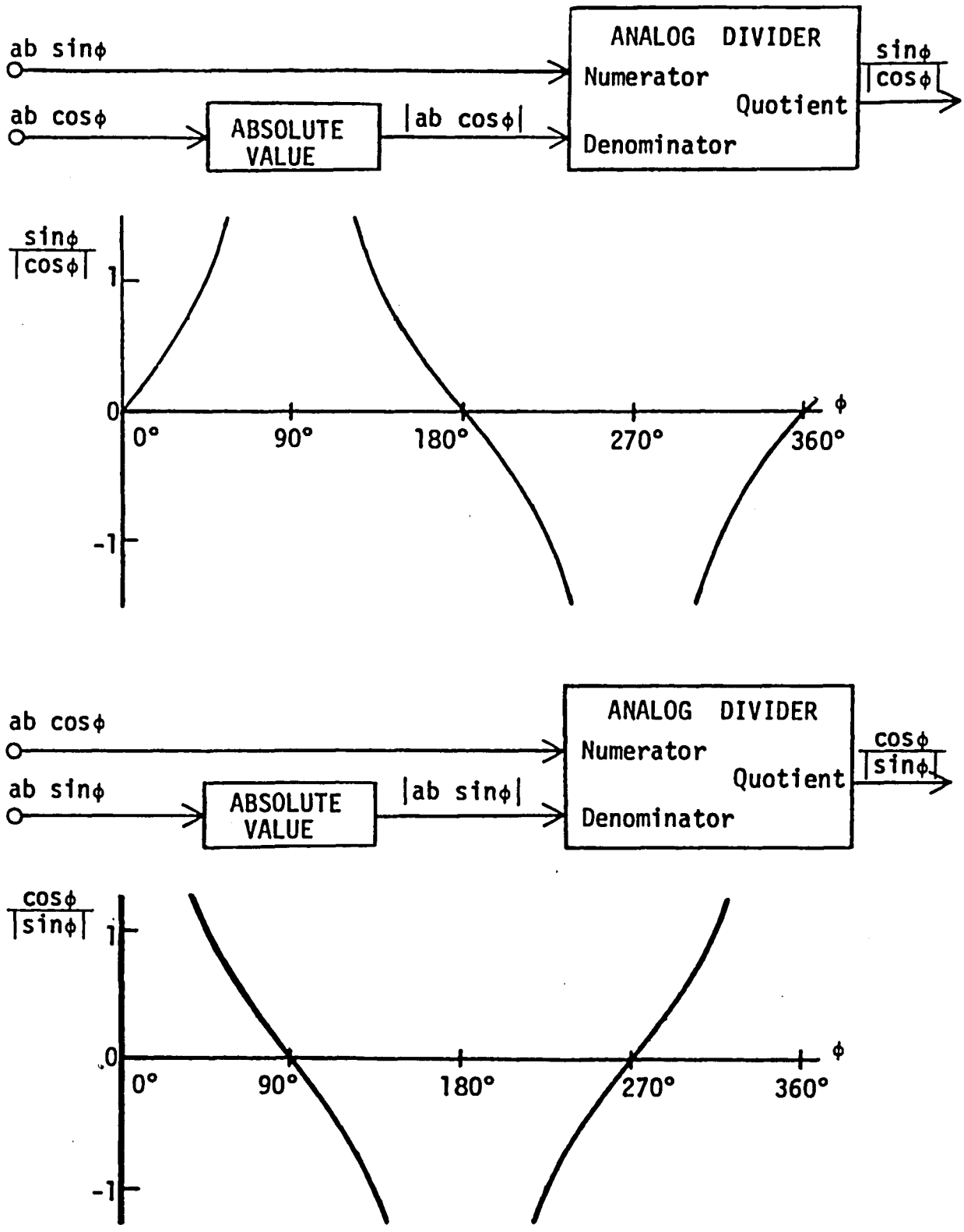


FIGURE 4 Analog divisions to remove initial amplitude dependences and the resulting functions.

and that one of the functions is always in the range minus one to plus one.

An analog circuit that generates as output the absolute value of its input signal is essentially a full wave rectifier. The accuracy of such a circuit usually becomes quite poor for input signal levels around zero due to nonlinearities when crossing from minus to plus and vice versa. In light of this fact, the above mentioned divisions should be examined to determine when their quotients may be affected by such errors. From Figure 4, it can be seen that ϕ is determined using the quotient $\frac{\cos\phi}{|\sin\phi|}$ over the intervals 45° to 135° and 225° to 315°. In these two intervals, the value of $\sin\phi$ is always in the range .707 to 1.000 or -.707 to -1.000 and does not go through or even approach zero. So, in these two intervals there should be no inaccuracies resulting from taking the absolute value of $\sin\phi$ as the denominator function. Over the remaining two intervals, ϕ is determined using the quotient $\frac{\sin\phi}{|\cos\phi|}$. In these two intervals the value of $\cos\phi$ is always in the range .707 to 1.000 or -.707 to -1.000 and does not go through or approach zero. So, in these remaining intervals there should also be no inaccuracies resulting from taking the absolute value of $\cos\phi$ as the denominator function. Thus, the use of absolute value circuits will not affect the accuracy of measuring any angle ϕ.

2.4 Sampling

The two signals $\frac{\sin\phi}{|\cos\phi|}$ and $\frac{\cos\phi}{|\sin\phi|}$ will have to be sampled for conversion to digital form for further processing as shown in Figure 5. Each signal is converted independently by its own sample and hold amplifier and 12 bit analog to digital convertor. The sample and hold amplifier output follows the analog signal input until the amplifier receives a sample and hold command. At this time, the output freezes at its current value, essentially sampling the input signal, and remains constant so that the analog to digital convertor can digitize the sample. Once the sample is converted to digital information, the sample and hold amplifier output again follows the input signal until another command is received.

The sampling rate will be limited primarily by the conversion time of the analog to digital convertors. With reasonable effort it is difficult to accurately sample and convert with 12 bit resolution in a time shorter than 25 microseconds. This conversion time is roughly ten times longer than 2.38μs, one period of 420 Khz. Hence, at least 10 periods of 420 Khz will occur between sample times. It is quite important to properly relate the sampling rate to this 2.38μs period of 420 Khz because the signals being sampled will contain spurious amounts of the 420 Khz signal and its harmonies resulting from inaccuracies in the previous

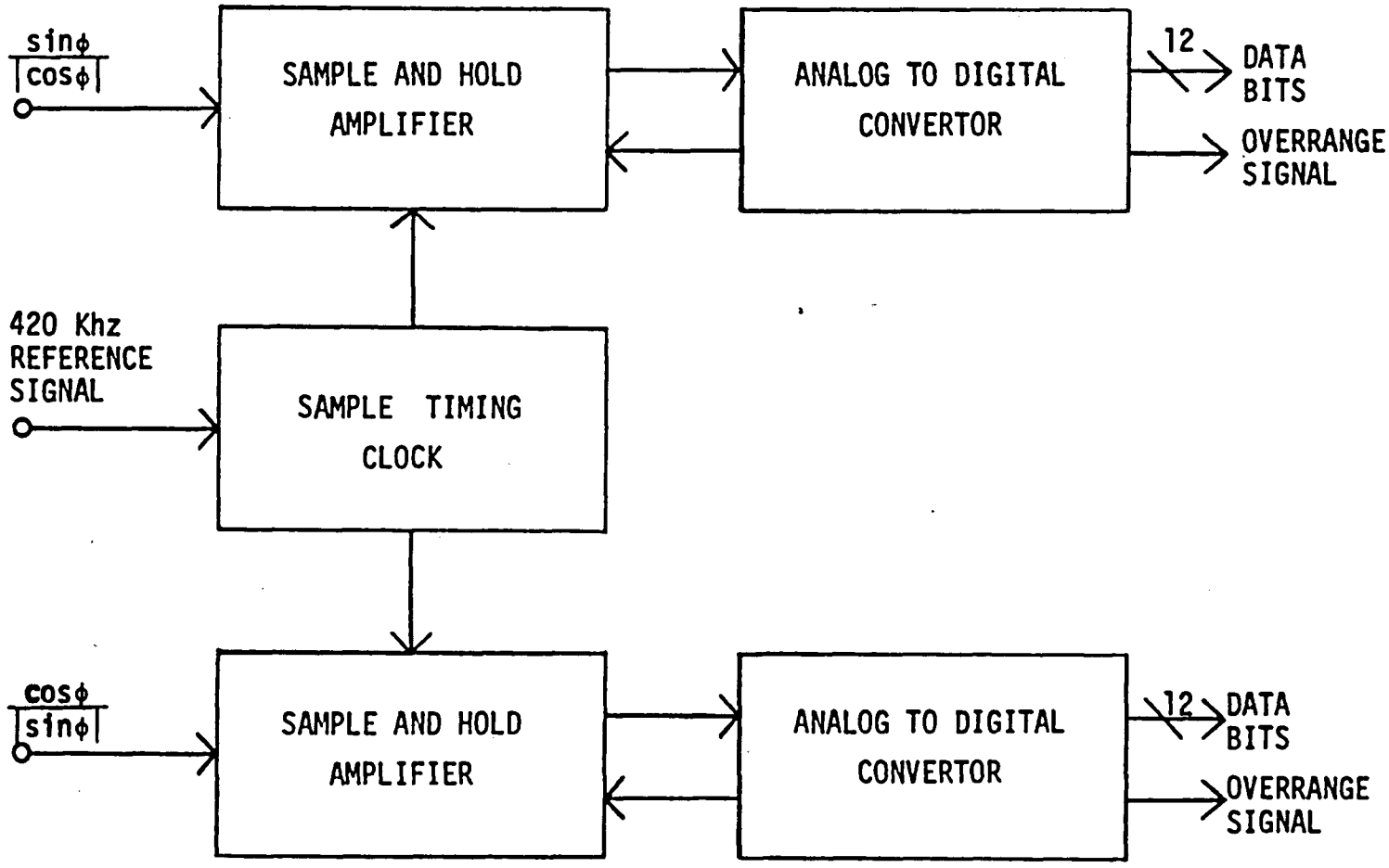


FIGURE 5 Sampling and digitizing $\frac{\sin\phi}{|\cos\phi|}$ and $\frac{\cos\phi}{|\sin\phi|}$.

multiplications and summations. If there are no integral relations between the sampling rate and 420 Khz, a periodic variation in the distance reading will result.

The following scheme was devised to generate a sampling rate which is both related to the spurious 420 Khz period and allows for adequate conversion time. With timing derived from the 420 Khz reference, a sampling clock generates a sample and hold command every 15 $\frac{15}{16}$ periods of that 420 Khz reference or every 37.95μs. Therefore, with respect to the 420 Khz period, samples are taken at 16 evenly spaced instances throughout the period, as shown in Figure 6. Each new sample is taken $\frac{1}{16}$ of a period sooner than the previous sample was taken. Thus, the sample times for every group of 16 consecutive samples span exactly 1 period of 420 Khz. By accumulating the samples in groups of 16 for averaging, any contributions in the sample values due to spurious 420 Khz signals will sum to zero because the average value of a sinusoid when effectively sampled over one or more periods is zero. As also shown in Figure 6, every group of 16 consecutive samples span exactly 2 periods of 840 Khz. Therefore, the accumulating of 16 samples for averaging will also eliminate any contributions to the samples from 840 Khz spurious signals.

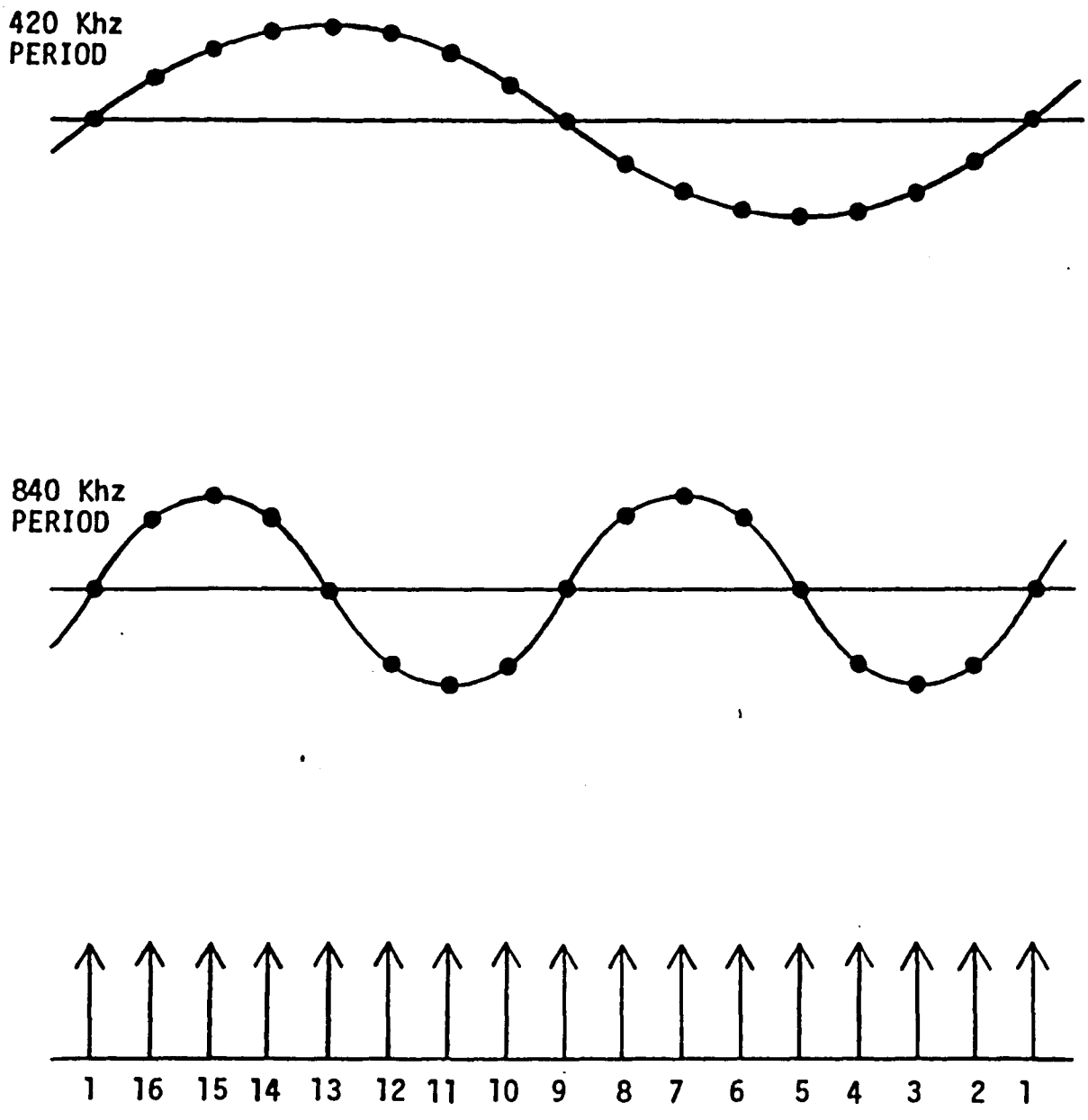


FIGURE 6 The sample times of a group of 16 samples with respect to the 420 Khz and 840 Khz periods. Sample 1 is arbitrarily referenced to the zero crossing for illustration purposes.

2.5 Angle Computation and Distance Display

The remaining operations required to interpret the phase angle, average the samples, and display a relative distance measurement are outlined in Figure 7. The two analog to digital convertors provide a 12 bit digital representation of each of the sampled signals $\frac{\sin\phi}{|\cos\phi|}$ and $\frac{\cos\phi}{|\sin\phi|}$. Since the sampled signals can be both positive and negative, the convertors are configured in a bipolar mode. For this reason, the most significant bit from the convertors can be interpreted as a sign bit. Also, for sample values exceeding the input range of the convertors, overrange signals are generated to indicate the validity of the convertors' output data.

One of the two digitized signals is selected by a two to one selector based on the conditions of the overrange signals. The selected function output is used as an address for a PROM lookup table, in which is stored the inverse trigonometric function to determine ϕ. Data from the lookup table represent the phase angle whose function appears as the address. It is only necessary to store a principal branch of the function, from -45° to +45°, because the additional quadrant information can be determined from the sign bits and the selected function. Based on these three signals, arithmetic logic units add or subtract the proper constant to the angle, to place it into the correct quadrant. The final

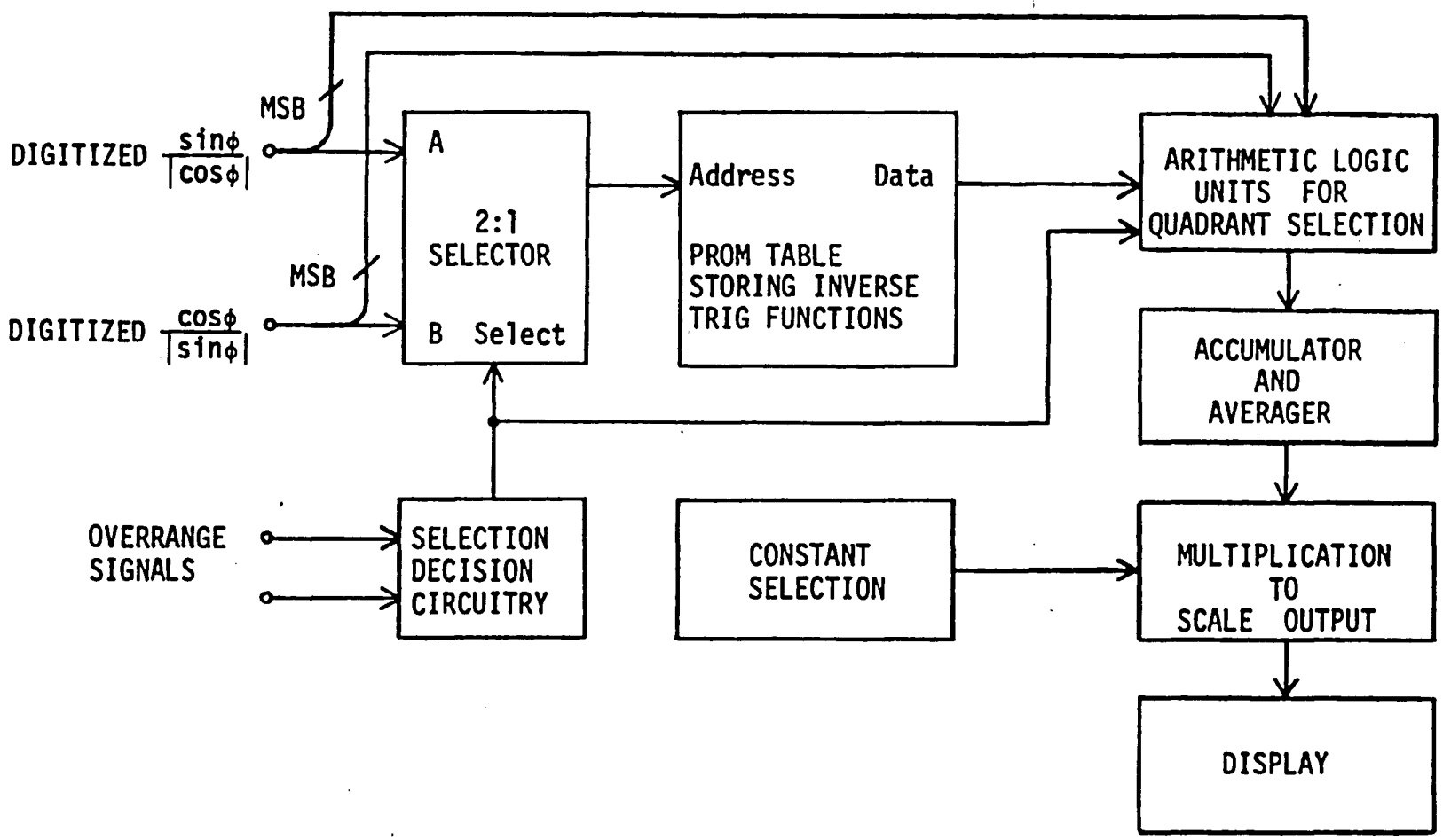


FIGURE 7 Block diagram of the remaining operations required to display a distance measurement.

fully decoded angle value is then summed into an accumulator to await averaging.

When the 16 samples to be averaged have been converted and accumulated, the resulting sum in the accumulator is divided by 16 to provide the averaged value of the phase difference ϕ. This value is then scaled to the actual distance by digital multiplication with a selectable constant determined in the following way. Due to the reflection from the target, the phase of the received signal changes 360° for every change in target distance of one half the wavelength of the microwave modulating frequency. Therefore, the scaling constant required to convert an angle measure to distance measure is given by the expression $\frac{.5\lambda}{360^\circ}$ or $\frac{\lambda}{720^\circ}$, where λ is the wavelength of the microwave modulating frequency. If λ is specified in millimeters, the distance measure will be in millimeters. The final product of this multiplication is then displayed on an LED readout as a distance measurement.

3. Crosscorrelating Phase Detector Construction

3.1 Preamplifiers

A crosscorrelating phase detector for the phase measurement system has been constructed using the harmonic cancellation scheme. The detector uses Analog Devices Model AD429B wideband

analog multipliers and National Model LH0024 operational amplifiers to implement the required analog operations as outlined in Figure 8. The reference and received signals are each buffered and amplified if necessary by a wideband preamplifier composed of an LH0024 operational amplifier. A schematic of the preamplifier appears in Figure 9. The preamplifier can provide up to 40 dB of gain over a 7Mhz bandwidth with the frequency compensation network shown. An offset adjustment is provided to null the output voltage to zero for zero input. A test point on the output is provided for alignment. Finally, the power supply inputs are bypassed to ground with filter capacitors.

The preamplifiers boost the amplitudes of the received and reference input signals to 10 volts peak before further processing. This peak value was chosen to utilize the full dynamic range available from the analog multipliers.

After construction, the preamplifiers were tested to experimentally measure their gains and phase delays at 420 Khz. A maximum gain of 38.5 dB and a phase delay of 17.0° were measured for the reference signal preamplifier. A maximum gain of 38.4 dB and a phase delay of 20.4° were measured for the received signal preamplifier. The phase delays appear to be troublesome because they will produce an additional 3.4° phase difference between the

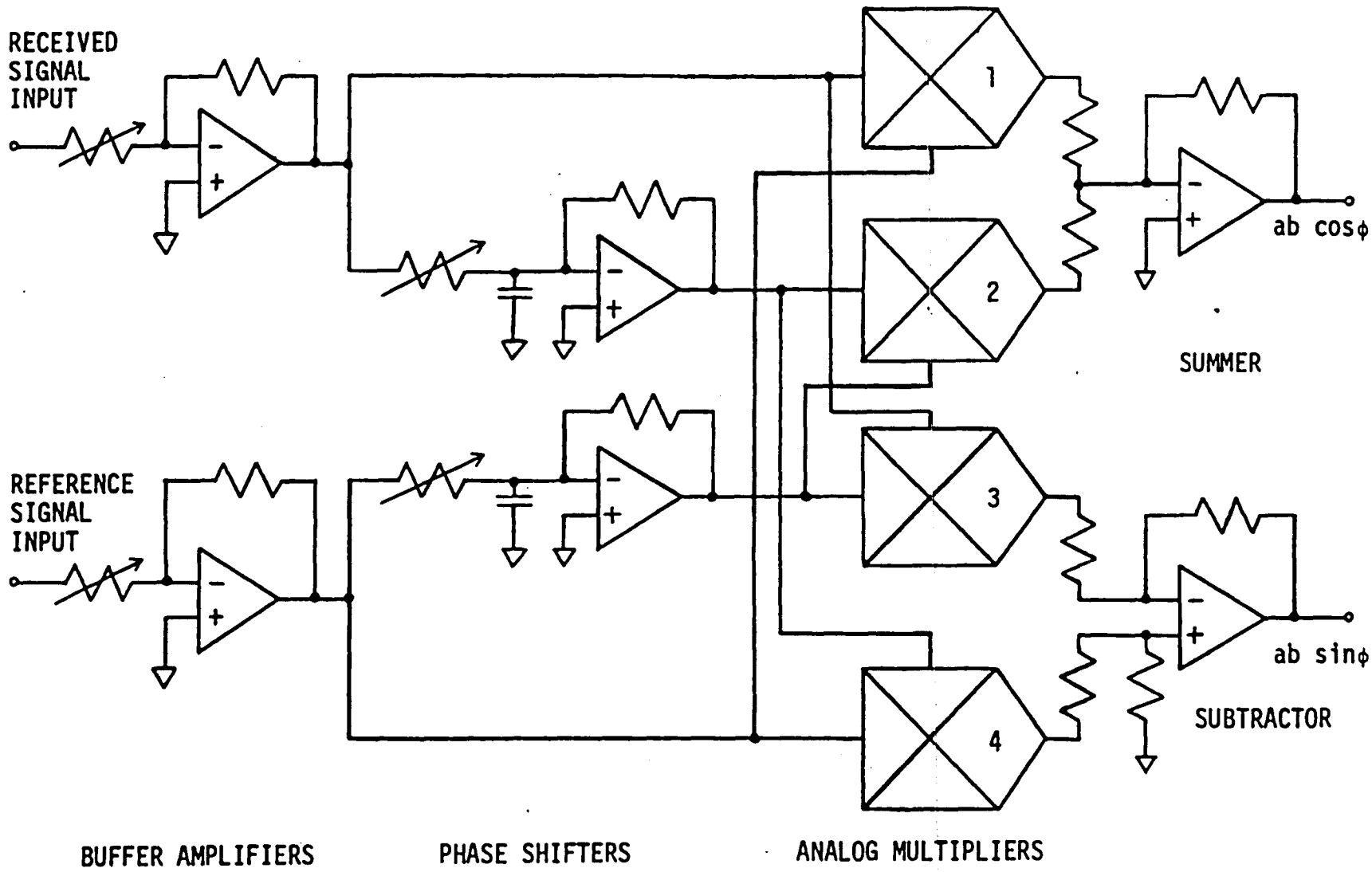
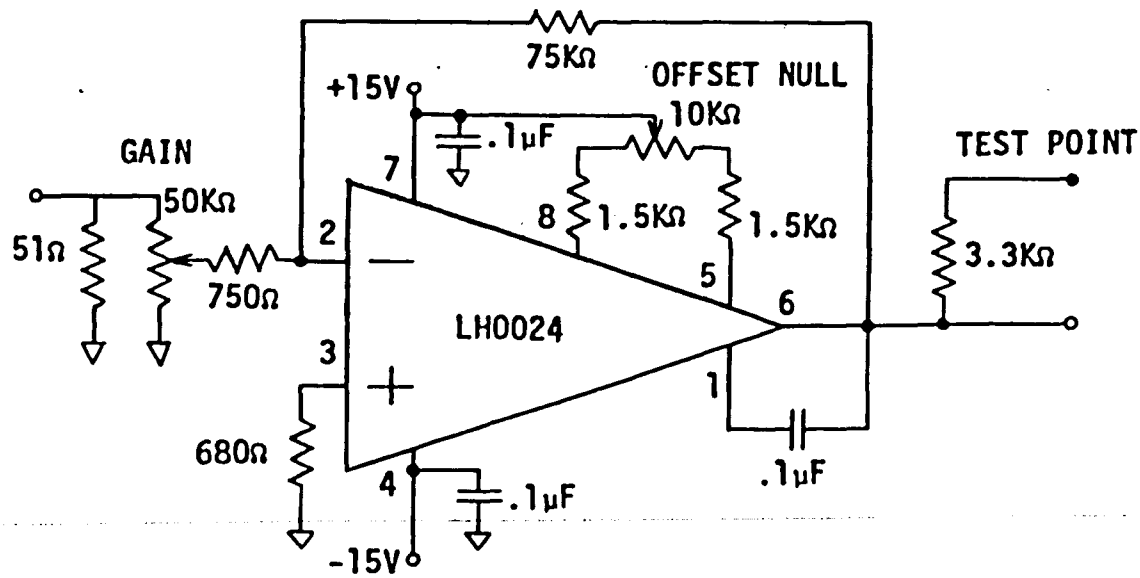
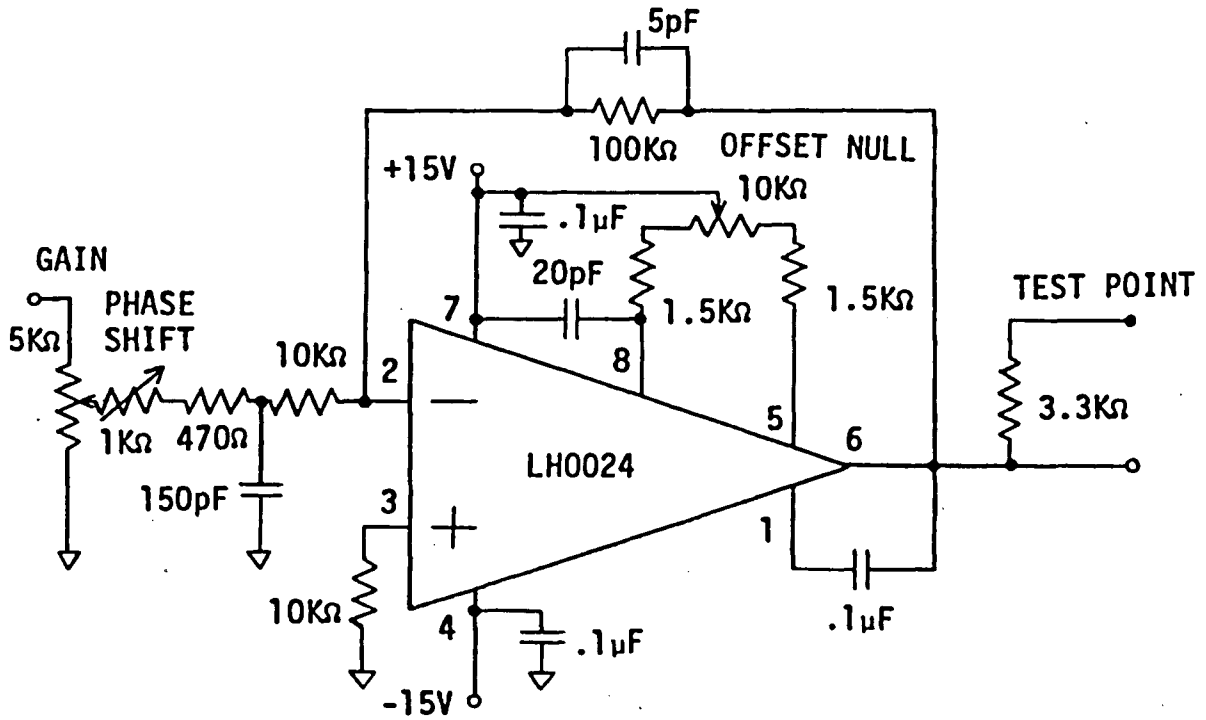


FIGURE 8 Functions required for a crosscorrelating phase detector using harmonic cancellation.



BUFFER AMPLIFIER



PHASE SHIFTER

FIGURE 9 Buffer amplifier and phase shifter schematics.

reference and received signals as these signals pass through the preamplifiers. This additional phase difference remains constant at 3.4° regardless of the true phase difference between the signals because the preamplifier delays are functions of frequency only, and the signal frequencies remain constant at 420 Khz. This 3.4° difference is then simply an offset which translates into a movement of the absolute location of the zero point of the distance measurement scale by $\frac{3.4}{360}$ or about 1 percent. Since at this time the final distance measurement is only to be a relative measurement, offsets or shifts in the entire scale are unimportant. Therefore, the phase delays due to the preamplifiers do not result in errors for relative distance measurements and will not have to be compensated for.

3.2 Phase Shifters

The two quadrature signals required for the crosscorrelation are derived from the buffered input signals by applying each buffered signal to a unity gain phase shifter using an LH0024 operational amplifier. A schematic of the phase shifter appears in Figure 9. The resistor-capacitor network (an integrator) at the input to the operational amplifier can be adjusted to provide a 90° phase shift between the input and output signals at 420 Khz with unity gain. The operational amplifier is compensated for a

20 dB gain by the 20pf capacitor, the 5pf feedback capacitor, and the .1μf output capacitor. With this compensation the bandwidth is about 2 Mhz. Again, an offset null adjustment, an output test point, and high frequency bypass capacitors on the power leads are provided for each phase shifter.

After construction, the phase shifters were tested and adjusted for 90° phase shifts with unity gain at 420 Khz so that the output of each phase shifter is a quadrature version of its input at the same amplitude of approximately 10 volts peak.

3.3 Analog Multiplications

The analog multiplications between received and reference signals are performed by four Analog Devices Model 429B wideband multipliers. The function realized by each multiplier is $\frac{XY}{10}$, where X and Y are the two analog input signals. These multipliers have a rated 3 dB bandwidth of 10 Mhz and a full bandwidth of 2 Mhz. Over this frequency range, full accuracy of .3% of full scale can be achieved with external trimming. This figure includes the effects of irreducible errors due to undesired leakage from the input signals through to the output signal, a situation referred to as feedthrough. Based on this accuracy figure, the amount of spurious 420 Khz signal observed at the multiplier output should not exceed 30mV peak for 10V peak inputs.

Figure 10 details the circuitry required for each multiplier, including the external trimming controls required to achieve highest accuracy. The X balance and Y balance adjustments compensate for DC input offset voltages and the output balance adjustment nulls the output voltage to zero for a zero input simultaneously on the X and Y inputs. The power supply inputs on each multiplier are bypassed to ground by high frequency filter capacitors.

3.4 Harmonic Cancellation Summations

The products from each multiplier, as shown in Table 1 under Figure 10, contain both a DC term proportional to either $\sin\phi$ or $\cos\phi$ and an 840 Khz term proportional to either sine or cosine. As shown back in Figure 3, by properly summing these products, the terms at 840 Khz will cancel, leaving only the DC terms proportional to $\sin\phi$ and $\cos\phi$.

The two products containing the 840 Khz terms that are proportional to the cosine are added using an LH0024 operational amplifier configured as a summing amplifier. A schematic of this summer appears in Figure 11. This circuit adds together the product signals at its inputs, forming a DC output proportional to $\cos\phi$. The circuit is designed to sum each input with unity gain. The operational amplifier is therefore compensated for unity gain

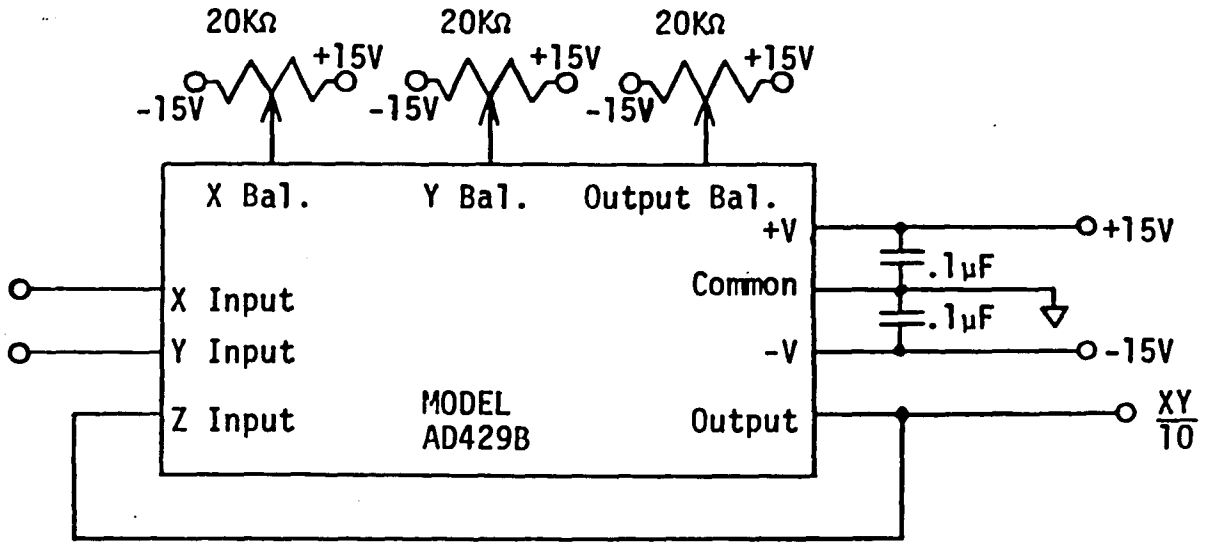
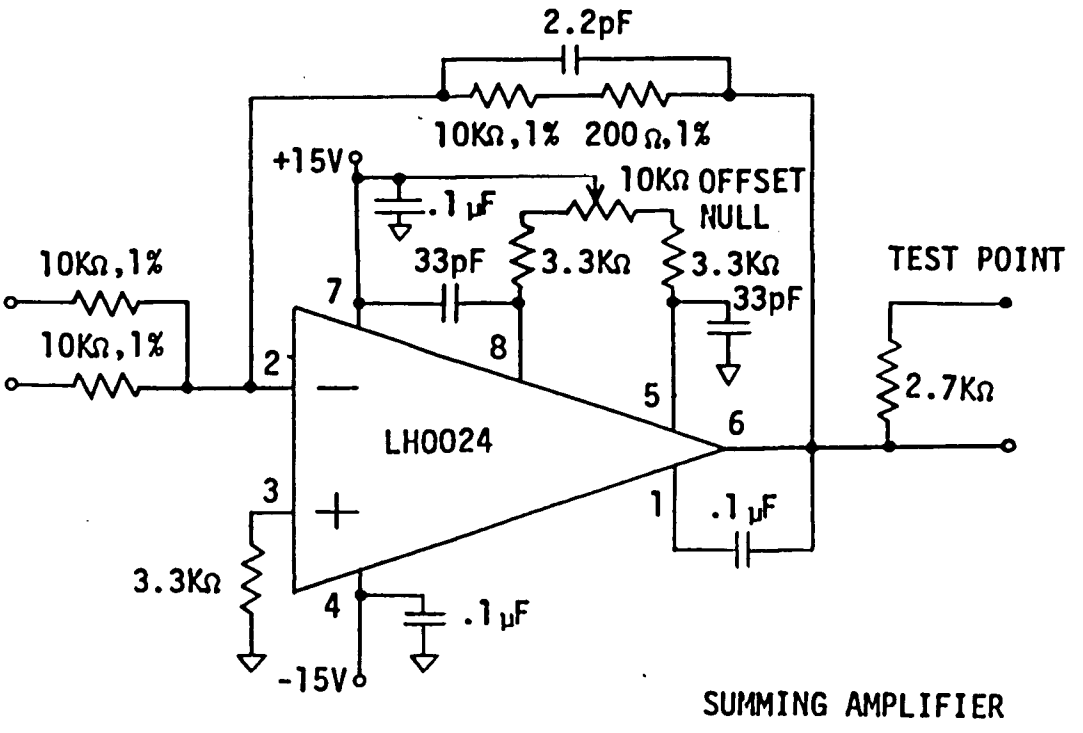


FIGURE 10 Schematic of an AD429B analog multiplier with external trimming adjustments.

Table 1

Multiplier Number	X Input (Reference)	Y Input (Received)	Output
1	$10\cos(\omega t+\theta-\phi)$	$10a\cos(\omega t+\theta)$	$5a\cos\phi + 5a\cos(2\omega t+2\theta-\phi)$
2	$10\sin(\omega t+\theta-\phi)$	$10a\sin(\omega t+\theta)$	$5a\cos\phi - 5a\cos(2\omega t+2\theta-\phi)$
3	$10\sin(\omega t+\theta-\phi)$	$10a\cos(\omega t+\theta)$	$-5a\sin\phi + 5a\sin(2\omega t+2\theta-\phi)$
4	$10\cos(\omega t+\theta-\phi)$	$10a\sin(\omega t+\theta)$	$5a\sin\phi + 5a\sin(2\omega t+2\theta-\phi)$



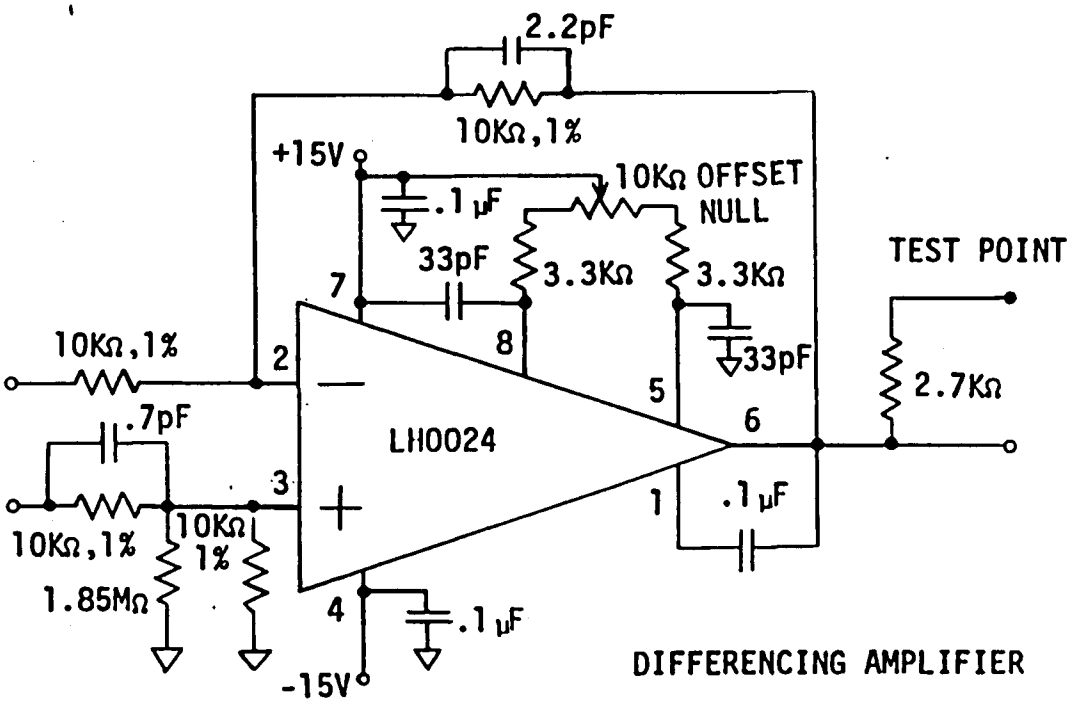


FIGURE 11 Summing and differencing amplifier schematics.

by the two 33 pf capacitors, the 2.2pf feedback capacitor, and the .1μf output capacitor. The bandwidth with this compensation is about 7 Mhz. Power supply bypass capacitors, an offset adjustment, and an output test point are again provided for this summer.

Since a gain of exactly unity for both input signals of this summer was desired, precision resistors were used in construction. After construction was complete and testing begun, the 200Ω precision resistor was added into the feedback loop to trim the summer for best accuracy.

The two products containing the 840 Khz terms that are proportional to the sine are subtracted using an LH0024 operational amplifier configured as a differencing amplifier. A schematic of this circuit appears in Figure 11. This circuit subtracts the product at its inverting input from the product at its non-inverting input and forms a DC output proportional to $\sin\phi$. The circuit is designed for unity gain and therefore the operational amplifier must be compensated for unity gain. The compensation is identical to that used in the previously described summer, namely the two 33pf capacitors, the 2.2pf feedback capacitor, and the .1μf output capacitor. The bandwidth again is 7 Mhz. Power supply bypass capacitors, an offset adjustment, and an output test point are all provided.

Since a highly accurate differencing amplifier was desired, precision resistors were again used in the construction of this circuit. After construction was complete, initial testing disclosed that it was necessary to add both a .7pf capacitance and a 1.85MΩ resistance onto the noninverting input as shown in Figure 11 for best accuracy.

The output of the summing amplifier, 10a $\cos\phi$ and the output from the differencing amplifier, 10a $\sin\phi$ are DC levels that can range from -10 to +10 volts peak depending upon the values of ϕ and a. Also present in the outputs are spurious signals at both 420 Khz and 840 Khz. The 420 Khz signals result from the previously mentioned multiplier feedthrough errors from the input signals. The 840 Khz signals are due to incomplete harmonic cancellation during summing or differencing operations.

3.5 Precision Rectifiers for Absolute Values

The dependence on a of the $\sin\phi$ and $\cos\phi$ signals is eliminated by forming the ratios $\frac{\sin\phi}{\cos\phi}$ and $\frac{\cos\phi}{\sin\phi}$ which are then used to recover ϕ. However, as detailed in section 3.6, the analog circuitry performing these divisions requires that the signal used for the denominator be restricted to positive values only. Therefore, two precision rectifiers are used to form the absolute values of the signals to be used as denominators. Figure 12 shows the basic rectifier circuit. For V_{in} negative, the first

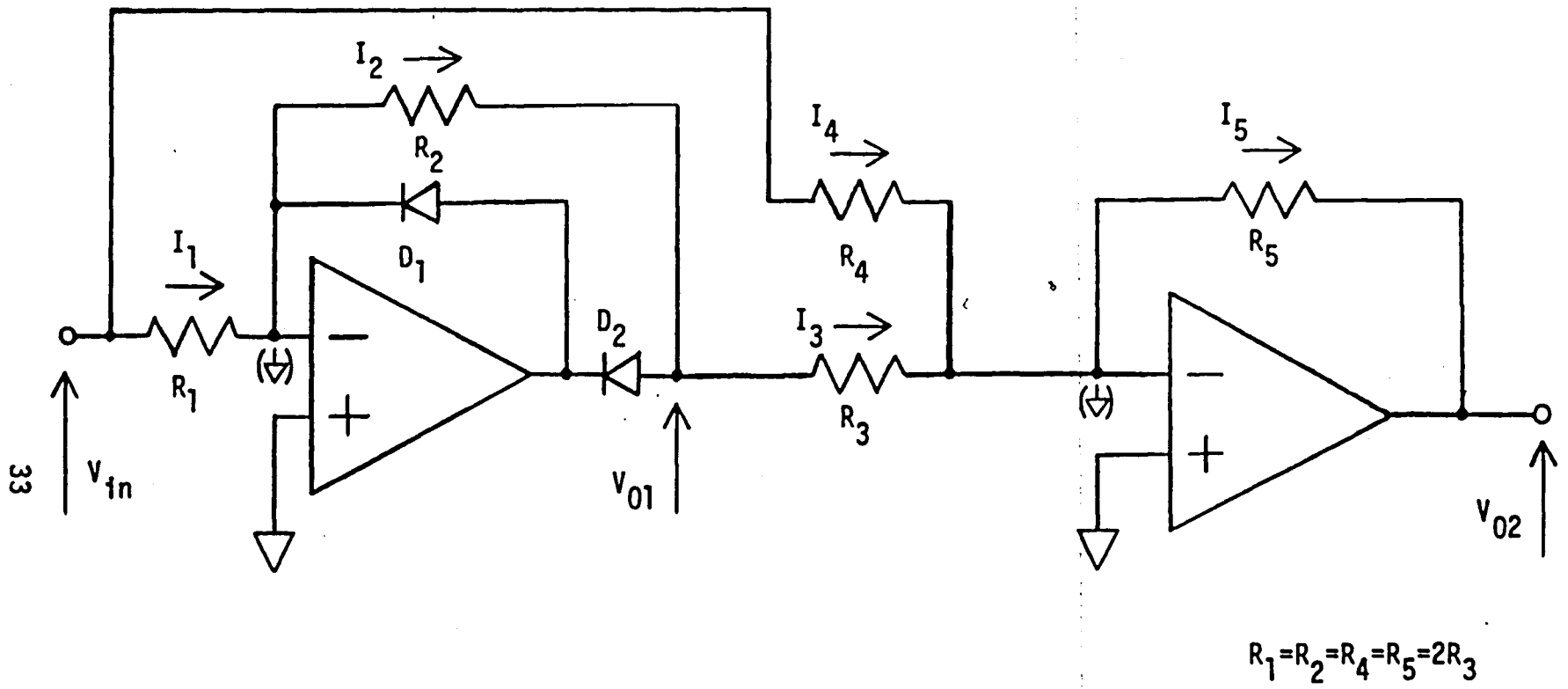


FIGURE 12 Precision rectifier circuit configuration.

operational amplifier will attempt to drive its output positive. The feedback diode D_1 will turn on and clamp that output to approximately .7 volts. Diode D_2 is reverse biased for any positive output voltage and is therefore off. Hence, the resistors R_2 and R_3 are in series. Both ends of this series combination are at virtual grounds due to the operational amplifiers. Therefore, no current can flow through these resistors and the voltage V_{01} must be zero. The second operational amplifier is configured as a standard inverting summing amplifier, with its output given by the equation

$$V_{02} = -\frac{R_5}{R_3} V_{01} - \frac{R_5}{R_4} V_{in}.$$

Since $R_5 = R_4 = 2R_3$, the equation simplifies to $V_{02} = -2V_{01} - V_{in}$. For V_{in} negative and therefore V_{01} zero, the equation reduces to $V_{02} = -V_{in}$ which is the absolute value function for V_{in} negative.

For a positive V_{in} input, the first operational amplifier will drive its output negative. The feedback diode D_1 will be reverse biased and therefore off, while diode D_2 will be forward biased and therefore on. A current of magnitude $\frac{V_{in}}{R_1}$ will flow through both R_1 and R_2 since their junction is at a virtual ground and current can flow nowhere else. Therefore, the voltage V_{01} must be $-\frac{V_{in}}{R_1} R_2 = -V_{in}$, since $R_1 = R_2$. Recalling that $V_{02} = 2V_{01} - V_{in}$ and replacing V_{01} by $-V_{in}$ reduces the equation

for V_{02} to $V_{02} = V_{in}$, which is the absolute value function for V_{in} positive. Therefore, the precision rectifier circuit shown in Figure 11 indeed produces as its output the absolute value of its input signal for both positive and negative inputs.

Type LM301AN operational amplifiers and type 1N914A switching diodes were chosen to construct each precision rectifier whose full schematic is shown in Figure 13. All operational amplifiers were compensated for unity gain using single pole compensation by placing a 33pf capacitor between pins 1 and 8. All operational amplifiers have power supply bypass capacitors and offset null adjustments. The circuits were constructed using precision resistors because the condition $R_1 = R_2 = R_4 = R_5 = 2R_3$ must be met for best performance.

As previously mentioned, the accuracy of such precision rectifier circuits can become quite poor around zero volts. Also, as previously shown, over the intervals in which each ratio is to be used, the denominator trigonometric function of ϕ is always between .707 and 1.000 or -.707 and -1.000. Since the amplitude of these functions is 10, the voltage inputs to the precision rectifier circuits over the intervals of interest are between 7 and 10 volts or -7 band -10 volts. Since these ranges do not include the region around zero volts, there will be no errors resulting from inaccuracies encountered in that zero volts region.

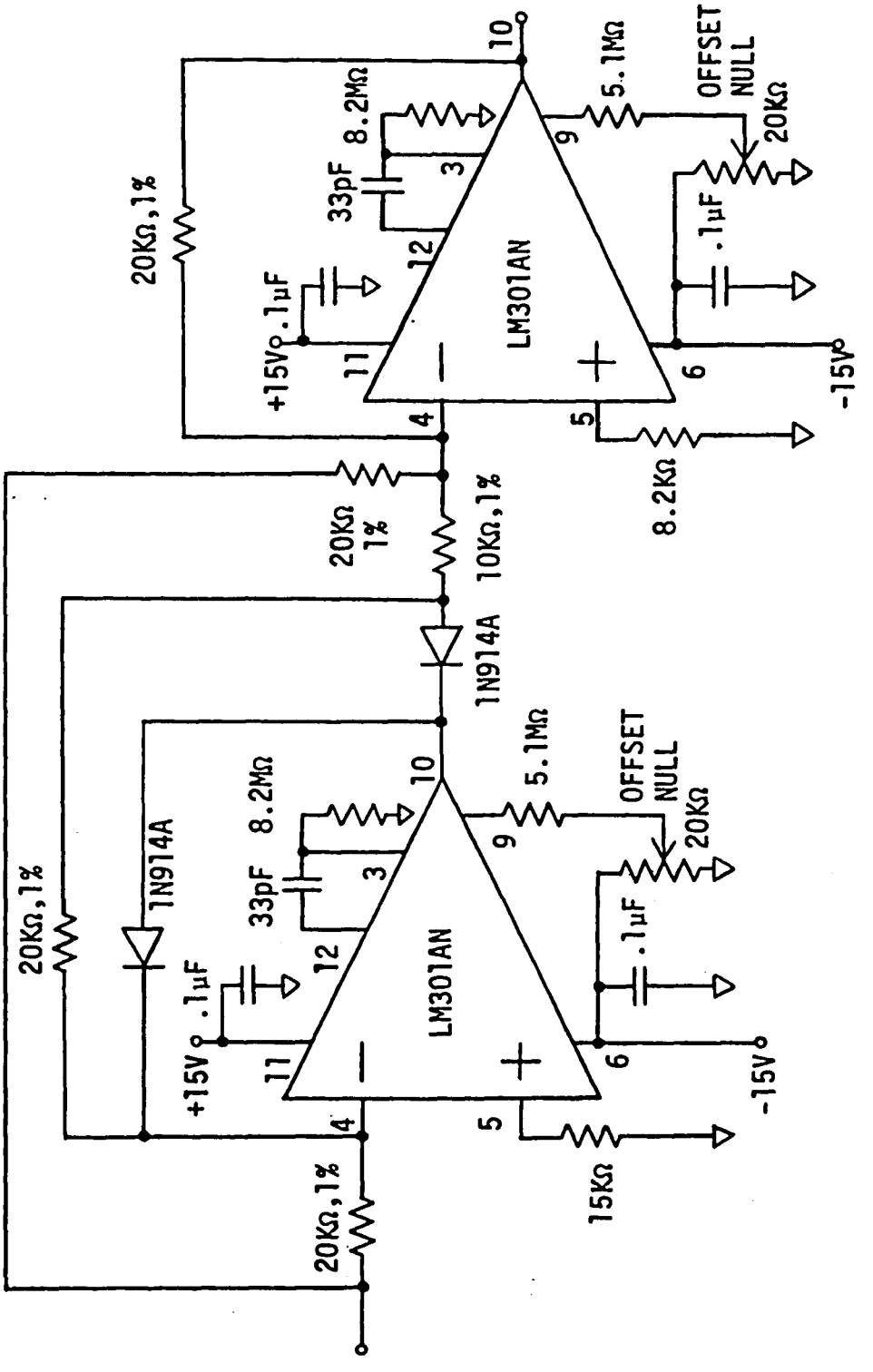


FIGURE 13 Precision rectifier schematic.

3.6 Analog Division

The divisions to eliminate the dependence on initial amplitudes can now be performed. Each two quadrant analog divider was constructed using an analog multiplier in the feedback path of an operational amplifier, as outlined in Figure 14. The following derivation of the transfer function for such a configuration shows that analog division is indeed accomplished. The multiplier produces the function

$$V_M = \frac{V_X V_Y}{10} = \frac{V_{out} \cdot V_2}{10} .$$

The voltage V_1 causes a current I of magnitude $\frac{V_1}{R}$ to flow through both R resistors. The junction of the two resistors is a virtual ground due to the operational amplifier. Therefore, V_M must also be equal to $-IR = -V_1$. Therefore $-V_1 = \frac{V_{out} \cdot V_2}{10}$. Solving for V_{out} results in $V_{out} = -10 \frac{V_1}{V_2}$.

At first glance it would appear that a divider created in this manner would work in all quadrants. However, if V_M and V_X have different signs, the multiplier looks like a negative resistance in the operational amplifier feedback loop, and instability results. To keep the signs of V_M and V_X the same, V_Y must be restricted to positive values only. A similar analysis for an analog divider using a non-inverting operational amplifier configuration leads to the same result that one of the two signal

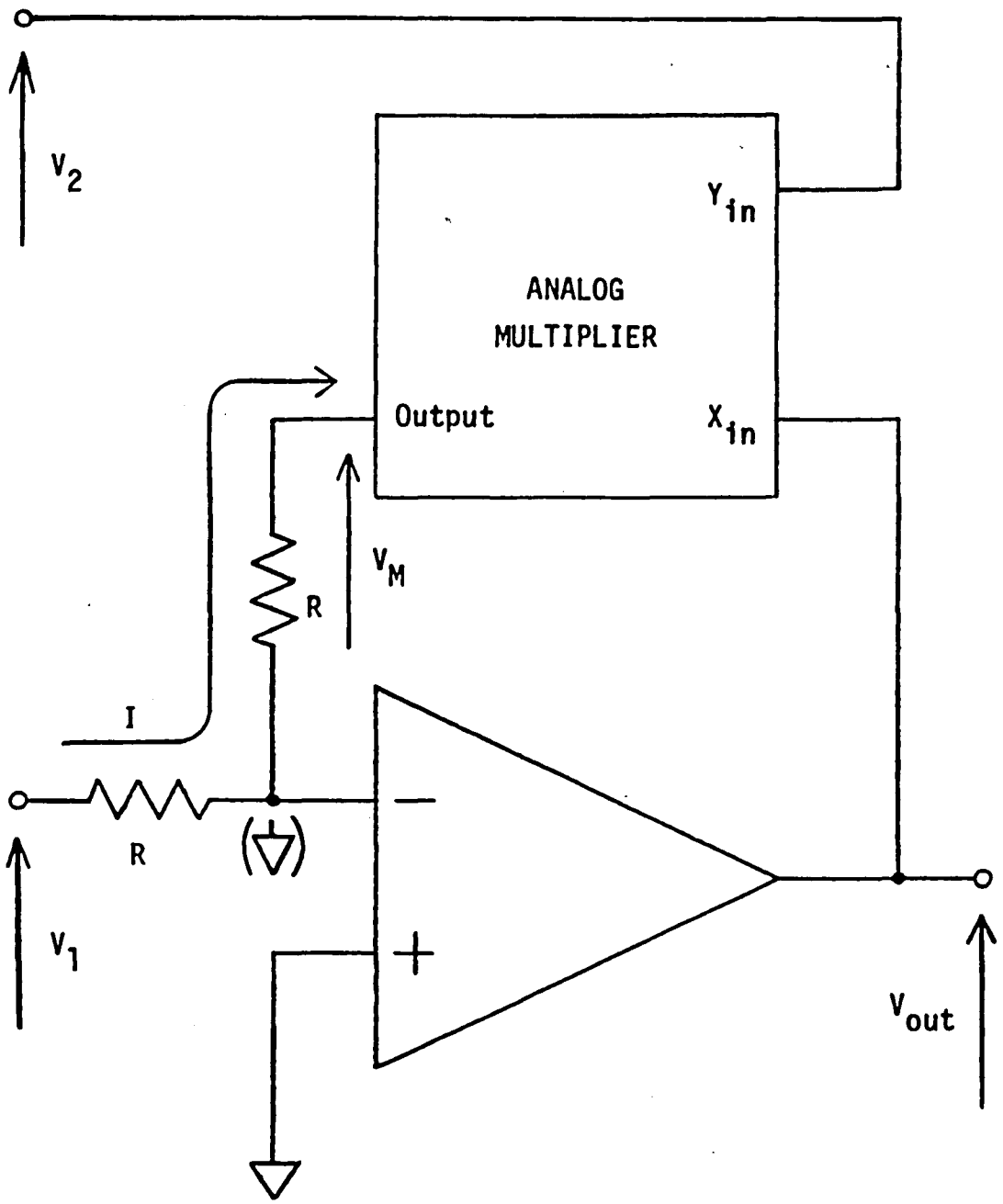


FIGURE 14 Implementing analog division using an analog multiplier as the feedback element of an operational amplifier.

inputs must be unipolar, restricting the divider to two quadrant operation.

The dividers were constructed as shown in Figure 15 using Zeltex model ZM606 multipliers and type AD301ALN operational amplifiers. The ZM606 multiplier has a 500 Khz 3 dB bandwidth and an accuracy of .25% with external trims. The X,Y null adjustment compensates for static feed-through errors. The output zero adjustment nulls the output for a zero input on the X and Y inputs. The gain adjustment trims the multiplier's gain. The type AD301ALN operational amplifier is again compensated for unity gain with a 33pf capacitor. An offset null adjustment is provided. Both the multiplier and the amplifier have bypass filter capacitors on the input power leads. Precision resistors were used to achieve highest accuracy.

Table 2, under Figure 15, lists the two input signals to and the output signal from each divider. Each divider output, $-10\frac{\sin\phi}{|\cos\phi|}$ or $-10\frac{\cos\phi}{|\sin\phi|}$ will be used to determine ϕ when that output is in the -10v to +10v range because only then is its ratio $\frac{\sin\phi}{|\cos\phi|}$ or $\frac{\cos\phi}{|\sin\phi|}$ in the desired -1v to +1v range used to determine ϕ as discussed in the overview. The following sample and hold amplifiers and analog to digital convertors are therefore configured for a -10v to +10 input level range. However, the divider outputs may be as large as ±15 volts. So, to avoid a drastic

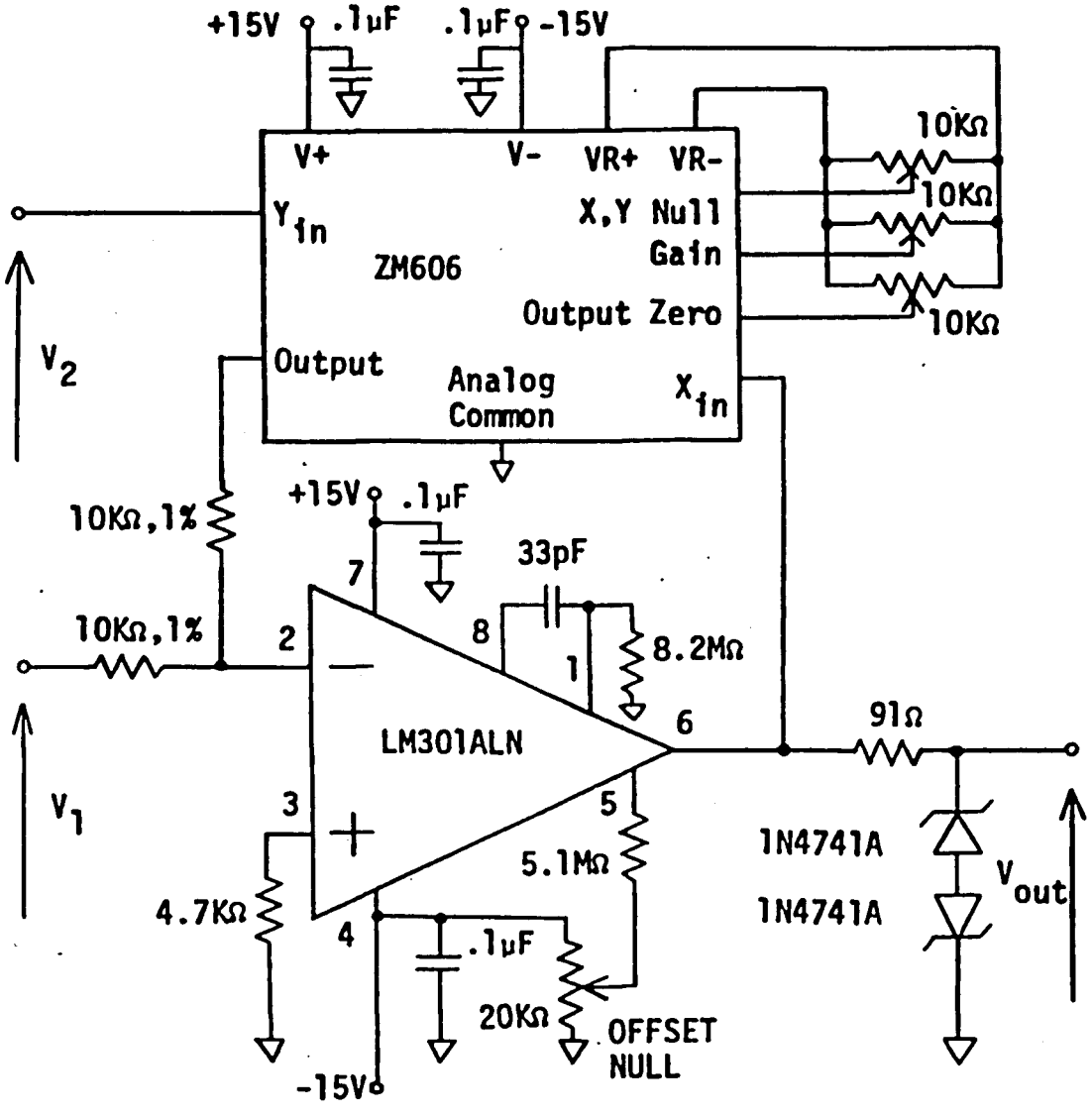


FIGURE 15 Analog divider schematic.

Table 2

Divider	V_1 (Numerator)	V_2 (Denominator)	V_{out}
1	$10a \sin\phi$	$\lvert 10a \cos\phi \rvert$	$-10 \frac{\sin\phi}{\lvert\cos\phi\rvert}$
2	$10a \cos\phi$	$\lvert 10a \sin\phi \rvert$	$-10 \frac{\cos\phi}{\lvert\sin\phi\rvert}$

overdriving of those following amplifiers and convertors, the output of each divider is limited to a range of approximately -11 to +11 volts by two 1N4741A 11 volt zener diodes and a 91Ω resistor.

3.7 Sampling and Analog to Digital Conversion

Each of the quotients $-10\frac{\sin\phi}{|\cos\phi|}$ and $-10\frac{\cos\phi}{|\sin\phi|}$ is simultaneously sampled and converted to a 12 bit digital code by the sample and hold amplifier and analog to digital convertor combination shown in Figure 16. The SHA1134 is an Analog Devices general purpose sample and hold amplifier and the ADC1133 is an Analog Devices 12 bit 25μs conversion time successive approximation type analog to digital convertor. The command to sample is received by the convertor which then controls the amplifier mode.

Upon receipt of the rising edge of the sample command, the convertor initializes its conversion sequence and sets the $\overline{\text{STATUS}}$ and MSB outputs low, and the STATUS and BIT 2 through BIT 12 outputs high, requiring a maximum time of 100ns. Conversion does not begin, however until the trailing edge of the sample command arrives. The $\overline{\text{STATUS}}$ output line is connected to the mode control input on the sample and hold amplifier. The high to low transition of the $\overline{\text{STATUS}}$ output during the convertor's initialization causes the amplifier to sample its analog input signal and hold that

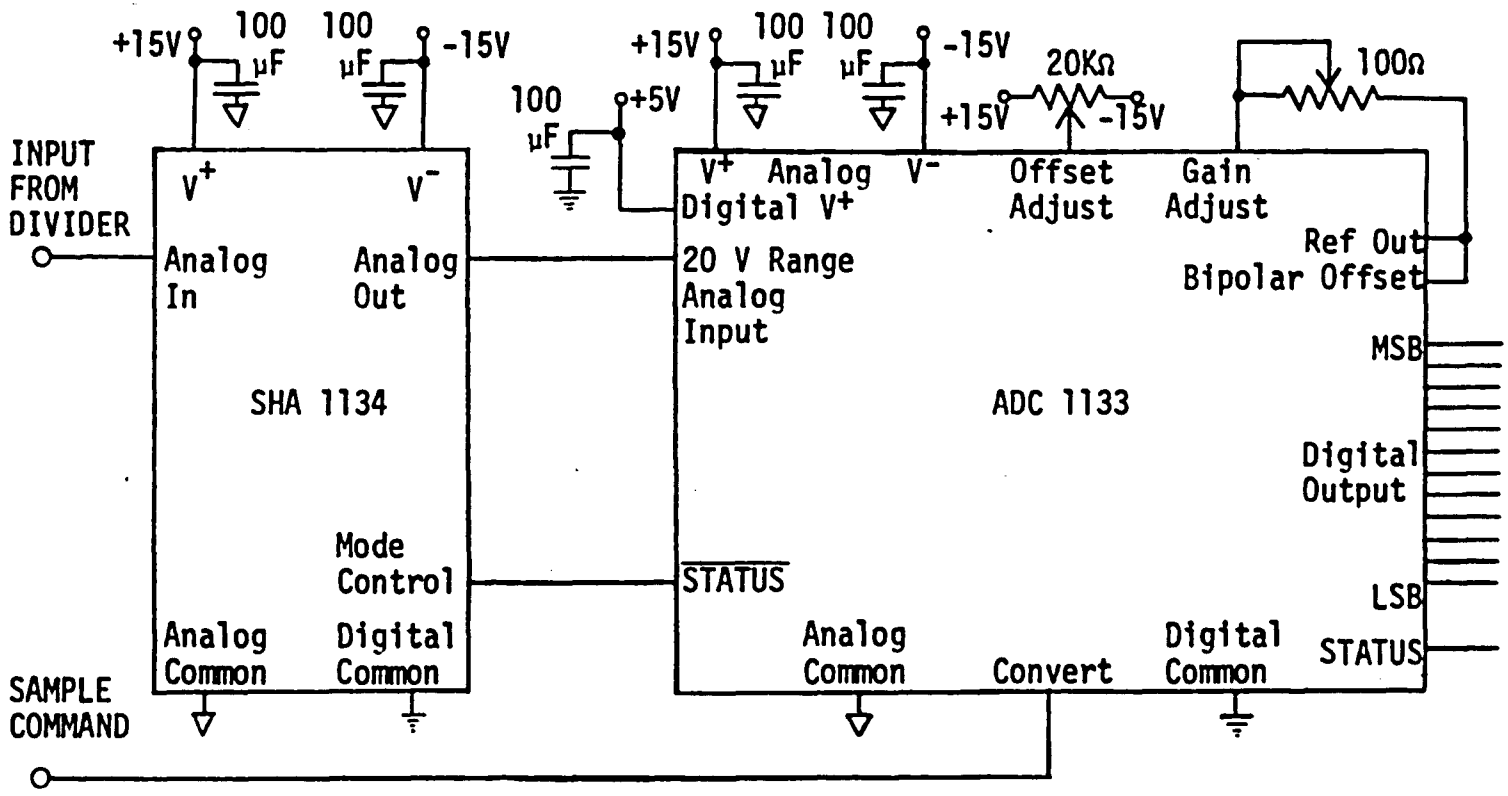


FIGURE 16 Sample and hold amplifier and analog to digital convertor schematic including trim adjustments.

sample value at its output. The time delay from receipt of this mode control transition to the onset of the hold mode, called aperature delay, for the SHA1134 is 50ns maximum. The output settling time to 0.01% of its final value is 1μs. Therefore, the conversion of this sample value should not begin until at least 1.050μs after the $\overline{\text{STATUS}}$ high to low transition. This requires the sample command to be at least 1.150μs long so that the trailing edge does not arrive too soon.

Once the trailing edge of the sample command occurs, the analog to digital convertor begins to create a digital code proportional to the sample value. The output lines are set in order, starting with the MSB line. When the LSB line is set, the STATUS and $\overline{\text{STATUS}}$ outputs return to low and high levels respectively, and the conversion is complete. The time required for conversion is 25μs.

When the $\overline{\text{STATUS}}$ output transitions back to a high level, the sample and hold amplifier output again follows the analog input. The time necessary for the amplifier output to acquire the input signal to 0.01% accuracy, called acquisition time, is 4.1μs maximum. Hence, the next sample command should not occur until at least 4.1μs after the previous conversion is complete. Therefore, the maximum rate at which samples are taken should not exceed one sample every 30.25μs to insure adequate times for settling and

conversion. This criterion is easily met by the sampling scheme devised in the system overview, which requires that a sample be taken every 37.95μs.

The SHA1134 has a gain of +1, ±0.04%. Since the analog voltage range from the previous divider circuits is -11 to +11 volts, the sample values at the amplifier's output will range from -11 to +11 volts. The droop rate of the amplifier's output while in the hold mode is a maximum ±200mV/S. This means that during the 25μs conversion time, the sampled output will change at most by ±5μv.

The ADC1133 is configured in a bipolar input mode over an input voltage range of -10 to +10 volts. Table 3 lists several analog input voltages and their corresponding digital outputs, which are in an offset binary code.

Table 3

Analog Input	Digital Output
+9.9951v	111111111111
+5.0000v	110000000000
+0.0049v	100000000001
+0.0000v	100000000000
-0.0049v	011111111111
-5.0000v	010000000000
-9.9951v	000000000001
-10.0000v	000000000000

For any analog inputs of +10 volts or more, the convertor generates all ones as output. For any analog inputs of -10 volts or less, the convertor generates all zeroes as output. The quantizing error for the convertor is $\pm\frac{1}{2}$ of a least significant bit, or 2.45mV. Two external trims, labeled offset adjust and gain adjust, are provided to properly calibrate the convertor.

To sample according to the scheme previously outlined in the system overview, the circuitry shown in Figures 17 and 18 was designed and built to generate a sample command every $15\frac{15}{16}$ periods of 420 Khz. The reference for sampling is obtained from the 420 Khz reference signal. The reference is converted to a TTL compatible square wave using an LM311 comparator. This comparator

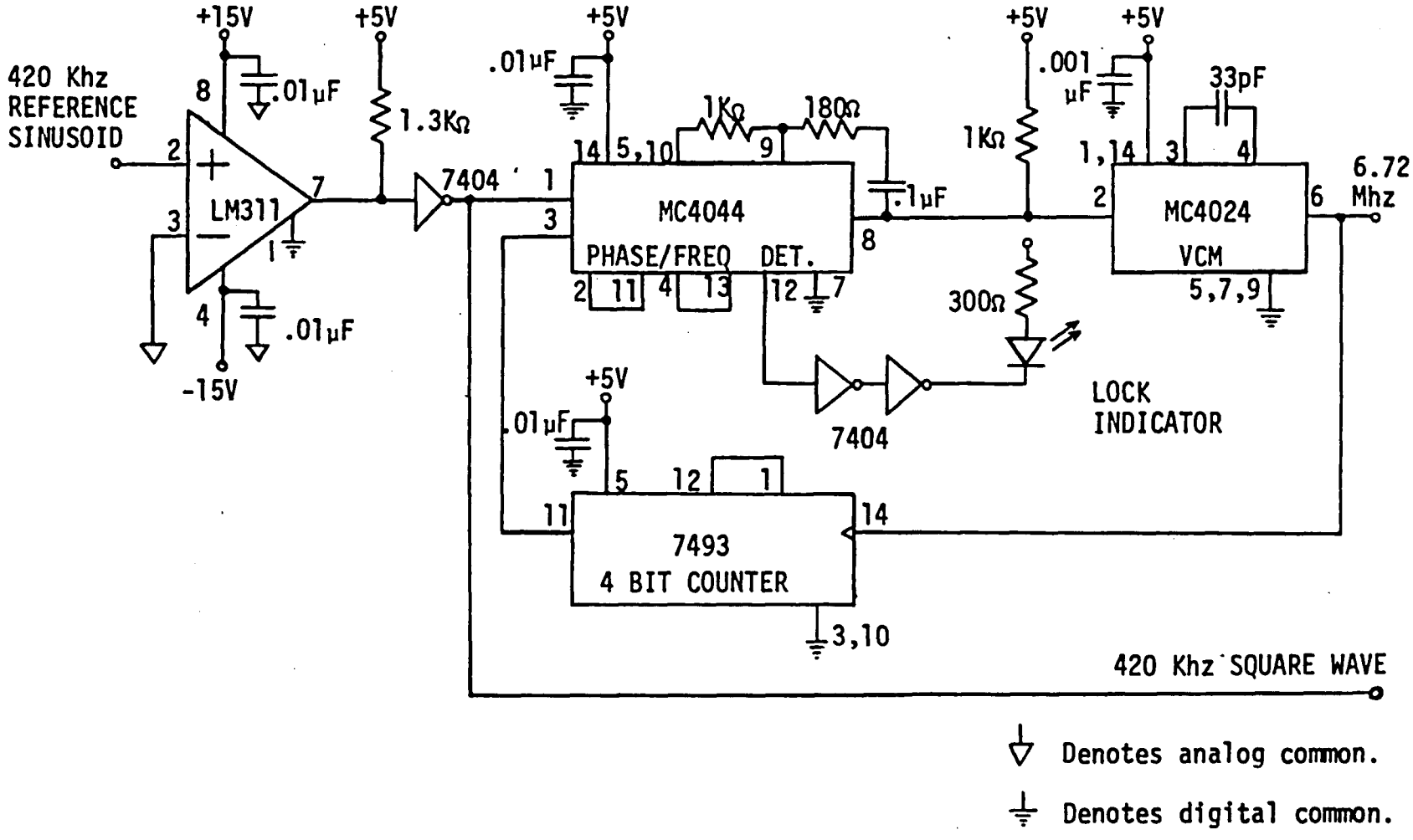


FIGURE 17 420 Khz square wave generator and 6.72 Mhz digital phase locked loop circuitry.

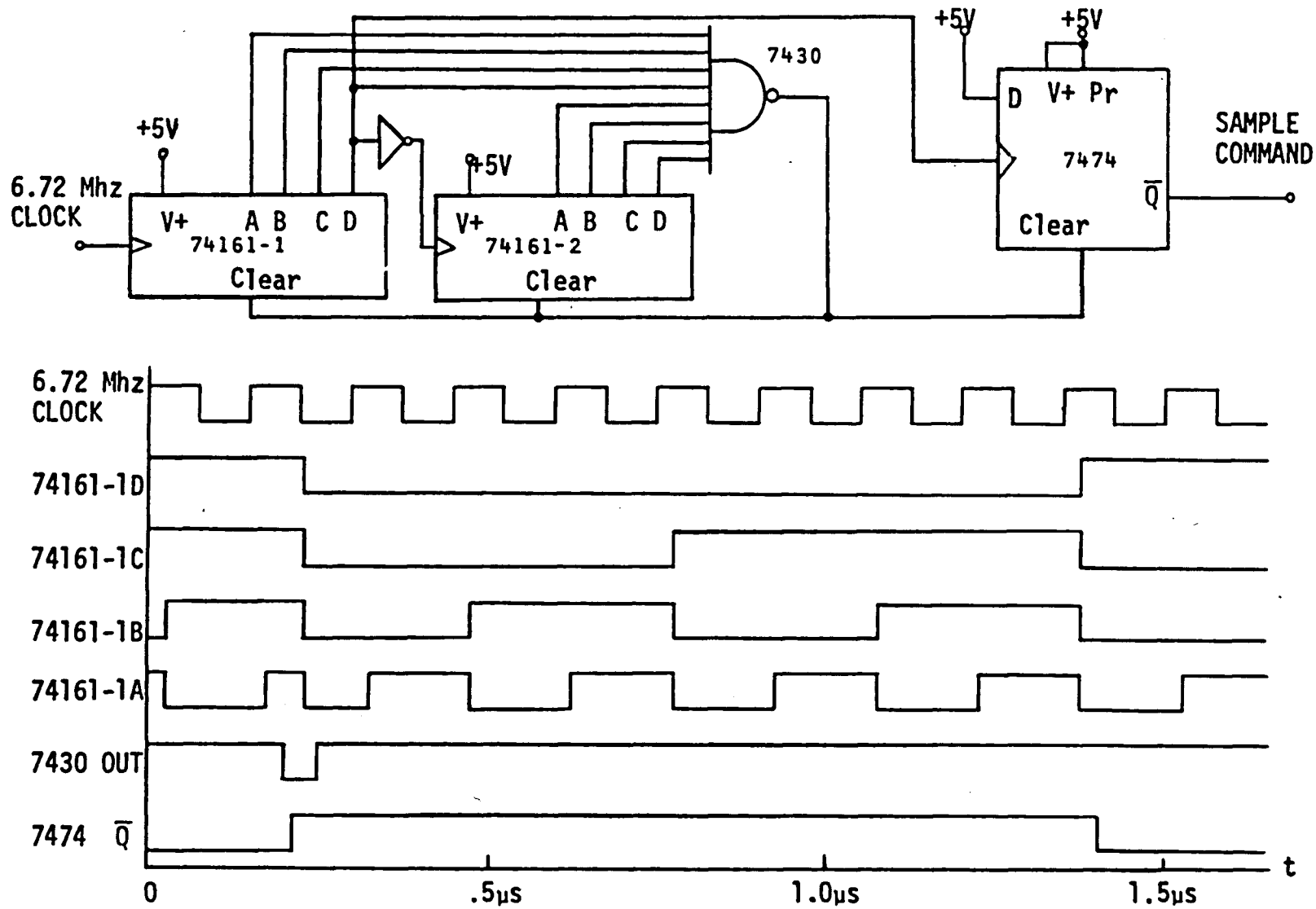


FIGURE 18 Count to 255 circuitry and timing diagram.

has independent ground connections to its internal input and output stages, which enables the input to reference the analog system ground and the output to reference the digital system ground. The comparator is configured to produce a high logic output when the 420 Khz reference is positive and a low logic output when the 420 Khz reference is negative. The invertor following the comparator is there to insure sharp transitions at the square wave edges. The resulting invertor output is a 420 Khz clock synchronized to the reference signal.

To divide the 420 Khz period into 16 divisions, a digital phase locked loop is used. The loop consists of a type MC4044 phase-frequency detector, a type MC4024 voltage controlled multivibrator, and a type 7493 4 bit counter. The phase detector compares the trailing edge transitions of the 420 Khz clock to the trailing edge transitions of the 4 bit counter output and produces a control voltage proportional to the frequency and phase differences between them. This control voltage is low pass filtered by the RC network around the phase-frequency detector and is applied as the control input to the voltage controlled multivibrator. The multivibrator produces a higher frequency square wave output proportional to the controlling input voltage over a frequency range determined by an external 33pf capacitor. To close the loop, the high frequency square wave output is applied to the

input of the 4 bit counter, which is configured to count to 16. The counter generates one square wave output for every 16 square wave inputs. To lock the loop, the counter's output must match the master clock's output in both frequency and phase. The multivibrator must therefore run at a frequency 16 times greater than 420 Khz, or 6.72 Mhz when the loop is locked. Hence, a 6.72 Mhz clock, which is synchronized to the 420 Khz clock, is created by this phase locked loop.

An out of lock signal is also available from the phase detector. This signal, high when the loop is locked, goes low as soon as the input signals do not match. The out of lock signal is buffered by two invertors to drive an LED which lights to indicate an unlocked situation.

Each period of the 6.72 Mhz clock occurs in 1/16 of a period of 420 Khz. Generating a sample command every 255 periods of the 6.72 Mhz clock will therefore result in a sample being taken every $15\frac{15}{16}$ periods of 420 Khz. Figure 18 shows the circuitry constructed to generate the sampling commands and a timing diagram depicting the output levels of the circuit components during the interval when each sampling command is generated. The zero for the timing diagram scale was chosen to coincide with the start of the 254th period of the 6.72 Mhz clock pulse. All propagation delay times are based on the maximum times specified for standard

TTL devices.

The two 74161 4 bit synchronous counters are configured to form an 8 bit counter which counts the periods of the incoming 6.72 Mhz clock. When the count reaches 255, all 8 output lines from the counter are high simultaneously. This forces the output of the 8 input nand gate low. This low is on the clear input to the counters, so all 8 counter output lines are reset to zero. The nand gate output is therefore forced high again, which releases the clear. These events take about 100ns or 2/3 of a clock period to complete, which means that when the next clock transition occurs, about 50ns later, it will be counted as the number one period in the next 255 count. The net result then is that the counter causes a 58ns negative pulse to be generated at the nand gate output for every 255 periods of the 6.72 Mhz clock.

Recalling that the sample command must be a positive pulse at least 1.150μs long, it is obvious that the 58ns negative pulse cannot be used for this purpose. Therefore, this shorter pulse is used to control a 7474 D type flip flop which generates the actual sample command. During most of the count to 255 interval, the flip flop is set because it was previously clocked during the 8th 6.72 Mhz clock period by the zero to one transition of the D output of the first 74161 counter. Therefore, $\overline{Q}$ is low. When the 58ns clear pulse occurs, the flip flop clears and $\overline{Q}$ goes high. The flip flop remains in this state until it is again clocked

during the 8th 6.72 Mhz clock period by the zero to one transition of the first 74161 D output. $\overline{Q}$ then goes low, and remains low until the next 58ns clear pulse occurs. Therefore, the $\overline{Q}$ output from this D flip flop goes high for 1.192μs once every 255 periods of the 6.72 Mhz clock and serves as the sample command.

3.8 Selection of Convertor Outputs

When each digital conversion is completed, the convertor output which is not out of range must be selected to interpret ϕ. The AD1133 convertors do not provide overrange signals that indicate when the input range is exceeded. However, recall that the output code for any input signal greater than or equal to +10 volts is all ones, and the output code for any input signal less than or equal to -10 volts is all zeros. One convertor output can be monitored for these codes. If these codes do not occur, the monitored output is selected and if the codes do occur, the other output is selected. It may appear that a problem can arise using this selection method at the very end of the valid input range to the monitored convertor, where its input voltage is exactly ±10 volts. Here, the output will look like an overrange and the monitoring network will select the other convertor's output. However, as stated in the system overview, both convertor outputs are simultaneously valid at the ±10 volt endpoints and

either convertor output may be used to determine ϕ. Hence, there is no difficulty in selecting the other convertor output in this case.

The circuitry in Figure 19 was designed to select the valid convertor output code by monitoring the $-10\frac{\sin\phi}{|\cos\phi|}$ convertor output for all zeroes or all ones. When either of these two situations occurs, the select line goes high and the 2:1 selectors are set to select the $-10\frac{\cos\phi}{|\sin\phi|}$ convertor output. Otherwise, the select line is low and the $-10\frac{\sin\phi}{|\cos\phi|}$ convertor output is selected.

The independent status signals from each convertor are combined as shown in Figure 19 to produce a single status signal. This signal remains high until both convertors have finished their conversion cycles, at which time it goes low. The 2:1 selector enable inputs are connected to this status line, disabling the selectors when conversions are taking place.

3.9 Table Lookup to Determine Angle

To determine the value of ϕ from the selected convertor data, a lookup table for the functions $-10\frac{\sin\phi}{|\cos\phi|}$ and $-10\frac{\cos\phi}{|\sin\phi|}$ was created and burned into 3 type 2708 1K by 8 eraseable programmable read only memory chips. The circuitry for the table is detailed in Figure 20. Eleven of the twelve selected data lines form the address to the lookup table. The least significant bit data line

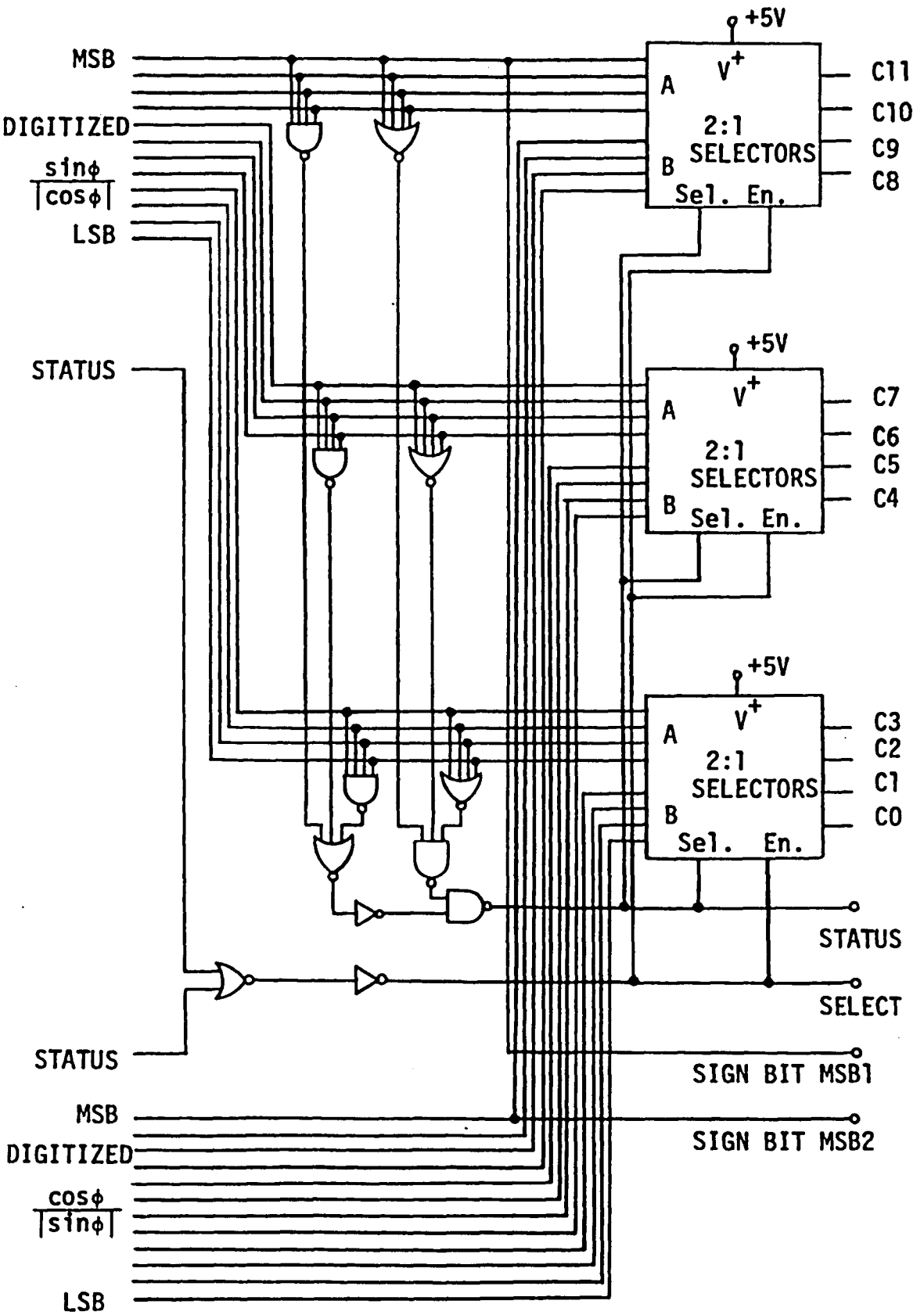


FIGURE 19 Selection and status circuitry.

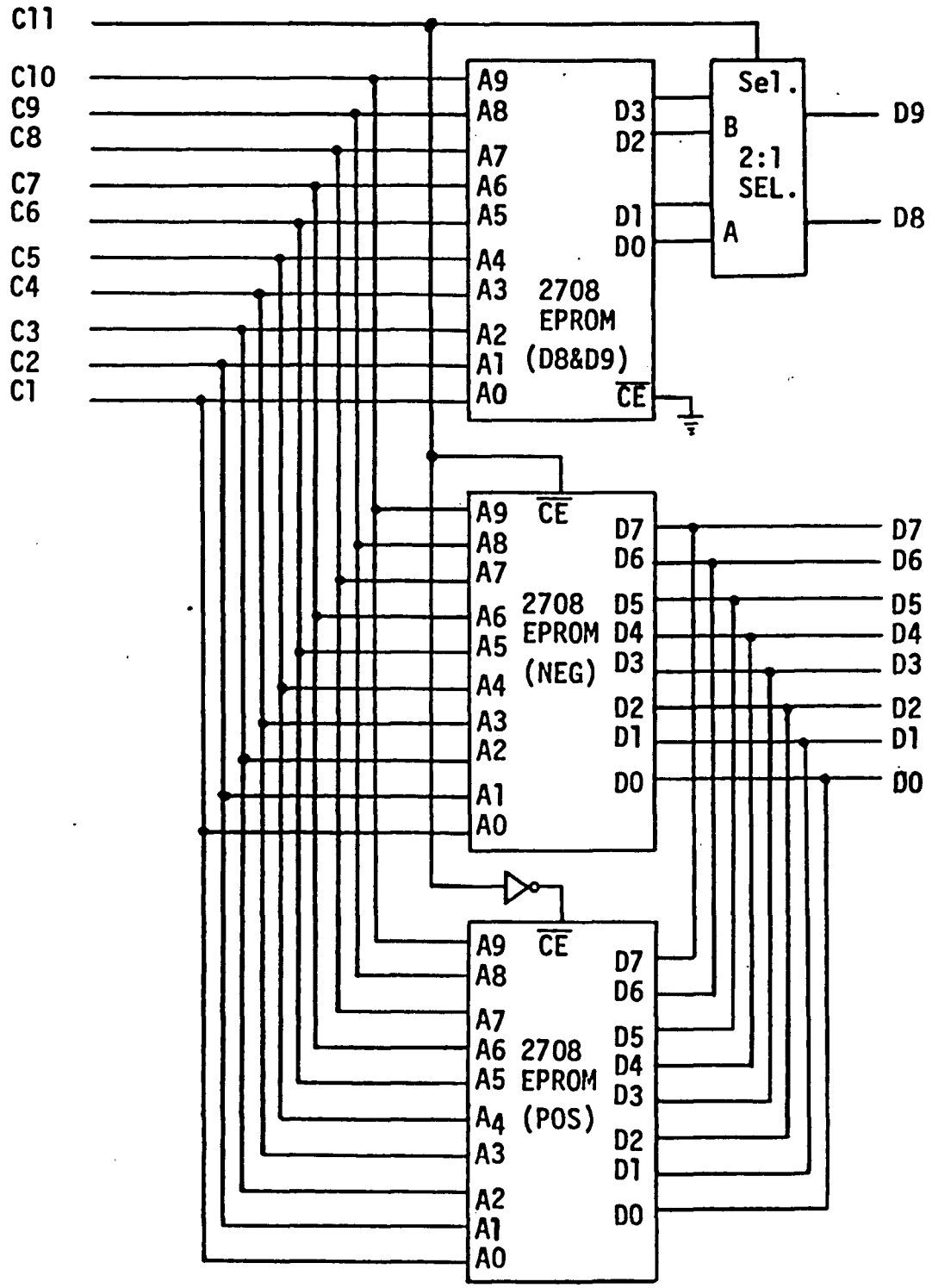


FIGURE 20 EPROM lookup table circuitry.

is not used in order to minimize the table size. Ten data bits of output from the table represent the angle. Since the two digitized functions have the same basic curve as shown back in Figure 4, only a principle branch of one function needs to be stored. The branch ranging from -45° to +45° was chosen. The status of the select line and the most significant bits from each convertor prior to selection are sufficient to later place the angle into its correct quadrant. In addition, since the sign of the function and the angle agree over the stored -45° to +45° range, there is no need to store a sign bit for the angle.

The three 2708 memory chips are arranged to form the lookup table in the following way. Each chip has 10 address line inputs which are connected to the selected convertor output bits 2 through 11. Each chip also has a chip enable input. One chip is used to store the lower 8 data bits for negative function values. A second chip, whose output is connected in parallel to this first chip, stores the lower 8 data bits for positive function values. The most significant bit from the selected convertor output, the sign bit, is connected to the chip enable on the negative function value chip. The complement of that sign bit is connected to the chip enable on the positive function value chip. When addressed, one of the two chips is enabled, based on the sign bit value, and supplies the data bits D0 through D7.

The third memory chip stores D8 and D9, the two highest order data bits, for both positive and negative function values. Outputs D0 and D1 of that third chip represent D8 and D9 for negative function values, and outputs D2 and D3 represent D8 and D9 for positive function values. These two pairs of data outputs are connected to a 2:1 selector. Based again on the value of the sign bit, which is connected to the select input line, the selector chooses the correct pair of data outputs from the third chip for data bits D8 and D9.

The angles stored in the lookup table are coded in the following way. The minimum value, 0.0°, has the representation $0000000000_{(2)}$ or $0_{(10)}$. The maximum value, 45.0°, has the representation $1000000000_{(2)}$ or $512_{(10)}$. All angles between 0.0° and 45.0° have a proportionally corresponding code between $0000000000_{(2)}$ and $1000000000_{(2)}$. This coding therefore allows resolution of the angle to .1°. The major advantage to this coding scheme is that the multiples of 45.0° which will be necessary to move the angle into the correct quadrant are easily represented as simple powers of two. For example, the code for 90.0° would be twice $512_{(10)}$ which is 2^{10}, and the code for 180.0° would be four times $512_{(10)}$ which is 2^{11}. This fact greatly simplifies the hardware required to accomplish the quadrant adjustments.

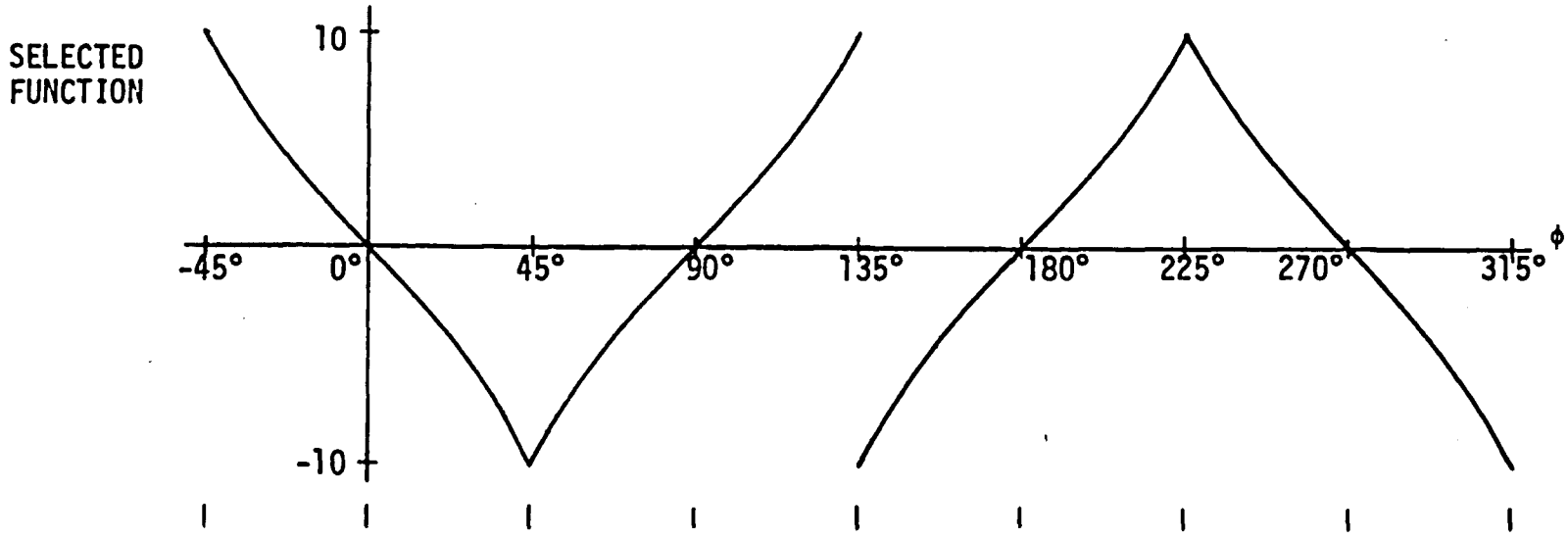
3.10 Angle Placement into the Correct Quadrant

Figure 21 contains a graph of the selected function versus the phase angle ϕ. Below the graph is a listing of the values of the select line and sign bits from each converted function for every 45° interval. As can be seen, each 45° interval has a unique combination of these three signals. Table 4 contains a listing for each 45° interval of the function to be performed on the data from the lookup table to place the represented angle in the correct quadrant.

Table 4

Correct quandrant for ϕ	Function to be performed on data from lookup table
-45.0° to 0.0°	0.0° - data
0.0° to 45.0°	0.0° + data
45.0° to 90.0°	90.0° - data
90.0° to 135.0°	90.0° + data
135.0° to 180.0°	180.0° - data
180.0° to 225.0°	180.0° + data
225.0° to 270.0°	270.0° - data
270.0° to 315.0°	270.0° + data

Again, each 45° interval requires a unique function to be performed on the data for that interval. Therefore, the three



SELECTED FUNCTION:	$\frac{\sin\phi}{\lvert\cos\phi\rvert}$	$\frac{\sin\phi}{\lvert\cos\phi\rvert}$	$\frac{\cos\phi}{\lvert\sin\phi\rvert}$	$\frac{\cos\phi}{\lvert\sin\phi\rvert}$	$\frac{\sin\phi}{\lvert\cos\phi\rvert}$	$\frac{\sin\phi}{\lvert\cos\phi\rvert}$	$\frac{\cos\phi}{\lvert\sin\phi\rvert}$	$\frac{\cos\phi}{\lvert\sin\phi\rvert}$
SELECT LINE:	0	0	1	1	0	0	1	1
MSB1 SIGN :	1	0	0	0	0	1	1	1
MSB2 SIGN :	0	0	0	1	1	1	1	0

FIGURE 21 Graph of the selected function versus ϕ and a listing of signal conditions over each 45° interval.

signals from the select line and the sign bits can be used to generate the functions for each 45° interval.

An addition or a subtraction and one of four constants must be chosen for each of the eight 45° intervals. For the addition and subtraction, a single signal arbitrarily chosen low for addition and high for subtraction is sufficient to specify the proper arithmetic function. Of the four constants, three are even multiples of 45.0° and are therefore represented as follows: 90.0° by $010000000000_{(2)}$; 180.0° by $100000000000_{(2)}$; 270.0° by $110000000000_{(2)}$. The fourth constant, 0.0°, is represented by $000000000000_{(2)}$. Bits zero through nine are all zero for all four constants. Therefore, signals representing just bits ten and eleven are sufficient to specify the constant, with all other bits set to zero.

For all 8 45° intervals, Table 5 lists as inputs the values of the select line and sign bits as well as the values for the addition/subtraction and bit ten and eleven signals to be generated.

Table 5

Values of Input Signals			Values of Functions to be Generated		
Select Function	$\frac{\sin\phi}{\lvert\cos\phi\rvert}$ sign bit	$\frac{\cos\phi}{\lvert\sin\phi\rvert}$ sign bit	Add/ Subtract (0/1)	Bit 11	Bit 10
0	1	0	1	0	0
0	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	1
0	0	1	1	1	0
0	1	1	0	1	0
1	1	1	1	1	1
1	1	0	0	1	1

By inspection, the desired bit ten signal is implemented by simply using the select line. Some combinational logic performed on the inputs is required to realize the bit eleven signal. Finally, the addition/subtraction signal is simply the exclusive or function of all three input signals.

To perform the required mathematical functions listed in Table 4, the circuitry pictured in Figure 22 was designed. The three 74181 4 bit arithmetic logic units and the 74182 carry look ahead generator are configured to form a fast 12 bit adder/ subtractor. The data from the lookup table are presented to the

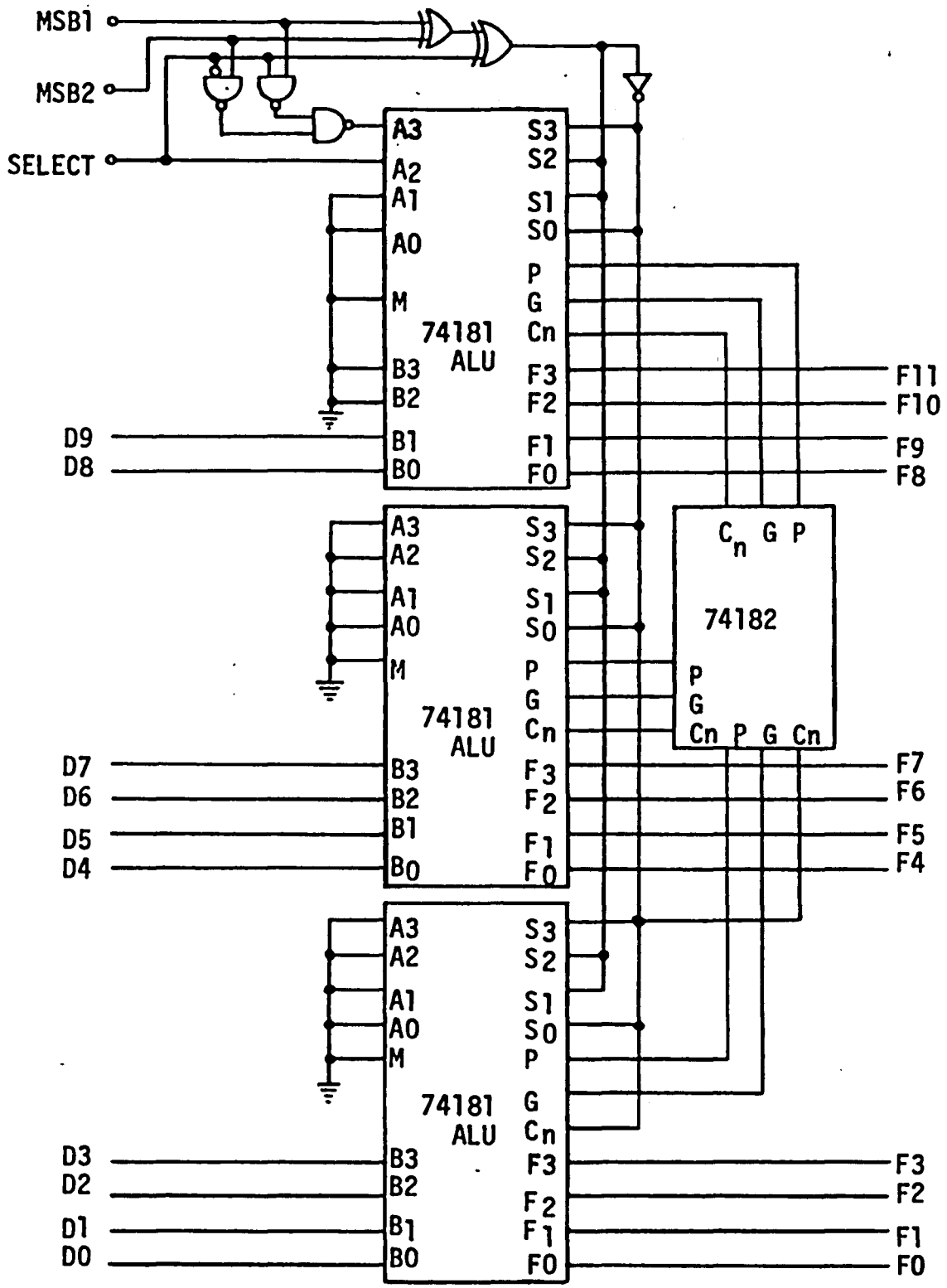


FIGURE 22 Arithmetic logic units and combinational logic required to implement Table 4 functions.

B inputs to be added to or subtracted from the constant presented to the A inputs. As previously specified, bits zero through nine of the constant are set to zero by grounding them. Bit ten is connected to the select line and bit eleven is realized by the combinational logic indicated. The addition/subtraction signal, created by the exclusive or gates, and its complement form the two required arithmetic logic unit operation codes for addition (1001) and subtraction (0110). The 12 output data bits from the adder/subtractor then represents the angle ϕ.

3.11 Averaging of Samples

These twelve data bits go to a 16 bit accumulator to be summed to previous results for averaging. As shown in Figure 23 the accumulator is composed of four 4 bit binary adders and 16 D type flip flops. The new data appear on the A inputs and the previous sum appears on the B inputs. The adders then compute a new sum which appears at the outputs. Upon receipt of the leading edge of a positive pulse on the clock line, the flip flops latch the new sum which replaces the previous sum and the accumulator is ready to receive a new input. The flip flop latch can be cleared by the application of a low level pulse on the clear line.

All of the operations from the initial convertor output selection to the addition performed by the four 7483 adders must

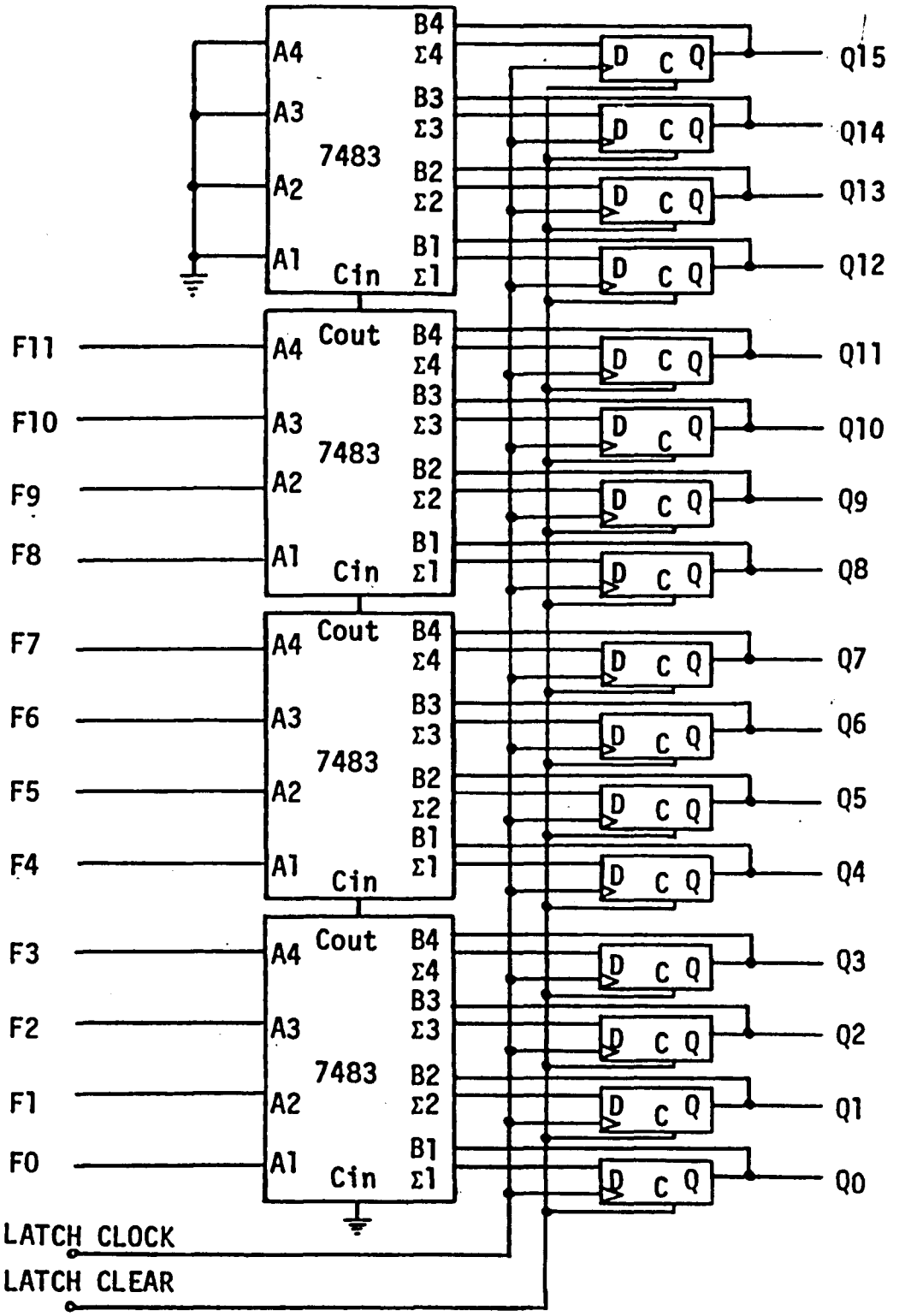


FIGURE 23 Logic elements necessary to implement a 16 bit accumulator with clear.

have time to occur before the flip flop latch receives its clock pulse. Based on figures for standard TTL maximum propagation delays, the times required for the previously described operations are as follows: convertor output selection, 115ns; table lookup, 485ns; arithmetic operations, 40ns; accumulator addition, 50ns. Thus, a total delay of about 700ns is required between the status transition indicating the convertors are finished and the leading edge of the latch clock pulse. The circuitry pictured in Figure 24 was designed to produce the latch clock pulse at lease 700ns later than the status transition time using existing signals. A timing diagram showing the signal levels at various component outputs during one cycle of operation is included in that figure. A JK type flip flop is clocked by the 1 to 0 transition of the status line when both of the digital conversions are complete. Since the J input is held high and the K input is held low, the $\overline{Q}$ output of the flip flop is forced low enabling the 7490 decade counter. The counter begins counting the 1 to 0 transitions of the 420 Khz clock connected to its A input. A 7445 decimal decoder is attached to the counter's output lines. As the counts proceed, the decoder output corresponding to the decimal value of the count is forced low for the duration of that count, which is 2.38μs. The output from line two of the decoder is inverted and serves as the latch clock pulse. The output from line 3 of the

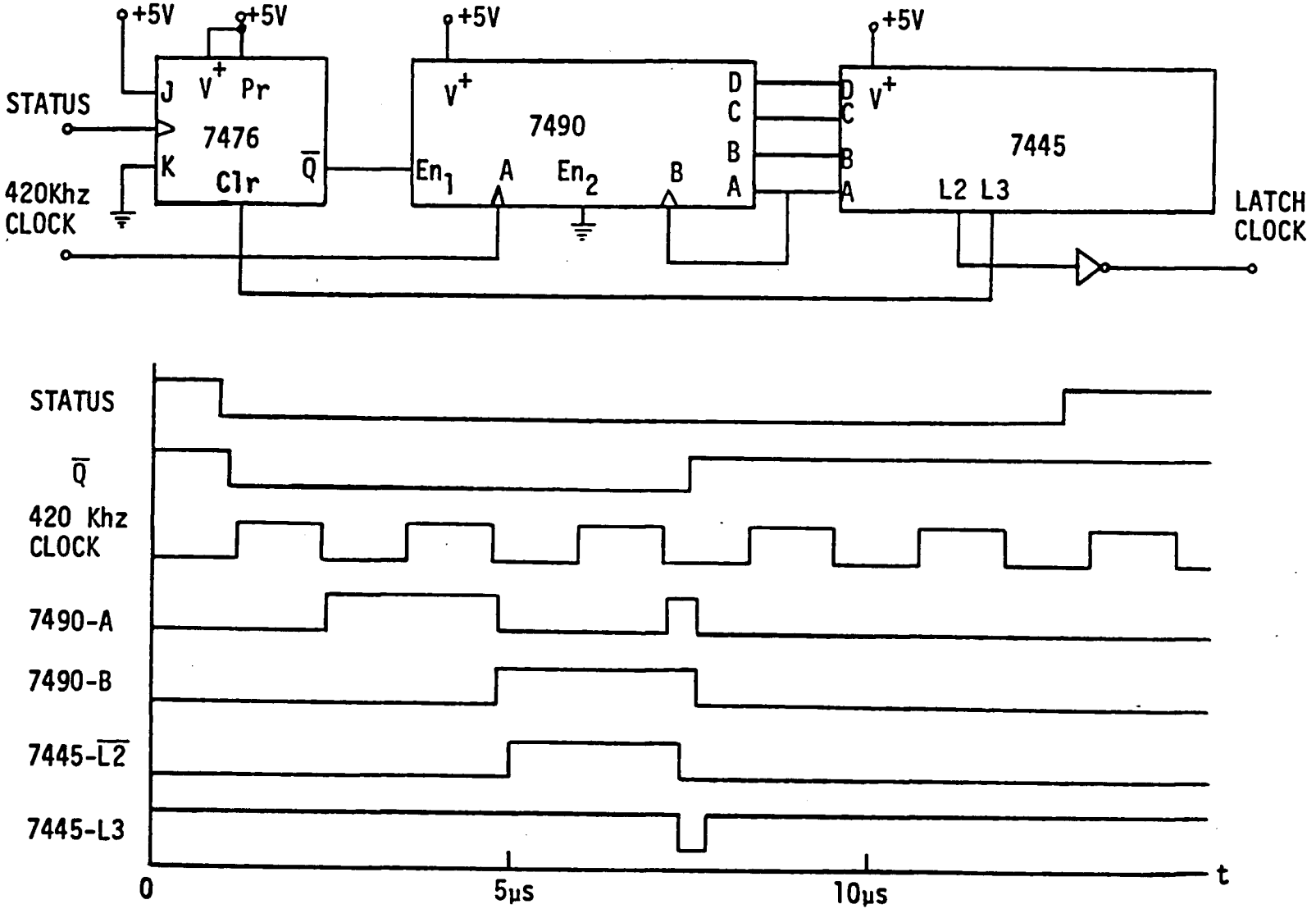


FIGURE 24 Circuitry to generate a latch clock pulse with the corresponding timing diagram.

decoder is used to clear the JK flip flop which disables the counter and resets it to zero. No further actions occur until the next 1 to 0 transition of the convertors' status line, at which time the cycle repeats. The latch clock pulse is therefore generated on the second 1 to 0 transition of the 420 Khz clock.

By examining the timing diagram, the delay between the convertor's status transition and the leading edge of the latch clock pulse can be determined. Since the convertor's status transition and the 420 Khz clock are independent signals, the first 1 to 0 420 Khz clock transition can occur from 0 to 2.38μs after the 1 to 0 status transition. However, the second 1 to 0 420 Khz clock transition must occur 2.38μs after the first. Therefore, the delay between the status transition and the latch clock pulse may vary from 2.38μs to 4.76μs. Since every value in this range of delay times is greater than 700ns, there is definitely sufficient time for all the required operations to be performed before the latch clock pulse occurs.

3.12 Scaling to a Distance Measurement

When 16 samples have been summed, the 16 bit binary output from the accumulator is divided by 16 to provide the averaged value of ϕ to be scaled to a distance measurement and displayed. This division is easily accomplished digitally by shifting the

binary point of the output four positions to the left, as each shift represents division by 2. To accomplish this shift in hardware, the four lower bits of the sum are discarded and the fifth bit becomes the new least significant bit. Since the remainder is discarded, the 12 bit quotient produced is the greatest binary integer after division by 16, with no roundoff. This quotient then represents the averaged value of ϕ.

The final operation to be performed is the scaling of the averaged value of ϕ to a distance measurement for display. As shown in Figure 25 a 7493 4 bit counter counts the trailing edges of the latch clock pulses to determine when 16 samples have been accumulated. When 16 counts have occurred, the D output of the counter clocks a JK flip flop which begins the timing sequence for the scaling operation. The averaged value of ϕ is presented as shown in Figure 26 to the X input of a 12 bit by 12 bit TRW model MPY-12AJ parallel two's complement multiplier. The predetermined constant required for proper scaling is provided at the Y input of the multiplier by setting the constant select switches. The product from the multiplier represents the distance measurement proportional to ϕ. The multiplier truly only performs an 11 by 11 bit multiplication since the sign bits of the inputs need only be exclusively or-ed to produce the product sign bit. Therefore, only the eleven highest order bits of the averaged

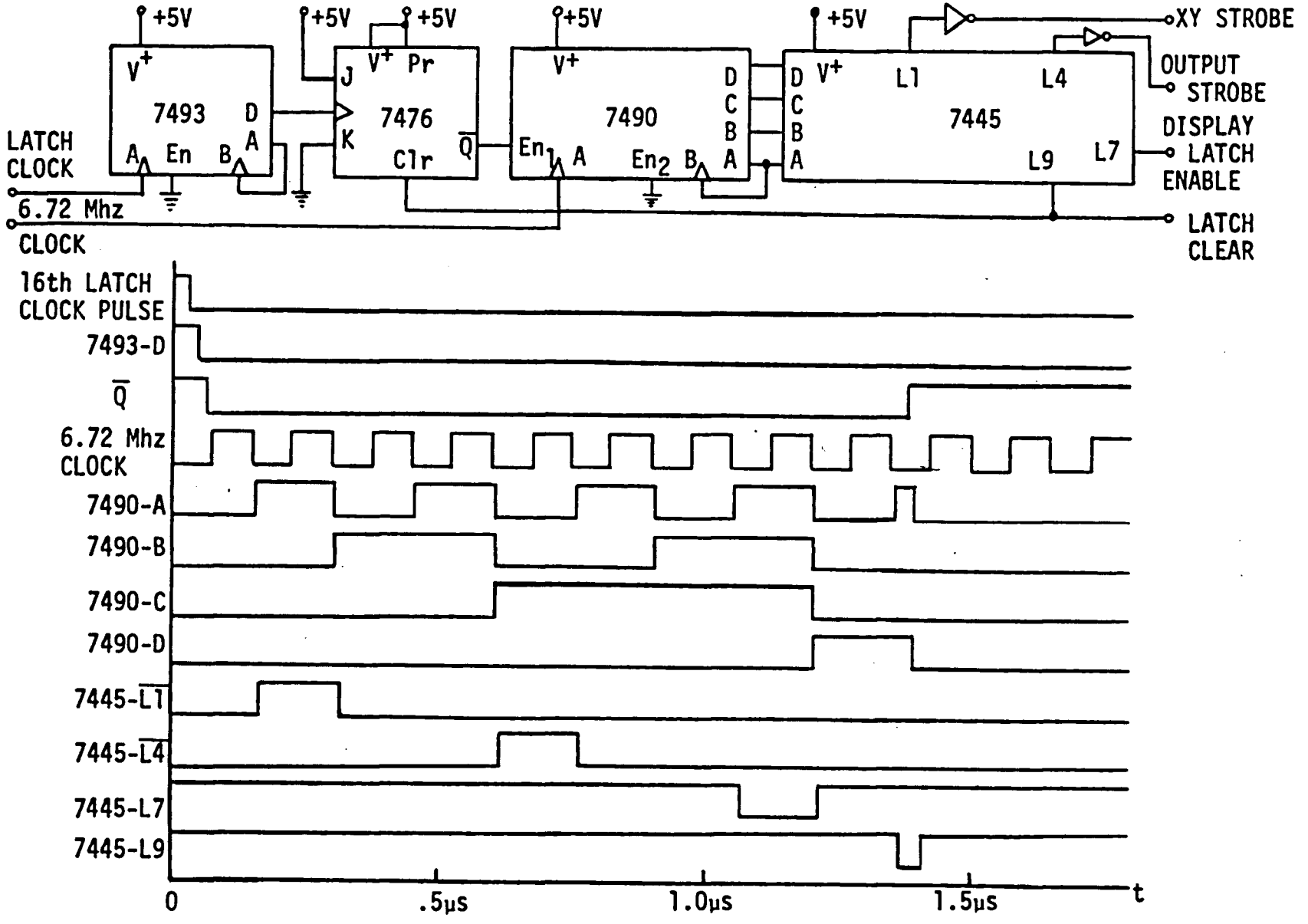


FIGURE 25 Circuitry to generate remaining timing signals and corresponding timing diagram.

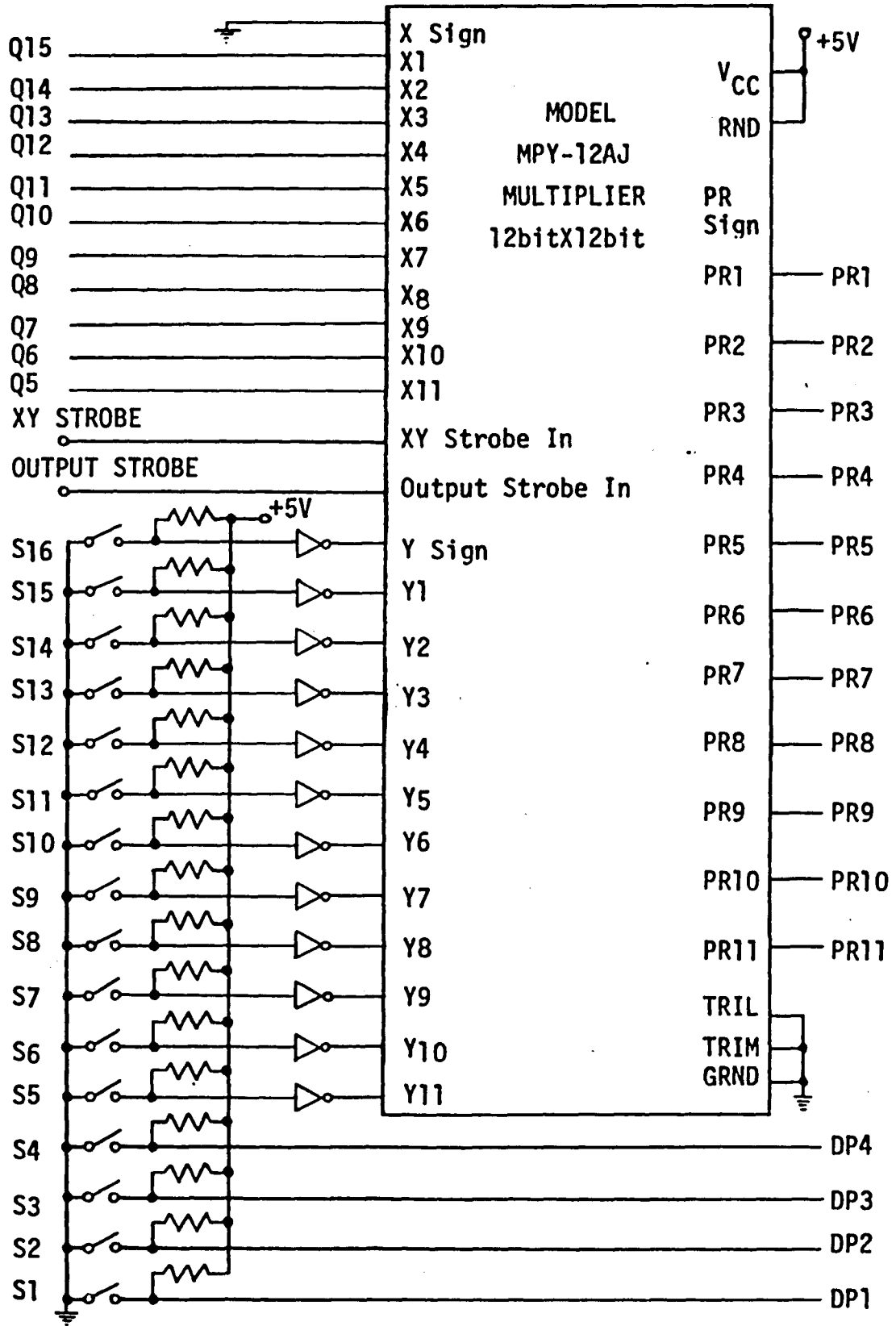


FIGURE 26 Digital multiplier configuration with constant select.

value of ϕ can be input to the multiplier. The least significant bit is neglected. The output from the multiplier will therefore only contain 11 valid bits.

The multiplier requires an XY input strobe to latch the data presented at the X and Y inputs and a product output strobe to supply the resulting product on its output lines. These strobes are generated by the remaining circuitry shown in Figure 25 in a manner similar to the one used to create the latch clock pulse. Once the JK flip flop is clocked, the 7490 decade counter is enabled by $\overline{Q}$ and begins counting 1 to 0 transitions of the 6.72 Mhz clock input. On the first count, the 7445 decoder output line 1 goes low for the 149ns duration of the count, generating after inversion a 149ns positive pulse for the XY strobe input on the multiplier. On the rising edge of that pulse, the X and Y input data are strobed in and multiplication begins. The multiplier requires 150ns to complete the multiplication operation. To insure the multiplier adequate time to perform the operation, the inversion of decoder output line 4, which is a 149ns positive pulse occurring 447ns after the XY input strobe, is used as the output strobe. On the rising edge of this output strobe, the product data begin to appear on the multiplier's output lines and are valid after a maximum delay of 50ns.

The scaling constant is specified to the multiplier in fractional two's complement format. This format was chosen because

it is the best way to accomodate a wide range of possible scaling constants with minimum effort. The first bit position in the constant is for the sign. The remaining 11 bit positions represent negative powers of 2 starting with 2^{-1} in the first position after the sign and ending with 2^{-11} in the last position. These 12 bits can therefore represent decimal fractions from 0 to ±0.9995 in increments of approximately 0.0005. Section 3.14 details the procedure for selecting the appropriate constant.

3.13 Display of Distance Measurement

The output data are now a binary representation of the measurement to be displayed. However, the Hewlett-Packard model 5082-7300 LED numeric indicators chosen for display require a binary coded decimal (BCD) input format. Therefore, the multiplier output data are converted from binary to the BCD format by eight 74185A binary to BCD convertor integrated circuits as shown in Figure 27.[5] The coded data are then displayed on the LED indicators.

These indicators require a negative latch enable pulse of at least 120ns to update the display for each new data input. The enable pulse must occur at least 250ns after the multiplier's output strobe to allow for all the intervening propagation delays. This enable pulse is provided as shown back in Figure 24 by the 7445 decoder output line 7, which produces a negative 149ns pulse

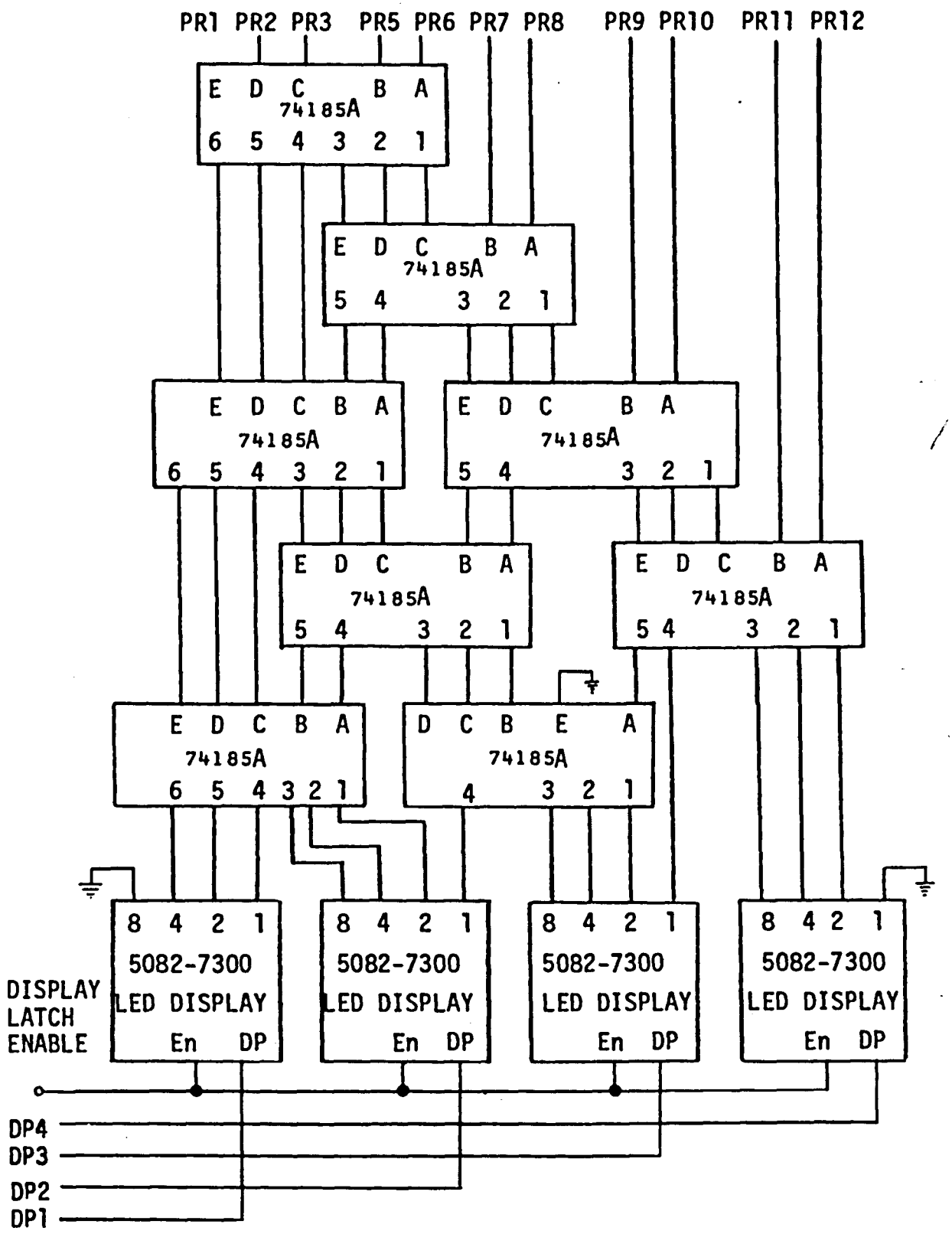


FIGURE 27 Binary to BCD conversion and display circuitry.

447ns after the multiplier output strobe. Once the display has been latched, the system is initialized to accept the first of the next sixteen samples by clearing the accumulator. This is accomplished by the 1 to 0 transition of the 7445 decoder output line 9, which is connected to the clear inputs of the flip flops in the accumulator's latch. That transition also clears the JK flip flop controlling the counter and decoder that generate the 149ns pulses. When that flip flop clears, the counter is disabled, resets to zero, and remains in that state until another sixteen samples have been accumulated. Since it takes 607μs to accumulate sixteen samples for display, the display is updated once every 607μs. Thus, 1,647 measurements are displayed per second.

3.14 Constant Selection

As previously mentioned and shown in Figures 26 and 27, the constant required to scale the angle measurement to a distance measurement is determined by the positions of the sixteen constant select switches S1 through S16. Four of those switches, S1 to S4, are each connected to the decimal point input of one of the four LED indicator's and therefore control the location of the decimal point in the displayed measurement. Turning on one of these four switches lights the decimal point in the corresponding

indicator. The remaining twelve switches, S5 through S16, determine the binary constant for scaling. Each switch corresponds to one of the 12 bit positions of the constant. Switch S16 sets the sign bit. Switches S15 to S5 consecutively set the bit positions corresponding to 2^{-1} to 2^{-11}. A switch is set on to place a 1 in its corresponding bit position, and is set off to place a 0 there.

The following scheme is used to determine the proper value of the scaling constant and therefore the proper positions for the constant select switches. For a measurement to be displayed as a distance, the wavelength λ of the modulating microwave frequency must be known. Due to reflection from the target, the phase of the received signal will go through a full 360° for every distance change of $.5\lambda$. Therefore, 360° corresponds to a distance of $.5\lambda$ A full 360° is represented by the digital output $1000000000000_{(2)}$ or $4096_{(10)}$ from the phase measurement system. Therefore, the conversion factor, in base ten, from degrees to distance is given by the ratio $\frac{.5\lambda}{4096}$. This ratio is converted to a binary fraction and switches S15 to S5 are set accordingly. Since the constants are always considered to be positive, S16 is always off. The decimal point is located after the fourth digit, so S4 is on. The units of length of the measurement agree with the units used to specify λ. Note that the actual phase measurement itself can be

displayed by specifying λ as 720mm and interpreting the displayed result in degrees.

If the decimal ratio turns out to be less than .1, it can be multiplied by 10 before conversion to a binary fraction in order to more fully utilize the available bits in the binary fraction. The displayed measurement can then be divided by ten by shifting the decimal point to the left by one digit to obtain the original ratio. This means turning on S3 instead of S4 when setting the constant select switches. If the decimal ratio is less than .01, it can be multiplied by 100 before conversion. The displayed measurement is divided by 100 by turning on S2 instead of S4. If the decimal ratio is less than .001, it can be multiplied by 1000 before conversion, with S1 turned on instead of S4 to divide by 1000.

As an example, the scaling constant for a microwave modulation with a 76mm wavelength is determined. The scaling constant for this wavelength is given by $\frac{(.5)(76)}{4096}$ = .009277mm/°. Since .009277 is less than .01, it is multiplied by 100 before conversion to a binary fraction to make maximum use of the available bits for scaling. The decimal fraction .9277 is then converted to the binary fraction $.11101101100_{(2)}$. The switches S15 to S5 are therefore set as follows: S15 on, S14 on, S13 on, S12 off, S11 on, S10 on, S9 off, S8 on, S7 on, S6 off, S5 off. The fraction

is considered positive, so S16 is off. Since the fraction is multiplied by 100 before conversion, S2 is the correct decimal point switch to turn on to properly locate the decimal point in the displayed measurement. With the constant select switches set in this manner, the display indicates the measured distance in millimeters for a 76mm wavelength microwave modulation.

4. Theoretical System Performance

4.1 System Accuracy

The accuracy of a measurement made by the previously described system is determined primarily by the accuracy of the analog multipliers used for the crosscorrelation and ratio formation. Analog multipliers possess nonlinearities which cannot be trimmed out by external means, resulting in errors in their output signals. The following analysis is to determine the accuracy of the phase measurement system for the worst case situation.

The Analog Devices model 429B multipliers have a maximum irreducible output error of .3% of full scale, or 30mV, for input levels on the order of 10v. For input levels less than 7 volts, this error decreases with decreasing signal, and is approximately given by the relationship $f(V_X,V_Y) \approx |V_X|E_X + |V_Y|E_Y$, where V_X and V_Y are the X and Y input voltage levels and E_X and E_Y are the

linearity errors associated with the X and Y inputs, expressed in percent of full scale. For the 429B multiplier, $E_X = E_Y = .2\%$ maximum. Since the outputs from two multipliers are added to perform harmonic cancellation of the 840 Khz terms, the 30 mV maximum errors from each multiplier add to a total 60mV error in each sum. Therefore, the division of each signal by the other to produce the ratios $-10 \frac{\sin\phi}{|\cos\phi|}$ and $-10 \frac{\cos\phi}{|\sin\phi|}$ has a 120mV error associated with it. In addition, the analog dividers producing these ratios have irreducible output errors due to the nonlinearities of the Zeltex ZM606 multipliers. The ZM606 multiplier has an irreducible output error of .25% of full scale, or 25mV. However, when configured as a divider, that error increases with decreasing denominator voltage by approximately $\frac{10}{|V_X|}$, where V_X is the denominator voltage. Since a quotient is only chosen when its denominator's magnitude is between 7.07 and 10.0 volts, the largest value for the expression $\frac{10}{|V_X|}$ is $\frac{10}{7.07} = 1.41$. Therefore, the output error from the analog divider is 35mV maximum. The total worst case error in each ratio signal is then 155mV, or approximately 1.5% of full scale output.

The slope of the inverse function used to recover ϕ has a maximum value of 1. Hence, a 1.5% error in the above ratios will result in a 1.5% error in the angle ϕ in the worst case. This translates to a 1.4° uncertainty in the angle ϕ. Assuming a 38mm

half wavelength for the microwave modulating frequency, the corresponding uncertainty in distance is 0.15mm.

If a low pass filter is used instead of harmonic cancellation to eliminate the 840 Khz terms, the accuracy figure is improved since the summation of two multiplier outputs is no longer necessary. The improvement in accuracy will be determined for the same worst case situation just analyzed. The lowpass filter scheme again has the initial 30mV error due to the 429B analog multipliers. After lowpass filtering, the divisions which produce the two ratio signals each have a 60mV maximum error in their quotients. The analog dividers performing those divisions again have the additional 35mV error in their outputs due to the ZM606 multipliers. Hence, the total worst case error in the ratio signals for the lowpass filtering scheme is 95mV. This results in an angle uncertainty of .86° and a distance uncertainty of 0.09mm for a 38mm half wavelength microwave modulation.

There are also errors associated with the analog to digital conversions and other digital operations comprising the remainder of the phase measurement system. As shown below, however, the effects on total system accuracy by these errors are small compared to those of the analog multipliers. Each analog to digital convertor has a maximum differential nonlinearity error of ±1 least significant bit (LSB) or ±4.9mV, and a quantization error

of $\pm\frac{1}{2}$ LSB or ±2.45mV. This differential nonlinearity leads to a maximum additional uncertainty of .04° in the phase angle ϕ, which is negligible compared to the uncertainties due to the analog portion of the system. The quantization error of $\pm\frac{1}{2}$ LSB indicates the resolution to which the analog voltage can be uniquely digitized. The specified ±2.45mV value for this error corresponds to ±.01°, indicating that the 12 bit conversion performed could resolve the phase angle to within .02°. However, since the accuracy due to the analog circuitry is on the order of 1%, resolution of the phase angle to .1° ±.05° by the digital portion of the system is sufficient.

The lookup table and arithmetic logic units do specify the phase angle to .1° ±.05°. However, the greatest integer division involved in the averaging operation always rounds down so that the final accuracy to which the digital portion of the system can specify the phase angle is .1° + .1°. The display is only specified to .2° + .2° because the least significant bit from the accumulator cannot be used by the digital multiplier when scaling. If this multiplier were replaced by a true 12 bit by 12 bit multiplier, the display accuracy would also be to .1° + .1°.

4.2 Effect of Noise on Distance Measurement

The presence of noise in the received signal will cause some deviations in the displayed distance measurement. An estimate of how the mean square deviation of displayed measurements relates to the signal to noise ratio of the received signal will now be determined. Methods to decrease that mean square deviation, thereby improving detector performance, will then be investigated.

The noisy received signal from the photomultiplier tube is first passed through a narrowband predetection filter of bandwidth Δf, centered at the frequency ω of the desired incoming sinusoid. This bandwidth Δf is much smaller than ω, so that the output of the filter is the desired signal, $X_o \cos(\omega t-\phi)$, and narrowband noise. Since the narrowband noise is a Gaussian random process, it can be expressed as $x(t) \cos\omega t - y(t) \sin\omega t$,[6] where $x(t)$ and $y(t)$ are the randomly varying amplitudes of the quadrature noise components. The noise component can also be rewritten as $c(t) \cos(\omega t+\psi(t))$ where $c(t)$ and $\psi(t)$ are the randomly varying amplitude and phase of the noise component. The expressions relating $c(t)$ and $\psi(t)$ to $x(t)$ and $y(t)$ are $c(t) = [x^2(t)+y^2(t)]^{1/2}$ and $\psi(t) = \tan^{-1} \frac{y(t)}{x(t)}$. The variance σ^2 of the random variables $x(t)$, $y(t)$, and $c(t)$ is given by $\sigma^2 = \overline{x^2(t)} = \overline{y^2(t)} = \frac{\overline{c^2(t)}}{2} = W\Delta f$.[7,8] Here $W\Delta f$ is the noise power over the

Δf bandwidth. The signal to noise ratio of the received signal after predetection narrowband filtering is given by $\frac{X_o^2}{2W\Delta f}$, where $\frac{X_o^2}{2}$ is the power of the $X_o \cos(\omega t+\phi)$ signal.

The detector forms a signal proportional to $\cos\phi$ by first multiplying the received signal, $X_o \cos(\omega t+\phi) + c(t) \cos(\omega t+\psi(t))$, by $\cos\omega t$ to obtain the first product for summation. The received signal is also phase shifted by 90°, forming $X_o \sin(\omega t+\phi) + c(t) \sin(\omega t+\psi(t))$, which is multiplied by $\sin\omega t$ to obtain the second product for summation. Since Δf is much smaller than ω, it is assumed that the phase shifter simply shifts the noise component as well as the signal component by 90° and does not alter the statistical properties of $c(t)$ or $\psi(t)$. The summation of the two products produces the signal $x = X_o \cos\phi + c(t) \cos\psi(t)$. The variance of this signal x is equal to the variance of $c(t) \cos\psi(t)$. Assuming that $\psi(t)$ is uniformly distributed over the interval 0 to 2π radians, the variance of $c(t) \cos\psi(t)$ is $\frac{c^2(t)}{2}$ or $W\Delta f$. Therefore, the variance of x is $W\Delta f$. By similar analysis; the other signal formed by the detector proportional to $\sin\phi$ is $y = X_o \sin\phi + c(t) \sin\psi(t)$. This signal y has the same variance as x, namely $W\Delta f$. Since the components $c(t) \cos\psi(t)$ and $c(t) \sin\psi(t)$ are essentially noise variations in the $\cos\phi$ and $\sin\phi$ signals, the signals x and y will now simply be written as $x = X_o \cos\phi$ and $y = X_o \sin\phi$ with the understanding that each signal

has a variance $W\Delta f$ due to the noise component.

These functions are combined to form the tangent of ϕ for table lookup. Therefore, changes in ϕ due to changes in $\tan\phi$ must be determined to relate deviations in ϕ back to the variances of x and y. Since $\frac{d(\tan\phi)}{d\phi} = \frac{1}{\cos^2\phi}$,

$$d\phi = \cos^2\phi \; d(\tan\phi)$$

Let $Z = \tan\phi = \frac{y}{x} = \frac{X_o \sin\phi}{X_o \cos\phi} = \frac{Y}{X}$, where $Y = \sin\phi$ and $X = \cos\phi$.

Then, $d\phi = \cos^2\phi \; dZ$

Now, $dZ = d(\frac{Y}{X}) = (\frac{-Y}{X^2})dX + \frac{1}{X} dY$

Since the deviations in X and Y due to noise, dX and dY, are uncorrelated,

$$(dZ)^2 = (\frac{-Y}{X^2} dX)^2 + (\frac{1}{X} dY)^2$$

Since the variances of dX and dY are equal,

$$(dX)^2 = (dY)^2$$

Then, $d\phi = \cos^2\phi \; dZ = \cos^2\phi \; \sqrt{(\frac{-Y}{X^2} dX)^2 + (\frac{1}{X} dY)^2}$

$$d\phi = \cos^2\phi \sqrt{\frac{Y^2}{X^4} (dX)^2 + \frac{1}{X^2} (dY)^2}$$

$$d\phi = \cos^2\phi \sqrt{\frac{Y^2}{X^4}(dX)^2 + \frac{1}{X^2}(dX)^2}$$

$$d\phi = \cos^2\phi \sqrt{\frac{Y^2}{X^4} + \frac{1}{X^2}}\, dX \qquad \text{but } Y = \sin\phi$$

$$X = \cos\phi$$

$$d\phi = \cos^2\phi \sqrt{\frac{\sin^2\phi}{\cos^4\phi} + \frac{1}{\cos^2\phi}}\, dX$$

$$d\phi = \sqrt{\sin^2\phi + \cos^2\phi}\, dX$$

$$d\phi = dX$$

The variance of ϕ is the same as the variance of the original received signal. Therefore, the mean square deviation, in degrees, of ϕ is given by $\sigma_\phi = 4.5 \quad W\Delta f$, where 4.5 is the voltage to angle conversion factor. The mean square deviation in distance is given by $\sigma_D = \frac{\lambda}{16} \quad W\Delta f$, where $\frac{\lambda}{16}$ is the conversion factor from voltage to distance and λ is the wavelength of the microwave modulating signal. The units of σ_D are those of λ.

As can be seen from this result, the mean square deviation in the distance measurement can be decreased by decreasing the bandwidth Δf. One way to effectively accomplish this decrease is to lowpass filter either the x and y signals or the $\tan\phi$ and $\cot\phi$ signals with a cutoff frequency f_o which is less than half the original Δf bandwidth. The mean square deviation in distance, as a function of f_o, is then given by $\sigma_D = \frac{\lambda}{16} \quad Wf_o$. Decreasing

f_o decreases σ_D at the expense of the time required to make a measurement.

Alternatively, the x and y signals or the tanϕ and cotϕ signals can be sampled and averaged in a digital manner. The magnitude of the impulse response for such a technique, as derived in the appendix, is given by

$$|H(\omega)| = \frac{1}{N} \left| \frac{\sin \frac{N\omega T}{2}}{\sin \frac{\omega T}{2}} \right|$$

where N is the number of samples and T is the time between samples. This magnitude response, shown in Figure , has a lowpass filter characteristic, with an effective cutoff frequency f_o generally considered to be that of the first zero, $\frac{1}{NT}$. Again, this f_o should be less than half of the Δf bandwidth of the predetection filter to significantly decrease the noise bandwidth. The mean square deviation in the distance measurement using this technique is given by

$$\sigma_D = \frac{\lambda}{16} \frac{W}{NT}.$$

In this case, σ_D can be decreased by increasing the number of samples or by increasing the time between samples, or both.

For the sampling scheme used in the previously described phase detector, the values of N and T are 16 and 37.95μs respectively. Therefore, the sample and averaging for the display has

an equivalent f_o of 1.647 Khz.

5. Conclusions

The system accuracy of this phase measureing subsystem is primarily determined by the analog multipliers. To significantly increase the system accuracy without affecting measurement speed, multipliers with smaller nonlinearity errors must be used. Alternatively, if measurement speed may be sacrificed, system accuracy can be increased by using low pass filters instead of harmonic cancellation to eliminate the undesired high frequency components. System accuracy increases because only two analog multipliers are required to implement the crosscorrelation if low pass filters are used, but four analog multipliers are required if harmonic cancellation is used.

The mean square deviation in the distance measurement due to noise in the received signal can be decreased by additional filtering to decrease the noise bandwidth Δf. This filtering may either be done before the detector by narrowing the bandwidth of the bandpass predetection filter or after the detector by low pass filtering the detector outputs. A smaller Δf or f_0 results in a smaller mean square deviation in the distance measurement at the expense of speed. Alternatively, the detector output can be digitally sampled and those samples averaged to decrease the mean square deviation. With the digital technique, increasing the number of samples taken for averaging or increasing the time period between samples decreases the mean square deviation. A combination

of both techniques may prove best to optimize the speed versus accuracy trade-off.

Due to the high speed at which the distance measurements are made, it would not be feasible to incorporate a microprocessor into this subsystem to perform any of the functions currently done by digital hardware. However, a microprocessor could be added to the subsystem to provide a means for storing the distance measurements or communicating them to a computer for further processing. A microprocessor could also be used in conjunction with a frequency counter to automatically specify the scaling constant for the distance measurement. By monitoring the frequency of the modulating microwave signal, the microprocessor could generate the appropriate information for scaling. If the frequency of the modulating microwave signal changed, the microprocessor would update the scaling constant to keep the displayed distance measurements accurate.

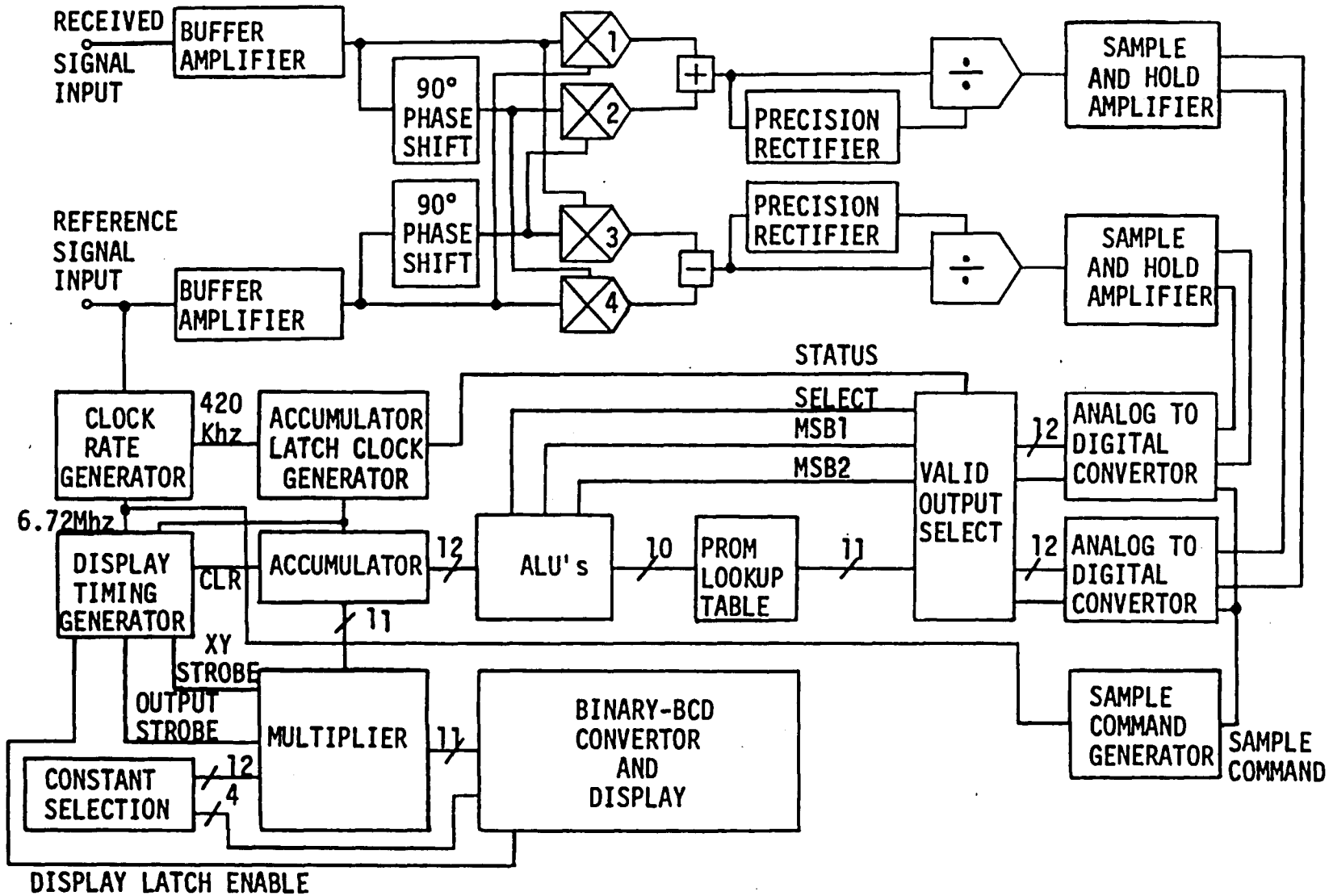


FIGURE 28 Functional block diagram of the phase measurement subsystem.

Appendix

1. Crosscorrelation between the received and reference signals. The crosscorrelation function for two periodic signals $f_1(t)$ and $f_2(t)$ is given by the expression

$$\bar{X}_{12}(\tau) = T \int_{-\frac{T}{2}}^{\frac{T}{2}} f_1(t) f_2(t-\tau) dt$$

Let $f_1(t) = a \cos(\omega t+\theta) + n(t)$ be the received signal and $f_2(t) = b \cos(\omega(t-\tau)+\theta)$ be the reference signal. Then

$$\bar{X}_{12}(\tau) = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} [a \cos(\omega t+\theta)+n(t)] [b \cos(\omega(t-\tau)+\theta)] dt$$

$$= \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} a \cos(\omega t+\theta)\ b \cos(\omega(t-\tau)+\theta) dt +$$

$$\frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} n(t) b \cos(\omega(t-\tau)+\theta) dt$$

Since the signal and the quantum noise are uncorrelated, the second integral is zero for all τ. Therefore,

$$\bar{X}_{12(\tau)} = \frac{ab}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \cos(\omega t+\theta) \cos(\omega(t-\tau)+\theta) dt + 0$$

$$= \frac{ab}{2T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \cos(2\omega t+2\theta-\omega\tau)dt + \frac{ab}{2T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \cos(\omega\tau)dt$$

$$= \frac{ab}{4\omega T} \sin(2\omega t+2\theta+\omega\tau)\Big|_{-\frac{T}{2}}^{\frac{T}{2}} + \frac{ab}{2T} t \cos(\omega\tau)\Big|_{-\frac{T}{2}}^{\frac{T}{2}}$$

$$= \frac{ab}{4\omega T} [\sin(\omega T+2\theta+\omega\tau) - \sin(-\omega T+2\theta+\omega\tau)] + \frac{ab}{2T} [\frac{T}{2}+\frac{T}{2}] \cos(\omega\tau)$$

Since $\omega T = 2\pi$,

$$\bar{X}_{12}(\tau) = \frac{ab}{4\omega T} [\sin(2\pi+2\theta+\omega\tau) - \sin(-2\pi+2\theta+\omega\tau)] + \frac{ab}{2T} T \cos(\omega\tau)$$

$$= \frac{ab}{4\omega T} [\sin(2\theta+\omega\tau) - \sin(2\theta+\omega\tau)] + \frac{ab}{2} \cos(\omega\tau)$$

$$= 0 + \frac{ab}{2} \cos(\omega\tau)$$

Since $\phi = \omega\tau$,

$$\bar{X}_{12}(\tau) = \bar{X}_{12}(\phi) = \frac{ab}{2} \cos\phi$$

2. Derivation of $|H(\omega)|$ for digital sampling and averaging.
The digital scheme of sampling a signal and averaging N of those samples together can be modeled as a delay line type filter, with N taps summed together, each with unity weight. The output from the summation is divided by N to obtain the average. This model is pictured in Figure 29.

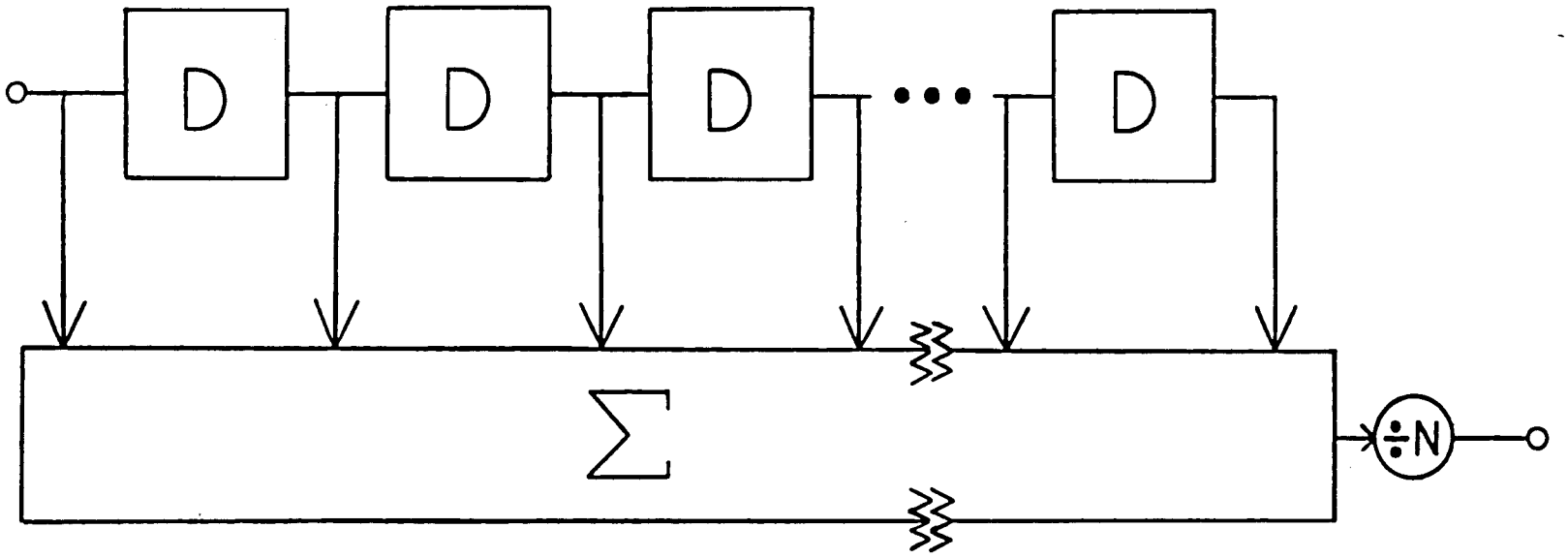


Figure 29 A tapped delay line filter model of digital sampling and averaging.

The impulse response of this structure is given by

$$h(t) = \frac{\delta(t) + \delta(t-T) + \ldots + \delta(t-(N-1)T)}{N}$$

The Fourier transform of h(t) is

$$H(\omega) = \frac{1}{N}\left(1 + e^{-j\omega t} + \ldots + e^{-j(N-1)\omega T}\right)$$

The finite sum in parenthesis can be written as

$$\frac{1 - e^{j\omega NT}}{1 - e^{j\omega T}} . \quad \text{Therefore,}$$

$$H(\omega) = \frac{1}{N}\frac{1 - e^{j\omega NT}}{1 - e^{j\omega T}}$$

$$H(\omega) = \frac{1}{N}\frac{e^{-j\frac{N}{2}\omega T}}{e^{-j\frac{1}{2}\omega T}}\frac{e^{j\frac{N}{2}\omega T} - e^{-j\frac{N}{2}\omega T}}{e^{j\frac{1}{2}\omega T} - e^{-j\frac{1}{2}\omega T}}$$

$$H(\omega) = \frac{1}{N}\frac{e^{-j\frac{N}{2}\omega T}}{e^{-j\frac{1}{2}\omega T}}\frac{\sin\frac{N}{2}\omega T}{\sin\frac{1}{2}\omega T}$$

$$|H(\omega)| = \frac{1}{N}\frac{|\sin\frac{N}{2}\omega T|}{|\sin\frac{1}{2}\omega T|}$$

$|H(\omega)|$ is then the magnitude of the impulse response of this digital sampling and averaging system. A plot of $|H(\omega)|$ appears in Figure 30.

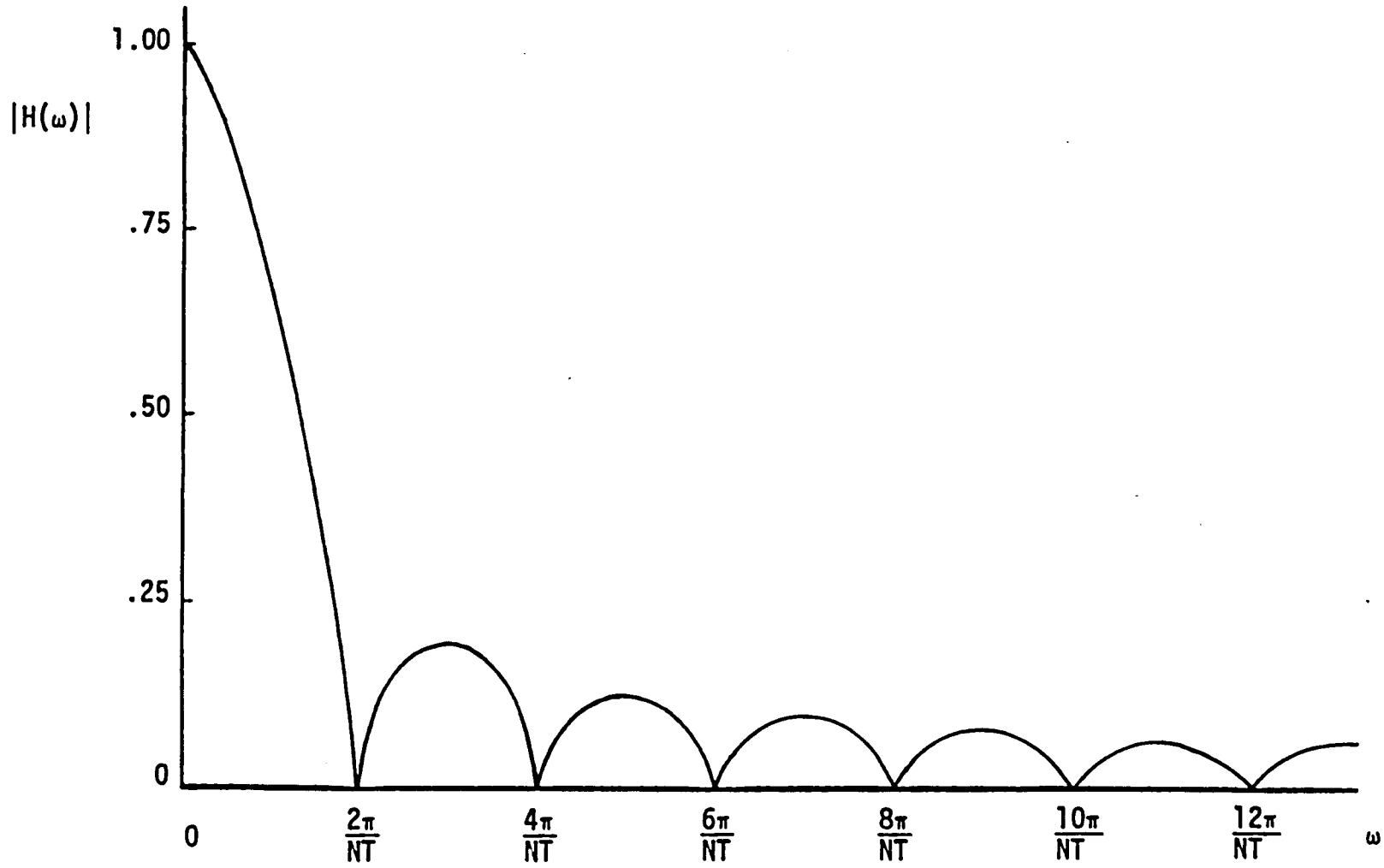


Figure 30 Magnitude of the impulse response of the tapped delay line filter of Figure 29.

References

1. "Design Study of a Lidar System for Close Range Distance Measurement", A Thesis by John R. Regazzi, Lehigh University, 1979.

2. "Light Modulators at 4 Ghz For Continuous Wave Short Range Lidar", A Thesis by Robert T. O'Hara, Lehigh University, 1979.

3. Wozencraft, J.M. and Jacobs, I.M., Principles of Communication Engineering, New York: John Wiley and Sons, Inc., 1965, p. 212.

4. Lathi, B.P., Signals, Systems and Communications, New York: John Wiley and Sons, Inc., 1965, pp. 515-529.

5. National Semiconductor TTL Data Book, Santa Clara, California: National Semiconductor Corporation, 1976, pp. 2-121.

6. Whalen, Anthony D., Detection of Signals in Noise, New York: Academic Press, Inc., 1971, p. 75.

7. Ziemer, R.E. and Tranter, W.H., Principles of Communications: Systems, Modulation, and Noise, Boston: Houghton Mifflin Company, 1976, pp. 272-273.

8. Rice, S.O., "Mathematical Analysis of Random Noise", The Bell System Technical Journal, Vol. 24, 1945, p. 48.

Vita

Carl John Haslett was born in Altoona, Pennsylvania on March 30, 1955. He is the son of Thomas E. and Patricia A. Haslett of Altoona. He graduated with honors from Lehigh University in May, 1977 with a Bachelor of Science degree in Electrical Engineering. He has been employed for the past three years by the Department of Electrical Engineering at Lehigh University as a teaching assistant initially and most recently as a research assistant. He is a member of the Broadcast, Cable, and Consumer Electronics Society of IEEE, and is also a member of the Eta Kappa Nu and Tau Beta Pi honoraries.