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Purwar, Ansha

**TITLE:**

# Characterization of Sonos Nonvolatile Semiconductor Memory Devices with Atomic Force Microscopy

**DATE:** May 28, 1995

# CHARACTERIZATION OF SONOS NONVOLATILE SEMICONDUCTOR MEMORY DEVICES WITH ATOMIC FORCE MICROSCOPY

by
Ansha Purwar

A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in
Electrical Engineering

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This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science.

May 6th, 1995
(date)

Dr. Marvin H. White
Thesis Advisor

Dr. Alastair D. McAulay
Chairman of Department

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# List of Symbols

Si = single crystalline silicon

PECVD = plasma enhanced chemical vapor deposition

LPCVD = low pressure chemical vapor deposition

TEM = transmission electron microscopy

XTEM = cross-sectional Transmission electron microscopy

PTEM = planar Transmission electron microscopy

HPT = hydrogen plasma treatment

PMA = post-metalization anneal

HF-C(V) = high frequency capacitance voltage

LF-C(V) = low frequency capacitance voltage

MOS = metal-oxide-semiconductor

FET = field effect transistor

q = electronic charge, 1.602E-19 (C)

$\epsilon_o$ = permittivity of vacuum, 8.854E-14 (F $\mathrm{cm}^{-1}$)

$\epsilon_s$ = relative permittivity of silicon, 11.7 (dimensionless)

$\epsilon_{ox}$ = relative permittivity of silicon dioxide, 3.9 (dimensionless)

$\epsilon_n$ = relative permittivity of silicon nitride, 7.5 (dimensionless)

$m_o$ = free electron mass, 9.11E-31 (Kg)

h = Planck's constant, 6.625E-34 (Js)

k = Boltzmann's constant, 1.38E-23 (J $\mathrm{K}^{-1}$)

$V_t$ = kT/q = thermal voltage at 300° K, 0.025860 (volt)

T = temperature at Kelvin (K)

$T_G$ = characteristic temperature which is a measure of the exponential density distribution of localized states (K)

$\overline{z}$ = average z height

$x_{eff}$ = Effective dielectric thickness

$x_{ot}$ = Tunnel oxide thickness

$x_{ob}$ = Blocking oxide thickness

$x_N$ = Nitride thickness

$V_{FB}$ = flat band voltage (volt)

$\triangle V_{FB}$ = flat band voltage shift (volt)
$V_G$ = applied gate voltage (volt)
$V_D$ = applied drain voltage (volt)
$V_S$ = applied source voltage (volt)
$V_{sub}$ = applied substrate voltage (volt)
$V_{ox}$ = voltage dropped across the insulator (volt)
$\phi$ = electrostatic potential (volt)
$\phi_s$ = surface potential (volt)
$\phi_{ms}$ = work function difference between metal and semiconductor (volt)
$\sigma$ = sheet conductance ($\Omega$ / $cm^2$)
$C_{eff}$ = Effective capacitance
$C_{ox}$ = oxide capacitance ($F/cm^2$)
$C_s$ = semiconductor capacitance ($F/cm^2$)
$C_{HF}$ = total capacitance of MOS capacitor at high frequency ($F/cm^2$)
$C_{LF}$ = total capacitance of MOS capacitor at low frequency ($F/cm^2$)
$Q_f$ = fixed charge in bulk material ($cm^{-2}$)
$D_{it}$ = interface state density ($cm^{-2}eV^{-1}$)
$N_T(E)$ = localized states density at energy E in the bandgap
$N_C$ = effective density of states of conduction band ($cm^{-3}$)
$N_V$ = effective density of states of valence band ($cm^{-3}$)
$N_{go}$ = localized states density just above the valance band edge
$N_{g'}$ = corrected $N_G$ value for the error of zero Kelvin approximation
$\rho$ = total excess carriers density ($C/cm^3$)
$\rho_c$ = excess density of carriers in the conduction band ($C/cm^3$)
$\rho_v$ = excess density of carriers in the valence band ($C/cm^3$)
$\rho_t$ = excess density of carriers trapped in the localized states ($C/cm^3$)
$\alpha$ = ramp rate
$Q_{gb}$ = Gate to bulk charge
$V_{gb}$ = Gate to Bulk Voltage
$I_g$ = Gate Current
$N_c$ = excess density of carriers in the valance band per unit area
$N_t$ = excess density of carriers trapped in the localized states per unit area
$E_g$ = energy gap at 300K
$E_V$ = bottom energy of valence band

$E_C$ = bottom energy of conduction band

$E_{Vo}$ = $E_V$ under thermal equilibrium condition

$E_{Co}$ = $E_C$ under thermal equilibrium condition

$E_x$ = electric field vertical to the semiconductor-insulator interface

$E_y$ = electric field parallel to the semiconductor-insulator interface

E = the total electric field in the semiconductor

$R_{ave}$ = Average Roughness

$R_{rms}$ = Root Mean Square Roughness

$R_{p-v}$ = Peak to valley Roughness

# Abstract

This thesis deals with the use of Atomic Force Microscopy (AFM) to study nanotopography of scaled SONOS [polysilicon - blocking oxide - nitride - tunnel oxide - silicon], nonvolatile semiconductor memory (NVSM) devices. The SONOS device consists of the ONO dielectric where the ultrathin tunnel oxide is 1-2 nm, the memory nitride is 5-7 nm and the blocking oxide is 3-5 nm. The tunnel oxide is thermally grown and thus is fairly uniform across the surface. The silicon nitride layer is deposited by LPCVD and contributes to the maximum surface roughness of the ONO dielectric. The blocking oxide is deposited by LPCVD, over the nitride, and densified.

In the process of scaling the SONOS devices, the variations in the vertical dimension of the multidielectric film gain prominence. The surface roughness of silicon nitride was varied by using different depositions and flow rates. The temperature range used in this thesis was 650° C to 725° C and the flow rates correspond to $NH_3$:$SiCl_2H_2$ ratios of 5:1 and 10:1. To study the nanotopography of the nitride layer, the instrument used in this thesis was the Atomic Force Microscope. The theory of the Scanning Probe Microscope is described with emphasis on the Atomic Force Microscope (AFM). Experimentally, the intermittent contact mode of the AFM works best on the deposited $Si_3N_4$ films. Silicon nitride samples deposited at 650° C with a flow rate of 10:1 had the least root mean square (rms) roughness of 0.33 nm as compared with other samples measured in the intermittent contact or tapping mode. On the other hand, contact mode operation of the AFM yields the least rms surface roughness of 0.17 nm at the temperature of 680° C with a flow rate of 10:1 as compared to other samples measured in the contact mode.

To study the effect of varying surface roughness on the electrical characteristics of a device, gridded and ungridded capacitors have been fabricated both with 12 Å and 18 Å tunnel oxide with $Si_3N_4$ deposited at different temperatures. Linear Voltage Ramp measurements of SONOS devices have been performed to correlate surface roughness, and device programming voltage and flatband voltage shift.

# Chapter 1

# Introduction

SONOS (silicon-oxide-nitride-oxide-polysilicon) devices are non volatile memories i.e. they do not lose memory when the power is turned off. SONOS capacitors are fabricated by forming tunnel oxide, storage nitride and blocking oxide as gate dielectric. Metal is then deposited on the above gate dielectric for contact. Extra fabrication steps are required for SONOS transistors due to the formation of source and drain.

A SONOS device fabricated on a p type substrate turns on when a certain positive voltage is applied to it. This voltage is termed as threshold voltage. The device is said to turn on when an inversion layer forms at the surface of the semiconductor. The inversion layer forms a channel in the SONOS transistor and drain current can be measured. The source and drain help supply the electrons in the inversion layer. Some of these electrons tunnel across the thin tunnel oxide and trap in the nitride when a positive gate voltage is applied. This is termed as WRITING of the device. The stored charge changes the threshold voltage of the device. When a negative voltage is applied to the gate of the device, the surface of silicon is accumulated with holes. Some of these holes tunnel to the storage nitride and neutralize the electrons. This is termed as ERASING of the device. Repeated WRITING and ERASING of the device can degrade the characteristics of the device and this is used as a measure of ENDURANCE of the device . The long term ability of the nitride layer to store charge is termed as RETENTION. Fig. 1.1 displays the cross section of a SONOS device [1].

For a SONOS device to be used in semiconductor disk application as EEPROM, more than 1,000,000 cycles of ERASE/WRITE and ten years of retention are required [2]. In DRAM application, due to regular refresh, long term retention is not required.

The gate dielectric of the SONOS device consists of tunnel oxide ($\approx 20$ Å ), storage nitride ($\approx 50$ Å ) and blocking oxide ($\approx 40$ Å ). The tunnel oxide is thermally grown

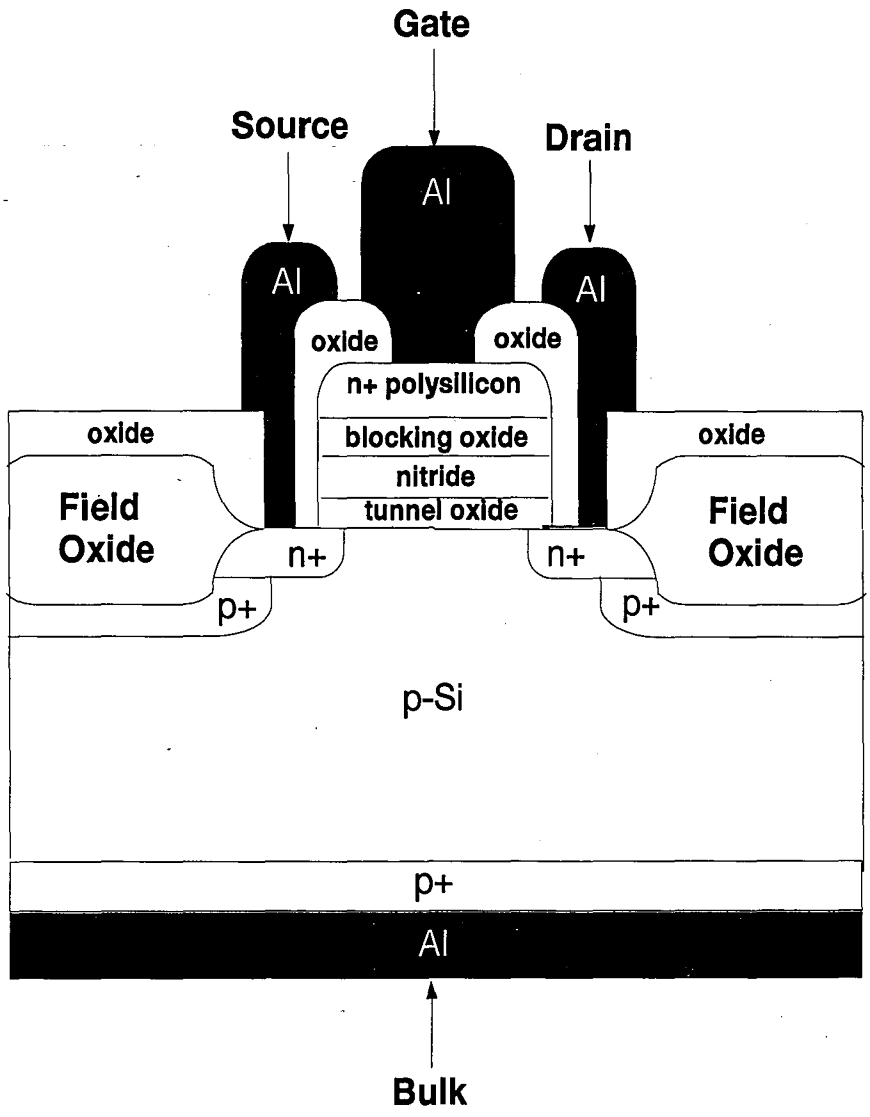

Gate
Source
Drain
Al
Al
Al
oxide
oxide
n+ polysilicon
blocking oxide
nitride
tunnel oxide
oxide
oxide
Field Oxide
Field Oxide
n+
n+
p+
p+
p-Si
p+
Al
Bulk

Figure 1.1: Cross section of a SONOS device

by wet or dry oxidation. At Lehigh University the tunnel oxide Can be grown in either a single wall furnace or in the triple wall furnace. The triple wall furnace yields less interface trap density (Dit) to begin with and the increase in Dit due to repeated ERASE/WRITE cycling is less compared to the single wall furnace [2]. The storage nitride is deposited by Low Pressure Chemical Vapor Deposition (LPCVD). It is a trap rich layer which traps charge in the ERASE/WRITE mode. The blocking oxide is LPCVD deposited and densified in the wet oxidation furnace. This thesis mainly deals with the nitride layer of the gate dielectric.

The nitride layer is important since it traps charge. The WRITE, ERASE, RETENTION operations of the device depend upon trapping of charge in the nitride layer. ENDURANCE of the device depends on the interface layer between silicon and silicon dioxide and the interface between silicon dioxide and silicon nitride. The degradation of tunnel oxide and storage nitride interface lead to problems in retention and endurance of the device. The storage nitride and blocking oxide interface degradation cause a problem in retention due to leakage of charge to the blocking oxide [2].

Previous studies on silicon and silicon dioxide interface show better time dependent dielectric breakdown characteristics if the silicon surface is atomically flat or has lesser surface roughness [3]. With decreasing polished-silicon-surface micro-roughness, the current density decreases. The microscopic uniformity of the top surface (not the silicon silicon dioxide interface) of the oxide grown on this silicon surface is affected by the roughness of the underlying silicon surface. Although this micro roughness is dependent on the roughness of the starting silicon surface, it is also strongly dependent on parameters like oxidation temperature. Gate oxide integrity was also found to be dependent on treatment of silicon surface with DI water and HF [4].

According to Ohmi et al. [5], channel mobility, along with charge to breakdown characteristics and electric field intensity, decrease with increasing silicon micro roughness. The paper found RCA clean ratio of $NH_4OH$:$H_2O_2$:$H_2O$ to be 0.05:1:5 followed by rinsing in DI water improved surface roughness characteristics.

Recently, the surface roughness of the nitride layer in stacked gate dielectric has gained prominence. In the SONOS device, as stated earlier, the ERASE, WRITE, RETENTION and ENDURANCE operations of the device are centered around the nitride layer. Due to scaling of SONOS device and DRAM's, the small variations in the vertical dimensions gain prominence. According to Roy and White [6], the electron tunneling from polysilicon asperities increases with increasing radius of the asperity. Similarly, nitride asperities could affect charge tunneling from the tunnel oxide and charge leakage to blocking oxide. Due to asperities at the silicon dioxide and silicon nitride interface, there could be degradation in retention characteristics due to back tunneling of charge through the oxide. The breakdown characteristics of the dielectric degrade with an increase in surface roughness of the nitride [7].

According to Tanaka et al., the surface roughness of the nitride layer increased due to increasing the deposition temperature. This increase in surface roughness intensified the electric field at certain points in the dielectric. This caused degradation in dielectric breakdown characteristics. Nitride layers deposited at three different temperatures were investigated - 680° C, 700° C, 780 ° C. Other deposition parameters like pressure and flow rates were also varied slightly while varying the temperature. The nitride layer deposited at 680° resulted in the least surface roughness when measured with the AFM and best electrical characteristics as compared to devices with other two deposition temperatures.

The composite ONO film was used to obtain dielectric constant and to suppress the leakage current. The blocking oxide film was important to eliminate electron trapping and to provide improved suppression of interface state generation under electrical stress for high reliability DRAM's [8, 9] and SONOS devices. The blocking oxide was deposited by LPCVD and later densified in the wet oxidation furnace. The strongest contributor to the surface micro roughness of the dielectric was the growth conditions of the nitride.

Currently, in any analysis of SONOS devices, a uniform dielectric thickness is assumed which provides a uniform electric field. The validity of this assumption rests on the surface roughness of the layers that compose the ONO dielectric. The tunnel oxide is thermally grown and the blocking oxide is deposited and densified. The silicon nitride layer is deposited by low pressure chemical vapor deposition (LPCVD). The rms surface roughness of ultra thin tunnel oxide is 0.46 Å and the $Si_3N_4$ is typically 3.3 Å in the contact mode of the AFM. Furthermore, as the SONOS devices are scaled down, the small vertical surface variations have a more prominent role in the analysis and brings into question the uniform thickness assumption. Erase, Read, Write and Retention models for the SONOS device all employ the uniform thickness assumption. Hence, any deviations from this assumption would affect the extracted device parameters and consequently, the validity of the models that describe the operation of the device.

## 1.1 Scope of this Thesis

The goal of this thesis was to study the effect of surface roughness of nitride layer on SONOS device performance with the help of the Atomic Force Microscope [AFM].

The goals for a scaled SONOS device are to obtain [10]

- Low programming voltage.
- Improved retention.
- Higher endurance.
- Faster programming time $t_p$.

An increase in the silicon nitride surface roughness causes

- Enhanced electron injection in MOS and SONOS devices
- Erase, Read, Write of the SONOS device may be affected [uniform injection may make a difference].
- Retention may be affected.

Table 1.1 describes the parameters affected by surface roughness. The most significant roughness to the ONO triple dielectric is contributed by the nitride, the parameters that affect the surface roughness of the nitride are studied. The LPCVD reaction that deposits the nitride is

| Parameters/Surface Roughness | HIGH | LOW |
|---|---|---|
| Low programming voltage | Good | Good/Bad |
| High Retention | Bad | Good |
| High Endurance | Bad[Slow ramping]<br>Good[Cycles] | Good |
| Fast $t_p$ | Good | Good/Bad |

Table 1.1: Effect of Surface Roughness on SONOS parameters

$3\ SiCl_2H_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$

The parameters that can be varied during deposition are:

1. Temperature
2. Flow Rate
3. Pressure
4. Thickness of the Nitride layer (or time of deposition)

The thickness of the nitride layer is usually fixed at $\approx 60$ Å [10], as devices are scaled. Therefore, variations in the thickness are not studied. In this thesis variations in surface roughness due to the first two parameters are studied.

The organization of this thesis is as follows:

In Chapter 2, the theory of Scanning Probe Microscopes (SPM) is described including the Atomic Force Microscope [AFM] in the contact, non contact and tapping mode (or intermittent-contact mode); Lateral Force Microscope [LFM]; Magnetic Force Microscope [MFM] and Scanning Tunneling Microscope [STM]. In Chapter 3, the fabrication sequence of SONOS capacitor for both gridded and ungridded capacitors is presented. The formation of the nitride layer and steps taken to measure the nitride thickness have been discussed. Next, Chapter 4 contains information concerning measurement techniques and experimental data gathered by these techniques.

Chapter 5 presents the conclusion of the work done and makes recommendation for future work. Appendix A describes taking images from the AFM [Park scientific Instrument] and sample preparation for the AFM surface topography measurements. Appendix B compares the contact and intermittent contact mode on silicon nitride samples sent out to Digital Instruments.

# Chapter 2

# Scanning Probe Microscopy

Scanning Probe Microscopes (SPM's) constitute of a number of instruments [11] i.e. Scanning Tunneling Microscope (STM) for studying the electronic density of states of conducting or semi conducting materials, Atomic Force Microscope (AFM) for studying the surface roughness of materials, Magnetic Force Microscope (MFM) for studying the magnetic properties of materials, and Lateral Force Microscope (LFM) for studying surface friction. Now STM's and AFM's are also being used for nanolithography of devices [12], [13]. Fig. 2.1 illustrates the basic operation of a Scanning Probe Microscope (SPM).

The sample is placed over a piezoelectric scanner which moves the sample under the tip in a raster fashion. A coarse positioning system brings the tip close to the sample. Data are gathered by sensing the deflections of the tip as the sample is rastered under it. A computer converts the data into an image [11].

## 2.1 Scanning Tunneling Microscopy

The Scanning Tunneling Microscope uses the tunneling mechanism for imaging. A bias is applied between the tip and the sample. The tip is kept about 10 Å from the sample surface. The electrons from the sample tunnel into the tip or electrons from the tip tunnel into the sample depending on the bias applied. A bias voltage around 5-10 V is generally applied. The sample and the tip have to be either conducting or semi conducting. Insulators cannot be imaged with the STM. The current flow between the tip and sample is used to generate the topography of the sample [11].

There are two ways of generating the topography with the STM :

- Constant Current

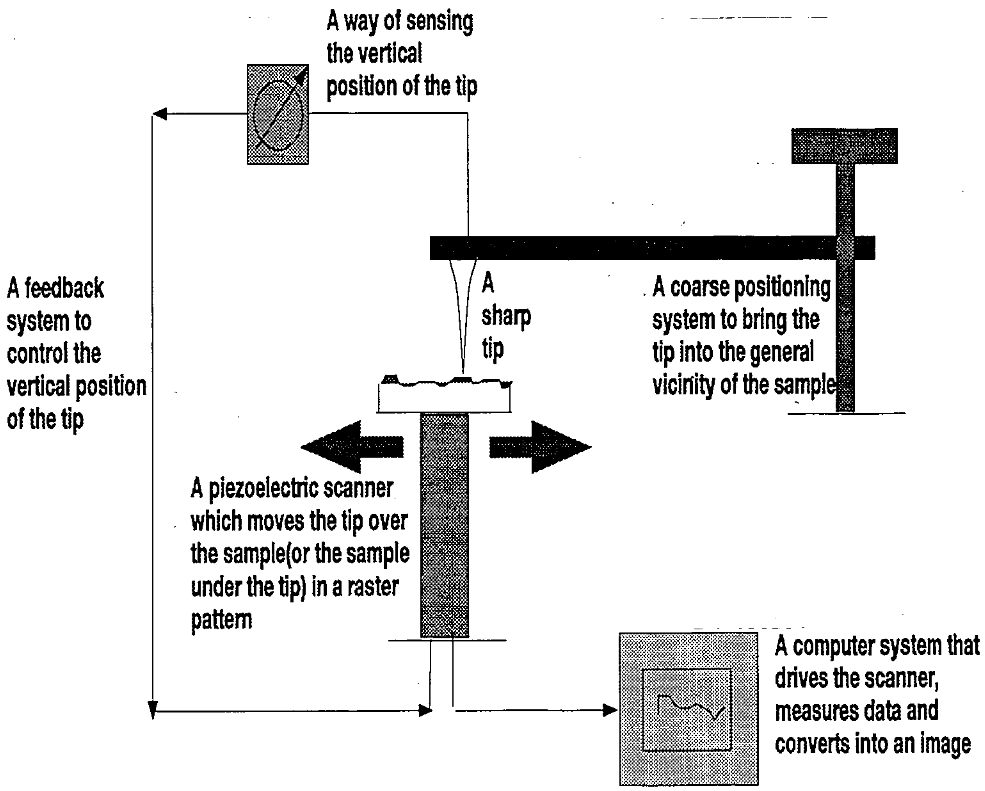

A way of sensing the vertical position of the tip
A feedback system to control the vertical position of the tip
A sharp tip
A coarse positioning system to bring the tip into the general vicinity of the sample
A piezoelectric scanner which moves the tip over the sample(or the sample under the tip) in a raster pattern
A computer system that drives the scanner, measures data and converts into an image

Figure 2.1: Schematics of generalized Scanning Probe Microscope [11]

- Constant Height

In the constant current mode, the current between the tip and the sample is kept constant. A feedback loop to the scanner moves the scanner up and down so that the current remains constant. The current has an exponential dependence on the sample-tip separation. For every 1 Å of sample-tip separation the current changes by an order of magnitude. The movement of the scanner constitutes the data set for generating the topography of the sample.

In the constant height mode, the height of the scanner is kept constant. The current changes value as it scans over the sample and that constitutes the data set. Fig. 2.2 illustrates the difference between constant current mode and constant height mode [11].

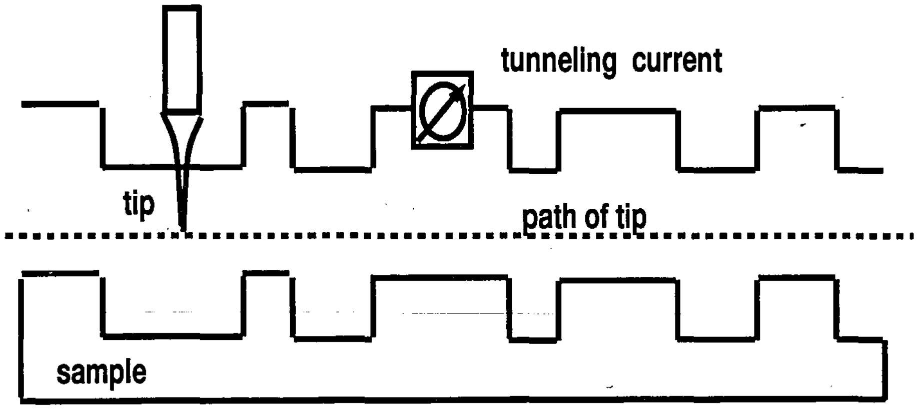
Tersoff and Hamann [14] developed the STM theory and found the tunneling current to be proportional to the surface local density of states. Their theory provides expression for intrinsic spatial resolution and dependence of the tunneling current on the tip size and shape.

## 2.2 Atomic Force Microscopy

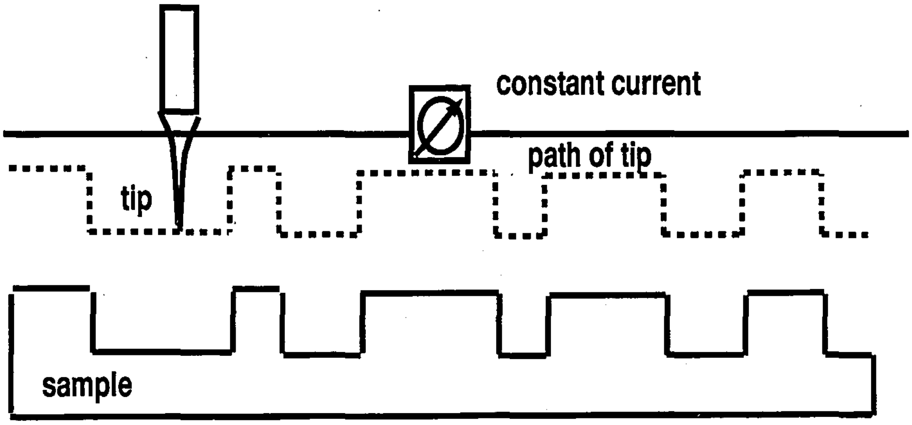
The repulsive or attractive force between two atoms is used as the imaging mechanism. The Atomic Force Microscope (AFM) introduced in 1986, gives insights in fields of surface science, electro-chemistry, biology and technology [15].

The Atomic Force Microscope (AFM) is characterized by [11]

- Sharp tip: The tip measures couple of microns long and often less than 100 Å in diameter. The tip is located at the free end of a cantilever 100-200$\mu$m.
- Forces between the tip and sample cause the cantilever to bend or deflect. A detector measures the cantilever deflections as the tip is scanned over the sample or the sample is scanned under the tip.


tunneling current
tip
path of tip
sample

**Constant Height**


constant current
path of tip
tip
sample

**Constant Current**

Figure 2.2: Constant height and constant current mode for STM [11]

- The deflections allow a computer to generate a surface topography map.
- Inter-atomic force called the van der Waals force.

The van der Waal forces play an important part in atomic interaction. Two atoms brought closer, initially attract and as the distance between them decreases they start repelling each other. When the forces of repulsion exceed that of attraction the atoms are said to be in contact.

Van der Waal forces are of three kinds :

- polarization i.e. permanent multi-pole moments
- induction
- dispersion

The attractive regime is the non-contact mode of operation and the repulsive regime is the contact mode of operation. Fig. 2.3 illustrates the contact and noncontact mode of operation.

### 2.2.1 Contact Mode

The tip and the sample are said to be in contact [11] if the attractive and repulsive forces balance each other. This distance is about 1-2 Å between the sample and the tip. A force is applied on the cantilever to keep it in contact with the sample. Due to the topography of the sample the cantilever experiences different repulsive forces at different points of the sample. These forces cause the cantilever to deflect. The deflection of the cantilever can be detected by various schemes [15].

- Tunneling
- Beam deflection
- Optical Interferometry.

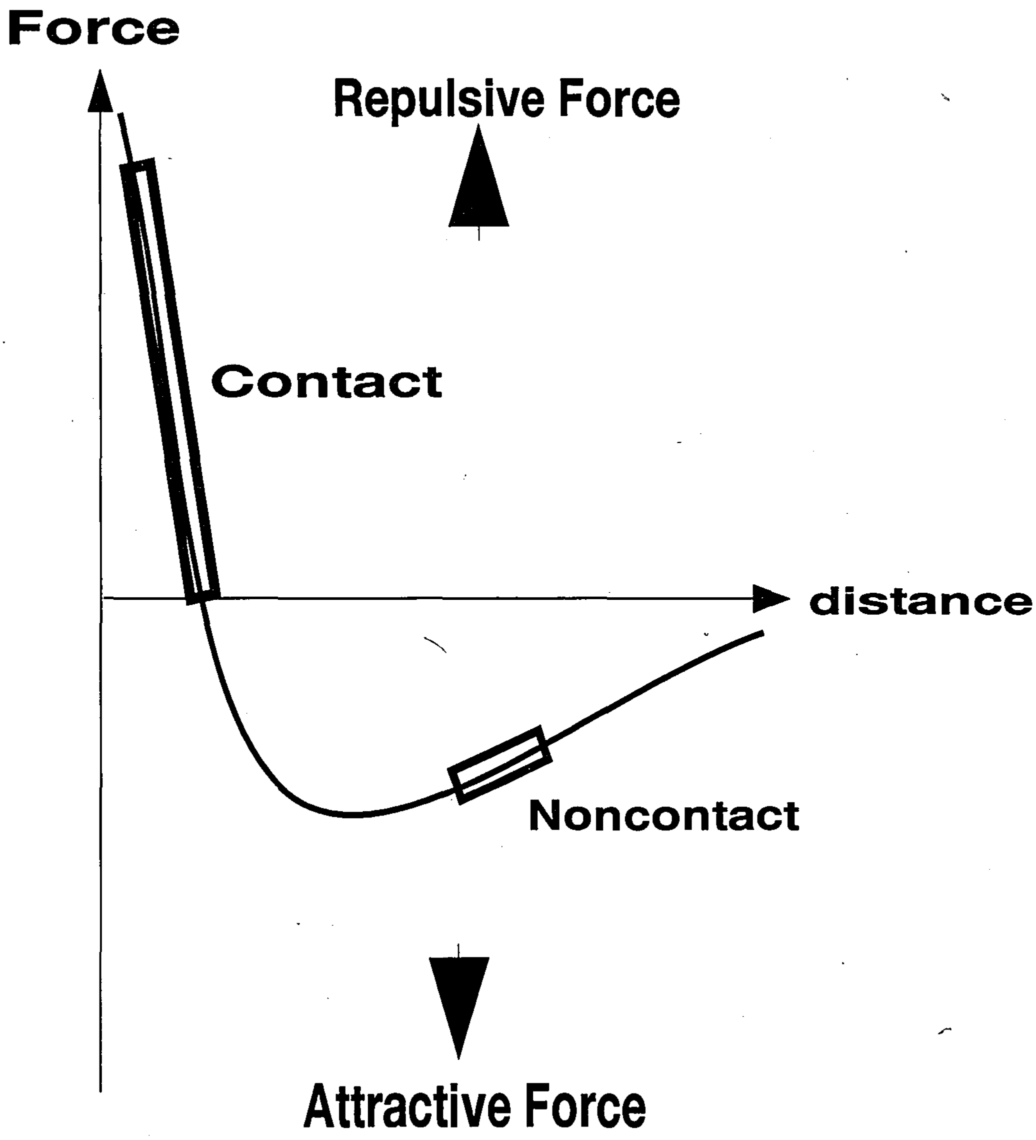

Force
Repulsive Force
Contact
distance
Noncontact
Attractive Force

Figure 2.3: Van der Waals force versus atomic separation. Atomic Force microscopes can be designed to operate in either of the two regimes indicated by heavy lines [11]

The most popular is the beam deflection scheme. Light from a laser diode is reflected onto a mirror and on the cantilever. The light bounces from the cantilever to a photo sensitive photo detector (PSPD). The PSPD is sensitive to position changes of up to 10Å. Due to the mechanical amplification of the ratio of distance between the PSPD and the cantilever, and the length of the cantilever, the PSPD can measure deflections up to 1Å [11]. The beam deflection technique is illustrated in Fig. 2.4

The contact mode also has two modes of operation.

- Constant Height
- Constant Force

The constant-force mode is similar to the constant-current mode in the STM. The forces between the sample and the tip are kept constant i.e. the cantilever deflections are kept constant. This is achieved by means of a feedback loop to the piezoelectric scanner. The scanner is moved in the positive or negative z direction to keep the cantilever deflections constant. The scanner movement constitutes the dataset to generate the topography of the sample.

In the constant-height mode the scanner height is kept constant i.e. no feedback circuit is used. The deflections of the cantilever are detected by the beam deflection technique and constitutes the data set for topography generation. The constant-height mode of operation is faster as there is no response time of the of the feedback circuit to account for and therefore can be used for real time imaging.

### 2.2.2 Non-Contact Mode

In this mode, the tip and the sample are kept around 100 Å away from each other. Since this mode lies in the attractive domain of the van der Waals force there is a danger of the cantilever falling on top of the sample due to large attractive forces. Thus a stiffer cantilever is required. Plus the slope of the van der Waals curve is much shallower i.e. there is less change in force with change in distance between the sample and the tip. The stiffer cantilever and the shallow slope make the cantilever

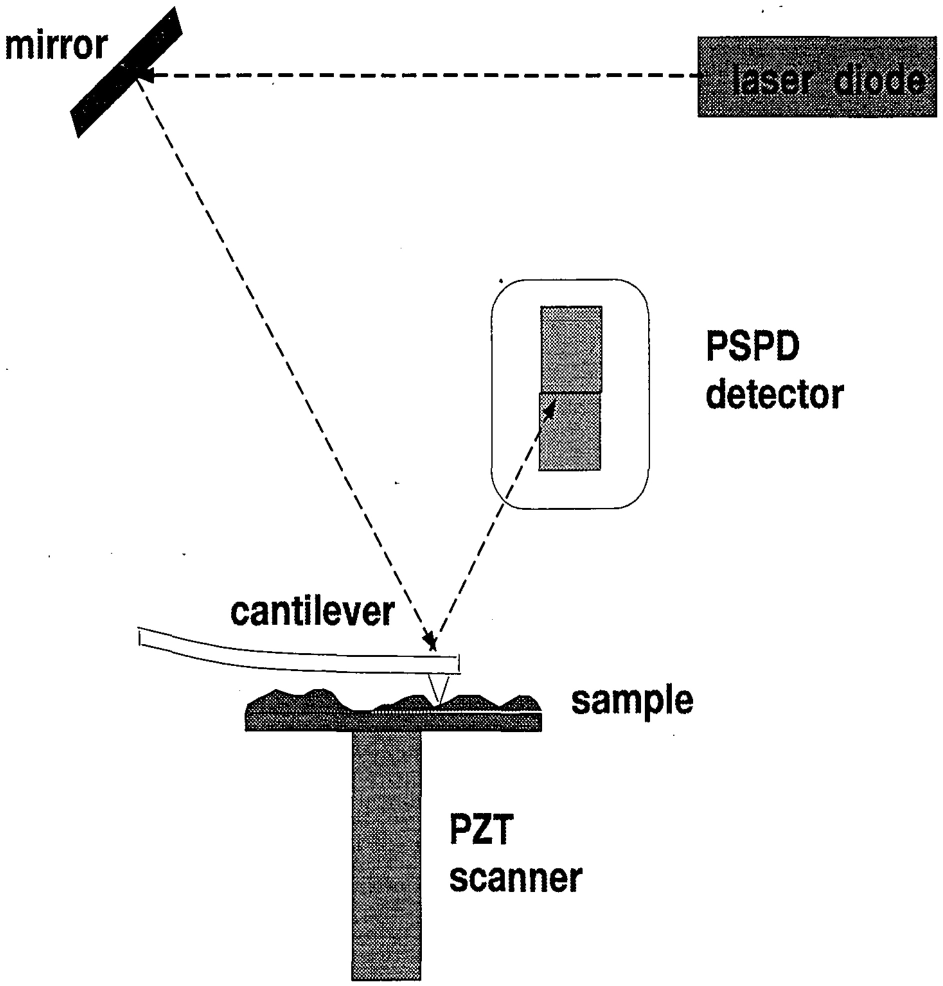

mirror
laser diode
PSPD
detector
cantilever
sample
PZT
scanner

Figure 2.4: Schematics of optical-deflection technique for detecting cantilever deflection(Beam bounce detection) [11]

deflect less with changes in topography. Therefore a more sensitive detection scheme is required. The cantilever is oscillated with its resonant frequency( 200-300 kHz) above the sample surface. Due to sample tip force interaction, the cantilever has one frequency at the top of its oscillation cycle and a different frequency at the bottom of its oscillation cycle. The oscillation frequency changes at the bottom with respect to the sample topography. The oscillation frequency is kept constant by means of a feedback loop. The scanner moves up and down to keep the frequency constant. The movement of the scanner is used as the data set for generating the sample topography.

The non-contact mode is useful as it doesn't contaminate the surface. But if there is a water particle on the surface, it will be imaged as part of surface topography. In the contact mode this water particle will not be imaged as the tip will penetrate this particle and image the surface accurately [11]

### 2.2.3 Tapping Mode

This mode is similar to the non contact mode. In this case the tip is oscillated with a high amplitude and it touches the sample in each oscillation. For $Si_3N_4$ layer in the SONOS device, this mode is optimum. It doesn't cause damage of the surface as is caused in the contact mode due to frictional or drag forces on the surface. It images the sample topography accurately as compared to non contact AFM where the sample topography could be imaged wrong due to a drop of water on the sample surface [11].

## 2.3 Lateral Force Microscopy

LFM is similar to contact mode AFM except the photo-sensitive photo-detector has a four quadrant measurement scheme rather than two quadrant measurement scheme as in the contact mode AFM. In the contact mode AFM, the deflections of the cantilever are measured by light reflecting off the cantilever on to the position sensitive photo detector. Light beam positioned at exact center corresponds to zero deflection. Any deviation from the center to the upper and lower quadrant yields the value of cantilever deflection. In the four quadrant scheme the difference between the sum of the upper two quadrants and the sum between the lower two quadrants gives the vertical deflection of the cantilever. Due to the frictional forces between the surface and the tip, the cantilever deflects vertically as well as twists laterally. This lateral twisting is measured by the difference between the sum of the left quadrants and the sum of the right quadrants [11].

## 2.4 Magnetic Force Microscopy

The magnetic force microscope operates similar to non-contact mode of operation. The tips in this case are coated with ferromagnetic material. The magnetic forces are detected with spatial variation and imaged. The question arises that since MFM and non-contact AFM are similar how do we differentiate between the topographical information and magnetic information. This is done by noting the distance of the tip from the sample surface. Magnetic forces persist longer than van der Waal forces. Therefore for MFM the tip can be further away from the sample. The nearer it is to the sample, the image represents topography rather than magnetic information [11].

## 2.5 Scanning Capacitance Microscopy

The STM or the AFM can be used to take capacitance measurements. When using the STM, the tip is used as the capacitance probe. For avoiding low frequency drifts in the capacitance caused by stray capacitance variations, the capacitance between the tip and the sample is modulated at high frequencies $\approx$ 30 kHz. A d.c. bias superimposed with a small a.c. voltage is applied to a semiconductor sample. The sample goes through accumulation, depletion and inversion of charge depending on the voltage applied. This varies the capacitance which is measured by sensors applied to the probe tip [?].

With the AFM, the cantilever with the probe tip is metalized. The metalized cantilevers are fabricated either by etching tungsten wires or by coating silicon-dioxide cantilevers with metal. The capacitance is measured by applying bias to the sample and attaching sensors to the probe. Both the topography and the capacitance can be measured simultaneously or independently.

# Chapter 3

# Processing Technology

In this chapter, fabrication sequence of gridded and ungridded SONOS capacitors is described. Gridded capacitors have an n+ grid ion implanted in the substrate.

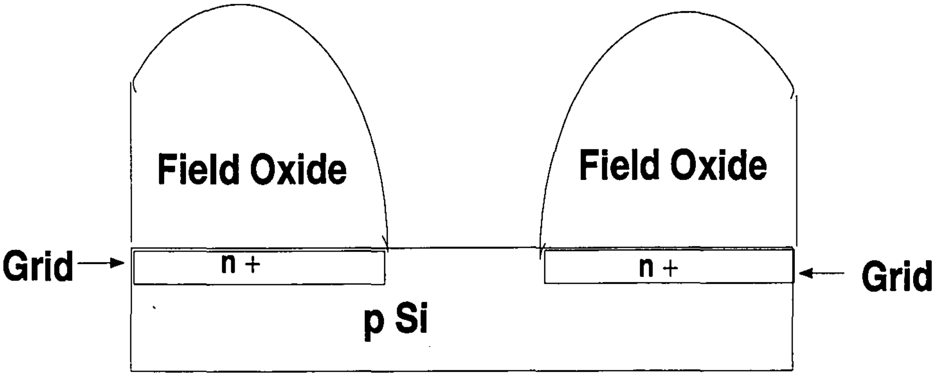


Figure 3.1: Gridded base before ONO Deposition

The n+ grid supplies the minority carriers during inversion. Thus a lesser voltage is required at the gate to invert the Si surface and charge injection to the nitride takes place at a lower voltage decreasing the programming voltage of the device. The same effect can be achieved on the ungridded wafers by shining light on them.

These capacitors were fabricated to study their electrical characteristics. The nitride deposition temperatures were varied to vary the surface roughness of the nitride layers.

## 3.1 Capacitors

SONOS Capacitors were fabricated using the ONO dielectric with the nitride layer deposited at three different temperatures. The deposition temperatures used were 650° C, 680° C and 725° C. Two types of capacitors were fabricated, gridded and ungridded. In both the types, two sets of wafers were fabricated, one with tunnel oxide thickness of 12 Å and the other with tunnel oxide thickness of 18 Å.

### 3.1.1 Ungridded Capacitors

1. Starting Material: p substrate $< 100 >$, 20-30 Ω-cm., 3 inch diameter
2. Active Area
   - (a) Furnace Clean
     5:1:1 DI Water:Ammonium Hydroxide:Hydrogen Peroxide, 75° C, 5 min.
     5:1:1 DI Water:Hydrochloric Acid:Hydrogen Peroxide, 65° C, 5 min.
   - (b) 1000 Å Oxide
     Wet Oxide, 900° C, 40 min.
   - (c) Etch (1000 Å oxide)
     BHF, 3 min.
3. Triple Dielectric
   At this point six sets of wafers with two wafers in each set were prepared.
   The first set of three wafers were processed as follows :
   - (a) Furnace Clean
   - (b) **Tunnel Oxide**: 18 Å
     Dry oxide, 700° C, 11 min., Ar anneal, 700° C, 30 min.
   - (c) **Memory nitride** : 50 Å
     LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 650° C, 38 min

**OR**

LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 680° C, 19 min

**OR**

LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 725° C, 7 min

(d) **Blocking Oxide** : 35 Å
LPCVD:0.8 torr, 100 sccm $N_2O$, 10 sccm $SiCl_2H_2$, 725° C, 14 min
Wet Oxide, 900° C, 30 min.

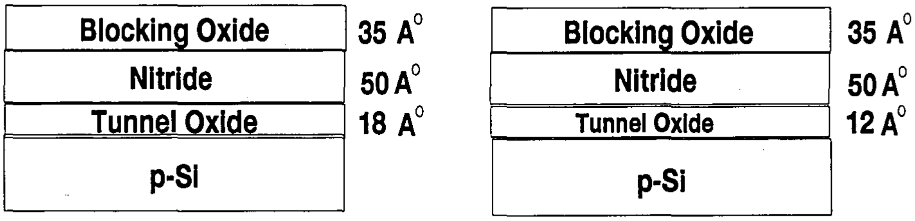

Blocking Oxide
35 A°
Nitride
50 A°
Tunnel Oxide
18 A°
p-Si
Blocking Oxide
35 A°
Nitride
50 A°
Tunnel Oxide
12 A°
p-Si

Figure 3.2: Ungridded capacitors with 18 Å and 12 Å tunnel oxide

The remaining three sets of wafers were processed as follows

(a) Furnace Clean

(b) **Tunnel Oxide**: Native Oxide(12 Å )
Dry oxide, 700° C, 11 min., Ar anneal, 700° C, 30 min.

(c) **Memory nitride** : 50 Å
LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 650° C, 38 min

**OR**

LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 680° C, 19 min

**OR**

LPCVD:0.3 torr, 100 sccm $NH_3$, 10 sccm $SiCl_2H_2$, 725° C, 7 min

(d) **Blocking Oxide** : 35 Å
LPCVD:0.8 torr, 100 sccm $N_2O$, 10 sccm $SiCl_2H_2$, 725° C, 14 min
Wet Oxide, 900° C, 30 min.

All six sets of wafers went through the following processing steps :

4. Metal

   (a) 6 KÅ Metal
   Al 99.9999 %, Evaporation

   (b) Photo 1 - Metal

   (c) Etch ( 6 KÅ metal)
   PAN Etch, 45° C, 2 min

   (d) Photo resist Strip

   (e) Plasma Etch backside(ONO)
   $CF_4$, 0.3 torr, 300 W, 5 min.

   (f) Q-tip Etch Backside
   A Q tip dipped in acetone is used to remove any remaining ONO layer and contamination from the back side of the wafer. 10:1 BHF, 10 min.

   (g) 6 K Å Metal backside
   Al 99.9999 %, Evaporation

   (h) Organic Clean Methanol 5 min.
   Acetone 5 min.
   5 times rinse

   (i) Anneal
   $H_2 : N_2$, 450° C, 30 min.

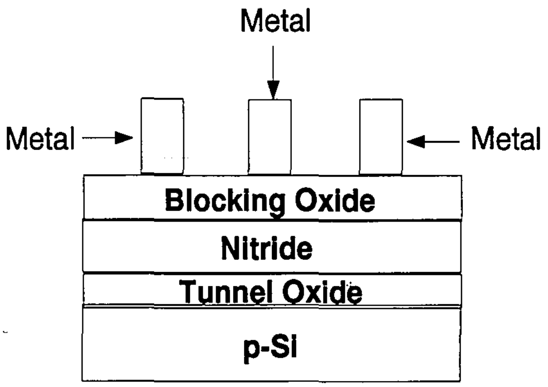


Figure 3.3: Ungridded capacitors after metalization

### 3.1.2 Gridded Capacitors

These following processing steps are performed on the gridded wafers before they follow the same processing sequence from step 3 onwards of the ungridded wafers.

1. Starting Material: p substrate < 100 >, 20-30 Ω-cm., 3 inch diameter
2. Active Area
   (a) Furnace Clean
   5:1:1 DI Water:Ammonium Hydroxide:Hydrogen Peroxide, 75° C, 5 min.
   5:1:1 DI Water:Hydrochloric Acid:Hydrogen Peroxide, 65° C, 5 min.
   (b) 1000 Å Oxide
   Wet Oxide, 900° C, 40 min.
   (c) 1000 Å Nitride
   LPCVD 0.3 torr, 100 sccm $NH_3$, 30 sccm $SiCl_2H_2$, 725° C, 60 min.

(d) Photo -1

(e) Plasma Etch (1000 Å nitride)
$CF_4$, 0.23 torr, 125 W, 8 min., both front and back sides

(f) Implant
Phosphorus

(g) Photo resist Strip

(h) Furnace Clean

(i) Anneal
$N_2$, 950° C, 60 min.

(j) 7000 Å oxide
Wet Oxide, 900° C, 60 min.

(k) Etch (thin oxynitride)
BHF, 1 min.

(l) Etch (1000 Å nitride)
$H_3PO_4$, 150° C, 60 min.

(m) Etch (1000 Å oxide)
BHF, 3 min.

Processing was completed by following sequence step 3 of the ungridded wafers.

## 3.2 Nitride Layer

The nitride layer of the ONO dielectric stores charge. To vary the surface roughness of the nitride layer it was deposited at three different temperatures 650° C, 680° C, 725° C. These three temperatures were selected because 725° C is the temperature currently being used in depositing the nitride during device fabrication at Lehigh, 680° C was reported[7] to be the temperature with the least surface roughness, 650° C was chosen to check temperatures below 680° C. Below 600° C a reaction between $NH_3$ and $SiCl_2H_2$ does not take place. There is a vast difference in the deposition times of nitride at these three temperatures. The reaction taking place is

$3\ SiCl_2H_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$

At 650° C, it took 37 min. to deposit a 50 Å nitride, at 680° C it took 19 min. and finally at 725° C it took 7 min.

While fabricating ONO devices, the tunnel oxide was thermally grown, the nitride was deposited by LPCVD and the blocking oxide was first deposited in the LPCVD and then densified in the wet oxidation furnace. During the formation of the blocking oxide some underlying silicon nitride was consumed. To measure the nitride thickness accurately [10], control wafers with known nitride thickness were used. After furnace clean, the thickness of one control wafer was measured by ellipsometer at five points to measure the thickness of the nitride lost during furnace clean. The same amount of nitride was lost by other control wafers. After required nitride deposition on device and control wafers, the control wafers were measured at five different points for the initial nitride thickness. Control wafers with known initial nitride thickness were used as controls in the blocking- oxide deposition and densification. After densification, the blocking oxide is etched away in buffered HF solution. After every 5 seconds, the thickness of the wafer was measured. The point where the etch rate changes, signals the complete removal of the blocking oxide. Ellipsometer measurements at this point yields the final nitride thickness.

In this chapter, the processing technology of gridded and ungridded SONOS capacitors was discussed. Both sets of capacitors have the nitride layer deposited at different temperatures.

# Chapter 4

# Measurements

## 4.1 AFM Measurements

The atomic force microscope yields a three dimensional image of the topography of the sample. After the required sample area is scanned, an image is generated by the software. The image can be processed i.e. the noise level could be reduced or a dust particle from the surface can be removed before information is extracted from it. Since the image is of atomic scale, the sensitive measurement may be affected by very low noise floors of the electronic circuit and the noise of the environment. The process of flattening removes this noise. It fits a smooth curve to the data points on the scan line. This curve can be a 1st order derivative curve to an 8th order derivative curve where the 1st order curve gives a straight line at the center of data points and the eight order curve tries to fit the points on the scan line exactly. While extracting data from the image, if there is a noticeable dust particle on the surface it can be removed from the image. The data extracted then consists of points without the dust particle.

The data can be extracted in two modes - line analysis mode and region analysis mode. The line analysis is done on a line drawn across the image of the scanned region. Region analysis is done on the whole region scanned. This thesis used region analysis of the surface.

### 4.1.1 Surface Region Measurements

The following information can be extracted from the image by the software [11]

1. Average Roughness: The average of all the data points in the scanned surface is calculated. It is calculated using the standard definition:

$$R_{ave} = \frac{\sum \mid z_n - \overline{z} \mid}{n} \tag{4.1}$$

where $\overline{z}$ = average z height

n is the number of data points taken over the scanned area.

2. RMS Roughness: The RMS roughness is root-mean-squared roughness of all the data points taken over the scanned area.

$$R_{rms} = \sqrt{\frac{\sum_{n=1}^{N}(z_n - \overline{z})^2}{n-1}} \tag{4.2}$$

where $\overline{z}$ = average z height

3. $R_{p-v}$: $R_{p-v}$ gives the maximum peak to valley separation within the scanned areas. $R_{p-v}$ is given by the difference highest data point and the lowest data point:

$R_{p-v} = z_{max}$-$z_{min}$

where n is the number of data points within the height profile.

4. Median height: The median height is defined as the median of all data points. A median is a point which has half the data points above it and the other half below it.

5. Mean height: Mean height is the mean of all data points. $\overline{z} = \sum z_n / n$

where $\overline{z}$ = average z height

6. Surface area: The surface area of the scanned area is measured by adding the surface area below each point. The surface area below each point is measured by doubling the triangle of adjacent data points and adding the two.

7. Volume: This is the volume under the scanned area. Here the zero reference is the minimum data point.

### 4.1.2 Height Histograms and Bearing Ratios

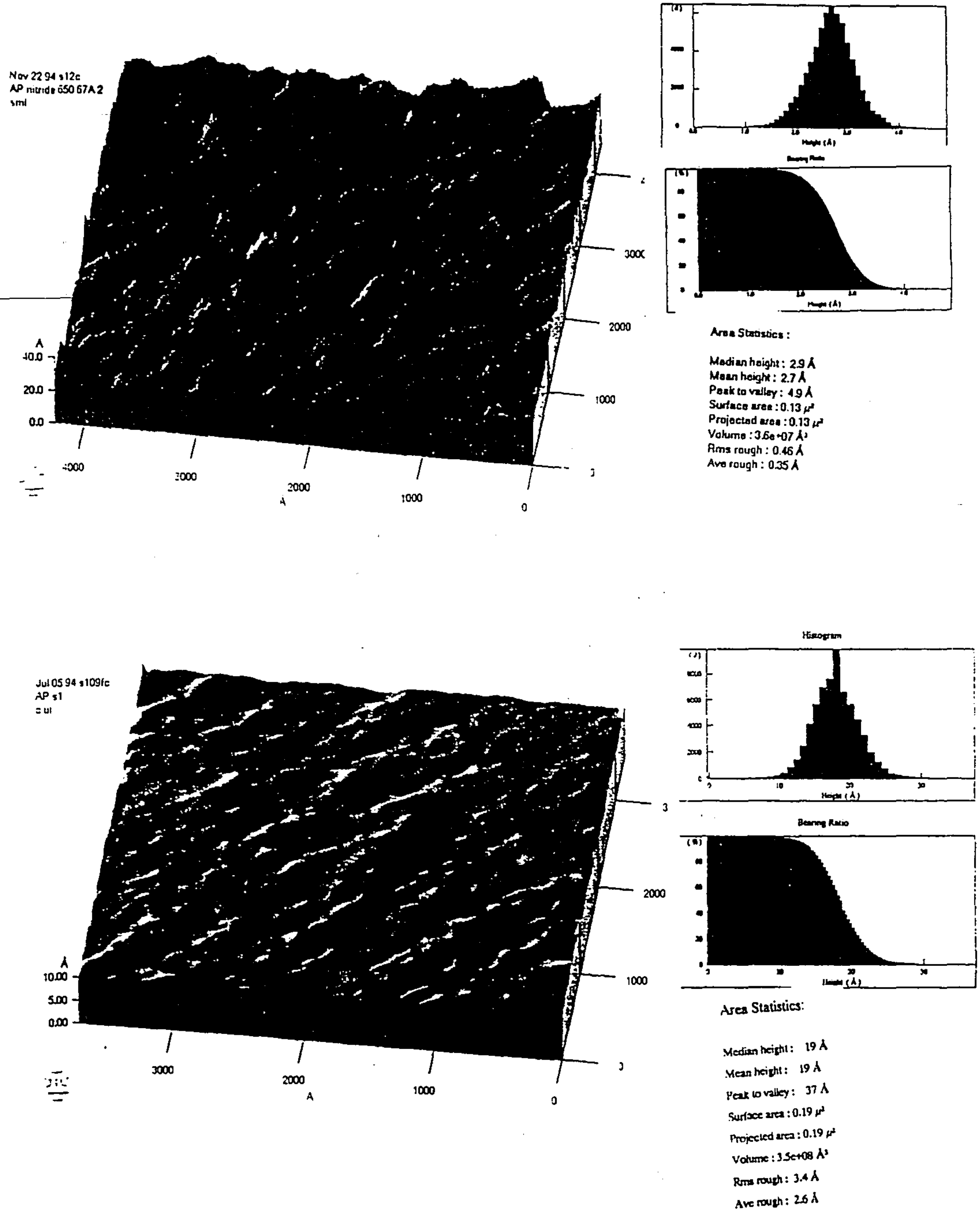
It is a bar graph of the heights of data points of the sample. The number of data points of the same height are counted and put on the bar graph as one bar. Usually height histograms have a Gaussian curve with the number of data points having the median height are the maximum.

The bearing ratio is the integral of the height histogram. It gives a plot of data points that lie above a certain height [11].

In this thesis the surface measurements have been done with the AFM. STM could not be used as it images conducting or semi-conducting surfaces and silicon nitride is an insulator. But silicon surfaces with no native oxide have been imaged under ultra high vacuum with the STM [16]. In ambient atmosphere, a native oxide grows over the silicon surface making the imaging of the silicon surface difficult. To overcome the problem the silicon surface is hydrogen terminated. One way of hydrogen passivating the surface is [17] by eliminating hydrocarbons from the surface by exposure to UV light in an atmosphere of oxygen. The silicon sample after going through clean procedures is heated in oxygen to about 200° C. It is then exposed to low pressure mercury lamp for 10 minutes. The sample is then dipped in 1% HF and rinsed in DI water. This sample is now stable in air for several hours though with some oxygen and fluorine contamination

### 4.1.3 Temperature Comparison

Four samples were selected. Three, each with a nitride deposited at a different temperature and one with no nitride. The sample with no nitride was chosen to provide a basis for initial surface measurement (fig. 4.1). The three different temperatures were 650° C, 680° C, and 725° C. As seen from figs. 4.1 and 4.2, the nitride layer deposited at 680° C has peak to valley roughness of 18 Å. The nitride layer deposited at 725° C has a larger peak to valley roughness of 28 Å and the one at 650° C has the largest peak to valley roughness of 37 Å.



Area Statistics :

Median height : 2.9 Å
Mean height : 2.7 Å
Peak to valley : 4.9 Å
Surface area : 0.13 $\mu^2$
Projected area : 0.13 $\mu^2$
Volume : 3.6e+07 Å$^3$
Rms rough : 0.46 Å
Ave rough : 0.35 Å

Area Statistics:

Median height : 19 Å
Mean height : 19 Å
Peak to valley : 37 Å
Surface area : 0.19 $\mu^2$
Projected area : 0.19 $\mu^2$
Volume : 3.5e+08 Å$^3$
Rms rough : 3.4 Å
Ave rough : 2.6 Å

Figure 4.1: AFM Images and data of Bare Si(top) and $Si_3N_4$ deposited at 650° C(bottom)

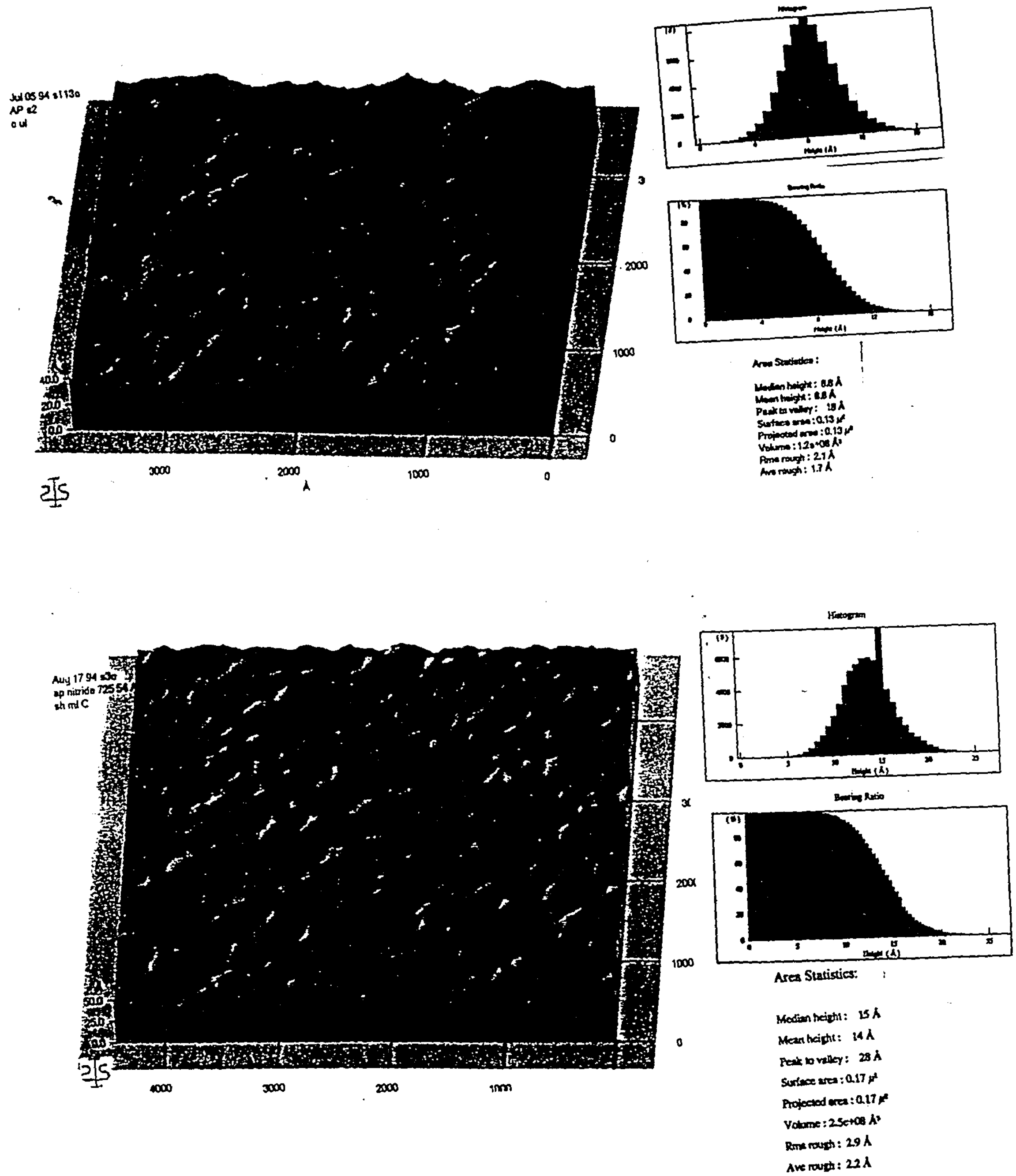

Jul 05 94 s113o
AP s2
o ul
Histogram
Height (Å)
Bearing Ratio
Height (Å)
3000
2000
1000
0
Å
2000
1000
0
Area Statistics :
Median height : 8.8 Å
Mean height : 8.8 Å
Peak to valley : 18 Å
Surface area : 0.13 µ²
Projected area : 0.13 µ²
Volume : 1.2e+08 Å³
Rms rough : 2.1 Å
Ave rough : 1.7 Å
Aug 17 94 s3o
ap nitride 725 54
sh ml C
Histogram
Height (Å)
Bearing Ratio
Height (Å)
4000
3000
2000
1000
2000
1000
0
Area Statistics:
Median height : 15 Å
Mean height : 14 Å
Peak to valley : 28 Å
Surface area : 0.17 µ²
Projected area : 0.17 µ²
Volume : 2.5e+08 Å³
Rms rough : 2.9 Å
Ave rough : 2.2 Å

Figure 4.2: AFM Images and data of $Si_3N_4$ deposited at 680° C(top) and 725° C(bottom)

### 4.1.4 Area Comparison

Area comparison was done using two modes with two different samples. For contact mode a $Si_3N_4$ layer of 43 Å was deposited at 650° C with a $NH_3$:$SiCl_2H_2$ flow rate ratio of 5:1. Areas of 4000 Å x 4000 Å and 1.47 $\mu$m x 1.47 $\mu$m were chosen. Surface roughness values remained the same over different areas of the same sample (fig. 4.3). The values may change if there was a dust particle in one and not in the other area.

For non-contact mode, a $Si_3N_4$ layer of 67 Å was deposited at 680° C with a $NH_3$:$SiCl_2H_2$ flow rate ratio of 10:1. Area of 4000 Å x 4000 Å and 1$\mu$m x 1$\mu$m were chosen. Here too, surface roughness values remained the same (fig. 4.4).

### 4.1.5 Intermittent mode and Non-contact mode

A 67Å nitride sample deposited at 650 ° C was chosen to study the different modes of the AFM. As seen from fig. 4.5, the intermittent- contact mode works the best for $Si_3N_4$ samples. The non-contact mode is likely to image dust particles on the surface thus giving unexpected surface roughness values. Intermittent-contact mode, on the other hand, touches the sample surface periodically removing the possibility of imaging dust. Intermittent-contact mode works better than contact mode as it eliminates drag on the sample surface and wearing of the tip.

### 4.1.6 Flow Rate Comparison

Two samples, both deposited at 650 ° C with $NH_3$:$SiCl_2H_2$ ratio of 5:1 and 10:1 were selected. From data we conclude that increasing the amount of $NH_3$ increases the surface roughness (fig. 4.6).

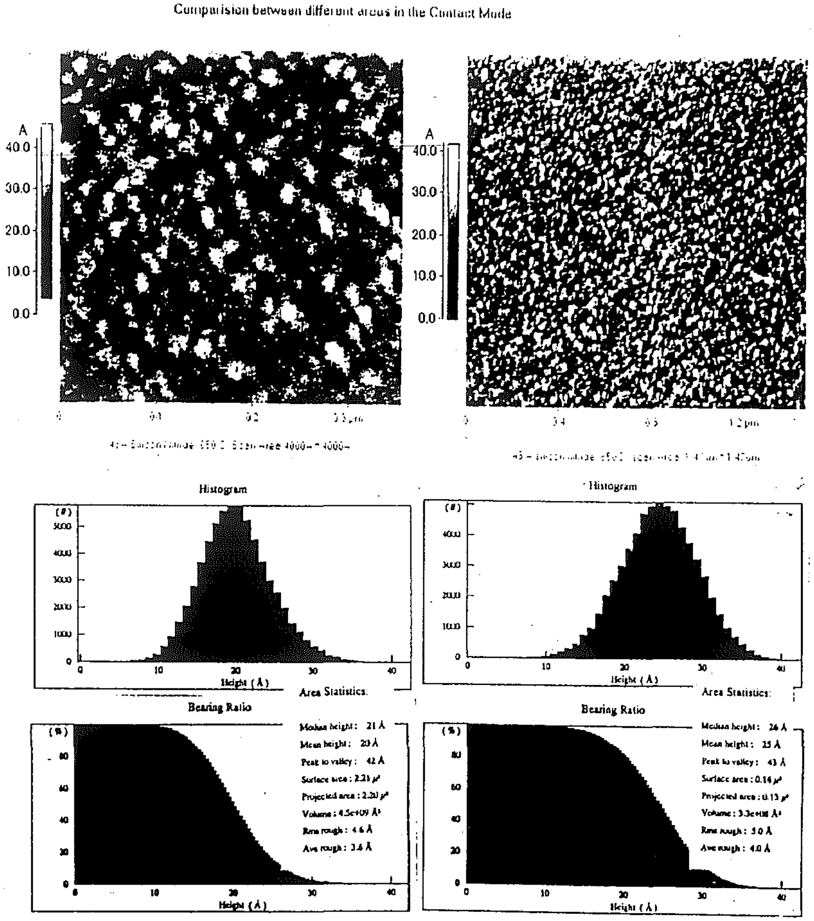
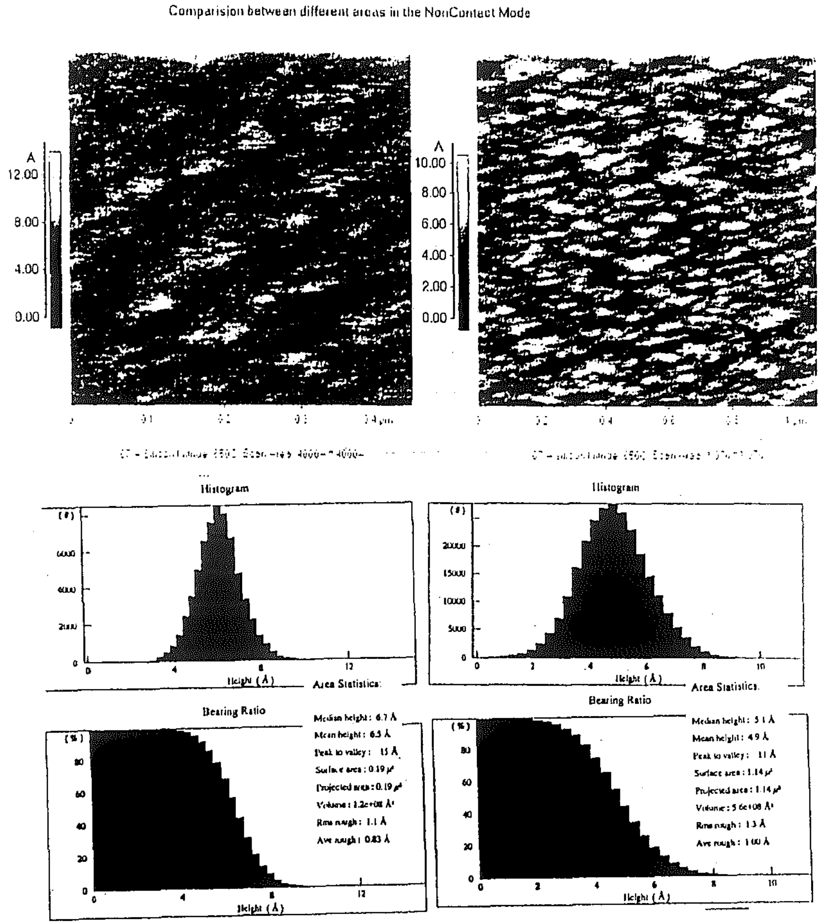


Figure 4.3: Contact mode Area Comparison



Area Statistics:

Median height : 6.7 Å
Mean height : 6.5 Å
Peak to valley : 15 Å
Surface area : 0.19 μ²
Projected area : 0.19 μ²
Volume : 1.2e+08 Å³
Rms rough : 1.1 Å
Ave rough : 0.83 Å

Area Statistics:

Median height : 5.1 Å
Mean height : 4.9 Å
Peak to valley : 11 Å
Surface area : 1.14 μ²
Projected area : 1.14 μ²
Volume : 5.6e+08 Å³
Rms rough : 1.3 Å
Ave rough : 1.00 Å

Figure 4.4: Non contact mode Area Comparison

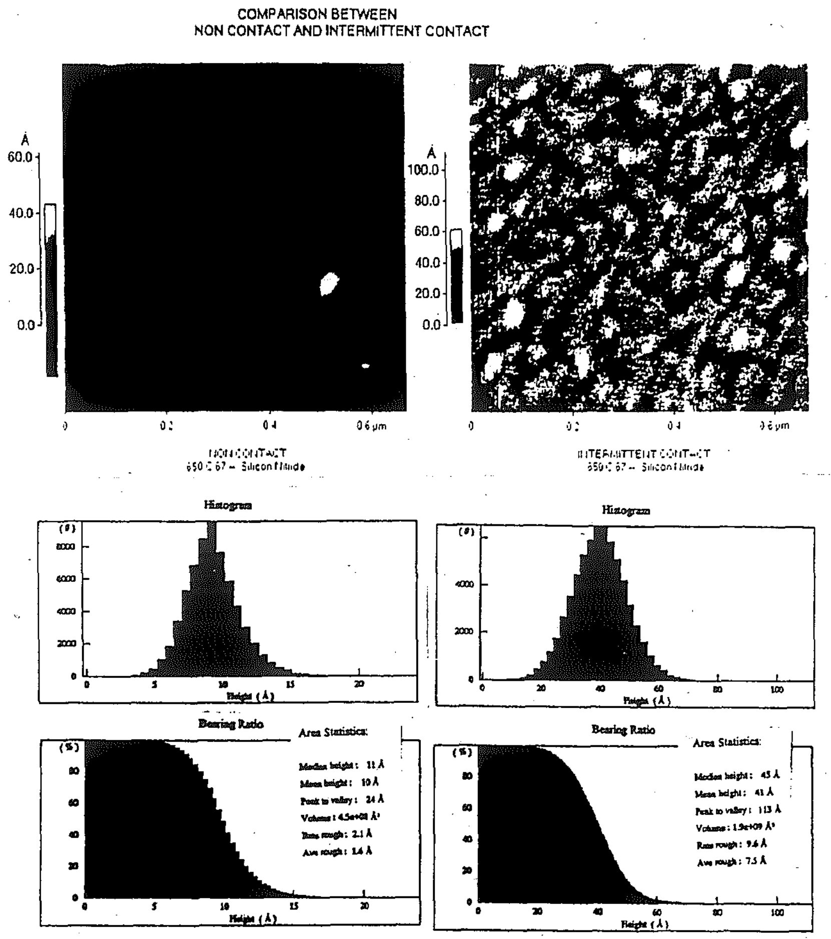
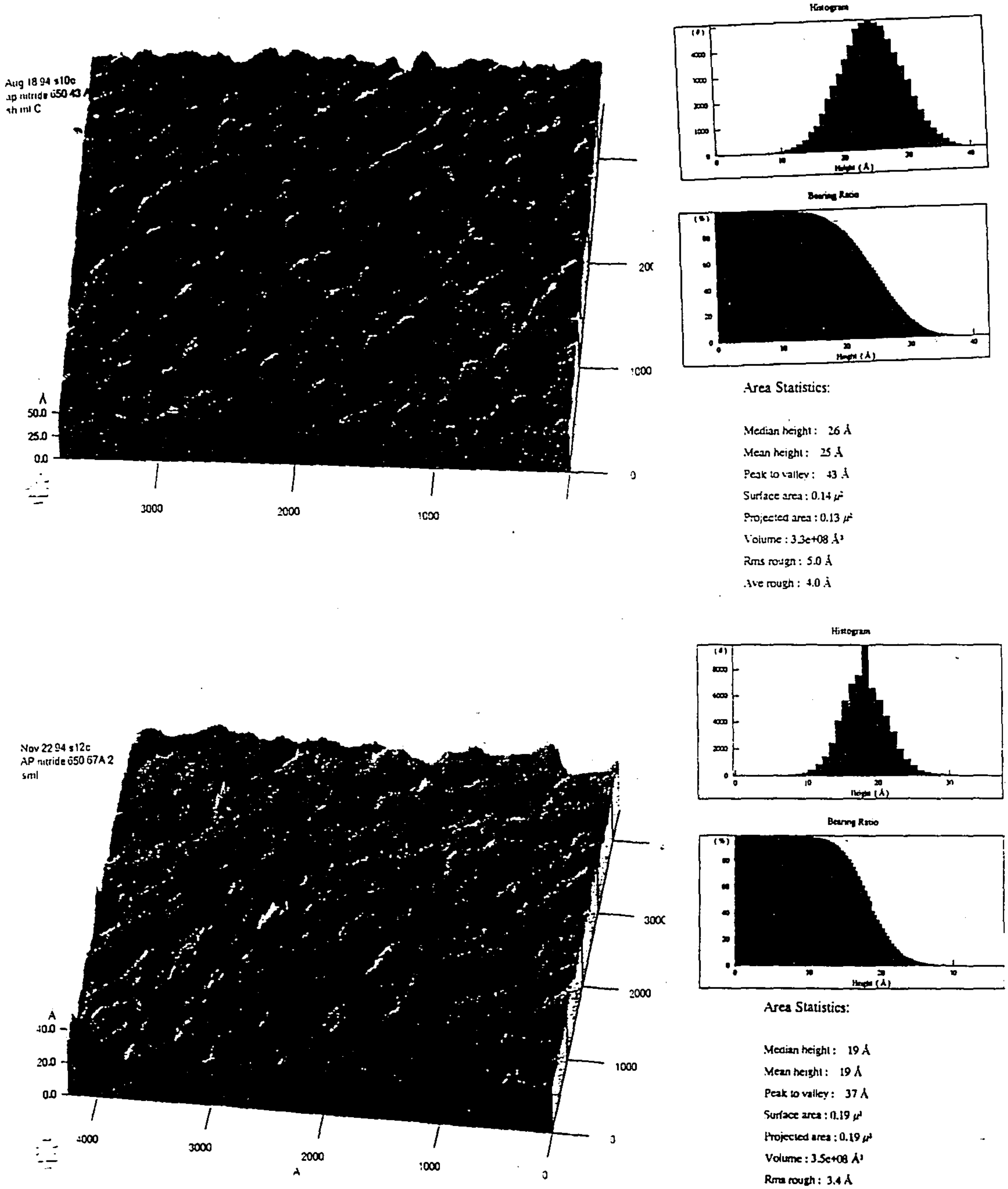


Figure 4.5: Intermittent mode and Non contact mode



Area Statistics:

Median height : 26 Å
Mean height : 25 Å
Peak to valley : 43 Å
Surface area : 0.14 $\mu^2$
Projected area : 0.13 $\mu^2$
Volume : 3.3e+08 $\text{Å}^3$
Rms rough : 5.0 Å
Ave rough : 4.0 Å

Area Statistics:

Median height : 19 Å
Mean height : 19 Å
Peak to valley : 37 Å
Surface area : 0.19 $\mu^2$
Projected area : 0.19 $\mu^2$
Volume : 3.5e+08 $\text{Å}^3$
Rms rough : 3.4 Å
Ave rough : 2.6 Å

Figure 4.6: Flow Rate Comparison of $NH_3$:$SiCl_2H_2$ ratio of 5:1 and 10:1

## 4.2 Electrical Measurements

### 4.2.1 Linear Voltage Ramp(LVR) Technique

The linear voltage ramp [18] was used to study programming of SONOS devices with charge storage in the nitride layer. The measurement was taken via National Instruments Lab-view virtual instrument: The software controls the function generator which supplies a linear voltage ramp to the bulk of the device. The linear voltage ramp was also fed to an A/D converter which supplied values of $V_{gb}$ to the computer.

$$V_{gb}=-V_{bg}$$

The gate of the device was connected to an electro-meter which measures the current from the device. The electro-meter was connected to the computer bus.

The current $I_g$, is given by

$$I_g = \frac{dQ_{gb}}{dt} = \frac{dQ_{gb}}{dV_{gb}}\frac{dV_{gb}}{dt} = \alpha C_{eff} \tag{4.3}$$

where $\alpha$ is the ramp rate and $C_{eff}$ is the effective capacitance.

For a device on a p type wafer, inversion occurs when the device is biased positively and accumulation when the device is biased negatively at the gate. As the voltage is swept from a negative voltage to a positive voltage the device undergoes accumulation, depletion and inversion of charge at the surface of the semiconductor. The capacitance changes accordingly and information about the stored charge can be extracted. The flatband voltage of the SONOS device changes as the device is first ramped in one direction and then in the other. The flatband voltage shift yields the memory window of the device at that particular voltage range.

The effective dielectric thickness can be calculated from from the effective capacitance. [10]

$$C_{eff} = \frac{Ig}{\alpha} \tag{4.4}$$

$$C_{eff} = A_g \frac{\epsilon}{x_{eff}} \tag{4.5}$$

where $A_g$ : Area of the gate

$\epsilon_{ox}$ : Oxide dielectric permittivity

$$x_{eff} = x_{ot} + x_{ob} + \frac{\epsilon_{ox}}{\epsilon_N} x_N \tag{4.6}$$

where $x_{ot}$ : tunnel oxide thickness

$x_{ob}$ : blocking oxide thickness

$x_N$ : storage nitride thickness

$\epsilon_N$ : nitride dielectric permittivity

The effective thickness values obtained from ellipsometry can be verified from LVR measurements.

Twelve wafers with SONOS capacitors were measured. Fig. 4.7 illustrates the sample set. Six gridded capacitors and six ungridded capacitors are shown. Out of six gridded capacitors, three have tunnel oxide thickness of 12Å. The other three have tunnel oxide thickness of 18 Å. On each set of three, the nitride was deposited at different temperatures. Similarly for the ungridded devices, three wafers have tunnel oxide thickness of 12 Åand the other three 18 Å. Each set of three again has nitride deposited at different temperatures.

Table 4.1 illustrates the nitride deposition conditions in these devices on different wafers. The temperature of deposition has been varied. The temperature of deposition changes the deposition rate. Thus nitride deposited at lower temperatures has a longer deposition time. The pressure (300 m torr) and flow rate ($NH_3$:$SiCl_2H_2$ ratio of 10:1) during all depositions has been kept constant.

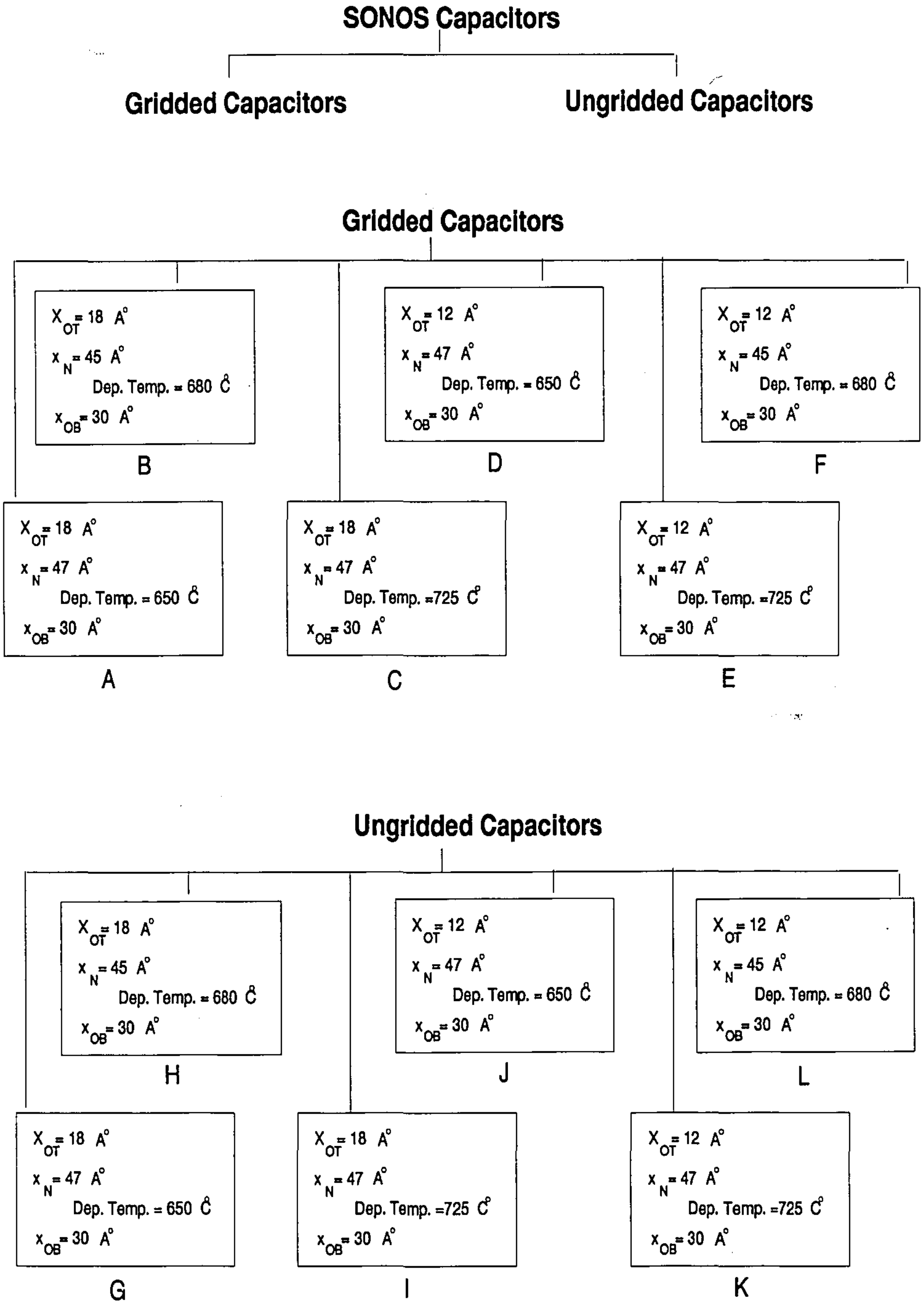

SONOS Capacitors
Gridded Capacitors
Ungridded Capacitors
Gridded Capacitors
$X_{OT}$= 18 A°
$x_N$= 45 A°
Dep. Temp. = 680 C°
$x_{OB}$= 30 A°
B
$X_{OT}$= 12 A°
$x_N$= 47 A°
Dep. Temp. = 650 C°
$x_{OB}$= 30 A°
D
$X_{OT}$= 12 A°
$x_N$= 45 A°
Dep. Temp. = 680 C°
$x_{OB}$= 30 A°
F
$X_{OT}$= 18 A°
$x_N$= 47 A°
Dep. Temp. = 650 C°
$x_{OB}$= 30 A°
A
$X_{OT}$= 18 A°
$x_N$= 47 A°
Dep. Temp. =725 C°
$x_{OB}$= 30 A°
C
$X_{OT}$= 12 A°
$x_N$= 47 A°
Dep. Temp. =725 C°
$x_{OB}$= 30 A°
E
Ungridded Capacitors
$X_{OT}$= 18 A°
$x_N$= 45 A°
Dep. Temp. = 680 C°
$x_{OB}$= 30 A°
H
$X_{OT}$= 12 A°
$x_N$= 47 A°
Dep. Temp. = 650 C°
$x_{OB}$= 30 A°
J
$X_{OT}$= 12 A°
$x_N$= 45 A°
Dep. Temp. = 680 C°
$x_{OB}$= 30 A°
L
$X_{OT}$= 18 A°
$x_N$= 47 A°
Dep. Temp. = 650 C°
$x_{OB}$= 30 A°
G
$X_{OT}$= 18 A°
$x_N$= 47 A°
Dep. Temp. =725 C°
$x_{OB}$= 30 A°
I
$X_{OT}$= 12 A°
$x_N$= 47 A°
Dep. Temp. =725 C°
$x_{OB}$= 30 A°
K

Figure 4.7: Capacitor Sample Set

| Sample | Flow rate $NH_3$:$SiCl_2H_2$ | Dep. Pressure | $x_N$ | Dep. Time | Dep. Temp. |
|---|---|---|---|---|---|
| A, D, G, J | 10:1 | 300 m torr | 47 Å | 38 min. | 650° C |
| B, E, H, K | 10:1 | 300 m torr | 45 Å | 19 min. | 680° C |
| C, F, I, L | 10:1 | 300 m torr | 49 Å | 7 min. | 725° C |

Table 4.1: Nitride Deposition Parameters

### 4.2.2 Gridded Devices

After checking numerous devices on each wafer, a representative LVR curve of each is presented. Comparing sample A, B and C which have the same tunnel oxide [18 Å] and the same blocking oxide [30 Å] thickness we see that the flat band voltage shift of A is the largest of 1.8 V with a programming voltage of 5 V.The flatband voltage of B is 1.5 V and C has no programming shift.

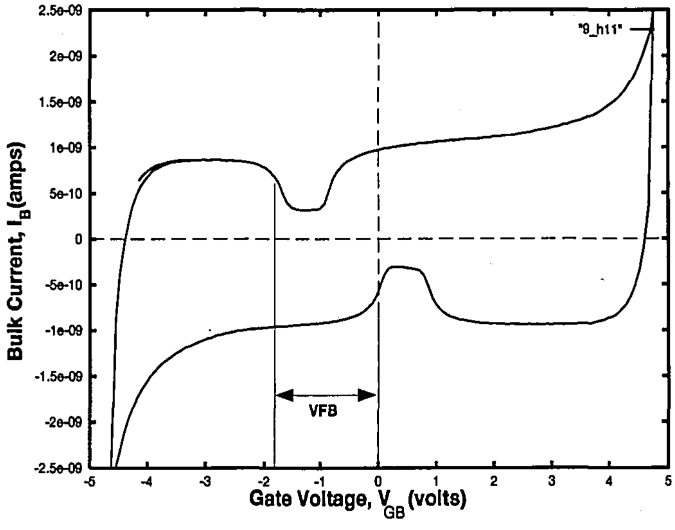


Figure 4.8: A Flat band Voltage shift of 1.8 V with nitride layer deposited at 650° C and area of 0.01 $cm^2$(Fig. 4.7 Sample A)

These measurements were taken on devices of area 0.1 cm x 0.1 cm. Looking at the smaller devices of area 0.0625$mm^2$ of the above wafers similar results were obtained 4.2.2, 4.2.2, 4.2.2.

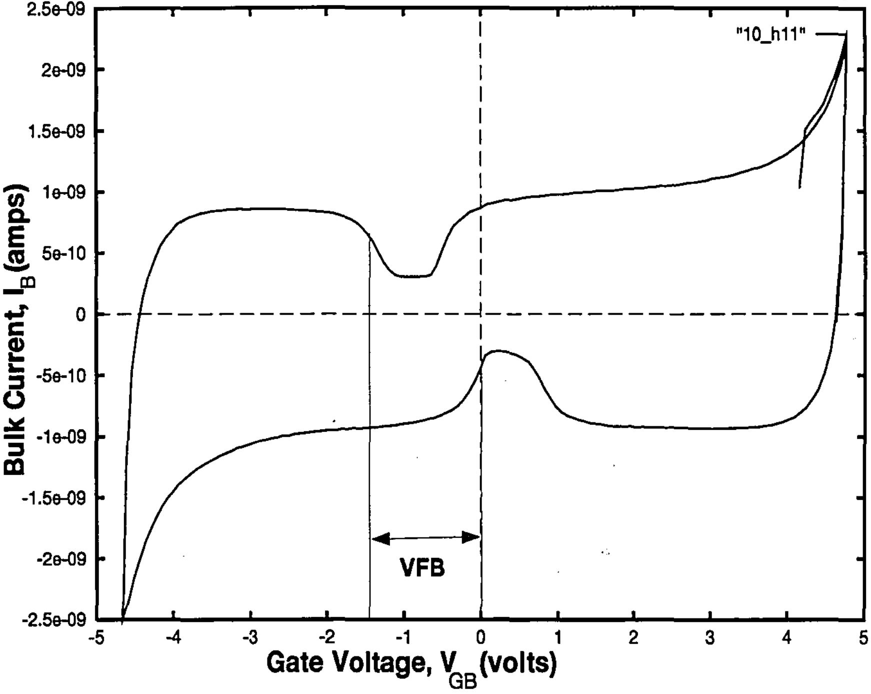


Figure 4.9: A Flatband Voltage shift of 1.5 V with nitride layer deposited at 680° C and area of 0.01 cm$^2$(Fig. 4.7 Sample B)

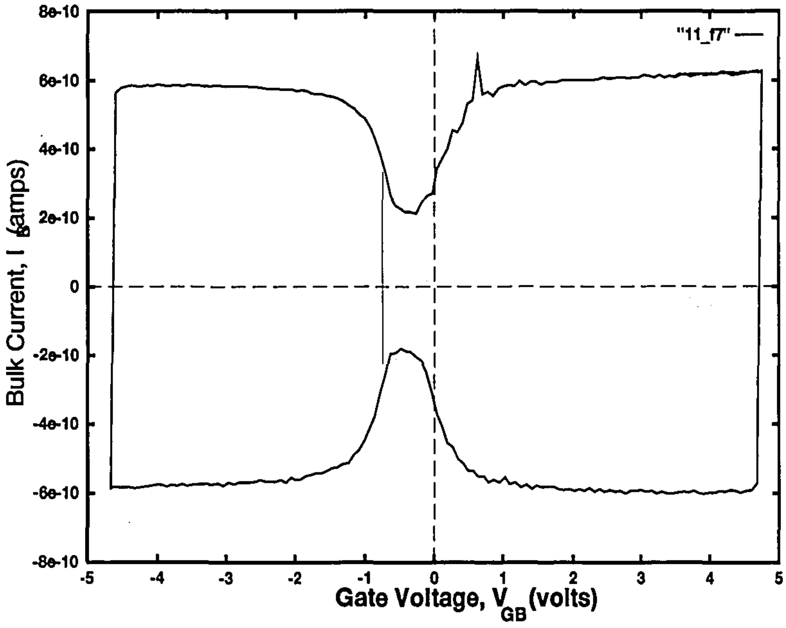


Figure 4.10: No Flatband Voltage shift with nitride layer deposited at 725° C and area of 0.01 cm$^2$ (Fig. 4.7 Sample C)

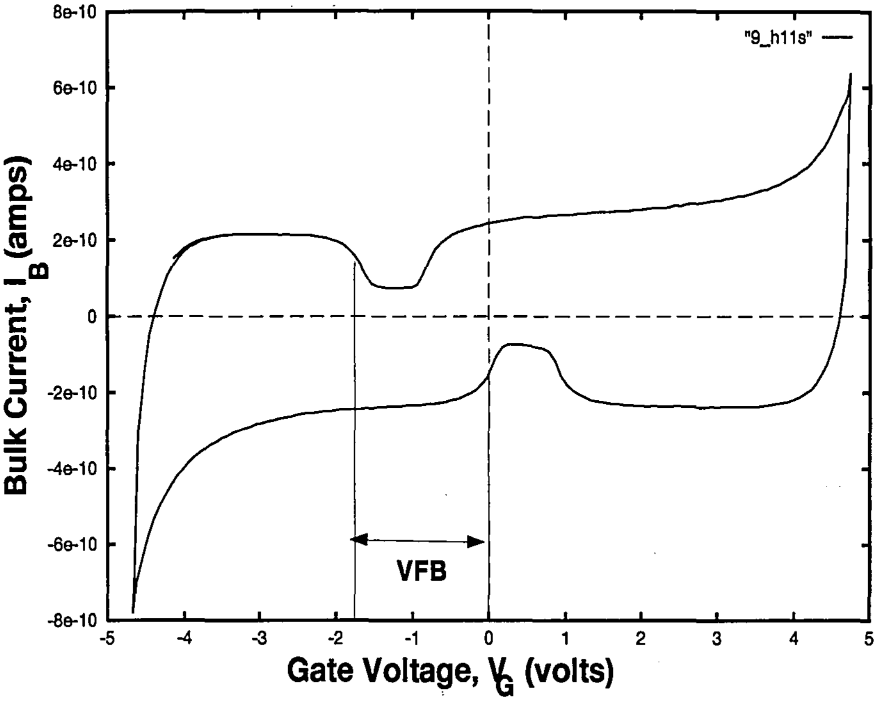


Figure 4.11: A Flatband Voltage shift of 1.8 V with nitride layer deposited at 650° C and area of 0.0625 mm$^2$ (Fig. 4.7 Sample A)

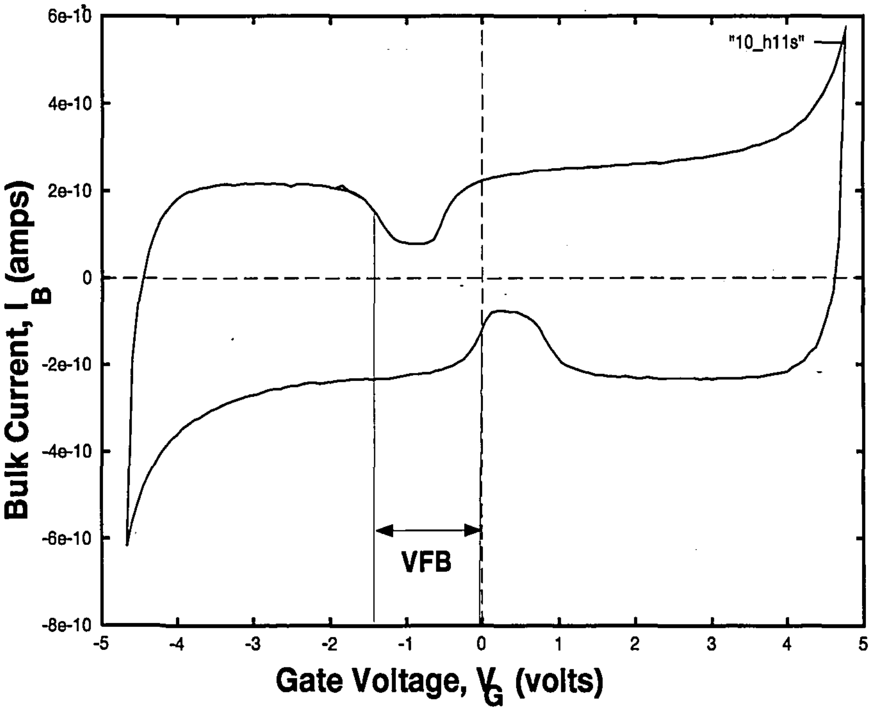


Figure 4.12: A Flatband Voltage shift of 1.4 V with nitride layer deposited at 680° C and area of 0.0625 mm$^2$ (Fig. 4.7 Sample B)

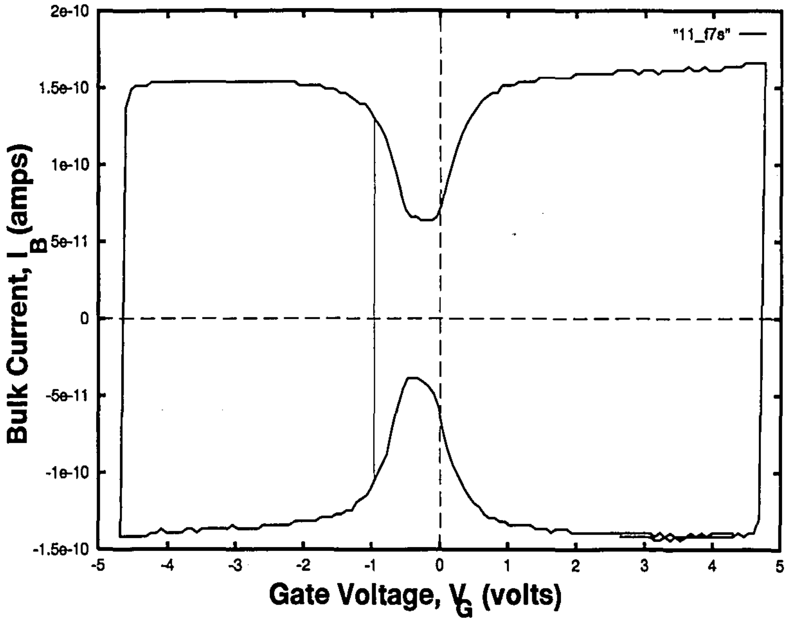


Figure 4.13: No Flatband Voltage shift with nitride layer deposited at 725° C and area of 0.0625 mm$^2$ (Fig. 4.7 Sample C)

Next D, E and F, samples which have an ultra thin tunnel oxide[12Å], nitride of similar thickness and blocking oxide[30Å] were compared. Here also sample D, where the nitride was deposited at 650° C, shows the greatest flat band voltage shift of 2V. Samples E and F had a flat band voltage shift of 1.9 V and 1.8 V respectively.

Wafers A and C were different only in their tunnel-oxide thickness. The flat band voltage shift in C was 0.2 V higher than A illustrating the fact that programming characteristics of devices can be directly related to the decrease in tunnel oxide thickness.

### 4.2.3 Ungridded Capacitors

Ungridded capacitors G, and H have the same tunnel oxide and blocking oxide thickness. The LVR curves, shown in Fig. 4.17 and 4.18, illustrate that sample G has the largest flat band voltage shift of 1.8 V followed by sample H with flat band shift of 1.5 V. They follow the same trend as the gridded wafers.

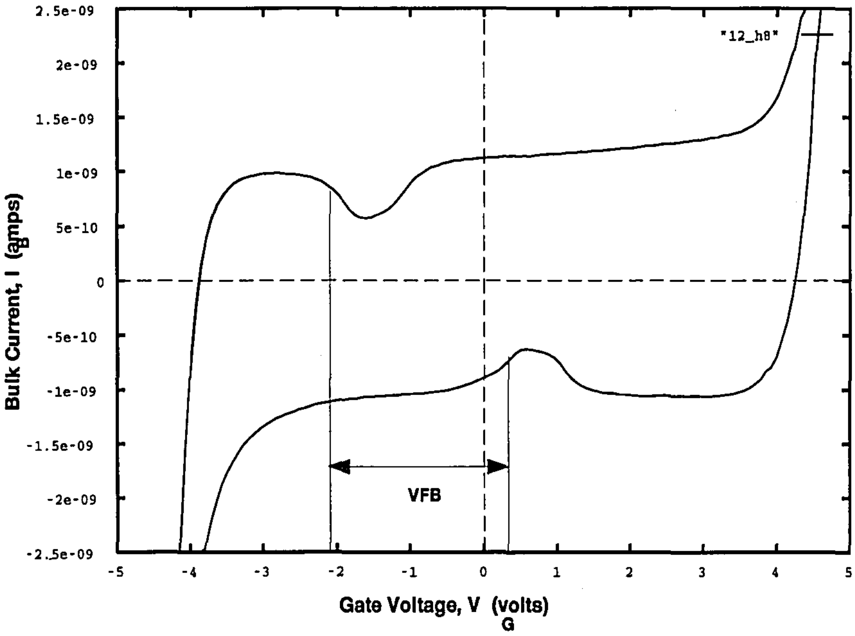


Figure 4.14: A Flatband Voltage shift of 2.2 V with nitride layer deposited at 650° C and area of 0.01 cm$^2$ (Fig. 4.7 Sample D)

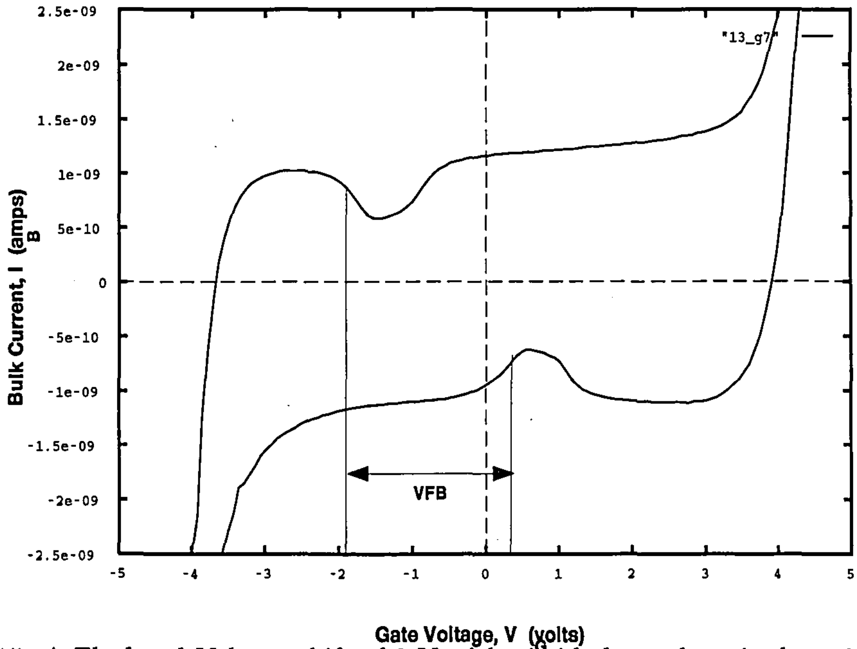


Figure 4.15: A Flatband Voltage shift of 2 V with nitride layer deposited at 680° C and area of 0.01 cm$^2$ (Fig. 4.7 Sample E)

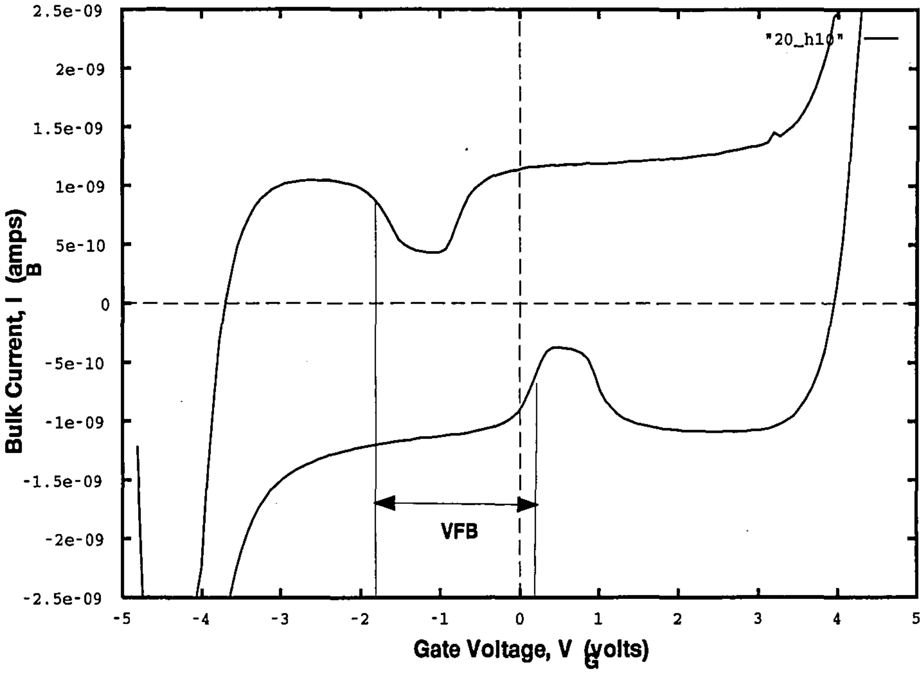


Figure 4.16: A Flatband Voltage shift of 1.8 V with nitride layer deposited at 725° C and area of 0.01 cm$^2$ (Fig. 4.7 Sample F)

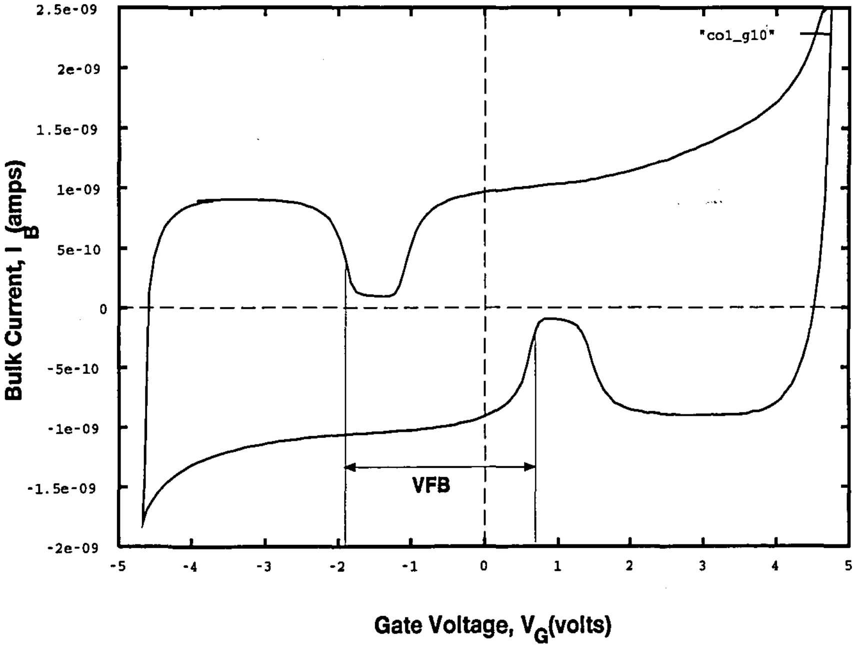


Figure 4.17: A Flatband Voltage shift of 2.5 V with nitride layer deposited at 650° C and area of 0.01 $cm^2$ ( Fig. 4.7 Sample G)

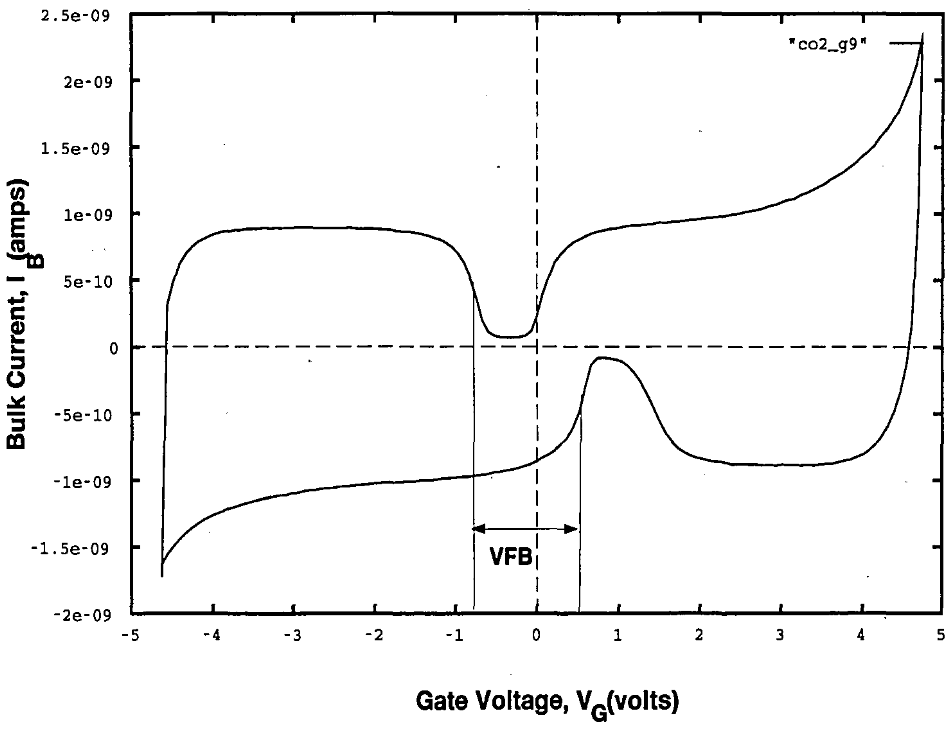


Figure 4.18: A Flatband Voltage shift of 0.9 V with nitride layer deposited at 680° C and area of 0.01 $cm^2$ ( Fig. 4.7 Sample H)

# Chapter 5

# Conclusions

## 5.1 Conclusions of this Thesis

The following conclusions can be made for this thesis

### 5.1.1 AFM Measurements

- For thick $SiO_2$ or $Si_3N_4$ samples, Atomic Force Microscopy is the best among all Scanning Probe Microscopes for studying the surface topography. The Scanning Tunneling Microscope can be used for bare Si samples with no native oxide or for samples with very thin oxide so that current can tunnel to the tip. Thus, for samples of $Si_3N_4$ of $\approx 60$ Å thickness, an insulating surface, Atomic Force Microscopy works the best.

- The intermittent-contact mode of the AFM is better than the contact and non-contact mode for $Si_3N_4$ samples. In contact mode, the $Si_3N_4$ tip touches the $Si_3N_4$ sample resulting in wear of the tip and yielding poor surface topography measurements. The non-contact mode may leave dust particles on the surface resulting in surface roughness values higher than expected. The intermittent-contact mode does not drag the tip on the surface, preventing wearing of the tip. It also touches the surface periodically thus imaging the actual surface and not dust particles on the surface.

- Due to scaling of devices, surface roughness of the dielectric layers is important. The differences in electric field in the dielectric effects charge storage and leakage from the nitride layer.

- Deposition temperature of nitride affects the surface roughness of the nitride layer. In contact mode, at 680° C, the RMS surface roughness of nitride layer was found to be minimum as compared to RMS surface roughness of nitride deposited at 650° C and 725° C. In intermittent-contact mode, the RMS surface roughness of nitride deposited at 650° C was minimum (Appendix B).

- Smaller ratio of $NH_3$:$SiCl_2H_2$ flow during nitride deposition resulted in a rougher surface of the $Si_3N_4$ layer.
- Different areas of the sample had the same surface roughness unless one area had a dust particle, which when imaged gave a different value of surface roughness.

### 5.1.2 Processing Technology

- Nitride deposition rate varies with different deposition temperatures. At 600° C, there was no reaction between $SiCl_2H_2$ and $NH_3$ at a pressure of 300 m torr. At 650° C 67 Å of $Si_3N_4$ was deposited in 38 minutes, at 680° C, 67 Å of $Si_3N_4$ was deposited in 19 minutes and at 725° C the nitride was deposited in 7 minutes.

### 5.1.3 Electrical Measurements

- The flat band voltage shift of capacitors varied with nitride deposited at different temperatures. 650° C deposited nitride capacitors exhibited the maximum programming shift followed by capacitors with nitride deposited at 680° C and then capacitors with nitride deposited at 725° C.
- The contact mode surface roughness data does not correlate with the flat band voltage shift. But, the intermittent contact mode surface roughness correlates well with the LVR measurements. Smaller value of RMS surface roughness gave larger flat band shift in the LVR measurements.

## 5.2 Recommendations for Future Work

- For future work, the surface roughness of the tunnel oxide and blocking oxide could be studied.

- A correlation between deposition temperature, surface roughness and flat band voltage shift could be established.
- The physical mechanisms correlating the surface roughness of the nitride layer and its effect on electrical characteristics of the device need to be understood. An analytical model for the study presented in this thesis could be formulated.
- The effect of surface roughness of the ONO dielectric on the electrical characteristics of SONOS transistors could be studied.

# Appendix A

# AFM Measurement and Sample Preparation

The AFM used for surface roughness measurements is the Park Scientific Instruments' Scanning Force Microscope SFM-BD2. Few specifications about the instrument.

Here are steps on how to take measurements with the AFM.

## A.1 Taking images from the AFM

1. Switch on computer and monitor.
2. Switch on color video monitor and printer.
3. Double click on PSI Data Acquisition (PSI-acq) icon to open the application.
    - By default Change Sample Mode.
    - Click on it.(Probe head is raised by Z stage. XY sample stage moves forward.)

| Mode | Z Resolution | Y Resolution | X Resolution |
|---|---|---|---|
| Contact | 0.2 Å | 1-2 Å | 1-2 Å |
| Non Contact | 10 Å | 50 Å | 50 Å |
| Intermittent Contact | 10 Å | 50 Å | 50 Å |

Table A.1: AFM (Park Scientific Instrument) Resolutions

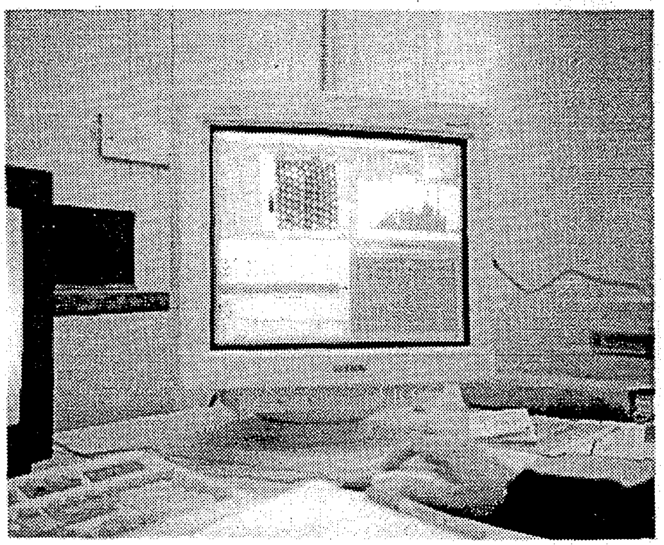


Figure A.1: Analysis of image to obtain surface measurements and statistics

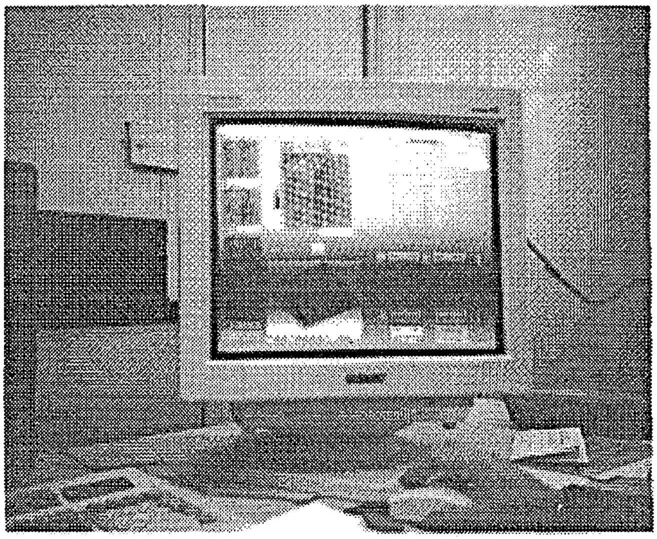


Figure A.2: Processing of data for a 3D image

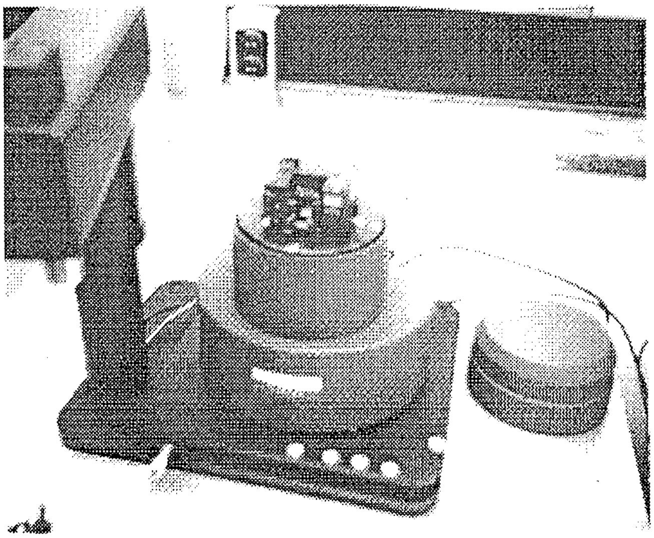


Figure A.3: AFM setup : Head, Sample Stage and Microscope

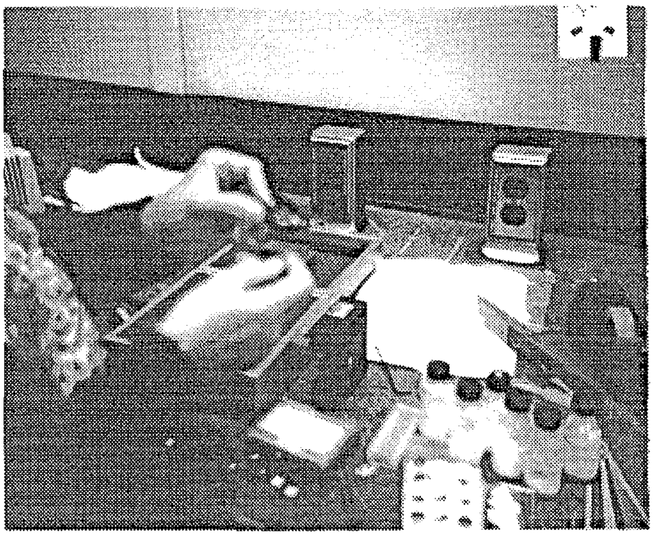


Figure A.4: AFM peripherals : Cartridge, Cassette and Tip

- Secure sample to one of the sample mounting disks supplied with the instrument.(Double sided scotch tape can be used).
- Slide the sample mounting disk into sample holder.Sample holder is magnetic. Scanner is beneath it.

4. Loading Probe
   - Probe comes pre-mounted on a ceramic cassette(50 disposable cassettes).
   - Mount cassette on a cartridge.
   - Raise probe head before loading or removing a cartridge.
   - Put the cartridge in by hand.
5. Auto Approach
   - In change sample mode click and hold Auto Approach button.
   - Deflection sensor alignments are checked.
   - Adjust laser intensity by laser beam steering screws.(3 to 4 red lights-laser intensity indicator should be on)
   - Adjust PSPD (position sensitive photo detector) adjustment screws to get green light in laser position indicator.
6. After auto approach move to take data and scan.

## A.2 Sample Preparation

1. Starting Material: p substrate $< 100 >$, 20-30 Ω-cm.,3 inch diameter
2. Active Area
   (a) Furnace Clean
   5:1:1 DI Water:Ammonium Hydroxide:Hydrogen Peroxide, 75° C, 5 min.
   5:1:1 DI Water:Hydrochloric Acid:Hydrogen Peroxide, 65° C, 5 min.

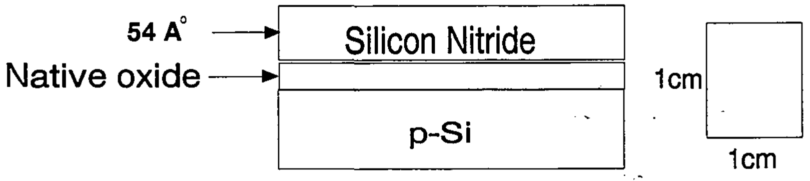
(b) The following three steps are performed on different wafers.

- 50 Ånitride
  LPCVD:0.3 torr,100sccm $NH_3$, 10 sccm $SiCl_2H_2$,650° C,38 min
- 50 Ånitride
  LPCVD:0.3 torr,100sccm $NH_3$, 10 sccm $SiCl_2H_2$,680° C,19 min
- 50 Ånitride
  LPCVD:0.3 torr,100sccm $NH_3$, 10 sccm $SiCl_2H_2$,725° C,7 min

3. Photo and hard baking of wafers.

4. Dicing of wafers into squares of area 1 $cm^2$.

5. Photo stripping



Cross section of sample    Top view of sample

Figure A.5: A typical sample with 54 Å of Silicon Nitride on it

# Appendix B

# Digital Instruments AFM Data

Three samples were sent out to Digital Instruments for surface roughness measurements in the contact and intermittent contact mode. The samples are as follows:

1. Sample I
   (a) Starting Material: p substrate < 100 >, 20-30 Ω-cm.,3 inch diameter
   (b) 18 Å$SiO_2$
   (c) 47 Å$Si_3N_4$
   $NH_3$: $SiCl_2H_2$ 10:1, 650° C
2. Sample II
   (a) Starting Material: p substrate < 100 >, 20-30 Ω-cm.,3 inch diameter
   (b) 18 Å$SiO_2$
   (c) 45 Å$Si_3N_4$
   $NH_3$: $SiCl_2H_2$ 10:1, 680° C
3. Sample III
   (a) Starting Material: p substrate < 100 >, 20-30 Ω-cm.,3 inch diameter
   (b) 18 Å$SiO_2$
   (c) 49 Å$Si_3N_4$
   $NH_3$: $SiCl_2H_2$ 10:1, 725° C

| | $R_{p-v}$ | Rms Roughness | Avg. Roughness |
|---|---|---|---|
| 650° C | 31.98 Å | 3.29 Å | 2.61 Å |
| 680° C | 31.35 Å | 3.41 Å | 2.71 Å |
| 725° C | 51.58 Å | 3.92 Å | 3.04 Å |

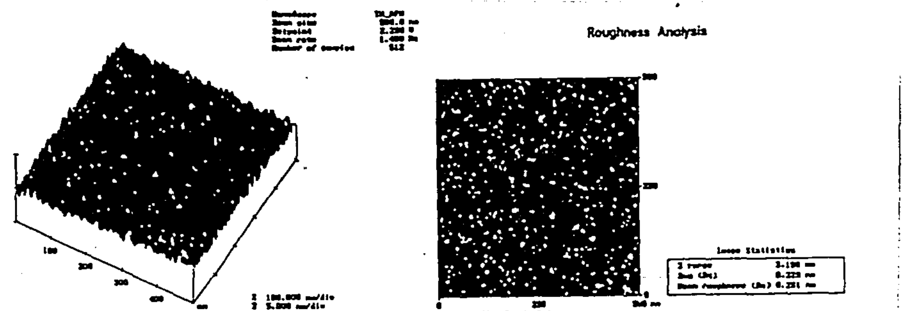
Table B.1: Tapping or Intermittent Contact mode (500 nm x 500 nm)

| | $R_{p-v}$ | Rms Roughness | Avg. Roughness |
|---|---|---|---|
| 650° C | 28.6 Å | 3.26 Å | 2.59 Å |
| 680° C | 31.58 Å | 3.31 Å | 2.63 Å |
| 725° C | 90.54 Å | 4.10 Å | 3.08 Å |

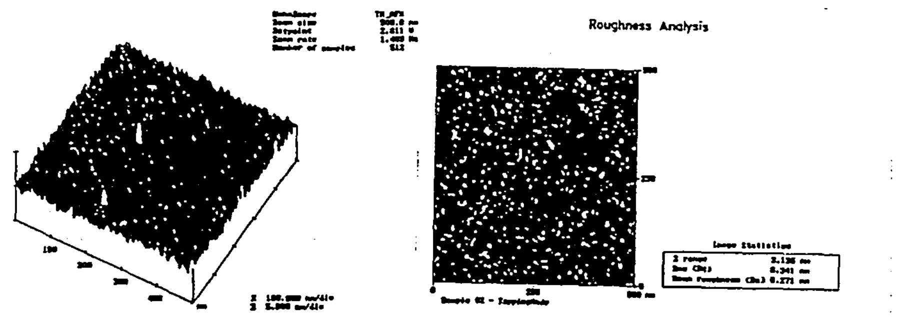
Table B.2: Tapping or Intermittent Contact mode (1000 nm x 1000 nm)

| | $R_{p-v}$ | Rms Roughness | Avg. Roughness |
|---|---|---|---|
| 650° C | 21.26 Å | 1.9 Å | 1.49 Å |
| 680° C | 23.54 Å | 1.73 Å | 1.36 Å |
| 725° C | 29.27 Å | 3.01 Å | 2.40 Å |

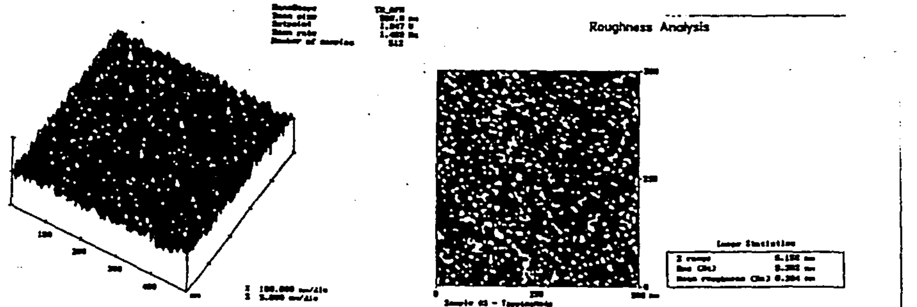
Table B.3: Contact mode (500 nm x 500 nm)



Sample #1 — TappingMode



Sample #3 — TappingMode



Sample #2 — TappingMode

Figure B.1: Tapping mode (500 nm x 500 nm)

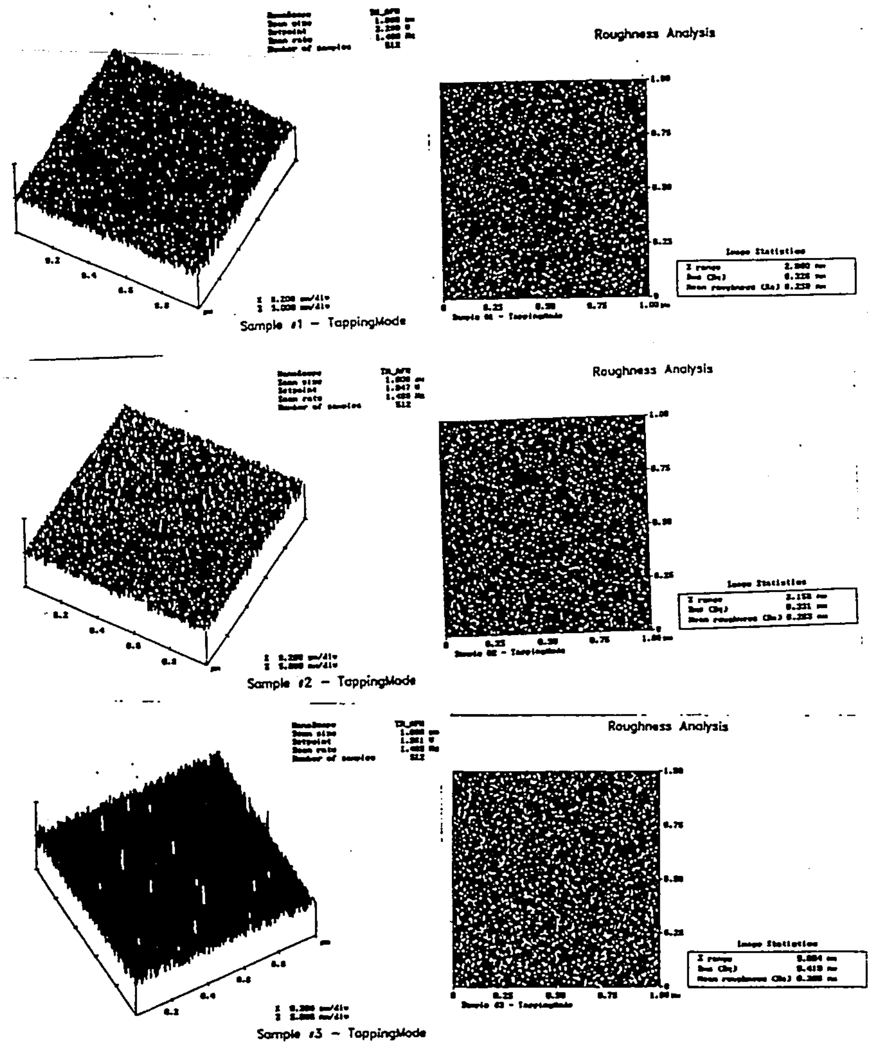
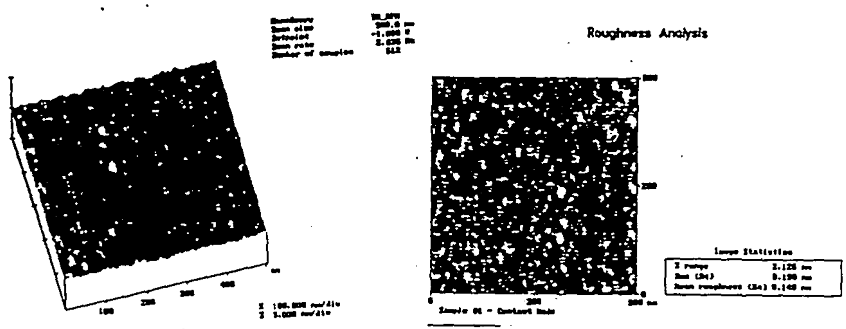
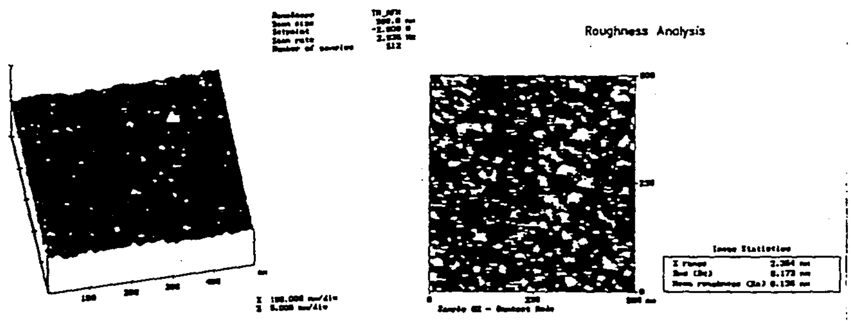


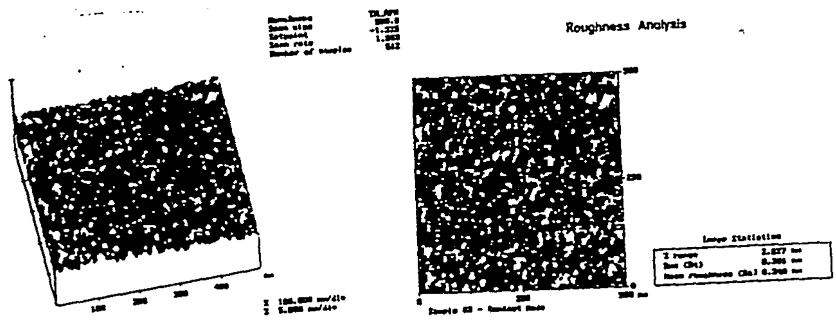
Figure B.2: Tapping mode (1000 nm x 1000 nm)


Roughness Analysis
Image Statistics
0
250
500 nm

Sample #1 – Contact Mode


Roughness Analysis
Image Statistics
0
250
500 nm

Sample #2 – Contact Mode


Roughness Analysis
Image Statistics
0
250
500 nm

Sample #3 – Contact Mode

Figure B.3: Contact mode (500 nm x 500 nm)

# References

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# Vitae

Ansha Purwar was born December 7, 1971 in Allahabad, India to Arun and Sushma Purwar. She went to Birla Institute of Technology and Science, Pilani, India from August 1989 and graduated with a Bachelor's Degree in Electrical Engineering in May 1993. She received admission at Lehigh University to pursue graduate studies in Solid State Devices. During her graduate studies, she has been awarded the ESTY - University Fellowship and a Sherman Fairchild Fellowship. She is an IEEE student member and a member of Women Engineering Society. Her interests include semiconductor device physics, with special interest in Scanning Probe Microscopy for studying semiconductor surfaces and SONOS nonvolatile memory application.

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