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Optimization of germanium implanted MOS devices for VLSI

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Optimization of Germanium Implanted MOS Devices For VLSI

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OPTIMIZATION OF GERMANIUM IMPLANTED MOS DEVICES

FOR VLSI

by

Martin Krajci

A Thesis

Presented to the Graduate and Research Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

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Certificate of Approval

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_9/26/95_
Date

Thesis Advisor

Co-Advisor

Chairperson of Department

Acknowledgements

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Abstract

Hot electron effect which causes degradation of MOS devices becomes more of a concern when the devices become smaller, such as is the case in very large scale integration (VLSI). Hot electrons is a name assigned to electrons which gain enough energy in the channel to surmount the Si/SiO_2 barrier and enter the oxide. Among several possible approaches to reduce this effect, germanium doping seems to be very promising. It was believed that it is germanium in the region of Si/SiO_2 interface which acts as additional scattering mechanism and thus reduces the hot electron effect. On the other hand, past studies showed that Ge presence in the oxide also increases electron trapping rate in the oxide and surface state density. In this study, cases of pre- and post- Ge implantation oxidation as well as their combinations were analyzed on MOS capacitors. Avalanche injection was used to measure the susceptibility of a device to hot electron degradation, and the method was also used to measure electron trapping rate in the oxide. The CV and QV methods were used to estimate the interface trap density. SIMS was used to study Ge concentration profiles in Si/SiO_2 samples. The results showed that the hot electron effect reduction due to Ge does not depend on the presence of Ge in the Si/SiO_2 interface region but on the presence of Ge in the bulk oxide. The results confirmed belief that presence of Ge in the oxide increases the electron charge trapping rate and that presence of Ge in the region of Si/SiO_2 interface increases the interface trap density. SIMS results also showed that Ge atoms have a strong tendency to migrate from SiO_2 into the silicon, where they pile up near the interface.

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Chapter 1: Introduction and Background

1.1. Introduction

With the advancement of the semiconductor technology which has currently progressed to very large scale integration (VLSI), development of smaller and faster devices has become the trend in the industry. These two factors go hand in hand, since the speed of a device is closely related to its physical size. Smaller devices have smaller gate and parasitic capacitances and thus can operate faster. Smaller devices allow also placing more devices into a single functional block and thus reducing the price. And with a smaller number of integrated circuit packages, system performance and reliability can be enhanced.

1.2. Scope of This Thesis

This chapter briefly introduces the subject of the hot electron effect and concerns associated with it. Common approaches to the hot electron effect reduction are also highlighted. The second chapter lists the methods utilized during this research and talks about the characteristic parameters which can be obtained by these methods. The third chapter presents the results of this research which are summarized in Chapter 4.

1.3. Hot Carrier Effect:

1.3.1. Introduction

As the MOS device becomes smaller, the electric field strength in the channel increases, and the electron's kinetic energy increases sufficiently to overcome the Si/SiO_2 potential barrier and cause appreciable electron emission into the oxide. These electrons with high kinetic energy are often referred to as "hot" electrons. It appears that this leads to generation of interface traps (surface states) and gives rise to a gate current. This is obviously a degradation of the device. The gate current I_g is commonly used as a measure of the device degradation.

As the electrons gain energy in the high field region flowing from source to drain, their energy reaches maximum around the drain and that is the region where most of the electrons surmount the potential barrier.

The source of hot electrons other than the channel current can also be the substrate current. Electrons either come from the bulk substrate region or are generated at the depletion region and drift towards the Si/SiO_2 interface. They gain energy from the high field in the depletion region. The hot electrons generated by high field in the substrate are referred to as the substrate hot electrons. The substrate hot electron effect is usually not significant in MOSFETS, unless the device has a heavily doped substrate and thus a much larger probability of a hot electron emission into the oxide, or the incident current is large (in cases such as elevated temperatures, forward biased junctions, or charge injection into the substrate from charge pumping of large MOS capacitors.)

1.3.2. Physical Model

The electrons gain energy from the electric field and accelerate towards the surface. At low fields their energy is too small to overcome the conduction band edge due to inelastic scattering. At about 20 kV/cm, optical phonon emission dominates the scattering process and the electrons' drift velocity saturates. At over 100 kV/cm, the electron starts to gain more energy than it can lose in the scattering and the electron-lattice equilibrium does not hold anymore.[1] After the electron's energy reaches a threshold value ϕ_I, the impact ionization becomes an important energy-loss mechanism. The combined mean free path can be expressed in terms of the contributions from optical phonon scattering (λ_p) and impact ionization (λ_I) as

$$\frac{1}{\lambda} = \frac{1}{\lambda_I} + \frac{1}{\lambda_p} \qquad (1.1)$$

The distance from the Schottky-lowered potential peak to the conduction band edge, X_c, represents most of the important parametric relationships. For example, increasing the substrate bias causes X_c to decrease. If we ignore tunneling and phonon absorption, for any $X < X_c$ the electrons have no chance to be emitted. If we assume that the most probable trajectory for an electron is the one with no scattering, the emission probability is

$$P = A e^{\frac{-X_c}{\lambda}}, \qquad (1.2)$$

where A is a normalization constant, and λ is the combined mean free path of the mean free paths due to optical phonon scattering and impact ionization.

1.3.3. Static Degradation

There are three distinct regions for the carriers of the gate current. For low gate voltages ($V_G \ll V_D$), the gate current is hole-dominated. The main damage species in this region are interface traps, trapped holes, and neutral electron traps. Obviously, this damage is not immediately apparent, since the electron traps show no charge.[2]

In the region when $V_G = V_D/2$, the substrate current is maximum and both holes and electrons are injected into the gate while interface traps are generated. At higher gate voltages, the gate current is predominantly carried by the hot electrons which fill the neutral electron traps in the gate.[3]

1.3.4. Dynamic Degradation

As shown by Mistry *et al.*, at AC operation the resulting stress damage is a combination of factors from all three regions for the DC stress.[2] The proposed AC stress damage function consisting of the three damage mechanisms account for the so-called enhanced hot carrier degradation.

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1.4. Hot Carrier Effect Reduction Techniques

1.4.1. Lightly Doped Drain (LDD)

Since the hot carrier effects are caused mainly by the high electric field near the drain, a common way to reduce it is by tailoring the doping profile in that region. The LDD (lightly doped drain) structure is currently the most often used technique. The idea is introducing a narrow self aligned lightly doped region in the area between the heavily doped drain and the channel area under the gate (Figure 1.1). In a conventional device, the electric field shows a strong peak in the region of the metallurgical junction and drops quickly to zero in the highly conductive n^+ region. In an LDD device, the peak of the electric field is extended and drops off slowly in the lightly doped region (Figure 1.2). Since the area of the graphs of electric fields for both conventional and LDD device has to be the same, the maximum field is reduced for a LDD structure. However, the introduction of a lightly doped region adds a series resistance between the channel and the drain. With scaling the channel to less than 0.5 microns, this resistance is not negligible. Additional problems were reported with the LDD structure as it is more susceptible to hot electron damage due to localized interface traps and trap charge located above the lightly doped drain.[4]
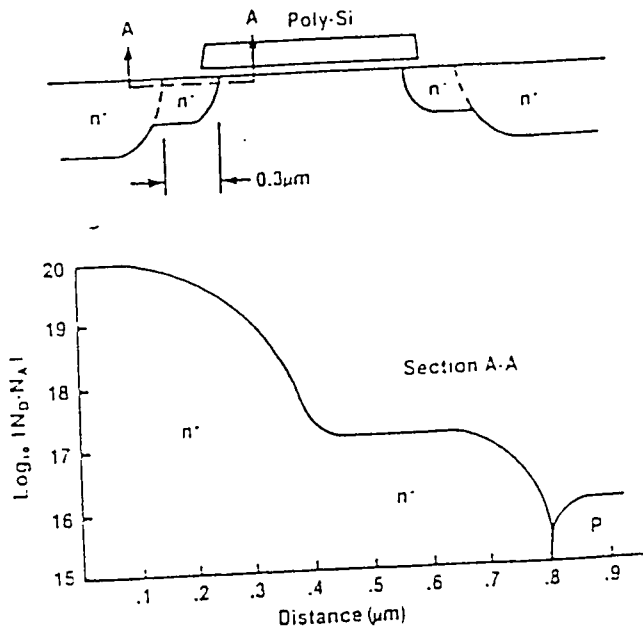
Figure 1.1 LDD Structure.
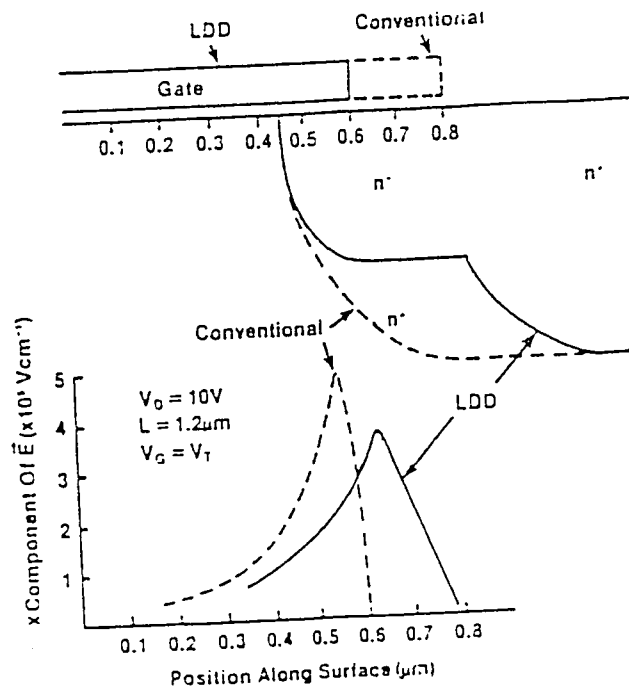
Figure 1.2. Magnitude of the electric field for the LDD and conventional devices at the Si/SiO₂ interface.

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1.4.2. Reduction of operating voltage

Another approach to reducing the hot carrier effect is reducing the electric field by lowering the operating voltage. The standard has dropped from 5V to 3.3V, and recently a 2.5V standard was introduced to the state-of-the-art CMOS devices. However, the size of the gate tends to decrease much faster than the operating voltage, and thus the potential for device degradation due to the hot-carrier effects is still increasing. In addition, in BiCMOS circuits, the reduced V_{dd} required for MOSFETs is incompatible with bipolar devices.

1.4.3. Other Methods

One approach to reduce the degradation due to hot carriers is to decrease the charge trapping in the insulator.

Ma *et al.* found that adding fluorine to the oxide significantly reduces the hot-electron induced interface traps.[5] They claimed that the bond strain distribution near the Si-SiO$_2$ interface may be decreased by the presence of fluorine in the SiO$_2$.

Xie and Young found that fluorine implantation can reduce slow interface traps and eliminate the turn-around effect during avalanche injection.[6]

Kouvastos, *et al.*, studied incorporation and chemical bonding of fluorine introduced into SiO$_2$ thin films by NF$_3$-enhanced oxidation of Silicon.[7] They observed fluorine bonding in the oxide network in the area of oxidizing interface and passivating the interface trap centers.

It was also observed that the incorporation of nitrogen at Si-SiO$_2$ interface reduces the hot-carrier effect.[8] The so-called reoxidized nitride oxide (RNO) acts as a barrier for impurity penetration into the SiO$_2$ and reduces the interface trap generation. However, electron trapping is inherent in nitride oxide and reoxidation is necessary to reduce the hydrogen concentration. This reoxidation reduces the degradation of V_t and g_m.

1.4.4. Germanium doping:

A novel idea to suppress hot-electron effects was introduced by Ng *et al.* The technique is based on introduction of neutral germanium atoms in the channel region.[9] Ge atoms, being neutral, do not change the field and thus do not change significantly the carrier mobility. However, they can introduce the additional scattering mechanisms for the "lucky" hot carriers. They explain it by the fact that the Ge atoms are larger and thus introduce the added scattering. The added scattering is often attributed also to the fact that SiGe has smaller energy bandgap than Si. Conceptually, the mobility of the channel carriers is largely determined from surface scattering whose mean free path is on the order of the inversion-layer thickness. A small number of "lucky" hot carriers escape some of these scattering events and thus have a longer mean-free path. The intention here is to introduce an additional scattering mechanism with a mean free path value larger than the one seen by the majority of the channel carriers. Then the MOSFET channel current is not modified, but the the "lucky" hot carriers lose energy due to the added scattering.
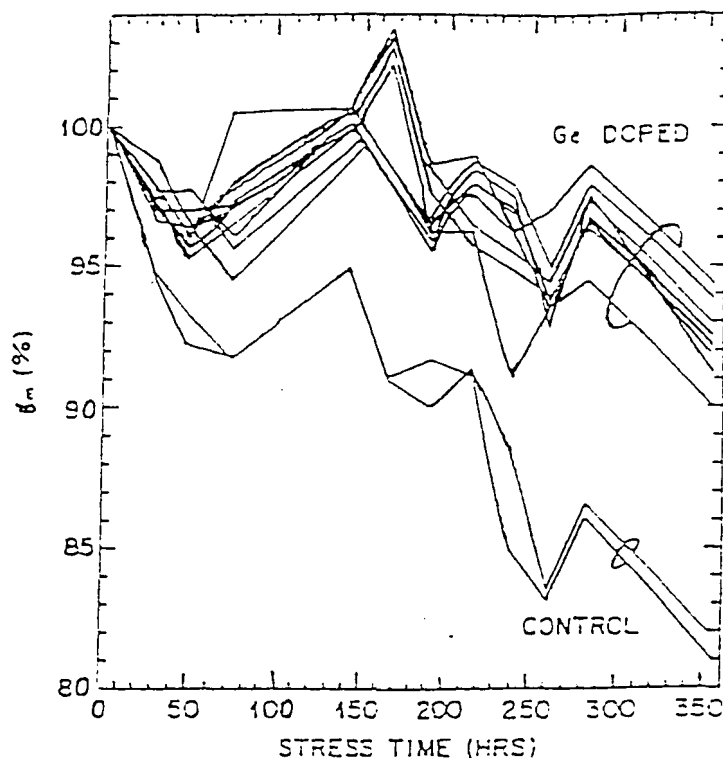
Figure 1.3 Transconductance g_m in the triode region relative to the initial value as a function of stress and time for the control devices and Ge-doped structures.

They showed that by introducing Ge impurities in the channel region of a Si MOSFET, the degradation rate under voltage stress is significantly reduced without modifying the initial characteristics (Figure 1.3).

Lin elaborated on this idea and showed that the population of hot carriers in Si is strongly reduced by the Ge implantation.[10] In his interface trap density study he found that when the Ge dose is equal to 10^{14} cm^{-2} the interface trap density increases. To obtain the maximum hot carrier reduction without increasing the interface trap density, the

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implantation dose should be less than 10^{14} cm^{-2}. He also studied the effect of the location of the peak of the Ge implantation and found the optimal location at the Si-SiO$_2$ interface (Figs. 1.4, 1.5).

Lin also showed, in his charge trapping study, that the trapping rate of the Ge implanted samples in the SiO$_2$ increases with the Ge dose. His explanation for this fact was that the increase in trapping rate results from the formation of GeO, since the Ge bonds that are not involved in the network formation act as very efficient electron traps. In a modified process, Lin implanted Ge before oxidation. His results showed that even though the trapping rate was reduced (Fig. 1.6), the hot-carrier reduction effect also diminished (Fig. 1.7), and the interface trap density increased.[2]
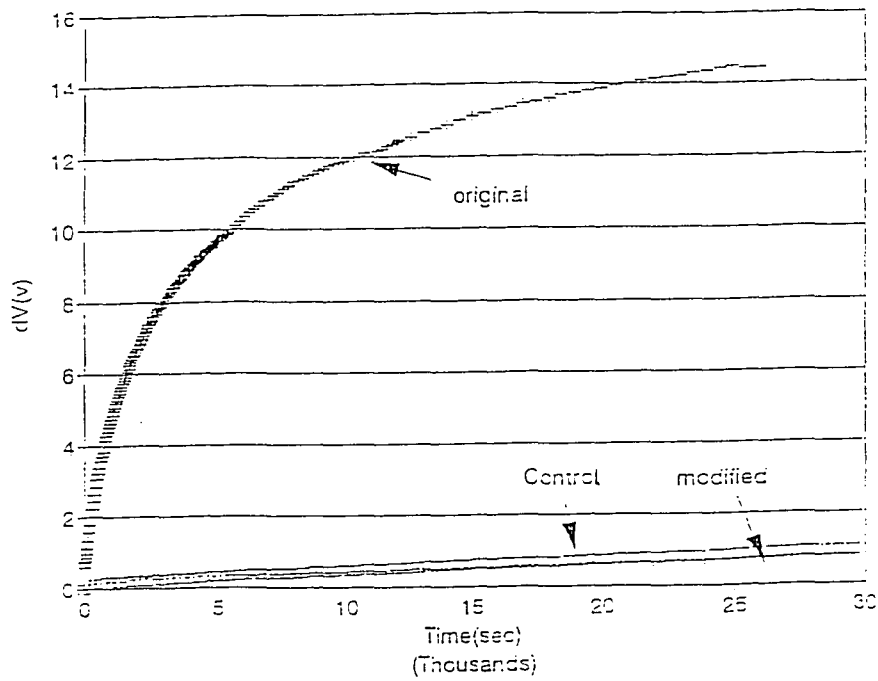
Figure 1.4 Avalanche injection current versus gate voltage curves show significant hot electron effect reduction for the case when germanium was implanted into the SiO_2. This reduction is weak for the case when the sample was oxidized only after germanium was already implanted in the silicon.
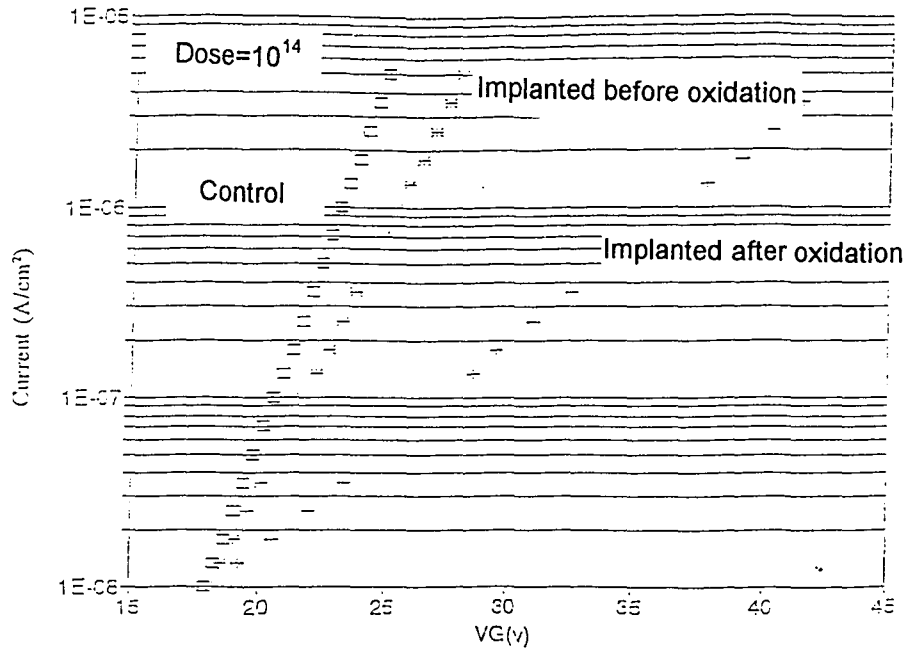
Figure 1.5 Flatband voltage shift versus time curves show significant increase in electron trapping rate for the case when germanium was implanted into the SiO_2. The electron trapping rate remains low for the case when the sample was oxidized only after germanium was already implanted in the silicon.

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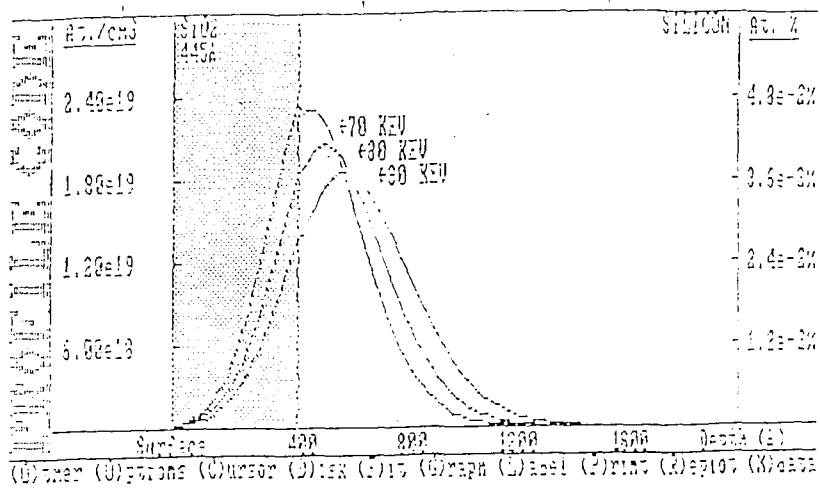
Figure 1.6 Simulated Ge profiles for various implantation energies in SiO₂/Si.
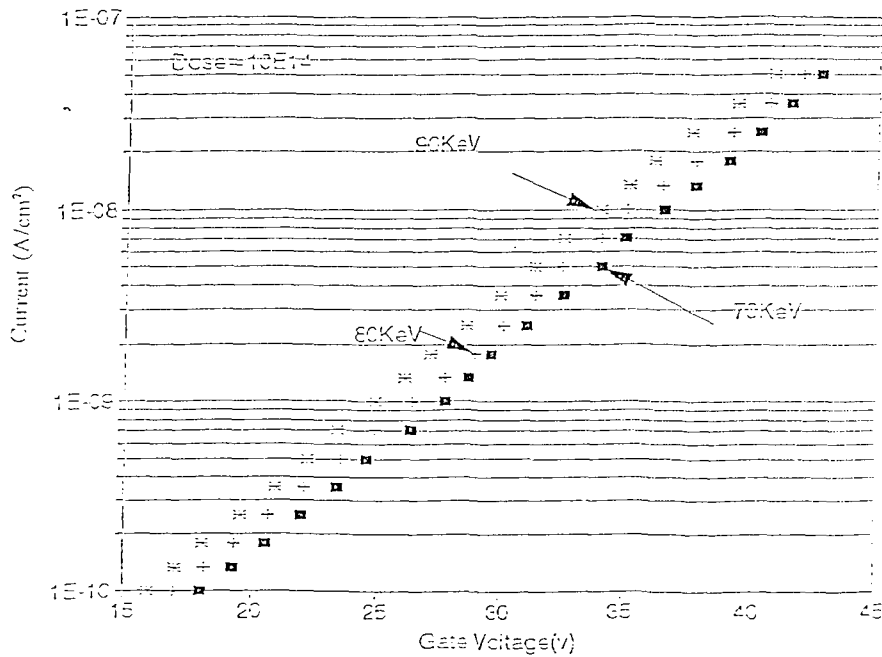
Figure 1.7 Avalanche injection current versus gate voltage curves show better hot-electron effect reduction if the peak of implantation is moved closer to the Si/SiO₂ interface.

Chapter 2: Experimental Procedures and Analytical Techniques.

2.1. MOS Capacitor:

MOS Capacitor is the simplest MOS structure and the structural basis for all MOS devices.

2.1.1. Manufacturing MOS capacitors:

The MOS capacitors for this set of experiments are manufactured on boron-doped p-type Si wafers. After the initial oxide was thermally grown on them, the wafers were sent for Ge implantation. Then if additional oxidation was required, it was performed. The wafers were then placed in an evaporator for evaporation of aluminum. The capacitors were then defined using a photolithography process, and the unwanted aluminum etched. Finally, the samples were thermally annealed.

2.2. High Frequency CV Measurement

The high frequency Capacitance-Voltage technique is a very useful method of analysis of MOS capacitors. The capacitance is defined *as C=dQ/dV*. It is a change of charge due to a change of voltage. The high frequency curve is obtained when the inversion charge is unable to follow the ac voltage. However, the dc bias should not be changed rapidly with insufficient time for inversion charge generation because then a deep depletion curve results.

The high frequency semiconductor capacitance in inversion is difficult to calculate exactly, even though exact expressions do exist. The following expression is accurate to 0.02% in strong inversion:

$$C_{S,HF} = \sqrt{\frac{q^2 K_S \varepsilon_0 N_A}{2kT\left\{2|U_F| - 1 + \ln\left[1.15\left(|U_F| - 1\right)\right]\right\}}},\qquad (2.1)$$

where $U_F = \dfrac{q\phi_F}{kT}$ is the Fermi potential. The flatband voltage is determined by the metal-semiconductor workfunction difference ϕ_{MS} and the various oxide charges through the equation

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{\gamma Q_m}{C_{ox}} - \frac{\gamma Q_{ot}}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}},\qquad (2.2)$$

where Q_f is the fixed oxide charge, Q_m mobile oxide charge, Q_{ot} is charge trapped in the oxide, and Q_{it} is the interface state charge. ϕ_{MS} is the metal-semiconductor workfunction, and ϕ_s is the semiconductor workfunction.

The effect of oxide charges on the flatband voltage shift is the greatest when the charge is near the Si-SiO$_2$ interface since it images all of its charge in the semiconductor. When the charge is located at the gate-oxide interface, it images all of its charge in the gate and has no effect on the flatband voltage. To account for the possible charge distribution throughout the oxide, a factor γ is introduced, which is defined by

$$\gamma = \frac{\int_0^{W_{ox}} (x/W_{ox})\rho(x)dx}{\int_0^{W_{ox}} \rho(x)dx},\qquad (2.3)$$

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where $\rho(x)$ is the oxide trapped or mobile charge per unit volume, and x is defined as the distance from the oxide-gate interface (i. e. $x=W_{ox}$ at the oxide-semiconductor interface.) The various charges and the workfunction difference result usually in a shift of the CV curve. The voltage shift can be theoretically evaluated at any capacitance; however it is usually measured at the so-called flatband capacitance C_{FB}., which is defined as the capacitance at the flatband voltage V_{FB}.. The flatband voltage is zero for an ideal high frequency CV curve (i. e. Q_{it} is assumed to be zero.)[11]

In the high frequency CV curve measurement for this experiment, a DC voltage is swept over a certain range with a 1 MHz small signal superimposed on it. Capacitance of the sample is measured at each point of the sweep and the CV curve is constructed. In our setup, we used a commercially available device 401 CV Plotter by Princeton Applied Research which incorporates all the features necessary to obtain a high frequency CV curve and provides a DC analog voltage outputs linearly proportional to the applied DC voltage and the corresponding measured capacitance, both as a function of time. These voltages were then sampled and recorded by a personal computer using a Keithley DAS-1600 data acquisition card.

2.2.1. Parameters extracted from a high frequency CV curve

The experimental CV curve can be compared with an ideal CV curve and the following parameters can be extracted.

The *fixed oxide charges* (Q_f) cause rigid shifts in the flatband voltage which can be used to determine the charge density.

The energy states of the *interface traps* are distributed throughout the silicon bandgap. As the gate voltage is swept from accumulation from inversion, it moves the Fermi level, it has to charge both the traps in the interface and in the semiconductor (since $Q_G=Q_S+Q_{it}$), assuming zero oxide charges, and therefore the charge state changes. As a result, the magnitude of the interface traps charge depends on the gate voltage. The presence of the interface traps will result in stretching out the CV curve.[2]
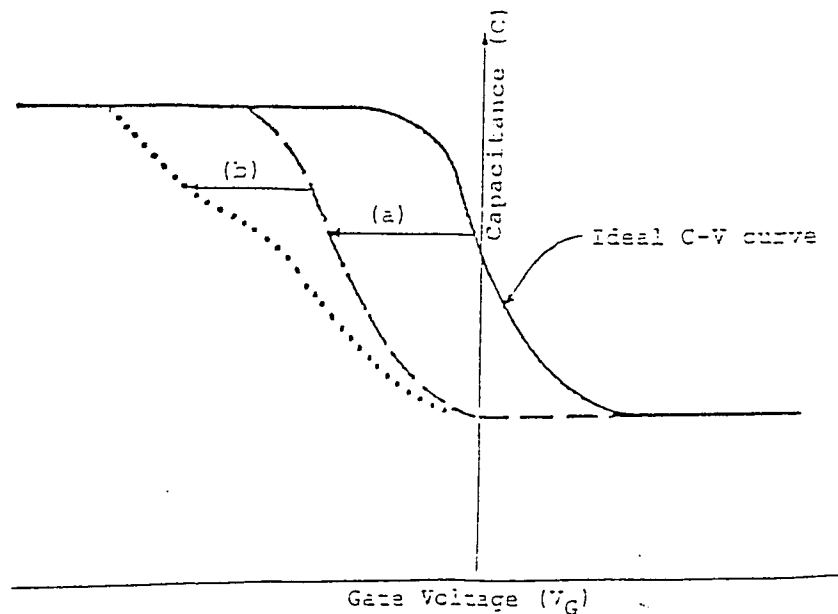
Figure 2.1 High frequency C-V curve for a p-type substrate MOS capacitor. (a) Rigid shift. (b) Stretch-out effect.

2.3. The QV Method

In this method (refer to Figure 2.2), a bias-independent reference capacitor C_i is connected in series with the MOS capacitor. Parasitic capacitances are usually so small that they can be neglected. A bias V_a is applied across C_i in series with the MOS capacitor. After steady state is reached, Va and the voltage across C_i, V_i is measured. The bias across the series is slowly varied point-by-point so that the MOS capacitor is always in a thermal equilibrium. From the known values,

$$V_G = V_a - V_i. \qquad (2.4)$$

Then the measured charge on the MOS capacitor is

$$\Delta Q_G = C_i V_i \qquad (2.5)$$

By varying the applied bias V_a the charge ΔQ_G can be obtained as a function of V_G. Next, the surface potential Ψ_σ is determined, as a difference between V_G and the voltage drop across the oxide, which is equal to Q_G/C_{ox}.[12]

$$\Psi_s = V_G - \frac{Q_G}{C_{ox}} - \Psi_0, \qquad (2.6)$$

where Ψ_0 is the surface potential for $V_G = 0$.

To determine Ψ_0, we assume that in accumulation the interface potential is at the edge of the silicon valence band (for p-type silicon) and for strong inversion it is at the edge of the silicon conduction band. The mid point between the measured values is taken for the mid gap point. This mid gap potential is then used as a reference point.

The obtained curve is then compared with a theoretical curve obtained by Kingston-Neustadter theory[2], and the shift of V_G between the experimental and theoretical curves is determined. This difference is caused by the interface trap charge, fixed charge in the oxide, and the work function difference between metal and SiO_2:

$$C_{ox}\Delta V_G = \Delta Q = Q_f + Q_{it} + \omega, \qquad (2.7)$$

where Q_f is the fixed charge in the oxide, Q_{it} is the interface trap charge, and ω is a constant associated with the work function difference. Since only the interface trap charge Q_{it} is dependent on the gate voltage V_G, the derivative with respect to Ψ_s, will be

$$\frac{\partial(\Delta Q)}{\partial\Psi_s} = \frac{\partial Q_{it}}{\partial\Psi_s}. \qquad (2.8)$$

The interface trap density is then given by an equation

$$D_{it} = \frac{1}{qA} \times \frac{\partial Q_{it}}{\partial\Psi_s}, \qquad (2.9)$$

where A is the area of the gate, and q is an electron charge.[2]

2.3.1. Experimental Setup:

The laboratory setup for the QV measurements is based on the basic QV technique. A voltage independent precision capacitor C_i is connected in series with the MOS capacitor. The measurement procedure is controlled by a personal computer. A 12-bit digital-to-analog converter generates the voltage in the range of ±5V. This voltage is buffered and amplified to obtain the value of V_a in the range of ±10V. The voltage V_i across the bias-independent capacitor C_i is measured by a Keithley 616 electrometer which has an input impedance greater than 2×10^{14} Ω. The analog output of the electrometer is brought to a 16-bit analog-to-digital converter which supplies the value of C_i to the personal computer. This voltage can be measured with a 0.3 mV accuracy. The software written by Ta-Cheng Lin[2] controls the procedure and calculates the results.
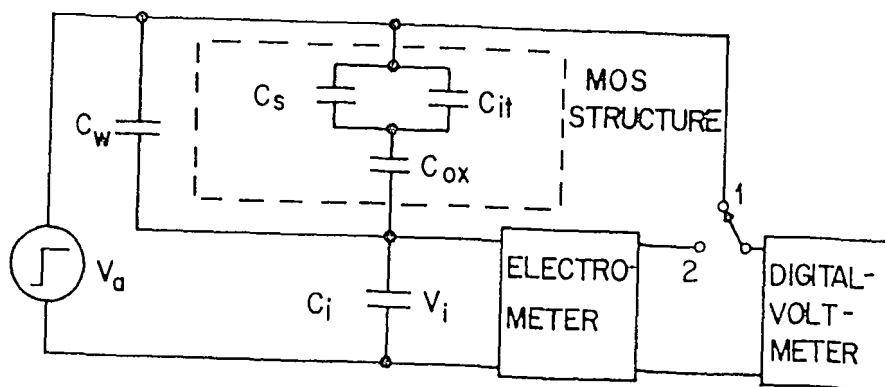
Figure 2.2 Basic QV measurement setup. In this analysis, the capacitance due to interface traps C_{it} is neglected. In our measurement, the voltage V_a is supplied and electrometer measured voltage read by a computer controlled system.

2.4. Avalanche Injection

In avalanche injection, carriers are accelerated by the applied electric field. When the field at the silicon surface reaches the avalanche breakdown value, carriers generated at the surface depletion layer are accelerated to energy high enough so that impact ionization occurs. Some of the electrons have enough energy to surmount the interfacial energy barrier and enter the SiO_2.

2.4.1. Physical Description

The first step towards avalanche injection is producing sufficient band bending to produce an avalanche plasma at the silicon surface of a MOS capacitor. To produce such band bending, the silicon must be driven to deep depletion. Deep depletion is produced by applying a large amplitude ac signal of a high enough frequency for minority carriers to follow. The band bending increases with increasing ac voltage, until the field at the silicon surface becomes high enough for avalanche breakdown. The avalanche plasma is generated once per cycle. A small number of the electrons have sufficient energy to surmount the interface energy barrier. In the oxide, these electrons tend to drift towards the gate driven by the electric field across the oxide, and through the external circuit which can detect a current pulse at each cycle. The injected current has to be emission limited, since significant trapping in the oxide may occur which causes a decrease in the injection current when the electron traps are filled and the field in the oxide is altered.

Figure 2.3 (a) illustrates one cycle of the oxide field produced by the external dc drive. At time $t=0$, the bands are assumed to be flat. The bands continue to bend as the

field increases until deep depletion is reached at time t_l. The avalanche breakdown begins

at the beginning of the time interval t_A. The breakdown is initiated by thermally generated

carriers and occurs at the silicon surface. Figure 2.2 (d) shows band bending at some time

during the avalanche breakdown period t_A, as electrons are excited from the valence band

to the conduction band of the silicon by impact ionization. Most electrons have energies

below the interfacial barrier height, and these form an inversion layer. However, some

have energies higher than the barrier height, and those do not get scattered back into

silicon but enter the oxide where they drift towards the gate. The avalanche injection is

terminated when the oxide field passes its peak value.

During the remainder of the cycle (Figure 2.3), when the band bending decreases

back towards the flatband condition, electrons in the inversion layer generated during the

interval t_A are injected back into silicon where they recombine. During the negative peak

of the cycle, when accumulation occurs, no carriers are injected into the oxide since the

holes at silicon surface see a barrier greater than 4 eV. Thus, the injected gate current is

unidirectional.

The avalanche injection method can be used as a measure of the hot electron effect

in MOS capacitors. Even though quantitative analysis of the energy distribution of hot

electrons is rather complicated, the curves of injection current density versus gate voltage

amplitude can be used to comparatively evaluate the magnitude the hot electron effect.

The avalanche injection method can also be used to obtain parameters related to

oxide charge trapping. The method consists in applying a signal generating avalanche

current through the MOS capacitor. The electrons in the oxide fill up the electron traps

and thus cause a flatband voltage shift. The value of this voltage shift reflects the trap density per unit area in the oxide.
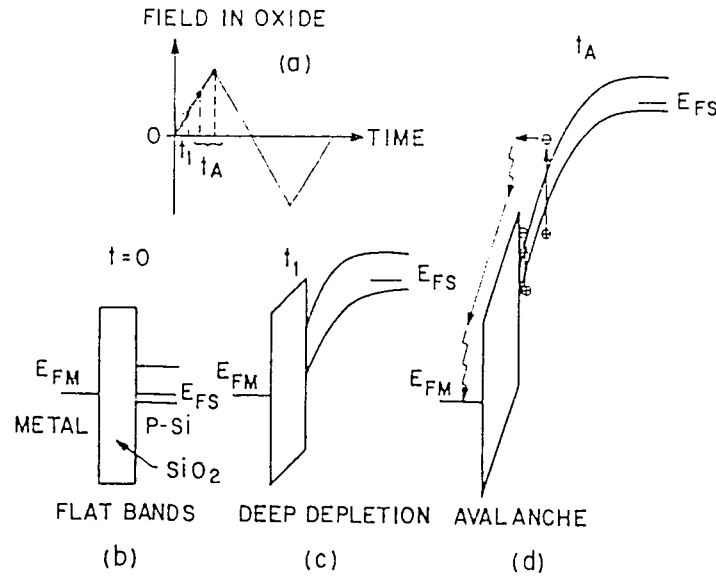
Figure 2.3 Diagram illustrating the principle of avalanche injection of electrons: (a) One cycle of the oxide field is produced by an external saw-tooth generator. (b), (c), and (d) show band bending in the silicon at various times during the cycle.
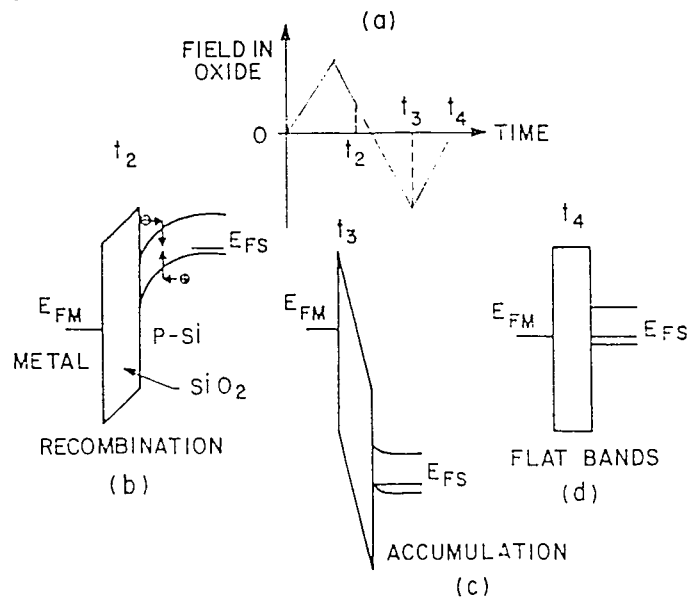
Figure 2.4 Diagram illustrating band bending in the silicon at various times after the avalanche portion of the cycle has been completed.

2.4.2. Experimental Setup

The experimental setup for the avalanche injection was designed by D.R. Young[13]. During the whole process of avalanche charge injection, the average DC current is kept at a constant value. A 150 kHz sawtooth signal is generated by an HP 3310A function generator as the applied source for avalanche injection. The automatic data acquisition system monitors the flatband voltage as a function of time or charge fluence.
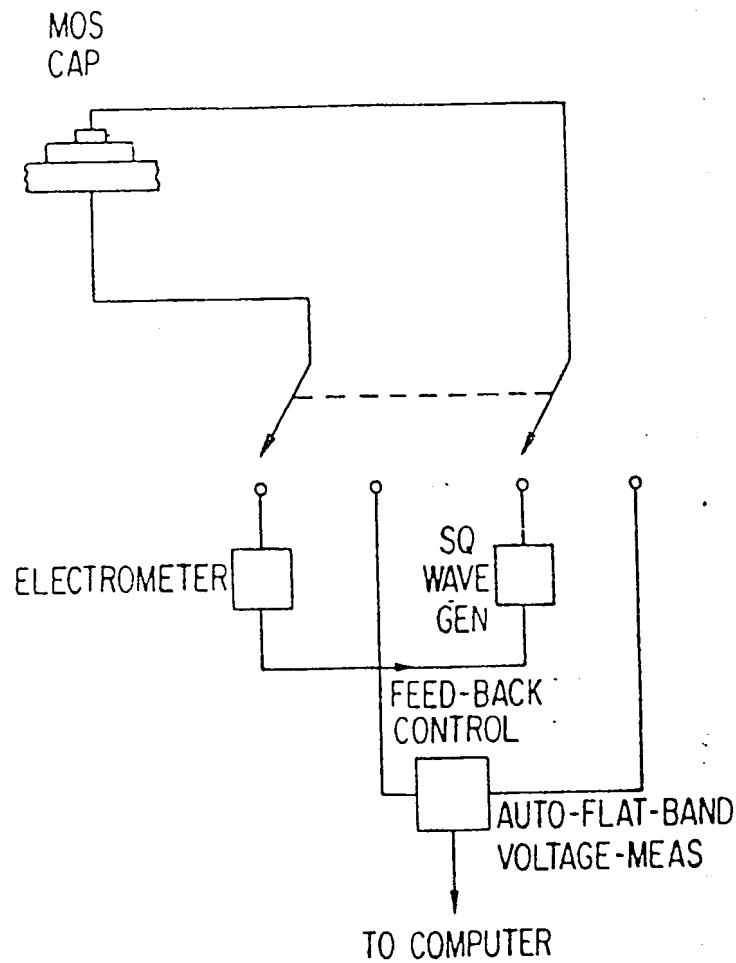
Figure 2.5 Schematic drawing of apparatus used for avalanche injection.

2.5. Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry (SIMS) is a powerful technique for analysis of impurities in solids. The technique relies on removal of material from a solid and analysis of the sputtered ionized species. Most of the sputtered atoms are neutral and cannot be analyzed. Only the ionized atoms can be analyzed in an energy filter and a mass spectrometer.

A SIMS doping concentration is produced by sputtering the sample and monitoring the secondary ion signal of a given element as a function of time. The "ion signal versus time" can be converted to a dopant concentration profile. The time axis is converted to a depth axis by measuring the depth of the crater at the end of the measurement. The crater depth measurement has to be done after each measurement since the sputter rate varies with spot focus and ion current. The secondary ion signal is converted to impurity concentration through standards of known dopant profile. To determine an unknown impurity profile in a sample, the secondary ion signal is calibrated by an implanted sample with a known impurity concentration profile.

Sputtering is a process in which incident ions lose their energy mainly by momentum transfer as they come to rest within the solid. In the process they displace atoms within the sample. Sputtering takes place when atoms near the surface receive sufficient energy from the incident ions to be ejected from the sample. The primary ion loses its energy in the process and comes to rest several tens to hundreds of Å below the sample surface.

SIMS determines the total impurity concentration, not the electrically active impurity concentration. Therefore the results obtained through SIMS may be significantly different from the results obtained in electrical characterization since the sample may contain ions which are not yet electrically activated.

The strength of SIMS lies in its accepted use of dopant profiling. It measures the dopant profile, not the carrier profile, and therefore it can be used for implanted samples before any activation anneals. SIMS also has a high spatial resolution.[11]

We are indebted to Dr. Charles Magee and Ephraim Botnick of Evans East, Plainsboro, NJ, for performing the SIMS depth profiles. Our samples were depth-profiled using instrument 6600 for ^{70}Ge ions. The primary bombarding species used were Ox+ under a 60° angle. The primary ion energy was 3 keV, beam current 100 nA, raster size 300×300 μm, detected area 120×120 μm, with electron beam compensation on. The depth scale was established by measuring the depth of each crater sputtered into the samples by a calibrated profilometer. The overall accuracy of the profiles can be expected in the 15 to 20 % range.

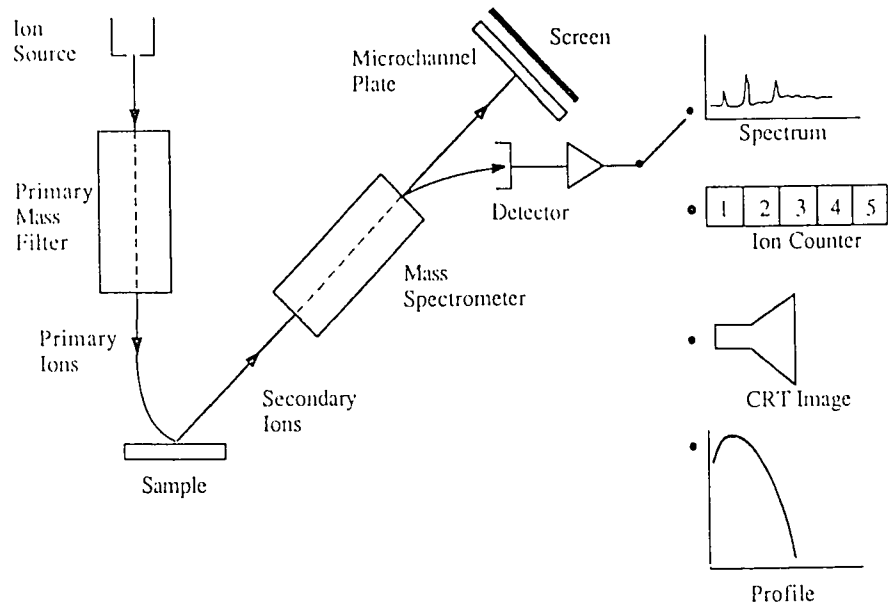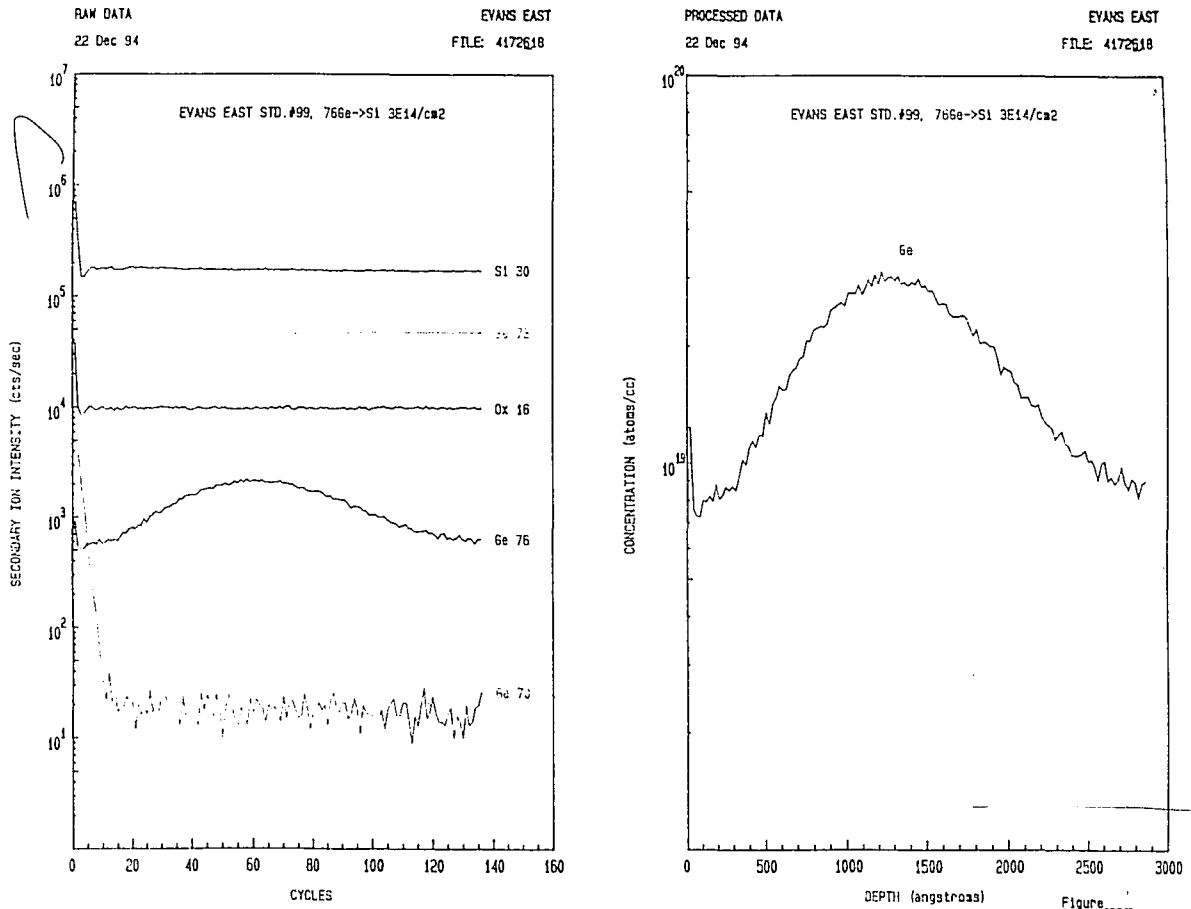**Fig. 2.6** SIMS Schematic.

Figure 2.7 Raw and processed SIMS data. The plots on the left are secondary ion intensity signals in cts/sec versus time cycles. The plot on the right is processed profile of ^{76}Ge concentration versus depth.

Chapter 3: Results and Discussion

3.1. Introduction

The experimental work concentrated on continuation of the work done at Sherman Fairchild Laboratory of Lehigh University by Ta-Cheng Lin.[2] Lin investigated the effects of Ge implantation on the electrical characteristics of MOS devices. He showed that the population of hot carriers in Si was strongly reduced by the Ge implantation. However, for higher Ge implantation doses than $10^{14}/cm^2$ he observed a significant increase in the density of interface traps, and so he established the Ge implantation dose of $10^{14}/cm^2$ as optimal. Further he studied the effect of implantation peak location on the hot carrier injection, and determined the optimum peak location to be at the Si/SiO_2 interface.

Lin's next observation was a dramatic increase in the trapping rate in the oxide in the Ge implanted samples. This rate increased with the Ge dose. To eliminate this negative effect, he proposed a method of implanting a sample before oxidation. However, with this method, even though the charge trapping was significantly reduced, only a very weak reduction of the hot electron effect was achieved.

In my research I attempted to compromise between the method proposed by Lin, and investigate the cases when some of the oxidation was performed before the Ge implantation, and some after. Four cases were studied and compared:

1. Ge implanted at the Si/SiO_2 interface, no additional oxidation. Marked 'None'.

2. Ge implanted at the Si/SiO_2 interface, 3 minutes additional oxidation. Marked '3 min'.

3. Ge implanted at the Si/SiO$_2$ interface, 30 minutes additional oxidation. Marked '30 min'.

4. Control sample, no Ge implanted. Marked 'Control'.

These cases were studied and whenever possible, the results were compared and/or matched with Lin's.

3.2. C-V Characterization

High frequency CV curves were obtained for each of the samples. The results are plotted on Figure 3.1. From the graph it is apparent, that the curves get stretched out with additional oxidation time. This suggests that the interface trap density increases with additional oxidation time. This observation is in accordance with Lin's observation of a larger stretch-out and increase of the strong inversion capacitance for the case of oxidation after implantation.

3.3. Avalanche Injection Measurements

3.3.1. Hot Electron Effect Reduction

The results of the avalanche injection current versus gate voltage amplitude measurement are shown on Figure 3.2. Ge implantation has proven a strong means to reduce the hot electron effect in a MOS device. Additional oxidation does not seem to reduce the hot electron effect as we expected; on the contrary, it appears to be
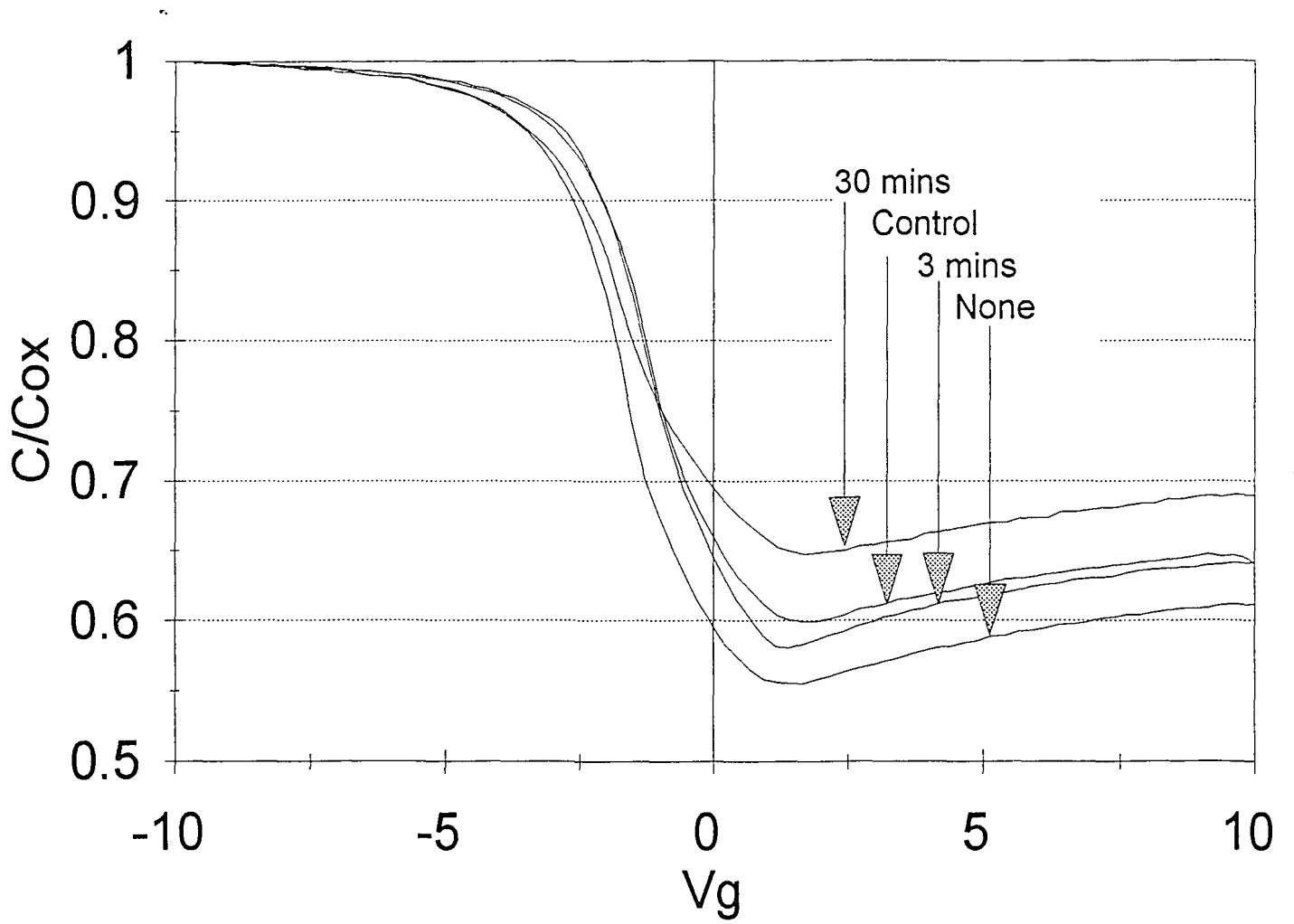
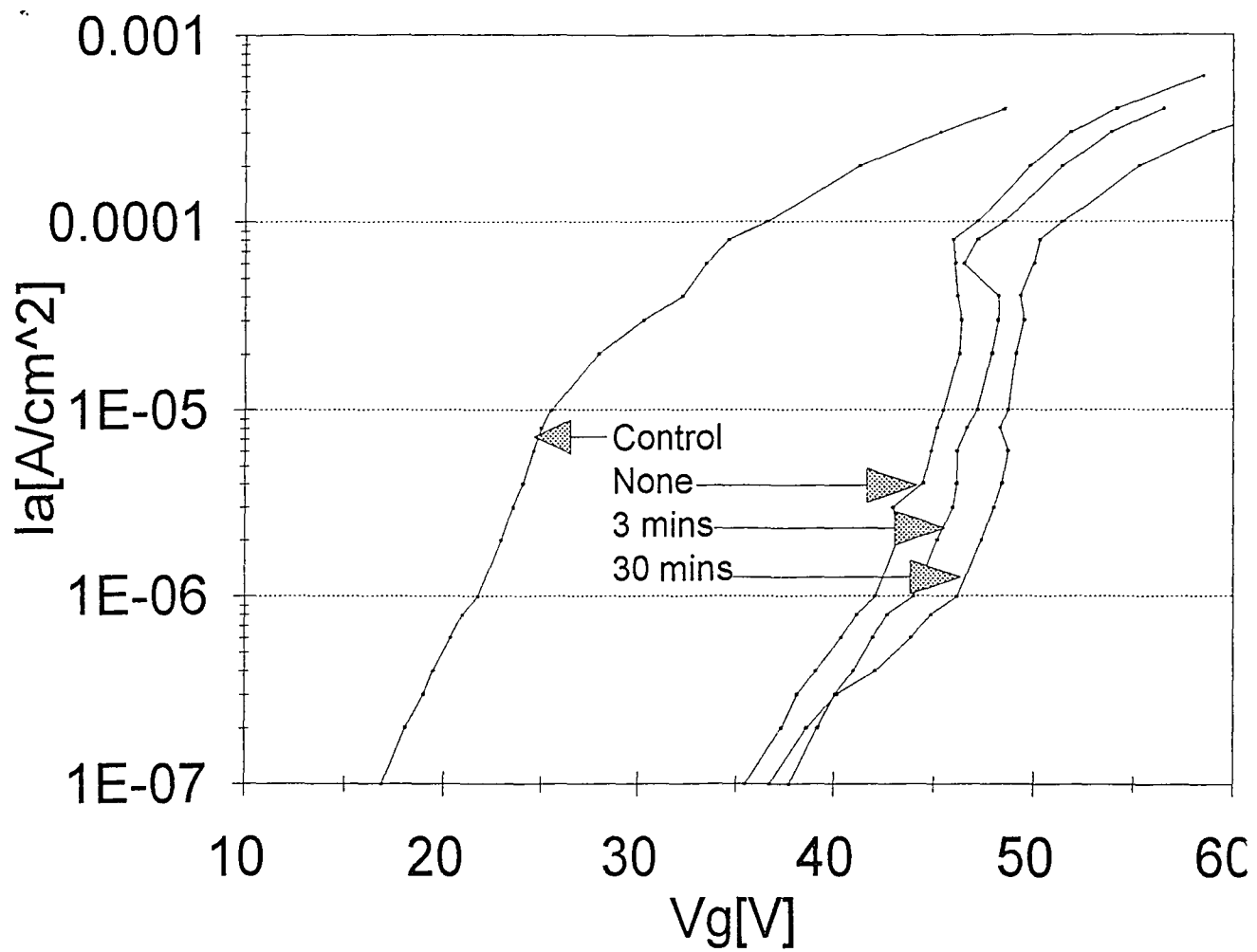**Figure 3.1** The CV curves for the four studied cases.

Figure 3.2 Avalanche current versus gate voltage signal amplitude curves for the four studied cases. These curves indicate the hot electron effect reduction.
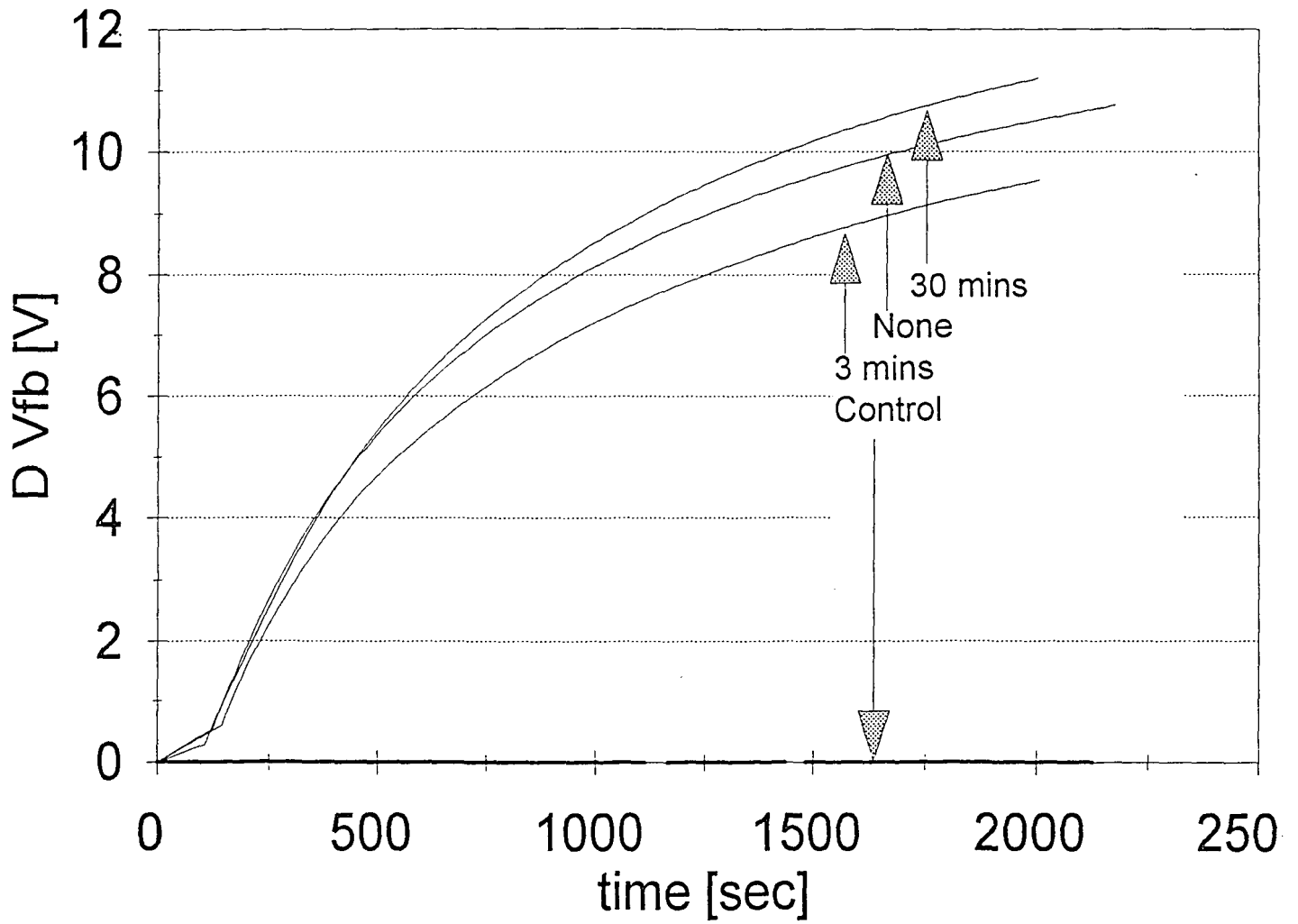
Figure 3.3 Flatband voltage shift versus time curves for an avalanche current density of 10^{-7} A/cm^2 indicate electron trapping rate in the oxide.

slightly enhancing it. This result comes also unexpected compared to Lin's observation of almost no hot electron effect reduction if the sample was oxidized after implantation.

3.3.2. Charge Trapping Study

The results of the charge trapping measurement performed for the avalanche current density of 10^{-7} A/cm^2 are shown in Figure 3.3. The control sample shows basically no tendency towards a flatband voltage shift in the duration of the measurement which was approximately 2000 seconds. Even though Lin's sample oxidized after Ge implantation followed the control sample very closely, when the oxidation was performed in part before and in part after oxidation, no noticeable reduction in oxide charge trap density was observed. The differences between the curves of Ge implanted samples on Figure 3.3 are within the range of accuracy of the method.

3.4. Secondary Ion Mass Spectroscopy (SIMS).

The SIMS plots in Figures 3.4 through 3.8 show germanium profiles for various combinations of pre and post Ge implantation oxidations. Here are brief explanations to each of the figures.

Figure 3.4 is a sample made for SIMS calibration. The sample was oxidized to 540 Angstroms and had ^{70}Ge implanted so that the peak of the implantation occurs in the middle of the oxide layer, that is approximately 270 Angstroms. The sample was annealed in N$_2$ for 30 minutes at 1000 °C. The resulting profile shows the original implantation

peak in the middle of the oxide layer, and some germanium buildup at the Si/SiO$_2$ interface.

Figure 3.5 is basically the same sample as Lin's oxidation after implantation. The germanium was implanted into silicon so that the position of the peak is exactly where the Si/SiO$_2$ interface would be after the sample is oxidized. The plot shows that germanium was strongly rejected from the oxide during oxidation and it piled up on the Si/SiO$_2$ interface.

The figures 3.6, 3.7, and 3.8 represent the pre and post Ge implantation oxidation cases of our study. From these figures it is obvious that germanium has a very strong tendency to migrate from SiO$_2$ to Si, especially in the region of the interface. Even though the initial germanium implanted in the oxide up to about midpoint of the original oxide remains the same for every case regardless of additional oxidation, the region where the oxide grew after implantation is strongly depleted of germanium. This is especially apparent in Figure 3.8. The peak Ge concentrations of the three cases are also slightly higher for the longer additional oxidation times: While in the case of no additional oxidation the peak is approximately at 3.8×10^{20} cm^{-3}, after 3 minutes of additional oxidation it increased to about 4.3×10^{20} cm^{-3}, and after 30 minutes to 5.5×10^{20} cm^{-3}.

3.5. QV Method To Determine The Density Of Interface Traps

Figure 3.9 presents the interface trap densities for the four cases under study. There is an apparent trend of increasing D_{it} with Ge implantation, and with the additional oxidation time.
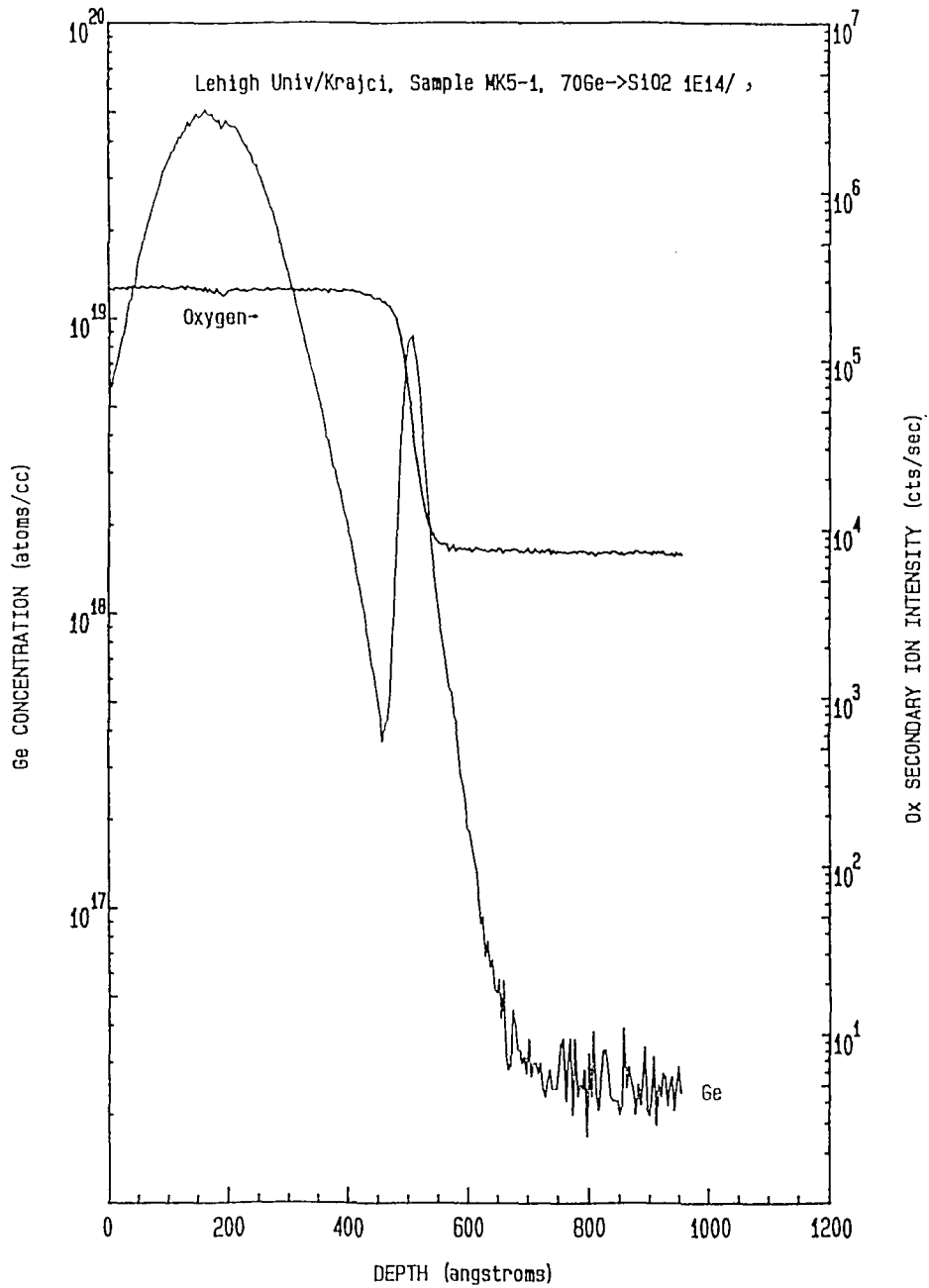
Figure 3.4 Germanium doping SIMS calibration profile. Germanium was implanted so that the peak occurs in the middle of the oxide layer.
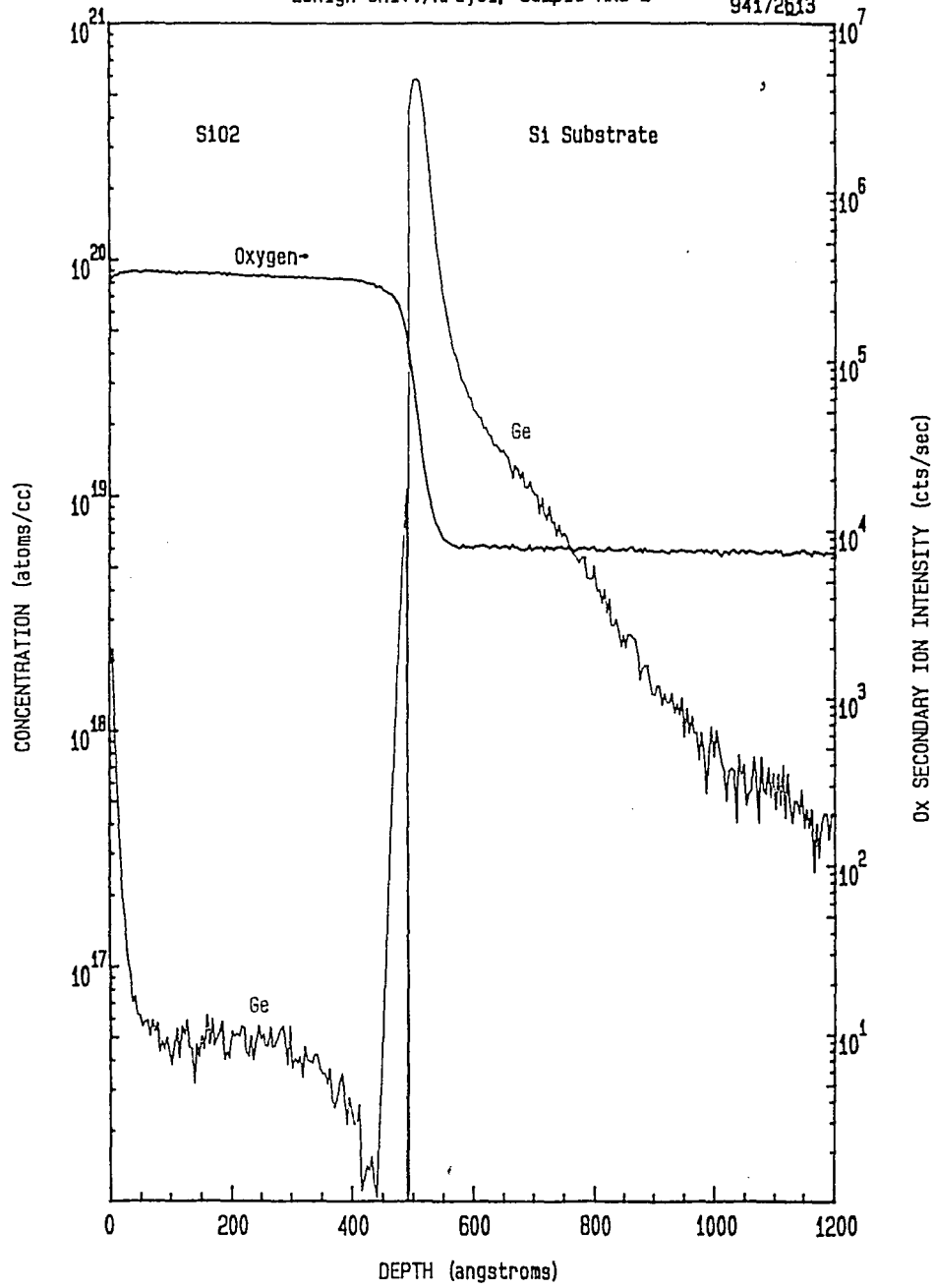
Figure 3.5 SIMS germanium profile for the case when germanium was implanted before oxidation.

Figure 3.6 SIMS germanium profile for the case when germanium was implanted at the Si/SiO₂ interface. No additional oxidation was performed.

Figure 3.6 SIMS germanium profile for the case when germanium was implanted at the Si/SiO₂ interface. 3 minutes additional oxidation was performed.

Figure 3.8 SIMS germanium profile for the case when germanium was implanted at the Si/SiO₂ interface. 30 minutes additional oxidation was performed.
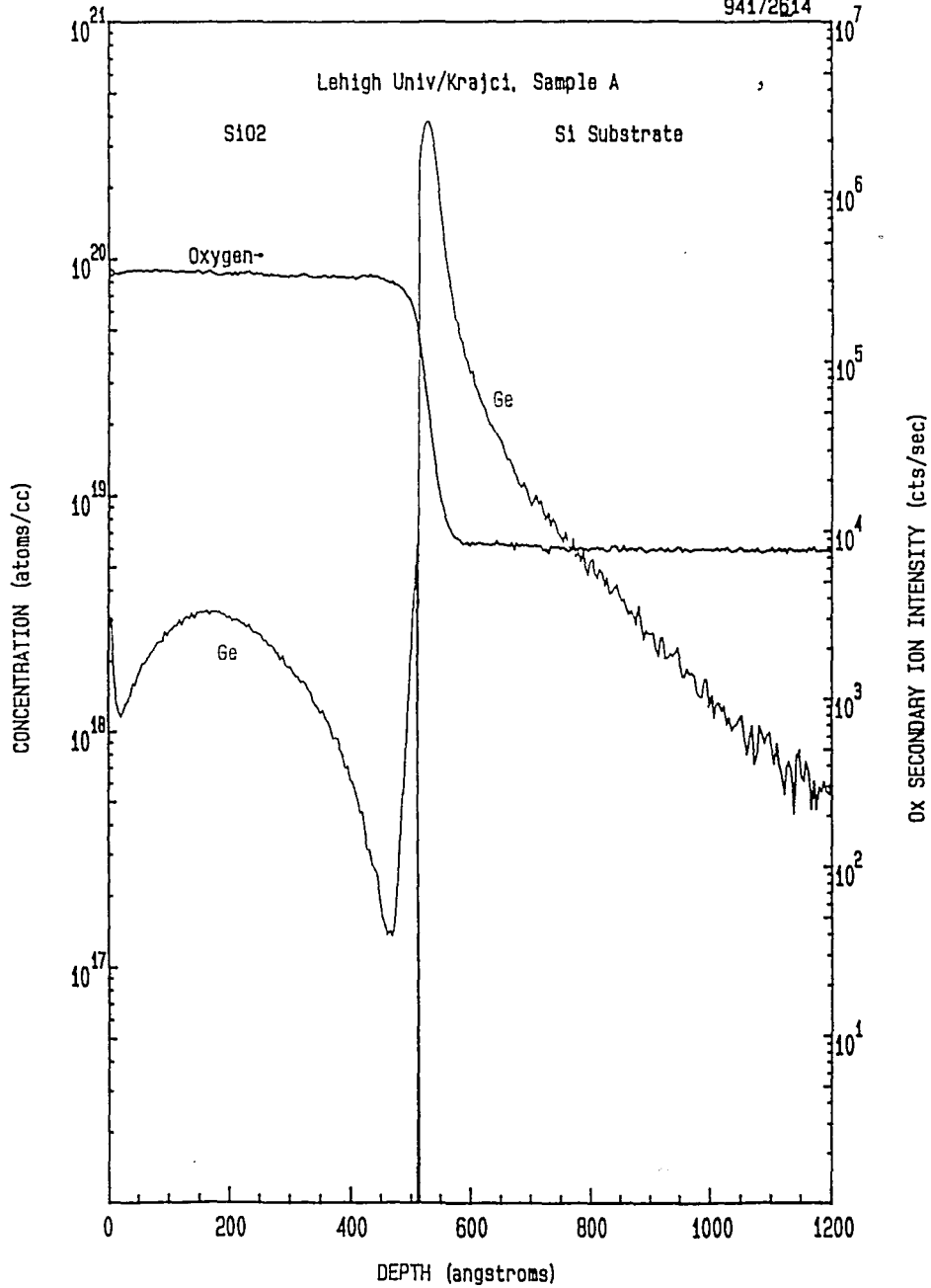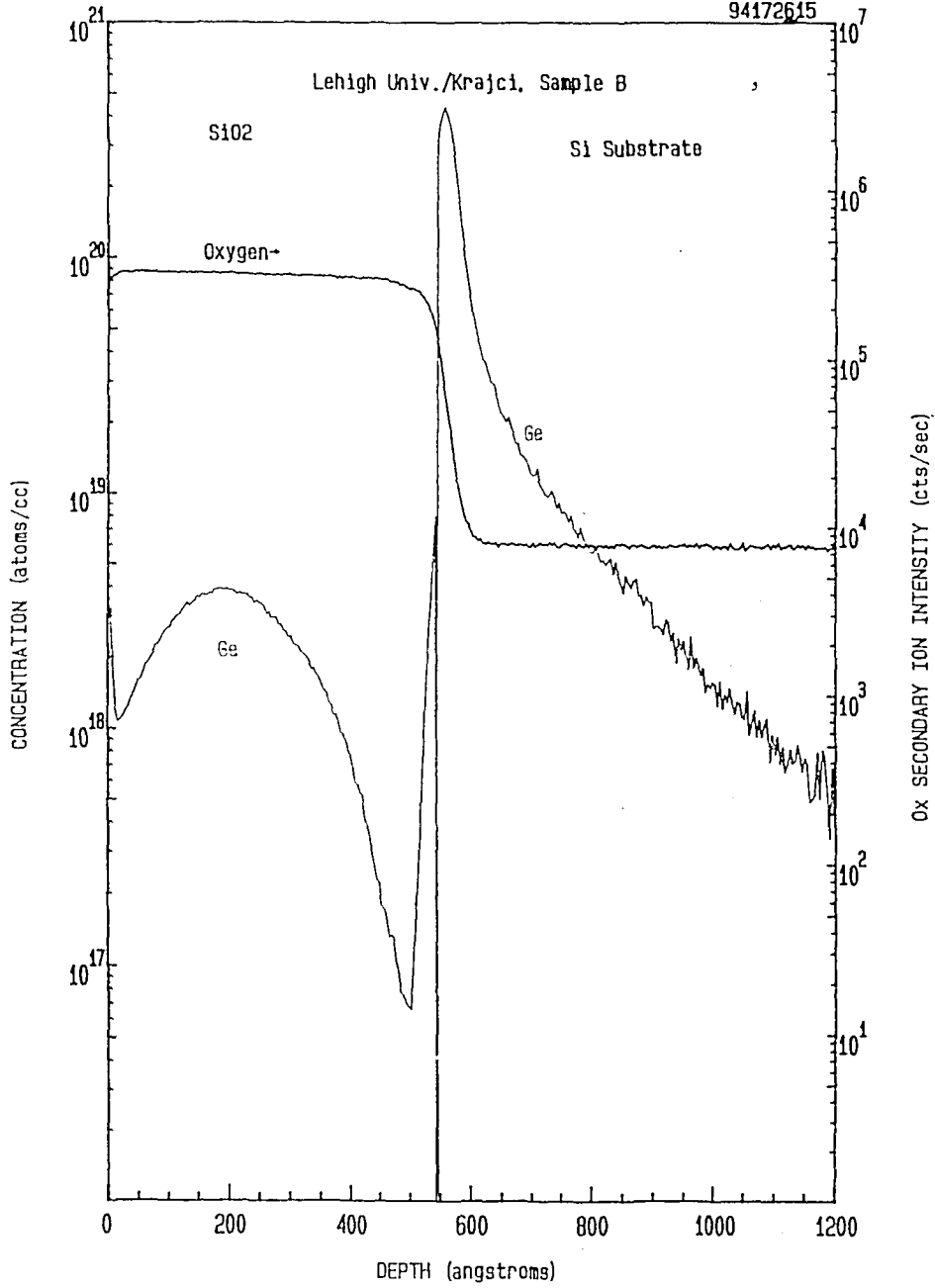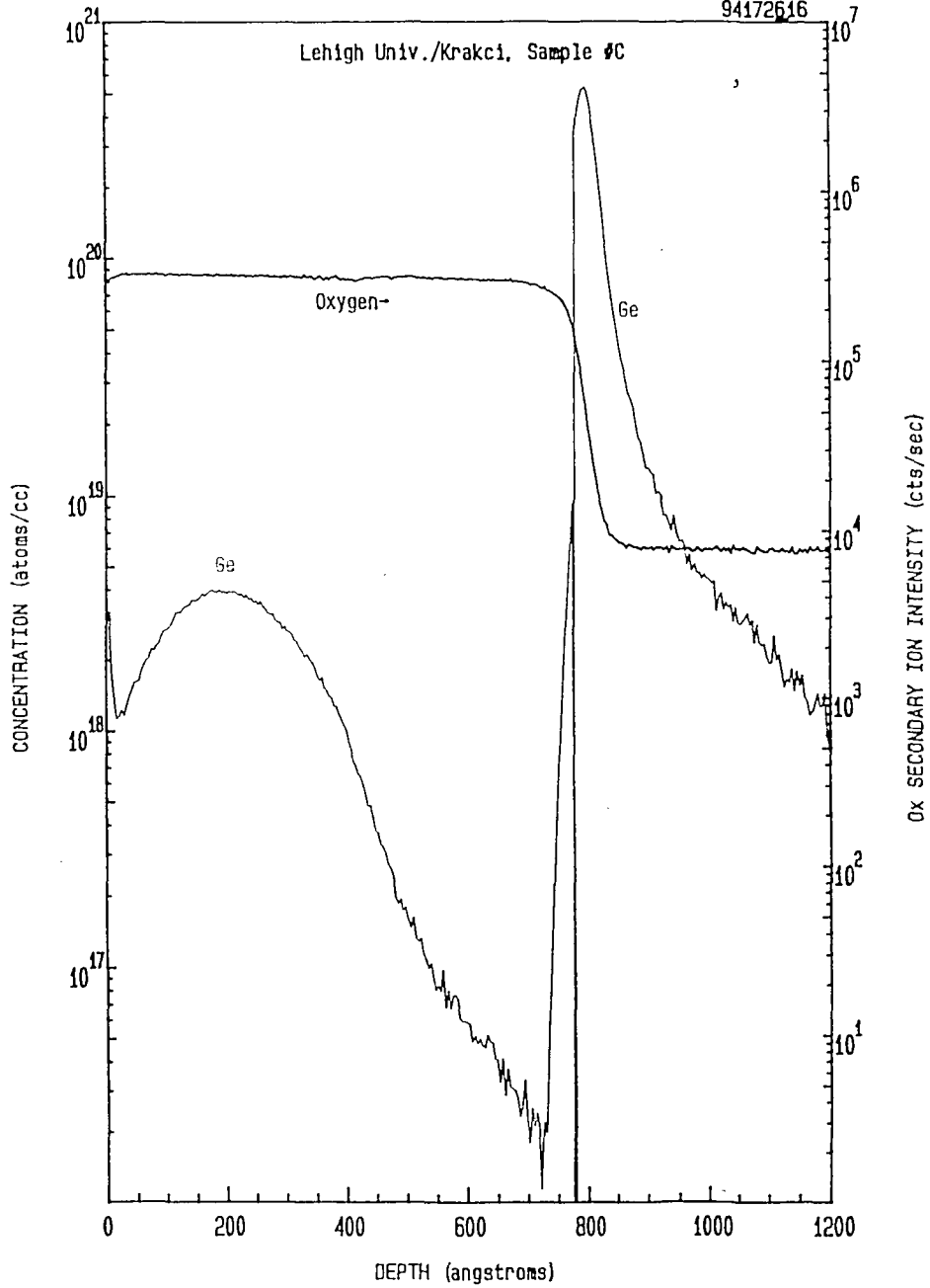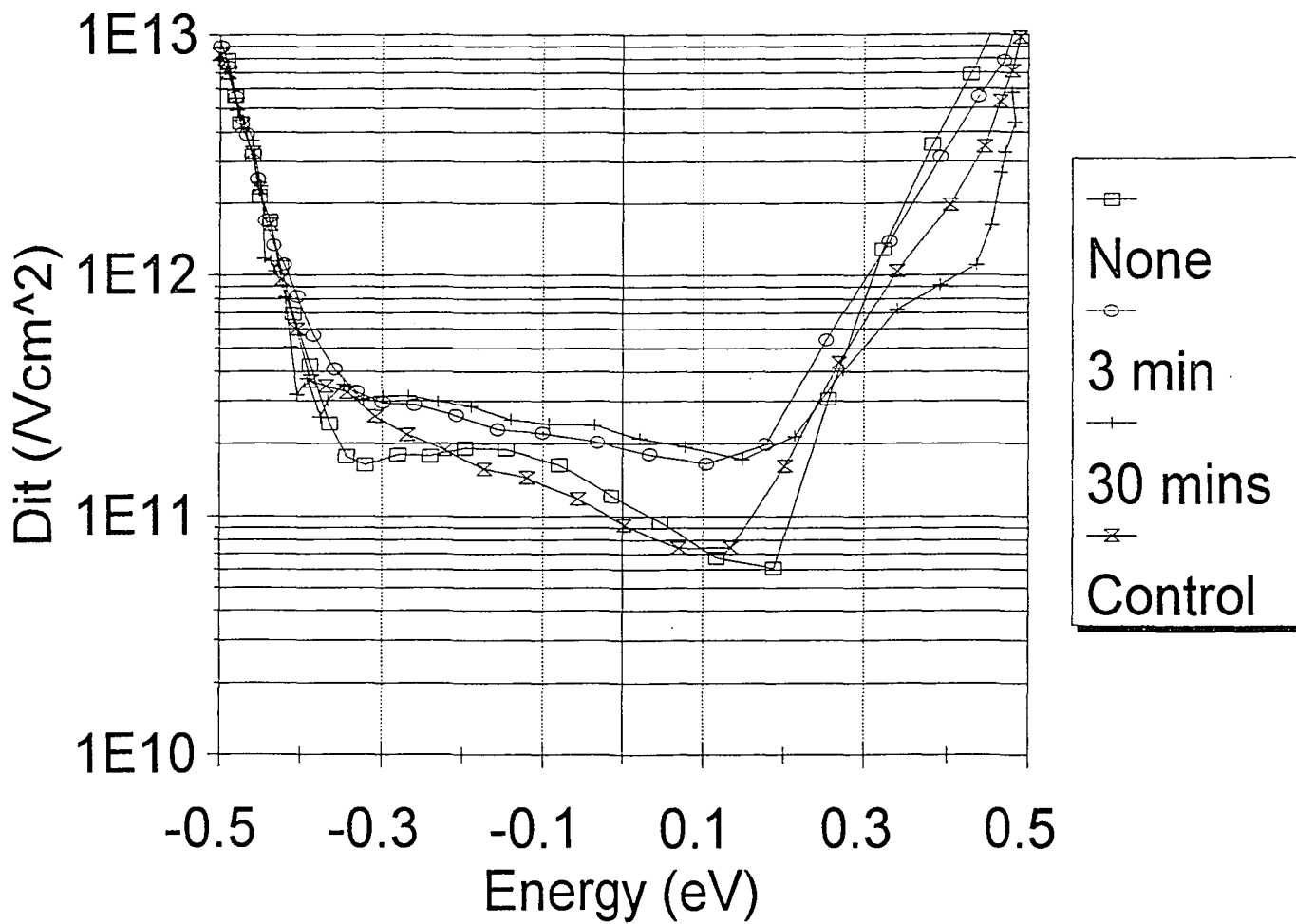
Figure 3.9 Interface trap densities for the four studied cases as determined by the QV method.

Chapter 4: Summary and Conclusions

4.1. Summary

This research study has helped us gain some insight into the process of silicon oxidation when germanium is present, and into further approaches towards utilizing the method of germanium implantation for reduction of the hot electron effect for small MOS devices used in very large scale integration (VLSI).

4.2. Analysis

Based on the presented results, we can form the following hypothesis of what is happening with germanium during the process of oxidation, and how it affects the electrical characteristics of a MOS device.

Even though germanium shows a very strong tendency to be rejected from the SiO_2 and pile up in Si near the interface, some of it remains present in the oxide. A surprising result came up by comparing Lin's case of oxidation after Ge implantation with the case of 30 minutes additional oxidation after the implantation. Even though both cases show very similar profiles of Ge distribution around the Si/SiO_2 interface as determined by SIMS, the reduction of the hot electron effect was very different: while the hot electron effect is significantly reduced when germanium was implanted into some SiO_2, this reduction is minimal when the implantation is into plain silicon. Lin expressed hypothesis that the optimal location of Ge implantation peak for maximum hot electron effect reduction is at the Si/SiO_2 interface. However, he only studied cases when the Ge implantation peak was in the silicon, not in the oxide. Therefore it is also possible that the

hot electron effect could be further reduced if the peak of the Ge implantation were placed in the oxide, and thus more germanium would be present in the oxide bulk. *It seems that it is the presence of germanium in the bulk oxide that is directly related to the reduction of the hot electron effect.* It remains a subject of further studies to examine the mechanism of this relationship actually is. It is possible that germanium in the oxide is incorporated in a partially oxidized state as GeO and the bonds that do not form into the network are involved in this observation.

This study also fully supports Lin's hypotheses that the presence of Ge in the bulk oxide is responsible for the increases in the trapping rate, and that piling up of germanium on the silicon side of the Si/SiO_2 interface increases the interface trap density.

4.3. Suggestions for Future Studies

Since it has become obvious that it is the germanium piled up on the silicon side of the Si/SiO_2 interface which increases the interface trap density, and that any thermal treatment causes migration of Ge atoms near the interface from SiO_2 to Si where it piles up, a process should be designed which minimizes the chances of germanium piling up near the interface in silicon. Should my hypothesis of the hot electron effect reduction being directly related to the presence of germanium in the bulk oxide prove correct, it would leave only two variables in the game: hot electron effect reduction on one side, and increased trapping rate on the other, and it would be only a matter of finding the optimal amount of germanium placed in the oxide to give a solution to the problem of hot electrons without negatively affecting other important parameters.

Bibliography

[1]P.E. Cottrell, R.R. Troutman, T.H. Ning, "Hot-Electron Emission in N-Channel IGFET's," *IEEE Trans. on Electron Devices,* vol. ED-26, pp. 520-533, 1979.

[2]T.C. Lin, "Characterization of Germanium Implanted MOS Devices," PhD Dissertation, Lehigh University, 1994.

[3]K.R. Hoffman, C. Werner, W. Weber, G. Dorda, "Hot-Electron and Hole-Emission Effects in Short n-Channel MOSFET's," *IEEE Trans. on Electron Devices,* vol. ED-32, pp. 691-699, 1985.

[4]Y. Toyoshima, "Mechanisms of Hot Electron Induced Degradation in LDD N-MOSFET," *IEDM Tech. Dig.,* pp. 786-789, 1984.

[5]T.P. Ma, "Dramatic Improvement of Hot-Electron-Induced Interface Degradation in MOS Structures Containing F or Cl in SiO_2," *IEEE Electron Dev. Lett.,* vol. 9, pp. 38-40, 1988.

[6]D.D. Xie, D.R. Young, "Electron Injection Studies on Fluorine-Implanted Oxides," *J. Appl. Phys.,* vol. 70, pp. 2755-2759, 1991.

[7]D. Kouvatsos, F.P. McCluskey, R.J. Jaccodine, F.A. Stevie, "Silicon-fluorine bonding and fluorine profiling in SiO_2 films grown by NF_3-enhanced Oxidation," *Appl. Phys. Lett.,* vol. 61, pp. 780-782, 1992.

[8]T. Hori, H. Iwasaki, "Improved hot-carrier immunity in submicrometer MOSFET's with reoxidized nitrided oxides prepared by rapid thermal processing," *IEEE Electron Dev. Lett.,* vol. 10, pp. 64-67, 1989.

[9]K.K. Ng, C.-S. Pai, W.M. Mansfield, G.A. Clarke, "Suppression of Hot-Carrier Degradation in Si MOSFET's by Germanium Doping," *IEEE Electron Dev. Lett.,* vol. 11, pp. 45-47, 1990.

[10]T.-C. Lin, D.R. Young, "Effects of Germanium Implantation on Metal Oxide Semiconductor Avalanche Injection," *Appl. Phys. Lett.,* vol.62, 1993.

[11]D.K. Schroder, *Semiconductor Material and Device Characterization,* Wiley & Sons, Inc., New York, 1990.

[12]E.H. Nicollian, J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology,* Wiley & Sons, Inc., New York, 1982.

[13]D.R. Young, E.A. Irene, D.J. DiMaria, R.F. De Keersmaecker, "Electron trapping in SiO_2 at 295 and 77°K," *J. Appl. Phys.,* vol. 50, pp. 6366-6372, 1979.

Appendix:Fabrication Sequence for MOS Capacitors

1. **Staring Material:**

   3 inch Si wafer, p-type, Bdoped, <100>, .14-.17 ohm-cm

2. **Oxidation**

   RCA clean

   oxidation: 1000°C, 45 minutes, dry oxide, ~500Å

   anneal: 1000°C, 15 minutes, 1.5 l/min N_2

   3. **Ge Implantation**

      implantation: Ge, 73 keV, 10^{14} cm^{-2}

         additional oxidation 3, 30 minutes, 1000°C, dry oxide

   anneal: 700°C, 15 min, 1.5 l/min N_2

4. **Metallization**

   Al deposition: evaporator

   photo: define gate area, 1mm×1mm

   etch: Al, PAN etch, 45°C, 3 minutes

   strip PR: PRS-2000

   anneal: PMA, 450°C, forming gas (H_2/N_2, 1:5)

Note: Indent indiactes steps performed only on selected wafers.

Vita

Martin Krajci was born on January 12, 1970, in Bardejov, Slovakia (formerly Czechoslovakia) to Mr. Albin Krajci and Mrs. Klara Krajciova.

In 1988 he started attending the University of Transport and Communications in Zilina, Slovakia, majoring in electrical engineering. In 1990 he was selected a scholarship recipient under the Freedom Lamp program, a project of the new democratic Slovak government with several US universities, and was assigned to study at Wilkes University in Wilkes-Barre, PA. He graduated from Wilkes University in 1993 summa cum laude with Bachelor of Science in electrical engineering. In August 1993 he started his graduate study at Lehigh University Department of Electrical Engineering and computer science as a research assistant in the group of Prof. R. Jaccodine. In June 1995 he took a position of electronics engineer in Artann Laboratories, East Brunswick, NJ.

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