

1996

A study of value chain linkages in the Microelectronics Group of Lucent Technologies

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Chou, Yuan-Ling
A Study of Value
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the
Microelectronics
Group of Lucent
Technologies

January 12, 1997

**A Study of Value Chain Linkages in the Microelectronics
Group of Lucent Technologies**

by

Yuan Ling Chou

*A Thesis
Presented to the Graduate and Research Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science*

in

Management of Technology

Lehigh University

December 20, 1996

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science in Management of Technology.

20 December 1996

Date

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ACKNOWLEDGEMENTS

The author would like to thank Dr. Ted Schlie, Dr. Peter Saunders and Dr. David Wu for a lot of guidance, references, feedback, encouragement and encouragement throughout the research process. Dr. Schlie in particular has been an outstanding advisor whose feedback and constant communication has made this thesis so much better.

The author is also indebted to to the staff of Center for Innovative Management Studies, Lehigh University, especially Sharon Kimmel, whose help has been invaluable.

I would like to express my sincere gratitude and appreciation to many at Lucent Technologies for unwavering support and extreme generosity of time, research materials and information, especially Andy Lum, Kevin Chynoweth, Paul Mostek, Mark Cortazzo, Rick Goulstone, Chuck Pearce, Dave Rehrig, Craig Oursler, Anna Lewis, and Russ Burrock. This thesis is a tribute to the people of Lucent Technologies, who have made it one of the most innovative companies in the world. A special note of thanks to my managers Andy Lum and Helen Wilkinson, who have given me the opportunity to participate in a most exciting learning experience - the MOT program at Lehigh.

Most of all, I would like to thank my family, who were there for me every step of the way.

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Abstract

The focus of the study was value chain linkages within the Microelectronics Group of Lucent Technologies, and their contribution towards competitive advantage. Michael Porter's Value Chain Model is a well-known construct for analyzing companies' activities and the linkages between activities. The model was used to analyze manufacturing operations within the IC Division (ICD) of Lucent Microelectronics.

The author found two cases of linkages in ICD. In the first case, changes in one activity had significantly impacted another. This linkage optimization had also substantially improved ICD's competitive position. The second case was a linkage that, if well-managed, could increase ICD's competitive advantage. Based on an analysis of both cases, the author recommended ways for Lucent Microelectronics ICD to improve its linkage management process.

Chapter 1: Introduction

Although the Microelectronics Group of Lucent Technologies has supplied electronic devices to telecommunications industry for nearly 50 years, it entered the merchant semiconductor market and started selling products to external customers only six years ago. Since then, Lucent has come a long way in making the changes and learning the skills needed to be a viable competitor in that market.

This study details the processes that Lucent Microelectronics implemented for doing competitive analysis and process improvement. Specifically, Microelectronics' value chain linkage improvement process is examined and illustrated through two case studies.

Part 1: Context

Chapter 2: Microelectronics Group, Lucent Technologies

History and Organization

Microelectronics (also known as ME) was originally part of the Western Electric division of AT&T. More recently, it became part of AT&T spin-off Lucent Technologies. The business originated from the invention of the transistor in 1947 by Bardeen, Brittain and Shockley of Bell Labs.¹ The first ever transistor assembly line was in fact located at ME's Allentown factory. Pre-1984 and divestiture, ME was part of a regulated monopoly. Like most monopolies, ME operated in an environment where competition, marketing, and market efficiency were not crucial considerations. As ME supplied most if not all the microelectronics needs of AT&T, it manufactured everything from memory devices to power supplies, and probably was not the most effective, efficient and competitive supplier for many of these products.

After the 1984 divestiture of AT&T, ME had to operate in a more competitive environment. Although it now had to compete with other component suppliers for business within AT&T, it was also free to sell

¹ Friedel, Robert "SIC Transit Transistor," American Heritage of Invention and Technology.

products to other companies, including AT&T competitors, as an OEM supplier. The rationale for this policy change was twofold: first, profit and loss responsibility was now pushed down to individual divisions and businesses; second, management recognized that the R&D investments in product development and manufacturing technology required for the company to become competitive were too large for a "captive" semiconductor supplier to realize. In addition, manufacturing facilities sized to meet only internal demand could not generate the economies of scale captured by the larger IC suppliers.

The change in environment was extremely difficult for the organization and people of ME because it meant a sudden 180 degree change in how things were done. The rules and the playing field were now very different. For ME, the transition happened only after a great deal of pain and changes at all levels of management. Reorganizations and even downsizing occurred in various businesses as management tried different strategies to streamline the organization and rejuvenate processes and product lines. ME did not become profitable until 1992, eight years after divestiture. Important tasks for ME management included an evaluation of the company's performance relative to the rest of the industry and a determination of ME's core competencies. This had to be done so management could best select the products, services, markets and businesses to focus on. As Curtis Crawford, ME president, put it:

"We were in a lot of product businesses because of the historical perspective that we had to supply all of the needs of the [AT&T] corporation. But, to go forward, we concluded that there are sourcing alternatives for the corporation that didn't have to come from us² ... Keep in mind that all of the AT&T business we have is earned from AT&T, just as it was earned from other customers. We compete on a purely commercial basis..."³

Crawford's strategy then and now is to stay with product lines in which ME can hold either first or second place in market share and discontinue less profitable products. The success of this strategy was demonstrated by AT&T-Microelectronics reaching sales of \$2.6 billion in 1995 after growing at a average rate of 15% per year in the past five years. In the same period, profits improved 60%.⁴ A major factor in

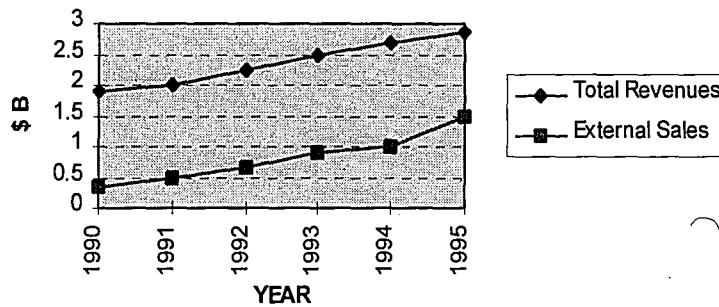
² Gold, Martin "AT&T Micro trims lineup: AT&T Microelectronics discontinues or sells off many products," Electronic Engineering Times (June 5, 1995): 1,27.

³ Berger, Jeffrey, Carol Haber "AT&T Micro to Boost Gear Firm," Electronic News 41 no. 2084 (September 25, 1995): 1, 70.

⁴ Gold: 1, 27.

this faster-than-industry growth is ME's customer diversification. As illustrated in figure 1, external customers accounted for 50% of ME's revenues in 1995 (versus 5% in 1990).

AT&T/LUCENT MICROELECTRONICS ANNUAL REVENUES



Source: AT&T Microelectronics

Figure 1: ME Revenues from External Customers versus Total Revenues

With AT&T's systems and equipment business spun off as Lucent Technologies, ME is well positioned to contribute significantly to this new company, both financially and through product diversification. ME is a component supplier to industries other than telecommunications, and therefore competes in different industries from the rest of Lucent. As such, ME generally has a different revenue stream from other Lucent divisions. This helps even out Lucent's monthly revenues and profits throughout the year.

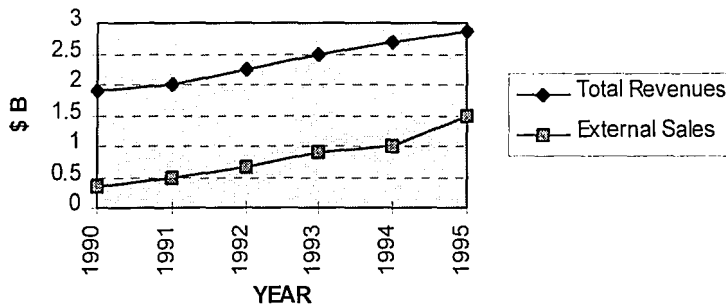
Integrated Circuits Group

There are two business units within Microelectronics: the Integrated Circuits Division (or ICD) and the Systems and Technologies Division. The focus of this study is ICD, which currently accounts for 52% of ME revenues. ICD develops, manufactures and markets integrated circuits for telecommunications switching and transmission, computing, wireless, and video and voice communications.⁵ It was formed in 1994 from the combination of three strategic business units under vice-president John Dickson.

⁵ AT&T Microelectronics Integrated Circuits Group, Application Report for the 1995 AT&T Chairman's Quality Award, (Allentown, P.A.: AT&T Microelectronics, 15 September 1995), xi.

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⁵ AT&T Microelectronics Integrated Circuits Group, Application Report for the 1995 AT&T Chairman's Quality Award, (Allentown, P.A.: AT&T Microelectronics, 15 September 1995), xi.

ICD's strategic focus is to (1) target high growth, high volume applications; (2) create application platforms that enable customers to add value and accelerate the introduction of their products and services; and (3) deliver leading-edge technology and services to satisfy the needs of original equipment manufacturers and other divisions of Lucent Technologies.⁶

There are five product families in ICD:

- Standard-cell Application Specific Integrated Circuits (ASICs) are customized devices designed for customers who require specific functionality and quality in ICs that will go into their end products. Usually, these needs cannot be adequately met by using off-the-shelf ICs such as Gate Array ASICs.
- Digital signal processors (DSPs) are ICs that perform the special-purpose signal processing required for speech synthesis, speech recognition and video compression.
- Telecommunication ICs are used to format, switch and transmit voice and data signals through the telephone system.
- Local area network (LAN) ICs are used to format and transmit digital data over a LAN. LANs are data communication systems used to connect various computers within the limited radius of an office or building.
- Field programmable gate arrays (FPGAs) are versatile, off-the-shelf ICs that customers can program to perform desired logic functions, with the goal of reducing time-to-market for ME customers introducing new products.⁷

As the strategic focus of ICD changed from that of a captive semiconductor supplier to that of a merchant IC vendor capable of partnering with leading customers to bring new technologies to market, competitive

⁶ Ibid, xii.

⁷ Ibid., xii.

analysis has become an integral part of ICD's strategic planning. Unlike before, ICD now had to know how it could compete by differentiating itself from others in the semiconductor industry.

Doing competitive analysis provides ICD with a measure of the following contributors to customer satisfaction: Product delivery, quality, price, design support, ease of doing business with, technology and sales effectiveness. In addition, competitive analysis complements ICD's situation analysis (or SWOT, short for Strengths, Weaknesses, Opportunities, Threats). These analyses, if regularly performed, give ME some insights into how to meet the needs of customers, employees and stakeholders in order to achieve corporate goals in financial returns, customer satisfaction and employee motivation.

ICD manufacturing, research and development and design sites are located worldwide. Key R&D and manufacturing locations include Allentown and Reading PA, Orlando FL, Spain, Singapore, and Thailand.⁸ In addition, ME works with a host of manufacturing partners in Japan, South Korea, Hong Kong, Singapore, Malaysia, and France. One recent organizational innovation was the location of ME design centers near customers in North America, Europe and Asia to provide better support and enhance information transfer.⁹

ICD Strategic Planning Process

ICD's criteria for success can be summed up succinctly: Maximizing CVA (Customer Value Added), EVA (Economic Value Added) and PVA (People Value Added). Financial success (EVA maximization) comes from maximizing customer satisfaction (CVA) and motivating and keeping employees happy (thus maximizing PVA). Although Lucent corporate management established these objectives, specific metrics measuring performance in each objective are set at the division level and cascade through all levels of the organization. Employee and management compensation are tied to the achievement of these goals.

⁸ AT&T Microelectronics Integrated Circuits Group, IC Group Operating Review, (Allentown, P.A.: AT&T Microelectronics, 19 February 1996), 2-5.

⁹ Ibid.

The annual ICD strategic planning process includes a five-year plan done each spring to establish long range objectives (known as the Spring Strategic Outlook or SSO) and a Fall Operating Plan (FPO), which is a detailed business plan for the following fiscal year. The SSO incorporates detailed industry projections, technology forecasting and competitive analysis. Additional inputs for strategic planning come from monthly functional reviews for each business unit, quality reviews, and quarterly ISO 9002 audits.

Chapter 3: Industry Structure

ICD is fortunate to be part of a fast-growing industry. Much of the growth in semiconductors comes from the convergence of computing and communications.

“Independent of each other, computing and communication tools have been improving at the annual rate of some 25 percent for at least the past two decades. This relentless compounding of capabilities has transformed a faint promise of synergy into an immense and real potential.”

Michael Dertouzos, Director of the Laboratory for Computer Science at MIT.¹⁰

Table 1 shows the five year revenue trends in the semiconductor industry, specified by segments and regions.

Table 1: Semiconductor Industry Revenue Growth (in % Sales Growth)

Table 1: Semiconductor Industry Revenue Growth (in % Sales Growth)	1994	1995	1996	1997 (Forecast)	1998 (Forecast)
Worldwide Chip Revenues	31.8	41.7	6.6	10.3	16
MOS Memory	28.0	64.7	0.3	2.7	15
MOS Microprocessors	31.3	40.2	16.1	20	20
MOS Logic (ASIC, gate array)	9.1	27.4	14.8	18	19.2
American Market	35.6	40	7.8	5.8	22.5
Japan Market	23.6	34.9	-0.1	6.6	10.8
European Market	35.2	42.9	-4.8	6.7	17.1
Asia Pacific Market	35.3	54.1	22.1	23	24

Source: Semiconductor Industry Association (October 1996)¹¹

¹⁰ Naisbitt, John, Global Paradox (New York, NY: Avon Books 1994): 98-99.

¹¹ Harris, Patricia, ed., Integrated Circuits International: An Elsevier Bulletin (San Jose, CA: Elsevier and Electronic Product News May 1995): 2.

ASIC Market Segment

There are three types of ASICs: Full-custom ASICs are ICs designed at the transistor level. Standard-cell ASICs and Gate Array ASICs are both semi-custom and designed using "cell libraries" (collections of macrocells and other IC building blocks). Every ASIC supplier has a proprietary cell library. Gate arrays are off-the-shelf ICs that customers can program to perform desired logic functions while Standard-cells are customized for each application.¹² A more inclusive overview of semiconductors can be found in Appendix 1.

Although the growth of the ASIC market slowed down in 1996 because of OEM inventory adjustments in the computer industry, there are many new high-volume applications that will contribute to continued strong growth for this market segment, e.g. LAN switches, networks, high performance work stations and cable.

As table 2 shows, the standard-cell and gate array ASIC market shares are increasing at the expense of full-custom ICs. Standard-cell ASICs are projected to dominate the ASIC segment of the semiconductor industry by the year 2000, with sales reaching \$17 billion.

Table 2: Worldwide ASIC Consumption by Product (\$US M)

	1996	1997	2000
PLD	2,049	2,428	4,887
Gate Array	6,960	7,724	11,258
Standard-Cell	6,837	8,553	17,204
Full-Custom	1,874	1,593	633
Total ASIC Market	17,720	20,298	33,982

Source: Dataquest (October 1996)¹³

A discussion of the ASIC segment of the semiconductor industry follows, using the categories defined by Porter in his model of competitive forces in an industry.¹⁴

Blough, Kelly and Jeff Weir, "World Chip Market to Grow 7.4 percent in 1997; Semiconductor Sales Should Approach \$200 Billion by 1999," Semiconductor Industry Association Press Release (October 30, 1996).

¹²McCall, Tom, Slower Growth for the 1996 ASIC Market (San Jose, CA: Dataquest, October 17, 1996): 1.

¹³ Ibid.

Rivalry Among Existing Firms

The competition among existing firms is keen. Although Lucent currently leads in market share for standard cells ASICs, it faces strong domestic and international competitors. As table 3 shows, the segment is highly concentrated, with the ten largest companies combined holding 60% world market share. Major ICD competitors include Texas Instruments, LSI Logic, Toshiba, NEC, Fujitsu, VLSI and Oki.¹⁵ Interestingly, the bulk of ASICs produced by Toshiba, NEC, Fujitsu and Oki are used by in-house customers. This was the situation facing ME just a few years ago.

Table 3: Revenues and Market Share of Top 10 ASIC Manufacturers.

Rank 1994	Rank 1993	Company	Total ASIC Sales (\$m)	Gate & Linear Array Sales (\$m)	Standard Cell Sales (\$m)	% Total ASIC Market
1	2	NEC	1000	720	280	9.3
2	1	Fujitsu	970	785	185	9.0
3	4	Toshiba	808	560	230	7.5
4	3	LSI Logic	770	615	155	7.2
5	5	Lucent	756	86	625	7.2
6	6	TI	655	110	445	6.1
7	7	VLSI	425	170	255	4.0
8	10	Oki	370	185	185	3.4
9	8	Hitachi	360	330	30	3.4
10	11	Motorola	345	285	55	3.2
		Other	4721	1549	1570	39.8
		Total	10730	5365	4015	100.0

Source: *Integrated Circuit Engineering 1995*¹⁶

Threat of New Entrants

Competition from new entrants is expected to increase in the future. There are currently over 100 suppliers worldwide, with more companies getting into this product-market segment because it is perceived to be "high end" and profitable for companies competing in it. One potent new entrant is IBM, whose semiconductor operation functioned as a captive in-house supplier until a year ago. IBM has leading edge design and manufacturing technologies but a higher cost structure at the moment than most in the industry.

¹⁴ Porter, Michael E., *Competitive Strategy: Techniques for Analyzing Industries and Competitors* (New York, NY: The Free Press, 1980): 3-33.

¹⁵ AT&T Microelectronics Integrated Circuits Group, *IC Group Operating Review*, Allentown, PA: AT&T Microelectronics (19 February 1996).

¹⁶ Harris, Patricia, ed. *Integrated Circuits International: An Elsevier Bulletin* (San Jose, CA: Elsevier and Electronic Product News, May 1995): 16.

IBM's cost structure is expected to improve if it increases its business and captures more market share¹⁷

Other strong new entrants include Asian semiconductor manufacturers such as Samsung and Hyundai.

They are entering the ASIC market by extensive investments in design capabilities, including acquisitions of smaller U.S. companies with strong chip design capabilities. This, coupled with their tremendous manufacturing and process capabilities from many years of DRAM manufacturing (manufacturing of high volume, low cost products), makes them competitive threats to other ASIC manufacturers.

Threat of Substitute Products and Services

Gate array ASICs are the primary substitute products for Standard-cell ASICs. In general, gate arrays are used for applications with less complex designs, or when shorter design and prototyping intervals are required. Although the design and prototyping intervals for Standard-cell ASICs have decreased in recent years, they are still longer than those for gate arrays. For gate array users, this shorter time-to-first-product allows for faster changes to product design and increased flexibility. The advantages that standard cells have over gate arrays are that they are smaller size, have lower power consumption, and can run at higher speeds. Also, customers who require maximum functionality on a small chip can get a one-chip solution with standard cells but not with gate arrays. On a per unit basis, standard cells are lower cost than gate arrays. In short, standard-cells are superior to gate arrays for high complexity, high volume applications. In general, the threat of substitution is low once a design is completed and the chip released into manufacturing because switching costs are high. By the time an ASIC is designed into an end-product, the customer has invested much time and effort into design and development. They would not turn to another supplier unless there were significant cost, delivery or quality issues with the current ASIC supplier. On the other hand, once a short-product-life-cycle product declines, the next new products might use a substitute.

¹⁷ AT&T Microelectronics, Competitive Analysis based on information from Dataquest, In-stat, and customer interviews, 1995.

Bargaining Power of Suppliers

In 1995, wafer fabrication was a bottleneck and became the industry growth limiter for that year. Wafer fab subcontractors had a lot of market power then because all semiconductor companies were competing for limited wafer fab capacity. This year, the addition of many new foundries and in-house wafer fabs and an overall slowdown in semiconductor demand led to a change in the balance of power.¹⁸ The 1996 capacity bottleneck was high-end, state-of-the-art chip package assembly. This capacity limitation did not affect all companies uniformly – it impacted manufacturers of complex microprocessors and ASICs more than it did manufacturers of memory devices. In the future, the bottleneck and bargaining power will undoubtedly shift to another group of suppliers in this complex value system.

Bargaining Power of Buyers

The bargaining power of buyers is high before a chip design is awarded to an ASIC supplier, and relatively low after a chip goes into design and production. Once a customer has worked with a supplier to design and qualify a chip, that customer is typically reluctant to work with another supplier to design and qualify a replacement chip. The leverage that ASIC customers have in negotiating with suppliers is the award of new business. If the customer is not happy with a certain supplier, it initiates a relationship with another supplier that would come to fruition a year or so later (the lead-time from chip design to customer receipt of first production parts). This also implies that customers with high volumes and shorter product life cycles have relatively more market power because they have a larger number of new designs they can award to ASIC companies.

Industry Analysis Conclusion

From ME's perspective, the drivers that will most affect the industry structure in ASICs are:

The threat of new entrants. The proliferation of consultants and commercially available software are contributing to industry standardization in ASIC design. Proprietary and customized design tools

¹⁸“AT&T semiconductor exec cites risks to industry growth,” EDGE, on & about AT&T 11, no. 391 (Jan 15, 1996): 2.

are becoming a thing of the past. In addition, other semiconductor companies are now entering the ASIC arena by partnering with or acquiring companies with strong design capabilities.

Bargaining power of suppliers. In 1995, wafer fab subcontractors had strong bargaining power because they were the capacity bottlenecks; In 1996, chip packaging subcontractors are in that situation, as there are only a few high-volume chip packaging companies in the world. They have become capacity limiters for ASIC and microprocessor semiconductor companies.

Going forward, ME has to understand the competitive pressures in the industry and continually scan the environment for any changes. Regular industry analysis helps ME understand the ASIC market better and become more proactive in dealing with competitive threats and optimizing opportunities. This is an exercise that ME can go through whenever it develops strategic and operational plans.

Lucent Microelectronics' Competitive Strategy

According to Michael Porter, there are three generic strategies a firm can use to achieve and sustain competitive advantage - cost leadership, differentiation and focus.¹⁹

Cost leadership: A firm using a cost and price leadership strategy seeks to become the low-cost producer in its industry. In turn, the customer experiences cost leadership in terms of lower prices. Sources of cost advantage include economies of scale, proprietary technology, and access to raw materials. To become successful, low-price producers typically sell a standard product and place tremendous emphasis on achieving economies of scale and cost advantage from all sources.²⁰ A firm achieving and maintaining overall price leadership will remain successful as long as its products are accepted by customers and not noticeably different in features and quality to the industry norm.²¹ According to Porter, there can be only one price leader in an industry. Unless a firm gaining a price advantage "persuades" others to abandon a

¹⁹ Porter: 26.

²⁰ Michael E. Porter, Competitive Advantage: Creating and Sustaining Superior Performance (New York, N.Y.: The Free Press, 1985), 11-14.

²¹ Robert M. Grant, Contemporary Strategy Analysis: Concepts, Techniques, Applications (Cambridge, MA: Basil Blackwell, Inc., 1991), 138-141.

price leadership strategy, it might become caught in a discounting and undercutting mode with competitors with disastrous consequences for profitability.²²

Another generic competitive strategy identified by Porter is differentiation. In general, a differentiating firm seeks to be unique in its industry on one or more buyer-valued dimensions. By doing so, it can command a premium price for its products or services. Another way to look at differentiation is as a strategy that creates value for the buyer through the firm's impact on the buyer's value chain. Sources of uniqueness stem from the impact of the following factors on the way activities are performed by the firm:²³

Policy choices: The policy choices that firms make about the way they perform activities can be a source of uniqueness. Such policy choices include the product features and performance offered, the intensity of an activity and the procedures governing the actions of personnel in an activity. For example, ME has a policy to respond to a customer request for price quotation within 24 hours of receipt. This policy improves the customer's perception about ME's responsiveness and adds to perceived uniqueness.

Linkages: Linkages can lead to uniqueness if the way an activity is performed affects the performance of another activity. For example, if ME improve its transportation system to ship product anywhere in the world within 48 hours, it provides value for customers because they can now get components more quickly to meet end-user requirements. The transportation activity in ME thus impacts customers' manufacturing, inbound logistics, and sales and marketing activities.

Timing: Uniqueness may stem from the firm's timing in performing an activity. For instance, a firm gains uniqueness by being first to market with a new product that customers require.

Location: An example of uniqueness that can stem from location is ME placing technical support offices near customer R&D facilities to improve communication and technology transfer between customer and ME engineers.

²² Porter: 13-14.

²³ Porter 124-127.

Learning: Proprietary learning is a good source of uniqueness. For example, if ME has a proprietary process to manufacture combined analog and digital ICs that no one else does, the process is a source of uniqueness for ME.

Integration and Interrelationships: Interrelationships and vertical or horizontal integration offers opportunities for uniqueness in activities. An example of a uniqueness stemming from integration is ME partnering with Lucent's Network Systems Group to develop customized chips for Asynchronous Transfer Mode equipment (Asynchronous Transfer Mode is a networking technology standard). ME could get to market faster with its four-chip solution because it developed the chips in parallel with Network Systems' development of their ATM equipment.

Even as it differentiates, a firm cannot ignore costs. The additional revenue from premium pricing can be easily nullified by a poor cost position.²⁴ Also, some sources of uniqueness can be more easily copied by competitors than others. For instance, firms can imitate policy choices more easily than they can linkages and learning. A firm that understands the drivers of its uniqueness can better maintain its currency and viability over time.²⁵ The risks of differentiation are:

- Differentiation may not be sustainable because (1) competitors imitate the uniqueness, or (2) the basis for differentiation becomes less important to customers;
- The cost proximity vis-à-vis competitors is lost;
- Other differentiating companies achieve greater segment differentiation.

By choosing to compete as a differentiator in most of its markets, Lucent Technologies should be cognizant of the value it provides customers and how it interacts with customers, suppliers, and competitors. In addition, value chain management is very important. In particular, Lucent has to create and provide value to the customer, either through lowering his costs or raising his performance.²⁶

²⁴ Porter: 14.

²⁵ Porter: 124-127.

²⁶ Grant: 138-141.

A third generic strategy proposed by Porter is focus. A focuser selects a segment or segment group in an industry to focus on, then tailors its strategy to serving them exclusively. This gives focusers a leg up on broader-based competitors who suboptimize across many segments in their value-chain. A focus strategy could either be on the basis of price (a price focus) or differentiation (a differentiation focus).²⁷

Chapter 4: Competitive Analysis in ICD

"The only thing that gives an organization a competitive edge, i.e.-the only thing that is sustainable, is what it knows, how it uses what it knows, and how fast it can know something new." (Prusak 1996, 16)²⁸

The two main competitive analysis techniques used by ICD are benchmarking and value chain analysis. However, as the concept of core competencies underlies competitive analysis, the discussion will kick-off with a brief description of core competencies.

Core Competencies

A key for firms seeking to maximize benefits from competitive analysis is a knowledge of the organization's core competencies. According to Prahalad and Hamel, a core competence is embedded learning, technologies or activities in a company that (1) provide access to a wide variety of markets, (2) make a significant contribution to the customers' perceived benefits from the end product, and (3) are difficult for others to imitate.²⁹ In other words, a core competency would consist of a set of activities within an organization that are (1) critical to the success of end products and services, and (2) performed more effectively or at lower cost than the competition.³⁰ Too often, managers think only in terms of the second criteria when they analyze a firm's value chain, do competitive analysis and decide on areas to invest in. They could thus miss attractive opportunities and chase poor ones. An area the firm is currently

²⁷ Porter: 15-16.

²⁸ Prusak, Laurence, "The Knowledge Advantage," Planning Review v24 (2) (March/April 1996): 6-8.

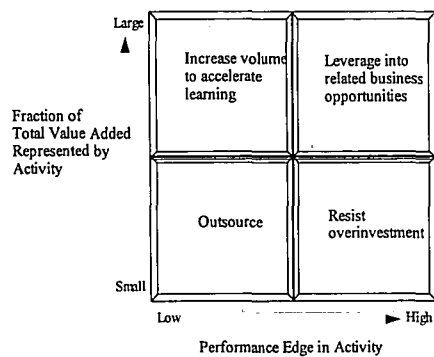
²⁹ Prahalad, C.K. and Gary Hamel, "The Core Competence of the Corporation," Harvard Business Review (May-June 1990): 83-84.

³⁰ Snyder, Amy F. and H. William Ebeling, Jr., "Targeting a Company's Real Core Competencies," The Journal of Business Strategy volume.13 issue 6 (November-December 1992): 26-32.

strong in might not be an area it necessarily wants to invest in. For instance, a firm may have an activity that adds substantial value to end products, but exhibits a performance gap compared to competitors. The firm may very well choose to invest a lot of additional resources to accelerate learning in this strategically important activity to gain long-term competitive advantage, even if it first has to catch up with competitors. In general, a firm's learning and expertise in an activity can be accelerated through increased investment of time and resources into that activity, and acquiring expertise through partnerships with other companies and/or acquisitions. Through partnerships and acquisitions, a firm can expand into new markets, increase its economies of scale or shorten its learning curve.

On the other hand, a firm may choose not to invest or focus additional resources on an activity that represents only a small fraction of the overall value of end products and services even if it was the world leader in this activity. Instead, it might invest just enough to protect its strength in the activity.

The ideal situation is for a firm to have a good competitive position in all activities that add substantial value to end products and services.³¹ This activity management philosophy is summarized in figure 2.



Source: AT&T Microelectronics

Figure 2: Corporate Activity Portfolio³²

Benchmarking

Benchmarking is a process used by companies to measure and improve products, services and work practices by comparing them against other organizations with best-in-class performances so as to gain

³¹ Snyder and Ebeling.: 29.

³² Snyder and Ebeling: 31.

competitive advantage.³³ Although it requires a lot of time and effort, benchmarking yields several benefits, especially for companies in fast-changing industries. First, managers can use the process to motivate employees and generate teamwork by channeling a sense of rivalry and competition from the marketplace deep into the organization. Employees and managers also find it more meaningful to know why they are called upon to be change agents if they can see specific competitive and industry realities instead of vague corporate goals. Benchmarking can also help calibrate people's expectations and views. People experiencing reengineering or major process changes typically go through a denial phase when proposed improvement goals are met with skepticism. Managers can use benchmarking results to demonstrate that the targets can indeed be reached. In general, establishing an external, dynamic base of reference through competitive benchmarking energizes the product and process improvement process by giving it real-world pull instead of the more typical pushing from a few determined managers. Last but not least, benchmarking is a way of coming up with better measurements for evaluating process and capability improvement.³⁴ As "what gets measured gets done", the use of benchmarking is important to companies going through reengineering efforts.

To use benchmarking as a source of ideas, companies should (1) understand the objectives they are striving to meet, (2) look for the best practice within and outside their own industry, and (3) not expect to be able to import processes or practices wholesale from other organizations.³⁵ In general, companies should focus benchmarking and reengineering efforts on areas of the company or value chain where maximum leverage can be achieved.

Benchmarking is comprised of three critical elements: planning, analysis and action. In the planning phase, the specific companies and areas of focus are defined. Analysis, the heart of the benchmarking cycle, involves evaluation of data collected from the companies selected. A company going through the

³³ Grinyer, Madeleine, Hilary Goldsmith, "The role of benchmarking in Re-engineering," Management Services v39n10 (Oct 1995): 18-19.

³⁴ Clark, Kim and Steven C. Wheelwright, Managing New Product and Process Development: Text and Cases (New York, NY: The Free Press 1993): 818-819.

³⁵ Grinyer, Madeleine, Hilary Goldsmith, "The role of benchmarking in Re-engineering," Management Services v39n10 (Oct 1995): 18-19.

action phase internalizes the learning from analysis and takes steps needed to improve performance and the organization.³⁶ This is typically when the payoff from benchmarking commences.

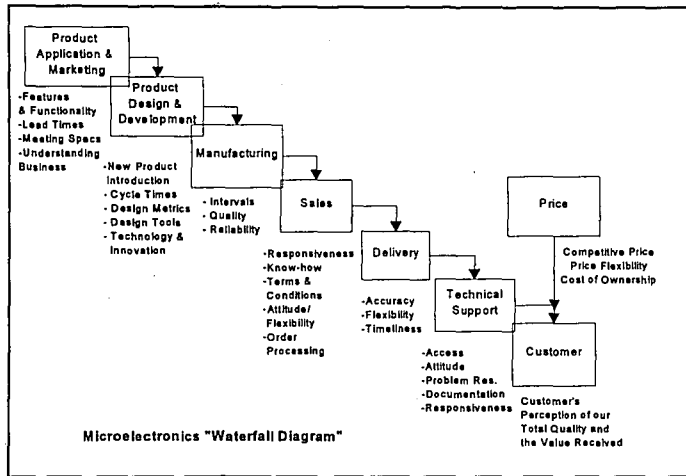
Components of Benchmarking within ICD

Customer Surveys and Continual Customer Contact

A major component of the ICD benchmarking process is the AT&T ME CVA Survey, a quarterly survey of ME customers to assess their perceptions of value received on product, service, quality and price. In addition to customer response on key attributes, the CVA survey includes information on customer satisfaction, repurchase intentions, recommendations and the expected level of business the customer plans to award ME in the coming year. ME started with annual surveys of domestic customers in 1990, expanding the scope and frequency of surveys over successive years. International and domestic OEM and internal customers are now surveyed quarterly.

In 1993, the ICD customer service organization analyzed the 1993 CVA survey data extensively to understand the key repurchase criteria of customers. Through factorial and multivariate regression analysis, the relative importance of key attributes governing customer purchase decisions was derived. These key attributes and weightings were verified by customer-originated "vendor report cards" rating ME against other suppliers. Two graphs of attribute relationships resulted from the analysis. The first is a "waterfall" outlining different processes that cascade to affect customer purchasing decisions (figure 3).

³⁶ The Verity Consulting Group, Inc. *A Hands-on Guide to Competitive Benchmarking: The Path to Continuous Improvement and Productivity Improvement*, Verity Press (Los Angeles, CA: 1991): 4.



Source: Lucent Microelectronics

Figure 3: Processes Contributing to IC Customers' Perception of Total Quality

The second graph of attribute relationship now used by ICD is an IC value tree showing the relative weights of attributes that contribute to customers' perception of value (figure 4).³⁷

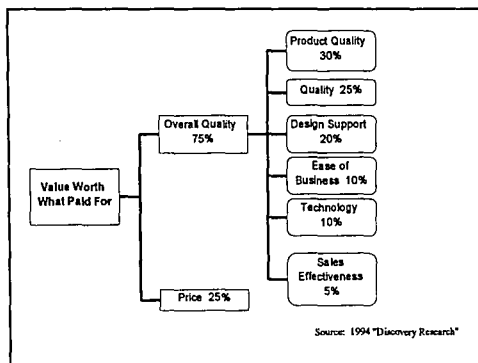


Figure 4: 1995 ICD Value Tree Showing How Key Attributes Influence Customers' Perception of Value

Other data inputs into ICD's benchmarking process include annual assessments by OEM customers and other Lucent divisions on ICD's performance relative to the best-in-class vendors. One illuminating two-part question that ICD likes to include in customer surveys is (a) Would that customer rank ME as a top ten supplier in the IC industry, and (b) Where ME would have placed in the top ten.

³⁷ Ibid., 7-9 to 7-14.

Although the various surveys yield valuable information about how customer perceive their experiences with ME, what has been just as if not more invaluable is frequent customer contact by ME people from various functions. By getting to know customers, managers in marketing, customer service, R&D, quality and manufacturing can calibrate how they are doing vis-à-vis competitors and customer expectations. Frequent customer contact has resulted in several process and product improvement initiatives within ICD.

Other Surveys

ICD has also commissioned independent survey firms to interview customers of major competitors using the CVA survey form. The goal of these interviews is to assess how these potential and current customers rate suppliers in terms of customer satisfaction levels, repurchase intentions and areas that they would like suppliers to improve in. Analysis of responses from competitors' customers and our customers yields valuable inputs on the relative value of ME products and services in the market.

Industry Experts, Consultants, New Hires

ICD subscribes to semiconductor industry market research services such as Dataquest, ICE and In-Stat. These services are a continual source of information regarding market trends, company financial data, and forecasts for products and application markets. In addition, consultants have been retained to research information on specific company performance or strategies. Yet another source of competitive and benchmarking information is ME attendance at semiconductor, computing and telecommunication trade shows and industry events. These are excellent forums for networking and learning. Last but not least, a source of information not usually mentioned in benchmarking literature is the small number of new market hires in ME who have worked in other companies. They bring a fresh and different perspective and a sense of what is important to other companies. Richard Schoenberger refers to such personnel as "knowledge carriers" and even suggests that firms implement policies to ensure that a certain percentage of job vacancies be filled by outsiders. These outsiders can help a firm keep up with outside trends and new ideas.³⁸

³⁸ Schonberger, Richard J., Building a Chain of Customers: Linking Business Functions to Create the World-Class Company (New York, NY: The Free Press 1990): 24.

Consortia and Joint Ventures

In general, ME has learned a great deal from other firms through participation in SEMATECH and bilateral alliances. Members of SEMATECH exchange information on ways to measure customer satisfaction, benchmark, develop future metrics, and establish industry standards for quality and reliability.³⁹ In addition, participation in SEMATECH, SEMI (the SEMATECH affiliated consortium of semiconductor manufacturing equipment, processing materials and software suppliers), SIA (Semiconductor Industry Association) and other consortia provide ME with entree into the world of semiconductor equipment and silicon suppliers.

In addition to consortia membership, ME also partners with other companies to improve almost every aspect of its value chain, from establishing distribution channels in newly opened markets to developing state-of-the-art wafer fab technology. Participation in consortia and alliances are valuable avenues for learning and benchmarking.

"By their very nature, all alliances mechanisms create direct and indirect windows of opportunity for gaining access to a partner's skills, technologies, core competencies, and even strategic direction." Lei and Slocum (California Management Review 1992, 84)⁴⁰

On the downside, I believe that although benchmarking through Sematech and other joint ventures has helped ME shape objectives and metrics to reflect world-class performance expectations, ME has not maximized its learning from partnerships and alliances, or diffused that learning effectively through the organization.

Value Chain

A value chain study is the other leg of ICD's competitive analysis. A firm's value chain consists of discrete activities performed in the design, production, marketing and distribution of products. Porter advocates the use of a firm's value chain as a basic tool for diagnosing competitive advantage and finding

³⁹ Gover, James E., "Analysis of U.S. Semiconductor Collaboration," IEEE Transactions on Engineering Management, Professional Technical Group on Engineering Management v.40, I.2 (May 1993): 109-111.

⁴⁰ Lei, David, John W. Slocum, Jr., "Global Strategy, Competence-Building and Strategic Alliances," California Management Review v.35, I.1 (Fall 1992): 84.

ways to enhance it.⁴¹ Comparing a firm's value chain with competitors' reveals differences that may determine competitive advantage.⁴² Value chain analysis can aid ICD in benchmarking its performance, activities, linkages and costs against the best-in-class, and identifying synergies that provide value to customers.

Part 2: Literature Search

"Gaining and sustaining competitive advantage depends on understanding not only a firm's value chain but how the firm fits in the overall value system." Porter (Competitive Advantage 1985, 34)

Chapter 5: Porter's Value Chain Model

A firm's value chain consists of strategic activities and linkages that contribute to value provided to customers, allowing the firm to achieve price advantage or differentiation. A value chain is the sequence of activities performed by the firm through which value is added to a product or service as it makes its way from inbound materials to final distribution and after-sales service.⁴³ According to the literature, a firm's value chain and the way individual activities are performed reflect the firm's history, strategies, implementation of strategies and the underlying economics of its activities.⁴⁴ Value can be defined by the amount buyers are willing to pay for what a firm provides, i.e. the price paid for the firm's goods and services. Value chain activities are technologically and strategically distinct. Each value activity employs purchased inputs, human and capital resources, and some form of technology for performing it.⁴⁵ Margin is the difference between price paid by the customer and collective costs of performing these activities.

⁴¹ Porter: 26.

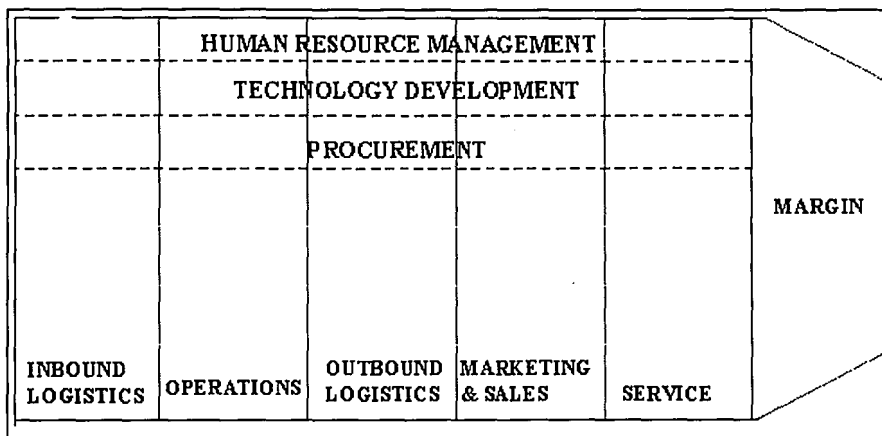
⁴² Porter: 39.

⁴³ Botkin, James W., Jana B. Matthews, Winning Combinations: The Coming Wave of Entrepreneurial Partnerships Between Large and Small Companies John Wiley & Sons, Inc. (New York, NY 1992): 26.

⁴⁴ Porter, Michael E. Competitive Advantage: Creating and Sustaining Superior Performance (New York, N.Y.: The Free Press, 1985), 36.

⁴⁵ Ibid., 38.

A generic value chain (shown in figure 5) consists of five primary activity and four support activity categories.



Source: Porter

Figure 5: Generic Value Chain⁴⁶

Primary activities contribute directly to the physical creation of a product or service, its sale and transfer to the buyer, and after-sales support. These include inbound logistics, operations, outbound logistics, marketing and sales, and service.⁴⁷ Support activities support and facilitate a firm's primary activities. They include infrastructure activities (e.g. planning, finance, MIS and legal services), technology research and development, human resource management, and procurement.⁴⁸

Another way that Porter characterizes primary and support activities is in terms of direct, indirect and quality assurance activities. Direct activities are those involved directly in creating value for the customer, such as production, product design and sales force operation. Indirect activities make it possible for the firm to perform direct activities on an ongoing basis. They are becoming increasingly important because they represent a large and fast-growing proportion of cost. In addition, they also play a significant role in differentiation through their impact on direct activities. Indirect activities are extremely diverse, including

⁴⁶ Bowman, Cliff *The Essence of Strategic Management* (New York, N.Y.: Prentice Hall, 1990), 63.

⁴⁷ Barney, Jay B. *Gaining and Sustaining Competitive Advantage*, Addison-Wesley Publishing Company, Reading Massachusetts, 1997): 176-178

⁴⁸ Grant, Robert M. *Contemporary Strategy Analysis: Concepts, Techniques, Applications* (Cambridge, MA: Basil Blackwell, Inc., 1991): 106-109

maintenance, production scheduling, sales force management and payroll administration. The third category is quality assurance (QA) activities, which ensure the quality of other activities. They include inspection, testing and reworking.⁴⁹

A full assessment of a firm's value chain should also include suppliers' and distributors' value chains, which comprise a value system. This is because they affect and are affected by the firm's performance.

Within the value system, activities can be connected by linkages. A linkage is the relationship between the performance of one value activity and the cost or performance of another. Linkages often exhibit opportunities in managing tradeoffs or coordination among activities to achieve an improved overall objective. A firm can derive as much if not more competitive advantage from managing linkages as it does from managing the activities themselves. Specifically, firms have the opportunity to create competitive advantage through value chain analysis by:

1. Changing the emphasis on specific activities through reallocating resources and management efforts.
2. Performing specific activities better or differently than competitors do.
3. Managing linkages among key activities better than competitors do.⁵⁰

Linkage tradeoffs can be optimized to add unprecedented value to a value chain. Some ways to influence linkages among activities include:

- Performing the same activity in multiple ways, e.g. the use of alternative technologies.
- Improving the cost or performance of direct activities through greater efforts on indirect activities.

An example of this is a company reducing the amount of paperwork that sales has to maintain so that sales people can spend more time developing strategic partnerships with customers.

⁴⁹ Porter: 43-44.

⁵⁰ Schlie, Theodore W., "The Contribution of Technology to Competitive Advantage," Ch. 7 Handbook of Technology Management, Gerald H. Gaynor, Editor in Chief, McGraw Hill, New York, p.7.12, 1996.

- Performing activities within the firm that can reduce the need to demonstrate, explain or service a product in the field, i.e. investments and efforts upstream reducing costs and improving customer value downstream.
- Performing quality assurance activities in different ways. For example, more effort on incoming inspection or better yet, supplier TQC, could lessen the need for finished goods inspection.⁵¹

In order to manage linkages among activities and optimize the value chain, a firm needs to put two things into place: First, information to identify, establish, and improve linkages among value activities. Effective information systems are key to gaining competitive advantage from linkages, creating new linkages and reducing the costs of managing current ones. In practice, many value-chain linkages have been derailed by a lack of an information exchange capability that support the required level of coordination and optimization between activities.⁵²

A second requirement for exploiting linkages is the firm's ability to manage across organizational lines for system level optimization versus subsystem optimization. As part of the value system, managing linkages can include upstream suppliers or downstream distributors and customers. As organizational resistance is often encountered by managers and change agents implementing linkage optimization across organizational boundaries, top management should carefully select the change agents who will lead the optimization efforts. In addition, management can support these efforts by offering incentives and setting up new performance measures to encourage new behaviors and beliefs.⁵³ Given that linkage optimization frequently leads to fundamental evaluations of how a firm manages business processes and subsequent reengineering, the ability to create and optimize linkages between key activities is likely to yield sustainable competitive advantages, i.e. ones difficult for competitors to duplicate.⁵⁴

⁵¹ Porter: 48-50.

⁵² Clark, Mac "Creating Customer Value: Information-Chain-Based Management," Information Strategy (Fall 1993): 13-14.

⁵³ Clark: 13-17.

⁵⁴ Porter: 50

Since linkages are generally harder for competitors to duplicate, they can become sustainable sources of competitive advantage. Lucent needs to optimize linkages as much as possible to compete successfully as a differentiator. This is one reason why the author chose to focus on value chain linkages and their contribution to ME's competitive advantage for this study.

Chapter 6: Constructing a Value Chain

The value chain mapping process is typically carried out in stages and coordinated with the needs of the business. The ICD effort will be used as an example in this discussion:

Large portions of the ICD value chain were mapped out and analyzed as a precursor to the implementation of two enterprise-wide MIS initiatives - Total Order Management (TOM) and Oracle Application Suite (OAS).

Total Order Management is a manufacturing software application that encompasses demand planning, resource planning and prioritization, manufacturing planning and availability/executive functions.

The goal of the OAS program is to successfully implement an integrated business solution that includes all Oracle Suite modules and business functionalities (including finance, human resource management, transportation, and marketing and sales), Electronic Commerce, TOM, and Manufacturing Execution System (MES) by 1998.

The impetus for both TOM and OAS implementation is increasing customers requirements and highly competitive markets demanding instant access to accurate information anytime and anywhere. In addition, the millennium dating problem would have made our existing order and inventory management systems wholly inaccurate by the year 2000 unless they were reprogrammed.

The value chain activities that ICD management chose to focus on were: (1) those possessing different economies, (2) those having a large potential impact on differentiation, and (3) those representing a

significant or growing proportion of cost.⁵⁵ These activities were then assigned to a value-chain category that best represented their contribution to the firm's competitive advantage, e.g. inbound logistics, technology development, etc. This helped ICD select the people and departments to further define and improve each value activity.

ICD mapped out process maps of the value chain, but did not consciously look for linkages. Ideally, the firm identifies how each value activity impacts others. Linkages usually come to the fore as value activities and process flows are analyzed through value chain mapping. According to Martin in The Great Transition, process flows that show the following characteristics are usually worth a second look as candidates for linkage management:⁵⁶

- The value stream crosses many functions and involves multiple narrowly defined jobs
- There are multiple hand-offs from one department to another
- There is high interval to processing time ratio
- The process has no clear owner
- The primary employee motivators are unrelated to value-chain customer
- There is an abundance of corporate politics
- The downstream inspector finds so many flaws in the products that they have to be sent back for rework
- Any exception to the rule causes excessive delays
- The process managers seek to increase the number of people working for them
- There is a major gap between what the customer considers ideal and what actually happens

⁵⁵ Porter: 45.

⁵⁶ Martin, James The Great Transition: Using the Seven Disciplines of Enterprise Engineering to Align People, Technology, and Strategy (New York, NY: American Management Association, 1995): 133.

Chapter 7: The Differentiation Strategy and the Value Chain

A firm's uniqueness for customers can be enhanced by (1)proliferating the sources of differentiation in the value chain, (2)making actual product use consistent with the end customer's intended use, (3)employing signals of value to reinforce differentiation on use criteria, and (4)employing information bundled with the product to facilitate both use and signaling. In addition, the cost of differentiation can be minimized by:

(1)exploiting all sources of differentiation that are not costly, (2)minimizing the cost of differentiation by controlling cost drivers, especially the cost of signaling, (3)emphasizing forms of differentiation where the firm has a sustainable cost advantage, and (4)reducing cost in activities that do not affect buyer value.

Porter recommends that companies change or break rules to create uniqueness. This can be done by:

(1)shifting the decision maker at a purchasing firm to make a firm's uniqueness more valuable, (2)discovering previously unrecognized purchasing criteria, and (3)preemptively responding to changing buyer or channel circumstances.⁵⁷ Although ICD did not consciously look for or manage linkages in its value chain, in the course of normal problem solving, it ended up optimizing some linkages that (1)yielded dramatic results after relatively modest changes were made, (2)were strategically important, (3)contributed greatly to core competence and were therefore key to achieving major competitive advantage, (4)were of great importance to major customers, and (5)were relatively easy to facilitate and implement.⁵⁸

Part 3: Research Question

Chapter 8: Research Question

Based on the literature search, the author chose to address the following research question in this study:

“Can we usefully validate Porter's concept of value chain linkages in Lucent Microelectronics' processes?”

In striving to answer this question, the study will focus on identifying actual cases of linkages and establishing the interdependencies between linked activities in terms of time, cost and performance.

⁵⁷ Porter: 153-158.

Chapter 9: Methodology

The methodology for investigating linkages within the Lucent Microelectronics value-chain included:

- Developing and obtaining detailed process “activity” maps of ICD’s manufacturing processes.

Interviews were conducted with the following people to obtain process map and activity cycle time and cost information:

An industrial engineer in the ICD manufacturing methodologies group who works with all ICD manufacturing facilities to capture cycle time information and reduce manufacturing intervals.

A process engineer in the Allentown bipolar wafer fab.

- Identifying cases where linkages between manufacturing and non-manufacturing activities existed, and where changes were made in one activity which enhanced the cost or performance of the other. These cases were identified through (1)interviews with process improvement engineers and managers in silicon materials and wafer fabrication, and (2)interviews with the ME manufacturing methodology group. The Paragon wafer linkage was identified for study because first, a linkage optimization occurred and was more successful than originally envisioned, and second, for what it could reveal about managing other linkages in the ME value system. The Flash linkage was identified because it promises large cost savings and better capacity utilization if it is managed effectively. In addition, a lot of the information was available because there was a project dealing with Flash activities.
- Interviews with various Lucent people and analysis of ICD documents to detail the nature and extent of the linkages. Interviews were conducted with the following people between April and November 1996:

For Paragon Wafer Linkage -

The lead Silicon Materials engineer on the Paragon project.

A Silicon Materials' cycle time and process improvement expert.

A senior engineer in the Allentown Wafer Fab Yield Improvement organization.

A Wafer Fab manufacturing manager in Allentown.

For Flash linkage -

An industrial engineer in the worldwide manufacturing methodologies group of Lucent Microelectronics who heads the FLASH project.

A technical manager in Bell Labs.

Chapter 10: Results and Interpretations

In the course of the study, two linkages were discovered in which significant changes had occurred and as a result made a significant impact on ICD's value chain. The effect of exploiting these linkages resulted in reduced overall costs within ICD's value chain and improved customer service. These linkages enabled ICD to offer customers highly differentiated products at lower cost, i.e. at a price that customers are willing to pay ICD for the differentiated products and services offered. It is a fact of life that though our customers have been willing to pay a premium for Lucent Microelectronics chips, they are constrained in the amount they can spend for electronics in their products. This is especially true for our ten largest customers, which are worldwide computing and/or communication companies. New products offered by these companies increase exponentially in functionality but not in price compared to the products they replaced. The contribution of these linkages to ME's ability to keep costs in check without compromising product quality and performance have made them invaluable. As this value chain study centered around the silicon manufacturing and wafer fabrication processes in Allentown, Pennsylvania, both linkages are found in that part of ICD's value chain.

Lucent Microelectronics is one of the most vertically integrated IC companies, which equips ICD with some unique advantages and capabilities resulting from an extended value system. These include

(1) improved ability to differentiate the end product, (2) better access to distribution channels, (3) better access to market information, and (4) proprietary knowledge.⁵⁹ The case of the first identified linkage, called “Paragon Wafer”, derives from ME’s vertical integration. This is relatively difficult for competitors to duplicate.

Paragon Wafer Linkage

The definition of two manufacturing processes within Lucent Microelectronics follows:

Lucent’s Silicon Materials Operation (henceforth referred to as Silicon Materials) makes it one of the most vertically integrated companies in the semiconductor industry. Silicon Materials manufactures wafers for wafer fabrication (the process to be described next). A wafer is a substrate made from a semi-conducting material such as silicon and used as a foundation for building integrated circuits (ICs for short). As stated above, ICs are minute devices used to perform various electronic functions. The input for Silicon Materials is raw silicon, and the output is silicon wafers for wafer fabrication. (A flowchart of the silicon materials manufacturing process can be found in Appendix 2).

Wafer fabrication is the highly complex process of building integrated circuits on silicon wafers, usually performed in a cleanroom. A cleanroom is a room where air, water, temperature, personnel, equipment and process chemicals are tightly controlled to prevent contamination of wafers during fabrication. Specific steps in wafer fabrication include ion implantation, photolithography and metal deposition. Photolithography can be further broken down into the oxidation, photoresist application, photoresist exposure, photoresist develop, bake, etch oxide, and photoresist removal process steps. In the wafer fab, wafers undergo the above steps several times to acquire the conducting, semi-conducting and insulating layers that enable the electrical circuitry to function as designed. The process is outlined in Appendix 3. When a wafer is completed in wafer fab, all the IC sites on the wafer are tested. The sites that pass the test are identified before the wafer is sawed up. These identified good chips are assembled into plastic or

⁵⁹ Porter, Michael E., Competitive Strategy: Techniques for Analyzing Industries and Competitors (New York, NY: The Free Press, 1990): 315-318

ceramic packages for use on printed circuit boards. Once ICs are assembled into packages, they are tested again before being shipped to customers.

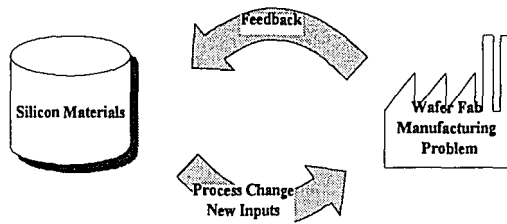


Figure 6: Paragon Wafer Linkage

The Paragon Wafer Project occurred in ME-Allentown in 1993 and 1994. The outcome of the project was higher wafer fab yields that resulted from process improvements in silicon materials. The project originated when two engineers in Allentown's MOS-V wafer fab observed in early 1993 that IC yields near the edges of wafers had over time declined compared to yields at the center of wafers. Analyzing the problem, they found that the lower yields were due to steppers not focusing as well at the edges of wafers because the edges were not "flat". Steppers are photolithography equipment that repeatedly expose and print images of a reticle (an IC circuit diagram) onto the surface of a wafer. Each image is the building block for an IC, which is created after further depositions and removal of conducting, semiconducting and insulating materials onto the wafer. When there was less than ideal flatness at the edges, an imperfect image was imprinted on the wafer surface, resulting in images "rolling off" the edges and short circuits occurring from the bridging of adjacent channels. Channels are the metallic lines etched into the wafer to form paths of conductance. These phenomenon resulted in lower wafer yields.

After the initial discovery, yield improvement and wafer fab process engineers consulted with silicon materials engineers to do root cause analyses. At this point, the quest for a flatter wafer became a joint effort between the wafer fab, yield improvement and silicon material engineering staff. All three groups were very much involved from the problem definition stage through problem solving and process improvement implementation. Upon further investigation, the teams found out why Silicon Materials and

Wafer Fab had not detected this problem earlier. Silicon Materials' wafer flatness inspection had been set up to measure various points on the wafer surface 6mm from wafer edge because this was as close to the edge as chips were deposited. As wafer fab technology had progressed and steppers had improved in accuracy, however, chips were now being placed as little as 3mm from the wafer edge. It turned out that Silicon Materials' quality process was not measuring the problem area.

Once the problem with flatness at wafer edges was discovered, Silicon Materials needed to come up with a flatter wafer, i.e. one that was flat throughout the wafer surface. The desired improvement in wafer flatness came from "Sinpol", a new wafer polishing process that was introduced into Silicon manufacturing in late 1993. It was developed by Jeff Koze in the Silicon Materials engineering group as a solution for the wafer flatness problem and patented by ME.

From the Silicon Materials perspective, various wafer and silicon process improvements were being investigated by members of the Silicon Materials engineering team as part of on-going R&D/engineering long before the wafer flatness issue came to the fore in Wafer Fab. These investigations included some precursors to "super flatness" technology.

Super Flatness

The key parameter for wafer flatness is how well steppers print on a wafer. Each stepper has a certain flatness budget⁶⁰ which has gotten smaller with each successive new wafer fab technology (the industry standard is currently channel lengths of 0.5 microns. Many companies are swiftly moving into 0.35 micron channel length technology).

Lucent developed a patented process, known as the Sinpol or lapped etch, to make very flat wafers. At lap (the flattest area of a wafer), any polishing degrades wafer flatness. However, if the wafer is covered with nitride prior to polishing, the high silicon spots on a wafer could be polished off while the low spots are protected by the nitride. This discovery was serendipitous. A batch of wafers going through the backseal

⁶⁰ A flatness budget is the maximum "bumpiness" on the surface of a wafer beyond which a stepper cannot focus a chip image on the wafer accurately. "Bumpiness" is the difference between the highest and lowest points on the

nitride process were polished in front as well as in the back. They turned out to be flatter than most wafers, and the “Super Flat” wafer was born. The extra flat wafers that Silicon Materials could now produce eliminated the edge roll-off problem in Wafer Fab and greatly improved process yields. The impact of Super Flat wafers is especially dramatic for larger chips where any number of chips recovered and usable increases the yield on that wafer tremendously (yield is the percent of good chips over available chips on a wafer). As ME is increasingly building larger chips for high end customers who demand a lot of functionality, the additional yield for larger chips enables ME to support these particular customers at lower cost. This makes a difference to the bottom line because chips for high end customers typically command a premium price.

The surface of a wafer can be divided into several sites, and the flatness within each site measured. The measure for wafer flatness is the percentage of sites meeting the flatness criteria. The larger the percentage, the “flatter” the wafer. ME wafers are considered higher quality than those produced by other suppliers because they are flatter.

In addition to super flatness, a number of product innovations and process changes championed by various Silicon Materials engineers were consolidated into the Paragon wafer project to produce a wafer that was superior in features, quality and reliability to the then industry standard wafer:

- Elimination of the secondary flat
- Backsurface laser marking
- Control of the primary flat bisector
- Pullback of the backseal
- Bright etch of the contour

wafer surface. For smaller channel length technologies, steppers have to focus the chip image more precisely and accurately, and this can only be done with a minimal amount of bumpiness, hence the term “flatness budget”.

These innovations represented the culmination of three years of process improvement and R&D efforts in Silicon Materials, tremendous teamwork within the Silicon Materials Group, and frequent communication and collaboration between Silicon Materials and Wafer Fab engineering.

There were several reasons why Silicon Materials was so intent on process and product improvement. First, silicon materials operations were outside ICD's mainstream interests, as all other facilities were geared towards the manufacture of semiconductors. It was thus viewed as a cost center by ME management and not the most strategically important area. It was an area into which ME had invested much money in the past and yet it was called upon to meet the increasingly stringent requirements of advanced wafer fab technology, such as the smaller channel length technologies in Orlando and Madrid. Silicon Materials was thus frequently called upon to demonstrate its value to ME, especially in times of strict budgetary constraints. Silicon Materials people were rewarded by their management for being creative and they were encouraged to "think outside the box" to make changes that would enhance productivity and delight the customer, i.e. wafer fab.

Second, Silicon Materials only made 5" and 6" diameter wafers, at a time when the industry standard wafer size was 8". As there was inherent wafer fab cost advantages from the use of larger wafers, ME already started out with a cost disadvantage relative to competitors. The use of smaller wafers was due to a combination of ME not being able to process the larger wafers without a brand new wafer fab and not being able to make the large capital expenditures necessary to build a new fab at the time because it had only just become profitable. Existing fab equipment, especially the older wafer fab equipment in Allentown, could not be retrofitted to accommodate larger wafers. In addition, the long lead times and huge capital outlays required for the construction of an 8" wafer fab (equipment lead times of up to a year, the cost of a new fab averaging US \$1 billion in 1994/95) made the transition to 8" wafers unfeasible in ME in 1994. With these wafer size limitations, ME had to make every square inch of every wafer count. Any silicon material and wafer fab yield improvements paid enormous dividends and were critical for ME to reach cost parity with competitors and essential for the long-term viability of ME in a very competitive industry. These above changes and improvements were required so that Lucent could be more competitive.

To aid in explanations of the changes represent in a Paragon wafer, a diagram of a typical silicon wafer is shown below:

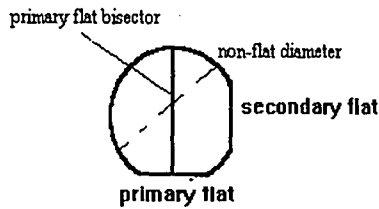


Figure 7: Illustration of Silicon Wafer

Elimination of the Secondary Flat and Backsurface Laser Marking

The impetus for these two process changes improvements came from frequent communication and feedback between the Wafer Fab Yield Improvement Team and Silicon Materials, plus brainstorming ideas by both groups on ways to increase the space available for chips on a wafer. This was critical at a time when Lucent used 5" and 6" diameter wafers in-house while much of the industry was moving to 8" wafers.

The industry convention then was to use the presence of a secondary flat to identify wafer type. Other than that, the secondary flat on a wafer served little purpose. Given that Silicon Materials was already using numbers that were laser scribed on wafers to convey information about the wafer, including wafer type, the secondary flat identification was found to be redundant and could be eliminated.

Around that time, the use of laser scribe numbers on wafers was reviewed as well. Silicon Materials used laser scribed numbers on the back of wafers to identify wafers while Wafer Fab used front-scribed numbers. The wafer fab yield improvement group wanted to have the size of laser scribes at wafer edge reduced because engineers found good chips on wafer right next to the laser scribed area. Laser-scribed areas on a wafer surface were non-usable for IC production.

The Yield Improvement and Silicon Materials Group reached a mutual decision to limit the information scribed on a wafer, condense the front surface laser scribing and eliminate the backsurface laser marking

There were two benefits to doing this:

1. The area available for chips on a wafer was increased;
2. Wafer contamination from material kicked-up during the laser scribing process was reduced.

Control of the primary flat bisector

The primary flat bisector was not typically a parameter measured and controlled by merchant silicon vendors. However, the reason Lucent controls the primary bisector is to prevent wafer alignment problems in the photolithography process. When wafers are mounted on a fixture before imprinting during the photolithography process, it is aligned if the wafer primary flat rests against a hard edge on the fixture. If the wafer is not aligned properly, the IC images may not be exposed and printed correctly on the wafer during the photolithography process. This decreases the yield and number of good chips on wafer. Silicon Materials' solution was to add one additional process step and an additional quality check to strictly control the primary flat bisector in the manufacture of silicon wafers.

Pullback of the Backseal and Bright Etch of the Contour

One innovation that Silicon Materials had come up with earlier was creating a backseal on wafers as a barrier to autodoping. Autodoping is caused by the movement of boron from the bottom wafer surface to the epi layers during the diffusion process, which causes contamination of the epi layer and degraded reliability. By creating a SiN layer, which acts as a diffusion barrier to the boron in the wafer, Lucent wafers can have contamination-free epi layers which increases yields in wafer fabrication. This nitride backed wafer is unique to Lucent. Other silicon suppliers do not know this innovation.

Unfortunately, the nitride backseal also created some new problems for Wafer Fab and Silicon Materials.

The backseal pullback and bright etch innovations originated from the efforts of a Silicon Materials engineer seeking to address a wafer breakage problem in ME's Madrid fab. He spent a few weeks in Madrid investigating why the Madrid wafer fab process was experiencing a relatively high frequency of wafer breakage. The initial suspect was micro-cracks formed in the wafer surface during the epi deposition process. A process change was introduced in Silicon Materials to prevent that from happening.

The layers of coating on a silicon wafer are illustrated on the following diagram:

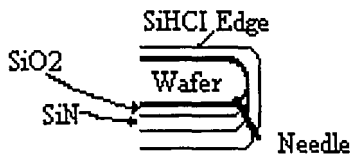


Figure 8: Epi layers on silicon wafer

After a wafer is sawed, it goes into the epi deposition process, where it undergoes the following steps to create a wafer backseal:

1. When wafers are first sliced off from the silicon column, they have rounded edges. The edges are then contoured.
2. A thin layer of Silicon oxide is deposited on the wafer. This creates an oxide layer around the wafer. This step is done in a furnace tube.
3. A thin layer of Silicon nitride is deposited on the wafer, creating a nitride layer around the wafer. This is also a furnace operation.
4. The front of the wafer is polished to remove the oxide and nitride layers from this surface.
5. The epi layer (formed from Silicon Hydrochloride) is deposited over the entire wafer.

The micro-crack problem was caused by the “pinholes” that formed in the nitride layer where it wrapped around the edge of the wafer (during step 3). Once that happened, silicon from the gas stream collected in the pinholes as the wafer was exposed to chloride gas during the epi process, forming tiny “needles” on the back surface of the wafer (illustrated in figure 8). As the silicon wafer is ground smooth later in the silicon manufacturing process, these “needles” break off, leaving micro cracks on the wafer surface and increased contamination that could create future process problems downstream. Silicon Materials implemented the following epi process changes to prevent formation of the microcracks: First, the amount of oxide and nitride deposited and allowed to seep into the wafer during steps 2 and 3 was reduced; Next, the SiO₂ and

SiN layers were smoothed out prior to the SiHCl₃ epi layer application; Last, the backseal was pulled back far enough so that there were no reactive gases and growth in the back layer during the epi deposition process. These process changes solved the micro-crack problem and made for a brighter and flatter edge and surface on wafers, which improved wafer quality and reliability. As it turned out, the wafer breakage problem in Madrid was caused not by microcracks, but by an equipment problem in wafer fab.

The epi backseal innovation is unique to Lucent. Wafers without an epi backseal made for a longer cycle time in Silicon Materials because the epi layer deposition would have to be done at lower temperatures to prevent multiple defects in the epi layer from auto doping. This created a bottleneck at this process step. With the back-sealed Paragon wafers, epi deposition can now be done at temperatures of more than 100 degree C, which increases efficiency in Silicon Materials.

Outcomes

The process and product improvements implemented by Lucent have made for unprecedented yield and reliability improvements. Several Silicon Materials engineers participate in industry groups like SEMI and help draft industry standards. They have a good sense of where ME is with respect to the rest of the silicon materials industry and feel that Lucent has developed and implemented some unique and advanced process capabilities. For instance, the use of nitrides as an autodoping barrier appears to be unique to Lucent, and the industry is only now moving towards the elimination of secondary flats on wafers. Also, many suppliers do not yet control the primary bisector parameter on wafers. At the moment, the only other firm doing bright etch of wafers is a Japanese firm, but their process is relatively more labor intensive and prolonged than Lucent's. These technological advancements have enabled Lucent to provide wafers at 1/2 to 2/3 the cost of commercially procured wafers..

The production qualification process for Paragon wafers in wafer fabrication was done by using these wafers for a total of 50 production lots in the Allentown wafer fabs. These were regular production lots started in the same week, so there was a good cross section of products, technologies, and chip sizes. Also, by using a cross section of products in each wafer fab, the mix also included high volume and low volume

products. The yields for these lots were carefully examined throughout wafer fab to make sure that there were no hidden problems with Paragon wafers. The results of using Paragon wafers were very promising. Yields improved 10 to 20% for some products.

As a result of these changes in the silicon materials process, the percentage of high grade wafers produced by the silicon materials facility improved. This resulted in a 16% improvement in IC yields from Allentown's MOS-V fab. Results were also excellent in ME's Orlando and Madrid fabs, though not to the same extent seen in Allentown because Orlando and Madrid had more advanced steppers to begin with. Orlando saw an 8% IC yield improvement from using Paragon wafers. The wafer fabrication yield improvements in Allentown, Orlando and Madrid produces many benefits, including lower IC manufacturing costs, higher capacity in wafer fabrication facilities (which when capacity is tight, has been the bottleneck processes in ME's manufacturing operations), higher revenue, better ROA and ROI, and improved profitability. This improvement has also led to ME being able to support a broader base of customers and being able to accept more business from them, which contributes to the long-term health of the business. An indication of the cost savings made possible by paragon wafers is illustrated in the following example.

According to reports, the cost of implementing all the Paragon wafer improvements in Lucent Technologies was approximately \$120,000. There was little incremental capital investment. The major new piece of equipment acquired by Silicon Materials for the Sinpol process was a furnace that the MOS-V wafer fab no longer needed. For Silicon Materials, the cost of the improvements and innovations consisted mainly of engineering time for research, development and operator training. Lucent's wafer fabs did not incur any additional costs to implement Paragon wafers because the wafers were optimized for use in Lucent's wafer fabs. To measure the financial impact of the Paragon wafer, consider a high volume product that Lucent ships at a rate of 50,000 units a month. This product or "code" (Lucent's term for specific ICs sold to customers) is fabricated in ME's Allentown wafer fab. Assuming that there are 200 potential sites on a wafer for this code, and that the former yield measured after wafer fabrication averaged 100 good chips per wafer, with Paragon wafers, the yield on this product improves to 116 good chips per

wafer (using the average yield improvement seen in Allentown). Assuming also that the yield from probe (wafer test after wafer fab) to package test is 85%, to measure the number of wafers needed to produce 50,000 units, then and now, is as follows:

Number of standard wafers needed: $50,000 \div 0.85 \div 100 = 588$ wafers

Number of Paragon wafers needed: $50,000 \div 0.85 \div 116 = 507$ wafers

588 ordinary wafers would have to be started in wafer fab to produce 50,000 shippable chips in three months time. With Paragon wafers, only 507 wafers are needed to support the same volume of business. This means there are 81 wafers that Lucent would not have to start each month to support the business for this customer. Multiply this impact by the hundreds of products manufactured by Lucent and one can envision how the increased manufacturing capacity now available within ME can lead to enormous cost savings and opportunities for additional revenues. For instance, if the cost of completing a wafer currently costs Lucent Technologies \$500, Lucent would save roughly \$40,000 for every 50,000 chips it ships, or \$0.80 per device. This is significant in a highly competitive market where business has been lost to competing bids which are cents lower per chip. In addition, if a customer should approach Lucent with an order for an additional 10,000 parts a month, Lucent now has the capacity to support most, if not all, of this new business without the need to make capital additions and enhancements. This would not have been possible with non-Paragon wafers.

Flash Linkage

The Flash project is affected by and affects ICD's weekly "wafer start" process. The process is described as follows: Every week, product planners from each internal business unit (BU) determine the number and type of product needed by the BU in 8 to 13 weeks (equivalent to manufacturing interval range) to meet customer requirements. The manufacturing interval for a product is determined by the technologies and factories used to manufacture the product. In general, a product manufactured with mature wafer fab technology and assembled using a highly available chip package has a relatively short manufacturing interval.

Customer requirements are communicated to the factory through placed orders or forecasts from the customer's procurement department. Once this information is available to ICD, product planners estimate the quantity of each product to start in wafer fab during the following week to best support customer demand and maximize ME's revenues. The quantity of wafers started are limited by the total wafer fab capacity available to ICD.

As mentioned earlier, a batch of a specific chip product is manufactured by printing distinct patterns on silicon wafers, and successive depositions and etching on the wafers until the printed circuitry is built up. Generally, several chips of one variety are created on each wafer. After wafer fabrication, wafers are sawed up to separate the chips on the wafer. The individual chips are inserted into chip packages or shells during the assembly process. The packaged chips are then shipped to customers, who will insert them into printed circuit boards.

When all ICD product planners have submitted their wafer start requirements, and the quantity of each type of product to be started the following week is finalized, factory planners for each wafer fab will collect all the required reticle sets and supply photolithography supervisors with a list of the quantity of silicon wafers to be imprinted with each reticle set.

According to reports, all wafer starts do not have equal impact on ME's capacity. This is because some products are more complicated and require more time and resources to manufacture. "Flash" time is the amount of time it takes for one wafer to get through the photo expose step in the photolithography process. Flash is an important factor to consider for capacity evaluation and planning because the photo expose process typically has one of the longest cycle time. As a result, photolithography steppers are usually bottlenecks in the wafer fabrication process. Since wafer fabrication is the most time consuming part of IC manufacturing, any process or product change that alleviates cycle time in wafer fabrication improves ME's capacity.

During the flash step, chip images are exposed onto a wafer. The cycle time at this exposure step depends on the size of the chip and the particular stepper used. As the figure 8 shows, the size and geometry of a particular chip determines the number of chip images that can be exposed at a time.

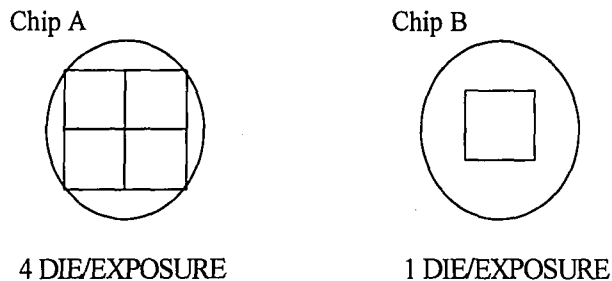


Figure 8: Impact of die size at the photo expose step

For instance, chip A is smaller than chip B and therefore four chip images of A can be exposed at a time versus one chip image of B for a certain type of stepper. The wafer surface will be completely filled with chips by repeated exposure of the image onto various areas of the wafer. If a 6" wafer can accommodate either 200 chips As or 200 chip Bs, the chip B wafer could take three to four times as long as the chip A wafer to process in photolithography.

As there could be as many as 800 ICs on a wafer, the number of die exposed at a time onto the wafer affects the number of flashes needed and significantly impacts the cycle time for the product at photo expose. This is because the photolithography cycle time is directly related to the number of times the stepper has to expose the wafer to the reticle.

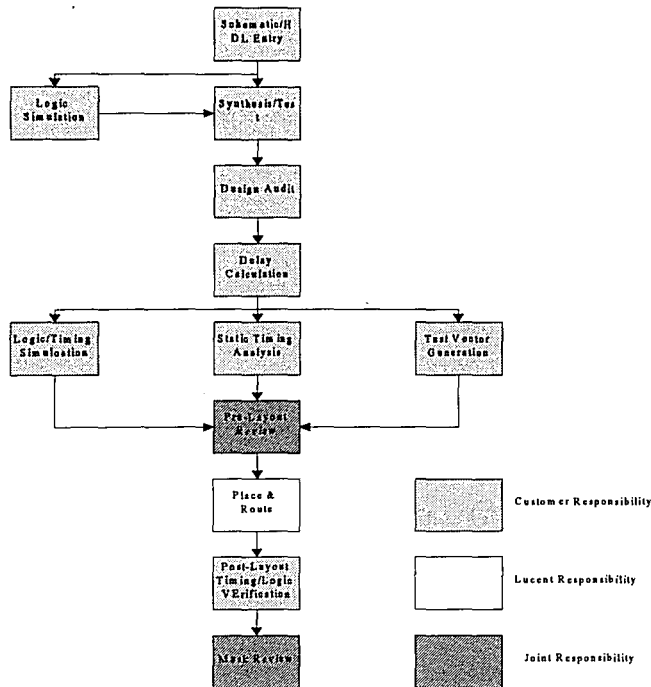
There are a number of linkages that could positively affect the "flash" or photo expose step in the wafer fab process. The first of these relates to the activity which assigns products to the various ME wafer fabs and schedules them.

In addition to chip size, the number of flashes also depends on flash window sizes of specific steppers. In this case, it is impacted by (1) the diagonal width of the window, and (2) the channel length of the product

(the smaller the channel length, the greater the chip density and the greater the number of chip images per exposure).

There are three kinds of steppers used within Lucent Technologies -- GCA (15mm window), G-Line (17 mm window), and I-Line (21 mm window). As each stepper has a window or aperture of a certain size, the number of IC images from the wafer reticle that can be exposed through the window varies. A chip with a die size requiring four flashes on a GCA stepper may require just one flash on an I-Line. This too impacts the capacity of steppers within ME and production scheduling of product at wafer expose. For example, ME's Madrid fab has a policy limiting the use of higher capacity I-Line steppers to photolithography processing of high volume products, thus maximizing wafer fabrication thruput and minimizing cycle time. Another implication of flash is the varying cycle time of the same product in different fabs because each has a unique mix of steppers. Allentown wafer fabs tend to have older equipment, including a higher percentage of GCA steppers in the stepper mix. On the other hand, the Orlando and Madrid wafer fabs have more G-Line and I-Line steppers. It therefore makes sense for the factory planning people and product planners to limit the manufacture of certain products to one or two specific wafer fabs. The above are some Flash-related considerations for marketing, R&D and manufacturing when making a decision on where new products are to be manufactured.

The second linkage relates to the circuit design activity which is performed in Bell Labs. ME could develop design-for-manufacturing guidelines that would minimize the number of flashes required for a product. These design rules would specify chip size limits that if followed, would optimize the flow of a product through the flash activity in wafer fab. The primary effort to develop these guidelines would probably come from ME manufacturing process engineers working with Bell Labs design tool engineers to develop new modeling files for chip designers. Below is a flowchart of ICD's ASIC design cycle. The Place & Route process step would be the point in the design process where the supplemental design rules for Flash impact chip design because this is step where the layout of circuits on a chip is defined.



Source: Lucent Microelectronics

Figure 9: ASIC Design Cycle in Lucent Technologies

Designing with Flash Design-for-Manufacturability rules in mind would enhance the manufacturability of ICD chips. This could minimize future occurrences of a chip being too large in relation to the size of the stepper aperture window to be printed at a rate of four or more images per exposure onto a wafer. Many chips currently being exposed at the rate of one image per exposure could have printed with four images per exposure had they been just a little smaller. This would have greatly reduced the number of flashes and cycle time through photo expose for these products, and improved wafer fab thruput and capacity utilization. The addition of new design rules, if it does not become too cumbersome for ME's designers and design tools, would truly benefit ME manufacturing. This is another instance where the greatest value added per change is early in the product life cycle when R&D designs a product.

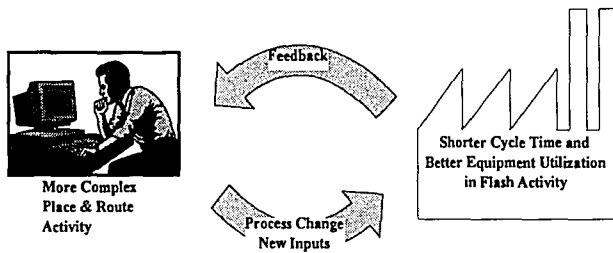


Figure 10: Flash Linkage

If implemented, Flash Optimization would not be the first instance of collaboration and linkage optimization between manufacturing and R&D. There have been numerous instances of collaboration between manufacturing engineers and Bell Lab engineers (Bell Labs owns the chip design process and development of new product technologies). For instance, the 0.9 micron wafer fab technology was a mature technology where incremental improvements were more likely to result from yield improvement efforts in large improvements. Even then, two consecutive design rule changes implemented to scale down devices by 10% each time enabled ICD to wring more capacity and capability out of a mature technology. In this case, the rules were proposed by manufacturing and implemented by a joint Bell Labs-manufacturing team. There were several benefits to scaling devices down in size. They include:⁶¹

- A design, if shrunk, will give more die per wafer because the die is reduced in size.
- For a standard chip size, larger logic or memory circuits can be achieved.
- Faster switching speeds are possible with small devices.

The first design rule change enabled ICD to scale down devices such that devices with 0.6 micron channel lengths could be manufactured using existing 0.9 micron technology. The second design rule change enabled ICD to manufacture 0.55 micron channel length devices using 0.9 micron equipment. This extended the useful life of equipment and facilities in Allentown, delaying the need to make additional capital investments to support demand for ME products. The process of changing design rules for scaled

⁶¹ Evans, A.G.R., "Design Rules, Verification and Scaling," in VLSI Circuits and Systems in Silicon, ed. Andrew Brown (London: McGraw-Hill Book Company, 1991), 340.

down devices was learned from ME's foundry customers, who do this routinely to cut costs and make the most of the technology they have.

Finally, ICD has already taken two immediate steps with respect to the Flash activity. Both would improve the overall ICD value chain:

1. The use of smaller aperture GCA and G-line steppers for manufacturing high-flash-time products has been curtailed. Instead, these are now run exclusively on larger aperture I-line steppers, which improves overall thruput in wafer fab.
2. A "flash" factor has been incorporated into the cycle time equation used by ICD to estimate manufacturing intervals for specific products, thus enhancing cycle time predictability for products and allowing ICD to improve capacity utilization.

Chapter 11: Analysis of Linkages

Lucent Microelectronics' Paragon wafer was a new and improved wafer which incorporated many technological innovations or process changes by the Silicon Materials group. The use of this wafer led to a 16% yield improvement in wafer fab.

Contributors to Linkage Management

The following observations were made about the factors that contributed to the Paragon wafers success story in ME-Allentown:

1. Frequent and extensive communications among the wafer fab process engineers, the wafer fab yield improvement team and silicon materials engineers certainly facilitated the success of this project. This was probably due to
 - (1) Co-location of silicon materials and wafer fab in Allentown. This enabled frequent collaboration, real time information transfer and evaluation, and face-to-face meetings. The importance of location for value-chain linkages is borne out by published studies. Linkages between operational and support activities for the purposes of coordination and control are

very important, and strongly affected by the locations of the activities. For example, innovation requires close coordination and communication between R&D, manufacturing and marketing. Geographical dispersion is a severe handicap towards such coordination. Quality control requires coordination and swift feedback between sales activities, assembly and component manufacture. And, overall cost efficiency requires that management be able to monitor and quickly respond to cost variances anywhere within the firm. Several U.S. and European companies which set up plants in low-wage countries discovered that the benefits from low wages are somewhat offset by issues such as the difficulty of coordinating material supplies, product assembly and market requirements; Some companies have also experienced low productivity or poor quality control because of culture and language gaps as well as slower learning curves.⁶² ME's own experience shows that communication, coordination and speed in reacting to changing market or industry conditions is relatively difficult in a firm with far-flung factories and sales offices.

(2) Personal friendships and long-time acquaintance among engineer and managers of wafer fab and silicon materials. Many of the engineers involved in the Paragon case had worked together in the past. This was probably due to the fact that Lucent's Allentown facility had been in existence for 50 years and provided a relatively stable environment with low staff turnover. Also, a member of the wafer fab yield improvement team had worked in Silicon Materials for many years prior to his move to wafer fab, facilitating the technology transfer and ease of silicon-related problem solving in wafer fab.

A major innovation in the Paragon project was the improved flatness at the edges of wafers, which led to significantly higher yields downstream for chips located near the edge of wafers. The problem with the wafers that ME used prior to Paragon wafers was that yields were very low for chips near the edge of wafers. This observation was first made by a member of the wafer fab engineering team. Later, the wafer fab engineers and yield improvement team discovered that it was due to insufficient flatness at the edge of

⁶² Grant, Contemporary Strategy Analysis, 293

the wafer, so the pattern imprinted on the wafer was “rolling off” at the edges. This feedback was fed back to Silicon Materials. What was significant about these transactions was that no one interviewed could definitively identify a single person to which problem observation and problem solving could be attributed. Although a silicon materials engineer received a patent for the process change implemented to improve wafer flatness, there seemed to have been much cross organizational collaboration and communication among all three engineering groups. Each step in the observation, discovery and process change process was characterized by much feedback and iterations among the three groups. Interestingly, although this was a multi-functional effort, the initial contacts were not made through “official channels” or the hierarchy. This seemed to make the problem solving and change processes more effective and efficient, and enabled implementation of far-reaching changes.

The fact that ME’s Silicon Materials Group is a captive supplier to Lucent meant that it was extremely responsive to feedback, inputs and requests from ME’ wafer fab facilities, especially Allentown. The wafer fab people interviewed recognized that they would not have gotten this same level of cooperation, responsiveness and problem solving if they had to work with a merchant silicon supplier. Problems found would not have been solved as quickly, and product improvements would probably not have been implemented as quickly. This is an instance where ME’s vertical integration facilitated problem solving. The resulting competitive advantage is sustainable because most of ME’s competitors are not in the silicon manufacturing business. Also, there likely would have been more organizational and cultural barriers to working together encountered in working with merchant suppliers than one that is in-house. Through cost savings, technological innovations and process and product improvements, Silicon Materials is currently supplying advanced wafers to ME wafer fabs for 2/3 the price charged by external suppliers. Another advantage of vertical integration to ME is that wafer fab gets better information from Silicon Materials than from merchant suppliers and can tailor their processes to make full use of the specific characteristics of the silicon wafers. The reverse is also true - Silicon Materials can change their process to best meet wafer fab requirements.

Another instance where co-location helped in the success of this case was the relatively easy implementation of Paragon wafers in the Allentown wafer fabs. Allentown became the early adopter of this process change in part because all its wafer fab engineers were located near the silicon engineers and could receive real-time help and advice in the implementation. In addition, the wafer fab engineering group had already bought into using the new wafers because they participated fully in the development of the new wafer process. Implementation at the Orlando and Madrid wafer fabs was relatively more challenging because of distance, time difference, and greater organizational and cultural barriers. In addition, the Orlando and Madrid factory managers and engineers had to be convinced about the efficacy of these new wafers.

Obstacles to Linkage Management

Although most groups grasped the fact that the use of Paragon wafers could improve yields and certainly were not opposed to the process changes, implementing the use of Paragon wafers in wafer fab still took a year. The reasons for the slowness of implementation included resistance from the following groups:

Engineering: Before they would support the change, design, process and product engineering groups had to be convinced of the benefits of Paragon wafer implementation because it was an extensive and fundamental change in wafer fab processing.

Hourly production people and supervisors: Resistance from this group may have originated from a fear of the potential complications caused by process changes.

Engineering management: As the funds available for process change implementation were limited, budgetary concerns were always an issue. In addition, this change crossed organizational boundaries, which meant that more change management, communication and hand-holding was required from the silicon and wafer engineering groups, making management's job more challenging.

The ICD culture has traditionally been one that was conservative, not highly accepting of change and in general, one that believes in competing through excellent product quality rather than low cost. In addition, the ICD organization is strongly functional, a characteristic it shares with many large, mature firms.

People are grouped primarily by discipline, each working under the direction of a specialized subfunctional manager and senior functional manager, The different functions coordinate activities and ideas through detailed specifications that all parties agree to at the outset and through occasional meetings where cross-functional issues are discussed. Over time, primary responsibility for product or process development passes sequentially, and often not very smoothly, from one function to another, a transfer style known as “throwing it over the wall.”⁶³ This strong disciplinary-based functionality was evident in the implementation of Paragon wafers. In Allentown, the fab and silicon engineering staff and managers were for the change, as were the product managers and product engineers, because of the yield improvement Paragon wafers promised for specific products. However, to satisfy constituents with different priorities, such as the wafer fab production organization and the quality department, engineering had to prove-in Paragon wafers by using them in 100 production lots in wafer fab. These wafers were tested exhaustively throughout wafer fabrication to verify quality, manufacturability and reliability before they could become a standard part of the wafer fab process. It is safe to speculate that some of ME’s competitors could have implemented a change like Paragon wafers without the series of tests and hurdles that seems to precede a change implementation in ME.

To better understand this organizational resistance to change, observations by Hayes, Wheelwright and Clark resulting from studies of numerous companies and manufacturing environments in transition seem particularly relevant. They note that much of an organization’s reluctance to implement new manufacturing and quality improvement programs may stem from the fundamental, wrenching and far-reaching transformations required throughout the enterprise. Although these changes primarily affect the manufacturing function, some amount of transformation is also required within other functions, impacting those functions and their relationship with manufacturing.⁶⁴ More than that, a significant change means that the organization’s fundamental assumptions and organizing principles must be realigned. This level

⁶³ Burgelman, Robert A., Modesto A. Maidique and Steven C. Wheelwright, Strategic Management of Technology and Innovation (Chicago, IL: Irwin, 1996): 666-667.

⁶⁴ Hayes, Robert H., Steven C. Wheelwright and Kim B. Clark Dynamic Manufacturing: Creating the Learning Organization (New York, NY: The Free Press, 1988): 344-345.

of transformation requires more stamina, commitment and dedication than most individuals and organizations are willing to undertake. This is why the change undertaken so often seems to fall short of intended goals.

Hayes, Wheelwright and Clark go on to list the type of obstacles to change typically encountered in various parts of the organization:

Obstacles to change within Manufacturing: (1)The assumption by everyone that the changes attempted are just another program for manufacturing improvement. Everyone therefore assumes that fundamental changes will not be required and it is just business as usual; (2)Because manufacturing is usually so large and complex in relation to other functions, fundamental changes in manufacturing take longer than those in other parts of the business. This trend is exacerbated by manufacturing also being the function under maximum short-term pressure to meet daily schedules and resolve operating crisis. Most manufacturing people spend so much time fire-fighting and making things work that they do not have the time or resources to eliminate the root causes of these problems; (3)The manufacturing organization's inexperience in dealing with anything other than tactical operating issues. Most manufacturing people who came up through the ranks learn that "getting product out the door" is all that counts. This set of pressures facing manufacturing has led to a preference for "playing it safe" and a reluctance to take risks in case mistakes are made, because mistakes are penalized. In the past, this has made it difficult to implement radical changes in manufacturing.

Obstacles to change within other functions: (1)The second-class image of manufacturing that has built up in many companies over the years, and the rest of the organization seeing manufacturing as a constraint instead of an asset. This is a vicious cycle because manufacturing organizations that fail to meet their commitments every month continually reinforce this negative image, which in turn undercuts manufacturing's efforts to improve itself. Over time, manufacturing in such organizations learns to "play it safe" and not take risks, i.e. making the numbers and focusing more on the short term.

proven to work as planned through extensive testing. There are advantages and disadvantages to this cautiousness: The advantage to full qualification of the process change meant no nasty surprises when the process change was implemented. On the other hand, ME lost up to a year of the yield improvements and productivity gains it could have achieved had it implemented Paragon wafers more quickly.

Other non-manufacturing obstacles are created by people advocating easy answers. To be fair, these people may in the past have been influenced by their impression of manufacturing's inability to fully support their goals and objectives. However, such people, who are usually from outside manufacturing, tend to look for actions that promise quick relief without fully understanding the problem, the environment or the solutions proposed. As dramatic changes in an organization take a lot of time and enormous effort, any energies deflected towards short-term palliatives make it even harder for the dramatic changes to happen in the organization. For instance, some people in the organization may advocate contracting out activities or moving them off-shore to reduce costs instead of undertaking a program for manufacturing improvement because the former is easier to do. Unfortunately, this may not be the optimal solution for the long-term health of the business.

Another obstacle to change is caused by possible changes to the balance of power within a firm. People who lose decision making freedom and other forms of power because of value chain activity and linkage optimization may well oppose changes because of their perceived "loss of power." Parochial concerns and some territoriality may come to the fore in times like this when significant changes are made, even when the changes are supported by most people within the firm.

One of the most important obstacles to change is lack of urgency within an organization. This is why CEOs often have to engender a sense of crisis throughout the organization. Without the sense of urgency, it is harder to implement far-reaching and fundamental change. Besides engendering the sense of urgency, senior managers must truly believe in the change initiatives they propose, and back them up with allocations of time and resources. It is very important for executives to "walk the talk" when they want to see change in an organization. Any change takes a lot out of the people involved, from the change agents

to functions that are peripherally involved in the change. Unfortunately, even when change implementation is done correctly, there is no guarantee that the change will turn out as planned. However, the alternative to change for an organization is unpalatable. A static organization runs the risk of quickly falling behind and losing ground to competitors who practice continual process improvement and is always looking for the next technological innovation to gain competitive advantage.

Part 4: Recommendations

Chapter 12: Recommendations for ICD

Flash Linkage Management

Change management is very important in the opportunity for management of the Flash linkage because it is a cross-functional and cross-organizational change. In addition, R&D has to support the effort for successful implementation of the change to occur. Based on the lessons learned from the Paragon wafer linkage, the following steps are recommended for managing the Flash linkage:⁶⁵

1. Analyze the organization and the need for change.

Analyze the impact of Flash design rules on both manufacturing and R&D. The benefits to manufacturing from this linkage optimization should be balanced against the costs and inefficiencies that R&D will experience. Data required for the analysis should include the number of products affected by the change, the capacity improvement expected after implementation and the additional costs to R&D. Manufacturing might choose to recommend guidelines pertaining only to products and processes where the change would make a tremendous difference.

2. Create a shared vision, common direction and an implementation plan. Once the extent and specifics of the change have been agreed to by manufacturing and R&D management, the change

⁶⁵ Jick, Todd D. "Managing Change" in The Portable MBA in Management, ed. Allan R. Cohen (New York: John Wiley & Sons, Inc., 1995): 344-366.

implementation plan will need to be communicated to everyone in those two organizations as well as other organizations that will be affected by the change. To get buy-in from all groups, the implementation team will have to address concerns and, if necessary, make changes or provisions to the plan. It is very important at this point for management to show their support for the implementation plan.

3. The management of organizations going through change must communicate the following through actions and words: (1)The future is a whole new ball game, i.e. it is no longer business as usual for the organization, (2)A sense of urgency, which could be fostered by linking the change to the company's strategic intent and competitive situation.
4. Develop a strong leader role. The right person in this role could make all the difference in the success of the implementation effort.
5. Line up political sponsorship. Even with management support, an implementation plan would take longer and not be as effective if the key decision makers and influential people in an organizations do not support the change. Often, these key decision makers and influential people are individual contributors and the extent of their influence would not show up on an organizational chart.
6. Develop enabling structures and reinforcements. When implementing change, it is very important to have all support structures, mechanisms, documentation and staff in place. In this case, manufacturing and R&D management could train lead users extensively in the new process so they can in turn be a resource for their respective groups during the implementation of the new process. Any new software and hardware installations should worked as planned without much inconvenience to the user. In addition, training classes, weekly support group meetings, hotlines and a support organization should be in place to help all users adjust to the new process.
7. Communicate, involve people, and be honest, i.e. frequent and open communication in all ways and forms.

8. Monitor, refine, and institutionalize the change: To maintain momentum after a change is implemented, management and the implementation team could put measures and milestones in place.

Organizational Recommendations

The author would like to make add the following recommendations for change in ICD's organization:

- Speed up the process and product improvement process by
 1. Reduce the hurdles and bureaucratic red-tape required by various functions within ME before a change can be implemented. One suggestion for doing so is to make improvement of the ME change process the focus of a cross-functional QIT (quality improvement team).
 2. Change from a bureaucratic hierarchy and a strong functional orientation to more flexible cross-functional teams in managing processes.
 3. Involve as many functions and groups as possible early on in a change implementation effort to increase buy-in and acceptance
- Continuation of the ME Awards program. The year-old ME Awards program was designed to recognize and reward teams or individuals who increase revenue, lower costs or improve quality in ME. This tangibly rewards employees who contribute above and beyond the call of duty, employees who 'think outside the box' to make any improvements, big or small, and teams that improve processes and products.
- ME management could foster more risk taking in the organization by rewarding and recognizing employees and teams that take risks and stretch. More importantly, there should be no punitive actions against mistakes made and risk-taking that failed. Employees have to feel 'safe' in order to stretch themselves and contribute fully.

As linkage management could provide ME with competitive advantage, it should be internalized into ME's culture and way of doing business. Following are some ways for ME to better manage linkages:

- Enhance organizational communication. To begin with, ME management could communicate the firm's goals, strategic intent, competitive situation and industry news often to all employees, using a variety of forums. It is especially important to reach hourly employees who traditionally have not received updates consistently. The efforts of ME management to change and implement new communication forums have been impressive. Such efforts include quarterly all-hands meetings, company-wide telecasts and monthly newsletters which are disseminated through email and person-to-person paper copies. The ME effort is complemented by Lucent's orientation sessions. This year, Lucent's top executives visited all corporate locations to give orientation seminars. This highly effective forum was used to communicate management's vision of the future and the type of corporation that Lucent will be; In addition, intra-organizational communication could be facilitated through use of regular meetings and communication sessions. These do not have to be formal. Individual group within ICD have weekly meetings. One in particular is known as "donut hours" (one can tell what kind of refreshments are offered at that meeting!). Groups and individuals that communicate and collaborate across functions could also be recognized for their efforts.
- Transform the organizational culture so that the organization becomes more of a "learning organization." According to Peter Senge, author of "The Fifth Discipline", an organization and its leaders must develop new disciplines to increase the speed and efficacy of learning.⁶⁶ These include

 - Build shared vision in the organization by (1) Encouraging personal visions,
 - (2) Communicating and asking for support from all people, (3) Internalizing visioning as an ongoing process, (4) Blending extrinsic and intrinsic visions, and (5) Distinguishing positive from negative visions.

⁶⁶ Senge, Peter M, "The Leader's New Work: Building Learning Organizations," Sloan Management Review (Fall 1990): 273-289.

- At a very fundamental level, develop systems thinking skills. These include (1) Seeing interrelationships beyond things, processes and snapshots, (2) Moving beyond blame, (3) Distinguishing detail complexity from dynamic complexity, (4) Focusing on areas of high leverage, and (5) Avoiding symptomatic solutions.

Two years ago, ME President Curt Crawford demonstrated his commitment to continual education by requiring all ME employees to receive 80 hours of training per year. This is a very good start to move the organization towards more learning and flexibility. When individuals are exposed to new ideas and new people through classes, conferences and self-directed instruction, their knowledge increases and more importantly, their thinking is stretched a little. An additional benefit to on-location classes is that they provide an opportunity to get people from various parts of the business together. This facilitates cross-functional interaction, communication and learning, which gets us to the next point.

- Facilitate cross-functional communication and team building within ME. One way to do so might be to institutionalize the process of pulling together “quick strike” cross functional teams to address specific problems. Examples of such teams are QITs (quality improvement teams) and information system implementation teams.
- Constant change has become part of the ME way of life. One indication of this is the number of people involved in change initiatives within the company. ME management has facilitated this development by putting their money where their mouth -- allocating the resources to implement changes, including some of its top people, and if necessary engaging consultants, trainers and facilitators to help local teams get off the ground quickly. As change makes for a chaotic environment and stressed employees, change management is in order at ME.
- ME could form value-chain focused teams to recognize and optimize linkages within the ME value system. Specifically, ME could propagate the teamwork and communications that made the

Paragon Wafer project such a success, empowering employees to reinvent and improve the value chain.

- Develop an organization focused on delighting customers. One way to accomplish this could be to encourage new relationships with third-parties in which both parties benefit, such as partnerships with customers, and joint venture with suppliers, competitors and complementary companies.
- Install information systems to get required information to the right people at the right time. This is a major focus for ICD that is being addressed by the Oracle Application Suite (OAS) and Total Order Management (TOM) implementations.

The author would like to conclude with some words from Tom Peters, who succinctly describes the attributes required for long-term success in a highly competitive industry.⁶⁷ One way or another, ME needs to start valuing the following attribute and incorporating them into the organization:

- A passion for failure
- A thirst for learning and homework
- A bias for action
- A taste for ambiguity
- An abhorrence for pompous and inflexible obfuscators
- A willingness to shoot straight
- A belief in the curiosity of everyone
- A hankering to be weird

⁶⁷ Peters, Tom The Tom Peters Seminar: Crazy Times Call for Crazy Organizations (New York, NY: Vintage Books, 1994): 284-285.

- A penchant for revolution
- A love of laughter and a sense of humor
- A aversion for the tepid response

Chapter 13: Conclusion

In general, linkage management offers ICD opportunities to develop sustainable competitive advantage that are not easily duplicated by competitors. As shown in this study, linkages have enabled ICD to remain competitive in a growing and highly competitive industry. As it turns out, both linkages the author studied were spontaneous linkage optimizations that led to synergies. To increase the chances of that happening in the future, ME must incorporate conscious linkage analysis and management into its strategic and operational planning process. This should not take too much additional effort and time on the part of ICD because linkage management can easily be incorporated into current planning and implementation processes. Following are some recommendations for doing so:

Strategic Planning

Through the benchmarking process, which currently includes interviews with customer and consultants, ICD can find out the biggest needs of various customers, their definition of the ideal supplier and the areas ICD could improve in. From this data gathering, ICD can assess customer needs that are not currently being met and identify areas for focused improvement efforts. The latter should include opportunities for linkage improvement between ICD value activities and the customer's value chain.

Once a year, ICD management and all departments can brainstorm ideas for their vision of the company ICD could be, without constraints. One result from the result can be a "wish list" that includes all the products and services that ICD doesn't offer but could, as well as all the activities that ICD could do or optimize to enhance the well-being of customers, employees and other stakeholders, but currently doesn't. Such a list could set people thinking,

especially if management wanted to set stretch goals to drive linkage optimizations and process improvements.

Operations Planning

Linkage management could be incorporated into this process using the mechanisms that currently exist for activity optimization. For example, a department could solicit feedback on operational effectiveness from upstream and downstream departments. Among other things, this would give the department some examples of situations where linkage management could improve its interactions and information flow with other departments. Next, the department managers can make one or two of these opportunities for linkage management an area of focus for the group.

Part 5: Learning

Chapter 14: Lessons Learned

The author felt that more time should have been spent up front to define the topic of this study and narrow the area of focus. In addition, the project scope was not defined up front but allowed to evolve over the course of the research. This meant that some research and interviews undertaken in the early days of the study became outdated and irrelevant by the time the thesis was written. A contributor to this outcome included starting the study with a vague topic (something along the lines of studying the Microelectronics Value Chain).

Another thing that could have done better was the use of more tools learned in Professor Alden Bean's project management course. Many of the concepts learned in that class, e.g. focusing on a goal, establishing metrics and doing periodic progress checks, would have been tremendously useful in the course of this project because it was very much a long-term, complex project.

All in all, the research and writing required in this study was a good exercise in discipline. As much of my research and study experience to date has been as a member of a team rather than individually, learning to pace and motivate myself was in some ways a learning experience.

One very positive experience from this research was the opportunity to work with the team of subject matter advisors formed by my thesis advisor. It was a privilege communicating, interacting and working with Professors Saunders and Wu

Another helpful exercise throughout the study was doing regular one page proposals or process descriptions about the value chains and Lucent Microelectronics for class assignments, updates to ICD management and updates to the “advisory board.” Much mileage were gained from these one-pagers because they became the basis for the thesis.

The decision to focus on manufacturing value chain linkages in Microelectronics and specifically the Paragon and Flash linkages was made after three interviews to understand process flows and activities within ME. The author found these “scope out the lay of the land” interview very useful for the study. Another good use of time was the process of mapping manufacturing activities and process flows in ME. Although it was time consuming because the information had to be collected from various people and documentation, it was a very worthwhile exercise because it enhanced understanding of the complexities of the ME value system.

Doing this research has been a very worthwhile and rewarding effort. It may have taken been longer than originally planned because this was the first time that someone had specifically focused on manufacturing linkages in the Lucent Microelectronics value chain, making it new territory in some ways. The lack of precedence made it hard to envision the scope of the project. Another factor that impeded progress was time constraints stemming from work responsibilities.

The author found that using the thesis topic as the basis of a final paper in an MOT course prior to starting the thesis was a useful exercise to define the research and writing.

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APPENDIX 1

A PRIMER ON SEMICONDUCTORS

Virtually all electronics used today incorporate semiconductors. These devices perform a wide range of functions in a variety of end-use products – from children’s toys , antilock brakes in automobiles, satellite and weapon systems, to a variety of sophisticated computer applications.

A semiconductor is an electronic device that can be switched to conduct or block electric currents. The popular term “microelectronics” is synonymous with “semiconductors.” Most semiconductor devices are made from silicon, although other materials such as gallium arsenide can also be used. Semiconductors can be divided into two main groups: integrated circuits (ICs) and discrete. Integrated circuits consist of many active and passive elements that are fabricated and connected together in a single chip. Discrete devices consist of a single switching element.

There are many types of discrete. These include diodes, rectifiers, transistors and optoelectronics. Optoelectronics are devices that produce light and can be used for displays, or to transmit and receive data over fiber optic cables.

Integrated circuits can be further classified into digital or analog devices. Digital ICs store and process information in binary numbers or bits. They perform arithmetical operations or logical functions by manipulating binary signals (on / off switches).

By contrast, analog devices deal with continuous scales in which each point merges imperceptibly into the next. These devices measure or amplify analog signals or convert analog signals to digital. The largest subcategory of analog devices are special consumer circuits, which are customized ICs for specific consumer applications.

Digital devices can be manufactured by two different processes. The first is metal oxide silicon or MOS, the other is digital bipolar. Traditionally, digital bipolar devices have been faster than MOS devices but require more power and generate more heat. Modern MOS processes are making this distinction obsolete, however. Both MOS and digital bipolar manufacturing processes can be used to create logic parts to perform arithmetic operations as well as memory devices that store data.

A number of different products fall under the memory category. Volatile memory products such as DRAMs (Dynamic Random Access Memory) can be used in temporary applications such as word processing documents. These need to be refreshed or saved because they lose the information once the power is turned off. SRAMs (Static Random Access Memory), a read/write memory, is another type of volatile memory.

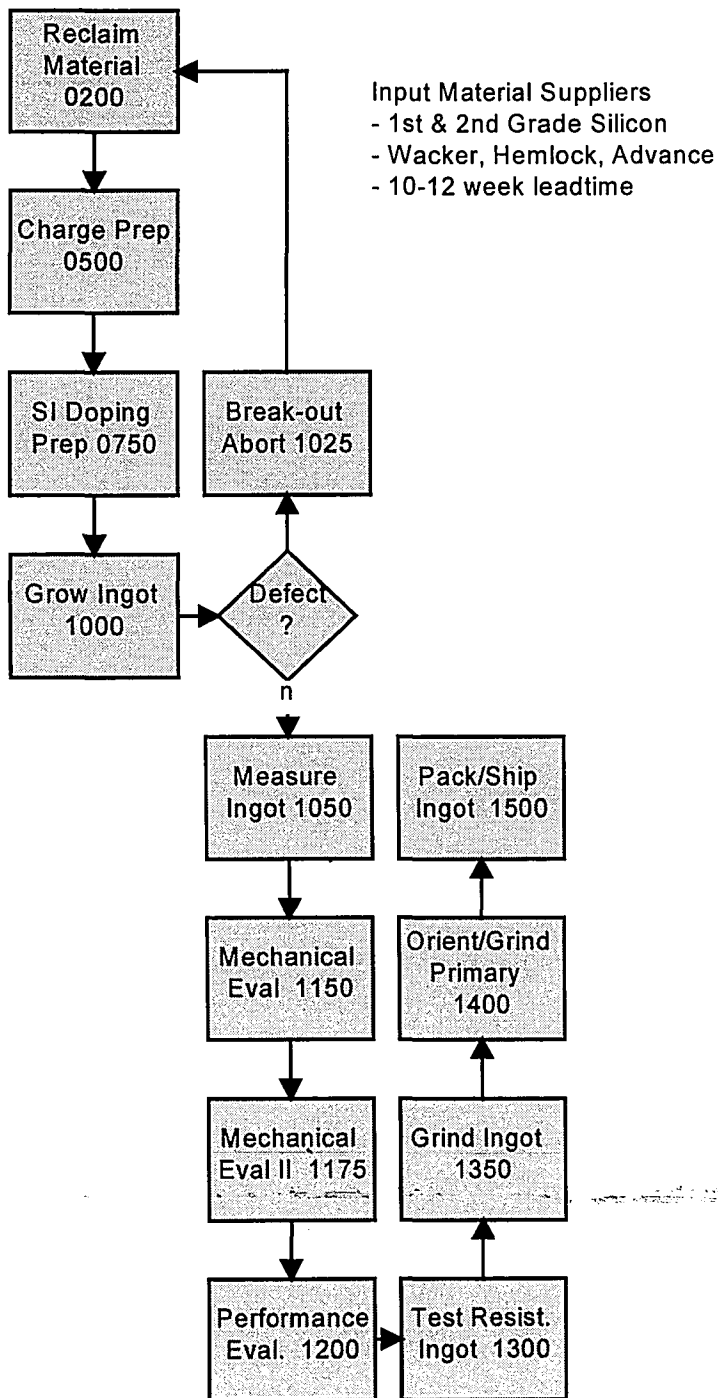
Non-volatile memory products retain information even after the power is turned off. These include ROM (Read Only Memory), EPROM (Erasable Programmable ROM), FLASH Memory.

MOS Micro devices include microprocessors, microcontrollers and microperipherals. Microprocessors are the “brains” of computers. A 32 bit microprocessor, typically used in today’s personal computers, processes 32 bits of information at one time. Microcontrollers have microprocessors as well as memory integrated on a single chip – a computer on a chip. A Digital Signal Processor (DSP) is a type of microcontroller. Microperipheral devices accompany microprocessors to handle a related function in a computer such as graphics.

MOS Logic chips handle the mathematical treatment of formal logic by translating AND, OR and NOT functions into a switching circuit or gate. The basic logic functions obtained from gate circuits form the foundation of computing machines. This category includes application-specific ICs (ASICs) such as gate arrays, standard cells and programmable logic devices. ASICs are semi-custom devices, with a customer specifying customized connections of standard elements.

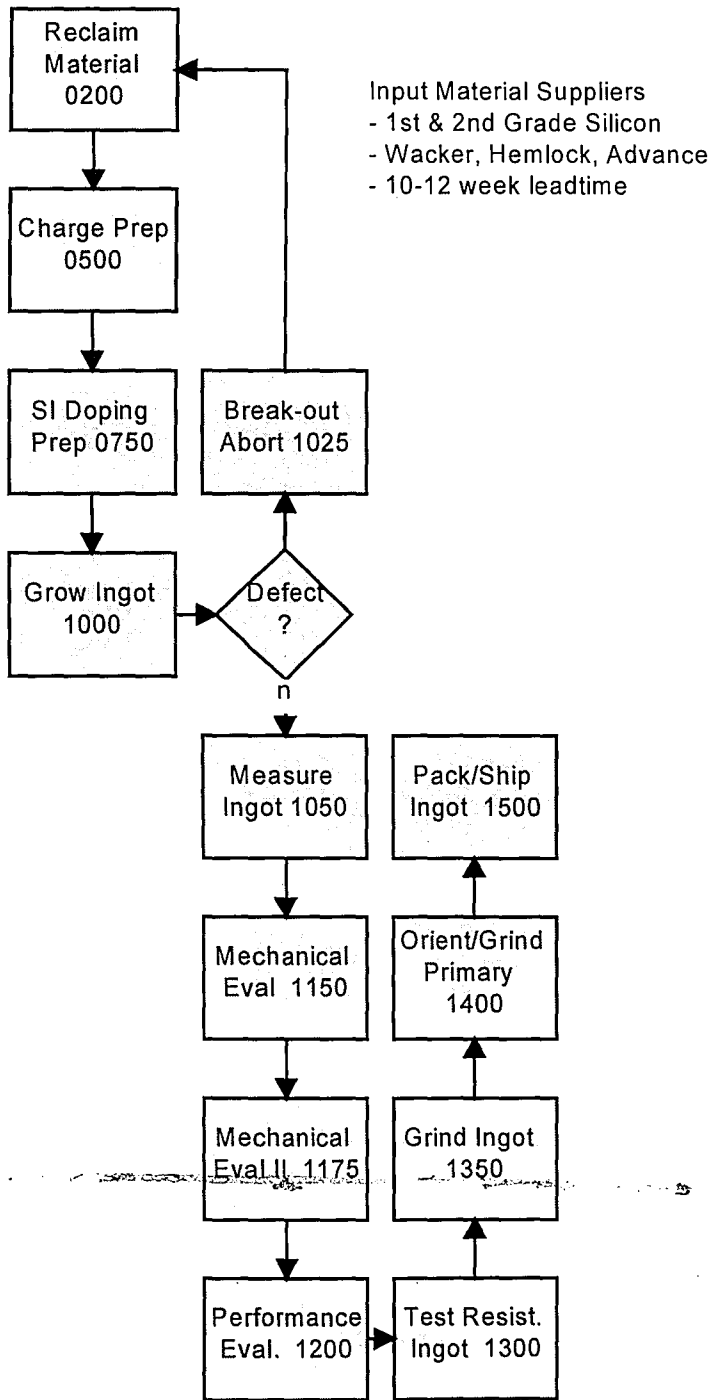
Appendix 2: Silicon Materials Manufacturing Process

INGOT GROWING



Appendix 2: Silicon Materials Manufacturing Process

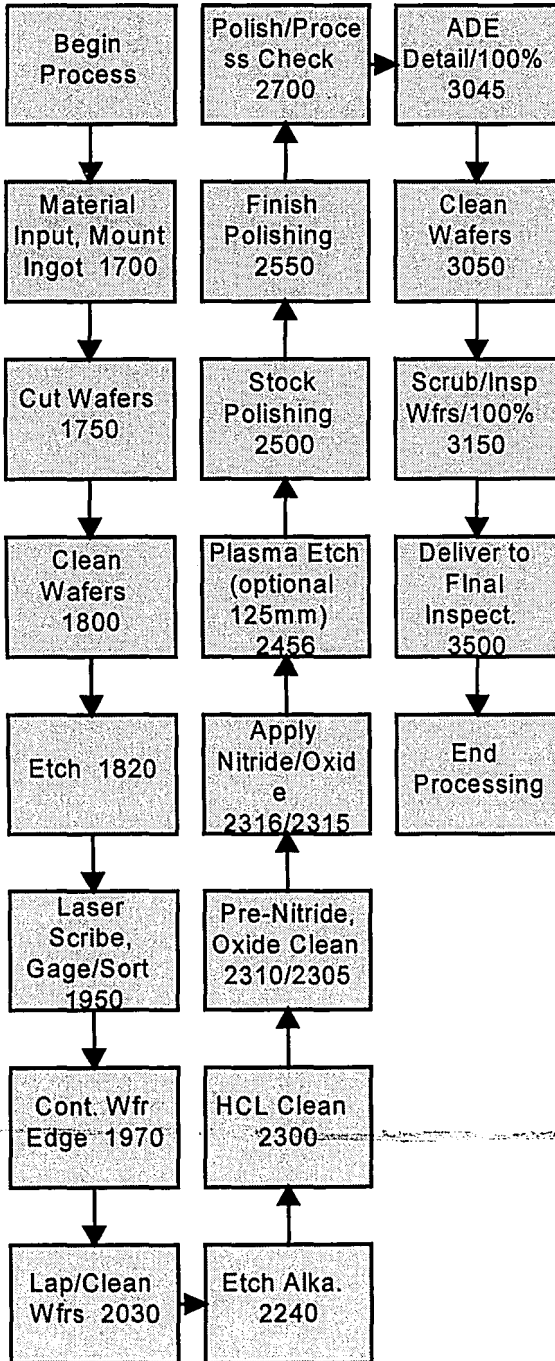
INGOT GROWING



Appendix 2: Silicon Materials Manufacturing Process

SAWING AND POLISHING

SILICON MATERIALS: (2) SAWING & POLISHING

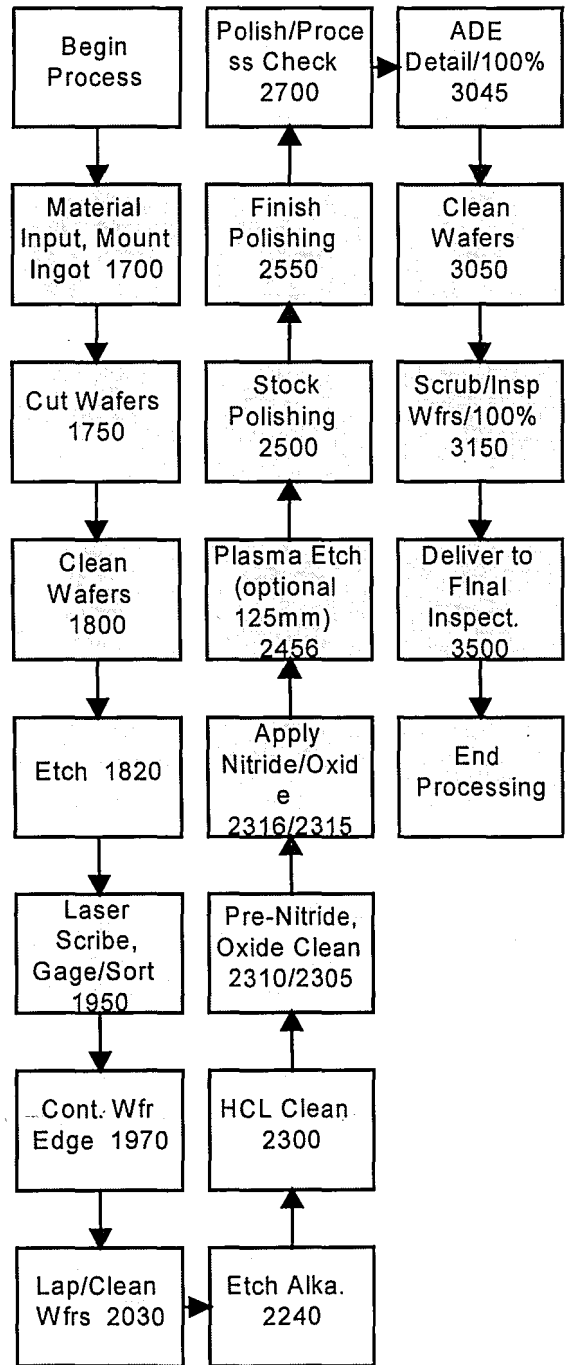


Linkage with Wafer Fabrication:
 Dielectric, Sawing and Polishing changes between steps 1750 and 3500 lead to higher grade (flatter) wafers. Changes include saw orientation, new polishing equipment, removing scribed number on wafer surface, checks & measurements of wafer edges, tightening specs on existing materials
 Benefits in wafer fabrication:
 Improved wafer fab yields, lower per chip manufacturing costs, higher available fab capacity, and revenues increase
 Net result - **Higher profits**

Appendix 2: Silicon Materials Manufacturing Process

SAWING AND POLISHING

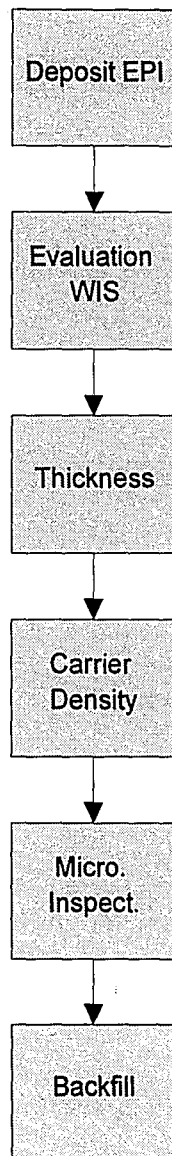
SILICON MATERIALS: (2) SAWING & POLISHING



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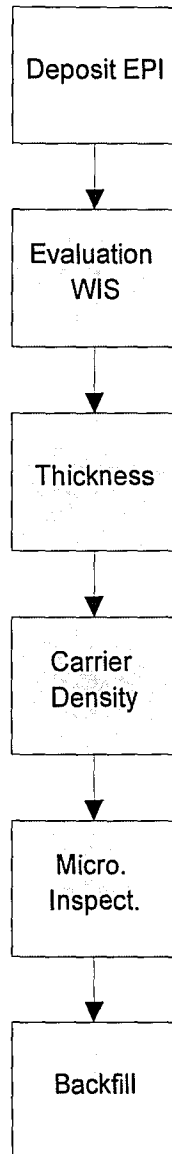
Appendix 2: Silicon Materials Manufacturing Process

INSPECTION AND TEST

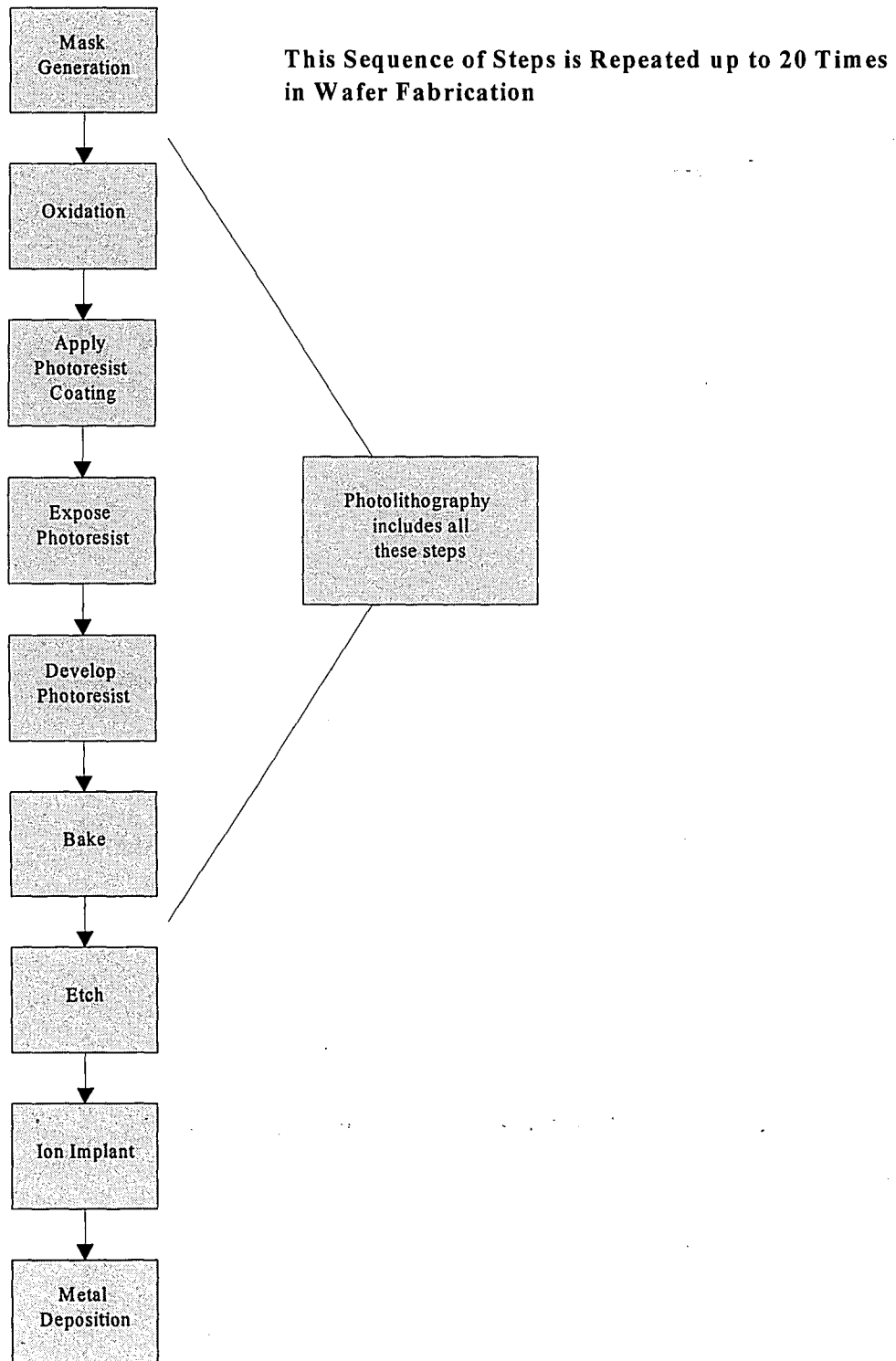


Appendix 2: Silicon Materials Manufacturing Process

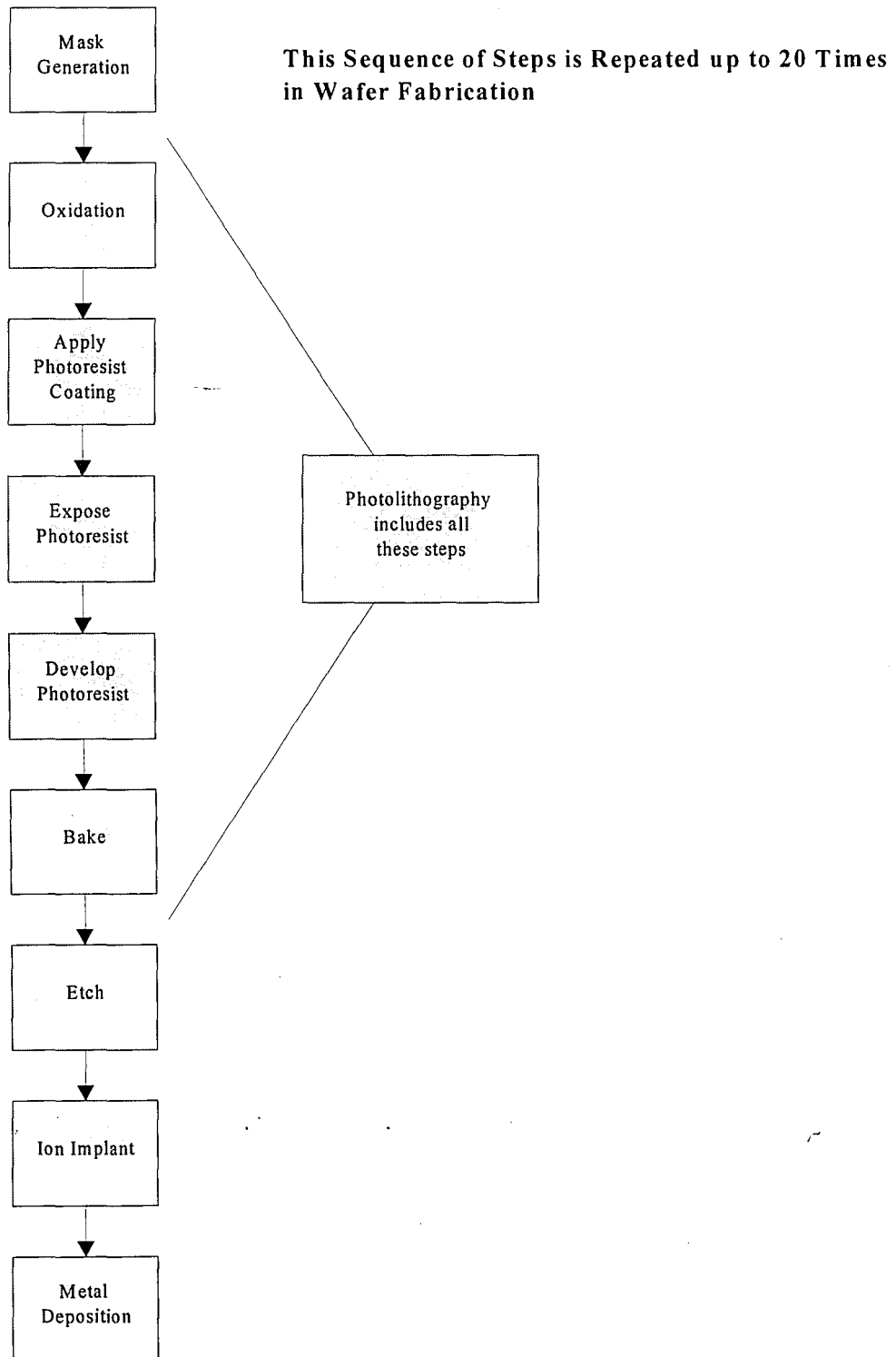
INSPECTION AND TEST



APPENDIX 3: WAFER FABRICATION PROCESS FLOWCHART



APPENDIX 3: WAFER FABRICATION PROCESS FLOWCHART



BRIEF BIOGRAPHY

Yuan Ling Chou was born in the Republic of Singapore on March 10, 1966, to Tai-Yun Chou and Tzen-Min Lee. Ling graduated from Cornell University with a B.S. in Industrial Engineering and Operations Research in 1987, and an M. Eng. In Industrial Engineering and Operations Research in 1988. From 1988 to 1990, she worked as a hardware quality engineer at Disk Memory Division, Hewlett-Packard Co., Boise, Idaho. She transferred into a manufacturing process design position in 1990. In 1993, she moved to Allentown, Pennsylvania to work at (then) AT&T Microelectronics as an ASSP (Application Specific Standard Products) product marketing engineer. In 1994, she started her M.S. in Management of Technology and also a new position as ASIC Product Planner in AT&T's Allentown facility. Ling currently supports Data Networking customers in the Integrated Systems Business of Integrated Circuits Division, Microelectronics Group, Lucent Technologies. She graduates from Lehigh University with an M.S. in Management of Technology in January 1997.

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