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A study of interface charges and mechanisms of subthreshold conduction in 4H silicon carbide (SiC) recessed-gate static induction transistors (RGSITs)

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A Study of Interface Charges and the Mechanisms of Subthreshold Conduction in 4H Silicon Carbide (SiC) Recessed-Gate Static Induction Transistors (RGSITs)

By

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Chairman of Department

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I would like to dedicate this thesis to my parents, Authur and Karen Fuerherm, for their guidance and continued support.

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Abstract

The Silicon Carbide (SiC) Static Induction Transistor (SIT) is based on the original SIT concept first proposed by J. Nishizawa in 1950. The SIT structure provides high breakdown voltage, high current density and high frequency operation while remaining thermally stable. SiC has a high breakdown field (10X), increased thermal conductivity (4X), increased saturation drift velocity (2X), and wide bandgap compared with comparable Silicon structures. These characteristics have made SiC SIT devices ideal for high power and high frequency applications.

Although the SIT offers the above-mentioned advantages, a reliability issue arises if charges are present in the overlying oxide in the 'shoulder' region between the source 'post' and the metallic gate electrode. The presence of charges in this region, if not controlled, will modulate the barrier height of the saddle point in the channel region which controls the current for a specific drain voltage, thereby reducing the holding voltage for a fixed OFF current specification. In this thesis, the influence of the oxide charge in the 'shoulder' oxide region on the operation of a 4H-SiC recessed-gate SIT (RGSIT) has been studied using Silvaco's Atlas software program. The effect of interface charge on the 'shoulder' region is seen to change the effective gate bias of the device. Therefore, RGSIT with positive/negative interface charge is expected to have its I-V characteristics shift to the left/right due to barrier height lowering/increase.

Additionally, the subthreshold operation of the SIT has been analyzed assuming thermionic emission of carriers flowing over a potential barrier located in the 'intrinsic'

region. The barrier heights, effective channel widths, and drain currents are calculated using a superposition analysis of the Poisson and Laplace components of the electrostatic potential in the 'intrinsic' region of the SIT. For a given gate-to-source bias, the analysis shows a barrier height decrease for an increasing drain-to-source bias. Additionally, the effective channel width increase due to a drain-to-source bias increase is shown to be minimal. Current due to thermionic emission is empirically fitted to experimental data of fabricated SiC RGSIT devices using the theoretical results of the barrier height and effective channel width.

Chapter 1
Introduction

1.1 Review of SiC

SiC is the most prominent of a family of materials that exhibit a one-dimensional polymorphism. The SiC polytypes are differentiated by the stacking sequence of the tetrahedrally bonded Si-C bilayers. While the individual bond lengths and local atomic environments are identical, the overall symmetry of the crystal is determined by the stacking periodicity. Each SiC bilayer, while maintaining the tetrahedral bonding scheme of the crystal, can be situated in one of three possible positions with respect to the lattice. The three most commonly known polytypes are 6H, 4H, and 3C. These different polytypes have a wide range of physical properties. The bandgaps differ among the polytypes ranging from 2.3 eV for 3C-SiC to 3.26 eV in 4H-SiC. Amongst these polytypes, 4H is most commonly used because of its superior electronic properties. A comparison of important semiconductor properties has been summarized in Table 1.1. It can be seen that SiC has much more promise in the area of high power and high frequency applications over that of Si. [1]

Property	Si	6H-SiC	4H-SiC	3C-SiC
Bandgap (eV) at 300K	1.12	3.0	3.26	2.3
Electron mobility RT, cm^2/Vs	1400	400 (// c-axis) 85 ($\perp$ c-axis)	960 (// c-axis) 800 ($\perp$ c-axis)	800
Breakdown Field (E_b), MV/cm	0.3	3	3	2
Thermal conductivity (c_T), W/cm	1.5	4.9	4.9	5
Saturation drift velocity (v_{sat}), 10^7 cm/s	1	2.0	2.0	2.0
Dielectric constant, k_s	11.9	9.7	9.7	9.7
Intrinsic carrier concentration, n_i (cm^{-3})	$1.45x10^{10}$	$2.3x10^{-6}$	$8.2x10^{-9}$	6.9

Table 1.1: Comparison of semiconductor properties for SiC and Si [2]

One major advantage that SiC enjoys over other wide band-gap semiconductors is an established, commercially available, process for the growth of high quality substrate material. Additionally, suitable dopants for SiC have been established; Nitrogen being the most popular n-type dopant, with Aluminum and Boron used for p-type dopants. Nitrogen acts as a donor level approximately 100 meV below the conduction band. Aluminum acts as an acceptor level at about 220 meV above the valence band. Boron has two acceptor levels at 330 and 700 meV above the valence band [3]. Diffusing dopants into SiC is extremely difficult, making implantation the sole way to introduce dopants for well and junction formation. Ion-implantation at room temperature tends to amorphize the SiC and limit ion-activation [4]. Therefore, implantation is performed at elevated temperatures near 700 °C with a subsequent anneal at near 1600 °C. Another feature that sets SiC apart from that of other wide band-gap semiconductors is its ability

to form a stable silicon oxide (SiO_2) layer when thermally oxidized as is the case of Si. Additionally, the large band-gap of SiC reduces minority-carrier generation rates and dramatically increases charge retention in MOS devices and would inherently increase the life-span of similar SiC MOS devices.

Present difficulties with SiC include a low diffusivity constant of ions, as previously mentioned, which may result in low surface dopant concentrations and increased contact resistances. Another important concern is the low mobility values seen in SiC inversion layers primarily due to high interface trap densities and surface roughness. It is obvious that progress is required in the fabrication of high quality gate oxides with low concentrations of fixed oxide charge and interface trap densities. The overcoming of these obstacles is very important for the fabrication of high speed, high power devices.

1.2 Historical Review of SIT

Operation concepts of the field effect transistor (FET) were offered by Lilienfeld in 1930 and 1933 [5],[6]. In 1952, Shockley provided a theoretical analysis of a FET, which provided much of the understanding of its operation. However, an ambiguity remained since after saturation, current remained constant against theoretical expectations. Nishizawa proposed the constant current under saturation to be a result of negative feedback of transconductance through the series channel resistance. Series channel resistance could be decreased and its effect minimized by the shortening of the channel length [5], [7], [8]. The decrease of the channel length and reduction of the series channel resistance produced output characteristics that are non-saturating or

"triode-like"; resembling the output of the triode vacuum tube or present-day short channel MESFETs and JFETs. In 1950, Nishizawa formulated the concept of a vertical device with short channel length, originally called the "analog-type transistor," now known as the SIT [5]. The vertical structure provides high breakdown voltage and high current density between the source and drain terminals. The SIT is a majority carrier device that eliminates speed dependence on minority carrier storage charge as seen in IGBT devices [9]. Electrons reach saturation velocity at high electric fields, allowing the devices to operate at high frequencies and high voltage levels. The SIT is also thermally stable because carrier mobility decreases with increasing temperature, eliminating thermal runaway.

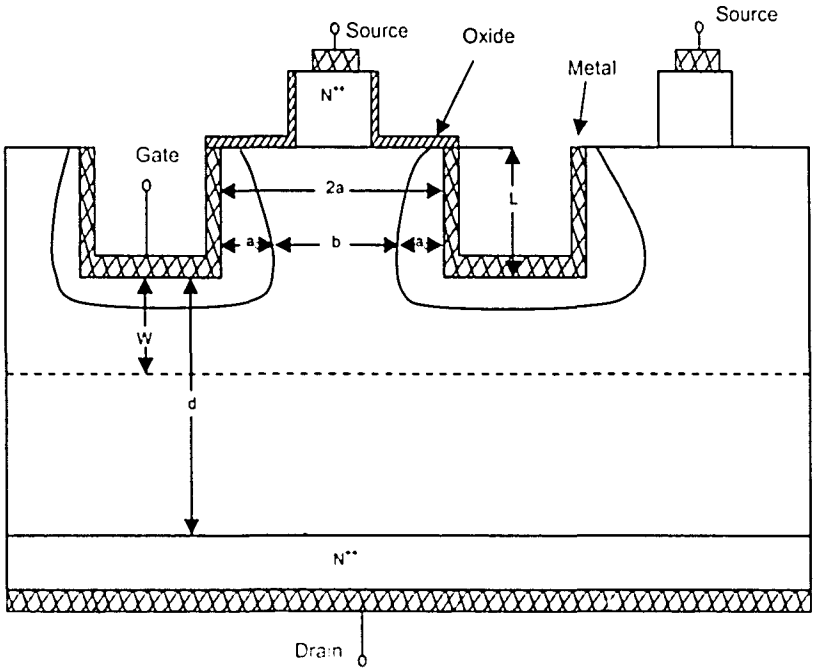

Figure 1.1 SIT structure showing cross-section dimensions [10]

The design of the SIT structure is shown in Fig 1.1 [10]. This particular structure is known as the recessed-gate SIT (RGSIT), with Schottky gates positioned in the trenches. The SIT is a vertical structure comprised of finger-like protrusions having the source contact at the top of the fingers, gate contacts surrounding the fingers and the drain contact resides on the underside of the structure. To make a power device, many of these fingers are connected in parallel to obtain the desired periphery. The device channel, otherwise called the channel width, is defined by the dimension of $2a$. A depletion region defined as a_0 forms in the channel semiconductor due to the built in potential, V_{bi} of the gate. The distance between the two depletion regions in the channel is defined as b. The distance from the bottom of the n^{++} source to the bottom of the recessed-gate/trench is defined by the dimension of L. The distance from the bottom of the recessed-gate/trench to the n^{++} drain is defined by the dimension of d. The distance between the bottom of the recessed-gate/trench to the end of the depletion region formed by the gate-to-drain reverse bias is defined as W.

Other arrangements of the gate electrode are possible. The planar SIT has p-n junctions as the gate electrode [5],[11],[12]. This was the configuration that was originally used in SITs when they were realized in Si. However, because of deep ion implantation difficulties, RGSIT structures are favored in SiC [13].

Chapter 2

Operation of the Static Induction Transistor (SIT)

2.1 Modes of Operation

The output I-V characteristics of the SIT are divided roughly into 4 different regions of operation as shown in Fig. 2.1. The SIT exhibits (A) ohmic conduction for a non-fully depleted channel at small drain and gate bias, (B) exponential current due to thermionic emission for a fully depleted channel and low drain bias, (C) space charge limited conduction (SCLC) at high current densities, and (D) velocity saturated space charge limited conduction (SCLC with v_{sat}) at high current densities with electrons approaching velocity saturation [14]. For each of these regions, approximate analytical formulas can be written. These formulas are useful to see a relationship between terminal voltage and current, but lacks accuracy. In practice, the total current may have overlapping contributions from each of these regions.

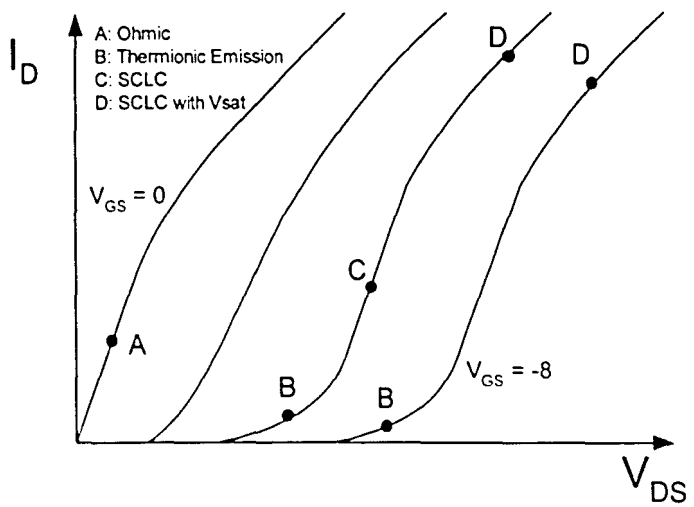

Fig. 2.1 Different current conduction mechanisms in a Static Induction Transistor (SIT)

2.1.1 Ohmic Conduction

At zero gate and drain bias, the channel is depleted to a width a_0 from each gate due to the built-in potential V_{bi}. The challenge of computing the ohmic conduction is defining the extent and shape of the depletion region around the Schottky gates. A simple approximation is to assume the depletion width can be computed by the one-dimensional depletion approximation and the depletion width itself is in the shape of a rectangular box as shown in Fig 2.2 [15]. This leaves a neutral channel of thickness $b=2(a-a_0)$ where ohmic conduction can occur.

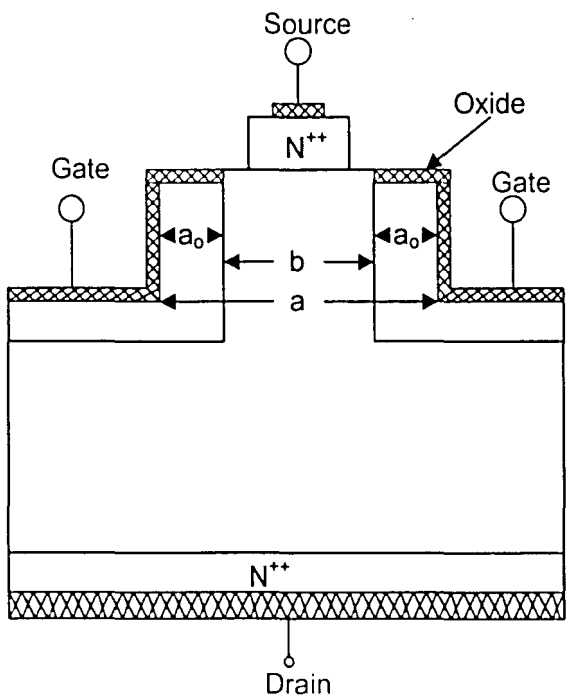

Figure 2.2 SIT structure showing rectangular depletion width [15]

Using the following equations, the intrinsic carrier density n_i, built-in potential V_{bi}, and initial depletion width a_0 can be approximated:

$$n_i = \sqrt{N_c N_v}\exp\left\{-\frac{E_G}{2kT}\right\} \tag{2.1}$$

$$qV_{bi} = q\phi_B - \left[\frac{E_g}{2} - kT\ln\left(\frac{N_D}{n_i}\right)\right] \tag{2.2}$$

$$a_0 = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}} \tag{2.3}$$

where N_c and N_v are the effective density of states in the conduction and valence bands. E_G is the bandgap of 4H-SiC, k is Boltzmann's constant, and T is absolute temperature. In Eqn 2.2 the barrier height, ϕ_B, is defined as the difference between the metal work function and the electron affinity of the semiconductor, $\phi_M - \chi$, and N_D is the doping density of the channel. The dielectric constant of 4H-SiC is ε_s and q is the electron charge in Eqn 2.3. The application of negative bias on the gate terminal relative to source bias will increase the depletion width as shown in Eqn 2.4.

$$a' = \sqrt{\frac{2\varepsilon_s\left(V_{bi} + |V_G|\right)}{qN_D}} \tag{2.4}$$

$$b = 2(a - a') \tag{2.5}$$

The resistance between source and drain can now be easily computed assuming the current flow is within rectangular box with width b and length $d + L$. The drain current due to ohmic conduction can be written as:

$$I_D = \frac{qA_c N_D \mu_n V_D}{L + d} \tag{2.6}$$

where *Ac* is the cross-sectional area for the current flow. If the gate-to-drain bias, V_{GD}, becomes more negative, then the depletion regions expand and the cross-sectional area narrows, which decreases the current analogous to a short channel JFET or MESFET.

2.1.2 Thermionic Emission

For a specific gate-to-drain bias, V_{GD}, the channel becomes fully depleted and a potential barrier forms in the channel to inhibit electron flow from source to drain. The potential barrier, shown in Fig 2.3, has shape of a saddle with its minimum value, ϕ_{B0}, located halfway between the two gate electrodes, y = 0. A majority of the current will flow through the small cross section in the center of the channel where the barrier minimum and saddle point, is located. The current flow in this mode is due to thermionic electron emission over the potential barrier and given by the expression [5], [7]

$$I_D = A_C A^{**} T^2 \exp\left\{-\frac{q}{kT}\Phi_{B0}\right\} \tag{2.7}$$

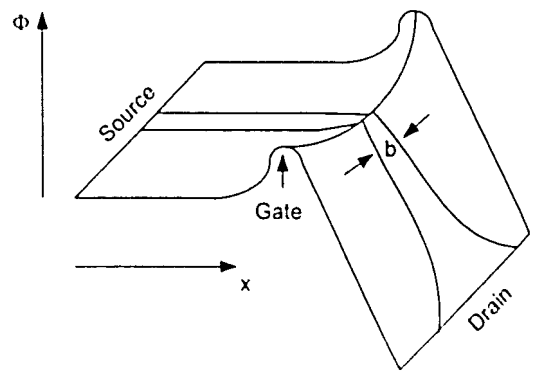

Fig. 2.3 Potential Saddle in SIT

where A_C, A^{**}, and T in Eqn. 2.7 are the cross section, Richardson's constant, and absolute temperature, respectively. Dimension b may vary in the SIT as shown in Fig. 2.3, making the calculation of the cross-sectional area difficult. We will define in Chapter 5, a dimension b_{eff}, which represents an effective width of the conducting channel.

The height of the barrier depends upon the two dimensional capacitive coupling (*static induction*) between the two gates, source and drain electrodes shown in Fig 2.4. The application of the drain bias results in the reduction of the barrier height, drain induced barrier lowering (DIBL), causing an increase of electron flow from source to drain through the means of thermionic emission.

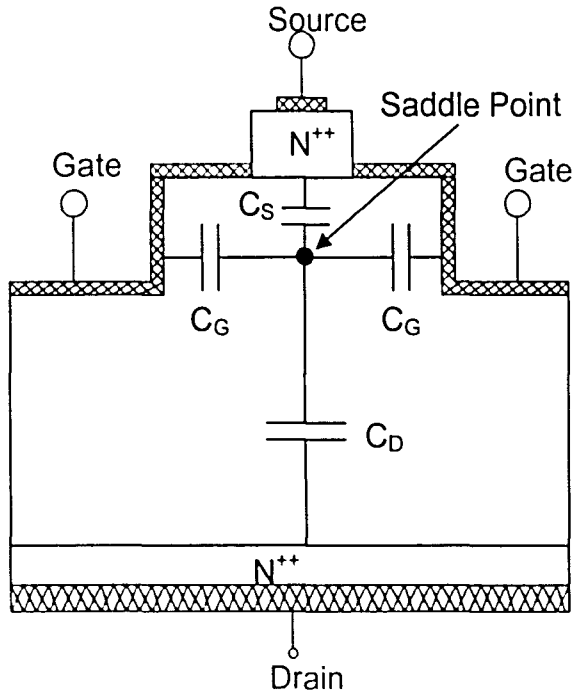

Fig. 2.4 The coupling capacitance determine the saddle point potential when a Static Induction Transistor (SIT) is completely depleted under bias voltages

The DIBL coefficient of the drain voltage can be found using a static charge analysis for a fully depleted structure. Eqn. 2.8 is the sum of charge to the various electrodes using the appropriate capacitances:

$$C_S(V_S - V_X) + 2C_G(V_G - V_X) + C_D(V_D - V_X) = 0 \tag{2.8}$$

where:

$$C_S = \frac{\varepsilon_S}{L/2} bp \tag{2.8.1}$$

$$C_D = \frac{\varepsilon_S}{d + L/2} bp \tag{2.8.2}$$

$$C_G = \frac{\varepsilon_S}{a} Lp\gamma \tag{2.8.3}$$

where p is the device periphery, γ is a field-enhancement factor due to electric field crowding near the edge of the gate electrodes, V_S is the source voltage, V_G is the gate voltage, V_D is drain voltage, and V_X is the saddle point potential. The DIBL coefficient can be obtained as follows:

$$-C_S \partial V_X - 2C_G \partial V_X + C_D \partial V_D - C_D \partial V_X = 0 \tag{2.9}$$

$$\alpha \equiv \frac{\partial V_X}{\partial V_D} = \frac{C_D}{C_S + C_D + 2C_G} = \frac{1}{2(1 + d/L) + \mu} \tag{2.10}$$

where:

$$\mu \equiv \frac{\partial V_D}{\partial V_G}\Big|_{V_S, V_X = \text{constant}} = \frac{2C_G}{C_D} = \frac{2L(d + L/2)\gamma}{ab} \tag{2.10.1}$$

where α is the drain-induced barrier lowering (DIBL) coefficient and μ is the voltage gain of the SIT device. The current flow, due to thermionic emission shown in Eqn. 2.7, can be re-written as

$$I_D = A_C A^{**} T^2 \exp\left\{-\frac{q}{kT}(\Phi_0 - \alpha V_D)\right\} \tag{2.11}$$

where Φ_0 is the barrier height at zero drain bias and α is the DIBL coefficient given approximately by $\alpha \approx 1/\mu$.

2.1.3 Space Charge Limited Conduction (SCLC)

As the drain bias is increased, the barrier induced by the gate electrodes is completely lowered ($\alpha V_D = \Phi_0$) and the current density in the cross-section becomes high. When the carrier concentration becomes higher than the doping density, n>>N_D^+, the current becomes SCLC. Assuming low-field transport, SCLC can be analyzed with the following Poisson's and current drift equations (assume steady state $\frac{\partial n}{\partial t} = 0$):

$$\frac{\partial^2 V}{\partial x^2} = \frac{-q\left(N_D^+ - n\right)}{\varepsilon_s} = -\frac{\partial \mathrm{E}}{\partial x} \tag{2.11}$$

$$J = -qnv \tag{2.12}$$

$$v = \mu_n \mathrm{E} \tag{2.13}$$

where v is the electron velocity (assumed low-field transport) and μ_n is the electron mobility in 4H-SiC.

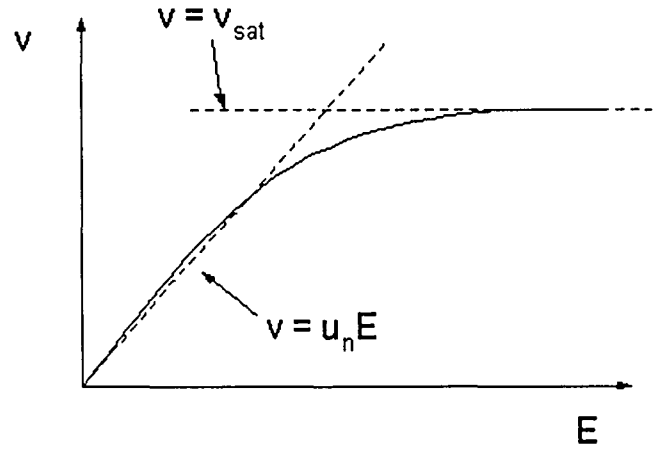

Fig. 2.5 Analysis of electron velocity in high/low field transport conditions

The SCLC regime I-V characteristics may be expressed by the following equation:

$$I_D = \frac{9}{8} A_c \mu_n \varepsilon_s \frac{V_D^2}{(L+W)^3} \tag{2.14}$$

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} + |V_{GD}|)}{qN_D}} \tag{2.14.1}$$

where W is the depletion width. Note, in Eqn. 2.14.1, as the reverse potential V_{GD} is increased, W is increased and when $W = d$, the n-region of the SIT is fully-depleted.

2.1.4 Velocity Saturated Space Charge Limited Conduction (SCLC)

As the drain bias is increased further, the electrons begin to reach their saturated drift velocity. This occurs when high electric fields span the SIT device. Assuming the carriers move with saturated drift velocity, v_{sat}, throughout the channel, the SCLC is given by

$$I_D = 2A_c\varepsilon_s v_{sat}\frac{V_D}{(L+d)^2} \tag{2.15}$$

Here W has been replaced with d, assuming the entire SIT structure has been depleted. The difference between the low and high field conditions can be determined by the current dependence on thickness of the transport region, d.

2.2 Small Signal Output Resistance, Voltage Gain, and g_m

Assuming a velocity saturated SCLC, the output resistance, r_0, voltage gain, μ, and transconductance, g_m, are related by the following expressions:

$$r_0 = \frac{\partial V_D}{\partial I_D} = \frac{(L+d)^2}{2A_C\varepsilon_S v_{sat}} \tag{2.16}$$

$$\mu \equiv \frac{\partial V_D}{\partial V_G} = \frac{2L(d+L/2)\gamma}{ab} \tag{2.17}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial V_D/\partial V_G}{\partial V_D/\partial I_D} = \frac{\mu}{r_0} \tag{2.18}$$

where the voltage gain, μ, is formulated using the capacitive coupling (Eqn. 2.10.1) and the output resistance, r_0, is formulated using the velocity saturated SCLC current equation (Eqn. 2.15). The transconductance, g_m, of the device can now be determined from Eqns. 2.16, 2.17, and 2.18

$$g_m = \frac{4L\varepsilon_S v_{sat}(d + L/2)p\gamma}{a(d+L)^2} \approx \frac{4L\varepsilon_S v_{sat} p\gamma}{a(d+L)} \tag{2.19}$$

From Eqns. 2.17 and 2.19, the voltage gain and transconductance may be improved by increasing the gate length, L, rather than decreasing the finger dimension a because of lithography and yield considerations. Additionally, device dimension d may be increased to improve the voltage gain, but at the expense of the transconductance and the DIBL coefficient (Eqn. 2.10).

2.3 Breakdown Voltage

As the reverse bias V_{GD} increases, the n-type 4H-SiC immediately under the Schottky gate depletes towards the drain electrode. When the entire drain region is depleted the electric field at the surface (y`=0) is

$$E_S = \frac{qN_D d}{\varepsilon_S} \tag{2.20}$$

which represents a punch-through situation. As the drain bias increases, the surface field is raised towards a critical field value, E_C. Normally, the surface breakdown at the outer

edges will take place before the field in the interior of the gate reaches the critical value. The ideal breakdown voltage, V_B, is given by the area under the trapezoidal electric field distribution shown in Fig. 2.7,

$$V_B = E_C d - \frac{qN_D d}{2\varepsilon_S} \tag{2.21}$$

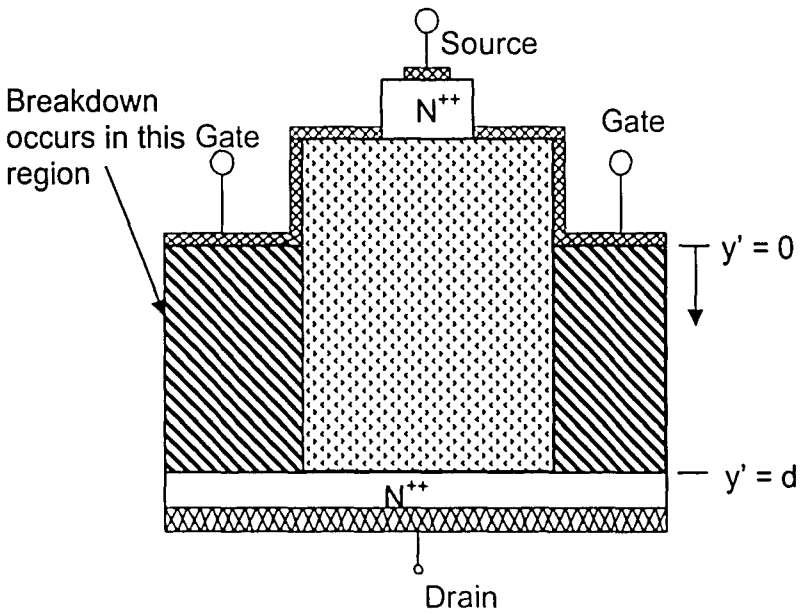

Fig. 2.6 Breakdown diagram of the SIT structure

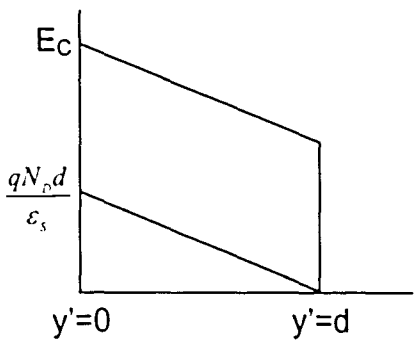

Fig. 2.7 Trapezoidal electric-field distribution

Eqn. 2.21 is valid for the punch-through case only. If the doping density, N_D, or the dimension d is high, a non-punch-through condition may occur as shown in Fig. 2.8. This being the case, the ideal breakdown voltage under these conditions is the area of the triangular electric field distribution:

$$V_B = \frac{E_C^2 \varepsilon_S}{2qN_D} \tag{2.22}$$

The condition for punch-through is given as:

$$E_C > \frac{qN_D d}{\varepsilon_S} \tag{2.23}$$

If the relationship of Eqn. 2.23 is valid, then the ideal punch-through expression for V_B given in Eqn 2.21 should be used. Otherwise, Eqn. 2.22 is appropriate.

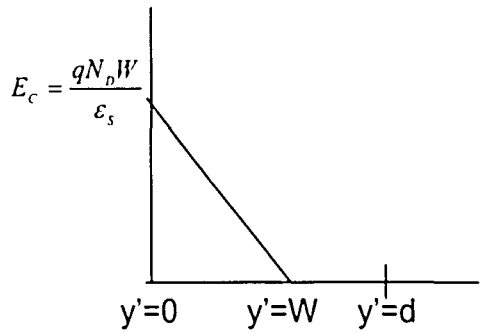

Fig. 2.7 Electric Field distribution for the Trapezoidal electric-field distribution in the non-punch-through case

2.4 Additional SIT Concepts

The basic theory of the SIT has been discussed in this chapter. The four different modes of SIT conduction have been described. Expressions for voltage gain, transconductance, output resistance, and breakdown voltage have been developed. There are trade-offs that occur between device performances and device dimensions and doping. Although power, RF performance, and thermal issues have not been considered in this thesis, the SIT has the capability of providing a large signal power gain at high frequencies, including S and X-bands. The maximum total power and operating frequency is determined by the scaling of the device. Thermally, the SIT is like most power devices where the heat is dissipated to a heat sink usually attached to the back of the wafer. As in most devices, there exists a maximum internal temperature at which the device can operate. In this sense, the SiC SIT has advantages due to its large energy band gap and thermal conductivity in comparison with Silicon power devices. Heat generation can be limited through pulse operations in which the device is allowed to cool between pulses [15].

Chapter 3

Software Modeling of the Recessed Gate Static Induction Transistor (RGSIT) in SILVACO ATLAS

The creation of computer-aided design (CAD) software to model and predict the physical behavior of semiconductor devices, both electrically and mechanically, has been of great assistance to engineers and scientists. The use of CAD software is different from empirical modeling (the obtaining of analytical formulae that approximates existing data). A physically-based simulation is an alternative to experiments as a source of data. Physical-based simulation has become important because it is frequently quicker and less expensive than performing actual experiments and may provide information and insight - quantities otherwise difficult or impossible to obtain through measurements [16]. As shown in the sections to follow, insight into the basic internal mechanisms associated with device operation can be explored easily using CAD software analysis. In this thesis, SILVACO software ATLAS has been used to model and simulate the device characteristics of the RGSIT.

3.1 Modeling the RGSIT Device Structure

When running a simulation with a simulator, such as ATLAS, an existing device structure can be read in from a file. In this thesis, a RGSIT device structure was created in a previous ATLAS program, which defined the dimensions and materials used in the device. The dimensions of d, L, and a used for the RGSIT device are 3.65μm, 1μm, and

0.75μm, respectively. Other dimensions, such as the N^{++} source length, N^{++} source height, and half-gate length are 0.7μm, 0.35μm, and 0.6μm, respectively. Additionally, a more lightly doped epitaxial layer, relative to the channel doping, has been incorporated in this RGSIT structure 0.35μm under the gate electrode. The N^- doping of the epitaxial layer, N doping of the channel, and N^{++} doping of the source and drain regions are set as $4x10^{15}$ cm^{-3}, $1.35x10^{16}$ cm^{-3}, and $1x10^{19}$ cm^{-3}, respectively. The drain contact is set as the entire under area of the SIT device. The gate is set as a square contact (for programming ease) surrounding the structure and the source is set at the appropriate spacing on the top finger. An oxide overcoat is placed in all areas not occupied by the metal and SiC. The various dimensions and doping levels can be seen in Fig. 3.1.

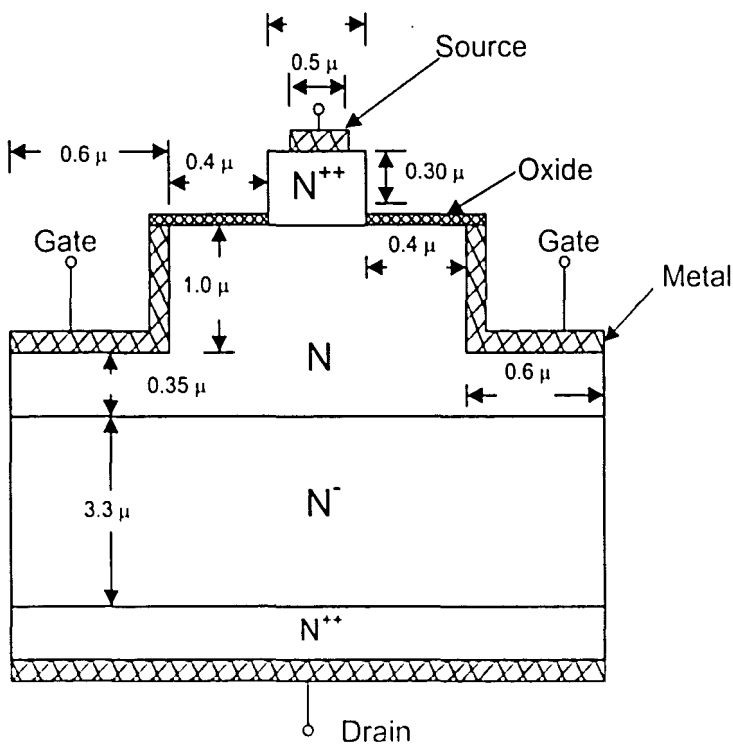

Fig. 3.1 Model dimensions used in Silvaco's ATLAS software

Using appropriate mesh point settings (calculation points), the RGSIT device is modeled into ATLAS as shown in Fig. 3.2.

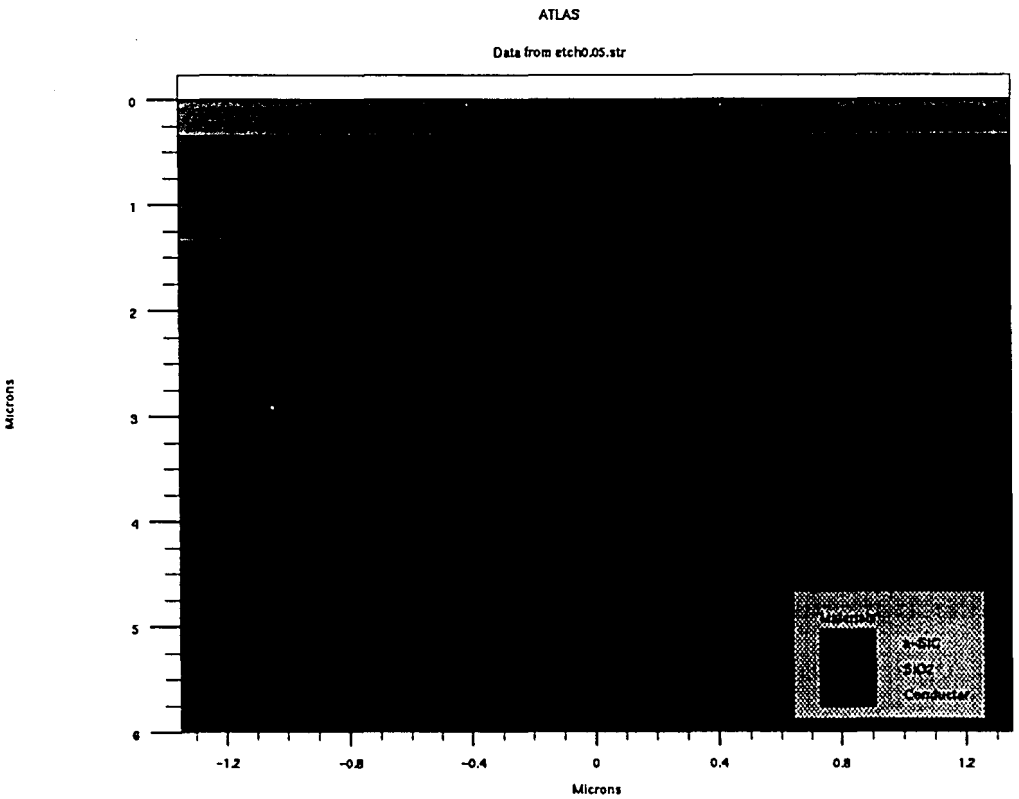

Fig. 3.2 Example of a RGSIT structure modeled in Silvaco's ATLAS software

Table 3.1 Physical parameters of the device used in the simulation of Fig. 3.2

Parameter Definition	Notation	Value	Units
Bottom of gate to drain	d	3.65	μm
Channel length	L	1	μm
Channel half-width	a	0.75	μm
Source/Drain doping	N^{++}	$1x10^{19}$	cm^{-3}
Channel doping	N	$1.35x10^{16}$	cm^{-3}
Epi-layer doping	N^{-}	$4x10^{15}$	cm^{-3}

3.2 Simulation of the RGSIT

Once an acceptable model of the SIT device is constructed, simulation and verification of the model commences. Additional data required for the 4H-SiC material is given by the following parameters: the bandgap, E_G, electron affinity, χ_s, electron mobility, μ_n, electron velocity saturation, v_s, work function, ϕ_m, and trap energy level, E_T, which are set at 3.25eV, 3.65eV, 350 $cm^2/(V\ s)$, $2.2x10^7$ cm/s, 5.05eV, and 0.5eV below the conduction band, respectively. Using varying gate voltages and sweeping the drain, the I-V characteristics of the device are analyzed. Additionally, the fields, potentials, and electron flows and velocities are analyzed in the SIT structure at fixed drain to gate voltages. Using gate voltages from V_{GS} = -6V ... -16V and sweeping the drain, the I-V characteristics shown in Fig. 3.3 are obtained.

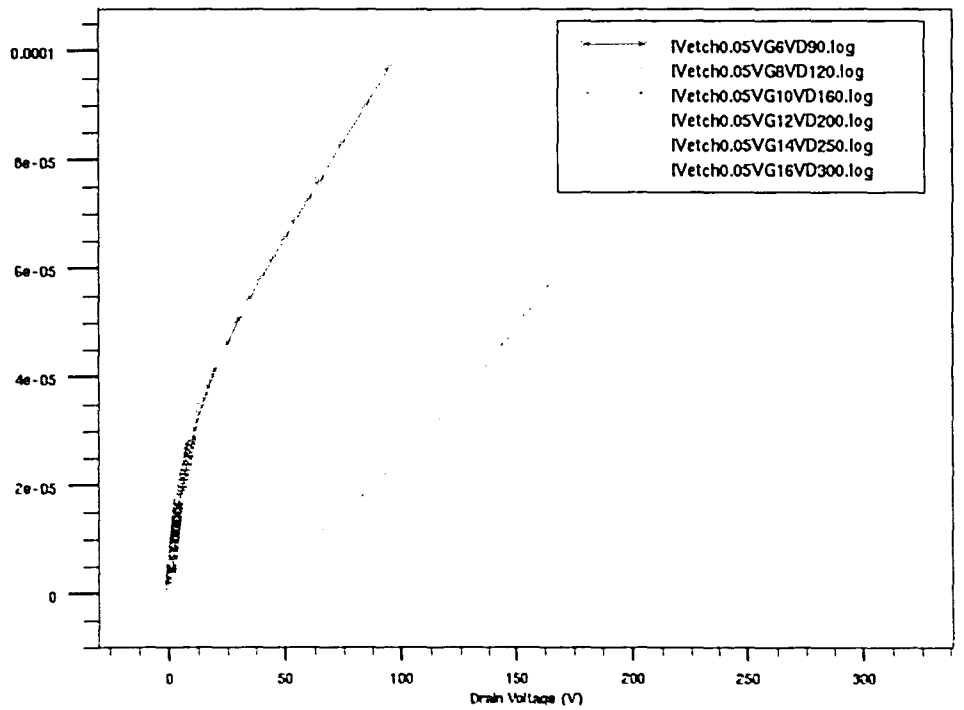

Fig. 3.3 Characteristics of a 4H-SiC RGSIT with V_{GS} = -6V ... -16V

From the simulations in Fig. 3.3, we can observe the various modes of operation. For example, in the far left I-V curve, V_{GS} = -6V, the channel region has not been fully-depleted and no barrier potential exists as shown in the simulations of Fig. 3.4. The SIT device, under these bias conditions, operates in the Ohmic conduction mode. As the drain-to-gate voltage increases, V_{DG} in the simulations, for a fixed V_{GS}, the channel becomes fully-depleted and a space charge region forms switching the mode of conduction to SCLC. In the far right I-V curve in Fig. 3.3, V_{GS} = -16V, the channel is fully depleted and a potential barrier exists (Fig. 3.5). The mode of operation is initially Thermionic emission as electrons cross over the potential barrier. As the drain-to-gate voltage increases, the barrier potential is modulated by the drain voltage. Once the barrier potential has been completely lowered, as shown in Fig. 3.6, the mode of operation switches to SCLC.

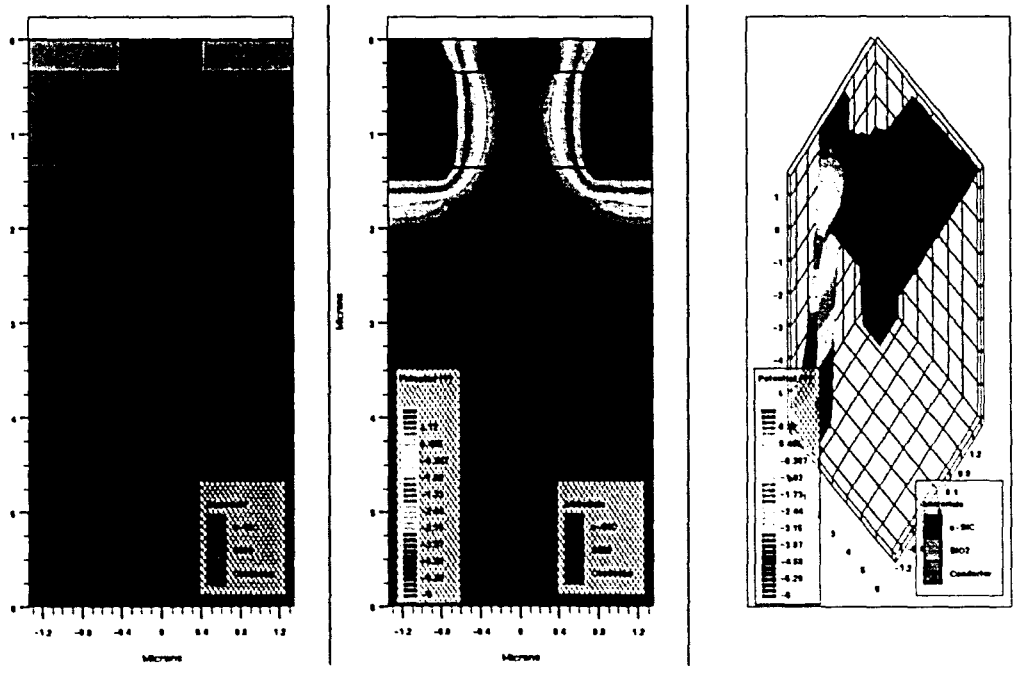

Fig. 3.4 4H-SiC RGSIT, V_G = -6V, V_D = 0V, Depletion region (left), 2-D potential (middle), 3-D potential (right). No potential barrier (no saddle point)

From the simulations in Fig. 3.3, we can observe the various modes of operation. For example, in the far left I-V curve, V_{GS} = -6V, the channel region has not been fully-depleted and no barrier potential exists as shown in the simulations of Fig. 3.4. The SIT device, under these bias conditions, operates in the Ohmic conduction mode. As the drain-to-gate voltage increases, V_{DG} in the simulations, for a fixed V_{GS}, the channel becomes fully-depleted and a space charge region forms switching the mode of conduction to SCLC. In the far right I-V curve in Fig. 3.3, V_{GS} = -16V, the channel is fully depleted and a potential barrier exists (Fig. 3.5). The mode of operation is initially Thermionic emission as electrons cross over the potential barrier. As the drain-to-gate voltage increases, the barrier potential is modulated by the drain voltage. Once the barrier potential has been completely lowered, as shown in Fig. 3.6, the mode of operation switches to SCLC.

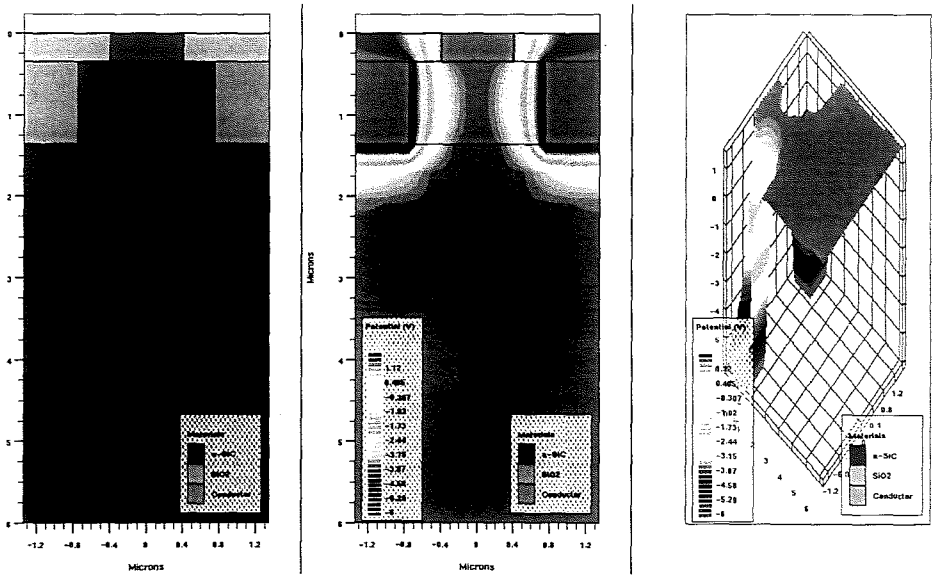

Fig. 3.4 4H-SiC RGSIT, V_G = -6V, V_D = 0V, Depletion region (left), 2-D potential (middle), 3-D potential (right). No potential barrier (no saddle point)

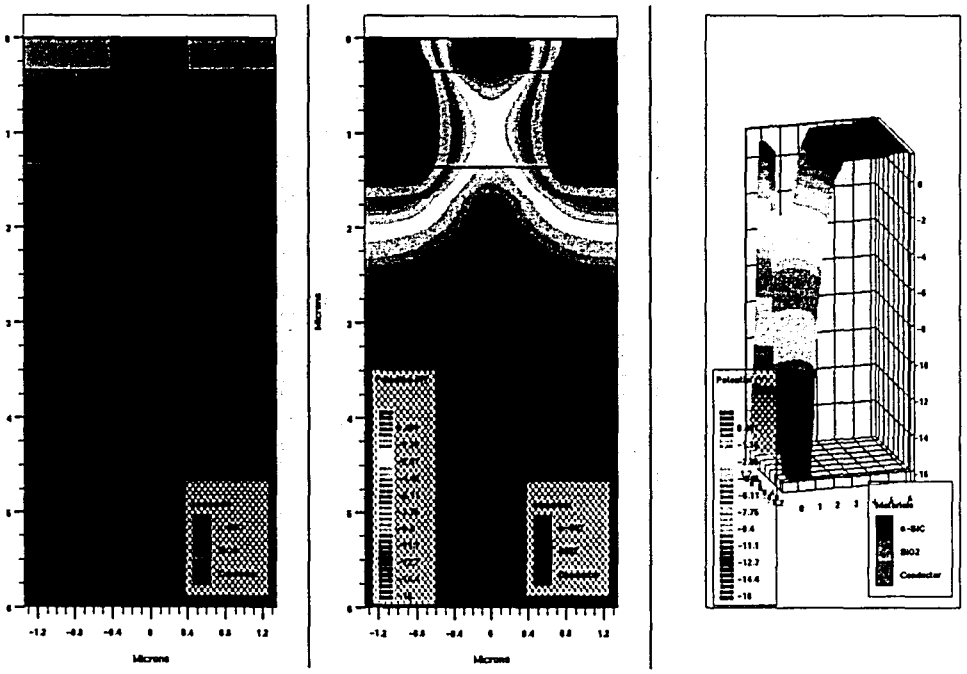

Fig. 3.5 4H-SiC RGSIT, V_G = -16V, V_D = 0V, Channel fully depleted (left), 2-D potential barrier (middle), 3-D saddle point (right)

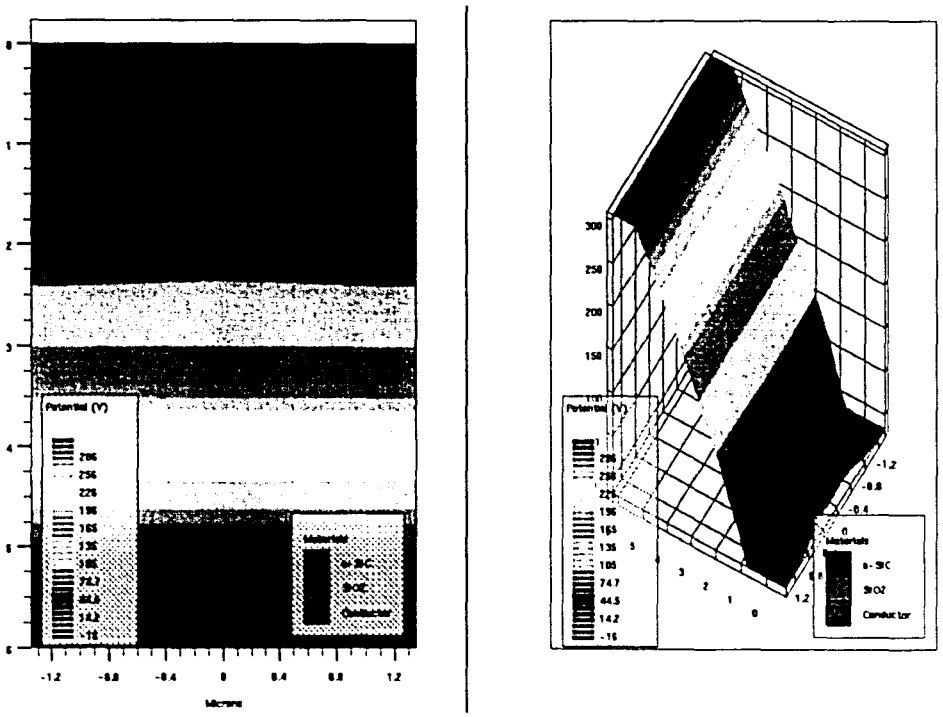

Fig 3.6 V_G = -16V, V_D = 300V, Barrier has been completely lowered, 2-D potential (left) 3-D potential (right)

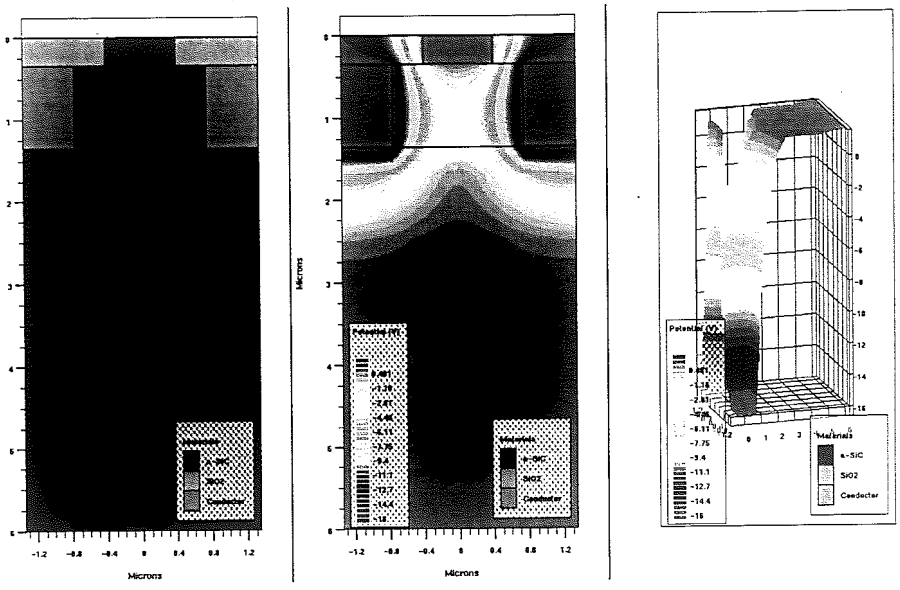

Fig. 3.5 4H-SiC RGSIT, V_G = -16V, V_D = 0V, Channel fully depleted (left), 2-D potential barrier (middle), 3-D saddle point (right)

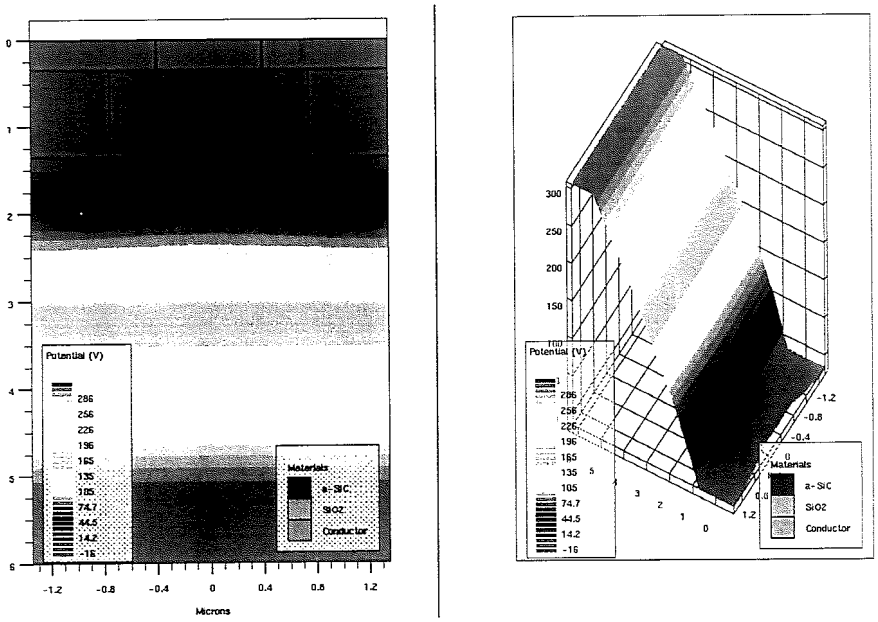

Fig 3.6 V_G = -16V, V_D = 300V, Barrier has been completely lowered, 2-D potential (left) 3-D potential (right)

3.3 Analysis of Simulation Results

From the above simulations, we can conclude Silvaco's ATLAS software presents a reasonable picture for the operational modes of the SiC SIT device, although some problems are apparent with regards to the magnitude of the results. When simulated drain currents at specific drain-to-gate voltages are compared with the drain currents given from actual tested devices, the simulated current level is a great deal larger than the actual device data. The photo of a 4H-SiC SIT device (5 cm width and 1.34E-3 cm^2 area) shown in Fig. 3.7 shows a gate voltage stepped from –6 to –16V. A 1mA drain current flows for V_G = -12V and V_D = 250V. A V_G = -12V and V_D = 200V in simulations suggest the drain current would be 2A! The reason for the elevated current level is not well understood; however, a problem with regards to velocity saturation and carrier mobility may contribute to this elevated current level. Electron velocities collected from simulations often exceed values for a programmed saturation velocity in the 4H-SiC material. In addition, problems with regards to the flow of current density have also been encountered, which Silvaco engineers are currently addressing.

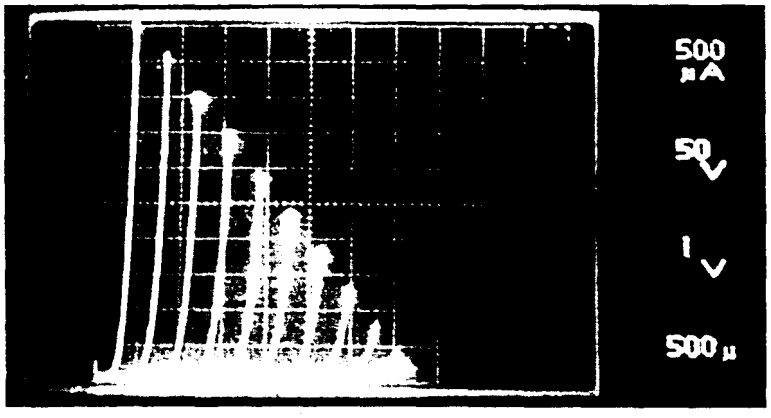

Fig. 3.7 Output I-V characteristics of a 4H-SiC RGSIT (5 cm width and 1.34E-3 cm^2 area)

Chapter 4

Interface Charges and their effect on the Operation of 4H-SiC Recessed Gate Static Induction Transistors (RGSITs)

4.1 Theory of Interface Charge Effects

The SIT may have issues relating to device reliability similar to previous studies with GaAs MESFETs [9]. The possibility exists that interface charges on the 'shoulder' region of the SIT device, shown in Fig. 4.1, serve to modulate the barrier height of the previously discussed saddle point, resulting in a changed drain current at a specific source to drain voltage.

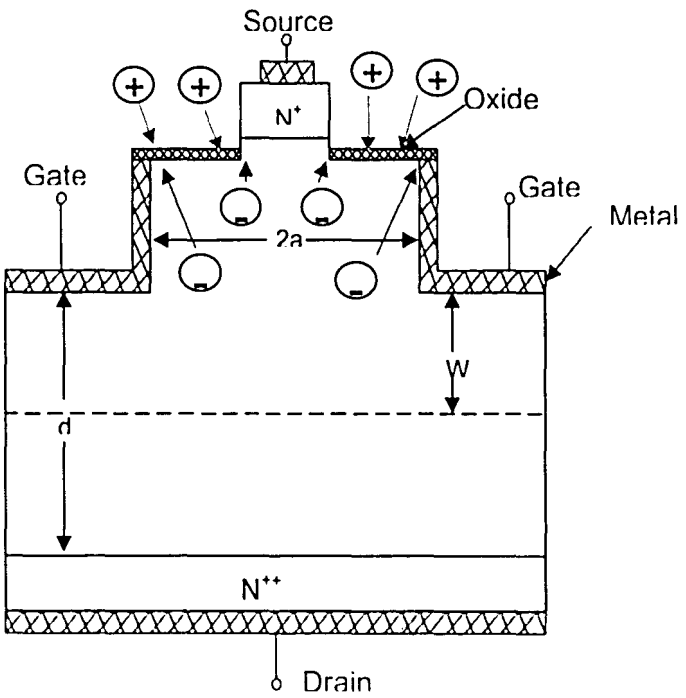

Fig. 4.1 RGSIT structure to be analyzed with interface charge on 'shoulder' region

Positive interface charge (possibly due to sodium contamination in an overlaying oxide) on the shoulder region may decrease the barrier height of the saddle point and negative interface charge (possibly due to electrons occupying traps at the SiC-SiO_2 interface) may increase the barrier height. Positive interface charge will effectively pull the internal electric fields towards the 'shoulder' region, inhibiting field penetration into the full channel of the device. The opposite is true of negative interface charge, allowing stronger fields to penetrate into the channel.

The effect of interface charge on the 'shoulder' region is to change the effective gate bias of the device. A RGSIT device with positive/negative interface charge on the 'shoulder' region will see an effective gate bias that is smaller/larger than the applied gate voltage. Therefore, a device with positive interface charge can maintain a fixed drain current at a lower drain bias than a device with no interface charge. It should also be true that a device with negative interface charge must increase its drain bias to maintain a fixed drain current with respect to a device with no interface charge. The expected impact on the I-V characteristics due to 'shoulder' interface charge is shown in Fig 4.2.

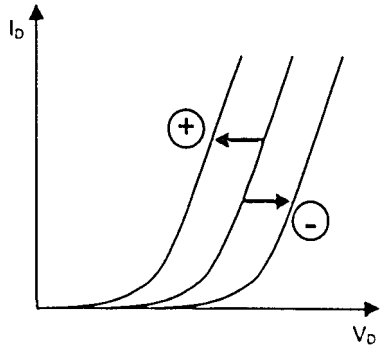

Fig 4.2: Positive interface charge is expected to shift the I-V curve to the left due to barrier height lowering. Negative interface charge is expected to shift the I-V curve to the right due to barrier height increase.

4.2 Simulation Analysis of Interface Charge Effects

Using interface charge concentrations of $Q^+ = 10^{12}$ cm^{-2} and $Q^- = 10^{12}$ cm^{-2} the potential barrier is modulated in the manner described in Fig 4.2. This value of Q^- is selected for ease of simulation. A negative charge concentration of 10^{13} cm^{-2} will not allow convergence. Fig. 4.3, 4.4, and 4.5 show the potential barriers for a specific drain-to-gate voltage, comparing barrier height to interface charge. With no interface charge on the 'shoulder' region, the height of the potential barrier with V_{GD}=-14 is 1.6V. With $Q^- = 10^{12}$ cm^{-2} negative interface charge concentrations on the 'shoulder' region, the potential barrier increases to approximately 1.8V at V_{GD}=-14V. A $Q^+ = 10^{12}$ cm^{-2} positive interface charge concentration decreases the potential barrier to approximately 1.5V under the same gate-to-drain bias. The effects of a given interface charge on the I-V characteristics can be viewed in Fig. 4.6 using the same gate-to-source biases, V_{GS}=-14V.

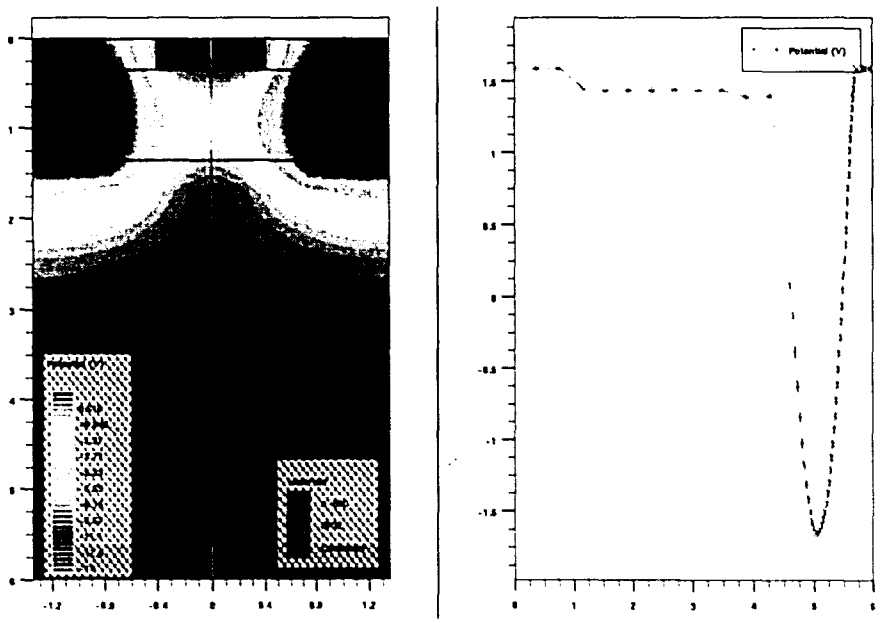

Fig. 4.3 Potential barrier with no interface charge, V_G = -14V V_D = 0V
Peak Potential Barrier value ~ -1.6V

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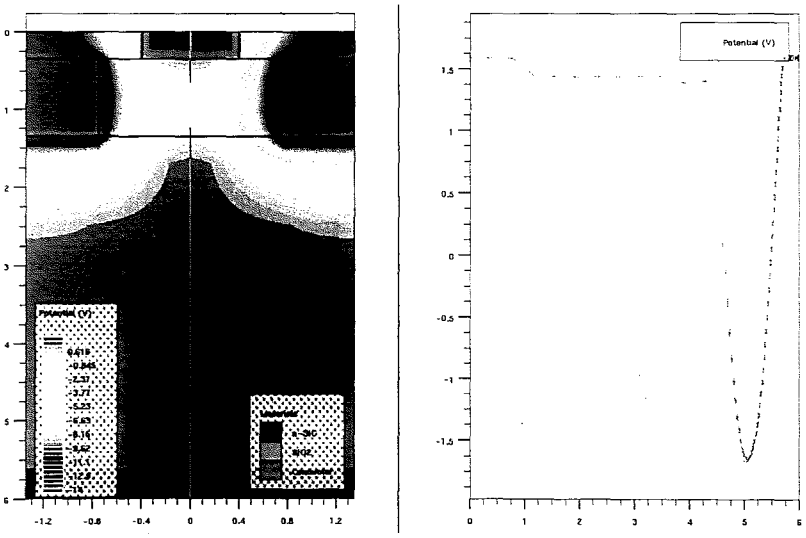

Fig. 4.3 Potential barrier with no interface charge, V_G = -14V V_D = 0V
Peak Potential Barrier value ~ -1.6V

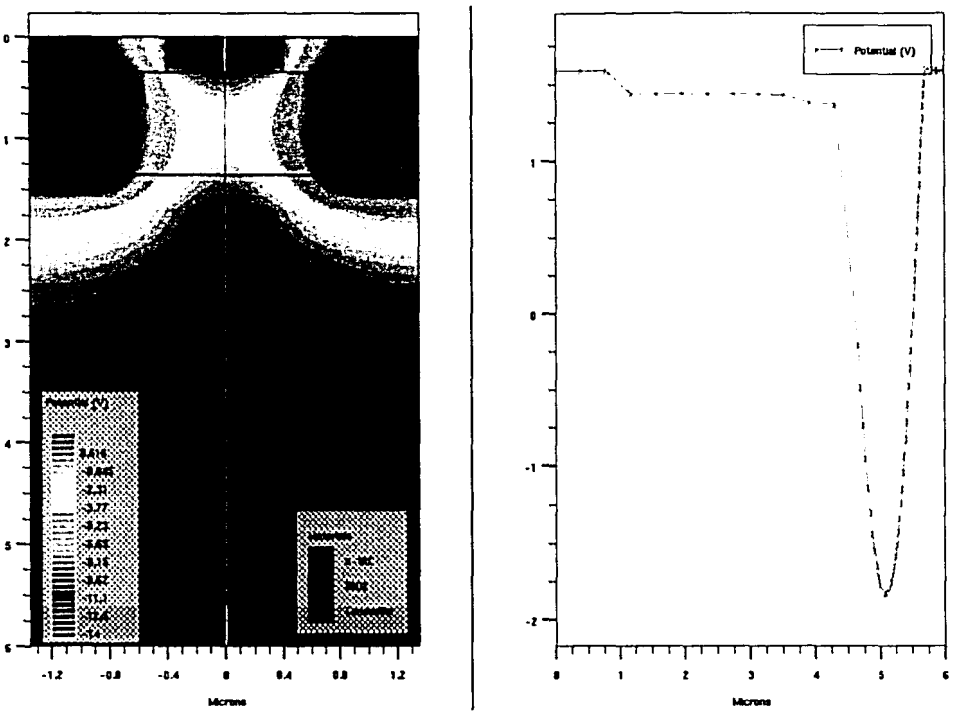

Fig. 4.4 Potential barrier with negative interface charge, $Q^- = 10^{12}\,cm^{-2}$, $V_G = -14V$, $V_D = 0V$ Peak Potential Barrier value ~ -1.8V

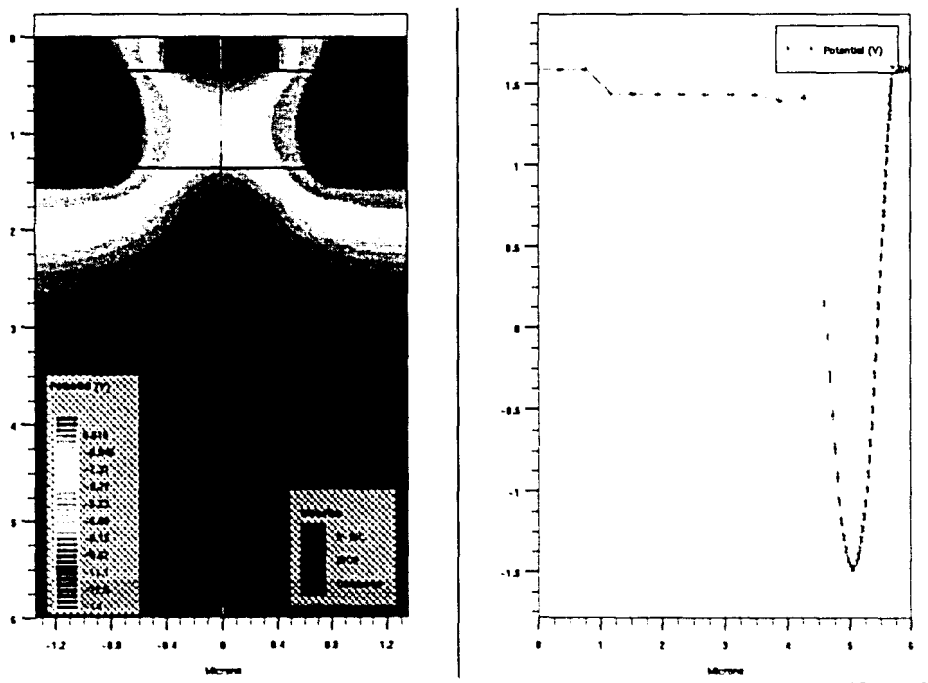

Figure 4.5 Potential barrier with positive interface charge, $Q^+ = 10^{12}\,cm^{-2}$, $V_{GS} = -14V$, $V_{DS} = 0V$ Peak Potential Barrier value ~ -1.5V

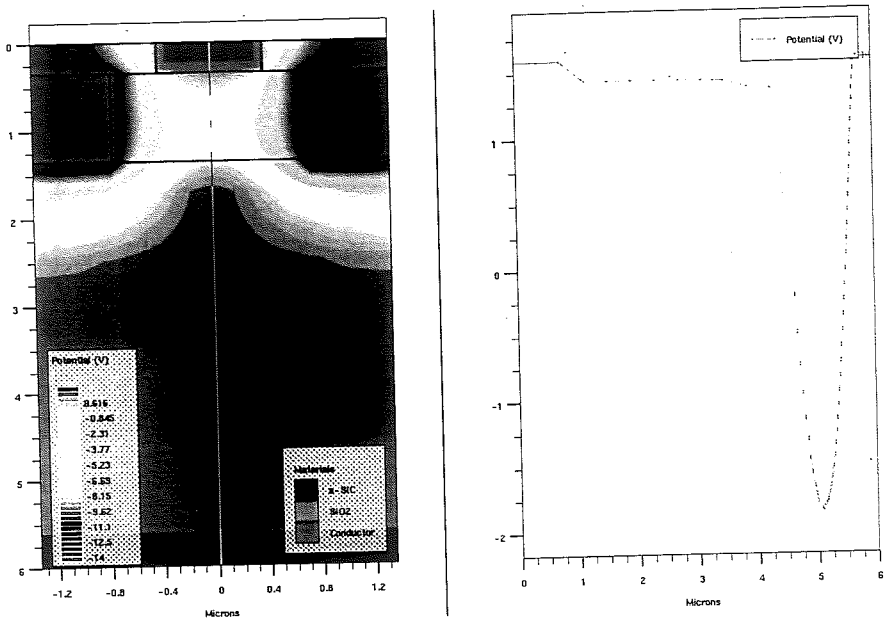

Fig. 4.4 Potential barrier with negative interface charge, $Q^{-} = 10^{12}\ cm^{-2}$, $V_G = -14V$, $V_D = 0V$ Peak Potential Barrier value ~ -1.8V

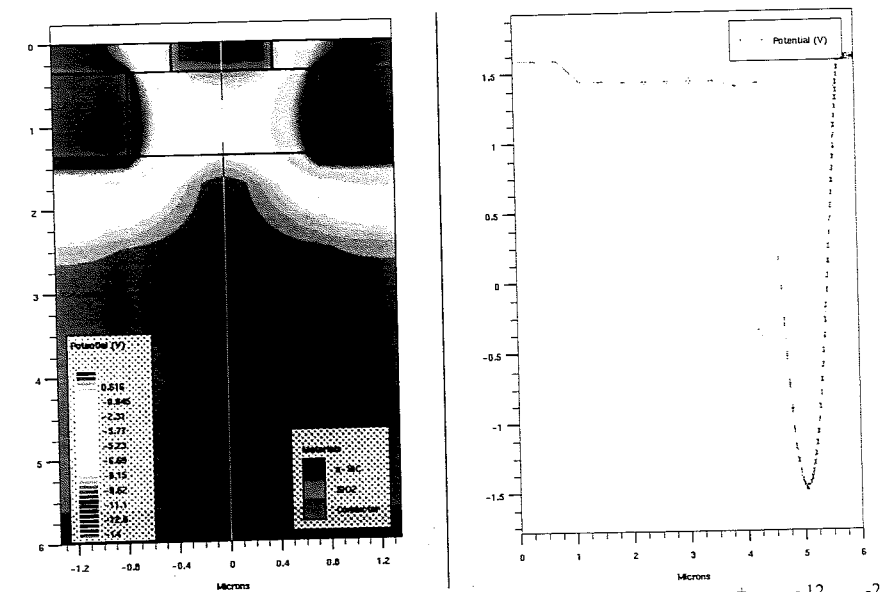

Figure 4.5 Potential barrier with positive interface charge, $Q^{+} = 10^{12}\ cm^{-2}$, $V_{GS} = -14V$, $V_{DS} = 0V$ Peak Potential Barrier value ~ -1.5V

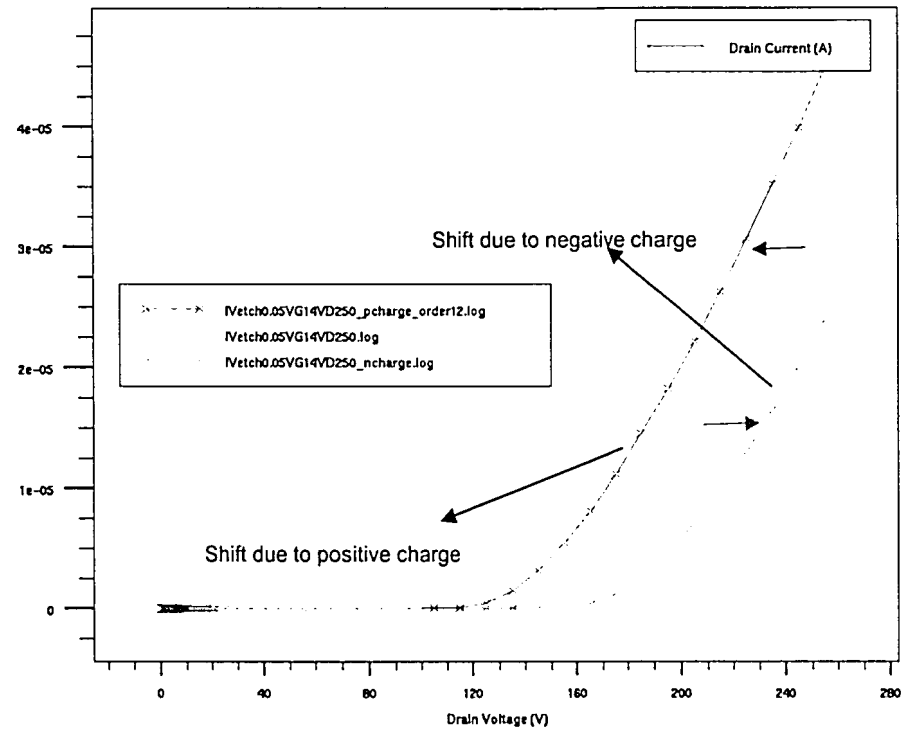

Fig. 4.6 I-V characteristics from left to right, $Q^{+} = 10^{12}\,cm^{-2}$, no charge, and $Q^{-} = 10^{12}\,cm^{-2}$ on the interface.

4.3 Sources of Interface Charge

Simulations have shown that interface charge on the 'shoulder' region may lead to unexpected I-V characteristics. Positive charge near the shoulder interface, based on previous experience with sources of contamination, is very likely to be due to an alkali ion contamination, such as sodium contamination of the oxide. Sodium present in processing equipment can contaminate devices. SIT device exposure to human activity during mid-processing can also lead to sodium contamination [17]. Negative interface charge can be a result of electrons occupying interface traps in the shoulder region. The sharp corners in the 'shoulder' region create a crowding of the electric field. High electric fields in the 'shoulder' region, shown in Fig. 4.7, can accelerate electrons into

the oxide where they become trapped leading to a negative interface charge. This section of the device is often a source of breakdown due to poor oxide quality and/or lack of thickness control. Fig. 4.7 illustrates an increase of 2 to 5 times in the magnitude of the electric field strength in the presence of a sharp corner (electric field crowding), which may be present in the shoulder region of the RGSIT.

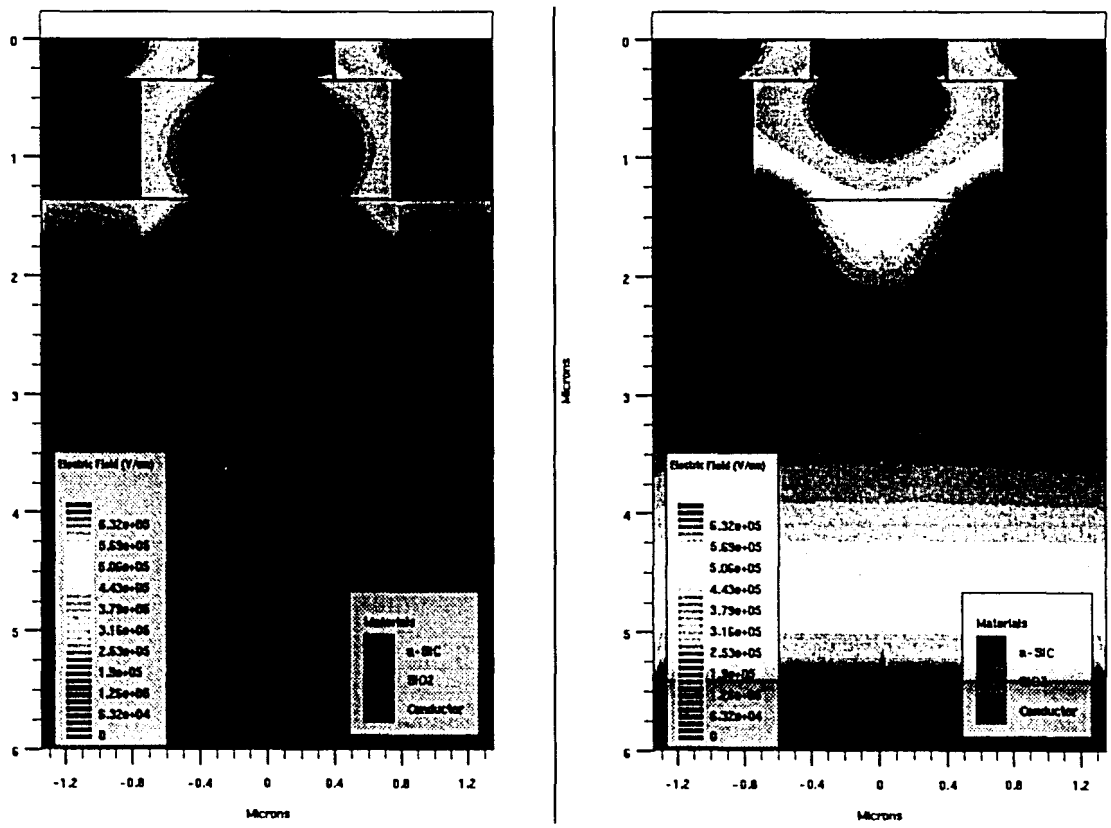

Fig. 4.7 Electric fields in corners of a RGSIT (left) V_{GS} = -14V (right) V_{DS} = 0V

the oxide where they become trapped leading to a negative interface charge. This section of the device is often a source of breakdown due to poor oxide quality and/or lack of thickness control. Fig. 4.7 illustrates an increase of 2 to 5 times in the magnitude of the electric field strength in the presence of a sharp corner (electric field crowding), which may be present in the shoulder region of the RGSIT.

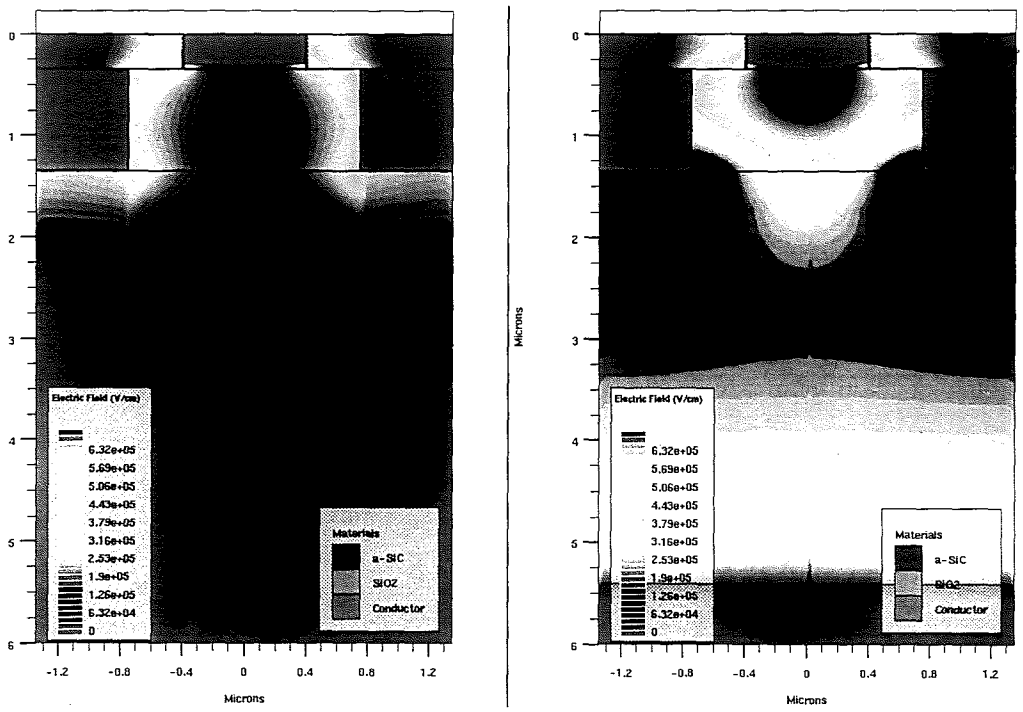

Fig. 4.7 Electric fields in corners of a RGSIT (left) V_{GS} = -14V (right) V_{DS} = 0V

Chapter 5

Modeling the Subthreshold Drain Current Characteristics in a Static Induction Transistor (SIT)

5.1 Introduction

With regards to the published literature, it appears the basic theoretical modeling of the SIT is lagging behind its practical realizations. This is particularly true in the subthreshold region, which experiences an exponential current dependence on the gate voltage. The drain current in this subthreshold region is the result of thermionic emission of carriers over a potential barrier [5],[7]. The height of the barrier is modeled by a linear dependence on gate and drain voltages. This assumption would be acceptable if the barrier height occurred at a fix location, which may not be the case in RGSIT devices. C. Bulucea and A. Rusu from the Polytechnic Institute of Bucharest have proposed a first order method of calculating the internal electrostatic potential in planar and RGSITs [18]. From their analytical method, the potential barrier height can be estimated.

Another factor required for analyzing the subthreshold drain current is the effective cross-section of current conduction in a SIT. As shown in Fig. 2.3, the width of the device, where electrons propagate, b, may vary depending on the location of the barrier height in the longitudinal or 'x' direction in the SIT. Therefore, an effective width, b_{eff}, must be calculated to estimate the total current flow in a SIT. As A. Strollo and P. Spirito have mentioned [19], several authors have developed a function that estimates

the effective width of the channel depending on the gate voltage and barrier height of the SIT.

In this chapter, the methods/results included in [18] and [19] shall be presented and re-analyzed. Then the subthreshold current due to thermionic emission, having been estimated using the results in [18] and [19], shall be compared to subthreshold I-V data collected from fabricated 4H-SiC RGSIT devices.

5.2 Defining the Intrinsic Region

The device model shown in Fig. 5.1 is an approximate description of the planar SIT device and is ideally suitable for the RGSITs. In this model, the channel and epitaxial layer share the same uniform doping and are re-defined as N^-. It is assumed that the channel and epitaxial layer are completely depleted. Additionally, the source and drain doping densities are re-defined as N^+. The electrical-field structure depicted in Fig. 5.1 illustrates the opposite action of two fields along the channel produced by the gate-source (E_A) and drain-source (E_B) voltages. This gives rise to a potential minimum, or barrier, which blocks the flow of electrons from the source to the drain. The location of the minimum potential can move anywhere along the channel axis, according to the relative strengths of the fields. The P^+/N^- junction replace the 'recessed' Schottky Metal Gate electrodes to control the barrier height in the channel and, thereby, the flow of electrons from source to drain electrodes. The built-in potential of the gate (same as that derived in Chapter 2) is still assumed to be that of a Schottky contact.

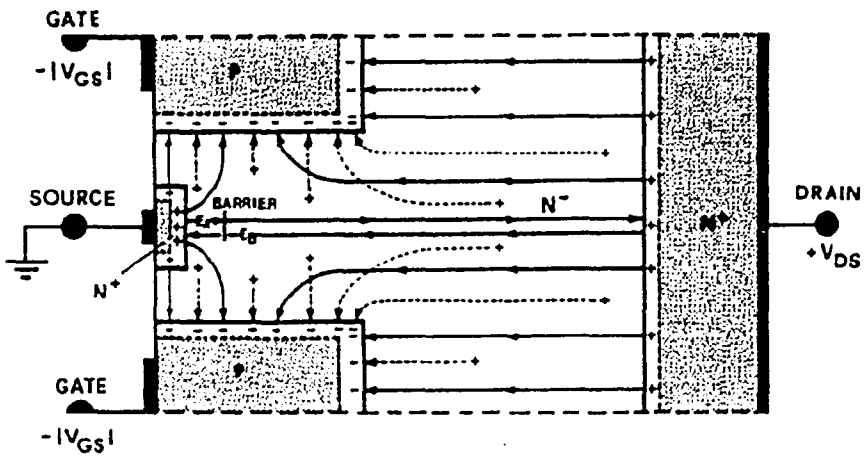

Fig. 5.1 A SIT geometric model illustrating barrier formation by the opposite actions of the electric fields generated by the gate-source and drain-source voltages [18]

In order to find a simple analytical function describing the electrostatic potential, $\phi(x,y)$, and the location of its minimum value, the main attention will be focused on the intrinsic region of the device shown in Fig. 5.2. The intrinsic region is defined as the area inside the **ABB`A`** rectangle. This is also the channel region of the device where the potential minimum occurs. The remaining region defined by the rectangle **CDD`C`** is referred to as the extrinsic region. Since the intrinsic region contains all of the biased contacts of the device except the drain contact, it is efficient to consider a point on the **BB`** boundary line biased by a virtual drain voltage now referred to as the intrinsic drain. The intrinsic drain $V_{DS}^{\bullet}$ is to be applied at the center point, $\mathbf{B}_0$, of the **BB`** boundary. The electrostatic potential along the **BB`** boundary has been given a cosine variation from the center value, $V_{DS}^{\bullet}$, to the constant potential along the **AB** and **A`B`** gate boundaries. The relationship between $V_{DS}^{\bullet}$ and the externally applied voltages of V_{GS} and V_{DS} will be discussed in the last section of this chapter.

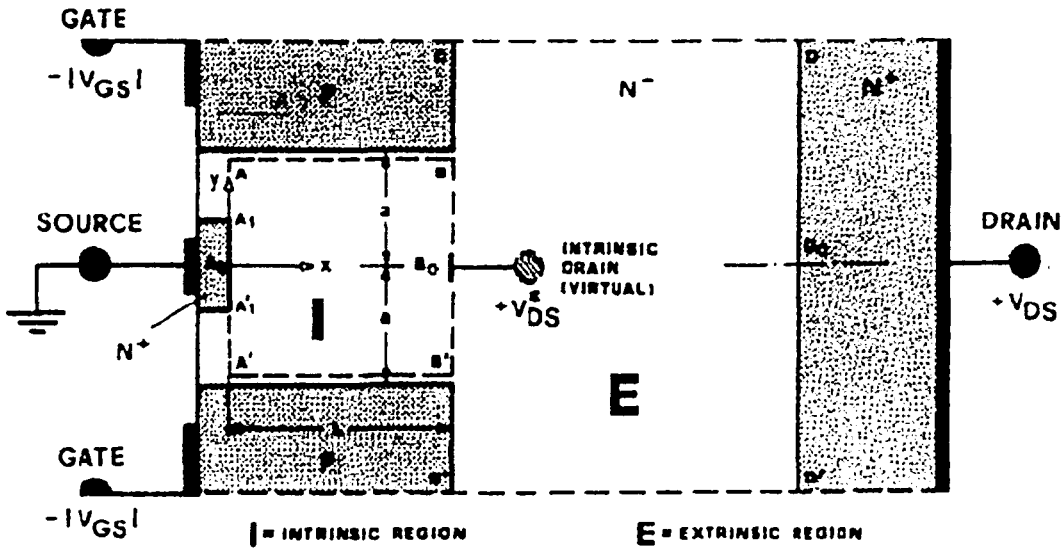

Fig. 5.2 SIT model is divided into an intrinsic region (**ABB`A`**) and extrinsic region (**CDD`C`**). A virtual drain, V_{DS}^{*}, is considered applied at point $\mathbf{B_0}$ [18]

5.3 Defining the Intrinsic Potential Function

The electrostatic potential in the intrinsic region must to be constructed to satisfy Poisson's equation. Therefore, the potential can be given as:

$$\frac{\partial^2\phi(x,y)}{\partial x^2} = \frac{\partial^2\phi(x,y)}{\partial y^2} = -\frac{qN_D^-}{\varepsilon_S} \tag{5.1}$$

Using the superposition principle, the potential function can be written as

$$\phi(x,y) = \phi_\rho(y) + \phi_0(x,y) \tag{5.2}$$

where $\phi_\rho(y)$ is the Poisson component (i.e. the component involving fixed and mobile space charge varying in the 'y' direction of the channel) of $\phi(x,y)$, and $\phi_0(x,y)$ is the

two dimensional Laplace component of $\phi(x,y)$ (i.e. the component free of space charge) due to the electrode biases. Based on the depletion approximation (i.e. neglecting mobile charges in the channel), the Poisson component $\phi_\rho(y)$ can be expressed by

$$\phi_\rho(y) = \phi_P\left[1-\left(\frac{y}{a}\right)^2\right]+\phi_G \tag{5.3}$$

where ϕ_G is the gate potential

$$\phi_G = -|V_{GS}| - V_{bi} - \phi_0 \tag{5.4}$$

and 'a' is the distance from the center of the source to the P^+ gate electrode. V_{GS}, V_{bi}, and ϕ_0 are the gate-to-source voltage, built-in potential of the gate (same as that derived in Chapter 2), and built-in potential of the source, respectively. Here we have assumed $V_{GS} < 0$. The built-in potentials can be calculated as

$$qV_{bi} = q\phi_B - \left[\frac{E_g}{2} - kT\ln\left(\frac{N_D}{n_i}\right)\right] > 0 \tag{5.5}$$

$$\phi_0 = \frac{kT}{q}\ln\left(\frac{N_D^+}{N_D^-}\right) > 0 \tag{5.6}$$

ϕ_P is a positively defined potential given by:

$$\phi_P = \frac{qN_D^- a^2}{2\varepsilon_S} > 0 \tag{5.7}$$

All potentials are referred to the source, where we assume $\phi_0(0,0) = 0$. Defining a positive pinch-off voltage, V_P, Eqn. 5.3 can be rewritten as

$$\phi_p(y) = -(|V_{GS}| - V_P + \phi_0) - \phi_P\left(\frac{y}{a}\right)^2 \tag{5.8}$$

$$V_P = \phi_P - V_{bi} > 0 \tag{5.9}$$

A natural Laplace function for the intrinsic SIT geometry, which satisfies the boundary conditions, can be defined as follows:

$$\phi_0(x, y) = \left[V_A \exp\left(-\frac{\pi x}{2a}\right) + V_B \exp\left(\frac{\pi x}{2a}\right)\right]\cos\left(\frac{\pi y}{2a}\right) \tag{5.10}$$

where V_A and V_B are constants to be determined, which have dimensions of volts. Eqn. 5.10 satisfies the Laplace equation, $\phi_0(x,y)$, and also vanishes at $y = \pm a$, so it does not interfere with the gate boundary condition imposed on the Poisson component. Eqn. 5.10 is similar to a function used by Shockley to describe the potential in the so-called extrapolated pinch-off region [20]. Combining Eqns. 5.9 and 5.10, the complete potential function is

$$\begin{aligned}\phi(x, y) = &-(|V_{GS}| - V_P + \phi_0) - \phi_P\left(\frac{y}{a}\right) \\ &+ \left[V_A \exp\left(-\frac{\pi x}{2a}\right) + V_B \exp\left(\frac{\pi x}{2a}\right)\right]\cos\left(\frac{\pi y}{2a}\right)\end{aligned} \tag{5.11}$$

Constants V_A and V_B are determined by imposing the boundary conditions on points A_0 and B_0 where L is the channel length (Fig. 5.2)

$$\phi(0,0) = 0 \qquad \phi(L,0) = V_{DS}^{*} \tag{5.12}$$

yielding

$$V_A = \frac{\mu_0}{\mu_0 + 1}\left[\left(|V_{GS}| - V_P + \phi_0\right) - \frac{V_{DS}^{*}}{\mu_0 - 1}\right] \tag{5.13}$$

$$V_B = \frac{\mu_0}{\mu_0^2 - 1}\left[V_{DS}^{*} + \frac{\mu_0 - 1}{\mu_0}\left(|V_{GS}| - V_P + \phi_0\right)\right] \tag{5.14}$$

where

$$\mu_0 = \exp\left(\frac{\pi L}{2a}\right) > 1 \tag{5.15}$$

is called the intrinsic electrostatic gain and characterizes the relative importance of the drain with respect to the gate in controlling the electrostatic potential. It is the equivalent of the triode gain factor μ_A used in the vacuum-tube literature.

We can prove $\phi(x,y)$, with constants V_A and V_B, satisfies Poisson's equation, Eqn. 5.1, as well as the boundary conditions at the gate electrodes and at the points A_0 and B_0. $\phi(x,y)$ is characterized by cosine potentials along the intrinsic region boundaries **AA`** and **BB`**. Due to the symmetric nature of the intrinsic region, this approximation is expected to provide an accurate description of the potential along the center axis of the region, $\mathbf{A_0B_0}$.

5.4 Calculating the Barrier Height

Since $\phi(x,y)$ is symmetrical in y, the potential minimum, $\phi_{\min}$, is expected to occur along the x axis and is easily obtained by setting the derivative of $\phi(x,0)$ equal to zero.

$$\frac{\partial\phi(x,0)}{\partial x} = \frac{\pi}{2a}\left[-V_A \exp\left(-\frac{\pi x}{2a}\right) + V_B \exp\left(\frac{\pi x}{2a}\right)\right] = 0 \tag{5.16}$$

yielding

$$x_{\min} = \frac{a}{\pi}\ln\left(\frac{V_A}{V_B}\right) \tag{5.17}$$

From this point, we can calculate the potential minimum, $\phi_{\min}$

$$\phi_{\min} = -\left(|V_{GS}| - V_P + \phi_0\right) + 2\sqrt{V_A V_B} \tag{5.18}$$

This solution gives $x_{\min} = L/2$ at $V_{DS}^{\bullet} = 0$ regardless of the gate voltage. Additionally, the solution shows, for a particular $V_{DS}^{\bullet}$, the barrier vanishes at the source end of the channel shown in Fig. 5.3. $V_{DS}^{\bullet}$ is limited by the condition

$$V_{DS}^{\bullet}(\text{lim}) = \frac{1}{2}\frac{(\mu_0 - 1)^2}{\mu_0}\left(|V_{GS}| - V_P + \phi_0\right) \tag{5.19}$$

Invoking the condition of $V_{DS}^{\bullet} \le V_{DS}^{\bullet}(\text{lim})$ ensures nonzero barrier and also $V_A > 0$. Since the minimum potential occurs at the $\mathbf{A_0B_0}$ center of axis where the current flows, the $\phi_{\min}$ calculated is the potential barrier height in the thermionic equation.

Table 5.1 Physical parameters of the device used for calculations of $\phi(x, y)$

Parameter Definition	Notation	Value	Units
Channel impurity concentration	N_D^-	1.35×10^{16}	cm^{-3}
Source/drain impurity concentration	N_D^+	1×10^{19}	cm^{-3}
Channel center to gate	A	0.75	μm
Channel Length	L	1	μm
Metal built-in voltage	V_{bi}	1.3	V

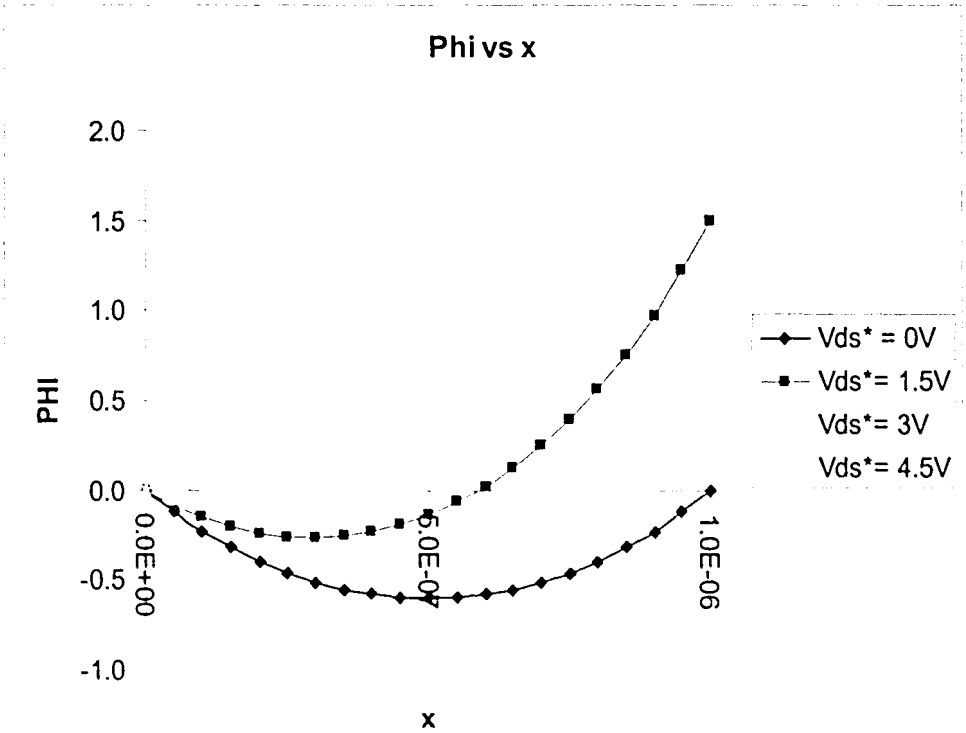

Fig. 5.3 Electrostatic potential, $\phi(x,0)$, along the channel axis for V_{GS} = -7V

5.5 Channel Effective Width, b_{eff}, in the Subthreshold Regime

For small current values the potential distribution in the channel of the SIT is not affected by the charge of electrons injected by the source. In the subthreshold regime, the device analysis can be performed by evaluating the carrier flow over the potential barrier in the channel. In previous a publication [19], this analysis has been developed by several authors [21]-[23] and can be summarized in the following paragraphs.

Due to the increase of $\phi(x,y)$ along the y-axis going from the channel center to the gate regions, the mobile carrier will be confined in a transverse length b_{eff} less than the minimum cross-section of the channel $2a$. Following the analysis of others [9], the effective channel width can be written as

$$b_{eff} = \frac{1}{n^*}\int_{-a}^{a} n(x^*, y)\partial y \tag{5.20}$$

which can be rewritten as

$$b_{eff} = \int_{-a}^{a} \exp\left[\frac{\phi(x^*, y) + \phi_{\min}}{V_T}\right]\partial y \tag{5.21}$$

where n^*, x^*, and V_T are the electron concentration at the saddle point, the abscissa of the potential minimum, and the thermal voltage, V_T = kT/q. If the potential distribution in the y direction is assumed to have a simple parabolic shape, then the integral in Eqn. 5.21 can be easily evaluated as

$$b_{eff} = a\sqrt{\pi}\sqrt{\frac{V_T}{V_{bi} + |V_{GS}| - \phi_{\min}}}\,erf\left(\sqrt{\frac{V_{bi} + |V_{GS}| - \phi_{\min}}{V_T}}\right) \tag{5.22}$$

In Eqn. 5.22, we see the effective channel width remains almost constant with increasing drain voltage, despite lowering the value of ϕ_{min}, due to the larger term of $V_{bi} + |V_{GS}|$.

5.6 Modeling Parameters and Experimental RGSIT Devices

Expressions have been developed to describe the barrier height and the cross-section of the SIT. The remaining factor to be analyzed is the relationship between $V_{DS}^{\bullet}$ and the externally applied voltages of V_{GS} and V_{DS}. We will assume $V_{DS}^{\bullet}$ is linearly dependent upon V_{GS} and V_{DS} [18]

$$V_{DS}^{\bullet} = V_0 + \alpha_G (V_{GS} + V_P) + \alpha_D V_{DS} \tag{5.23}$$

where V_0, α_G, and α_D are geometry and doping dependent constants. This linear relationship is a result of the linearity of Poisson's equation and is valid as the boundaries of the source, gate, and drain electrodes are fixed. Using numerically calculated data, the values of V_0, α_G and α_D were found to be -0.02, 0.76 and 0.20, respectively [18].

In our work, a similar approach has been used with the exception subthreshold data has been taken from fabricated 4H-SiC RGSIT devices. As a result, the thermionic emission equation has been able to model accurately the subthreshold I-V characteristics of the fabricated devices. The results of this study are described in the next two sections.

5.6.1 I-V Characteristics of the Experimental 4H-SiC RGSIT Devices

The experimental 4H-SiC RGSIT devices are common source devices each with a source length of 2.5 cm per cell. The geometries of these devices are reasonably close to the values employed in the simulations and listed in Table 3.1. The devices are hermetically sealed with a lidding operation in dry nitrogen. An example of a packaged RGSIT under test is shown in Figs. 5.4 and 5.5, with its lid removed.

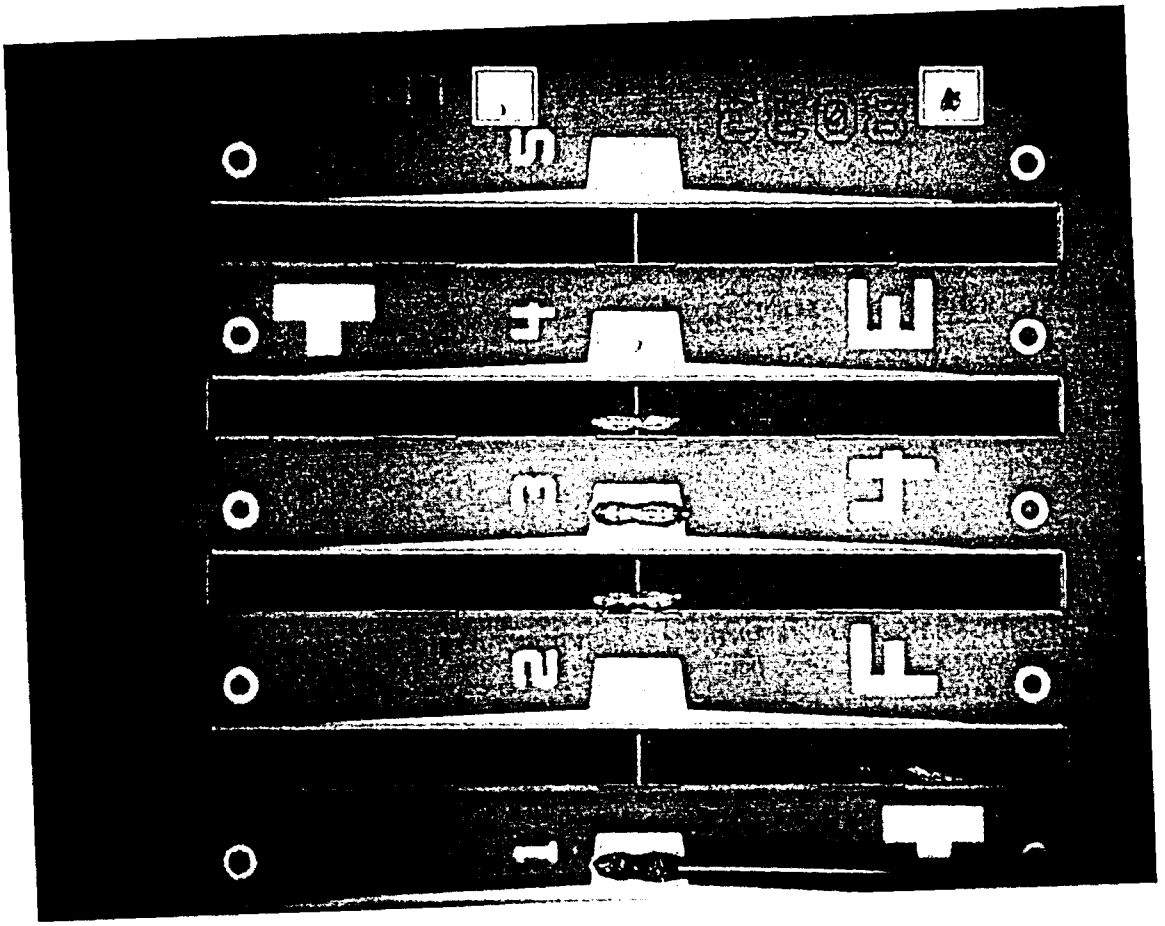

Fig. 5.4 4H-SiC RGSIT package showing four of the common source devices

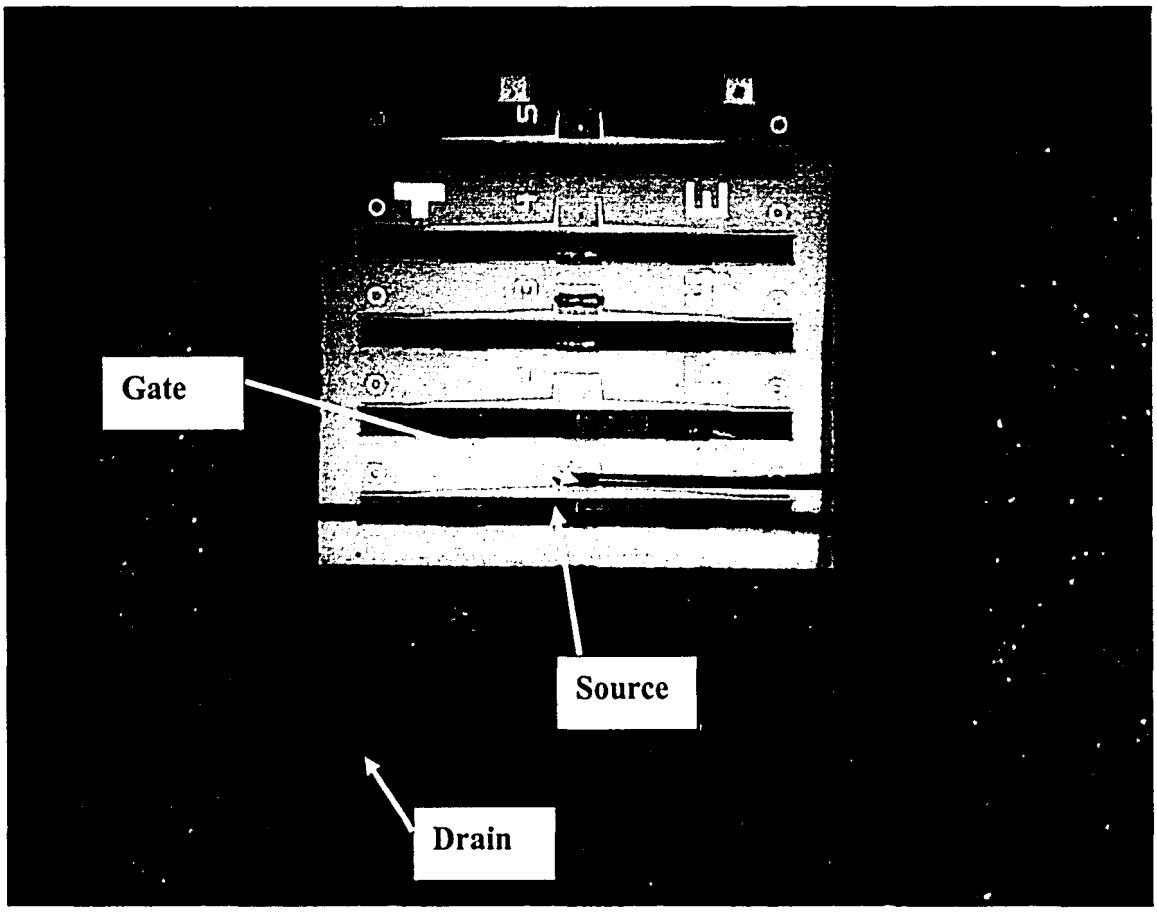

Fig. 5.5 4H-SiC RGSIT package showing connections of source, gate, and drain

Using a HP 4145A Semiconductor Parameter Analyzer connected to a computer running National Instruments LabVIEW®4, version 4.0.1, the drain current was measured for a fixed gate voltage, V_{GS}, while sweeping the drain voltage, V_{DS}. The I-V characteristics of a common source device are shown in Figs. 5.6 and Fig. 5.7.

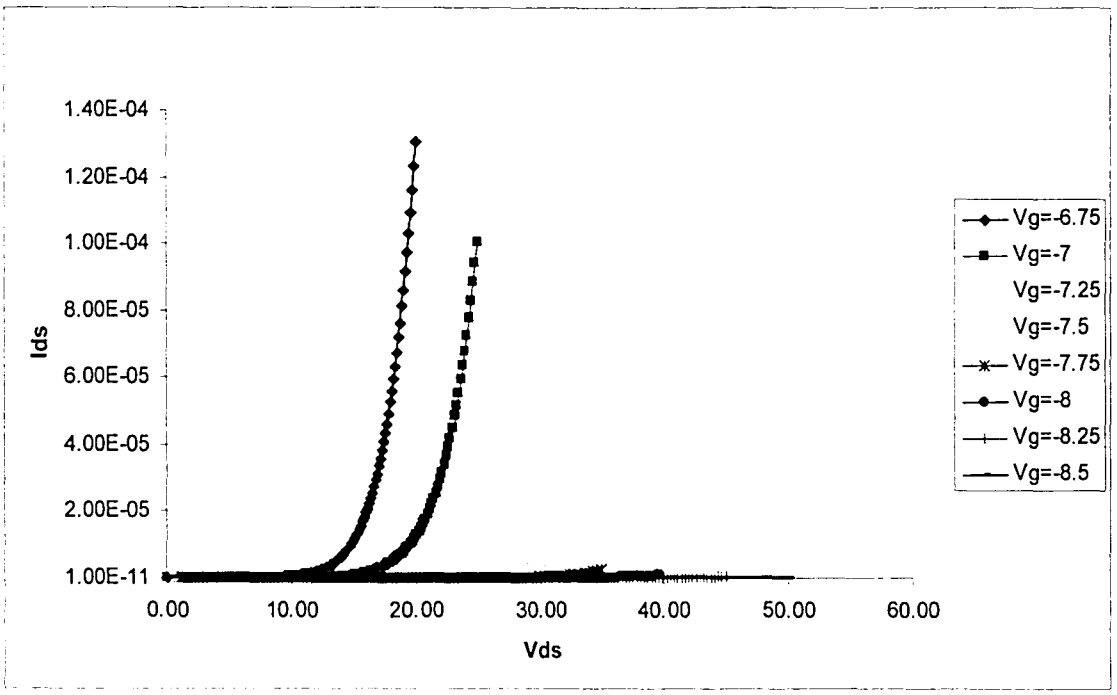

Fig. 5.6 Drain current vs. drain voltage for fixed gate voltages

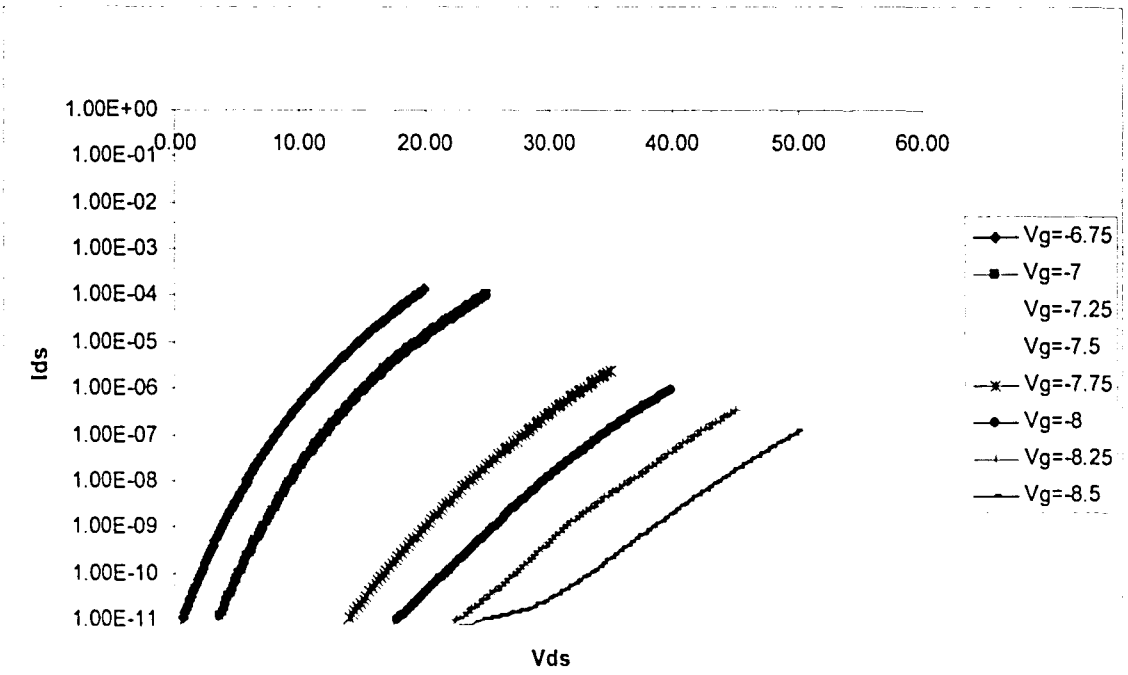

Fig. 5.7 Logarithmic drain current vs. drain voltage for fixed gate voltages

5.6.2 Determination of Modeling Parameters

Considering the experimental 4H-SiC RGSIT device measurements in Fig. 5.7, the subthreshold region shall be referred to as the operation where the drain current values are less than 1μA. The subthreshold I-V characteristics of the experimental 4H-SiC RGSITs are compared with the computed subthreshold currents using the thermionic emission equation (Eqn. 2.7). Using the results of [18] and [19] to compute the barrier height (Eqn. 5.18) and effective width (Eqn. 5.22), values for V_0, α_G, and α_D are chosen to fit the experimental data. The values are V_0, α_G, and α_D 0, 0.45, and 0.08, respectively. The fitted curves are shown in Fig. 5.8. The experimental subthreshold current is accurately modeled with the thermionic emission equation using the empirically fitted drain voltage. As the drain current exceeds 1μA, SCLC becomes the dominate mode of operation and thermionic emission has less influence on the I-V characteristics.

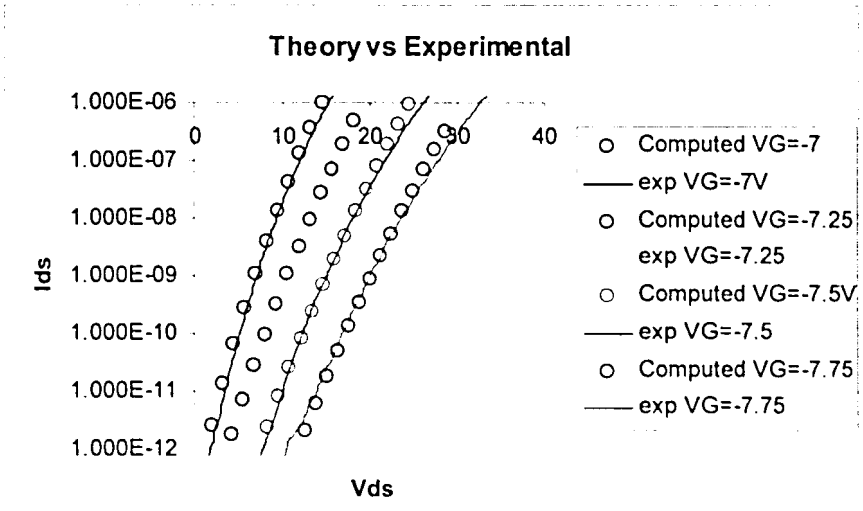

Fig. 5.8 Computed drain current overlaid by experimentally collected data

Once the calculated drain voltage is known, the change of the effective width, b_{eff}, (Eqn. 5.22) with respect to the change of the drain voltage is shown in Fig. 5.9. As the drain voltage increases, the increase in the effective width is minimal due to the large term $V_{bi}+|V_{GS}|$ in Eqn. 5.22. In addition, the values of the effective width are reasonable when compared to the channel half width, a. As is expected theoretically, and observed in simulation, the carriers are pinched into a small channel near the center of the device due to the potential barrier and the geometry of the saddle point.

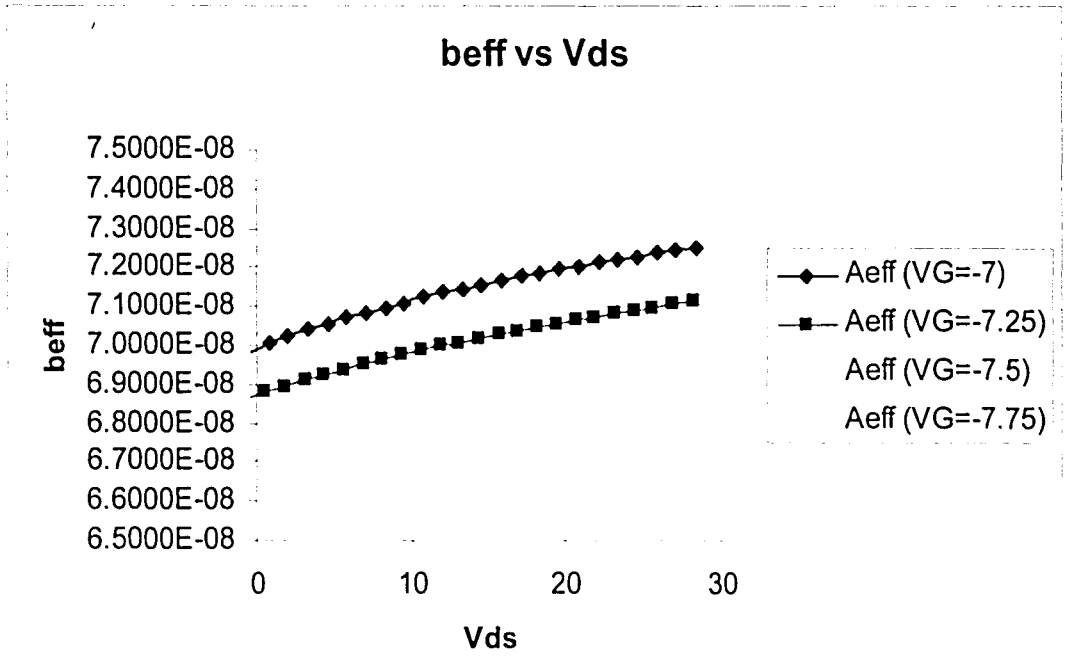

Fig. 5.9 Effective width, b_{eff}, vs. Drain voltage, V_{DS}

Chapter 6
Conclusions

6.1 Conclusions

The results presented in this thesis included the study of the 4 different regions of the Static Induction Transistor (SIT) operation. In addition, the simulated effects of interface charge on the operation of 4H-SiC recessed-gate SIT (RGSIT) devices are examined. Finally, the mechanisms of subthreshold conduction are analyzed.

6.1.1 Effects of Interface Charge on the Operation of 4H-SiC RGSIT

The presence of interface charge on the 'shoulder' region has been shown to modulate the barrier height of the saddle point in the channel region which controls the current for a specific drain voltage. A RGSIT device with positive/negative interface charge on the 'shoulder' region will see an effective gate bias that is smaller/larger than the applied gate voltage. The expected impact on the I-V characteristics due to positive/negative 'shoulder' interface charge is to shift individual I-V curves, for a fixed V_{GS}, to the left/right due to barrier height lowering/increase.

6.1.2 Results of Modeled Subthreshold Drain Current

The barrier heights, effective channel widths, and drain currents have been calculated using a superposition analysis of the Poisson and Laplace components of the electrostatic potential in the 'intrinsic' region of the SIT. For a given gate-to-source bias,

the analysis shows a barrier height decrease for an increasing drain-to-source bias. Additionally, for a particular drain-to-source bias, the barrier vanishes at the source end of the channel. Current due to thermionic emission is empirically fitted to experimental data of fabricated SiC RGSIT devices using the theoretical results of the barrier height and effective channel width; a linear approximation is used relating the intrinsic drain voltage to the actual drain and gate voltages. Knowing the linear intrinsic drain approximation coefficients, V_0, α_G, and α_D, it can be seen that an increase in the drain voltage increases the effective width minimally; the path of the carriers in the channel region is relatively independent of the drain voltage.

6.2 Recommendations

6.2.1 Further Study of Interface Charge

As stated previously, positive interface charge near the shoulder interface is very likely to be due to an alkali ion contamination, such as sodium contamination of the oxide [17]. Sodium present in processing equipment can contaminate devices. SIT device exposure to human activity during mid-processing can also lead to sodium contamination. Negative interface charge can be a result of electrons occupying interface traps in the shoulder region.

Continued work with Silvaco engineers to discover the reason for differences between simulations and experimental device structures is recommended. We should examine another simulator from a company called Integrated Systems Engineering (ISE), which has a 3D simulation package called DESSIS with a 2D/3D Editor and Process

Emulator called DEVISE. Another simulator package from Syborg, which operates on PC platforms, should also be considered as possible upgrade from Silvaco ATLAS. Results from these simulators may portray a more accurate prediction of experimental RGSIT devices. Furthermore, the refinement of simulation structures and models with experimentally determined modeling parameters extracted from device structures is recommended.

6.2.2 Further Study of Subthreshold Conduction

To further aid in the understanding of the subthreshold region, I propose a more extensive study to accurately model the modulation of the barrier height due to the drain voltage at the electrode. Furthermore, experimental techniques to extract modeling parameters from SiC RGSIT devices employing the various modeling expressions described earlier in this thesis should be determined. These techniques already exist for silicon-based devices and should be developed for the SiC RGSIT device structures.

References

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Appendix

SILVACO ATLAS: DEVICE SIMULATOR

A.1 Introduction to Silvaco ATLAS

Silvaco ATLAS is a physically-based two and three dimensional device simulator capable of simulating a wide range of devices including diodes, FETs, BJTs, and IGBTs. ATLAS incorporates advanced physics models for mobility, band-gap narrowing, tunneling, together with defect and trap states. ATLAS is also flexible in the sense that the user can optimize the models to the user's liking. [16]

To simulate a device, the user needs to specify the device geometry, physical parameters, and the various physics models that will govern the operation of the device. ATLAS has a library of materials that the user can choose from to construct the device. The user is also allowed to change individual parameters of the materials.

A.2 ATLAS Installation

ATLAS is presently installed in the SOLARIS work environment in Packard Lab. Due to slow networking speeds, high mesh point simulations using ATLAS can take long times to finish. Shifting simulation software from the UNIX servers to the recently purchased desktop computers has been proposed, though not yet achieved, i.e. simulator package from Syborg.

A.3 Modeling a Structure in ATLAS

ATLAS is normally used in conjunction with the VWF Interactive Tools. These include Deckbuild, Tonyplot, DevEdit, MaskViews and Optimizer [16]. In this work, Deckbuild and Tonyplot were used to create, simulate, and visualize the modeled devices. Deckbuild provides the interactive run time environment. For specifying the device geometry, doping profiles, interfaces, and boundaries in ATLAS, a command file must be written and saved with the extension *.in.

The command file contains a sequence of statements first starting with the command, "go atlas". The mesh grid (calculation points) is defined using x and y coordinates. High concentrations of mesh points will provide good simulation accuracy but at the expense of calculation time; the trade-offs between accuracy/precision and simulation time is adjusted through the mesh grid. Once the mesh is specified, every part of the mesh must be assigned to be a particular material type, performed in the "region" statements. After the regions and materials have been specified, at least one electrode contact (max of 50) must be defined using the "electrode" statement. Finally, the doping distributions are specified in the "doping" command. To output and save the structure to a file, use the "save out" command and save the structure with the extension *.str. When your file is complete, you may stop ATLAS by using the "quit" command. An example code that specifies a RGSIT structure is given in the following section. The file name is etch0.05.in

A.4 Example of Modeling File for a RGSIT in ATLAS

```
go atlas

mesh

x.mesh l=-1.35  s=0.05
x.mesh l=-0.75  s=0.03
x.mesh l=-0.35  s=0.01
x.mesh l=0      s=0.02
x.mesh l=0.35   s=0.01
x.mesh l=0.75   s=0.03
x.mesh l=1.35   s=0.05


y.mesh l=0    s=0.05
y.mesh l=0.3  s=0.01
y.mesh l=0.35 s=0.01
y.mesh l=1.35 s=0.04
y.mesh l=1.7  s=0.4
y.mesh l=6    s=0.4

#eliminate columns x.min=0 x.max=4 y.min=1.1 y.max=4

region num=1 x.min=-0.4 x.max=0.4   y.min=0  y.max=0.35  material=a-SiC
region num=2 x.min=-0.75  x.max=0.75   y.min=0.35  y.max=1.35
material=a-SiC
region num=3 y.min=1.35  y.max=6
material=a-SiC
region num=4 x.min=-1.35 x.max=-0.4  y.min=0  y.max=0.35
material=oxide
region num=5 x.min=0.4   x.max=1.35   y.min=0  y.max=0.35
material=oxide
region num=6 x.min=-1.35  x.max=-0.75   y.min=0.35  y.max=0.4
material=oxide
region num=7 x.min=0.75   x.max=1.35   y.min=0.35  y.max=0.4
material=oxide


elec num=1 x.min=-0.25 x.max=0.25 y.min=0 y.max=0 name=source
elec num=2 bottom name=drain
elec num=3 x.min=-1.35    x.max=-0.75   y.min=0.35    y.max=1.35
name=gate
elec num=4 x.min=0.75  x.max=1.35   y.min=0.35    y.max=1.35  name=gate



doping uniform conc=4e15    n.type y.min=1.7   y.max=5
doping uniform conc=1.35e16 n.type y.min=1.35  y.max=1.7
doping uniform conc=1.35e16 n.type x.min=-0.75 x.max=0.75 y.min=0.35
y.max=1.35
doping uniform conc=1.35e16 n.type x.min=-0.4 x.max=0.4 y.min=0.3
y.max=0.35
```

```
doping uniform conc=1e19 n.type x.min=-0.4 x.max=0.4 y.min=0 y.max=0.3
doping uniform conc=1e19 n.type y.min=5 y.max=6

save outf=etch0.05.str master

tonyplot etch0.05.str

quit
```

A.5 Simulating the Modeled Structure

To simulate a saved device structure, *.str, another command file must be written and saved with the extension *.in. The electrode, material, and physics models and parameters can be adjusted in this file. The adjustable parameters are easy to change and listed in entirety in the ATLAS user's manual [16].

ATLAS uses several numerical methods for calculating the solutions to semiconductor devices. There are three different types of solution techniques; Gummel (de-coupled), Newton (coupled), and Block. From these techniques, ATLAS can calculate DC, AC small signal and transient solutions. Voltages must be defined on each of the electrodes. In simulations, the device starts with zero bias on all electrodes and solutions are obtained by stepping the biases from the initial equilibrium condition. Voltage step sizes must be limited otherwise convergence problems will arise.

An example command file for the simulation of a modeled device is given in the following section. The file name is etch0.05VG10.in

A.6 Example of Simulation File for a Modeled RGSIT in ATLAS

```
go atlas

Title Drain Sweep for SiC SIT For VG20
mesh inf=etch0.05.str

# specify the semiconductor material parameters for 4H-SiC
contact name=gate workfun=5.05
mater material=a-SiC taup0=20e-9 taun0=20e-9 eg300=3.25 affin=3.65
mater material=a-SiC mun0=450 mup0=100 eab=0.191 edb=0.065 vsatp=2e7
vsatn=2.2e7


models srh conmob analytic fldmob boltzmann incomplete ioniz print
numcarr=2 temperature=300
#mobility mref1n.watt=100 mref2n.watt=120 mref3n.watt=400
#mobility mref1p.watt=20 mref2p.watt=25 mref3p.watt=100


mobility material=a-SiC mu1n.caug=0.0 mu2n.caug=450 ncritn.caug=1.94e17
ncritp.caug=1.76e19 alphan.caug=0.0 alphap.caug=0.0 deltan.caug=0.61
deltap.caug=0.34 mu1p.caug=15.9 mu2p.caug=100 betap=-2.5 gamman.caug=0
gammap.caug=0 betan.caug=-2
mobility material=a-SiC betan=1.2
mater material=a-SiC ETRAP=0.5 TAUN0=20e-9 TAUP0=20e-9 NSRHN=3e17
NSRHP=3e17

#interface x.min=-0.75 x.max=-0.35 y.min=0.35 y.max=0.35 QF=1e14
#interface x.min=0.35 x.max=0.75 y.min=0.35 y.max=0.35 QF=1e14


output flowlines e.lines e.field e.mobility h.mobility e.velocity

solve init
method gummel newton trap
solve vgate=-0.1 vstep=-0.1 nstep=9 name=gate
solve vgate=-1.2 vstep=-0.2 nstep=19 name=gate
solve vgate=-6 vstep=-0.5 nstep=15 name=gate
solve vgate=-10 outf=etch0.05VG10.str master


method gummel newton trap
log outf=etch0.05VG10.log master
load inf=etch0.05VG10.str master
solve vdrain=0.01 vstep=0.1 vfinal=4.5 name=drain
solve vdrain=5 vstep=0.25 vfinal=10 name=drain
save outf=etch0.05VG10VD10.str master
solve vdrain=11 vstep=1 vfinal=19 name=drain
solve vdrain=20 vstep=5 vfinal=50 name=drain
save outf=etch0.05VG10VD50.str master
solve vdrain=55 vstep=10 vfinal=105 name=drain
save outf=etch0.05VG10VD105.str master
```

```
solve vdrain=110 vstep=10 vfinal=170 name=drain
save outf=etch0.05VG10VD170.str master
solve vdrain=175 vstep=10 vfinal=225 name=drain


save outf=etch0.05VG10VD225.str master
tonyplot etch0.05VG10.log

quit
```

A.7 Viewing of Simulation Results

The output I-V characteristics of a simulated device is saved into a pre-named file with the extension *.log. Additionally, the structure of a device can be saved during mid-simulation to a file with extension *.str. This provides a 'snap shot' of the device at a particular bias point. Both the I-V characteristics, *.log, and the device structures, *.str, can be viewed using Tonyplot.

Tonyplot plots the I-V characteristics saved in the *.log files and the device structure saved in the *.str files. Tonyplot provides the option of viewing the doping profiles, electric-field strengths, potential distributions, current flows, electron velocities, etc. of the device structure. Using Tonyplot, it is also possible to create 1-D cutlines and 2-D and 3-D contour plots.

In conclusion, the simulation results seen in this thesis are plotted using Tonyplot and then cropped using Microsoft Photo Editor.

Vitae

James D. Fuerherm was born October 25, 1980 in New York City, NY to Mr. Authur Fuerherm and Mrs. Karen Fuerherm. He attended Lehigh University from August 1998 to May 2002 and graduated with a Bachelor of Science Degree in Electrical Engineering. He was also the recipient of the Philip Francis du Pont Memorial Prize in Electrical Engineering for being the highest-ranking senior in electrical engineering. Continuing his education at Lehigh University, he received admission to the Electrical Engineering graduate program in the Fall 2002 to pursue a Master of Science degree. He took the opportunity to become a research assistant at the Sherman Fairchild Center under the tutorage of Professor Marvin H. White. He is a member of the Sigma Phi Epsilon fraternity and the Sigma Xi honor society. He also plays tennis and enjoys weight-training.

END OF TITLE