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A study of metastability in CMOS latches

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A STUDY OF METASTABILITY IN CMOS LATCHES

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ABSTRACT

Digital systems are most conveniently designed as synchronous systems in which a clock provides for the timing of the individual components. In such systems, however, there is no way to prevent asynchronous inputs from changing near the active edge of the system clock, leading to errors in interpreting the sense of the input value.

Synchronizers, in the form of latches, have been used to provide the synchronous system with conditioned inputs having the proper setup and hold times. These synchronizers have, however, been known to fail through a phenomenon known as metastability.

After introducing the metastability problem, this thesis provides a theory for latch behavior during metastable operation. The theory is then applied to a D-type latch used as a synchronizer in low frequency applications. The example is then followed by a discussion of improvements in circuit design techniques that have been attempted in the past, followed by an in-depth look at four newer latch designs. The functionality of each design is presented, as well as their metastability recovery characteristics, their susceptibility to critical input timing, and their Mean Time Between Failures.

The preferred implementation is a D-type latch followed by a series of inverters, known as a Gabara Latch. It's mean time to failure can be several orders of magnitude greater than the simple D-latch.

1. INTRODUCTION

It is well known that synchronous systems, that is, systems which maneuver data using a single clock signal, are the most convenient to design. Any violation of the synchronous design style could greatly complicate design, increase the required analysis, negate the use of some powerful design aids, make useless several testability schemes, and in general, increase design time and the risk of system failure.

In a synchronous system [15,33], circuit operation is guaranteed provided it is physically correct and setup and hold restrictions are met at all flip-flops. Also, the designer need not be concerned about combinatorial logic transients (glitches) unless they become an input to a flip- flop near its active clock edge. Propagation delay through the combinatorial logic circuit is, however, a crucial design criterion. The state of the system depends entirely on the state of the clocked elements (flip-flops). This simplifies the design, maintenance, and testing of the system. The outputs are predictable, given steady-state inputs, hence simplifying circuit troubleshooting. Finally, there exist computer algorithms which accurately analyze the behavior of synchronous systems, thus facilitating larger designs.

A synchronous system, however, imposes the requirement that its primary inputs must not change near the active edge of the main clock, since this would cause glitches and generally unpredictable system outputs.

Guaranteeing that asynchronous inputs do not change near an active clock edge is usually impossible considering that the the sending system is controlled by a clock which is out of phase and at a different frequency than the receiving system (figure 1.1a), or the sending system may be combinatorial, thus not be controlled by a clock (figure 1.1b), or there may be a large delay in the transmission line between the sending and receiving systems causing de-synchronization of the inputs to the receiving system (even though the two systems may have the same clock) (figure 1.1c). A practical instance of the above

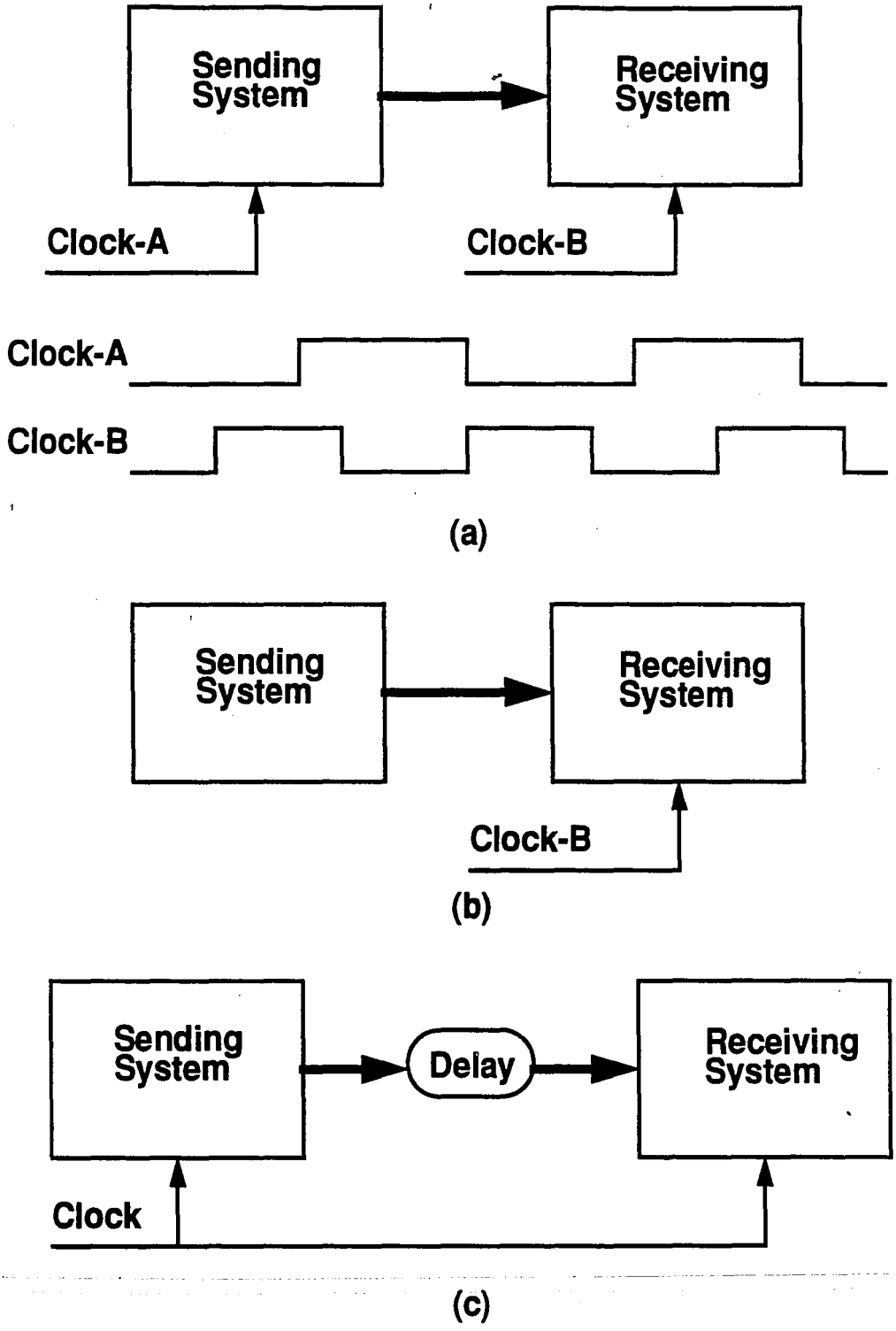


Figure 1.1. Asynchronous Systems.

scenarios is a microprocessor, in itself a synchronous system, which inevitably must interface with a keyboard, printer, or modem. Each of the latter sub-systems operates in a different time frame than that of the microprocessor.

The exchange of information across this interface presents serious design challenges and is typically handled by the use of a circuit called a "synchronizer", since it is intended to produce an output signal that is in synchrony with the master clock.

Synchronizers in the form of D-latches (flip-flops) have been used to strobe asynchronous inputs of the synchronous system and provide it with conditioned signals having the proper setup and hold times, hence incorporating the inputs into the receiving system's time frame. This has been accomplished, but not without problems.

Consider a system sending a digital signal (for example, a human finger), and a system receiving the signal and processing it (for example, the keyboard of a personal computer). The sending and the receiving systems have different "clocks". The receiving system must realign the digital signal supplied by the sending system to its own clock before further processing the signal. Digital data realignment is carried out by "capturing" the asynchronous input data into a D-latch timed by the clock signal of the receiving system.

When a transition of the data input occurs well away from the active edge of the clock, the circuit functions normally. However, since the sending and the receiving clocks can be different in frequency and in phase, the data transition can occur within a narrow window around the active edge of the clock. When this happens the latch's internal circuitry may not acquire enough information from the input at the time when the D-latch input is closed. This causes the flip-flop or latch output voltages at Q and its inverse, QN, to approach and linger at an unstable equilibrium value of about $V_{DD}/2$, referred to as the metastable state [1-31].

The metastable state can be the cause of system malfunctions in the form of synchronization failures. A synchronization failure due to metastability is said to occur when an undecided flip-flop with logically undefined outputs is sampled by other digital circuitry, thus propagating non- binary signals through binary systems. The non-binary state is clearly illegal since the synchronous system is only expecting binary states.

The synchronization failure of a flip-flop due to metastability occurs under critical input timing conditions, when narrow pulses (also referred to as runt pulses) occur on the clock input, or when inputs change simultaneously. These critical timing situations cannot be avoided, as explained above. On the other hand, synchronization failures due to metastability must be eliminated or at least kept to a minimum.

It is then clear that a solution which effectively deals with metastable operation is needed. The key is the design of a synchronizer which can resolve the metastable state and make the system more resistant to metastable operation.

In order to design such a synchronizer, an understanding of latch behavior before, during, and after metastable operation is required.

2. THEORY

Binary information implies elementary memory elements of a bistable nature -- one state denoting a logic "0", the other a logic "1".

A bistable element [44] is a regenerative circuit which can exist indefinitely in either of two stable states and can be caused to make an abrupt transition from one state to the other.

2.1 Stable States of a Bistable Element

A bistable element may be produced by interconnecting two inverters as shown figure 2.1. The output of each inverter is connected to the input of the other. If output Q of inverter I1 is a logic "1", then the input to inverter I2 is also a "1". As a result, the output of I2 is a logic "0" (QN=0). If QN=0, a "0" is present at the input of I1; the output of I1, therefore, is a logic "1". With no external signals, the circuit remains in its stable state with Q=1 and QN=0. The flip-flop can be forced to change its state by shorting the Q terminal to ground or by supplying a suitable trigger to the input of I1. If the trigger to I1 is a "high", the input to I2 will automatically become a "low", resulting in QN=1. After the trigger is removed, the output of the flip-flop remains at Q=0 and QN=1. This state prevails until another trigger signal forces a change of state. It may be concluded that Q equals a logic 0 or 1 when QN equals a logic 1 or 0 respectively.

Synchronization has been accomplished using such a bistable device (a latch or flip-flop). The most popular synchronizing element is the CMOS D-type latch.

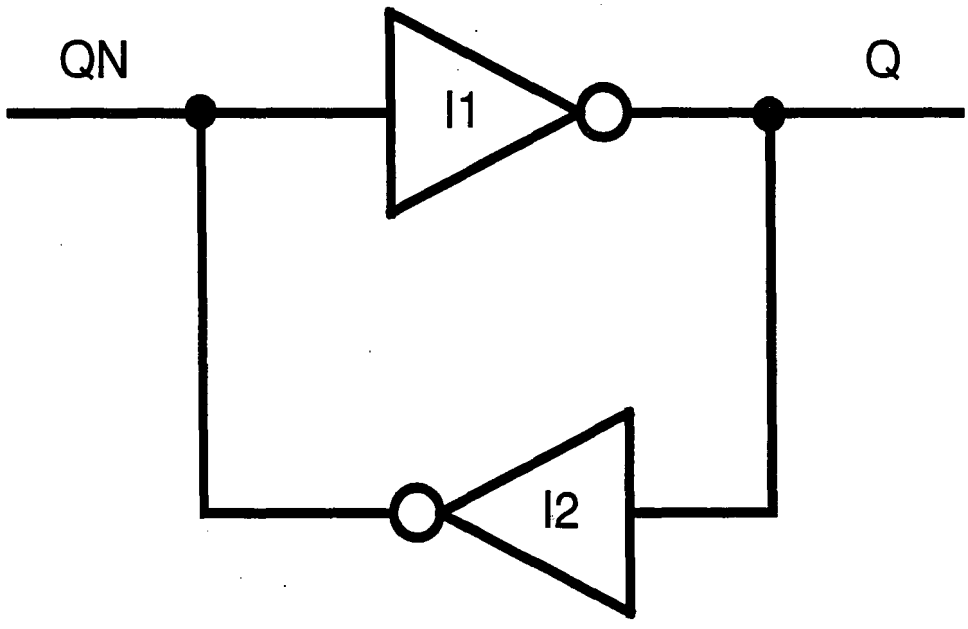


Figure 2.1. Bistable Element obtained by cross-coupling two inverters

2.2 CMOS D-latch operation

A CMOS D-latch (level sense), shown in figure 2.2, is used to store 1 bit of data. When CK is high and CKN is low, data D drives the latch, and node Q assumes the logic level of D, and QN the complement. Data D comes from other logic and must make a transition and settle before CK and CKN make down and up transitions, respectively. After the clock transition, input D is unable to further influence the state of the latch, and the latch is closed. The transition of the data must occur sometime before the clock transitions. The minimum time required to store the data is called the setup time. If the data transition occurs before the setup time, the value after the transition is stored in the latch. If the transition occurs after the setup time, the value before the transition is stored The latter case results in a logic error. The setup time may be different for up and for down data transitions. Figure 2.3 summarizes the positive level-sense D-latch operation.

2.3 Metastable State

Every bistable device must necessarily have a region of metastability. A flip-flop, like any other bistable system, can be described (figure 2.4) by some energy function, P(x), with two local energetic minima which represent the stable states of the system, and an energy barrier between the two stable states. The energy barrier must be overcome in order to switch the flip-flop from one state to the other.

Consider the mechanical system of an inverted pendulum (figure 2.5). The energy function, P(x), can be compared to the potential energy of the mechanical system which has two local minima, right and left, and its maximum in the center. The force of gravity holds the pendulum at a stable state in either the rightmost or the leftmost position. Switching from one state to the other can be accomplished by pushing the weight up to its maximum position and letting it fall onto the opposite stop.

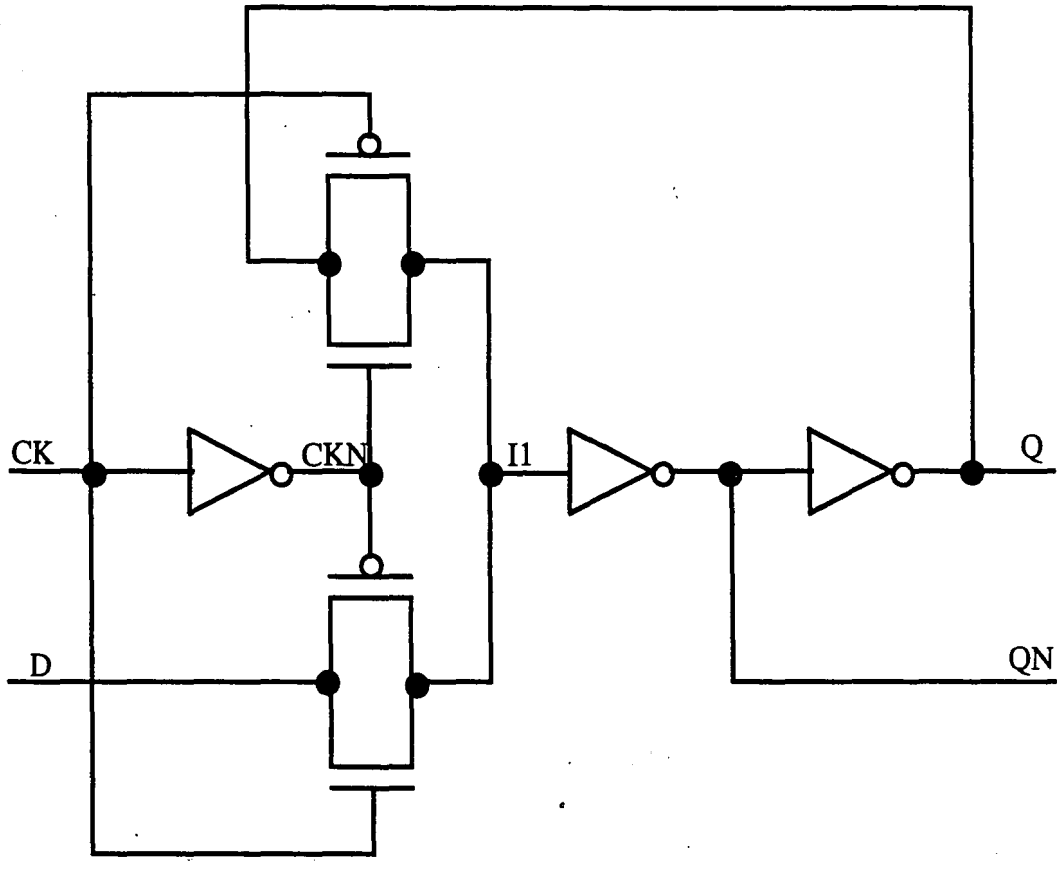


Figure 2.2. CMOS D-type Latch

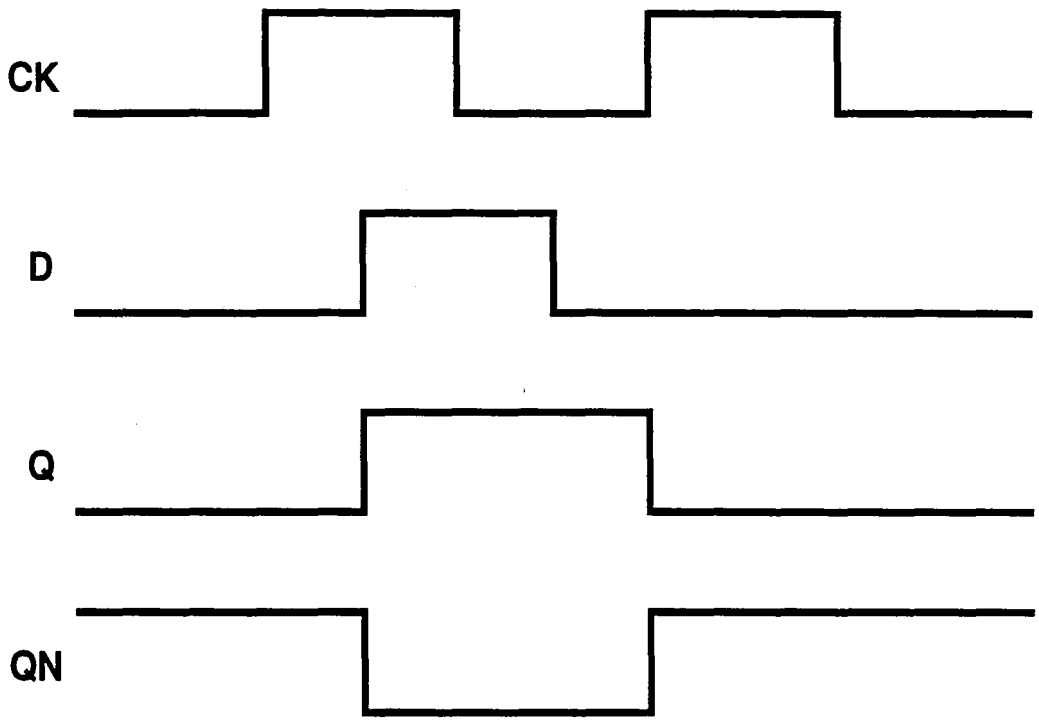


Figure 2.3. Level-sense latch operation.

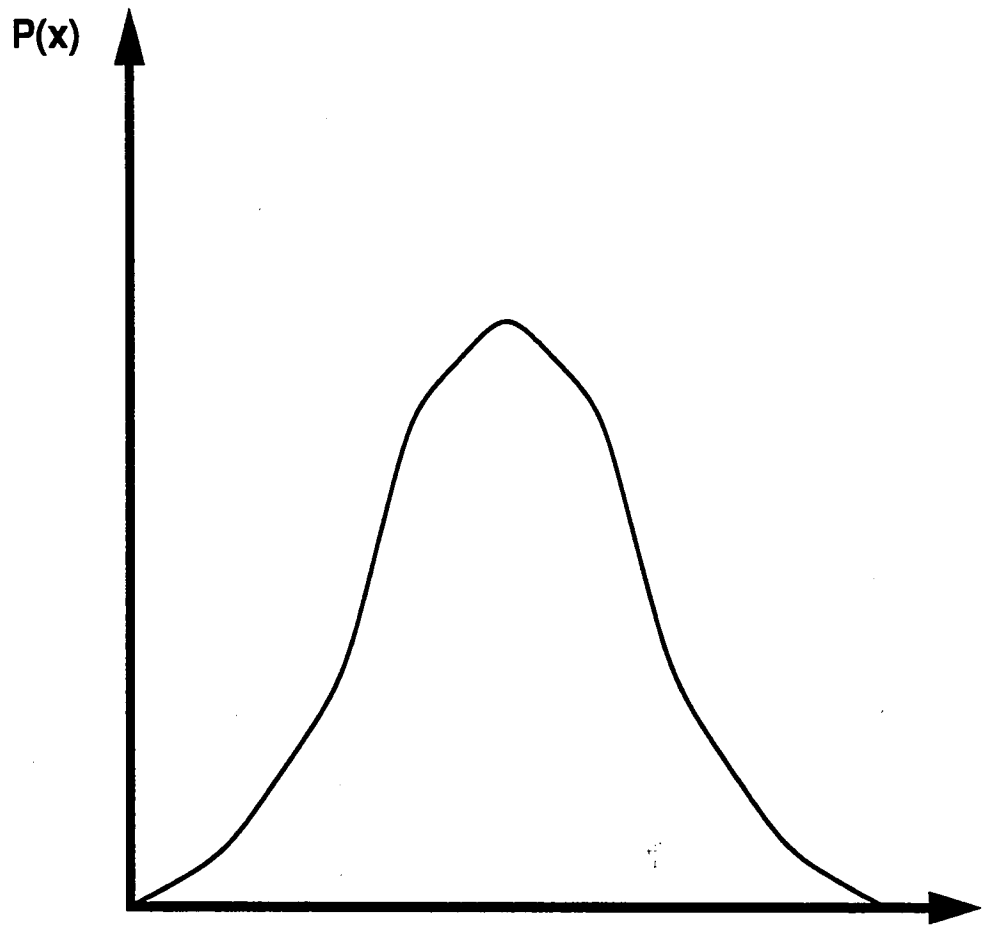


Figure 2.4. Energy function describing a flip-flop

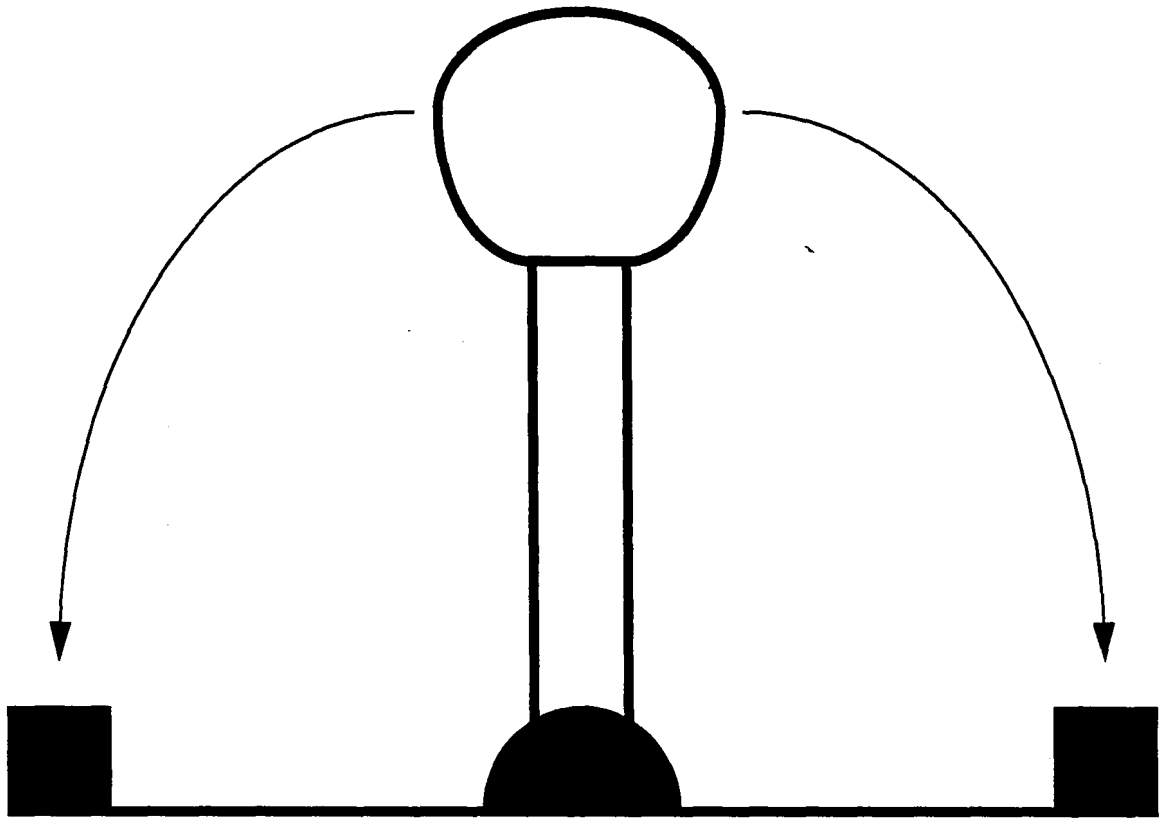


Figure 2.5. Mechanical system analog of a latch

If the pendulum is left in one of its stable states, given by the minima in figure 2.4, it will stay there indefinitely until enough energy is provided to surmount the potential maximum and to allow the system to re-equilibrate in the other potential minimum.

If the "right" amount of energy is supplied to the pendulum at one of its potential minima, there is a finite probability that it will rise to its potential maximum and linger there for an indeterminate amount of time before resolving to fall to either of its potential minima. During this event, the flip-flop is in neither of its stable minima, but half-way in between. Hence the term "meta" stable. The duration of this event is unpredictable. One can however compute the probability of entering the metastable state.

2.4 CMOS D-latch metastability and MTBF

As previously explained, the latch behavior of a flip-flop, can be described by a pair of static gates (inverters) tied back to back (figure 2.6), representing the non-linearity of the flip-flop, and a linear dynamic network (R, C) describing its dynamic behavior. This is an equivalent circuit for the latch which applies as long as it continues to operate linearly [11].

The possible states of such a latch are depicted in figure 2.7. If both inverters are identical, the latch is in the metastable state when $V_1 = V_2$.

The situation in which both inverters are operating as amplifiers and in which both output voltages are the same, is one of unstable equilibrium. To show the behavior of the flip flop near this unstable equilibrium or metastable region, the small signal model is invoked.

In figure 2.6, the gain A is the nominal gain of the amplifier, neglecting all capacitive loading. The resistance R is the output impedance of a stage. The capacitance C is the parallel combination of the capacitance seen looking into the input and any other parasitic capacitance.

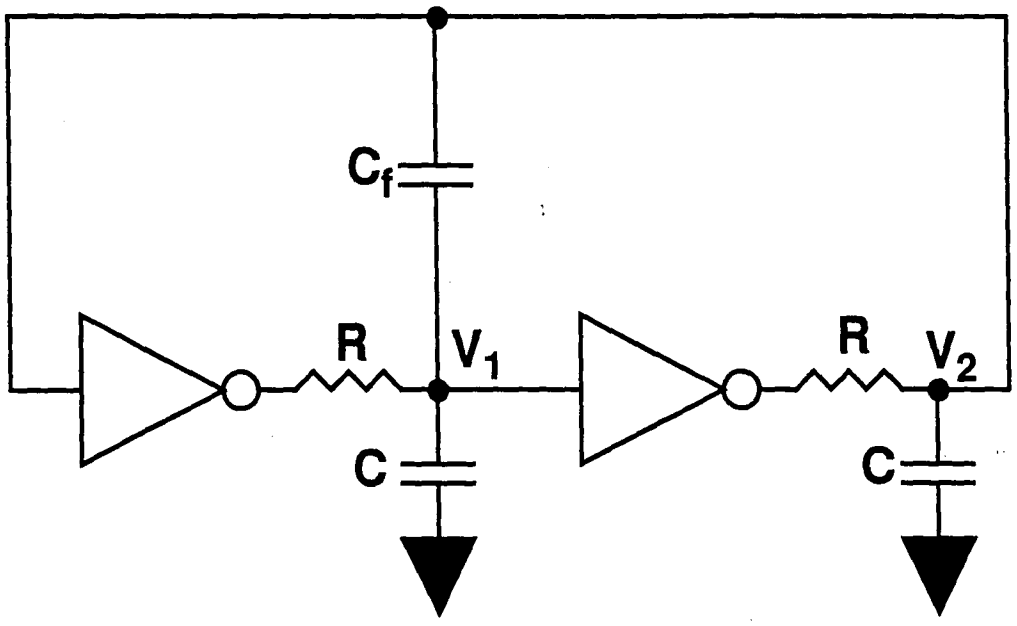


Figure 2.6. Equivalent latch circuit during linear operation.

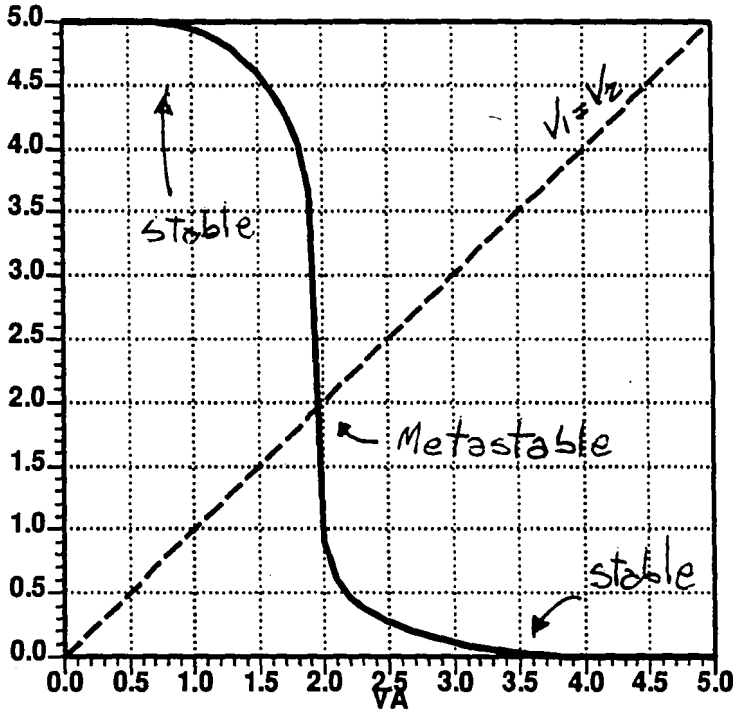


Figure 2.7. Possible states of cross-coupled inverters.

If V_1 and V_2 are, respectively, the voltages on the two capacitors with the polarities as in figure 2.6, Kirchhoff's current law yields

$$\frac{AV_2 - V_1}{R} - C\frac{dV_1}{dt} = 0 \qquad 2.4.1$$

and

$$\frac{AV_1 - V_2}{R} - C\frac{dV_2}{dt} = 0 \qquad 2.4.2$$

Equation 2.4.1 can be rewritten in the form

$$RC\frac{dV_1}{dt} + V_1 - AV_2 = 0 \qquad 2.4.3$$

and equation 2.4.2 can be rewritten in the form:

$$RC\frac{dV_2}{dt} + V_2 - AV_1 = 0 \qquad 2.4.4$$

Subtracting 2.4.4 from 2.4.3

$$RC\frac{d}{dt}(V_1 - V_2) + V_1 - V_2 + A(V_1 - V_2) = 0$$

and letting

$$V_{12} = V_1 - V_2 \qquad 2.4.5$$

then V_{12} represents the displacement of the node voltages of equal amounts and in opposite direction, which causes the regenerative action to take place and returns the flip-flop to one of the stable equilibrium states.

Replacing the expression for V_{12}, we get

$$RC\frac{dV_{12}}{dt} + V_{12} + AV_{12} = 0 \qquad 2.4.6$$

and rewriting this equation in a more familiar form we have

$$\frac{dV_{12}}{dt} + \frac{A+1}{RC}V_{12} = 0 \qquad 2.4.7$$

The solution to this type of linear differential equation

$$\frac{dy}{dt} + By = 0 \qquad 2.4.8$$

takes the form

$$y(x) = Ke^{-Bx} \qquad 2.4.9$$

therefore the general solution is

$$V_{12}(t) = Ke^{-Bt} \qquad 2.4.10$$

where

$$B = \frac{A+1}{RC} \qquad 2.4.11$$

If we let

$$\tau = \frac{RC}{A+1} \qquad 2.4.12$$

then τ represents the rapidity of the regenerative action, that is, how fast the flip-flop can snap out of metastability. The smaller the value of τ, the faster the latch will exit the metastable state.

The initial condition is found by considering $t=0$ the time at which the finite difference in voltage between V_1 and V_2 is such that metastability is produced at the outputs of the latch.

Replacing $t=0$ into equation 2.4.10 we get:

$$V_{12}(0) = K \qquad 2.4.13$$

The particular solution is then

$$V_{12}(t) = V_{12}(0)\exp\left[\frac{t}{\tau}\right] \qquad 2.4.14$$

This shows that the voltage difference between the two sides will grow exponentially with time as the flip flop comes out of the metastable region.

A latch should be designed in a way that establishes the exponential growth very quickly. In order for this to happen, the quantity

$$\tau = \frac{RC}{A+1}$$

must be minimized. This is achieved by maximizing the denominator, and minimizing the numerator.

By taking a closer look at the components of τ, one can see that A, the nominal gain of the amplifier, is basically its transfer function and is calculated as follows:

$$A = g_m R_0 \qquad 2.4.15$$

where g_m is the transconductance of the driving inverter, R_0 is the output impedance of the driving inverter, R is the output impedance R_0, and C is the total capacitance at the node being driven.

The total capacitance includes parasitic routing, fanout gate capacitance, and overlap capacitance between gate and source/drain regions. It is calculated using

$$C = C_L + C_R + C_M \qquad 2.4.16$$

where C_L is the fanout loading capacitance, C_R is the routing parasitic capacitance, and C_M takes into account the overlap capacitance.

The latter, however, is in essence a Miller capacitance since it couples the output of an amplifier to its input. The application of the Miller Theorem (figure 2.8) results in the multiplication of the factor

$$1 - A$$

to the overlap capacitance value, where A is the small signal voltage gain of the amplifier from equation 2.4.15. Figure 2.9 shows that the overlap capacitance of each inverter of the cross-coupled pair, C_{F1} and C_{F2}, is combined in parallel to obtain a lumped overlap capacitance, C_F. The Miller capacitance is therefore calculated by:

$$C_M = C_F(1 - A) \qquad 2.4.17$$

where C_F is lumped overlap capacitance calculated by summing the parallel capacitors C_{F1} and C_{F2} in figure 2.9:

$$C_F = C_{F1} + C_{F2}$$

By replacing the terms in the exponential part of equation 2.4.14 it can be rewritten as:

$$\frac{t}{\frac{RC}{A+1}} = \frac{t}{\frac{R_0[C_L + C_R + C_F(1 + g_m R_0)]}{g_m R_0 + 1}}$$

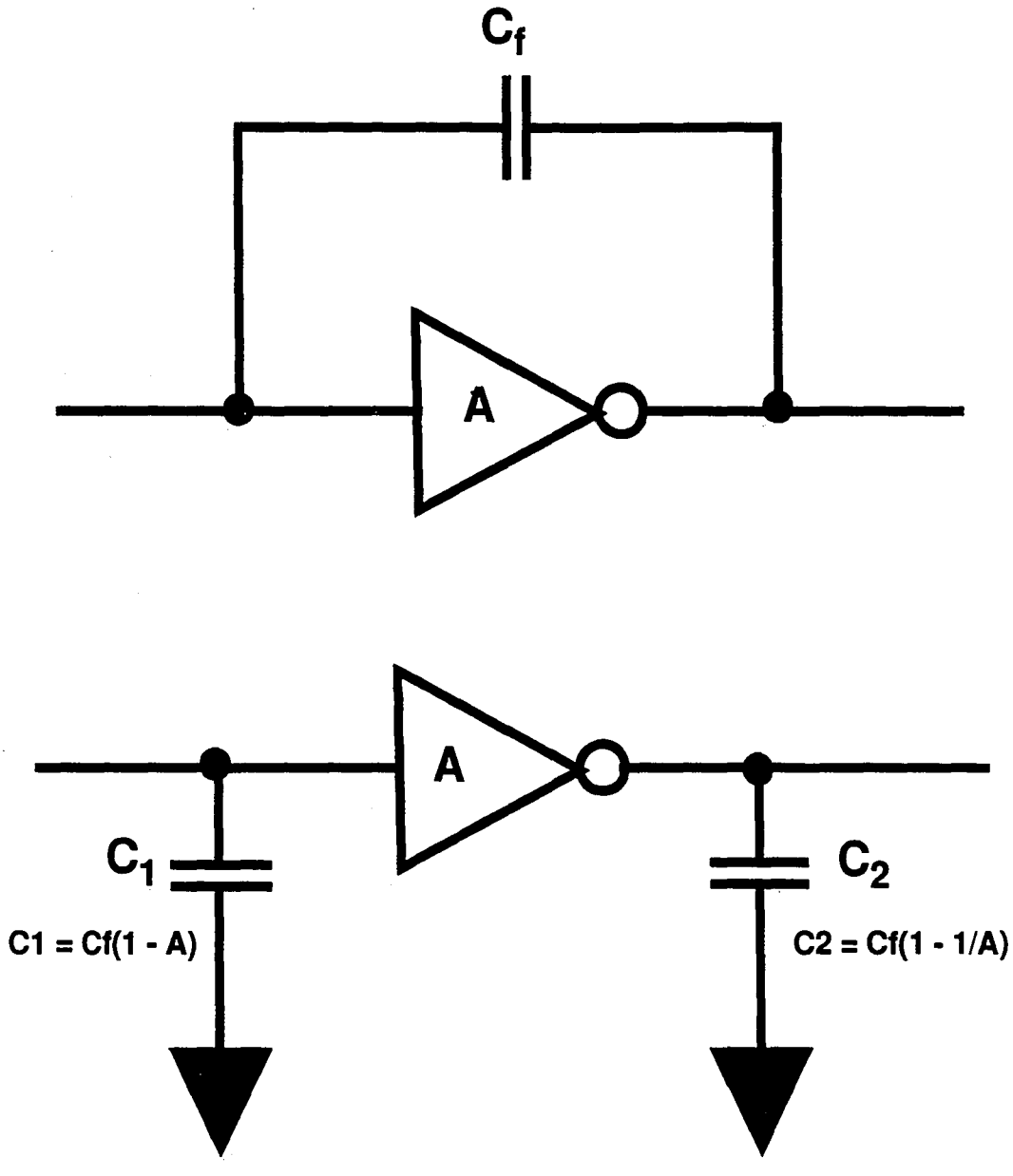


Figure 2.8. Application of the Miller Theorem.

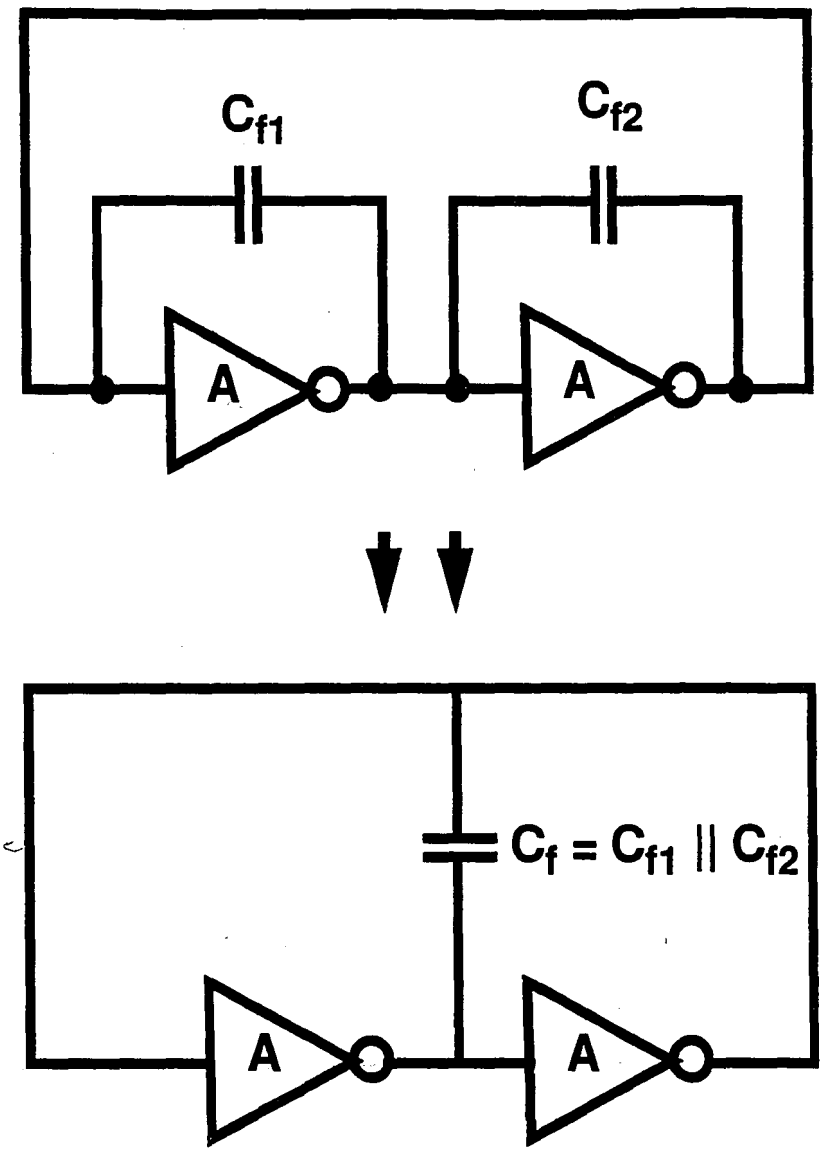


Figure 2.9. Effect of overlap capacitance

$$\approx \frac{t}{\frac{R_0(C_L+C_R+C_F+C_F g_m R_0)}{g_m R_0}}$$

$$= \frac{t}{\frac{R_0(C_L+C_R+C_F)+R_0 C_F g_m R_0}{g_m R_0}}$$

$$= \frac{t}{\frac{1}{gm}(C_L+C_R+C_F)+R_0 C_F} \qquad 2.4.18$$

Replacing the above expression into equation 2.4.14 we get a form which more closely resembles the physical parameters of the circuit:

$$V_{12}(t)=V_{12}(0)\exp\left[\frac{t}{\frac{1}{gm}(C_L+C_R+C_F)+R_0 C_F}\right] \qquad 2.4.19$$

Equation 2.4.19 describes the behavior of the cross-coupled inverter pair during the process of metastable decay, and shows that the exponential increase of the difference in V_1 and V_2 is dependent on g_m. Increasing the transconductance of the cross-connected inverter pair will increase the rate with which the flip-flop exits the metastable state. Decreasing the total capacitance at nodes 1 and 2 also helps the exponential increase of the difference in V_1 and V_2. $V_{12}(0)$ is the difference in voltage between nodes 1 and 2 at the beginning of the metastable state (at $t=0$, the time when the clock has closed the input data path). Figure 2.10 shows the generation of the metastable state when the input data changes within a critical time window.

From figure 2.10 we can see that the decision time t_D (the time it takes to attain solid digital voltage levels at the latch outputs) can be expressed as the sum of the propagation delay of the flip flop (t_{PD}) and the time to resolve the metastable state (recovery time t_R):

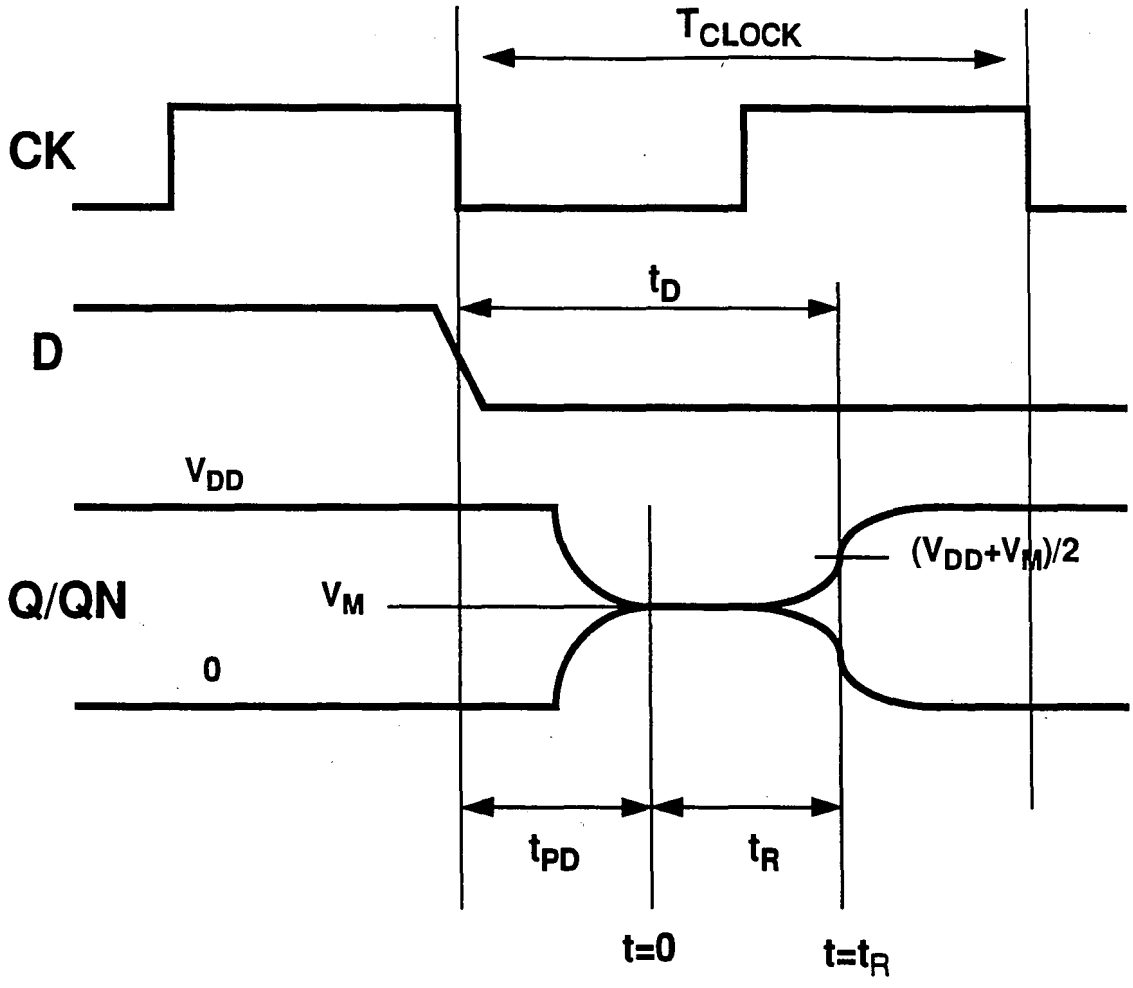


Figure 2.10. Generation of metastable state.

$$t_D = t_{PD} + t_R \qquad 2.4.20$$

The measurement points for t_R are here defined as the point where the latch outputs first reach the metastable voltage V_M ($t=0$ in figure 2.10), to the time point where the slope of the output voltage curve is at its greatest ($t=t_R$ in figure 2.10). The corresponding voltage axis points are V_M, which can be calculated using the DC saturation current equations of MOSFET's, and $(V_{DD}+V_M)/2$.

The parameter t_R is related to the latch during the metastable state. We can then substitute it into equation 2.4.19 to find $V_{12}(0)$, the difference in voltage between nodes 1 and 2 at the beginning of the metastable state:

$$V_{12}(t_R) = V_{12}(0)\exp\left[\frac{t_R}{\tau}\right] \qquad 2.4.21$$

from which $V_{12}(0)$ is derived as

$$V_{12}(0) = V_{12}(t_R)\exp\left[-\frac{t_R}{\tau}\right] \qquad 2.4.22$$

However, since $t_R = tD - t_{PD}$ we get

$$V_{12}(0) = V_{12}(t_R)\exp\left[-\frac{t_D - t_{PD}}{\tau}\right] \qquad 2.4.23$$

From equation 2.4.23 we can derive the decision time t_D

$$t_D = t_{PD} + \tau \ln\left[\frac{V_{12}(t_R)}{V_{12}(0)}\right] \qquad 2.4.24$$

This relationship shows that as $V_{12}(0)$ decreases, the time it takes the latch to resolve the metastable state increases. That is, the closer the voltages at nodes 1 and 2 are, the longer it takes a latch to recover

from the metastable state.

The decision time, t_D, can be specified as a system requirement, thus enabling the calculation of $V_{12}(0)$. Then, if the nodal voltage difference is less than $V_{12}(0)$ it will take longer than t_D to resolve the metastable state. $V_{12}(0)$ can therefore be considered a metastable voltage window δ_V.

A small difference in voltage between nodes 1 and 2 resulting in the metastable state implies that the input data voltage was within the metastable voltage window at the time the clock closed the input data path (sample time). We can then relate the metastable voltage window to the time axis. Figure 2.11 shows this relationship. If we define the input data slew rate as

$$input\ data\ slew\ rate = \frac{V_{DD}}{t_{FALL}} \qquad 2.4.25$$

then the following relationship is valid:

$$\frac{V_{DD}}{t_{FALL}} = \frac{\delta_V}{\delta_T} \qquad 2.4.26$$

and therefore the metastable time window is

$$\delta_T = \delta_V \frac{t_{FALL}}{V_{DD}} \qquad 2.4.27$$

An asynchronous data transition has no correlation to the phase of the input clock; therefore, its probability density function is unity for one clock period (figure 2.12). The metastable time window is a slice of the clock period T_{CLOCK} and the probability that a data transition will occur within the critical window δ_T is

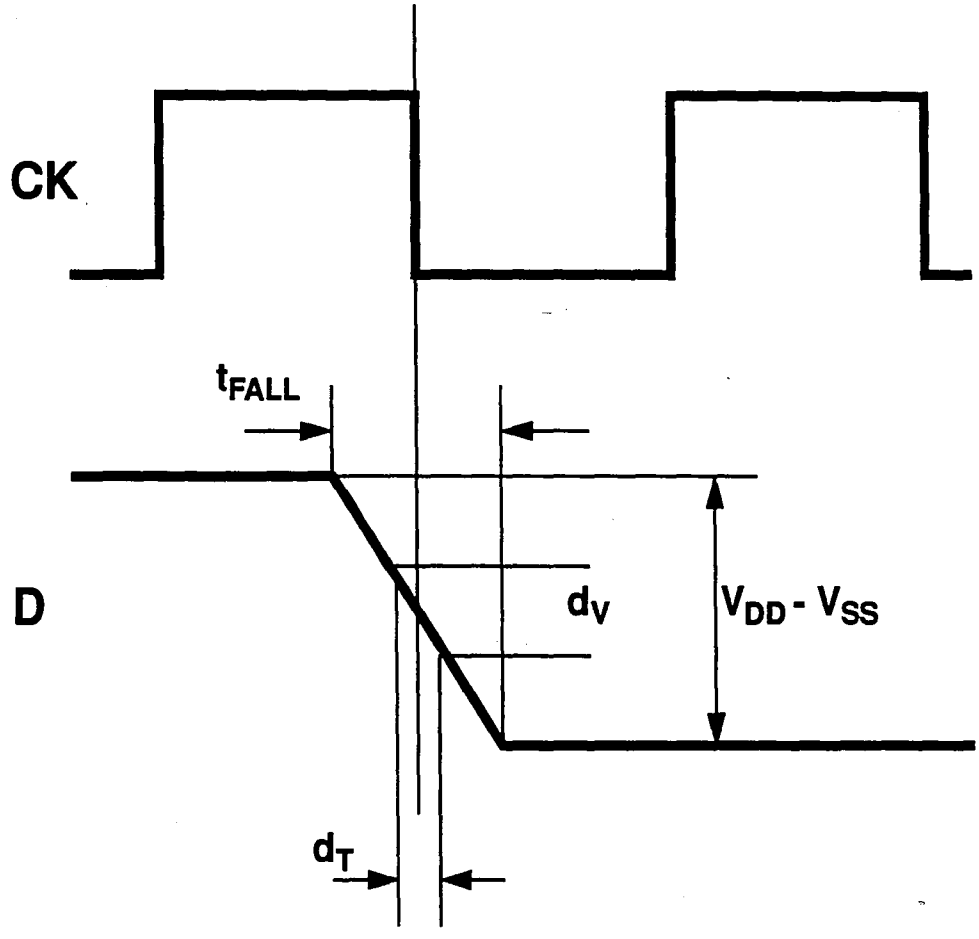


Figure 2.11. Relationship between d_T and d_V

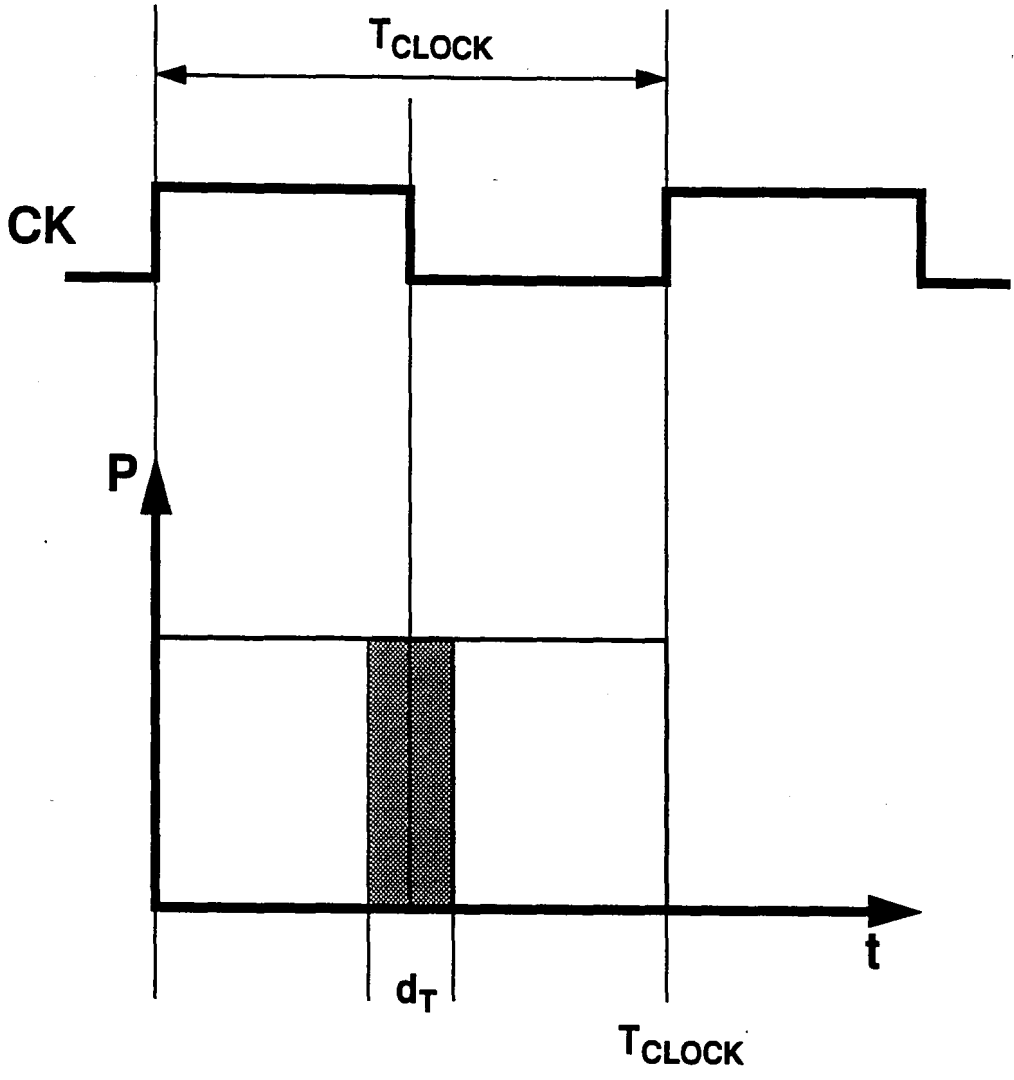


Figure 2.12. Probability density function of data transition

$$P = \frac{\delta_T}{T_{CLOCK}} \qquad 2.4.28$$

The number of probable occurrences of the metastable state depends on the frequency of the input data, and is represented by

$$N = 2Pf_{DATA} = 2\delta_T f_{CLOCK} f_{DATA} \qquad 2.4.29$$

the factor 2 is included since each transition of the data signal passes through the metastable voltage window, and there are 2 transitions per period.

The Mean Time Between Failures is defined as

$$MTBF = \frac{1}{N}$$

$$MTBF = \frac{1}{2\delta_T f_{CLOCK} f_{DATA}} \qquad 2.4.30$$

which is a measure of the reliability of a synchronizer.

3. EXAMPLE

The theory presented in the previous section will now be applied to a practical example: a positive level-sense D latch designed in the AT&T 1.75μm CMOS technology.

This standard cell has been used as a synchronizer for low frequency applications, and it serves well as an application vehicle for the above theory.

In this section, we will be calculating the reliability of the positive level-sense D latch as a synchronizer. Therefore we will conclude with an actual number for the Mean Time Between Failures (MTBF) which was presented at the end of the last section as the measure of synchronizer reliability.

Metastability is established when the internal nodes of the regenerative latch circuit are at the same voltage level. Referring to figure 2.2, these nodes are I1, QN, and Q. Therefore the metastable state occurs when

$$V_{I1} = V_{QN} = V_Q = V_M \qquad 3.1.1$$

where V_M is the metastable voltage.

The metastable voltage can be calculated using DC equations for the MOS devices of the inverters in the feedback loop. Let's assume that the metastable voltage is in the range $V_{DD}/2$, and that the threshold voltages for each transistor is $V_{TP} = 1v$ and $V_{TN} = 1v$. Referring to figure 3.1, we see the following

$$V_{DSP} = 2.5v$$
$$V_{GSP} = 2.5v$$
$$V_{TP} = 1v$$

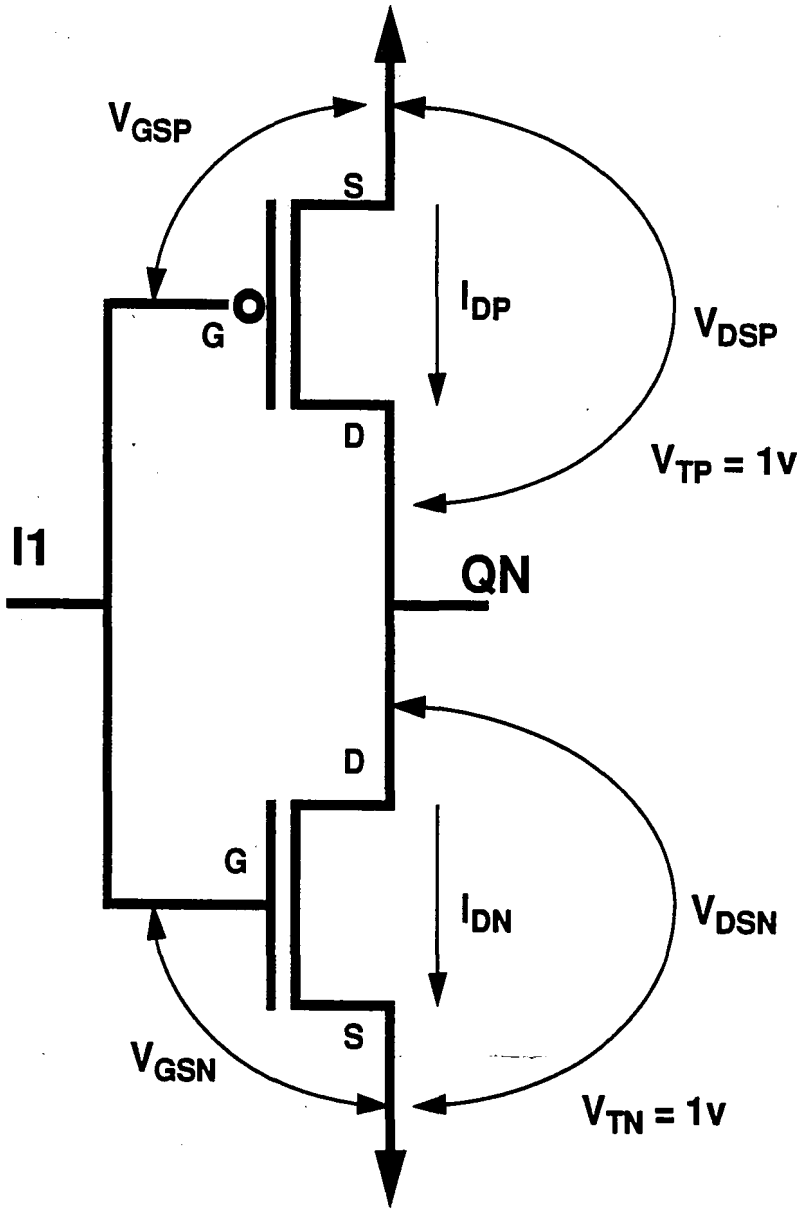


Figure 3.1. CMOS Inverter Voltages and Currents.

therefore the saturation condition for the P-transistor

$$V_{DSP} > V_{GSP} - V_{TP} \tag{3.1.2}$$

is satisfied and the P-transistor in is saturation. The same is true for the N-transistor

$$V_{DSN} = 2.5v$$
$$V_{GSN} = 2.5v$$
$$V_{TN} = 1v$$

$$V_{DSN} > V_{GSN} - V_{TN.} \tag{3.1.3}$$

With the two devices in saturation, we know that their drain currents are equivalent; therefore, by using the saturation equations for drain current

$$I_D = \frac{1}{2}\mu\frac{W}{L}C_{OX}(V_{GS} - V_T) \tag{3.1.4}$$

and equating them

$$I_{DP} = I_{DN} \tag{3.1.5}$$

we get an expression for the metastable voltage

$$V_M = \frac{\sqrt{k_P}\,V_{DD} - \sqrt{k_P}\,|V_{TP}| + \sqrt{k_N}\,V_{TN}}{\sqrt{k_N} + \sqrt{k_P}} \tag{3.1.6}$$

where

$$k_{[NP]} = \mu C_{OX}\frac{W}{L} = \mu\frac{\varepsilon_0\varepsilon_{OX}}{t_{OX}}\frac{w}{L} \tag{3.1.7}$$

The previous equations can be evaluated by using the AT&T $1.75\mu m$ CMOS parameters as an example

Parameter	Symbol	Value	Unit
width of P-transistor	WP	18	μm
length of P-transistor	LP	2.25	μm
width on N-transistor	WN	18	μm
length of N-transistor	LN	2.25	μm
P-channel mobility	μP	223	
N-channel mobility	μN	542.1	
oxide thickness	t_{OX}	2.5e-6	μm

and using the values

Value	Symbol	Value	Unit
power supply voltage	V_{DD}	5	volts
relative permittivity of SiO2	ε_{OX}	3.9	
permittivity of vacuum	ε_0	8.854e-14	Fcm^{-1}

in equation 3.1.6 to calculate the metastable voltage

$$V_M = 1.927v.$$

The manual calculation serves as a first order approximation of the metastable voltage. A circuit simulator can give us a more precise calculation of V_M, by simply performing a DC analysis of the latch circuit of figure 2.2. AT&T's ADVICE simulator yields a metastable voltage value of $V_M = 1.96943v$.

Once the metastable voltage is calculated, we can initialize the latch circuitry at V_M and use ADVICE to

calculate the voltage gain A and the output impedance R_0.

The ADVICE transfer function analysis provides the following values at the input voltage V_M:

$$A = -38.56$$
$$R_0 = 3.481 \times 10^4 \, ohms$$

The total nodal capacitance can be manually calculated using equation 2.4.16. The components of this equation are shown in figure 3.2. C_{DN}, C_{DP}, and C_R can be manually calculated from models extracted directly from the mask geometries. C_G, the gate capacitance, and C_{OV}, the overlap capacitance, must be calculated using the transistor dimensions and processing model parameters. From the manual calculation

$$C_T = 0.914 pF.$$

We now have the components necessary to calculate the regeneration factor τ using equation 2.4.12:

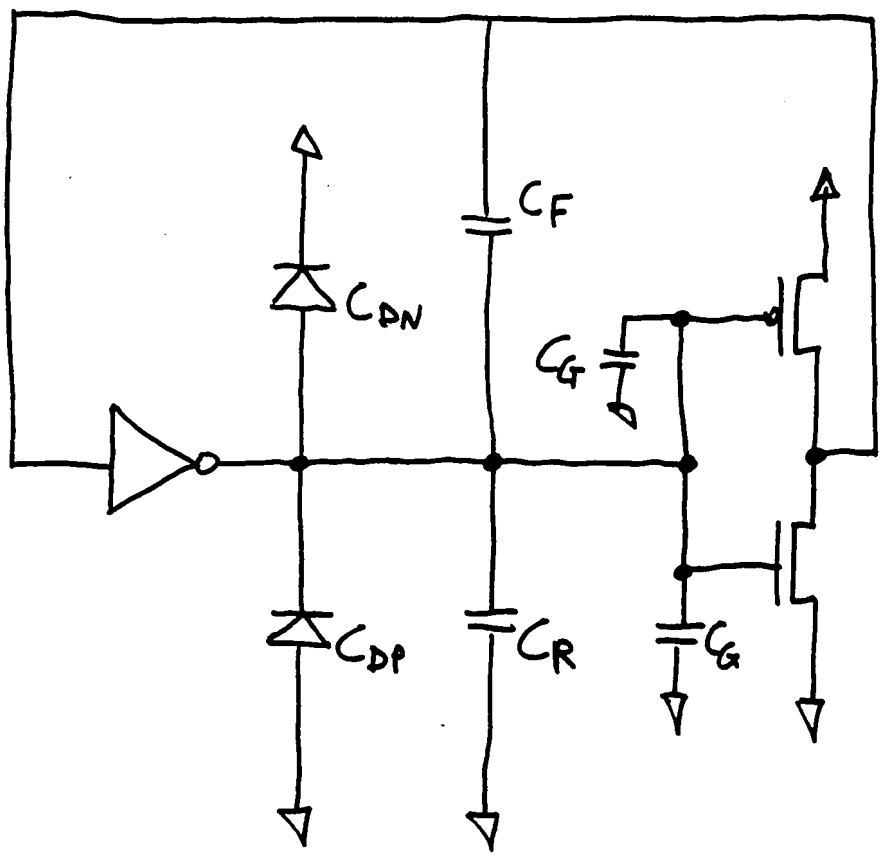
$$\tau = \frac{RC}{A+1} = \frac{R_0 C_T}{A+1} = 8.0454 \times 10^{-10} \, seconds$$

or $\tau = 0.805$ nanoseconds.

The calculation of the metastable voltage window necessitates some basic system requirements. Suppose we're concerned with synchronizing keyboard input with the CPU of a high powered personal computer running at 25Mhz, then the clock frequency is

$$f_{CLOCK} = 25 \times 10^6 \, Hz$$

and the period is



$$C_F = 2(C_{OVN} + C_{OVP})(1 - A_V)$$

Figure 3.2. Total nodal capacitance components

$$T_{CLOCK} = \frac{1}{f_{CLOCK}} = 40ns$$

The decision time required by the system should take into account circuit dependencies. To illustrate this point, figure 3.3a shows an example of a circuit which employs a synchronizer at the front end followed by some combinatorial logic and another latch. Figure 3.3b shows the possible timing of this circuit.

The synchronizer (FF1) must resolve the metastable state before it is sampled at FF2 on the next clock cycle thereby constituting a synchronization failure. The timing components which delay this resolution are the synchronizer propagation delay (t_{PD}), the metastable state resolution time (t_R), the delay through the combinatorial logic (t_{CMB}), and the setup time of FF2 (t_{SU}).

Considering all these factors, a decision time allowance of half the clock period is enough to provide us good margin:

$$t_D = \frac{1}{2} T_{CLOCK} = 20ns$$

From the circuit simulation of the latch, the propagation delay is $t_{PD} = 2ns$.

The voltage level used for the measurement of the end of the metastable resolution time, $V_{12}(t_R)$, is the point following the metastable state where the slope of the latch output curve is the largest. This level is given by

$$V_{12}(t_R) = \frac{V_{DD} + V_M}{2}$$

$$V_{DD} = 5v$$
$$V_M = 1.96943v$$

so $V_{12}(t_R) = 3.4847 volts$.

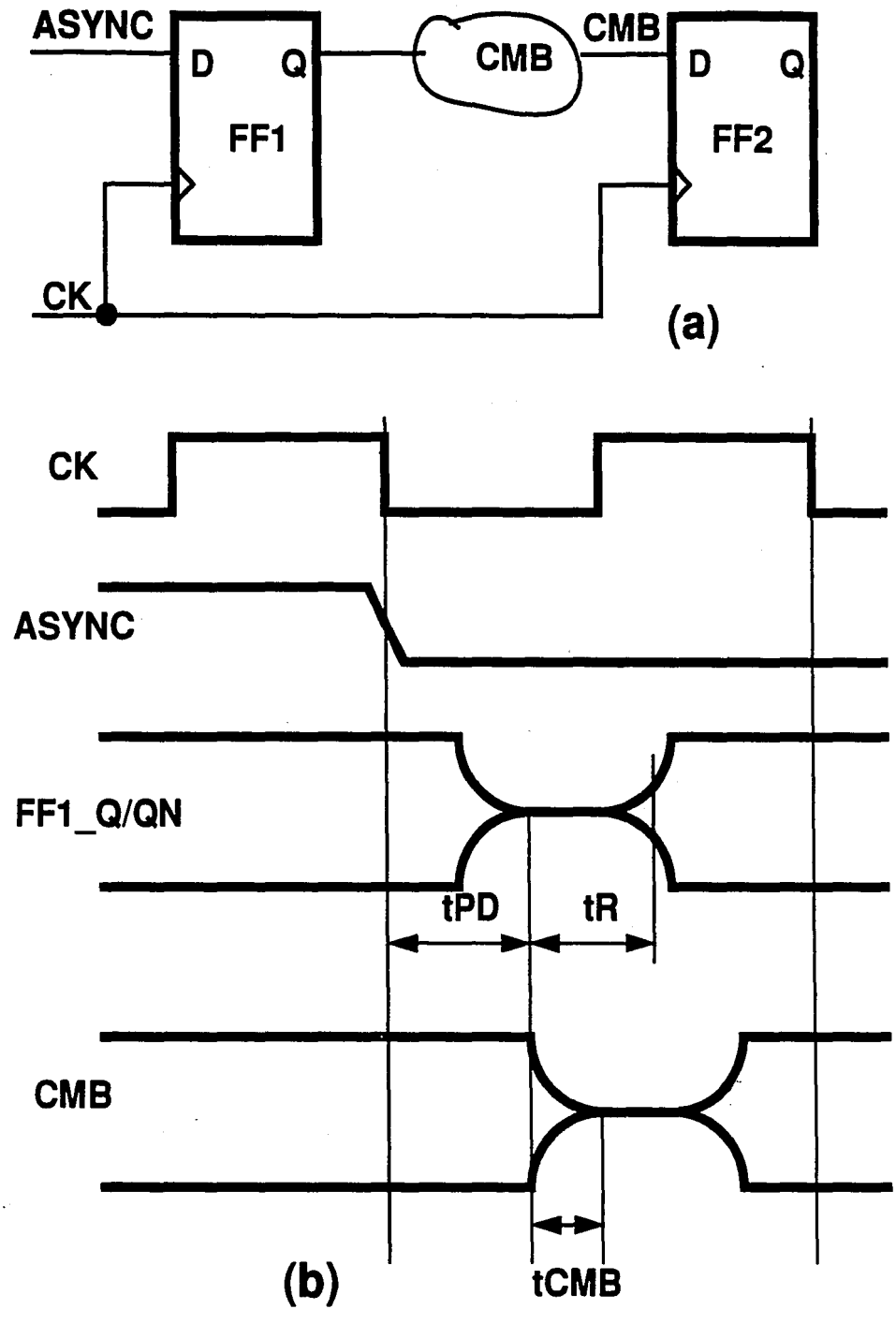


Figure 3.3. Example of synchronizer implementation and resulting waverforms

We can now find the metastable voltage window using equation 2.4.23:

$$\delta_V = V_{12}(t_R)\exp\left[-\frac{t_D - t_{PD}}{\tau}\right]$$

and thus, $\delta_V = 6.694\times10^{-10}\,volts$.

This value means that if the voltage difference between the internal nodes of FF1 is less than δ_V, it will take longer than t_D to resolve the metastable state.

The metastable time window can be calculated using equation 2.4.27:

$$\delta_T = \frac{t_{FALL}}{V_{DD}}$$

The asynchronous input data fall time is assumed to be 10 nanoseconds thus, $\delta_T = 1.3388\times10^{-18}$ seconds.

The calculation of the MTBF requires the input data frequency. Recall that the input data comes from the keyboard. Assuming an average typist typing 30 words per minute, and an average of 5 characters per word:

$$30\frac{wds}{\min}\times5\frac{chars}{wd}\times\frac{1\min}{60\,sec} = 2.5\frac{characters}{second}$$

This indicates that the keyboard is struck an average of 2.5 time each second or a input data frequency of $f_{DATA} = 2.5\,Hz$.

Then, using equation 2.4.30

$$MTBF = \frac{1}{2\delta_T f_{CLOCK} f_{DATA}}$$

we can calculate the Mean Time Between Failures

$$MTBF = 5.9755 \times 10^9 \, seconds$$

or, $MTBF = 189.48 \, years.$

Based on this failure rate, the synchronizer may seem acceptable until we consider a higher input data frequency, $f_{DATA} = 12 \times 10^6 \, Hz$, which happens to be the frequency of operation of the MIDI (Musical Instrument Digital Interface) board which is connected directly to system bus on a personal computer.

Using equation 2.4.30, the Mean Time Between Failures now becomes

$$MTBF = 1.2449 \times 10^3 \, seconds$$

and the synchronizer will probably fail every 21 minutes!

4. IMPROVEMENT TECHNIQUES

4.1 Discussion

An number of papers have been published, concentrating on device-level techniques [20,21,23,27,29] and gate-level techniques [5,25,27,28] to improve the performance of a synchronizer under metastability conditions, hence increase its reliability.

The device-level techniques concentrate on improving the Gain-Bandwidth product of the cross-coupled inverters forming the regenerative feedback loop of the basic latch. This is primarily accomplished through appropriate sizing of the N and P transistors of the inverters in the feedback loop with additional attention to minimizing the parasitic layout capacitances. The work of Flannagan [20] is valuable in the sense that it gave a comprehensive view of the device optimization strategy. The MOS capacitances in this work, however, are too simplified. The work of Sakurai [27] is based on that of Flannagan but takes into account the complexity of parasitic capacitances and concludes with a more accurate recommendation for optimal device size. Furthermore, Sakurai also shows that adding inverters in the feedback loop for the sake of increasing the loop gain does not improve the metastability problem.

The gate-level techniques present several ways of improving the reliability of synchronizers by attempting to detect or correct metastability externally to the synchronizing latch. Kleeman and Cantoni [25] have masterfully presented the problem and several ways to improve reliability, including a pausable clock by metastable detection (figure 4.1), extending the allowed settling time by cascading flip-flops (figure 4.2), including a Schmitt Trigger between cascaded flip-flops (figure 4.3), and using a majority-vote or redundant scheme (figure 4.4). The work by Horstman et al. [28] investigates cascaded

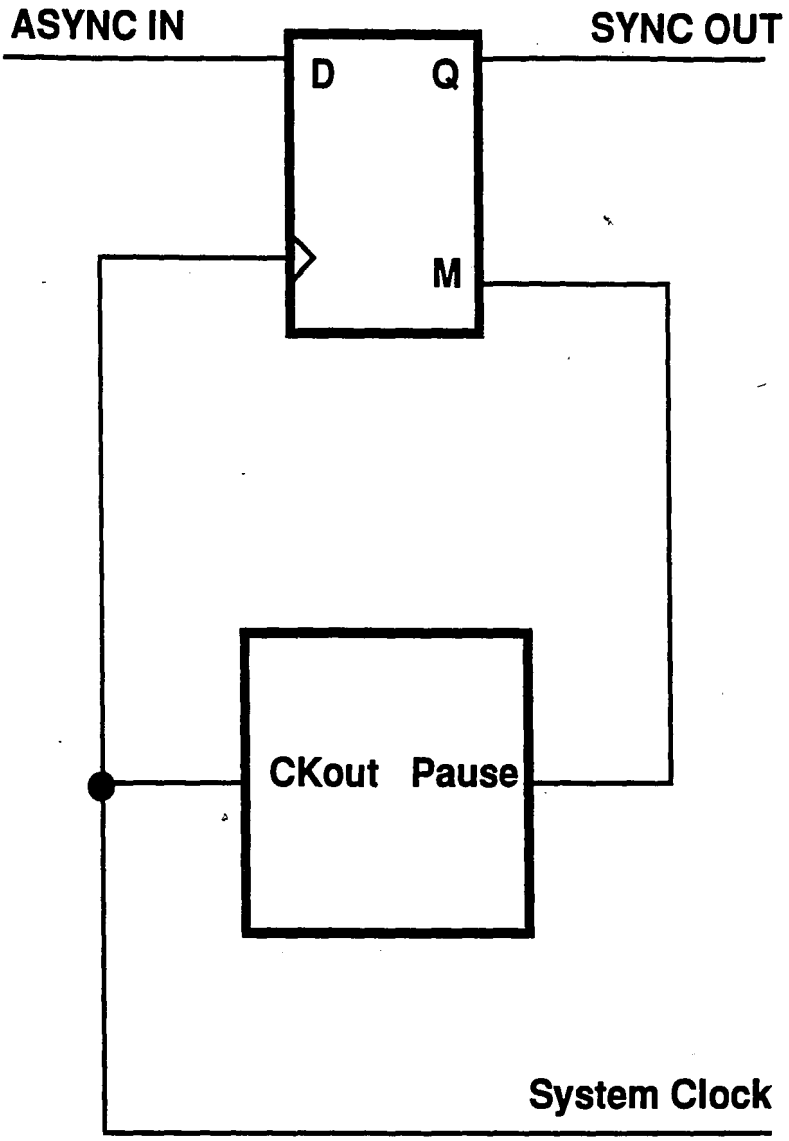
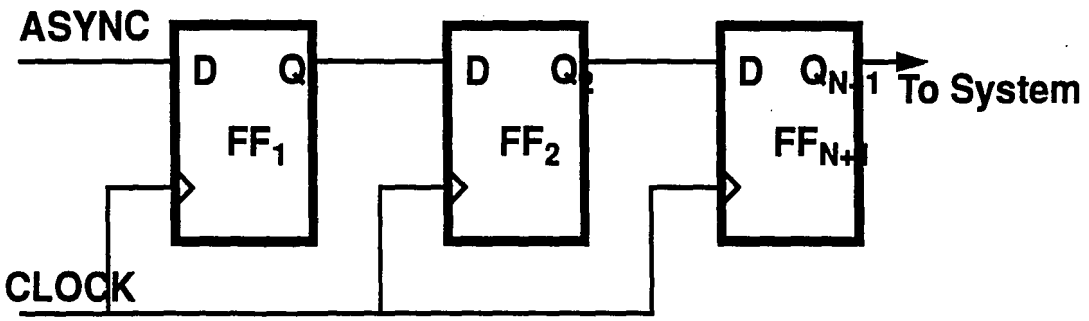


Figure 4.1. Use of metastable detection and pausable clock.



N+1 Cycles Needed for Synchronization

Figure 4.2. Block diagram of synchronizer consisting of cascaded flip-flops.

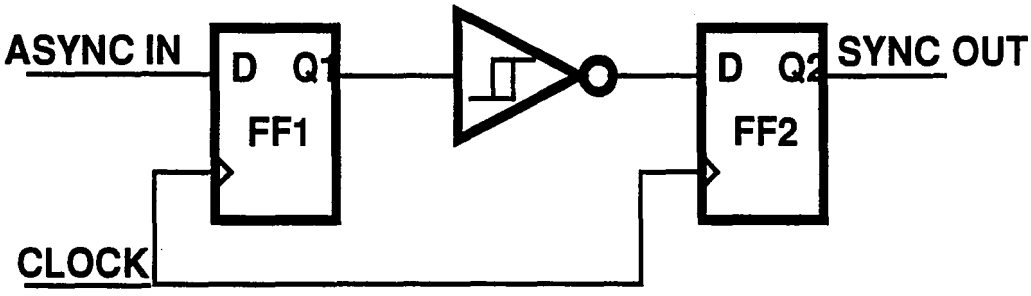


Figure 4.3. Schmitt Trigger synchronizer

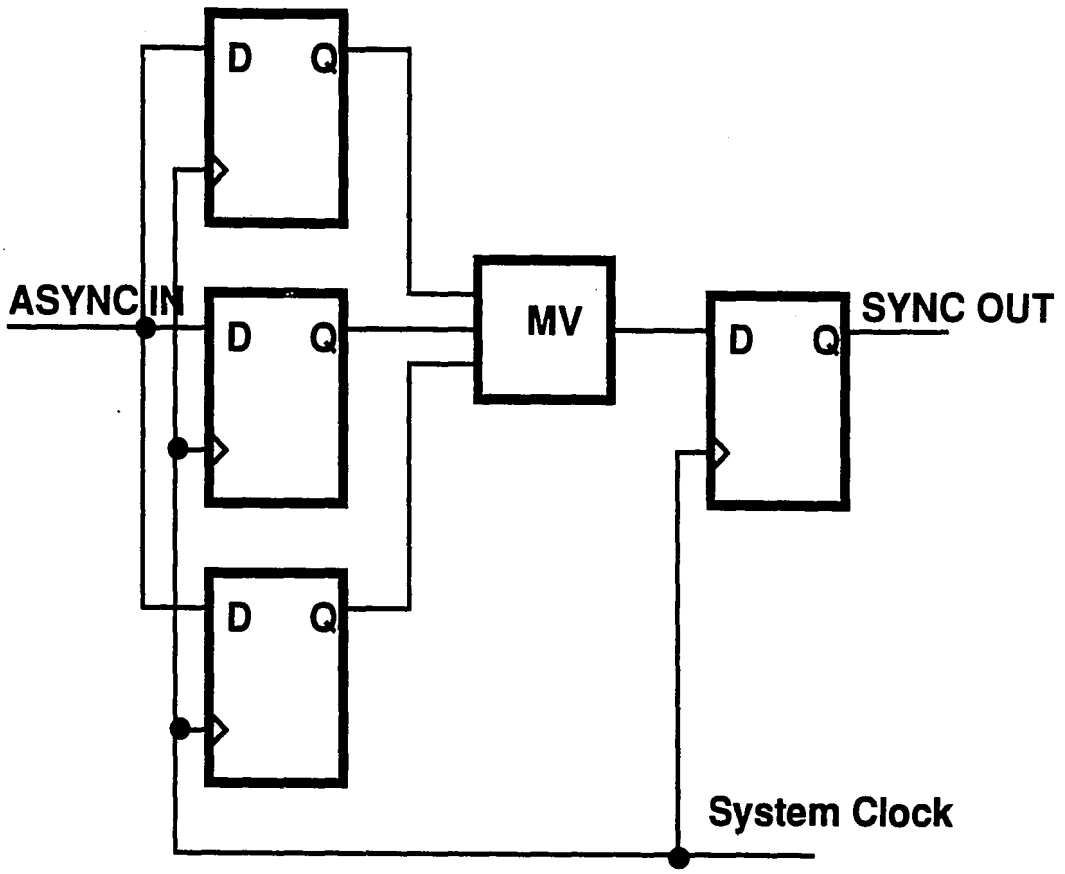


Figure 4.4. Use of redundant flip-flops and majority vote.

D-type flip-flops with a delay element on the clock path to the second flip-flop (figure 4.5). These techniques have been shown to improve the metastability problem to various degrees with the extended decision time being the best at lowering the probability of synchronization failure. However, all of the latter techniques require additional circuitry for each asynchronous input and multiple or extended clock cycles. The pausable clock technique in particular requires control over the main system clock, a rare commodity when dealing with system components such as VLSI chips (synchronous systems within themselves).

4.2 Improving the Basic D-type Latch

The following section deals with alleviating the metastability problem of the basic D-type latch. The circuit is commonly used as a synchronizer, and is used here as a building block for gate-level metastability improvement techniques. A latch which has increased MTBF due to metastability will further improve other methods which make use of this latch.

In order to make a meaningful comparison between the latch designs which will be presented, the same application of the is chosen: the synchronizer is used as in figure 4.6, with a clock frequency of 25 Mhz, and a data frequency of 2.5 Hz.

4.3 FD1S1A Positive Level Sense D-latch

The basic D-latch latch was introduced earlier in this paper, and provided a vehicle with which the Mean Time Between Failures (MTBF) was derived and calculated. It has been shown that for low frequency applications, the MTBF may be acceptable. The FD1S1A is an implementation of the basic latch design from the AT&T Standard Cell library, and is a possible solution for low frequency applications.

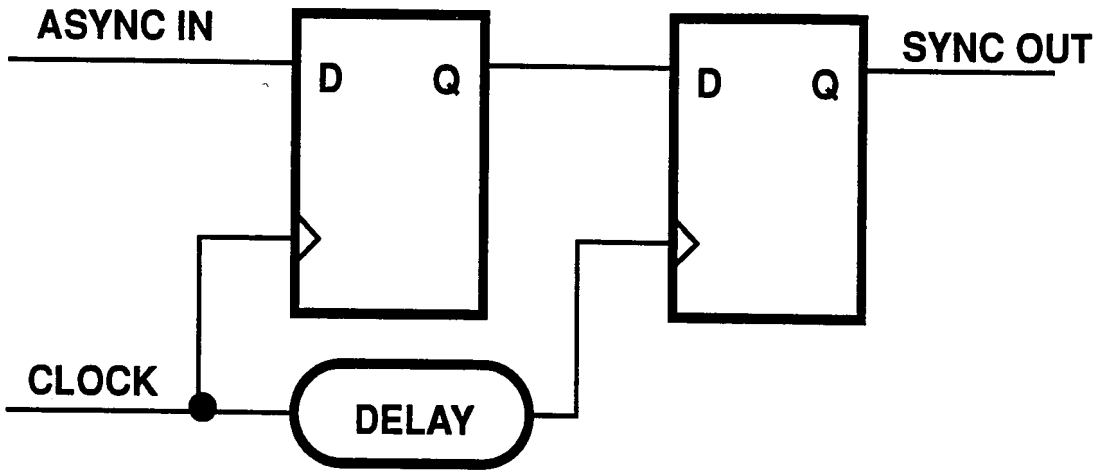


Figure 4.5. Use of delay element in clock line.

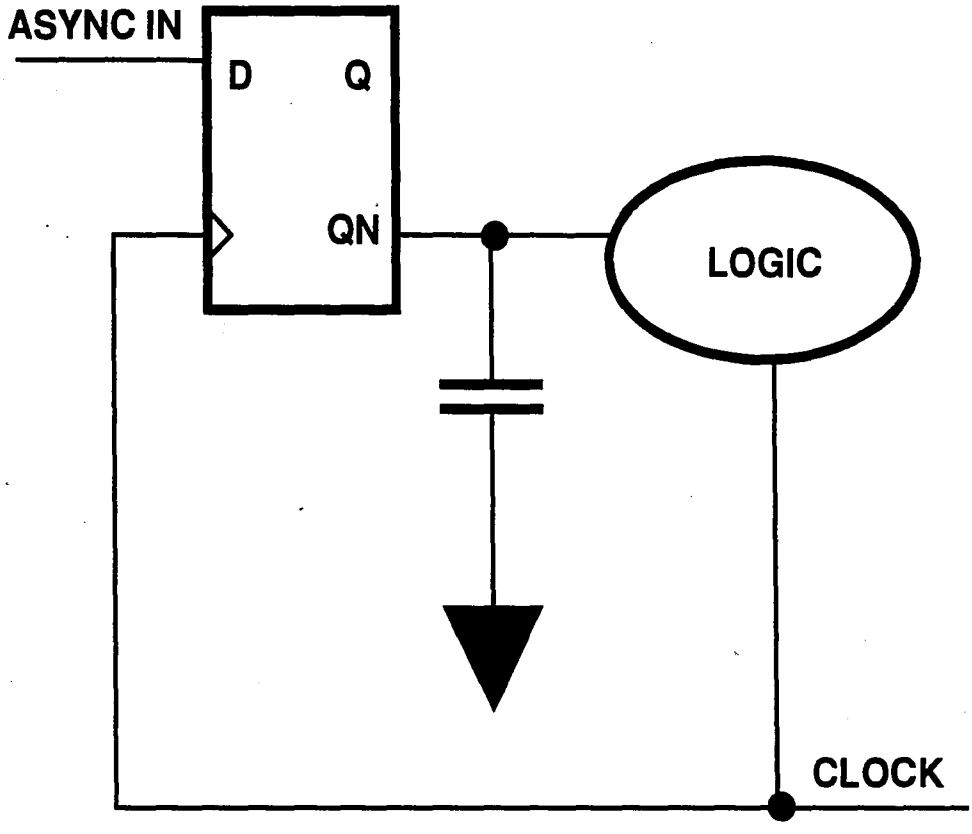


Figure 4.6. Example of application of the basic D-type latch synchronizer.

Functionality

Figure 4.7 shows a page from the AT&T 1.75um CMOS standard cell library catalog which defines the functionality of the FD1S1A and provides its schematic diagram. Figure 4.8 summarizes the operation of the latch by plotting the input and output waveforms as a result of a circuit simulation. Figure 4.9 shows the same simulation results and includes the internal nodes of the latch.

Recovery From Metastability

To demonstrate the characteristics of the latch around the metastable state, a transient analysis of the circuit can be performed. The input timing must be precisely controlled to trigger the occurrence of the metastable state, that is, the input data must be at the "correct" level during the metastability window. In practice, this is a lengthy trial-and-error procedure.

However, a fairly easy way to simulate the ability of the latch to deal with the metastable state can be obtained by assuming the latch to be initially at the metastable point. Figure 4.10 shows the result of a simulation of the metastable decay of the FD1S1A, that is, its recovery characteristics from the metastable state. This transient analysis was performed by biasing the internal nodes of the latch at the metastable voltage point V_M, which was calculated in chapter 3. The figure shows the rapidity with which the latch exits the metastable state. The voltage levels at Q and QN begin to diverge due to thermal noise [32,48], as modeled by the simulator, and also noise due to simulation error margin [48]. Once divergence is reached, formula 2.4.21 describes the behavior of the circuit.

Based on the waveforms shown in figure 4.10, the metastable state has a duration of several nanoseconds, therefore, the FD1S1A is prone to failures due to metastability.

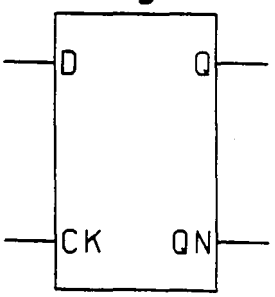
Static D-Type Flip-Flop

FD1S1A

Positive-level-sense
8 grids, 10 transistors

INPUTS: D, CK
OUTPUTS: Q, QN

Schema Symbol



Delay Information

	Input Signal Name	Setup Time (nS)	Path Propagation Delay (nS)				
			From INPUT	To OUTPUT	FANOUT		
					1	3	10
Area Optimized			D_0 D_1	Q_0,QN_1 Q_1,QN_0	7 7	11 11	27 24
Performance Optimized			D_0 D_1	Q_0,QN_1 Q_1,QN_0	6 6	10 10	22 20

VDD = 4.5 V, T = 100°C, WCS Process

Truth Table

INPUTS		OUTPUTS			
		OLD		NEW	
D	CK	Q	QN	Q	QN
X	0	0	1	0	1
X	0	1	0	1	0
0	1	X	X	0	1
1	1	X	X	1	0

X = Don't care.

Model for Motis Simulation

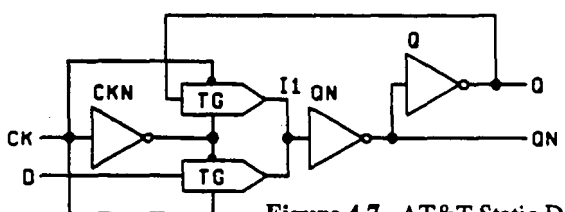


Figure 4.7. AT&T Static D-type Flip-flop - FD1S1A

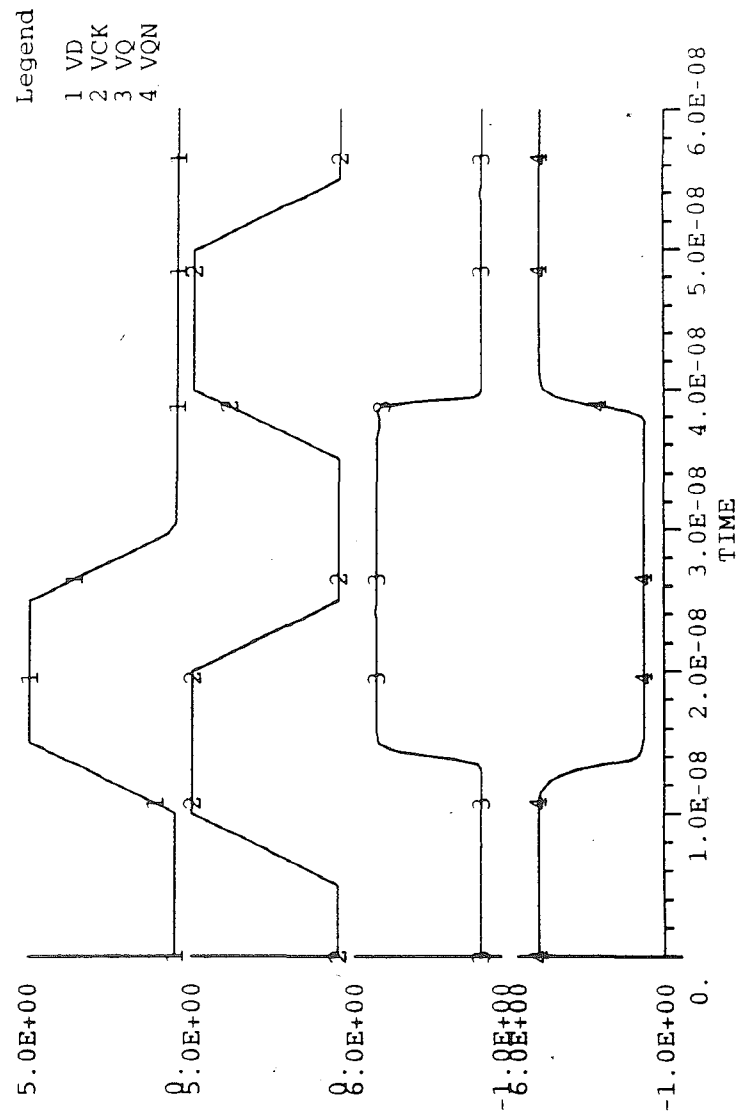


Figure 4.8. Functional Simulation of FD1S1A

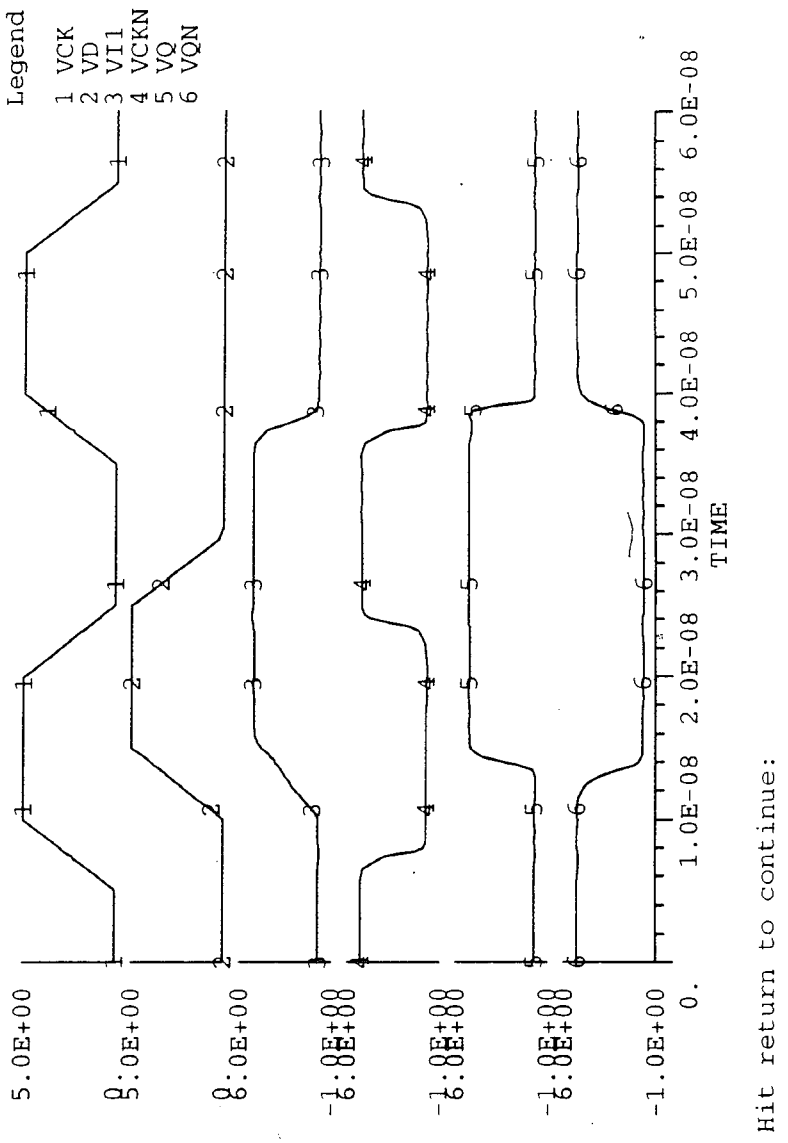


Figure 4.9. Simulation of FD1S1A including internal nodes.

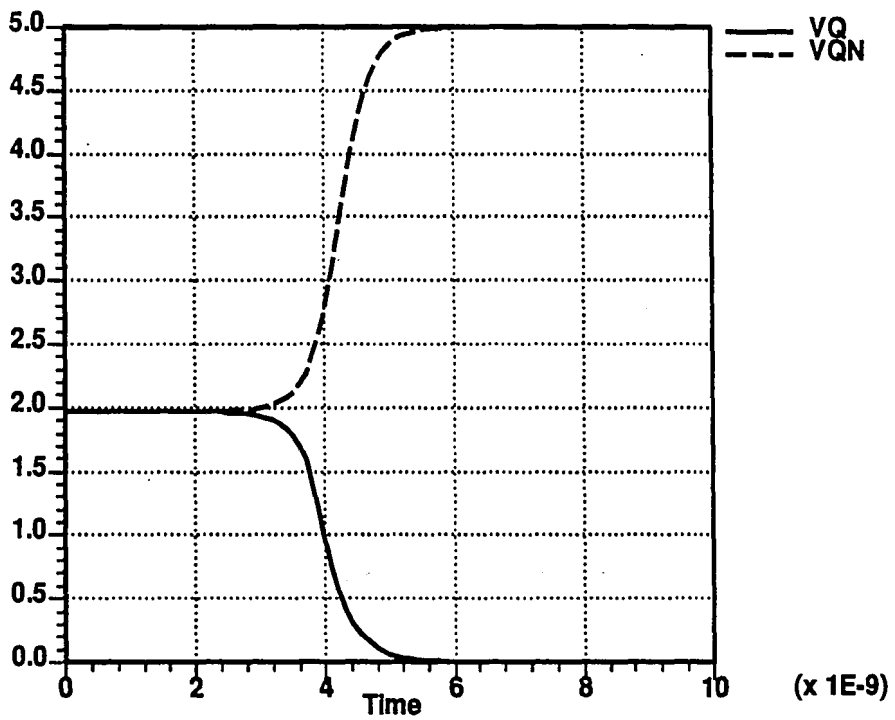


Figure 4.10. FD1S1A recovery characteristics

Simulation Under Critical Input Timing

A simulation using critical input timing can now show the behavior of the latch before, during, and after the metastable state.

Figure 4.11 shows the latch operation due to data switching within the metastability window. An actual metastable state is produced lasting several nanoseconds. Figure 4.12 shows the latch outputs and the relationship between the latch inputs. In this case, the critical relationship between the input data VD and the input clock VCK is established when the data leads the clock by exactly 3.5065 ns.

This time interval is the defined as a critical relationship since it is the delay between the input data and the input clock which causes a voltage level close to the metastable voltage V_M to be latched at the internal node I1. Once the input data path is closed, the high gain feedback loop propagates the metastable voltage very quickly around itself and the circuit behaves a depicted in figure 4.10 and its behavior is described by equation 2.4.21.

Mean Time Between Failures

The calculation of the MTBF for the FD1S1A has already been presented in section 3. It will be briefly discussed here.

In chapter 3 we found that the metastable voltage window for the FD1S1A depends upon the allowed decision time and the propagation delay of the data path, and is calculated using equation 2.4.23. The voltage window was found to be:

$$\delta_V = 6.694 \times 10^{-10}\ volts$$

Assuming an input data fall time of 10 nanoseconds, the metastable time window is calculated from

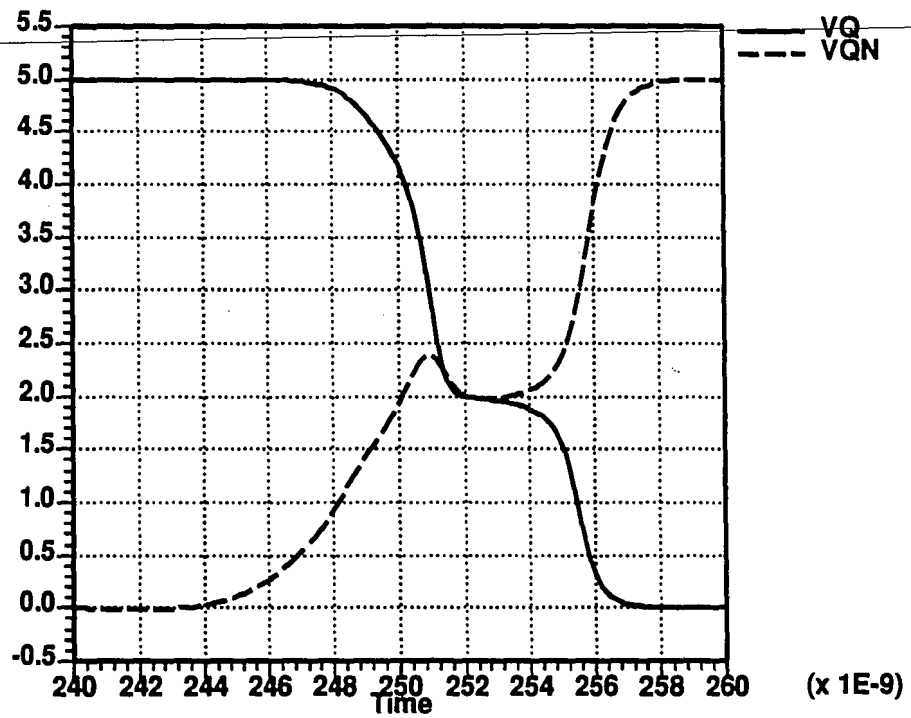


Figure 4.11. FD1S1A under critical input timing

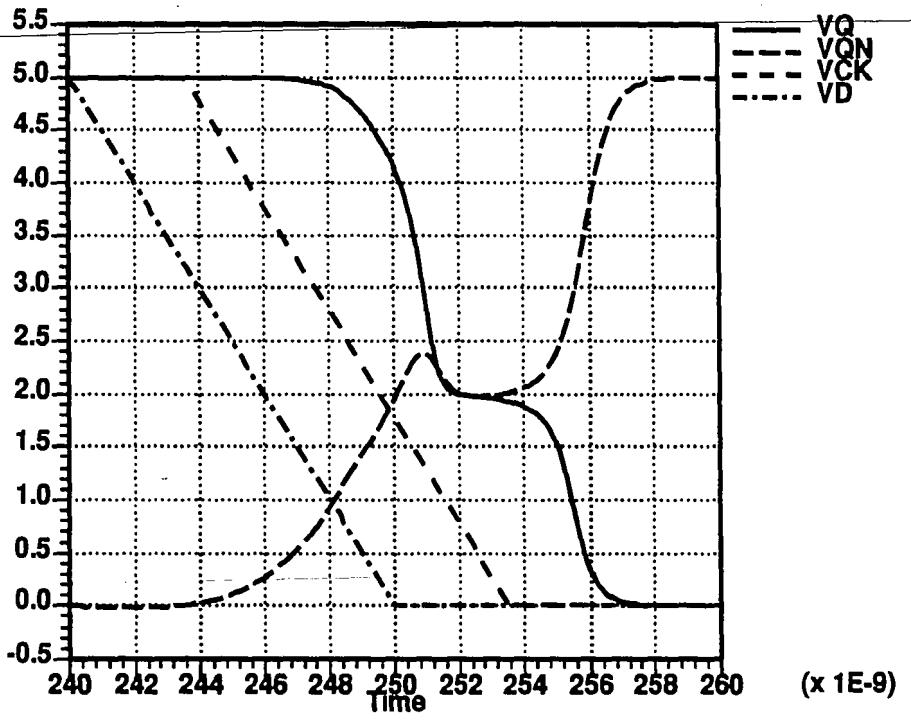


Figure 4.12. Clock and Data added to display

equation 2.4.27, and is

$$\delta_T = 1.3388 \times 10^{-18} \, seconds$$

The metastable time window is a component of equation 2.4.30 which yields the MTBF. The other components of the equation are the clock frequency, $f_{CLOCK} = 25 \times 10^6 \, Hz$, and the data frequency, $f_{DATA} = 2.5 \, Hz$.

Using these values, the MTBF for an FD1S1A is

$$MTBF = 5.9755 \times 10^9 \, seconds$$

or, $MTBF = 189.48$ years.

4.4 Gabara Latch Circuit

The FD1S1A has reasonable MTBF as a synchronizer when used in low frequency applications, that is, low input data frequencies. However, these implementations of low frequency synchronizers are continually decreasing as the evolving VLSI technologies enable faster and faster circuits. A more reliable circuit is needed at higher frequencies. The Gabara Latch [31], named after the the original designer, is a level-sense D-type latch which has been incorporated in the design of an Application Specific Integrated Circuit (ASIC) for broadband switching operating at 180Mhz. In that application, the MTBF due to metastability was increased from 4 seconds to 1000 years.

Functionality

The level-sense latch with improved MTBF is depicted in figure 4.13 [31]. The feedback path consisting of two inverters and a transmission gate (FINV1, FINV2, and T2) is separated from the

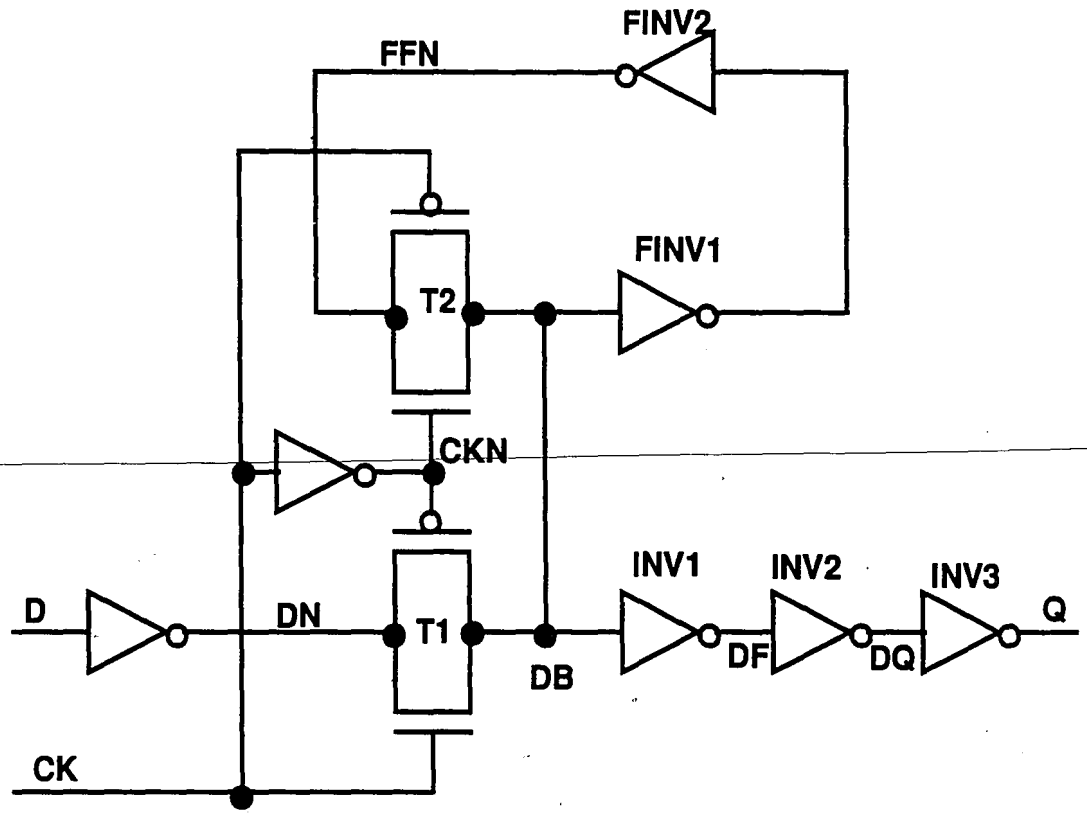


Figure 4.13. Schematic diagram of the Gabara Latch circuit.

feedforward path consisting of three inverters (INV1, INV2, and INV3). These two paths can be designed independently. The feedback path can be sized to adjust the resolution of the metastability window while the feedforward path retards the propagation of the metastable state to Q. Note that the inverter INV1 can be sized small so that the parasitic load capacitance of its gate can be minimized at node DB providing yet a higher resolution capability at this node. The gain of the feedforward path can be readjusted by the size of INV2 and INV3 or additional inverters can be added in series depending on the frequency of operation or on the value of the capacitive load of the next latch. In previous circuit designs of latches, the feedback and feedforward paths share a common path through at least one inverter, preventing independent design of these two paths.

Figure 4.14 displays the waveforms as a result of a functional simulation of the latch. The input waveforms are identical to those applied to the FD1S1A. The output waveforms are expected to be identical as well since the latch is to perform the same function. Visual comparison of figure 4.14 with figure 4.8 confirms the functionality.

The inverters INV1 and INV2 are identically sized to FINV1 and FINV2. However, as we will see later, it is interesting to note that the waveforms at nodes DF and FF are different when the latch is near the metastable point. This occurs because the feedback path consists of a closed loop path (360*degree* phase shift) with a short delay, while the feedforward path does not close on itself. The feedback path resolves the voltage at DB, while the multi-stage inverter feedforward path decreases the possibility of the propagation of the metastable state. Both paths have inverters with high gain to allow the latch to have a higher MTBF. The number of inverters in the feedforward path is determined by the maximum frequency of operation.

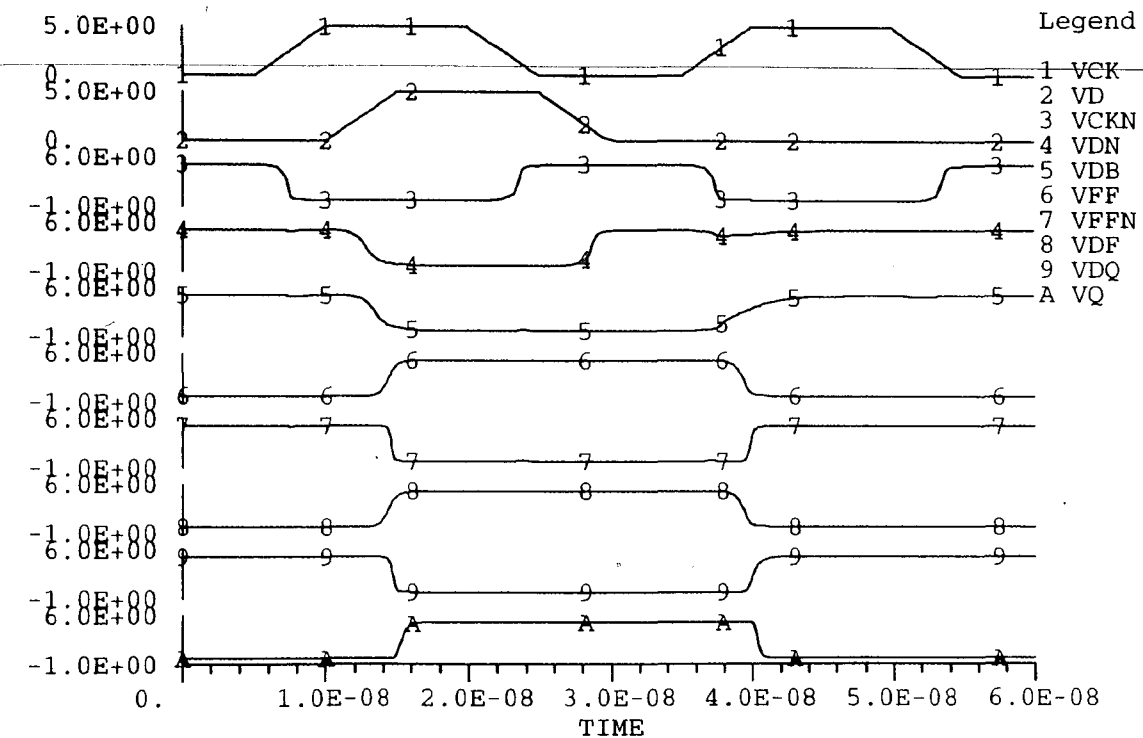


Figure 4.14. Functional simulation of Gabara Latch

Hit return to continue:

Recovery From Metastability

A quick measure for the susceptibility of the latch to the metastable state can be obtained by forcing the internal nodes of the feedback path to the metastable voltage value of 1.96943 volts, and performing a transient analysis. The nodes of the feedforward path are initialized at genuine digital voltage levels since that is their true state immediately after the input clock samples the input data within the metastability window. Figure 4.15 shows the result of the simulation of the Gabara latch exiting the metastable state. A visual comparison between figure 4.15 and figure 4.10 shows that the Gabara latch obtains a dramatic improvement in decision time with respect to the FD1S1A. The main reson for this is the decreased capacitance in the feedback loop, therefore a larger bandwidth. A standard latch, such as the FD1S1A, "sees" the load of the next stage and the load of the routing to that stage at its outputs which are part of the feedback path. Reduced capacitance at the nodes of the feedback path reduces the time required for the regenerative action, τ, as calculated by equation 2.4.12. A linear reduction τ translates into an exponential increase in the voltage difference between the nodes of the feedback path as calculated in equation 2.4.22.

Simulation Under Critical Input Timing

It is worthwhile, at this point, to investigate the circuit's performance under critical input timing. Figure 4.16 shows the waveform at the output node Q as a result of a simulation using critical input timing. Each cycle of the waveform represents the response of the circuit to increased clock to data skew. The input data is kept steady while the clock period is varied by 0.00001 ns at each cycle. The result is that at the beginning of each period, the clock to data skew is increased by a very small amount. Such fine resolution is required to see a metastable state of reasonable duration. This method has greatly facilitated the search for the metastability window through simulation. Figure 4.16 shows the equivalent of 11 simulations with varied clock to data skews.

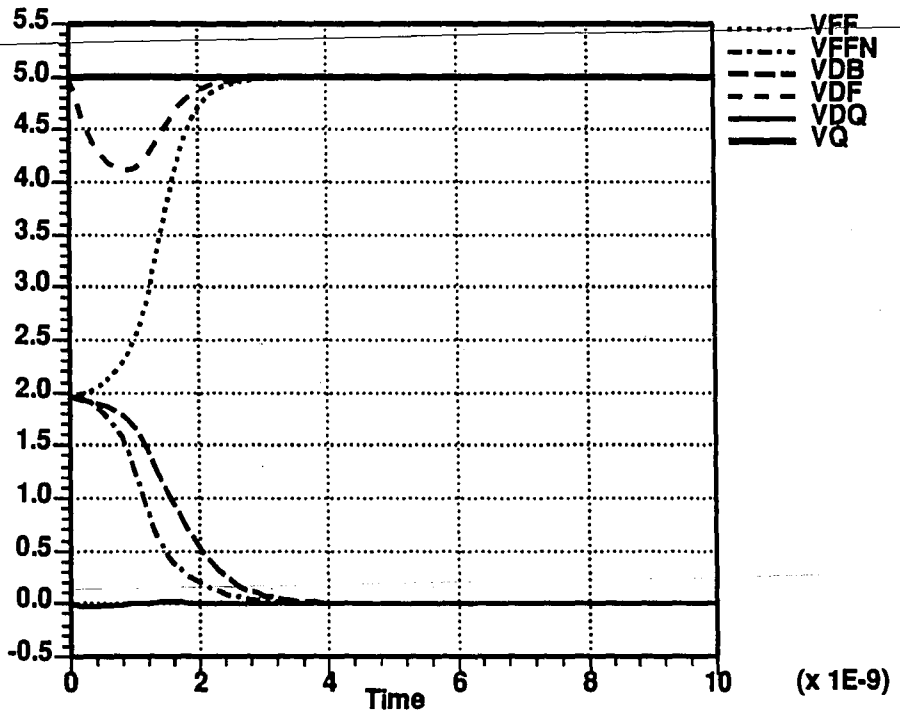


Figure 4.15. Gabara Latch recovery characteristics

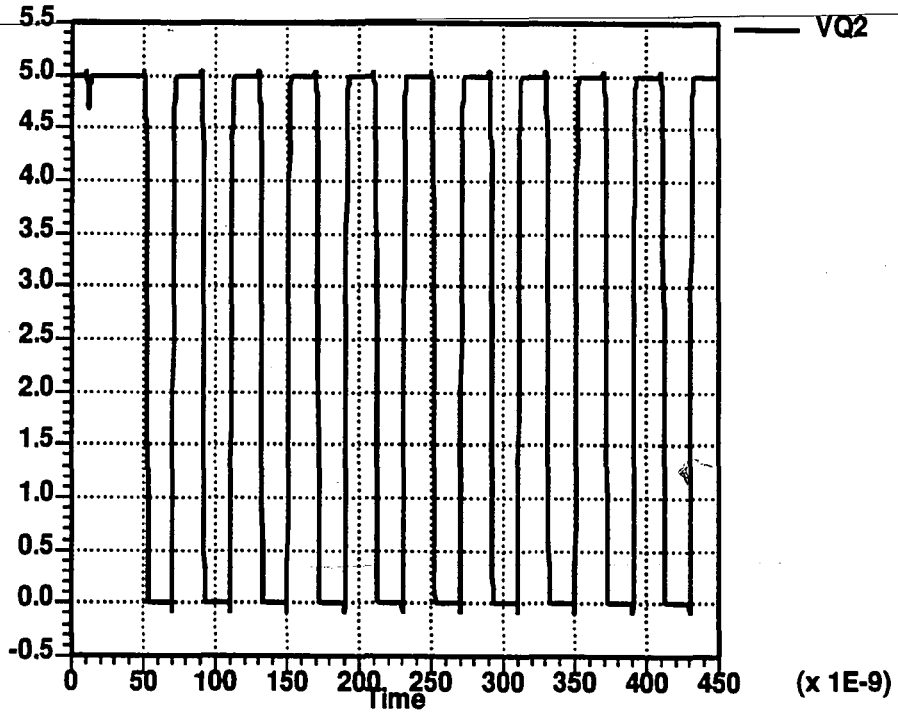


Figure 4.16. Gabara Latch output waveform under critical input timing

There appears to be no metastable state at the output of the latch, VQ, in figure 4.16. Figure 4.17 is a close-up of the first two clock cycles. At the beginning of the first cycle, data is apparently sampled to be high, since the output is high. The second cycle reveals that the data was sampled to be low since the output is low. The resolution of clock to data skew is exactly the same as that of the FD1S1A simulation; therefore, we expect the occurrence of the metastable state at the output. The Gabara latch does not exhibit metastability at the output Q.

It is interesting, however, to look at the behavior of the internal nodes of the latch. Figure 4.18 again presents the close-up of the first two clock cycles but also shows the waveforms at the internal nodes. Even though the output waveform VQ2 is not exhibiting the metastable state, the nodes of the feedback path are. VFF and VFFN clearly loiter around the metastable voltage (1.96943 volts) following the clock and data high to low transition. Figure 4.19 is a close-up of the first cycle including the internal nodes. The duration of the metastable state is about 2.5 nanoseconds. Figure 4.20 is a close-up of the second cycle including internal nodes. The metastable state is clearly visible although its duration is less than in the previous figure.

Mean Time Between Failures

In order to see a manifestation of a metastable state, even for a short duration, at the output Q of the Gabara Latch, its duration at internal node DB must be greater than the propagation delay through the three inverters INV1, INV2, and INV3. This is because each inverter will respond to an input voltage V_M after a propagation delay. Its allowed resolution time, that is, the time that it takes the internal node DB to resolve the metastable state, can be increased by the sum of the propagation delays of the three inverters.

From the relationship in equation 2.4.24 we know that a long lasting metastable state is a result of a

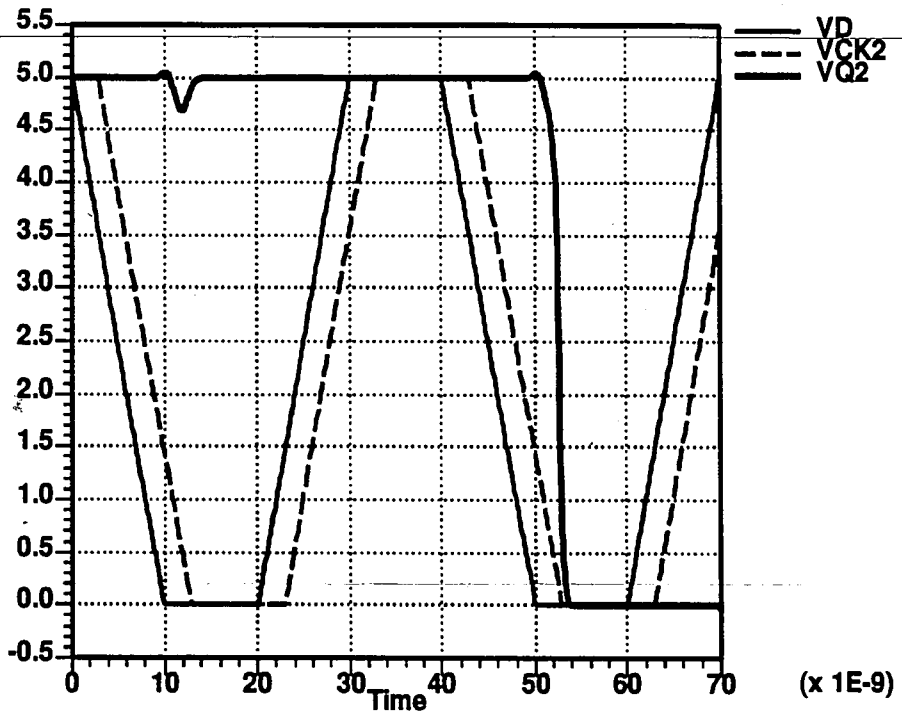


Figure 4.17. Close-up of first two simulation cycles

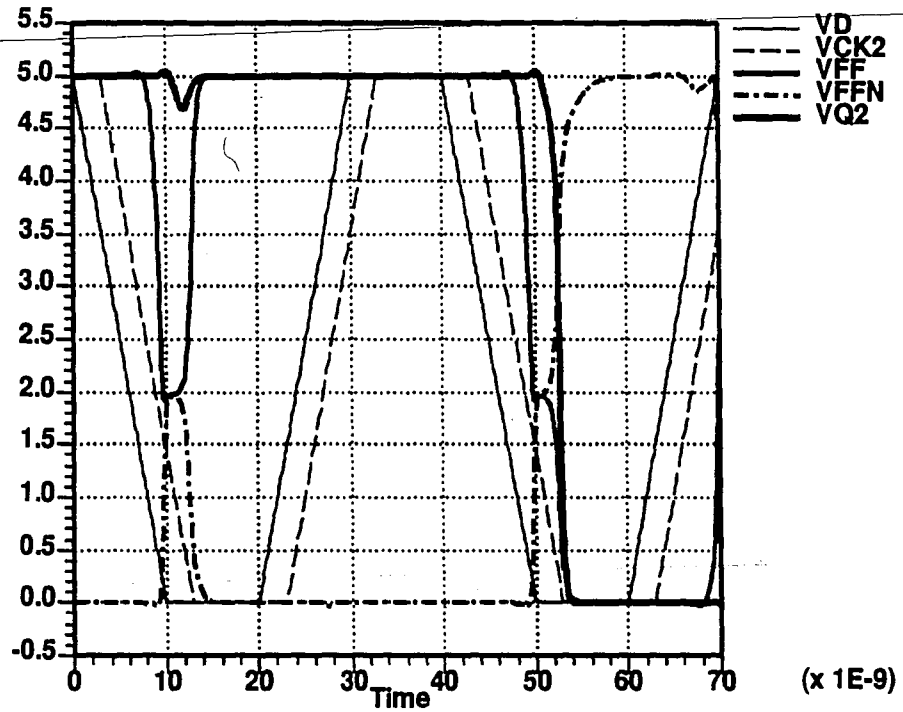


Figure 4.18. First two cycles including internal nodes

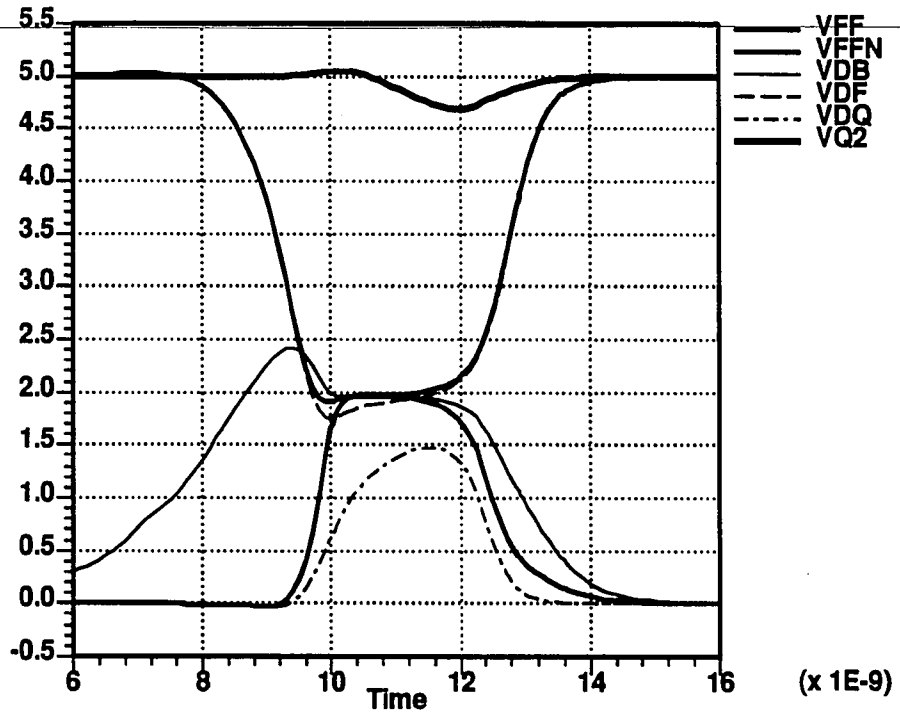


Figure 4.19. First cycle including internal nodes

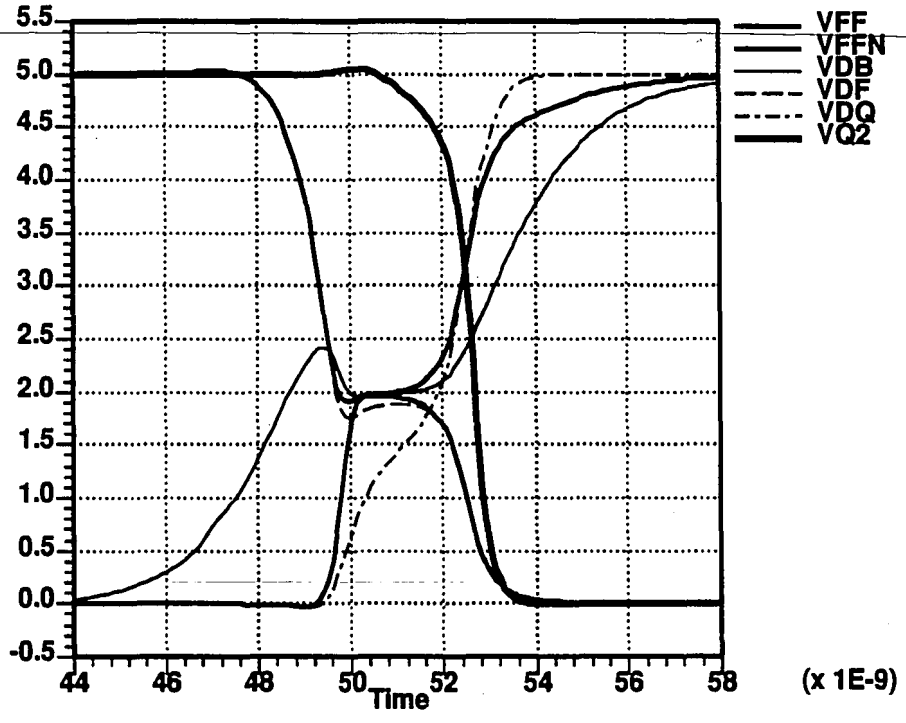


Figure 4.20. Second cycle including internal nodes

decrease in the metastable voltage window. The increase in allowed resolution time in the Gabara Latch essentially decreases the metastable voltage window, decreasing the metastable time window, hence increasing the Mean Time Between Failures.

The metastable voltage window of the Gabara Latch is found to be

$$\delta_V = 1.35 \times 10^{-12}\, volts$$

and assuming an input slew rate of 10 nanoseconds, the metastable time window is

$$\delta_T = 2.7 \times 10^{-21}\, seconds$$

so the Mean Time Between Failures of the Gabara Latch is:

$$MTBF = 2.9 \times 10^{12}\, seconds$$

or, $MTBF = 93973\, years.$

Comparing this result with the MTBF of the FD1S1A found to be 189 years, the Gabara Latch offers greater reliability.

4.5 Modified Gabara Latch Circuit

Although the Gabara latch circuit has been shown to possess a large MTBF, it is still susceptible to failure if the duration of the metastable state is longer than the propagation delay of the feedforward path. This section presents an latch design which makes use of a Schmitt Trigger.

The addition of a Schmitt Trigger was suggested as a solution [5] to the metastability problem by using it within the feedback loop. This implementation has its shortcomings [8]. The circuit in this section

uses the Schmitt Trigger as an additional protection against the occurrence of metastability at the latch outputs by inserting it in the feedforward path. A brief discussion of the behavior of the Schmitt Trigger is appropriate at this time.

Schmitt Trigger Buffer

A circuit implementation of the Schmitt Trigger buffer is depicted in figure 4.21 [35,36,37]. The important design parameters for a Schmitt Trigger buffer are the reverse trigger voltage V- and the forward trigger voltage V+. V- is the point at which the output will switch when the input voltage is reduced from V_{DD} to 0 volts. V+ is the switching point when the input voltage is increased from 0 volts to V_{DD}. Since V- is less than V+ the Schmitt Trigger exhibits hysteresis within these two values. Figure 4.22 shows the voltage transfer characteristics of a Schmitt Trigger buffer using a W/L ratio of 9 for each device. V- is about 1.5 volts and V+ is about 3.0 volts. The width of the hysteresis zone is then 1.5 volts. A transient analysis can be performed to verify the AC operation of the circuit, as shown in figure 4.23. This figure shows the result of such a simulation using both slow rise and fall input waveforms.

Changing the W/L ratio of critical devices MP3 and MN3 modifies V- and V+, and thereby the width of the hysteresis region. For example, by changing the ratios of MP3 and MN3 to 18, the hysteresis region can be increased to 2.2 volts. Figure 4.24 shows the voltage transfer characteristics for the modified circuit where V- is 1.3 volts and V+ is 3.5 volts. Figure 4.25 shows the results of the corresponding AC analysis.

A wider hysteresis region, however, produces longer propagation delay through the Schmitt Trigger; therefore, a compromise between propagation delay and width of hysteresis region must be reached for an actual implementation.

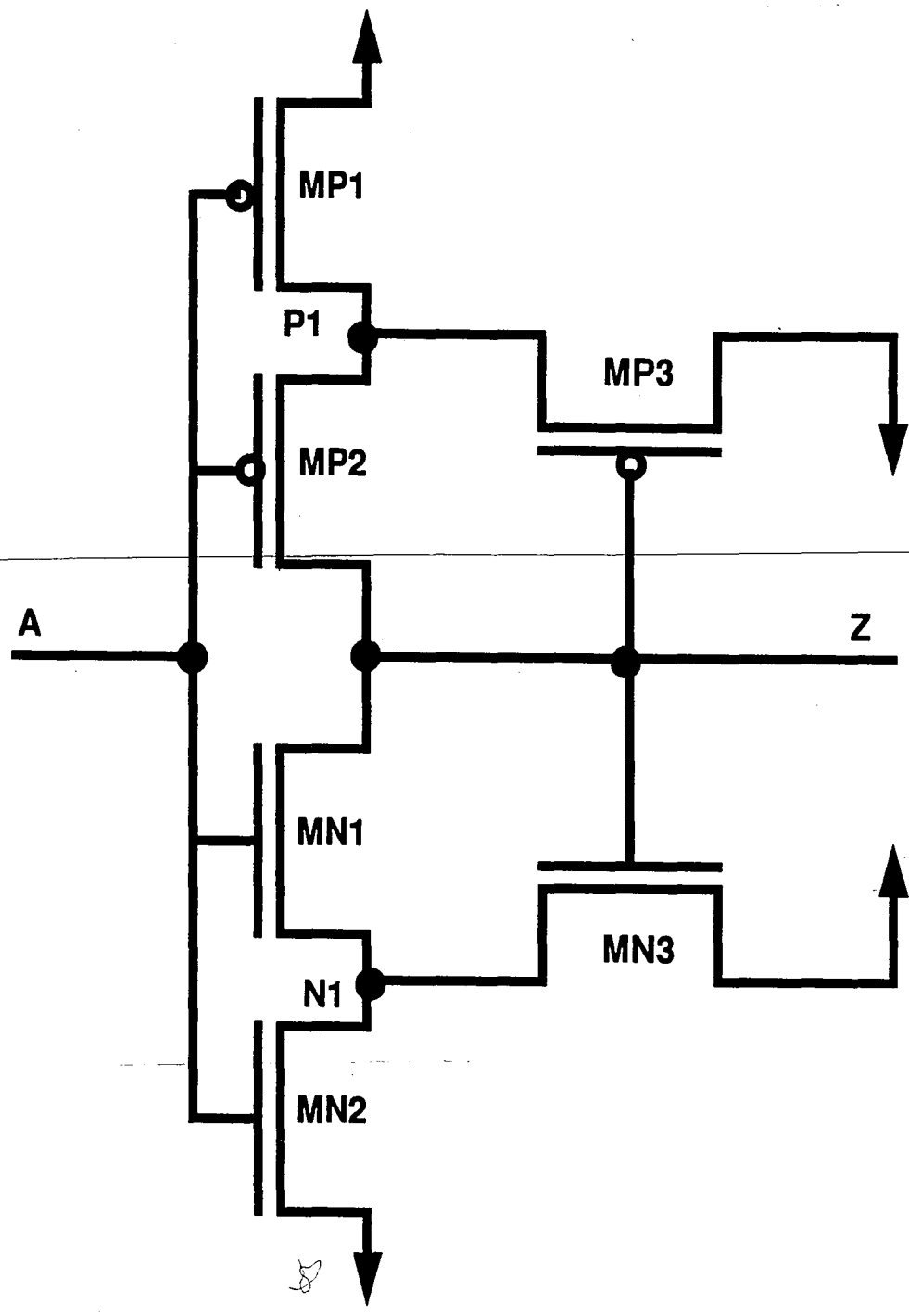


Figure 4.21. Schematic diagram of Schmitt Trigger Buffer.

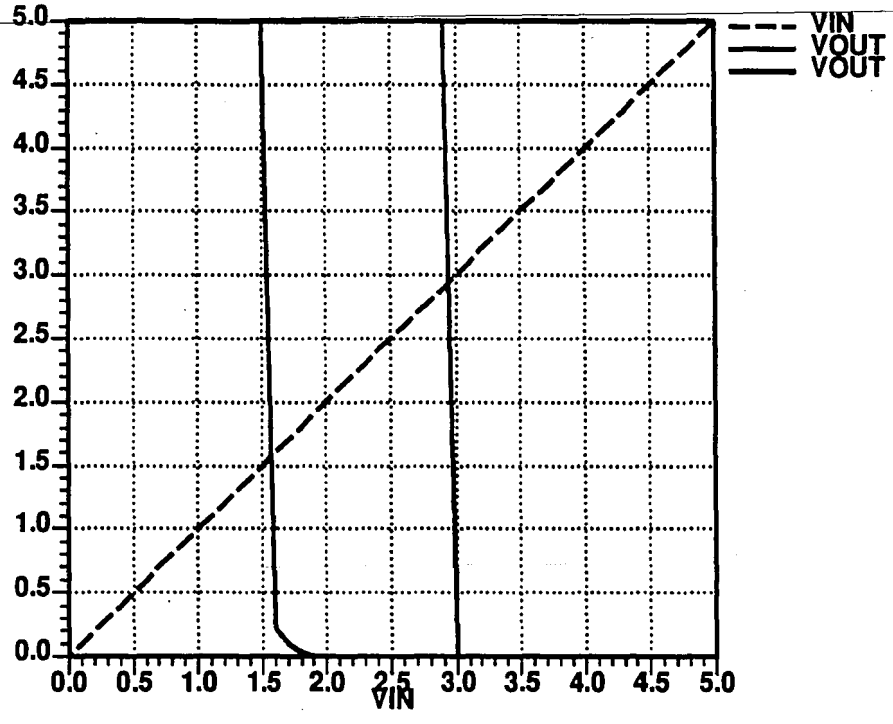


Figure 4.22. VTC of Schmitt Trigger

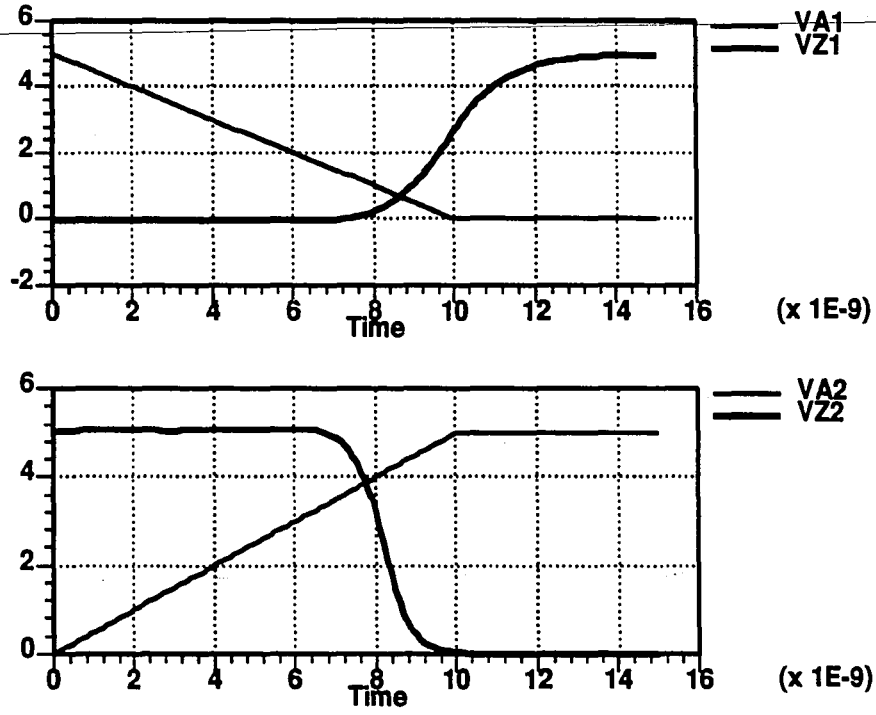


Figure 4.23. AC Analysis of Schmitt Trigger

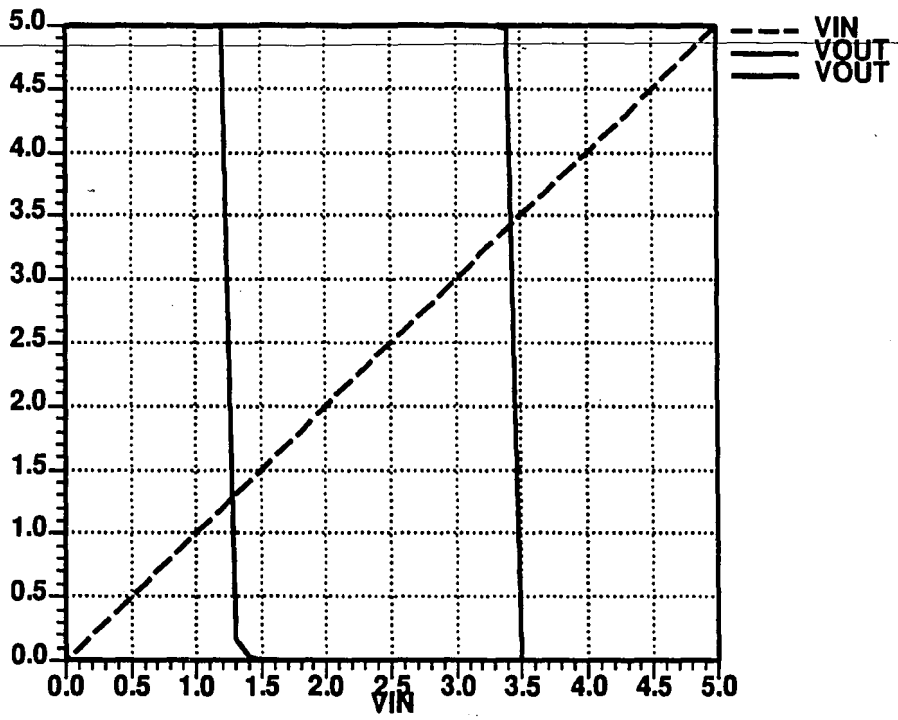


Figure 4.24. VTC of modified Schmitt Trigger

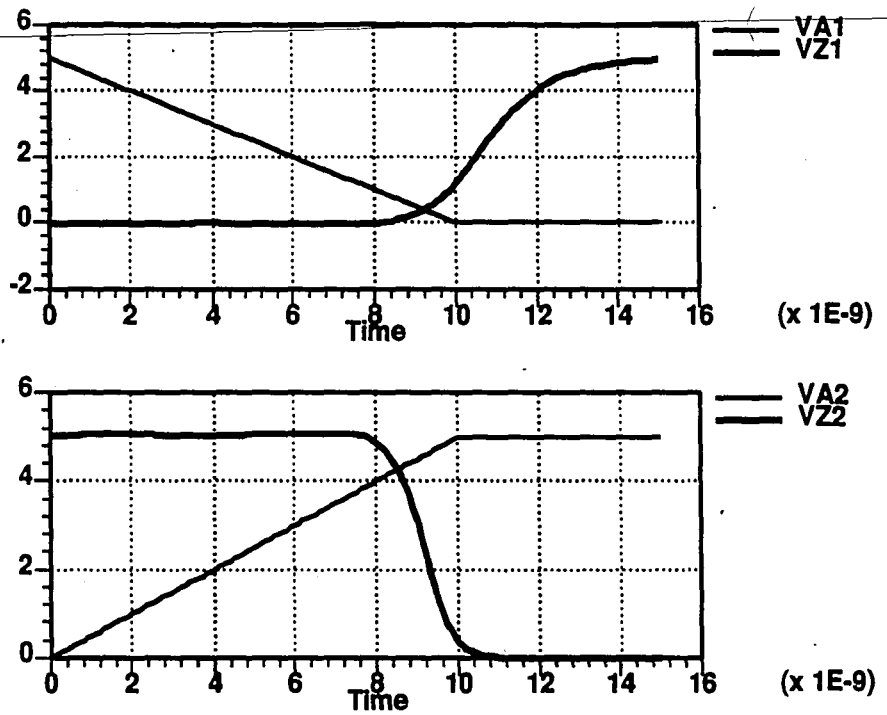


Figure 4.25. AC Analysis of modified Schmitt Trigger

Implementation of Schmitt Trigger

Figure 4.26 shows the Gabara latch circuit with the implementation of the Schmitt Trigger. The latter has been substituted in place of inverter INV2. This appears to be the optimum position since its output is buffered to provide additional drive capability, and its higher input capacitance is decoupled from the feedback loop to maintain the recovery time.

Functionality

Figure 4.27 shows the result of the functional simulation of the latch and displays inputs, outputs, and internal nodes. Visual comparison to figure 4.14 reveals that the circuit operations of this circuit and the original are identical.

Recovery From Metastability

The resolution characteristics, as shown in figure 4.28, verify that the feedback loop is unaffected since they are the same as the original Gabara circuit.

Simulation Under Critical Input Conditions

The feedforward characteristics of the modified Gabara latch do, however, change. Figure 4.29 shows the result of a transient analysis performed by incrementing the data-clock skew at each clock cycle. This is the same type of simulation depicted in figure 4.16. A visual comparison of the two figures points out that the original circuit shows a tendency for output switching prior to the beginning of output toggling, whereas the modified circuit does not. Figure 4.30 is a close-up of the portion of the simulation shown in the previous figure immediately before output toggling occurs. The output node VQ2 appears very stable although the internal nodes are in the metastable state. In contrast, figure 4.19

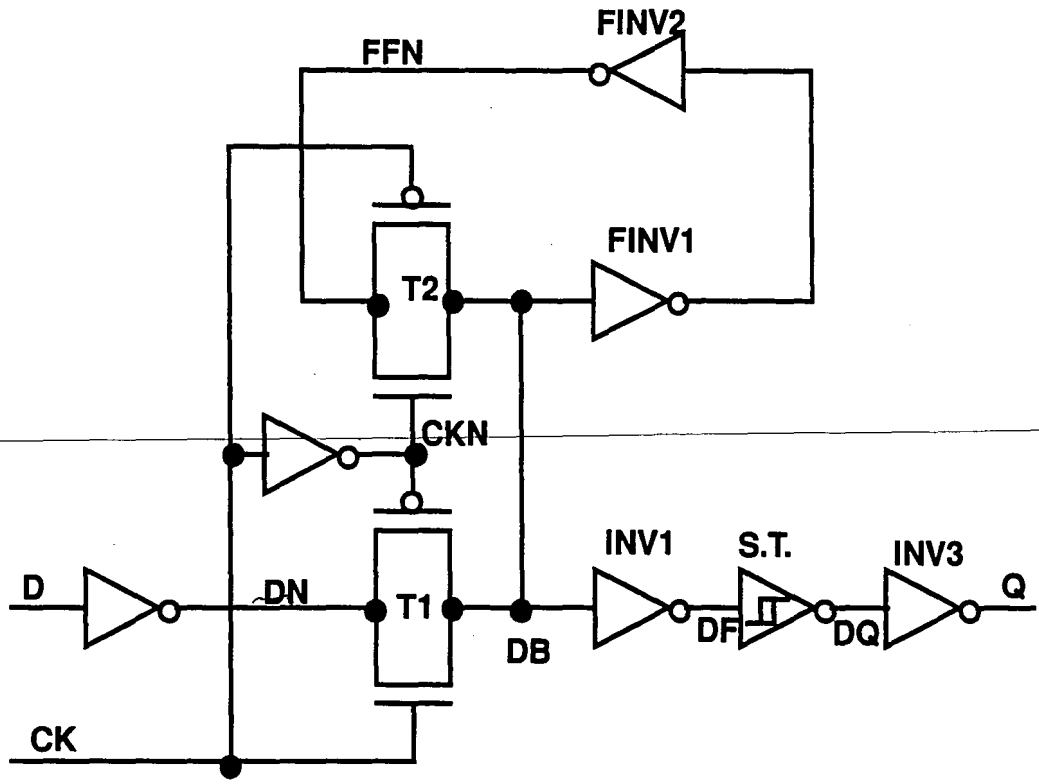
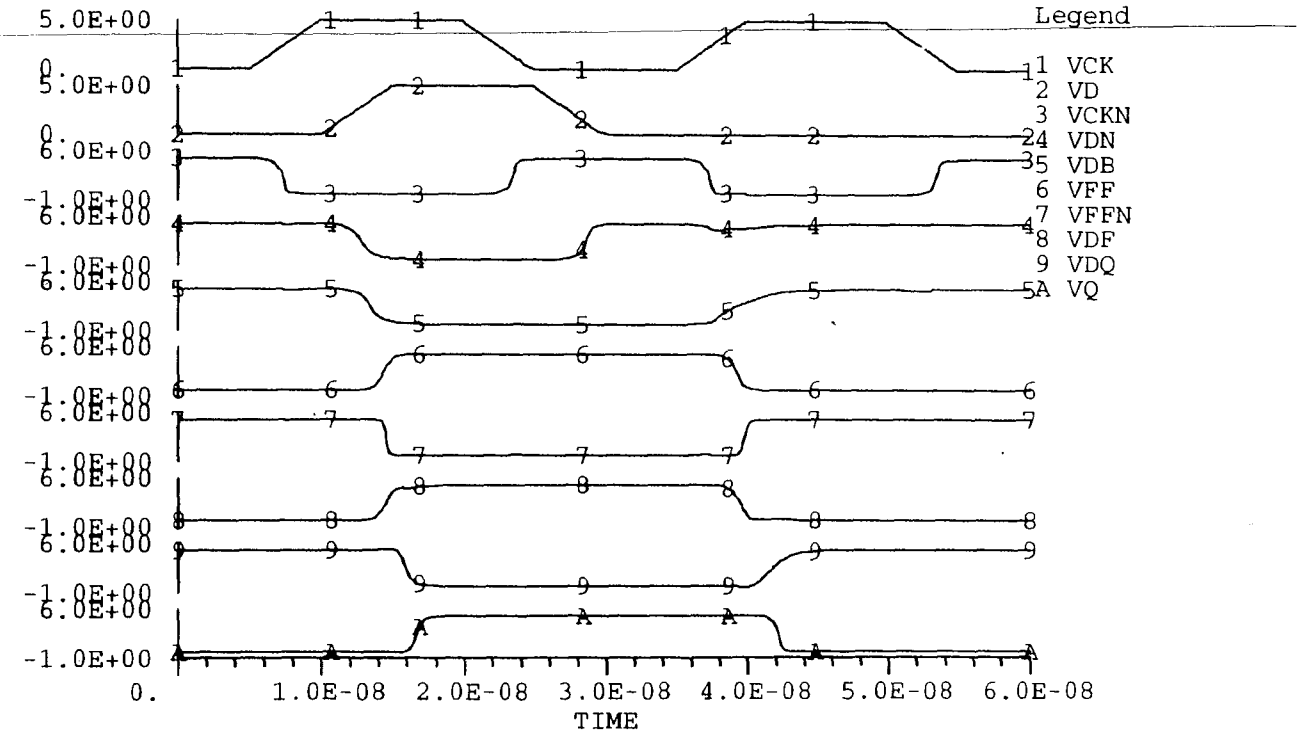


Figure 4.26. Implementation of Schmitt Trigger in modified Gabara Latch.



Hit return to continue:

Figure 4.27. Functional Simulation of modified Grabara Latch

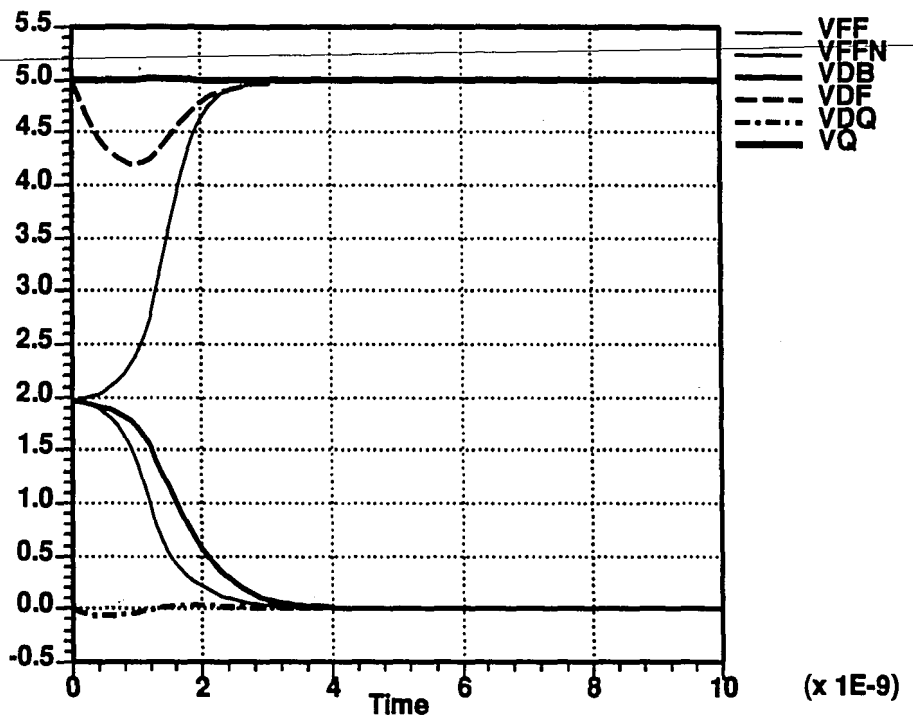


Figure 4.28. Modified Gabara Latch recovery characteristics.

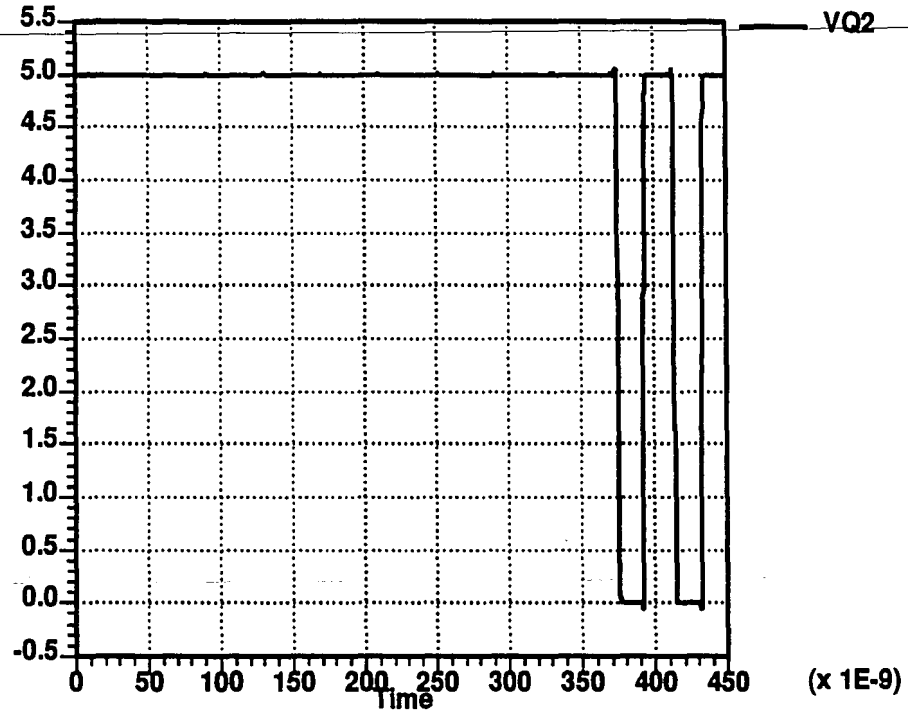


Figure 4.29. Output waveform under critical input timing

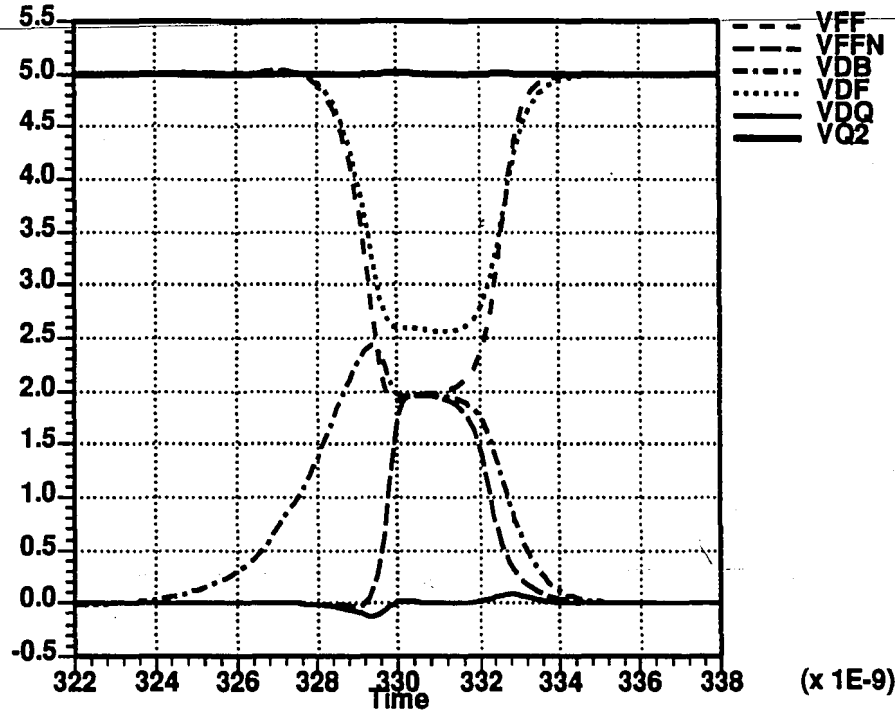


Figure 4.30. Close-up of cycle before output toggling

shows that the output VQ2 begins to switch but then remains in the same state due to the short duration of the internal metastability. Figure 4.31 is a close-up of the very next cycle, where the output toggles. It shows a very clean output waveform without "hesitation" or metastability.

From the comparison of figures 4.19 and 4.30, it is clear that a long-lasting metastable state will affect the output of the Gabara latch, and although there is no apparent perturbation at the output of the modified circuit, more decisive evidence is needed to fully appreciate the benefit of implementing a Schmitt Trigger. A smaller test circuit, as shown in figure 4.32, can be constructed which emulates the final stages of the feedforward path. The waveform at input A can be made to approximate the actual input to the Schmitt Trigger before, during, and after metastability. The duration of the metastable state can then be changed to observe the effect of long duration on the Schmitt Trigger. Figure 4.33 shows the result of simulation using the latter circuit and setup for an input transition from V_{DD}, to the metastable voltage V_M, to 0 volts. Figure 4.34 shows the simulation results for the opposite input waveform. In both cases, the Schmitt Trigger output is not affected even with a metastable state lasting over 100 nanoseconds. The figures also show the effect of the metastable input on the internal nodes of the Schmitt Trigger N1 and P1. Referring to figure 4.21, N1 is the connection between MN1, MN2, and MN3; P1 is the connection between MP1, MP2, and MP3. Figure 4.33 shows that internal node P1 has a value of about 2.5 volts while input A is at V_M, and output Z is low. The output being low means that MP3 is definitely on, thus connecting P1 to ground. Node P1 should then be 0 volts. Its value, however, is 2.5 volts which means that MP1 must be on. The MP1 and MP3 path represents a voltage divider between VDD and ground. This means that current is flowing, and power is being dissipated. A display of the transient current can easily verify this. Figure 4.35 shows the waveform of the current flowing from the V_{DD} current source. While the input of the Schmitt Trigger is at V_M, there is a 1mA current flowing. This means that there is a DC path from power to ground through MP1 and MP3, hence power is dissipated.

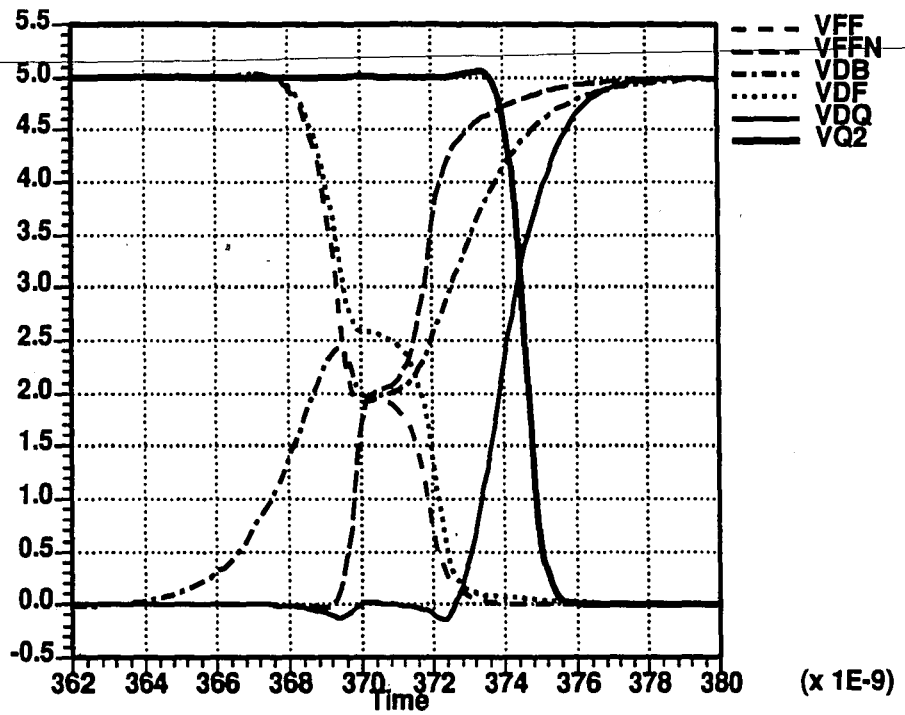


Figure 4.31. Close-up of cycle when output toggles.

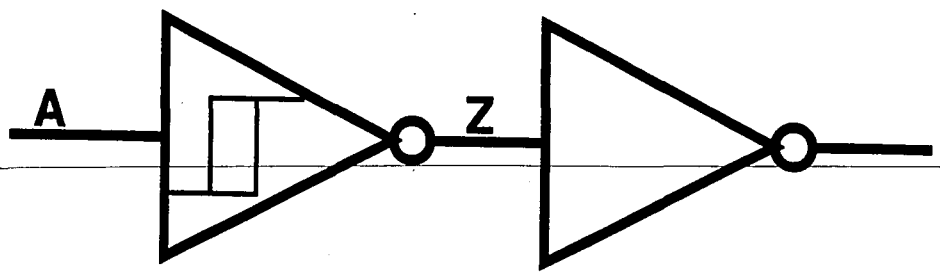


Figure 4.32. Schmitt Trigger test circuit

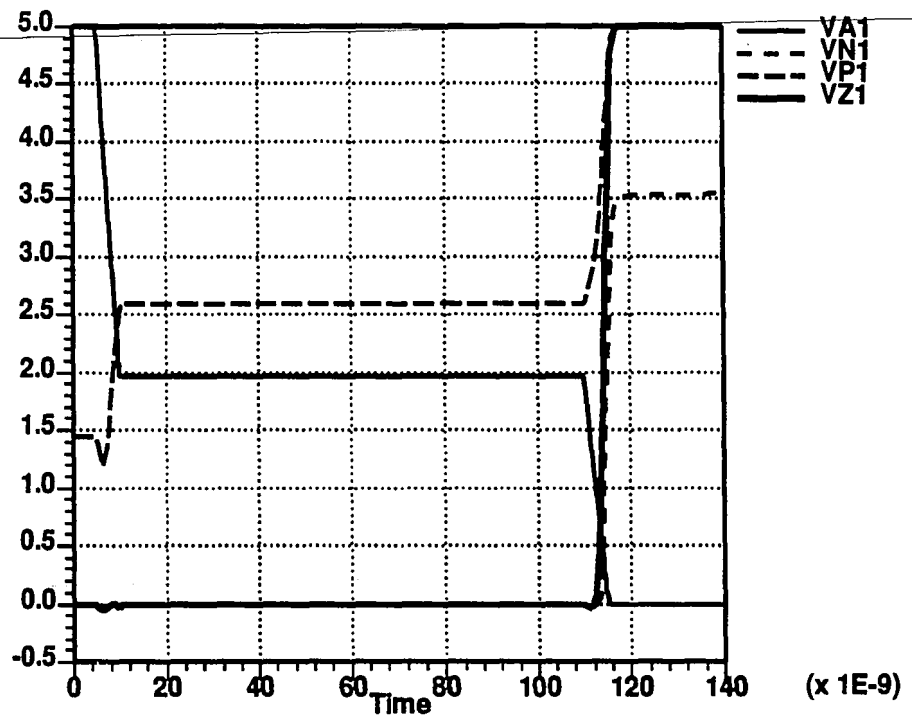


Figure 4.33. Analysis of Schmitt Trigger with metastable falling input.

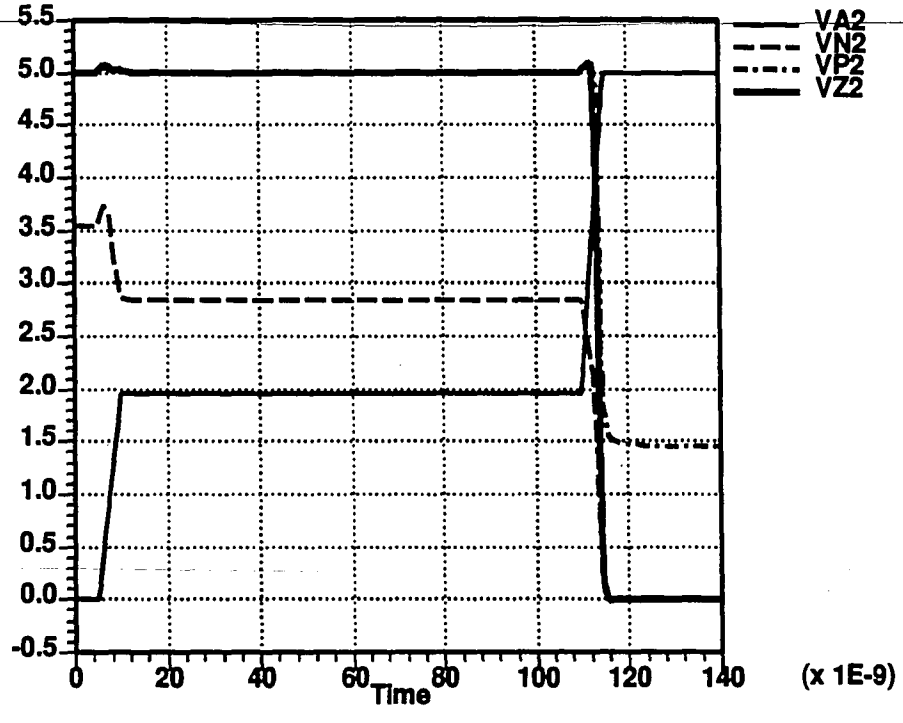


Figure 4.34. Analysis of Schmitt Trigger with metastable rising input.

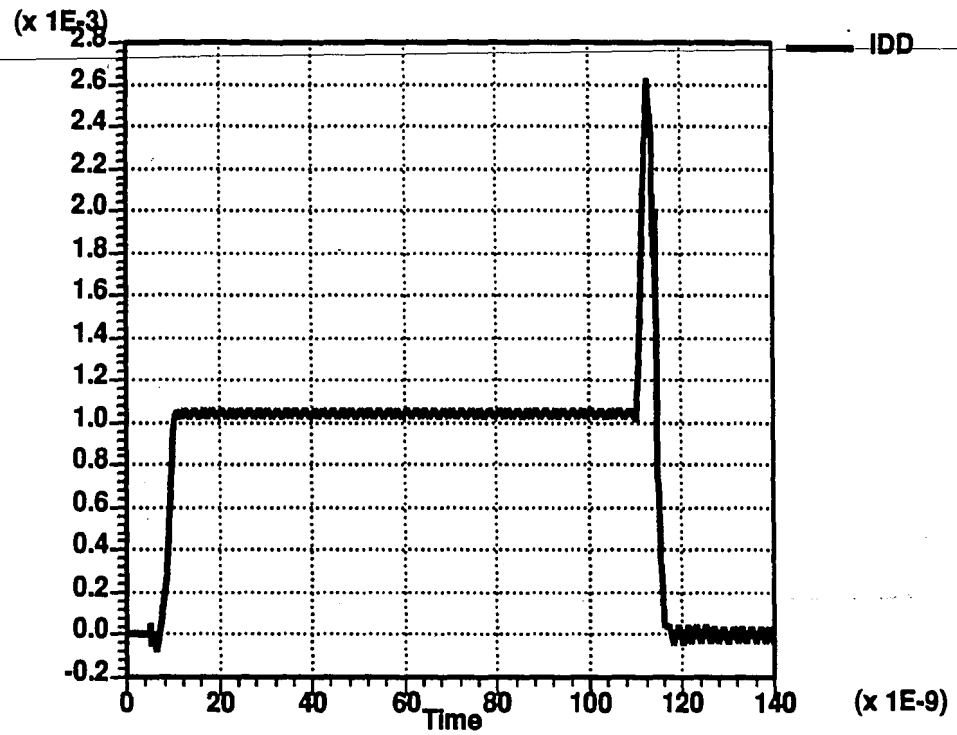


Figure 4.35. V_{DD} current waveform.

The high power dissipation of the Schmitt Trigger is a known, important issue [37]. It is especially aggravated by slow ramping inputs, and in this case an input which lingers around the metastable voltage for a period of time.

Mean Time Between Failures

The failure mode of this latch due to metastability is somewhat different than the previous circuit. The Schmitt Trigger responds to a metastable state at its input with a delayed rail voltage at its output. This size of the delay depends on the duration of the metastable state. The metastable state can be long enough to induce a delay which causes the output of the synchronizer to be latched by following stages at the end of the clock period while the output is at a metastable voltage level. This situation is unlikely because the metastable state must last through the entire clock period, and, given the sharp transition of the Schmitt Trigger, the metastable voltage window of the following stages is greatly reduced. The Mean Time Between Failures of the Modified Gabara Latch is therefore greater than the original Gabara Latch.

4.6 Offord Latch Circuit

The Offord Latch circuit [50], named after the original designer, is depicted in figure 4.36. It consists of the basic FD1S1A latch augmented with a series P and N transistor pair connected between input D and internal node I1.

Functionality

The logical functionality of the circuit can be verified by simulation. Figure 4.37 shows the result of the simulation and displays the waveforms for input, output, and internal nodes of the circuit. Visual

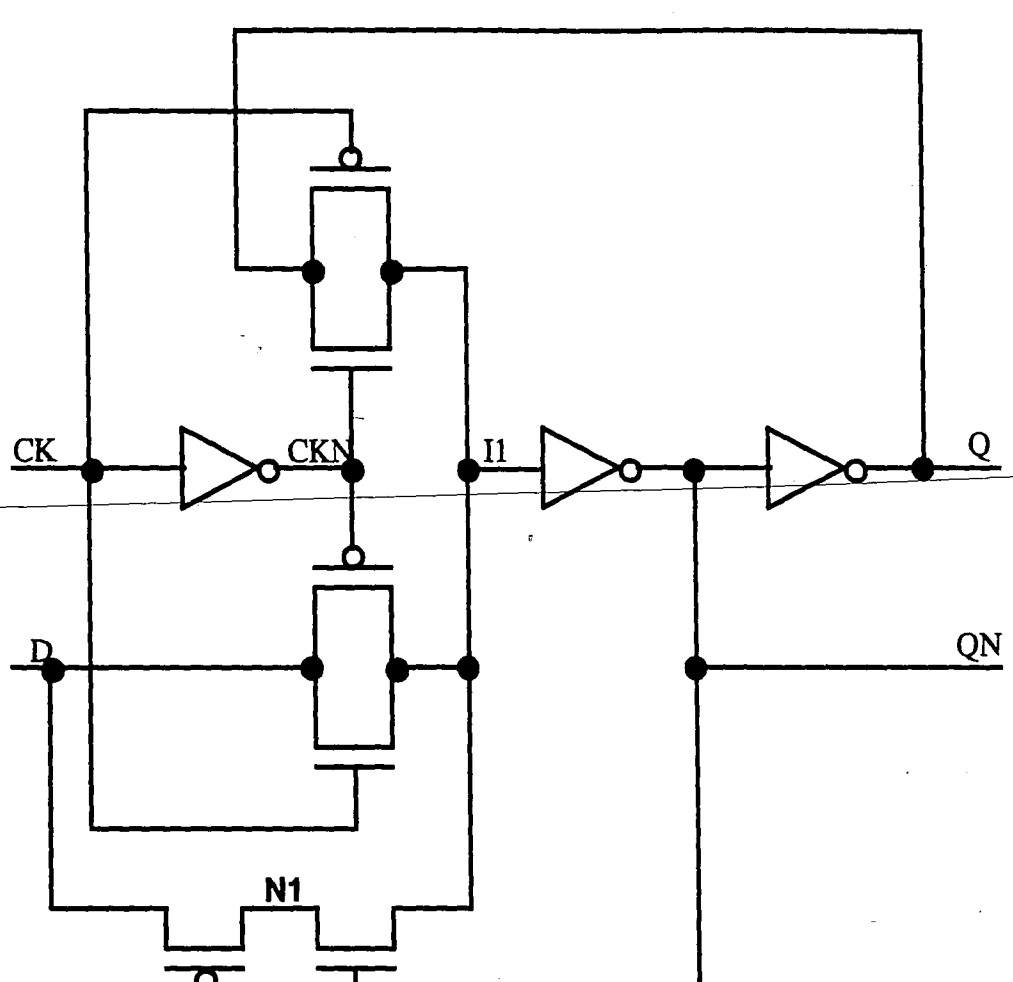


Figure 4.36. Schematic diagram of Offord Latch.

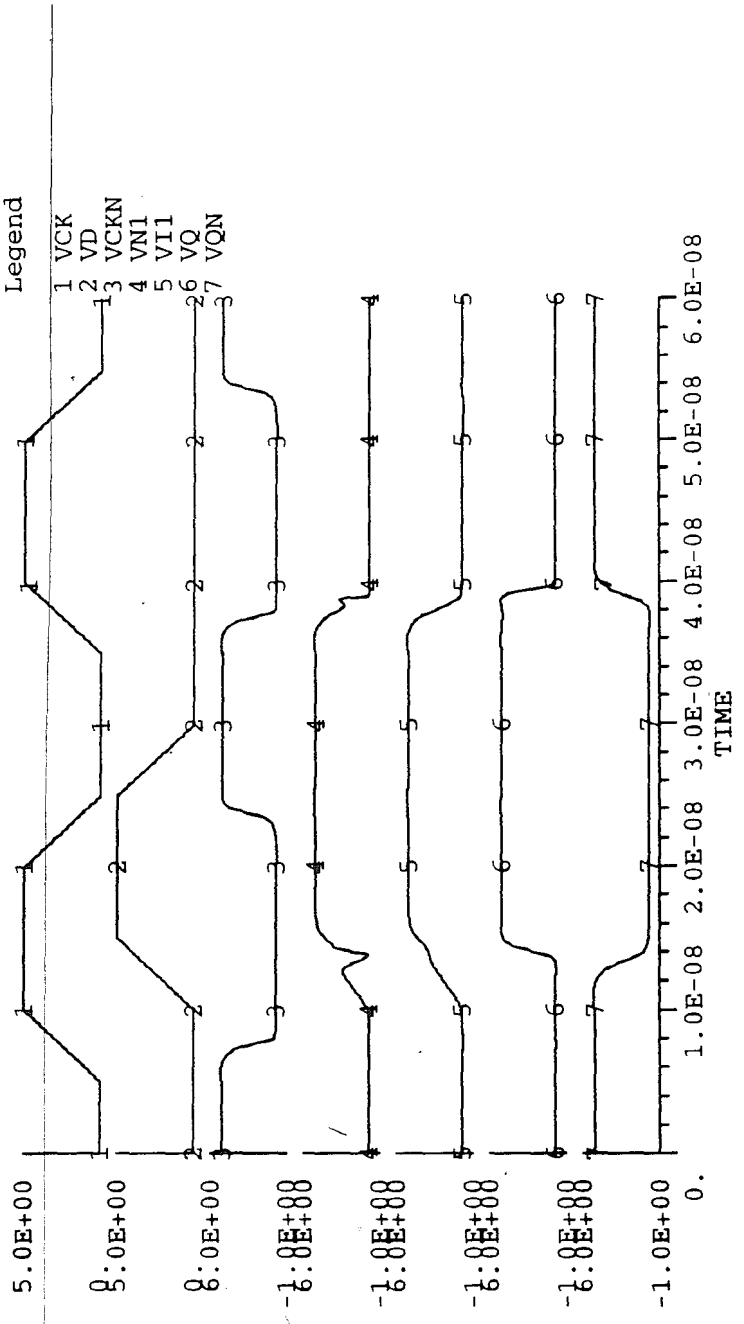


Figure 4.37. Functional simulation of Offord Latch

comparison of the primary inputs and outputs between figure 4.37 and figure 4.9 confirms that the operation of this circuit is identical to that of the FD1S1A standard cell latch.

The principle behind the addition of the series N and P transistors is enjoyably simple. Assume a metastable state at QN, that is, QN is at the metastable voltage V_M (1.96943 volts). This voltage should be enough to turn on both N and P transistors sufficiently to complete the path between input D and internal node I1, thus taking the latch from the metastable state to the state of the input D. When QN assumes a rail voltage level, the D-I1 connection is severed because one of the transistors will not be conducting, so that the normal operation of the latch is not affected.

The operation is verified by the functional simulation shown in figure 4.37. However, verification of the metastability correction characteristics requires a closer look.

Recovery From Metastability

By setting the internal nodes of the latch to the metastable voltage of 1.96943 volts, and performing a transient analysis, we can see how the additional transistors affect the recovery characteristics of the Offord latch. Figure 4.38 shows the results of the simulation. It is apparent from a comparison of figure 4.38 with figure 4.10 that the recovery characteristics of the Offord latch are slightly worse than the FD1S1A. In principle, the circuit has much better recovery characteristics, but in simulation the opposite is found. Simulation of the circuit under critical input timing is not necessary since we know that its metastable characteristics are worse than those of the FD1S1A. However, a first-order analysis of the reason why the circuit has not produced the desired results is in order.

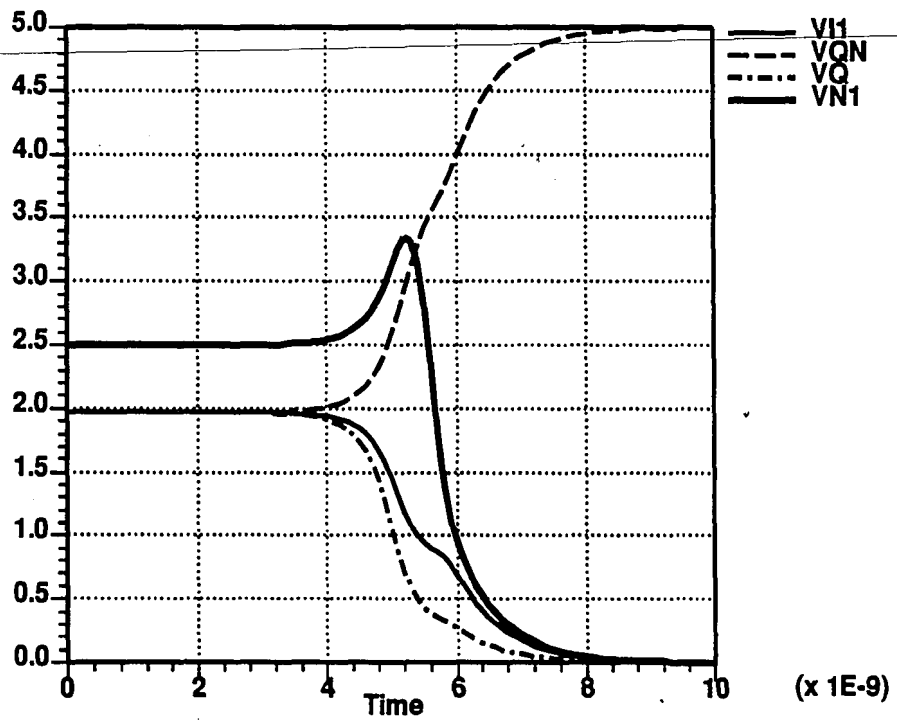


Figure 4.38. Offord Latch recovery characteristics.

Offord Latch First-Order Analysis

The body effect on both the N and P transistors which are series connected between input D and internal node I1, and their gate-source voltage during the metastable state must be taken into account. Figure 4.39 shows the portion of the Offord latch which should contribute to a faster recovery from the metastable state.

Consider the structure in figure 4.39a, with a voltage at D of 0v. The body effect must be considered since the voltage between the source and the body of the N-transistor is non- zero. The same is true for the P-transistor. Assuming 0 volts at D, and 2 volts at I1:

N-transistor

$$V_{SB} = V_{I1} - V_{SS} = 2volts$$

P-transistor

$$V_{SB} = V_D - V_{DD} = -5volts$$

A calculation of the threshold voltage including the body effect due to a non-zero V_{SB} component is in order. The threshold voltage including the body effect is defined as:

$$V_T = V_{TO} + G_{DC}(\sqrt{|-2\phi_S + V_{SS}|} - \sqrt{2|\phi_S|})$$

where V_{TO} is the threshold voltage at zero bias (VSB = 0), G_{DC} is the body effect coefficient, ϕ_S is the surface electrostatic potential, and V_{SB} is the source-to-body voltage.

From the AT&T 1.75μm CMOS process parameters we can extract the following:

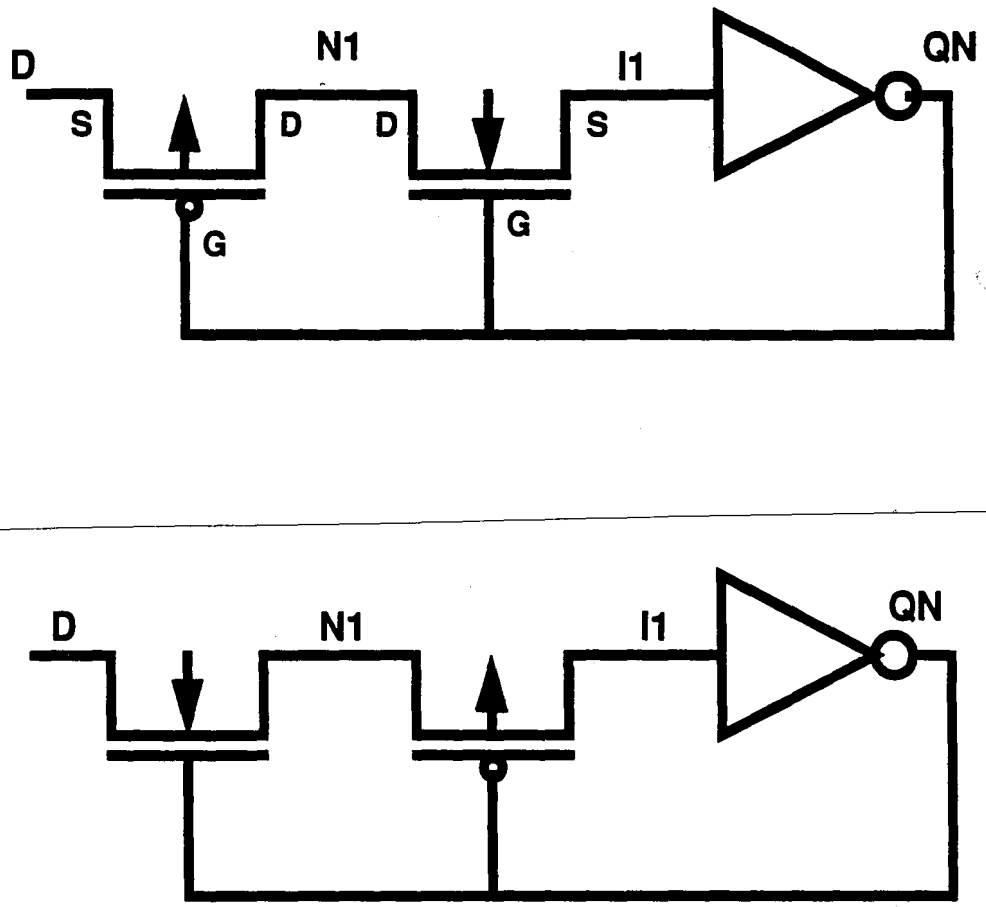


Figure 4.39. Circuit contributing to a faster recovery from the metastable state.

Parameter	N-transistor	P-transistor	Unit
V_{TO}	0.8389	-1.368	v
G_{DC}	0.6	0.6	v
$2\phi_S$	-0.75	0.71	v

Using the above parameters, $V_{TN} = 1.32 volts$, and from figure 4.39a we see that $V_{GSN} = 0 volts$, then

$$V_{GSN} < V_{TN}$$

therefore the N-transistor is off.

Similarly

$$VTP = -2.236 volts$$

$$VSGP = 2 volts$$

$$VSGP > VTP$$

and P-transistor is also off when the input D is at 0v. When the D input is at 5 volts, the P-transistor is on, but the N-transistor is still off, and the path is still not closed. Figure 4.40 shows a simulation of the Offord Latch with the D input set at 5 volts.

The configuration of figure 4.39b suffers from similar anomalies. With $V_{SB} = -3 volts$, the threshold voltage of the P-transistor increases, and since $V_{GS} = 0 volts$, the P-transistor remains non-conducting. With input D at 0 volts, the N-transistor, on the other hand, is on since:

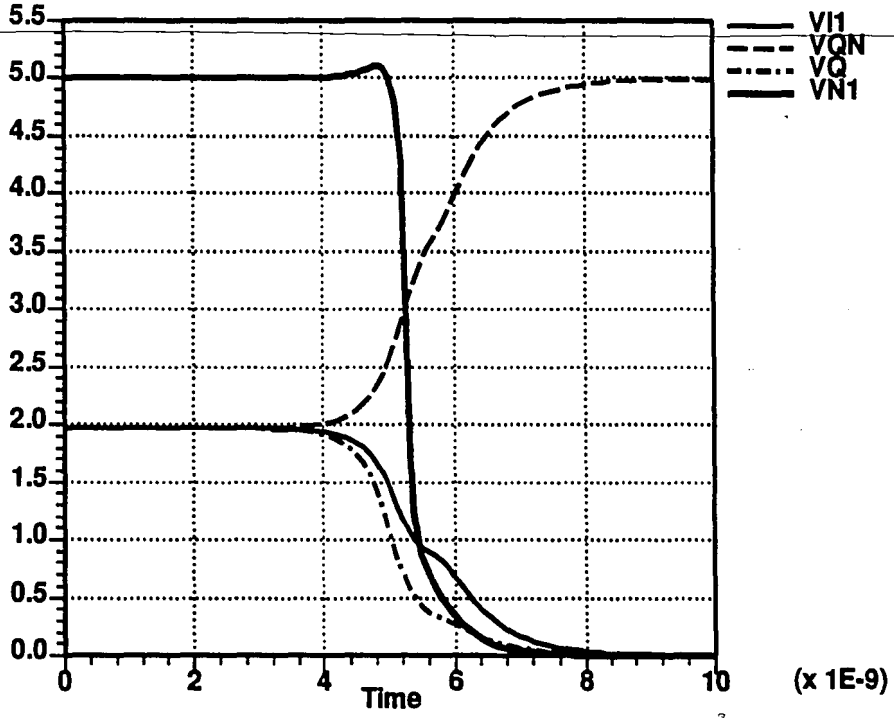


Figure 4.40. Recovery characteristics with input D at 5v

$$V_{SB} = 0 volts$$

$$V_{TN} = V_{TON} = 0.83 volts$$

$$V_{GSN} = 2 volts$$

$$V_{GSN} > V_{TN}$$

but if the input D is at 5 volts the N-transistor if off as well.

Based on the previous analysis, the series N and P transistors added to the basic latch do not improve its characteristics of recovery from the metastable state, therefore, the Offord Latch is prone to failures due to metastability with a Mean Time Between Failures essentially equivalent to the FD1S1A.

5. CONCLUSION

This thesis has discussed metastability in CMOS latches - a phenomenon which causes intermittent failures in systems requiring synchronization. These failures arise from the attempt to synchronize asynchronous inputs to a synchronous system by the use of a latch known as a synchronizer. The asynchronous input of the synchronizer are sampled at regular intervals by a system clock. Since the arrival of an asynchronous input is impossible to predict, there is a finite probability that it will violate the setup and hold time of the synchronizer. When this happens the operation of the synchronizer diverges from the normal digital mode and its internal circuitry operates in the high-gain linear mode where small-signal models best describe its behavior.

Along these lines, the theory behind the linear operation has been presented. This has enabled the formulation of an equation which predicts the exponential recovery from the metastable state. The equation is then used to define a metastable voltage window and the related metastable time window. An expression was then derived for the Mean Time Between Failures (MTBF) whose components are the metastable time window, the clock frequency, and the data frequency. The MTBF is a measure of the reliability of a synchronizer, and is used as a figure of merit.

The FD1S1A, a D-type latch designed in the AT&T 1.75μm CMOS technology, was then used as an example to apply the theory, and to calculate the MTBF. From this calculation, it is clear that the FD1S1A is reliable enough to use in low frequency applications. The examples used in the calculation are for a system in which a keyboard is interfaced to a CPU. The CPU operated at a frequency of 25Mhz, while the keyboard provides the asynchronous input at a frequency of 2.5Hz.

The FD1S1A, however, turns out to be very unreliable in high frequency applications. Instead, the Gabara Latch can be employed as a synchronizer with improved Mean Time Between Failures. Its

characteristics of recovery from the metastable state appear to be much better that those of the FD1S1A as a result of ADVICE simulations. Further simulations show that in order to see a metastable voltage at the latch outputs, the duration of the metastable state has to be quite long. This contributes to the decrease in the width of the metastable voltage and time window and in turn a dramatic increase in the Mean Time Between Failures. The addition of a Schmitt Trigger in the feedforward stage of the Gabara Latch seems to increase the MTBF even further. The drawbacks of this addition are increased power dissipation, and the small potential for causing metastability at the next clocked stage. The latter is due to the Schmitt Trigger's response to a metastable voltage at its input with a corresponding delay at its output.

Although the Offord latch operates under the self-correcting principle using the metastable voltage itself, simulations show that its recovery characteristics are no better, if not worse, than those of the FD1S1A. The Mean Time Between Failures for this latch is then the same, or slightly higher, than the FD1S1A.

The original Gabara Latch appears to be the preferred choice for reliable synchronization. Although the Modified Gabara Latch has higher MTBF, the high power consumption makes it an unreasonable choice as a synchronizer.

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