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The application of log domain filtering to explicit RMS detection

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The Application of Log Domain Filtering to Explicit RMS Detection

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Abstract: A method of implementing an explicit RMS detector is developed. Log domain filtering is applied to the averaging section in the RMS detector. The processing in the detector is done completely in the log domain, allowing for a large dynamic range at the input. The application of the log filters eliminates the need for the feedback loop that is used in implicit RMS detectors. The limitation of using only first order filters is also eliminated. The use of higher order filters is shown to give a better approximation to the ideal "sliding window" impulse response. Specifically, a second, third, and fourth order approximation to a one second pulse is calculated. The approximations result in transfer functions that are used to develop biquad filter sections. The biquad sections were then implemented using log domain filtering circuits. Once the filters were proven out, the logging and squaring circuitry was added at the front end, and the square rooting and exponentiating circuitry was added at the back end. Four complete RMS detectors were designed, one for each of the filters of order one through four. All four detectors were shown to be operational with a sine, square wave, and pulsed input. Bursts of sines and pulses were then used to show that the higher order filters gave a better approximation to the ideal "sliding window". The fourth order circuit performed the best.

Chapter 1.0: INTRODUCTION

RMS (Root Mean Square) is a useful measure for analyzing the magnitude of an AC signal. Electronic circuits have been designed to calculate the RMS value of an input signal. There are two popular methods used in RMS detection. These methods include implicit, with settling time and bandwidth problems, and explicit which has dynamic range problems. The development of log domain filters in the past few years has allowed for improvements to be made to the explicit detectors by allowing the calculation to be done completely in the log domain.

The purpose of this work is to develop an RMS detector using the explicit calculation by applying log domain filtering techniques. The use of log domain filters will improve the detector in two ways. The entire calculation is done in the log domain, so dynamic range problems are eliminated. The second improvement involves the averaging section of the detector. The proposed design will allow for a higher order filter to be used in taking the average of the square of the input. It will be shown that this will produce a result closer to the "ideal" result that comes from the pure mathematics.

Focus will begin with a background on RMS and RMS detectors in general. The explicit and implicit methods of calculation will be explored. The filtering section will then

be analyzed and general improvements proposed. To implement the filters in the log domain, some background on these filters will be covered. The improvements to the normal filter will be included in the log design. The major design improvement involves the application of the log filter in the averaging circuit, but the design will be extended to include the other parts of the RMS detector. The filters will be incorporated with these other sections and the entire design evaluated as a complete system. The results will show that high performance explicit RMS detectors can be realized by applying log domain filters for the averaging section.

Section 1.1: RMS Detectors

RMS or Root Mean Square is one way of characterizing the magnitude of an AC signal. The RMS value is determined by squaring the input, averaging the squared values over a given time period, and taking the square root of the result. Practically, this is equivalent to finding the DC value that would produce the same amount of heat in a fixed load as the AC signal in question.

The crest factor of a waveform is another measure that is associated with the RMS value. Crest factor is defined as the ratio of the peak value of the waveform to its RMS value. Symmetrical square waves and DC signals have crest factors of one. Other waveforms may have higher crest factors. A sine wave, for instance, has a crest factor of 1.414.

The RMS value is often used to characterize a signal for controlling the way a signal is processed. One typical use of the RMS value is the control of gain. In an automatic gain control circuit the RMS value is computed in a feedback loop which then controls the gain applied to the input signal.

Because electronic calculation of the RMS value is desired for the above applications, RMS detectors were developed. The simplest and earliest method of measuring RMS involved a thermal RMS to DC conversion. The heating value of the input signal is compared to the heating value of a known, calibrated DC source. The DC source is adjusted to match the heating of the input, and the DC value is equivalent to the RMS value of the input. In varying ambient temperatures, performance of this system may be affected. Although the concept is simple and correct, the realization is very difficult. Because of the difficulties encountered, a purely electrical detector was developed.

Both implicit and explicit methods are used in the calculation of the value in electrical RMS detectors. These methods differ in the order of mathematical operations. Both give the same result, but there are advantages and disadvantages to each method.

Explicit calculation follows the mathematical formula exactly. The input signal is squared, then averaged, then rooted. The method is very straight forward, and the processing is done by cascaded stages. The biggest problem

with the implementation is caused by limited dynamic range. Signals are squared as soon as they enter the device (or circuit). This causes a signal with a 10:1 dynamic range to become 100:1 after the squaring circuit. The dynamic range of input signals must therefore be limited to the square root of the dynamic range internal to the detector. The advantages with this scheme include wide bandwidth and high speed accuracy.

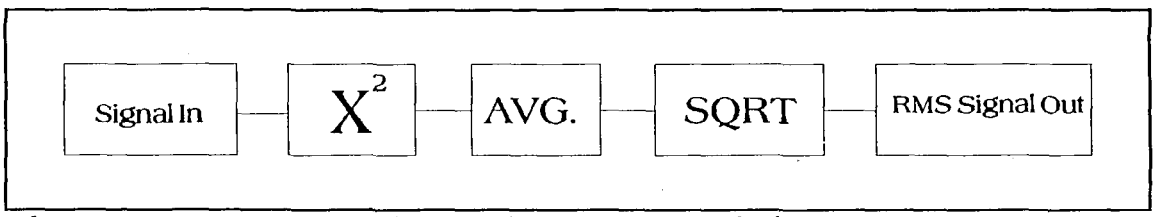


Figure 1. RMS Detection Using the Explicit Method of Calculation

To overcome the limitations in the explicit conversion, the equation for calculating RMS was manipulated to reorder the operations. Feedback is used to scale the input as it is being squared, thereby reducing the dynamic range restrictions. The first stage now not only squares the input, but at the same time, it calculates an implicit square root by dividing by the average value at the output. The second stage finds the average value. The implicit method results in greater dynamic range and fewer components. This in turn translates into lower cost to implement. There are new problems introduced by this method, however. Because of the feedback, bandwidth becomes an issue. Since the averaging filter is in the feedback path, it is limited to one pole.

Any additional poles will add more than 90° of phase shift, causing instability. The capacitors in the filter determine the settling time.

There are two types of circuitry commonly used to calculate RMS using the implicit method. The first uses direct multiplication and division using standard multiplier/divider chips.

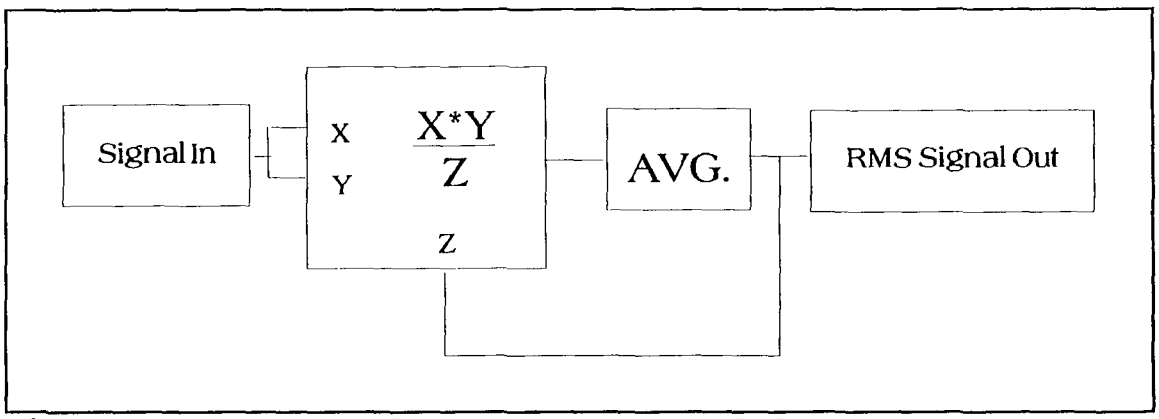


Figure 2. RMS Detection Using the Implicit Method of Calculation

The second type uses log/antilog techniques. The logging technique further reduces the restraints on dynamic range.

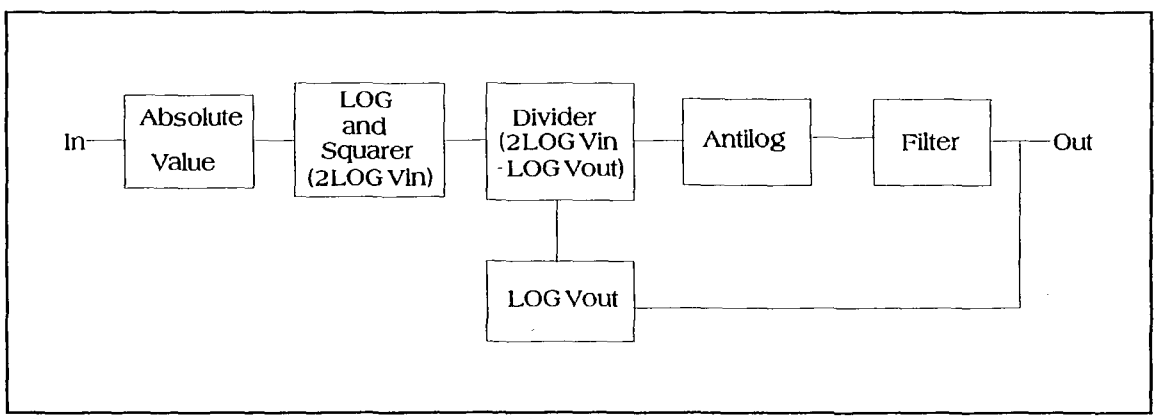


Figure 3. Implicit Calculation Using Log Domain

The log/antilog circuitry is not used in the explicit

case because of the lack of log domain filters. The log signal must be converted back to normal scale before the averaging filter. Because the averaging occurs before the square root, the antilog of the signal will again impose dynamic range restrictions. The goal of this work is to show that a new method of filtering using nonlinear processing in the log domain is ideally suited to function as the averaging circuit in an explicit RMS detector.

The dynamic range problems of the explicit detector can be overcome by operating completely in the log domain. By using a filter that operates on a signal that has been logged, the problems of the explicit detector are avoided. The input to the detector can be logged, squared (doubled in the log domain), averaged using the new filter, and square rooted (divided by two in the log domain). The result is then exponentiated to convert back to the original domain.

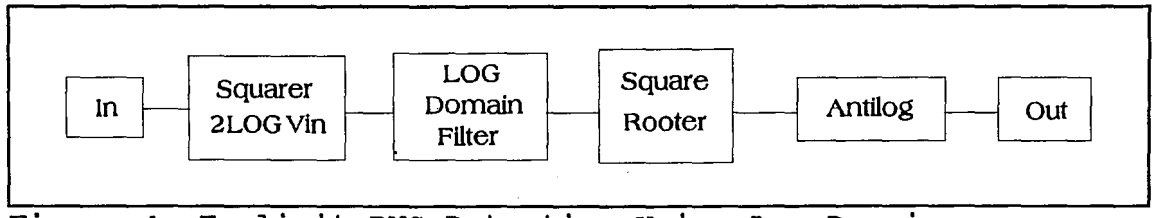


Figure 4. Explicit RMS Detection Using Log Domain Techniques

This value is the RMS value of the input computed explicitly without the normal disadvantages.

The entire circuit for RMS detection will be developed in this work, but the effort is directed mainly at the application of log domain filters to the averaging circuit.

Chapter 2.0: Filtering in the RMS Detector

The background and foundation of the general RMS detectors were covered in Chapter 1. This chapter will cover the basics behind the filtering section in the detectors. Some background on log domain filtering will also be covered.

Section 2.1: Averaging Circuit in RMS Detectors

The averaging in an RMS detector is typically done using a single pole, low pass filter. The measurement of RMS is done over some predetermined time period. The time period is the "memory" of the circuitry and is set by the time constant of the filter. Low pass filters average by their very nature. In implicit systems, the averaging time and settling time must be balanced to achieve the desired results. Since this work is directed at explicit calculation, the balance is not as critical due to a lack of feedback.

The first step taken was to look at the filter itself. The industry standard is a single pole filter because of the stability concerns. With the hope of defining a sharper cutoff on the average window or circuit "memory", equations were developed for second, third, and fourth order circuits. Not only will log filters be applied for explicit calculation, but better averaging circuits using this concept will also be addressed.

The averaging filter determines how the time window over

which the RMS value will be calculated. Ideally, a time period, τ, would be defined and the input signal would be equally weighted in that time period. Input signals outside that time period would be weighted by zero and not figure into the calculation. This concept can be thought of as a unity gain sliding window with duration τ.

To approximate the sliding window, it is desirable to have an impulse response that has quick rise and fall times with a flat amplitude for a fixed duration. This project will show that higher order analog filters can be used to attain better approximations to the square pulse window.

The first step was to determine the desired response. The Laplace transform of a square pulse is $1/s*(1-e^{-sT})$. The Taylor expansion of this response was used to develop the filters. By equating the transfer function of a higher order filter with the first several terms of the Taylor expansion of the square pulse, an approximation could be made.

This mathematical approximation was carried out for second, third and fourth order filters. The transfer functions for these filters are shown in equations one through three.

Second Order

$$\frac{12}{s^2+6s+12} \qquad (1)$$

Third Order

$$\frac{2s^2+120}{s^3+12s^2+60s+120} \quad (2)$$

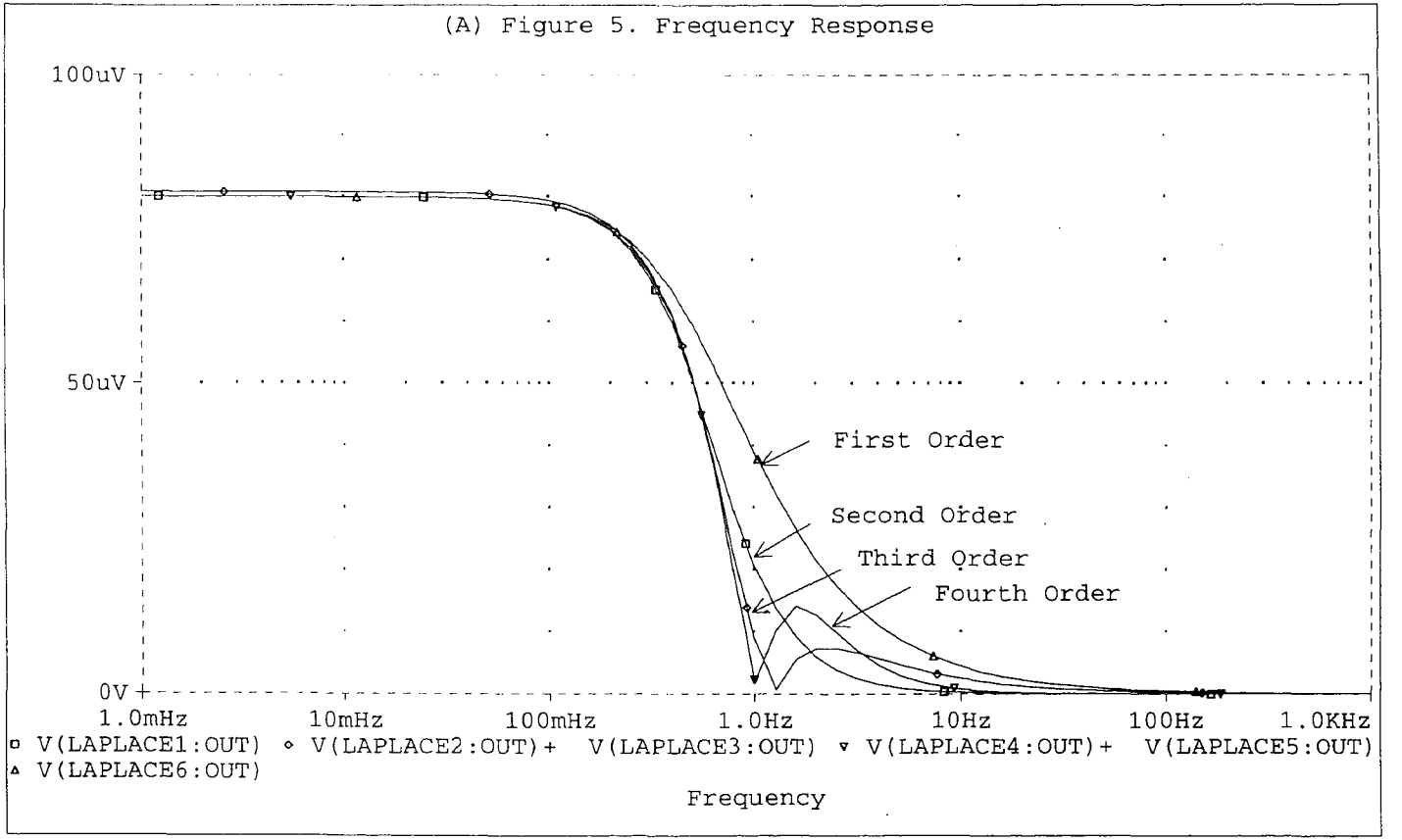
Fourth Order

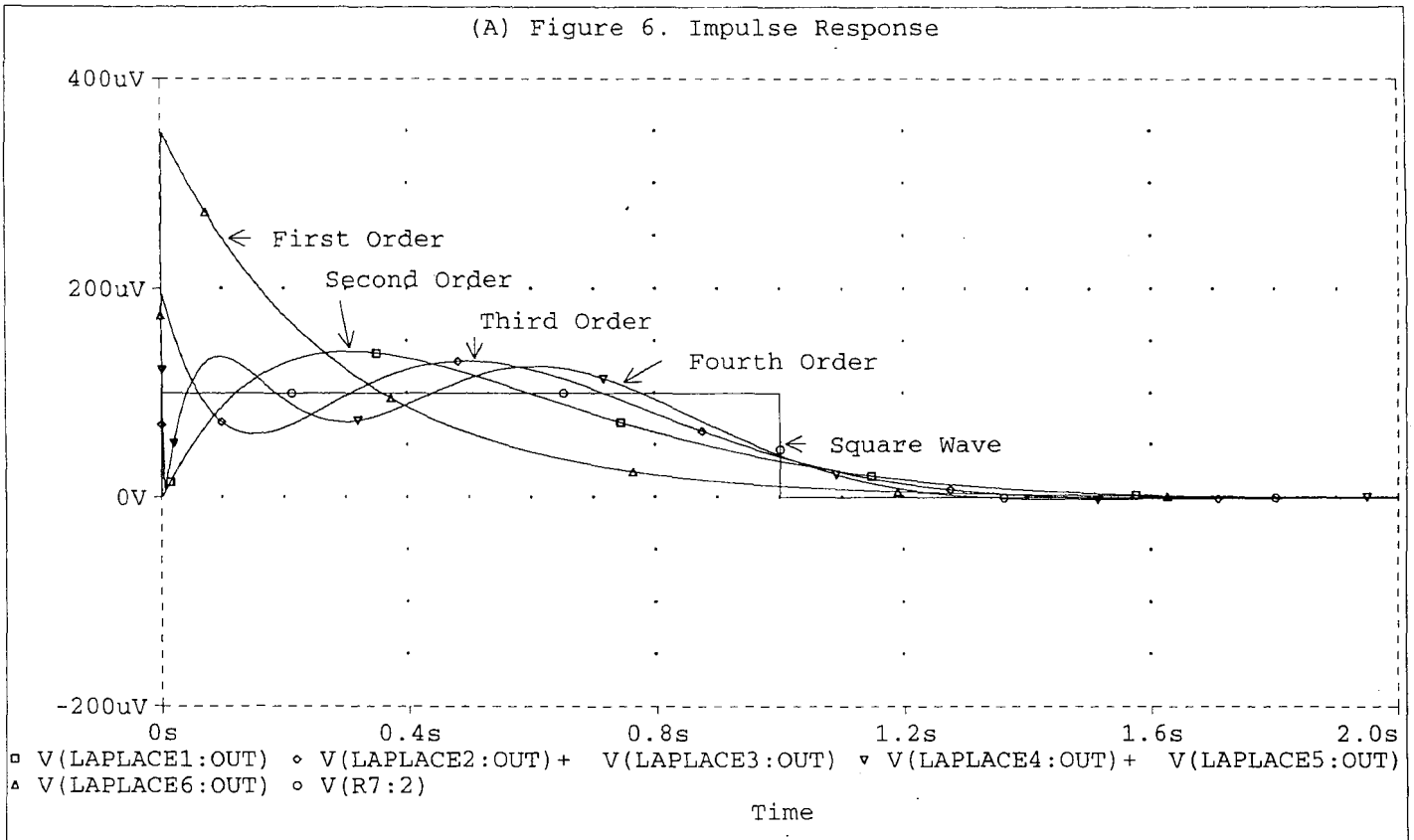
$$\frac{40s^2+1680}{s^4+20s^3+180s^2+840s+1680} \quad (3)$$

The impulse response of each of the transfer functions was modeled using the analog circuit behavioral modeling tool in Design Center by Microsim.

The second order response resembled a half period of a cosine wave with very sharp rise and fall times. The third order response had a second sharper peak on the rising edge. The fourth order response also had double peaks but seemed to be getting closer to the desired square pulse because the peaks were becoming more symmetrical. As expected, the cutoff became sharper in the frequency domain as the order of the filter was increased. See Figure 5 for the frequency responses and Figure 6 for the impulse responses described above. An example of the square pulse that is the ideal implementation of the filter is also shown with the impulse responses. The standard one pole filter that is used in implicit detectors is also shown for illustrative purposes.

In order to come closer to a real world model, the equations were transformed into smaller subsections that could


(A) Figure 5. Frequency Response
100uV
50uV
0V
First Order
Second Order
Third Order
Fourth Order
1.0mHz
10mHz
100mHz
1.0Hz
10Hz
100Hz
1.0KHz
V(LAPLACE1:OUT)
V(LAPLACE2:OUT)
V(LAPLACE3:OUT)
V(LAPLACE4:OUT)
V(LAPLACE5:OUT)
V(LAPLACE6:OUT)
Frequency


(A) Figure 6. Impulse Response
400uV
200uV
0V
-200uV
First Order
Second Order
Third Order
Fourth Order
Square Wave
0s
0.4s
0.8s
1.2s
1.6s
2.0s
V(LAPLACE1:OUT)
V(LAPLACE2:OUT)+
V(LAPLACE3:OUT)
V(LAPLACE4:OUT)+
V(LAPLACE5:OUT)
V(LAPLACE6:OUT)
V(R7:2)
Time

be modeled as biquad filters. The third and fourth order responses were decomposed into first and second order sections. Partial fraction expansion was used and the sections were summed (a cascaded solution did not seem as desirable with the log domain filters). The mathematical equations were again checked before any circuitry was designed.

It should be noted that some slight differences were evidenced at this modeling point. These differences were due to truncation and round off error in the mathematical model. The fourth order equation was the most sensitive. The parameters seemed very reasonable. The highest Q was below one. The ω's in these circuits were all below 10. All waveforms were normalized to approximate an ideal window of one second duration. Using different durations of the ideal window would produce different ω's. The frequency can easily be scaled for any response later in the design.

The equations were broken down into first and second order stages to allow the filters to be designed in more manageable sections. These stages are in parallel because of the partial fraction expansion. This means that the input is fed to each section and the outputs are summed. A background on the theory and design of log filters is now appropriate.

Section 2.2: Log Domain Filters

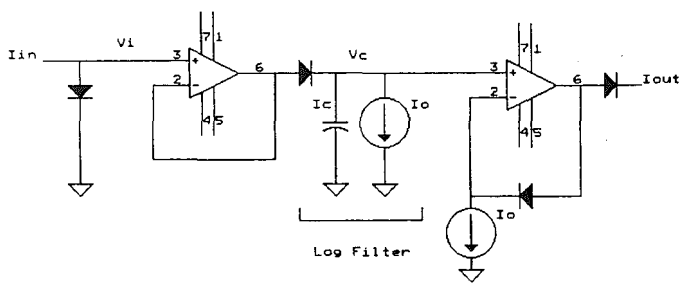
This section will cover some of the background on log

domain filters. The evolution and some very basic theory will be covered. The goal here is not to describe the exact theory behind the filter sections, but to provide enough background so that the filters designed later make sense. Since the general biquad model has already been developed, it is not necessary to redevelop it each time. There are some simple equations that can be used to change the parameters for specific applications.

Adams[1] introduced the idea of filtering in the log domain. He showed that processing on the natural logarithm of an input signal could produce an output that was a filtered version of the input once the signal was exponentiated. His circuitry consisted only of diodes, capacitors, current sources, and operational amplifiers. Although the processing is nonlinear, the overall transfer function produced a linear filtering on the input. By changing the value of the internal current sources, the filter itself becomes tunable.

The introduction of this concept was completed with a simple example. The circuit is shown in Figure 7.
V_c is the log of a linearly filtered version of the input. The Op Amp acts as a level shifter and the last diode acts as an exponentiating circuit. Equations 4 through 12 show the results analytically.

$$V_i = \frac{1}{k} \ln\left(\frac{I_i}{I_s}\right) \tag{4}$$



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$$I_C = I_S e^{k(V_i - V_c)} - I_O = C\frac{dV_c}{dt} = CV_c \tag{5}$$

$$I_{out} = I_s e^{k[V_c + (1/k)\ln(I_o/I_s)]} = I_o e^{kV_c} \tag{6}$$

where k = q/KT.

Combining the above equations yields

$$C\dot{V}_c e^{kV_c} = -I_o e^{kV_c} + I_s e^{kV_i} \tag{7}$$

$$= -I_o e^{kV_c} + I_s(I_i/I_s) \tag{8}$$

$$= -I_o e^{kV_c} + I_i \tag{9}$$

Defining X = e^{kVc} yields

$$C\frac{dX}{dt} + kI_o X = kI_i \tag{10}$$

$$I_{out}=I_o X \tag{11}$$

Therefore,

$$\dot{I}_{out}+\frac{kI_o}{C}I_{out}=\frac{kI_o}{C}I_i \tag{12}$$

Equation 12 is a linear differential equation relating I_{in} to I_{out}. The result is that the output is equivalent to that of a one pole, low pass filter with a cutoff frequency of kI_o/C. The kI_o term can be related to the resistance in a small signal model of a filter. The small signal model has cutoff equal to 1/RC. Setting the cutoff frequencies from the log model and the small signal filter model equal to one another yields $1/RC = kI_o/C$ or $R = 1/kI_o$. This means the diode has a dynamic impedance inversely proportional to the quiescent current flowing through it. The I_o term allows for the electronic tuning of the filter.

A complete methodology for log domain filter design was developed by Frey[2]. Drawbacks such as inherent non-linear distortion were overcome with the elimination of the Op Amps and a more structured mathematical design procedure. By replacing the operational amplifiers, higher speed and

bandwidth were gained by using a strictly current-mode approach.

The design technique begins with the desired transfer function for the filter. A general, second order biquad section provides the basis for this particular work.

$$H(s)=\frac{as^2+b\omega_o s+c\omega_o^2}{s^2+s\omega_o/Q+\omega_o^2} \tag{13}$$

The transfer function is then transformed to the state space realization shown in equations 14 and 15.

$$\begin{vmatrix}\dot{x}_1\\ \dot{x}_2\end{vmatrix}=\begin{vmatrix}0 & 1\\ -\omega_o^2 & -\omega_o/Q\end{vmatrix}\cdot\begin{vmatrix}x_1\\ x_2\end{vmatrix}+\begin{vmatrix}B_1\\ B_2\end{vmatrix}\cdot aU \tag{14}$$

$$Y=\begin{vmatrix}1 & 0\end{vmatrix}\cdot\begin{vmatrix}x_1\\ x_2\end{vmatrix}+aU \tag{15}$$

where:

$B_1 = (b-a/Q)\omega_o$

$B_2 = [c-(b-a/Q)/Q-a]\omega_o^2$

There are many equivalent state space models of the linear transfer function. Some of these sets will not allow the direct implementation with real world circuit compo-

nents. Because of this problem, the translation from the transfer function to the state space model must meet certain constraints. The final state matrix is then scaled to produce a set of nodal equations.

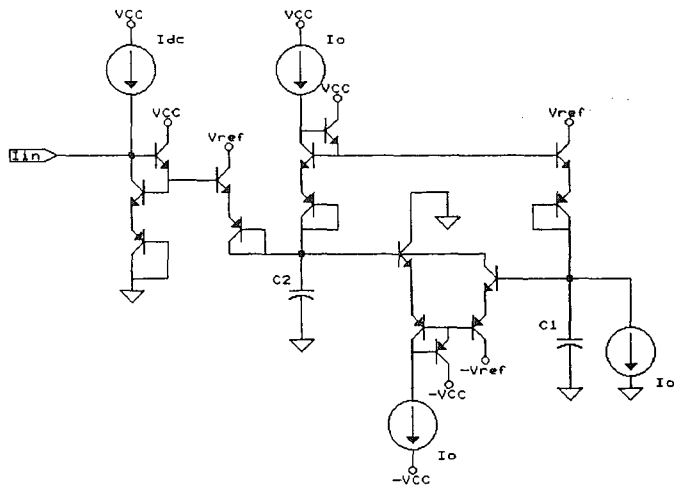
At this stage, variables that were part of the mapping are constrained by fixing a frequency value to a current value. This pairing is done with the maximum current and maximum frequency at which the filter will be expected to operate. The nodal equations are then used to develop circuitry. Figure 8 shows the circuitry for the general implementation of the biquad transfer function.

The I_{DC} current at the input is injected to assure that the transistors are biased on for all values of I_{in}. Also note that each diode junction is synthesized by an NPN and PNP pair of transistors. This pairing is done to eliminate the need to match NPN and PNP characteristics that is present when the devices are used by themselves. The four transistor groupings also have a fifth transistor added. This improvement compensates for degradation that occurs when the gain approaches the ß of the transistors. The fifth transistor improves the current gain by ß. It also reduces the base current errors (the base does pass some current, unlike the ideal model).

The output equation for the biquad circuit is:

$$y = I_{c1}e^{kV1} + I_{c2}e^{kV2} + DU \qquad (16)$$

This equation shows that the final output is achieved with a



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linear combination of various output nodes in the circuit (the traditional voltage based biquad also requires a combination to produce the output).

It should be noted that log domain biquads can produce lowpass, bandpass, and highpass responses depending on how the node outputs are summed. Also, log filters can be cascaded or summed like traditional filters to produce higher order circuits.

Chapter 3.0: Designing the Detector Sections

The filtering concepts from the last chapter are applied to the RMS detector application. A front and back end are developed to complete the design of each of the RMS detector blocks from Figure 4.

Section 3.1: Application of Log Filters to the Averaging Circuit

The basic model of the biquad filter can be applied to any design criteria. The general section which was developed from the parameters a, b, and c can have the specific values substituted in. From these variable values, the circuit component values can be calculated and the circuit tailored to generate a particular transfer function. Circuits of higher order can be created by breaking the large circuit into smaller first and second order sections.

The first step in the design of a log domain filter is to develop a desired transfer function. The transfer function must then be broken into simplified biquad sections. The transfer functions for the desired second, third, and fourth order responses have been developed and shown above. The third and fourth order equations must be simplified and put in the proper form.

To simplify these two equations, there are two possible methods. The first is to break the equations into the product of sections. Each section would have at most a

quadratic term in the denominator. This would result in a squared term in the numerator of these specific equations. Building a biquad with this term requires a straight feed through of the input to the output. Although this is not a problem, it is not as desirable as a system in which only the output from the filter is used. If this method was chosen, the filter sections would be cascaded.

The other simplification strategy involves partial fraction expansion. This expansion will result in a sum of lower order transfer functions. Each section's output is then summed to generate the total response. This method was used to generate the sections used in this design. The choice was based on a design preference that simplifies the circuitry. The equations that will be used to generate the biquad filters are as follows.

Second Order

$$\frac{12}{s^2+6s+12} \tag{17}$$

Third Order

$$\frac{12.35}{s+4.6}+\frac{-10.35s-43.28}{s^2+7.36s+25.84} \tag{18}$$

Fourth Order

$$\frac{4.595s-54.23}{s^2+8.42s+45.95}+\frac{-4.595+79.71}{s^2+11.58s+36.5} \tag{19}$$

From these equations, the coefficients are easily calculated. For the second order response, a and b are

equal to zero and c is one. The third order is in two parts. The first part yields a equal to zero, b equal to -2.036, and c equal to -1.675. The second part is first order with c equal to 12.35. The fourth order section also has two parts. The first has coefficients b equal to .678 and c equal to -1.18. The second section is made of b equal to -.760 and c equal to 2.180.

The values of Q and ω must also be determined. The Q's and ω's are shown below.

Second Order:	Q = .5774	ω = 3.464 Radians
Third Order:	Q = .6907	ω = 5.083 Radians
		ω = 4.600 Radians
Fourth Order:	Q = .8051	ω = 6.779 Radians
	Q = .5221	ω = 6.046 Radians

Other values that must be determined include k and λ. The value of k is equal to twice q/KT because there are two diode junctions caused by the NPN and PNP pairing. K can be selected arbitrarily. λ is equal to I_{max}/ω_{max} or any other pairing of a current and frequency. I_{max} is the maximum current that will be allowed to flow through the circuit. It should be chosen so that all transistors are biased properly. It should also be such that normal operating currents through the base emitter junction approximate a pure exponential relationship. I_{max} will be set to be 100 μA. ω_{max} will be set at the actual value of ω required for each section. This value is chosen because the filters will not be

tuned in this proof of concept. For future applications, it would be desirable to set ω_{max} higher to allow tuning of the time window for specific applications of the detector. Since ideal transistors are being used to simulate the design, current and frequency values may exceed the maximum values set above. The maximum values are only important when real components are being used in the design.

The value of the capacitors can now be calculated. There are two capacitors for each biquad section. The equations to calculate the values follow.

$$C_1 = (k\lambda/2Q)\{\sqrt{(1 + 4Q^2)} - 1\} \quad (20)$$

$$C_2 = (k\lambda/2Q)\{\sqrt{(1 + 4Q^2)} + 1\} \quad (21)$$

Substituting the application variables into equations 20 and 21 gives the following values for the capacitors.

Second Order: C1 = 263.77 μF C2 = 1263.55 μF

Third Order: C1 = 200.94 μF C2 = 770.57 μF

C3 = 434.78 μF

Fourth Order: C1 = 164.05 μF C2 = 530.36 μF

C3 = 141.18 μF C4 = 774.72 μF

The capacitor in the single pole section of the third order equation was calculated using the equation $C = kI_o/\omega_o$. The capacitor values are too large to be realizable on a typical silicon integrated circuit, but are suitable to prove the concept of applying this type of filtering to RMS detectors.

The values can easily be scaled at a later time.

The final calculations required involve the current sources feeding the grounded capacitors. These sources directly figure into the output equation:

$$y = I_{c1}e^{kv1} + I_{c2}e^{kv2} + DU \qquad (22)$$

The DU term is equal to zero because of the decision to simplify so that the a coefficient was equal to zero. The D matrix includes the a coefficient.

The currents can be calculated using the following equations:

$$I_{c1} = (\Lambda/Q - 1)a - \Lambda b + c \qquad I_{c2} = -(1/Q)\Lambda a + \Lambda b$$

$$\Lambda = 1/(2Q)\{\sqrt{(1+4Q^2)} + 1\} \qquad (23)$$

The currents may have a positive or negative value. The source itself does not take on a negative value, it only determines whether it will push or pull current in the output section. The branches for these currents are attached to a current mirror and the negative valued source branches pull current from the output side. The following values were calculated for the higher order circuits.

Third Order	IC1 = -90.11 μA	IC2 = -63.44 μA
Fourth Order	IC1 = -239.88 μA	IC2 = 121.90 μA
	IC3 = 396.01 μA	IC4 = -178.00 μA

The second order section does not have multiple terms in the numerator and does not require any scaling. The single pole

section of the third order equation also does not require any special output modification.

All component values for the circuit have now been determined. The values can be substituted into the basic biquad circuit and the output sections organized on the proper side of the current mirror. The schematics showing the second, third, and fourth order circuits are shown in Figures 9, 10, and 11 respectively.

Section 3.2: Discussion of Results

The customized log filters were modeled in PSPICE. Ideal transistor models were used throughout all the simulations. It has been shown by Frey[2] that real transistors behave in a manner that is almost identical to the ideal in circuits with Q's less than five and maximum frequencies less than 5 MHz. Although only the ideal case is being shown in this work, the prior work suggests that the use of real components would give similar results.

Both the frequency response and the impulse response were modeled for each of the three filters. The responses were measured using PSPICE's AC Sweep and Transient Analysis functions. Two parallel current sources were used to stimulate the input of the circuits. The first source was 80μA peak AC for the frequency portion. The impulse response was determined by stimulating the input with an impulse created using the source-pulse feature in PSPICE.

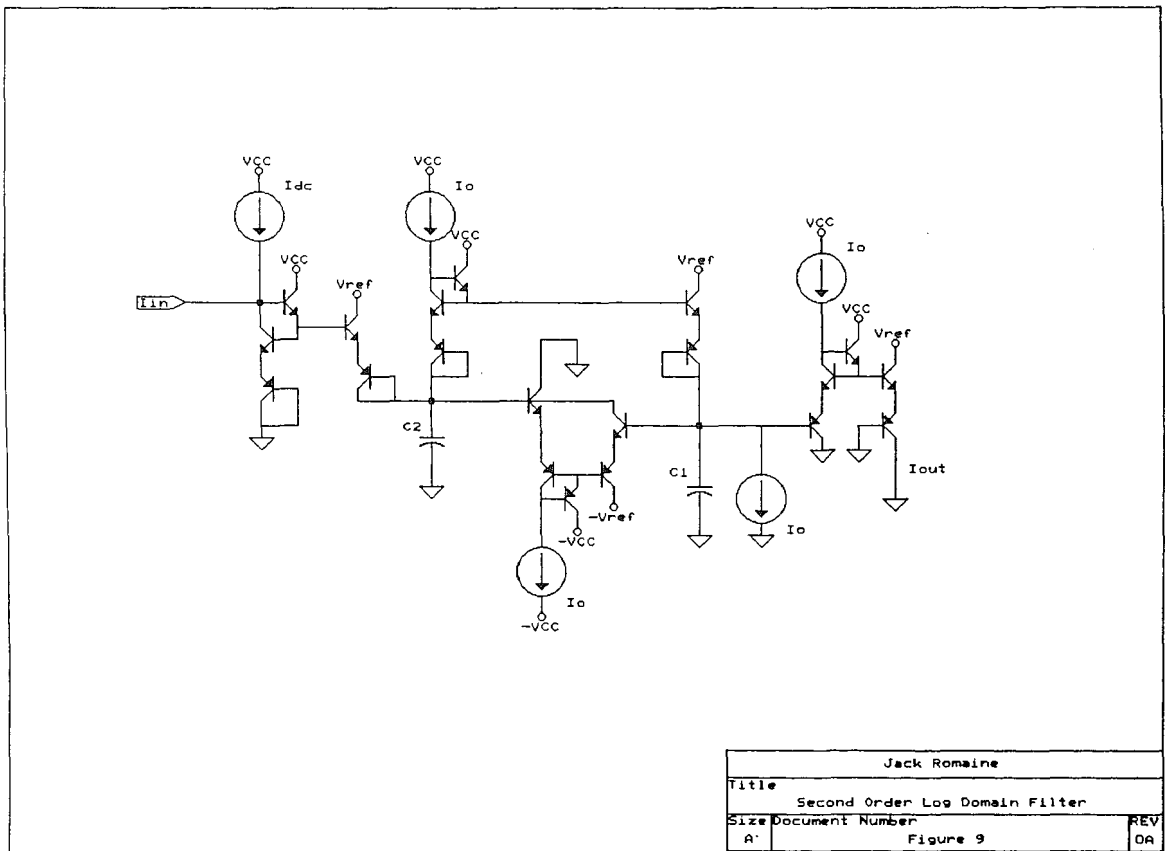
VCC
Idc
VCC
Vref
Iin
VCC
Io
VCC
Vref
C2
-Vref
-VCC
Io
-VCC
Vref
C1
Io
VCC
Io
VCC
Vref
Iout
Jack Romaine
Title
Second Order Log Domain Filter
Size
A
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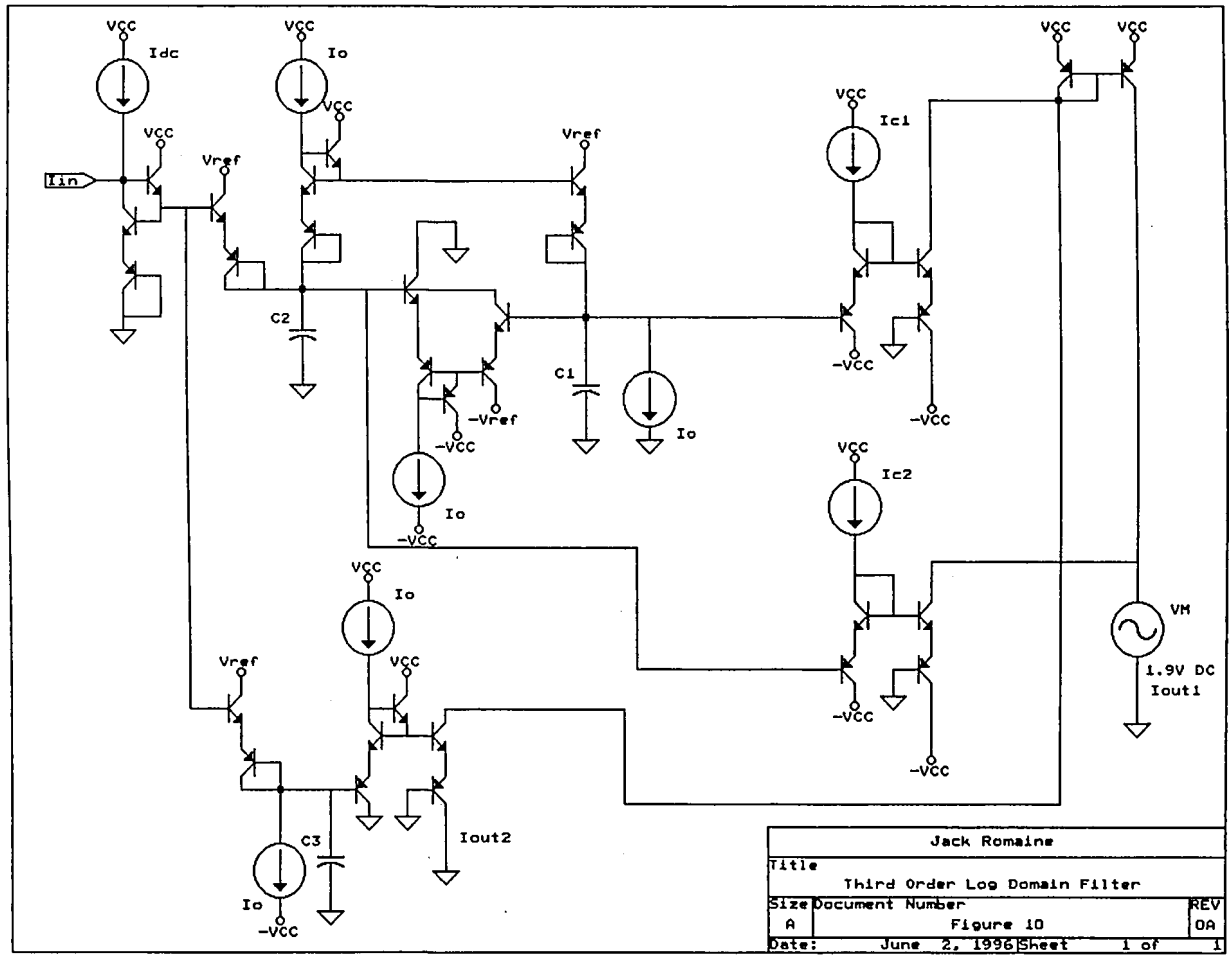
Figure 9
REV
0A
Date:
June 2, 1996
Sheet
1 of
1


VCC
Idc
Io
Iin
Vref
C2
C1
-Vref
-VCC
Ic1
Ic2
VM
1.9V DC
Iout1
Iout2
C3
Jack Romaine
Third Order Log Domain Filter
Figure 10
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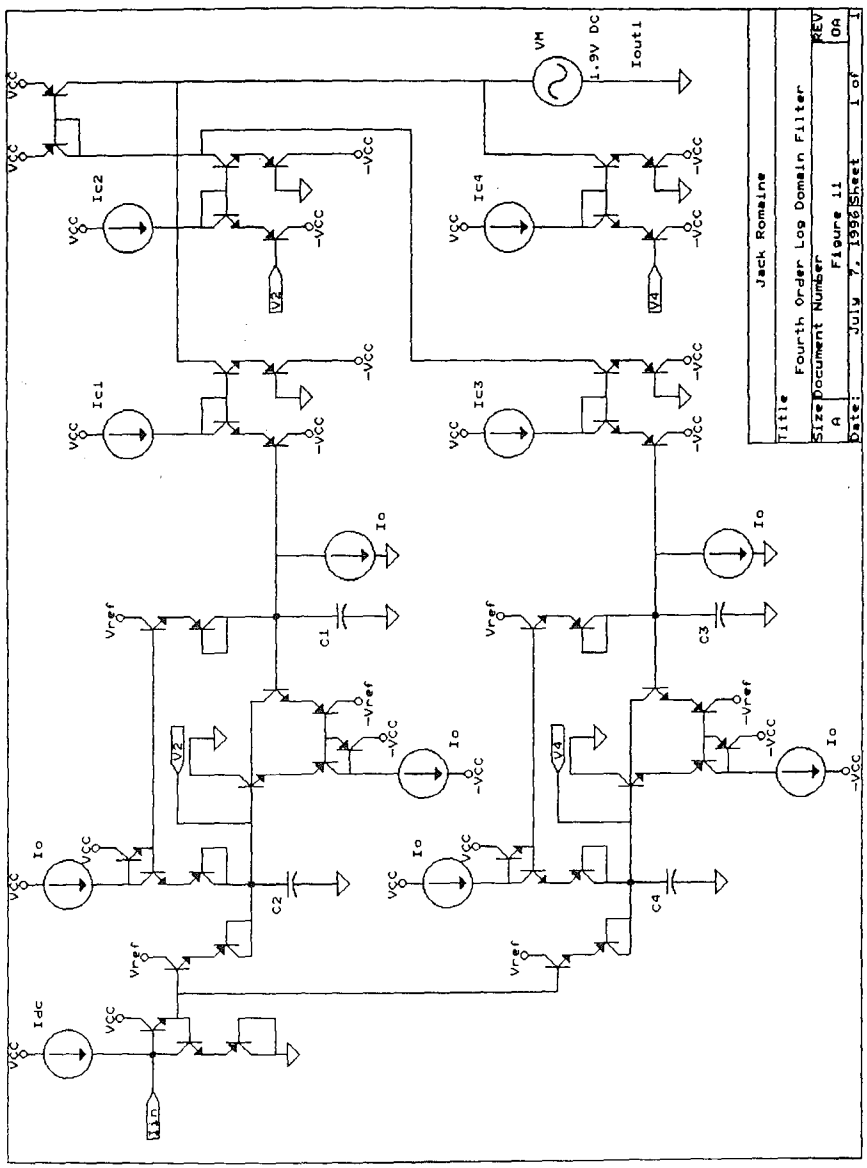
Jack Romaine
Fourth Order Log Domain Filter
Figure 11
July 7, 1998
VM
1.9V DC
Iout1
Idc
Io
Vref
C1
C2
C3
C4
Ic1
Ic2
Ic3
Ic4
V2
V4
Vin
VCC
-VCC

The waveform started at DC for 1μs then went to 100μA for 1ms with 1μs rise and fall times. The time differences between the pulse width of this waveform and the cutoff frequency of the filters makes this a sufficient approximation to a true impulse.

The results of this testing are expected to match the results shown in Figures 5 and 6. These circuits are using ideal parts to model the same transfer function that was modeled in these earlier figures. If the circuits were designed properly, the only differences should be in the roundoff error resulting from the calculation of the capacitor values and the capacitor currents.

Figures 12 through 17 show the modeled responses from the log filter circuits illustrated in Figures 9 through 11. Figures 12 and 13 show the frequency and impulse responses of the second order system. Both plots agree with the expected results. A comparison between the earlier figures and these shows no discernable differences. Figures 14 and 15 show the response of the third order filters. There is once again no difference that can be distinguished. Figures 16 and 17 represent the frequency and transient responses of the fourth order circuit. As expected these results match the expected responses. Based on this analysis, the log filter designs are correct. The mathematical transfer functions are being correctly modeled by the circuitry. The filter section that does the averaging has now been

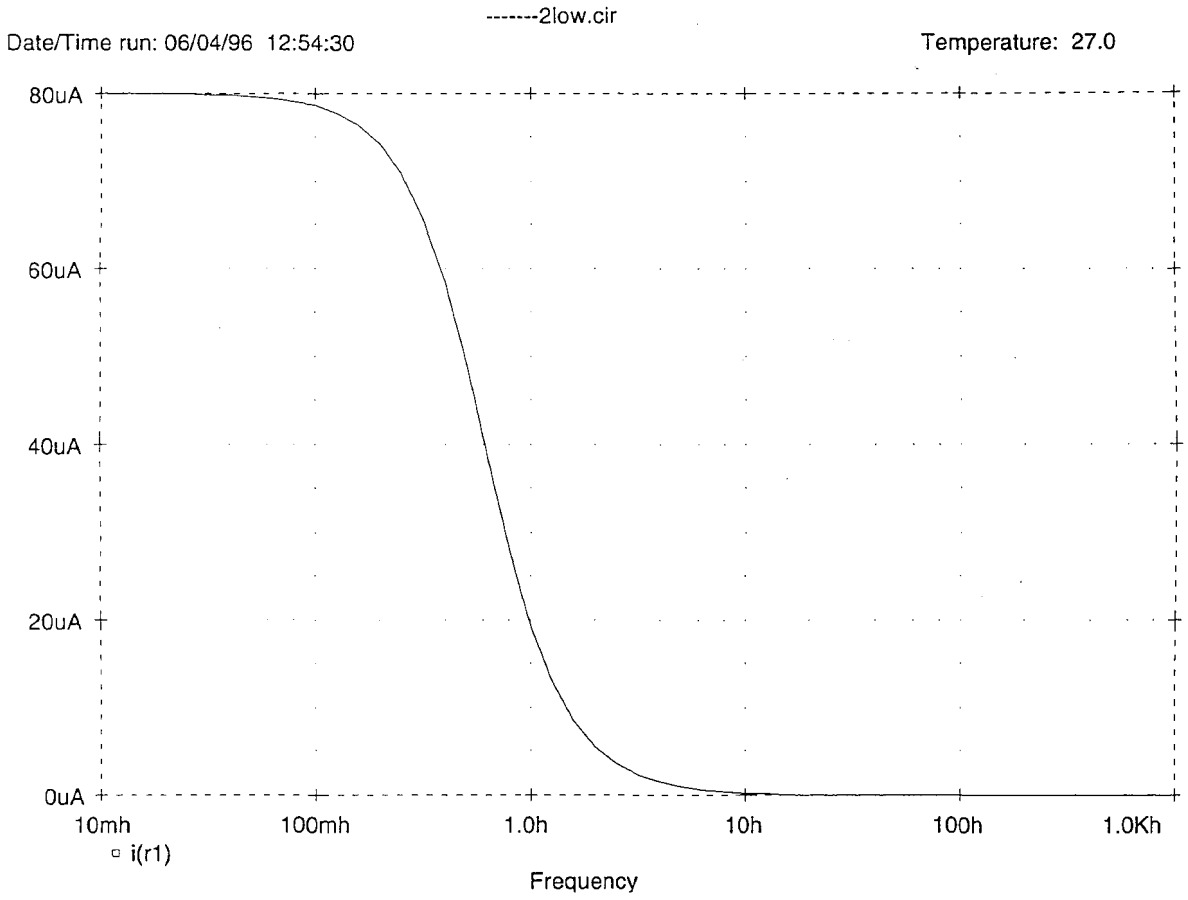

Figure 12. Second Order Frequency Response

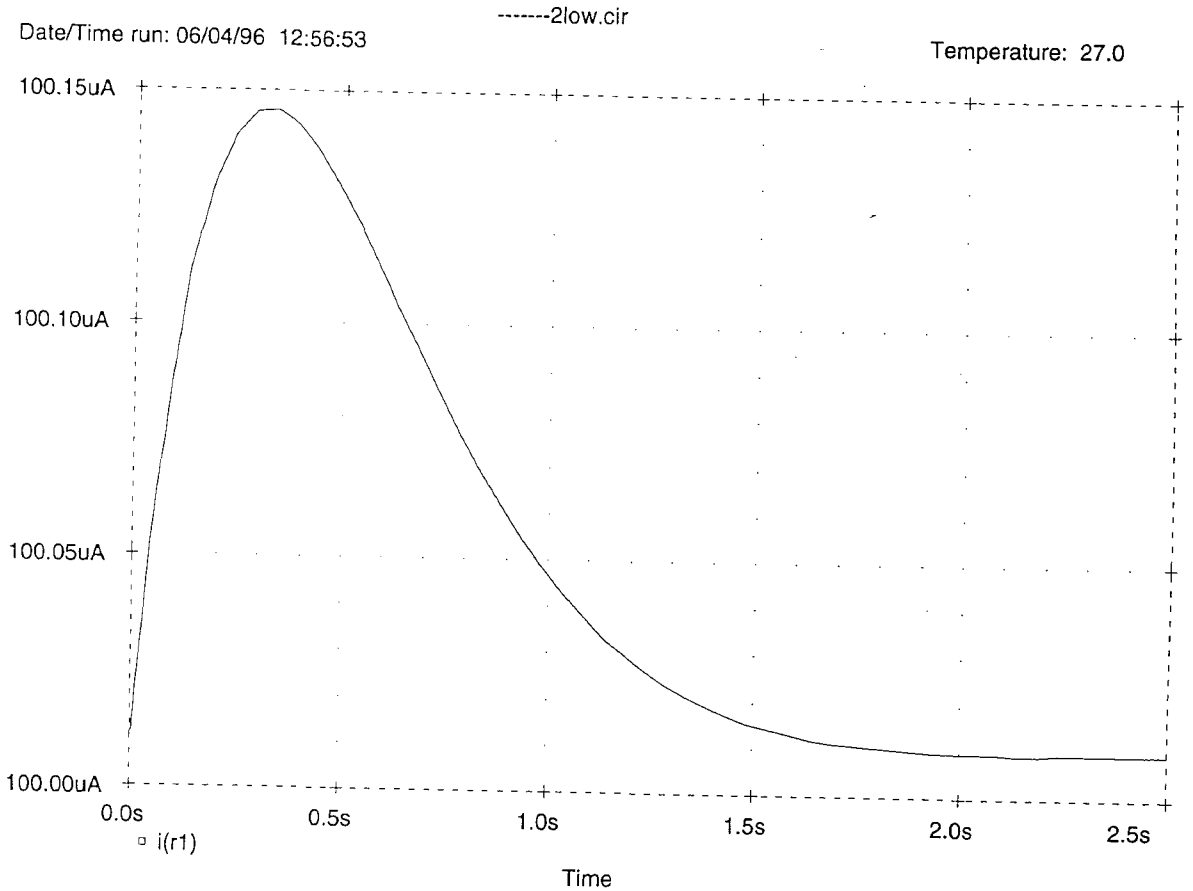

Figure 13. Second Order Impulse Response

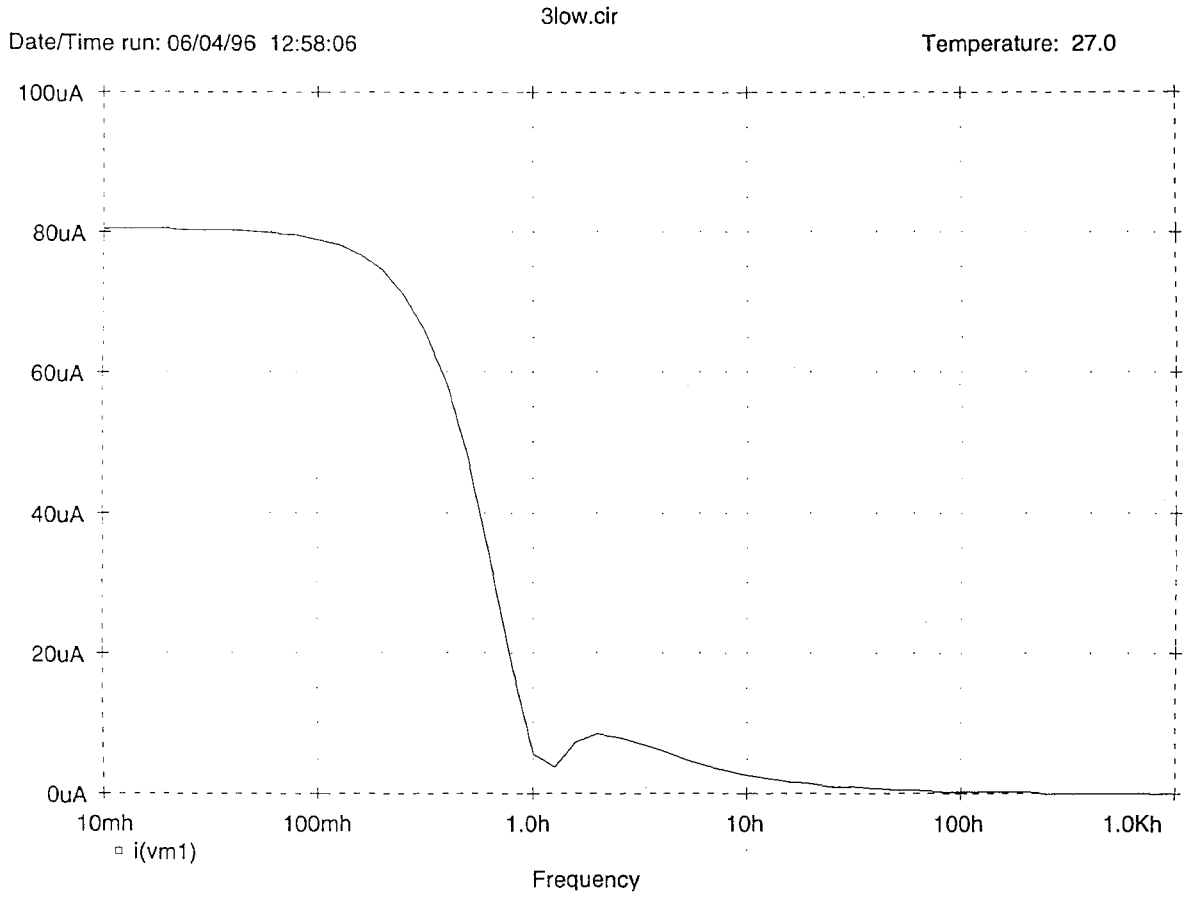

Figure 14. Third Order Frequency Response

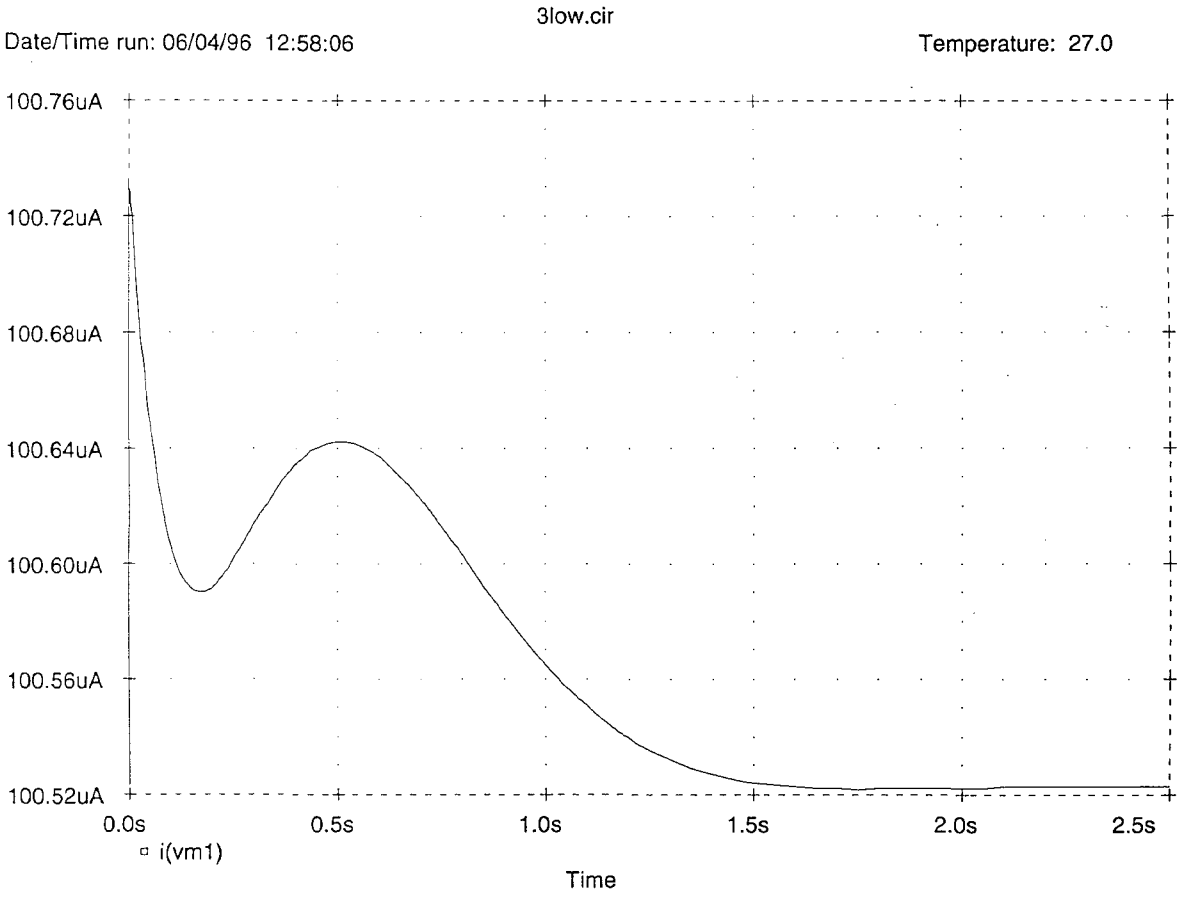

Figure 15. Third Order Impulse Response

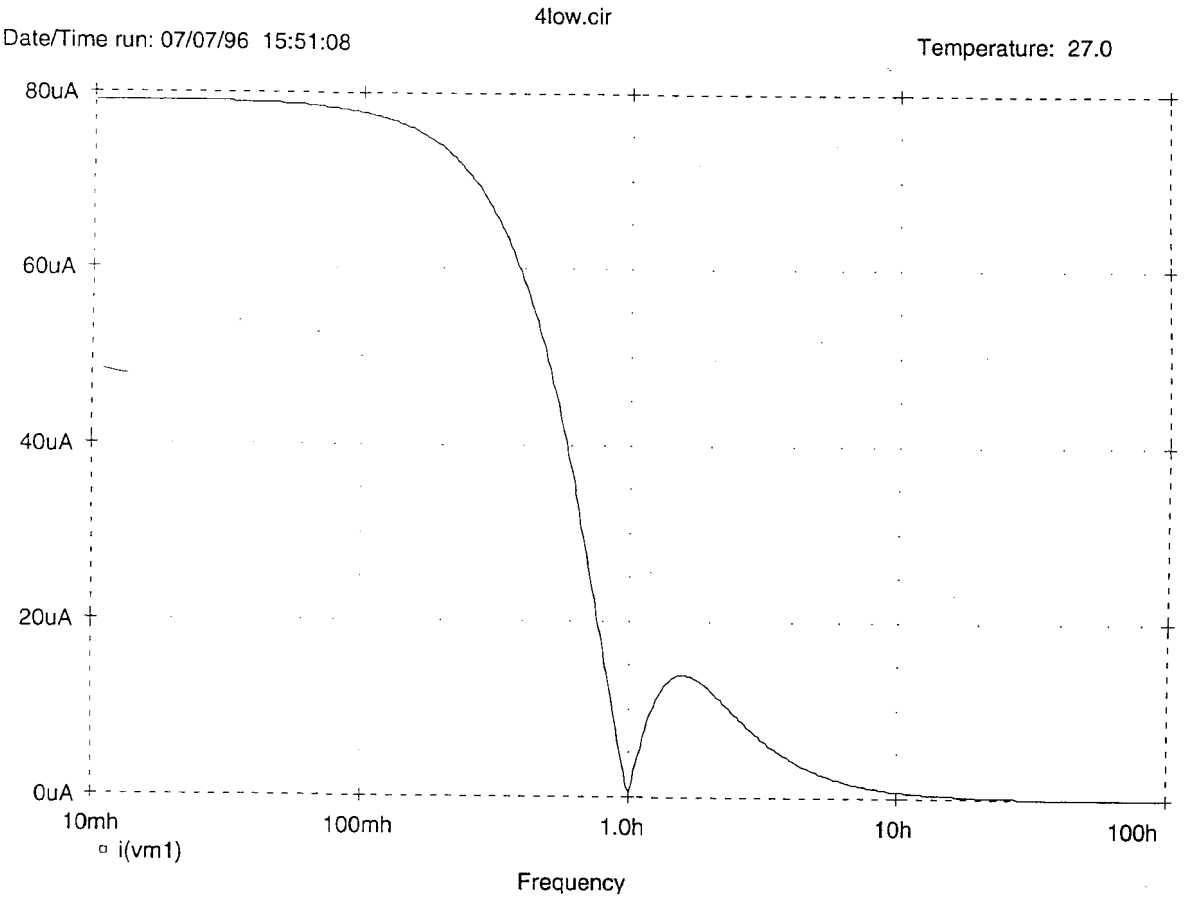

Figure 16. Fourth Order Frequency Response

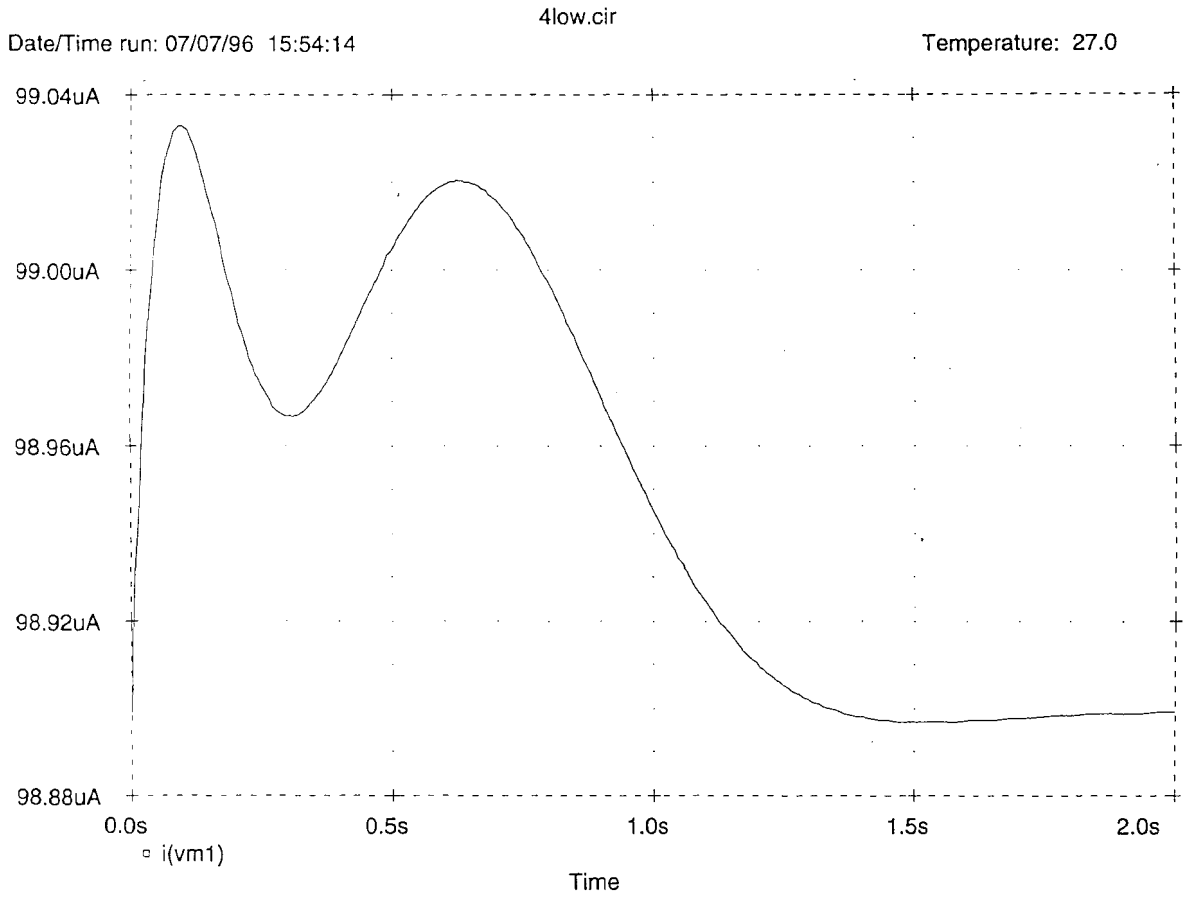

Figure 17. Fourth Order Impulse Response

completed with these log domain filters.

Section 3.3: Squaring Circuit

In Figure 4 (the proposed log based, explicit RMS detector) the first block in the diagram takes the log of the input signal. The second block effectively squares the signal by doubling the log ($x^2 = 2\log x$). In the implementation of this detector, these first two blocks will be combined into one circuit. The circuit operates by forcing the current through a diode junction to produce a voltage that is the log of the input signal. In this case, as in the log filters, each junction is made of an NPN and PNP pair to eliminate the matching concerns. The equation representing this is $V_i = (1/k)\ln(I_{in}/I_s)$. By adding a second set of junctions in series after the first, the equation is doubled. The doubling occurs because the current flowing through both sets of junctions is equal. This yields twice the natural log of the input.

$$V_i = (1/k)\ln(I_{in}/I_s) + (1/k)\ln(I_{in}/I_s) = (2/k)\ln(I_{in}/I_s) \quad (24)$$

A level shift on the input is also performed to raise the input level before the drop through these sets of junctions. The shift up is the same amount as the drop down, or in this case, two sets of junctions. The circuitry is shown in Figure 18.

Iout
Vref
Vcc
Iin
-Vref
-Vref
-Vref
Jack Romaine
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Logging and Squaring Circuit
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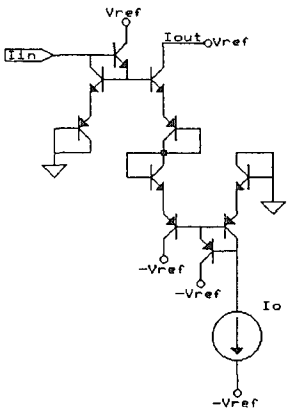
Section 3.4: Square Rooter

The final blocks in Figure 4 show a square rooter and an exponentiator. The square root is occurring in the log domain so it is simply a divide by two ([2logx]/2 = logx compared to $\sqrt{(x^2)} = x$). The last two sections will be combined in the same way as the first two sections were. Here, the inverse functions are taking place. The filter voltage is forced across a diode junction to produce a current. The current is an exponentiated version of the voltage $I_{out} = (I_s e^{kv})$. NPN and PNP pairs are again used for each junction. By cascading two junctions, the thermal voltage term is doubled, producing a $1/(2V_T)$ term, which translates to square rooting after exponentiating. The same level shifting required with the input circuit is also required here. Circuitry to perform these functions are shown in Figure 19.



Jack Romaine		
Title: Square Rooting and Exponentiating Circuit		
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Date: June 2, 1996	Sheet 1 of 1	

Chapter 4.0: A Complete RMS Detector Design

The sections developed in the last chapter are now combined into complete RMS detector designs. Four separate detectors are developed, one for each averaging filter. These designs are then tested and evaluated to show the benefits of the higher order sections.

Section 4.1: Putting It All Together - An Explicit RMS Detector

All of the sections in the block diagram in Figure 4 have now been described and shown individually. Now these circuits must be combined to create the complete RMS detector. The logging and squaring circuit accepts the input to the detector. It should be noted that this detector is set up to only accept positive input signals. This input restriction forces the absolute value of a waveform to be taken before applying it to the RMS detector. The front logging circuitry on the log filters must be stripped off since this function has already been taken care of. The back end exponentiating circuitry must also be stripped off of the log filters. This function will now be performed by the last stage. After the log filter comes the rooter/exponentiator. The output current from this last stage is the RMS level of the input to the first stage.

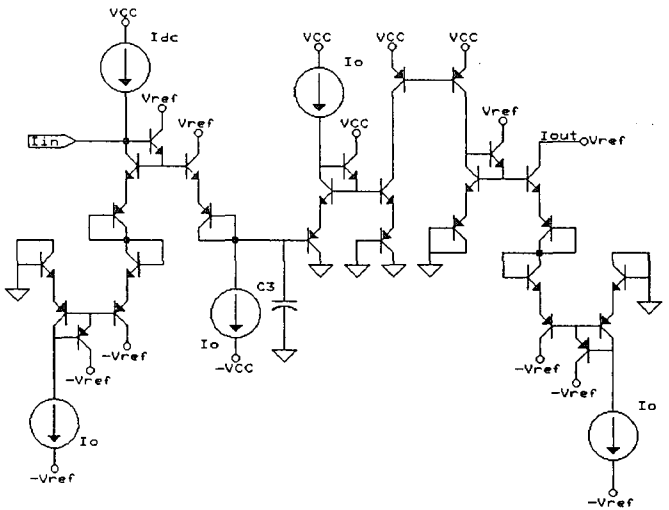
Four separate RMS detectors will be created. The

second, third, and fourth order circuits described above will be used, as well as a first order section to show the response of the most common detectors that are currently available. The only difference between these detectors will be the averaging sections. By creating four separate circuits, the effect of the averaging filter's order can be seen by looking at the overall output of the detector. The schematics showing the complete detectors are shown in Figures 20 through 23. Testing of the four detectors is done in the next section.

Section 4.2: Comparison of the Four Log Domain, Explicit RMS Detectors

The circuits will be stimulated with various input signals to compare how well they perform as RMS detectors. By injecting signals with known RMS values, the error from each detector can be measured and compared. The testing will begin with basic signals and progress to more complicated functions.

The first set of inputs to the detectors will be constant periodic signals. It is expected that no deviation will occur in any of the detectors. These inputs will show that the detectors calculate the correct RMS value. Three inputs will be included in this set. The first will be a sine wave with an 80μV peak. The second will be a 50% duty cycle square wave with 80μV peak. An 80μV peak square wave



Jack Romaine		
Title: RMS Detector w\First Order Filter		
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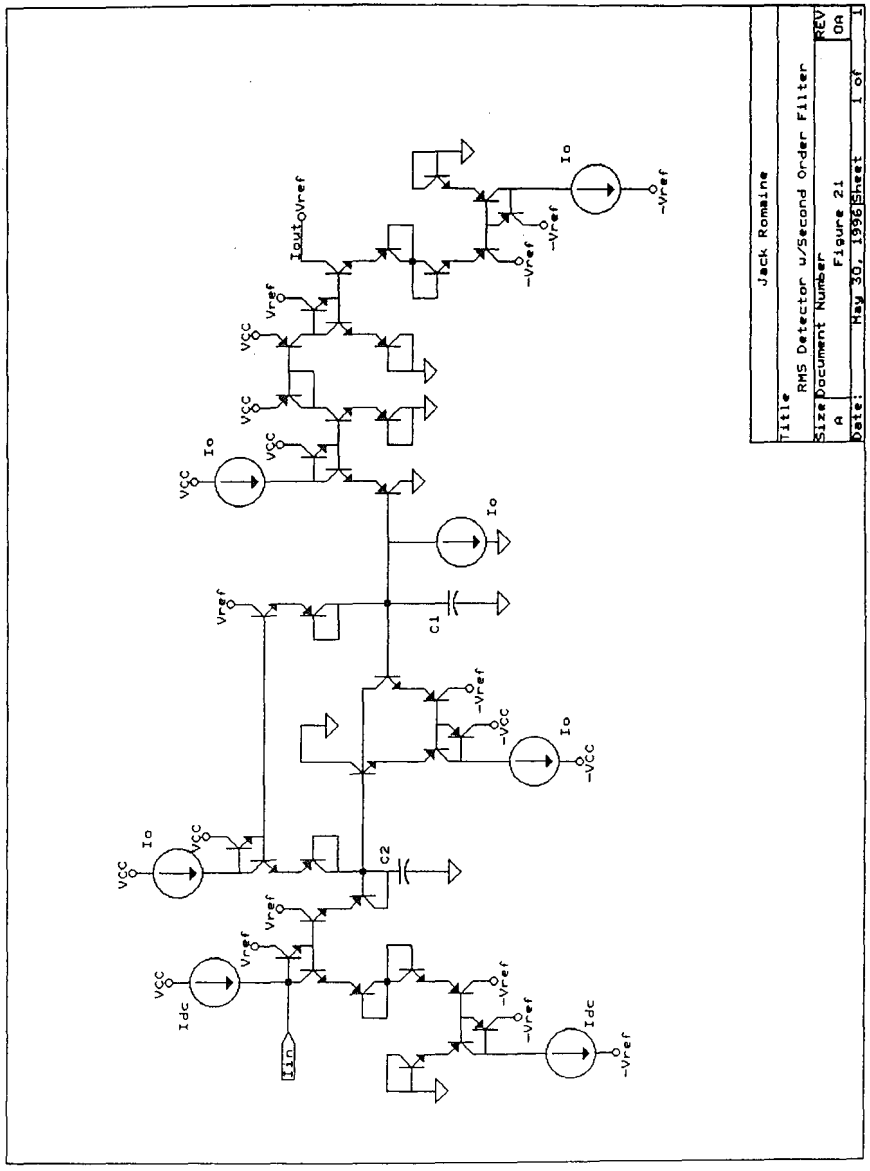
Jack Romaine
RMS Detector w/Second Order Filter
Figure 21
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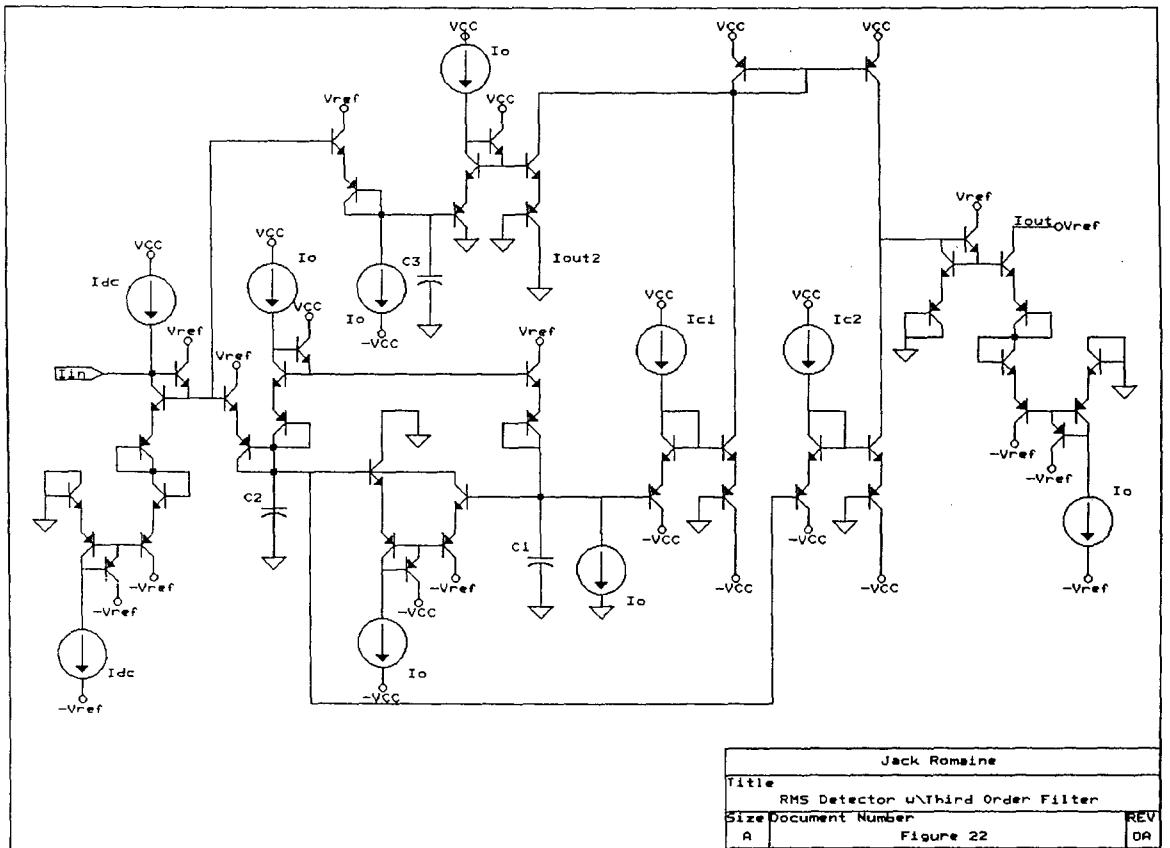
Sheet 1 of
Iout
Vref
-Vref
VCC
-VCC
Io
Idc
Iin
C1
C2


VCC
Io
Vref
Iout2
C3
Idc
Iin
C2
C1
Ici
Ic2
Iout
-VCC
-Vref
Jack Romaine
RMS Detector w\Third Order Filter
Figure 22
June 2, 1996

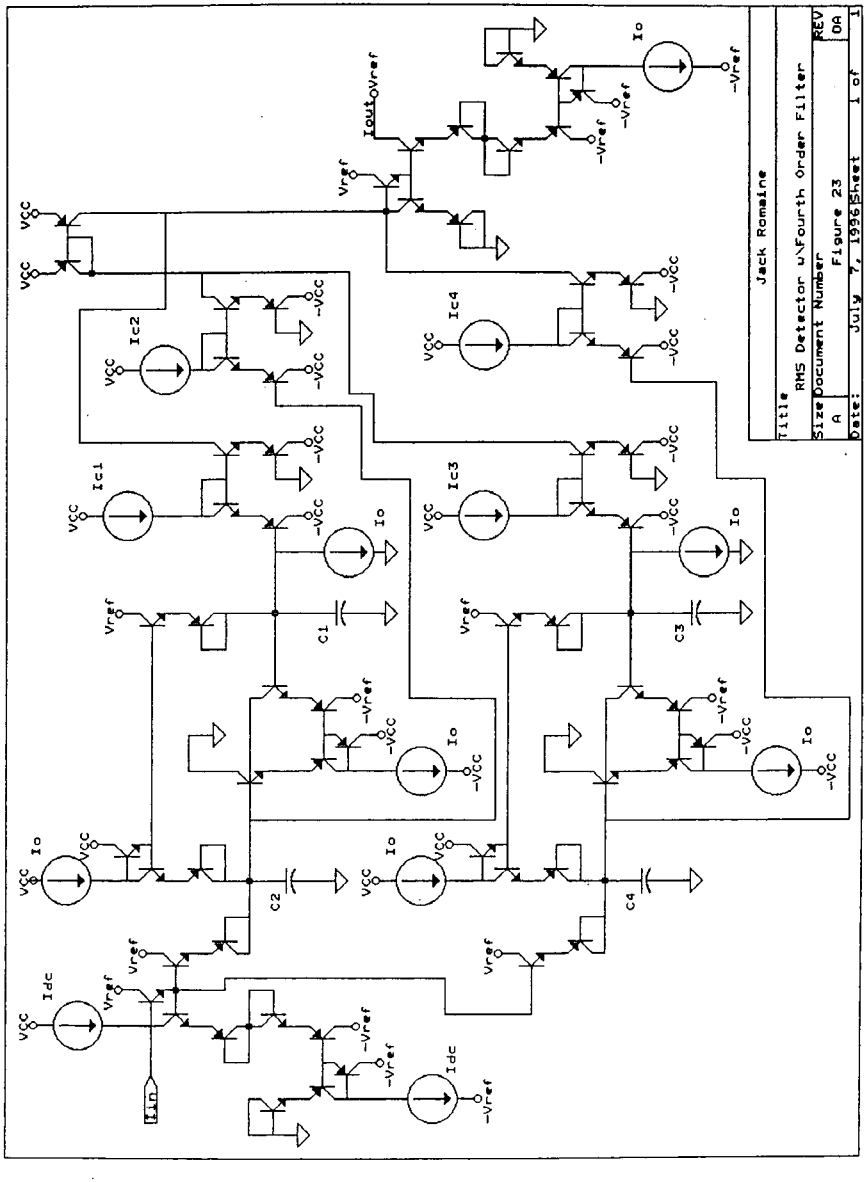

Jack Romaine
RMS Detector w\Fourth Order Filter
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Figure 23
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July 7, 1996
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1
Iout
Vref
-Vref
VCC
-VCC
Io
Idc
Ic1
Ic2
Ic3
Ic4
C1
C2
C3
C4

with a 10% duty cycle will be the final input of this test group. The expected outputs are 56.56μV, 80μV, and 10μV respectively.

The second set of inputs will test the transient response of the detectors and should show the differences in the averaging sections. The sine wave and 10% duty cycle square wave from above will be repeated, but the signals will now run for two seconds, abruptly stop and remain off for two seconds, and then start again. This will show the charge and discharge effects caused by the averaging filter. The steady state values will be the same as above. For reference, Figures 40 through 44 are included at the end to show the raw input waveforms.

The circuits all generated the correct RMS value for the first set of signals. The rise times and shape of the rising curves varied from circuit to circuit. The outputs from the four detectors are shown in figures 24 through 31. A fixed DC current of 100μA was injected at the input to the detector along with the input signals. This DC value should be added to the expected value at the output. All output values are correct after the settling time of approximately 1.5 seconds for each of the detectors. The difference in the filtering sections is shown by differences in the rise and fall curves. As the order of the filter is increased, the rise and fall curves become better approximations to the desired square pulse.

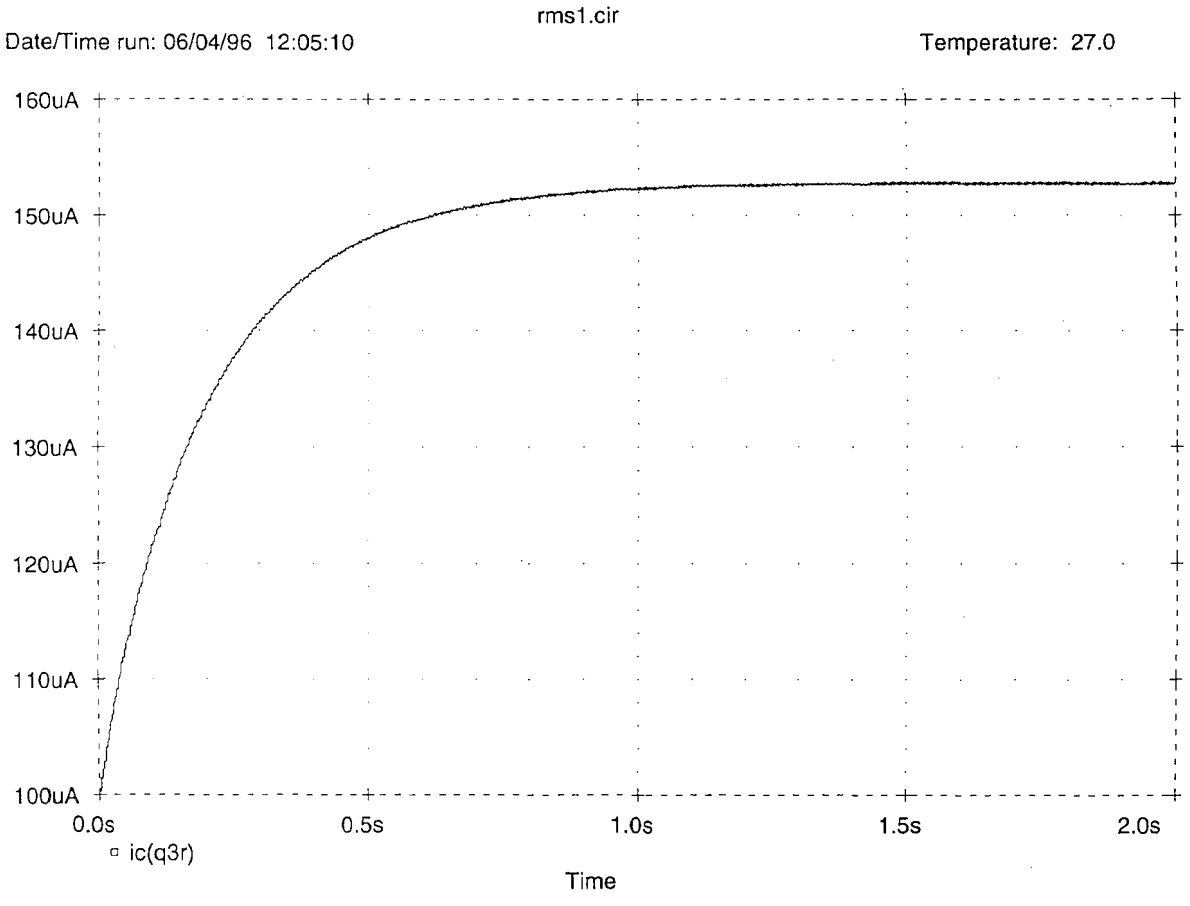


Figure 24. 1st Order RMS Response to Sine Input

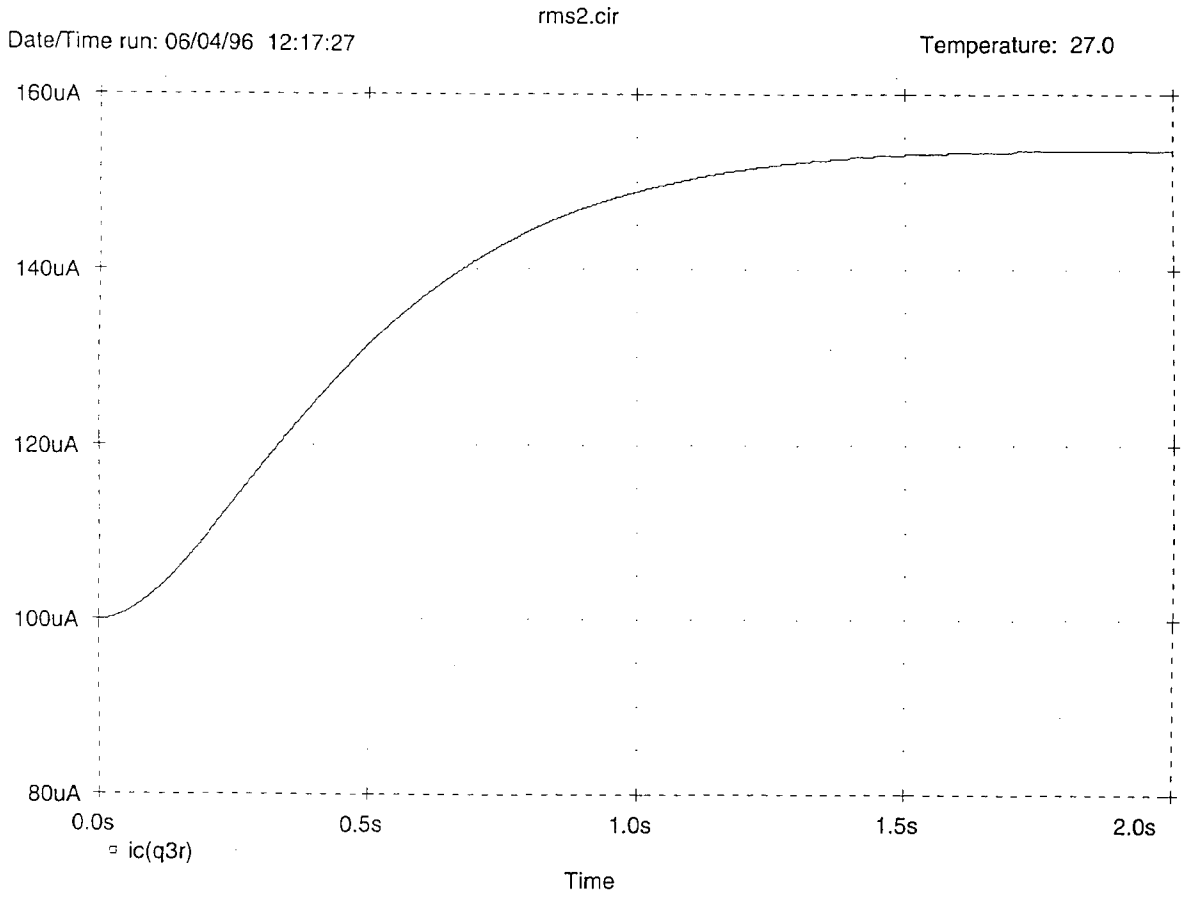


Figure 25. 2nd Order RMS Response to Sine Input

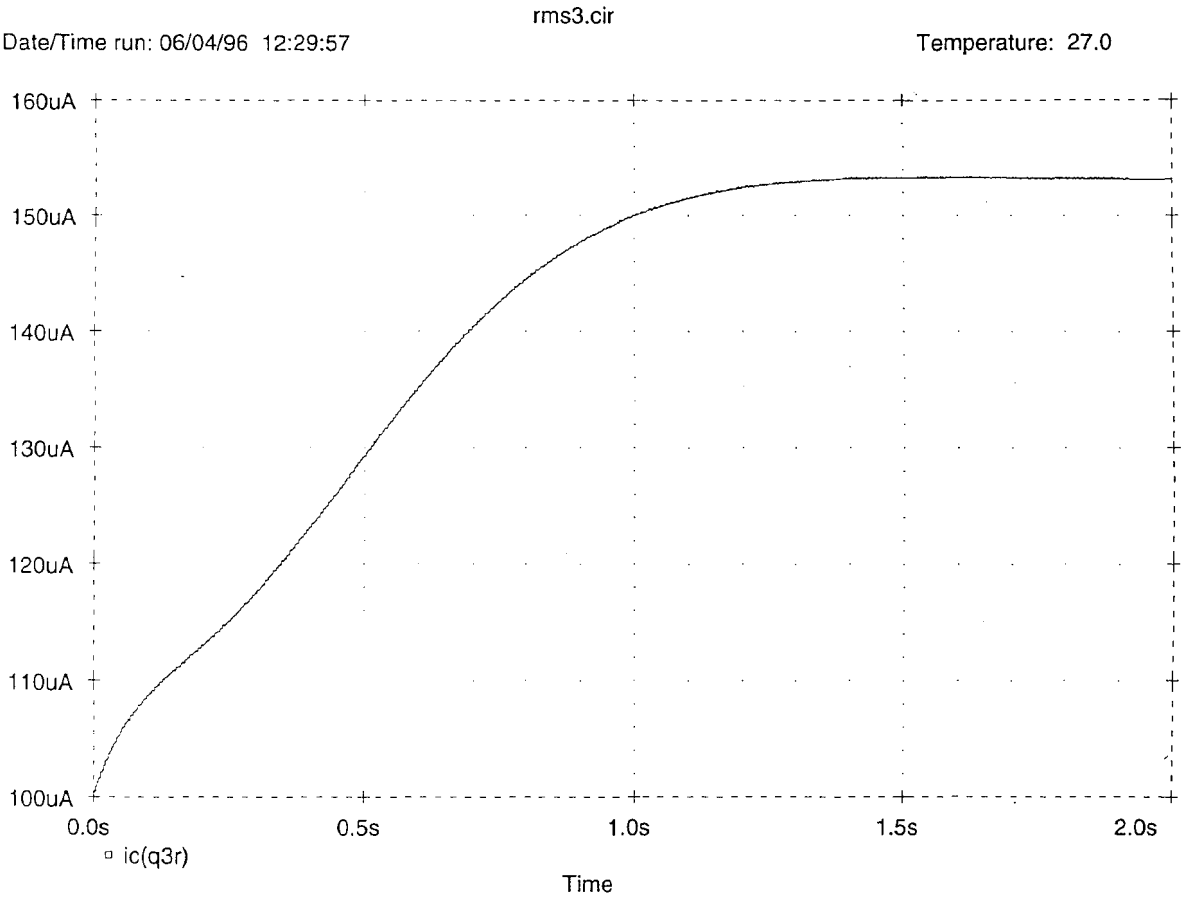


Figure 26. 3rd Order RMS Response to Sine Input

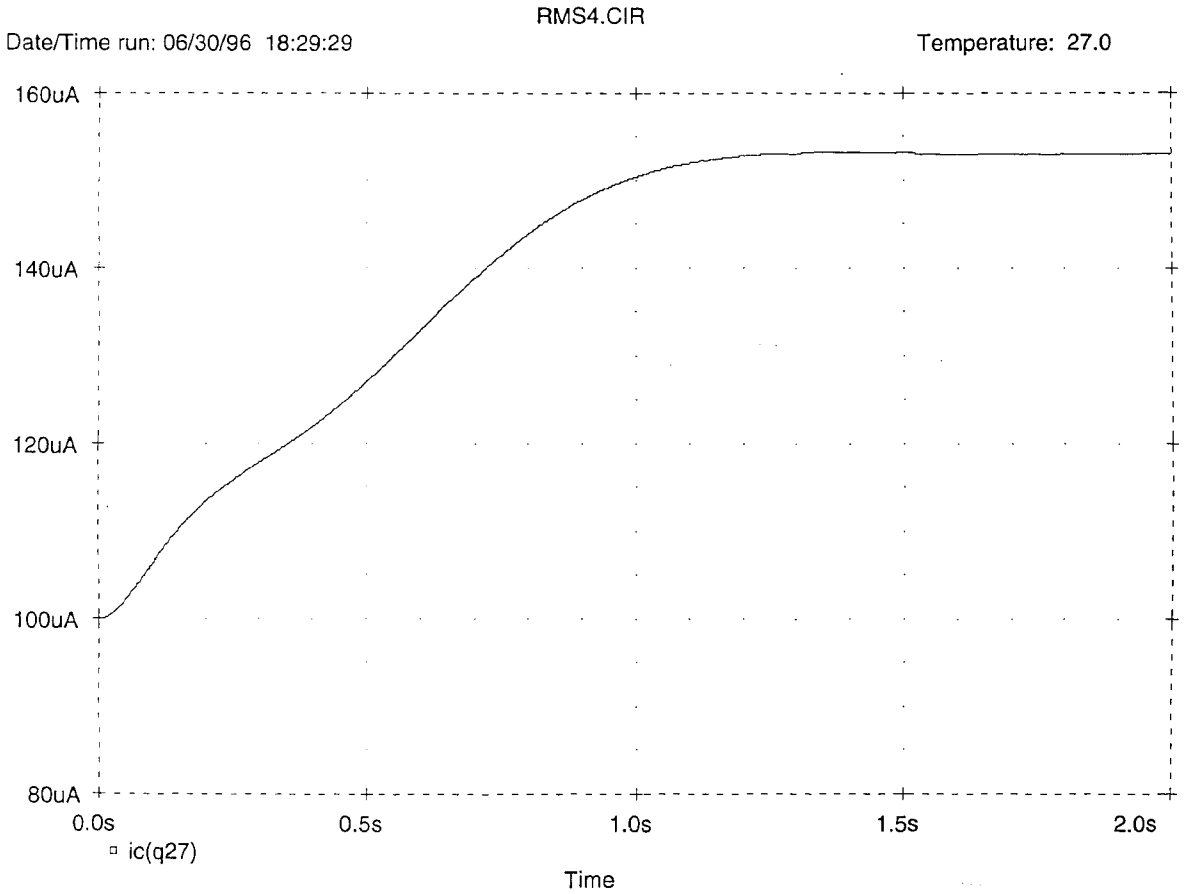


Figure 27. 4th Order RMS Response to Sine Input

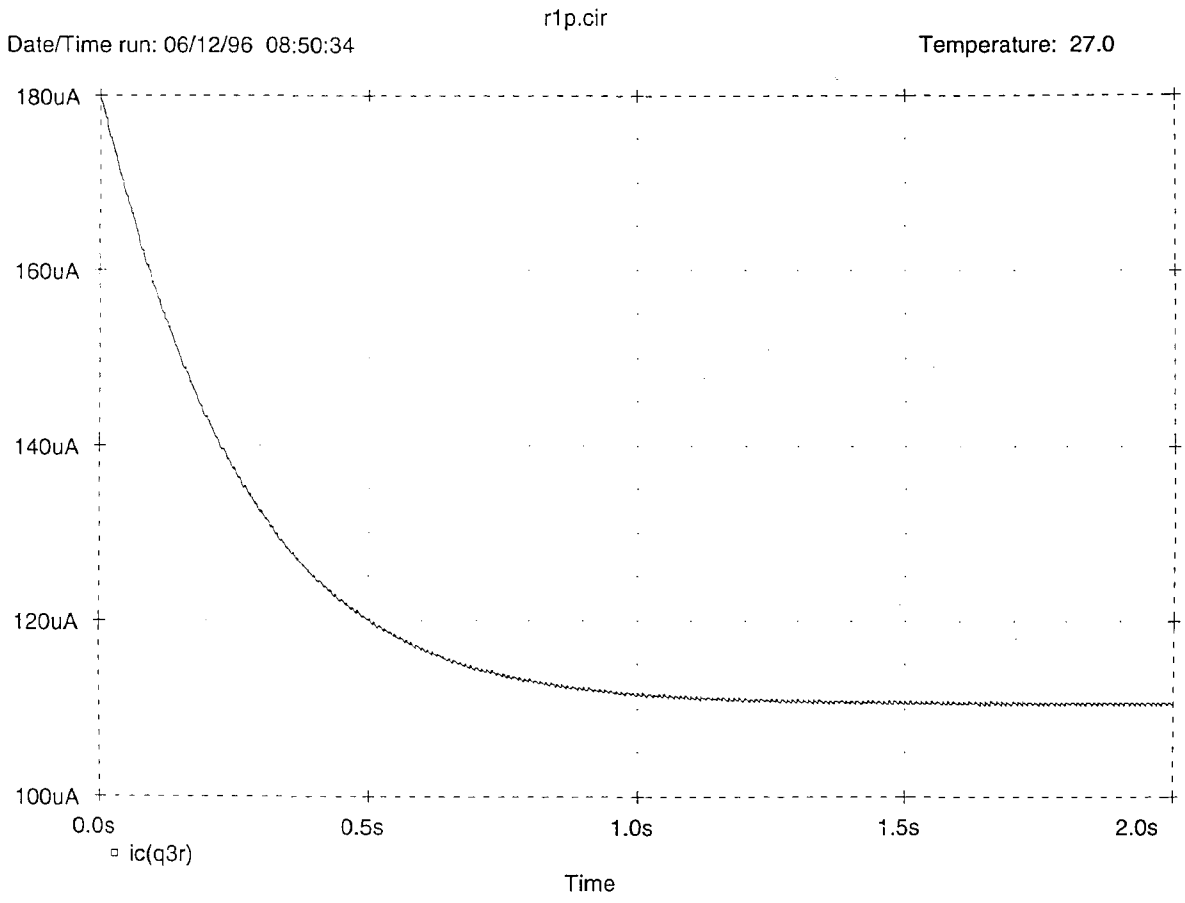


Figure 28. 1st Order RMS Response to 10% Duty Cycle Pulse

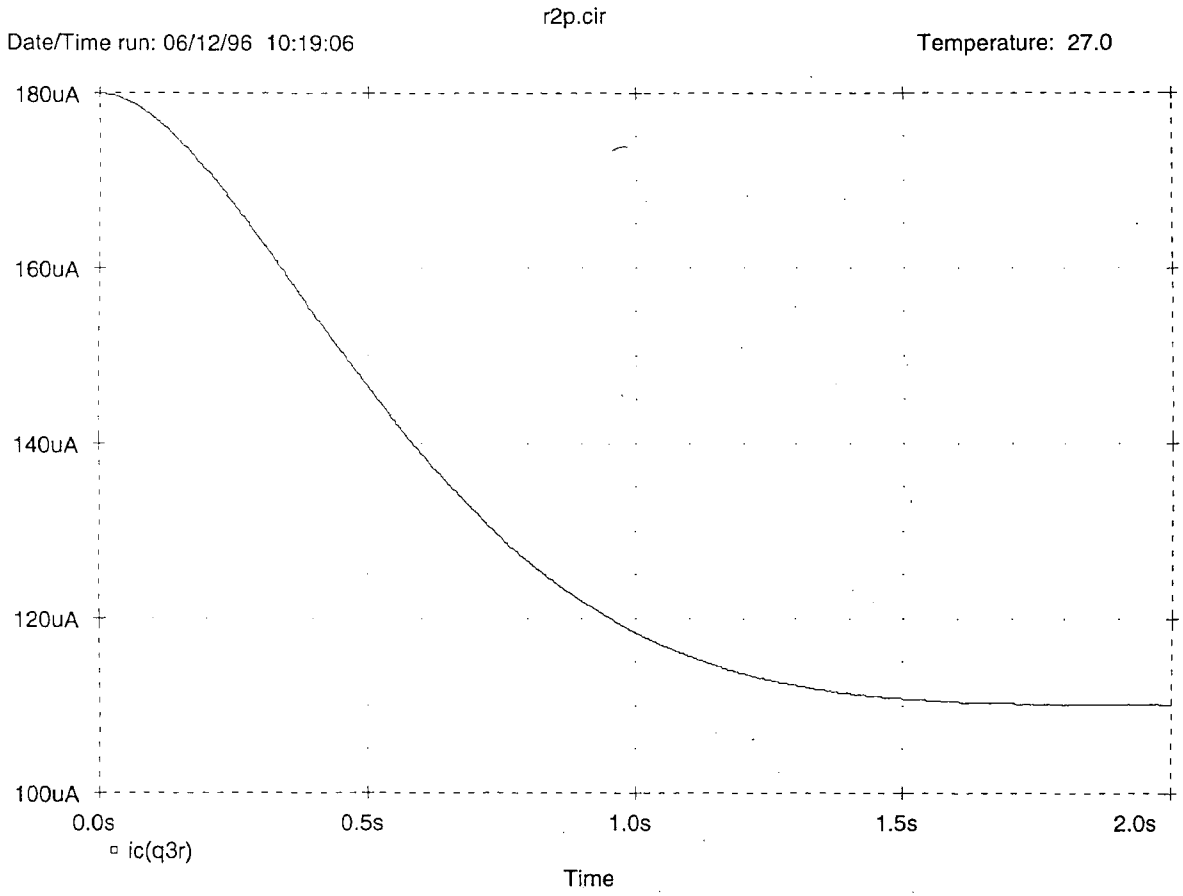


Figure 29. 2nd Order RMS Response to 10% Duty Cycle Pulse

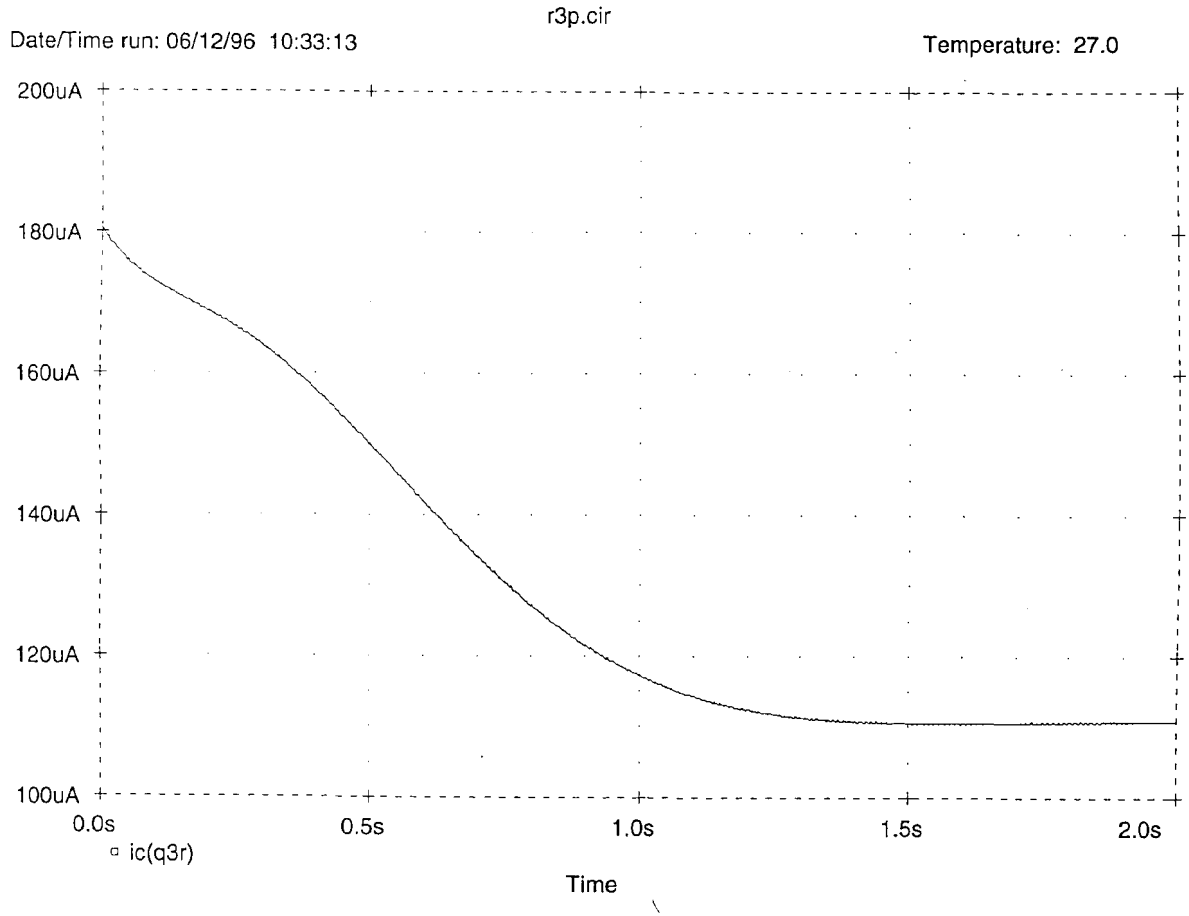


Figure 30. 3rd Order RMS Response to 10% Duty Cycle Pulse

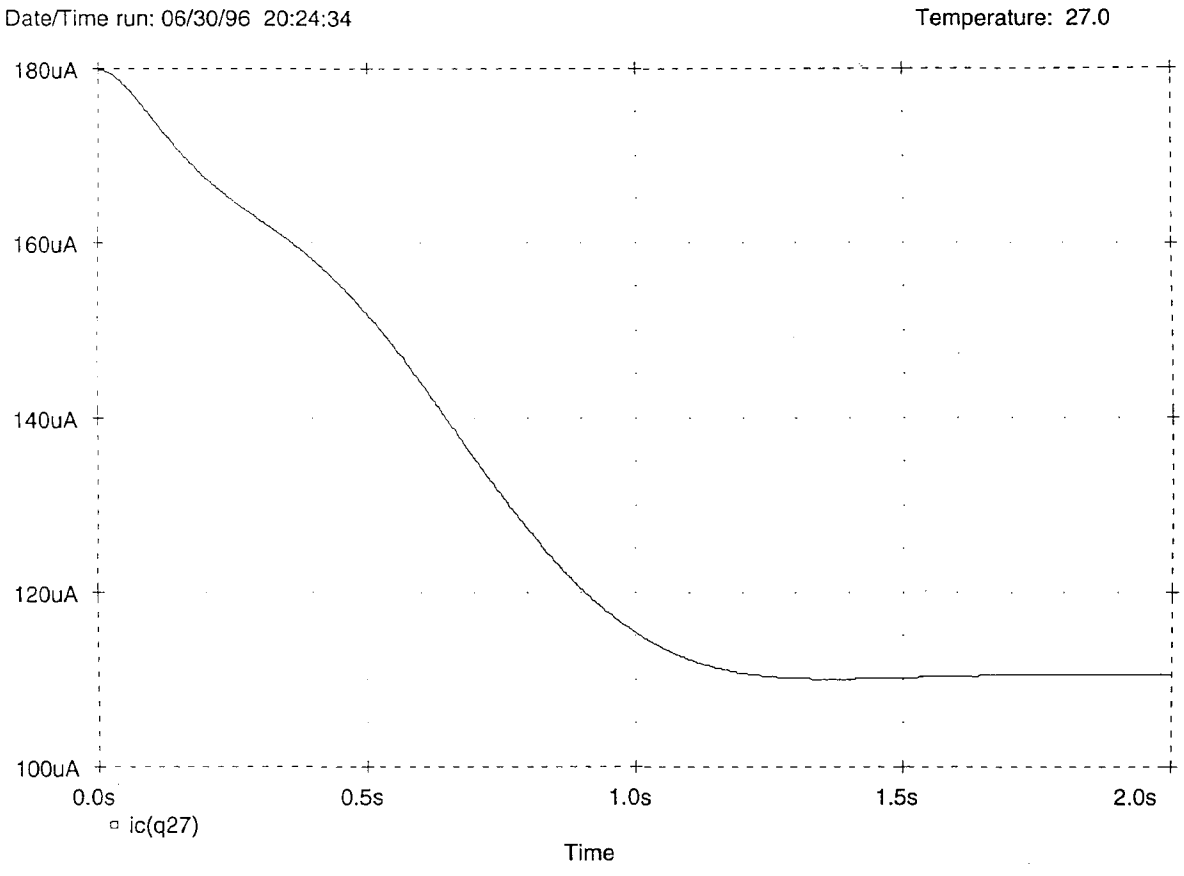


Figure 31. 4th Order RMS Response to 10% Duty Cycle Pulse

The results have shown that RMS detectors can be made using higher order filters. The advantages of using the higher order filters will now be shown with the burst waveforms described above. The objective in RMS detection is to find the RMS value for a given window of time. A better approximation to the "sliding window" has been attempted using higher order filters. Since the window is set at 1.5 seconds, and the signals are presented to the detectors for 2 second bursts, the ideal output will rise for 1.5 seconds and hold at the correct value (plus the DC offset). The RMS value of the burst will be held for .5 seconds, and will then begin to fall again. During the off time in the cycle, the output should settle to the constant DC value injected by 3.5 seconds, hold until 4 seconds, then begin to rise again. The simulations will be run until about 4.5 seconds to show just over one full cycle.

Figures 32 through 35 show the responses to the sine bursts. It is immediately obvious that the higher order filters generate an output that is closer to the ideal sliding window. There is improvement evident for every increase in the order. The fourth order looks the best and the first order looks the worst.

The response to the 10% duty cycle pulse bursts is shown in figures 36 through 39. The results are the same as those described for the sine bursts. The higher order filters again show a dramatic improvement.

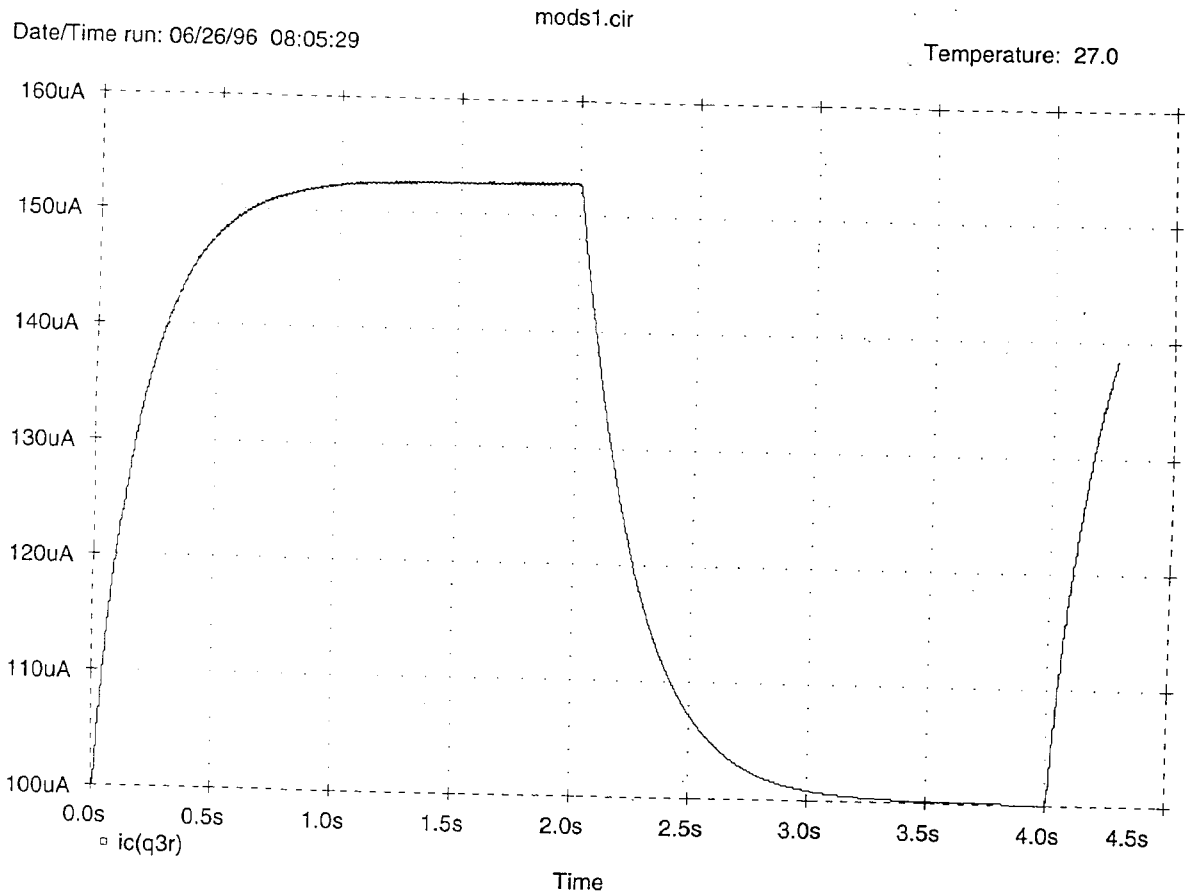


Figure 32. 1st Order RMS Response to Sine Burst

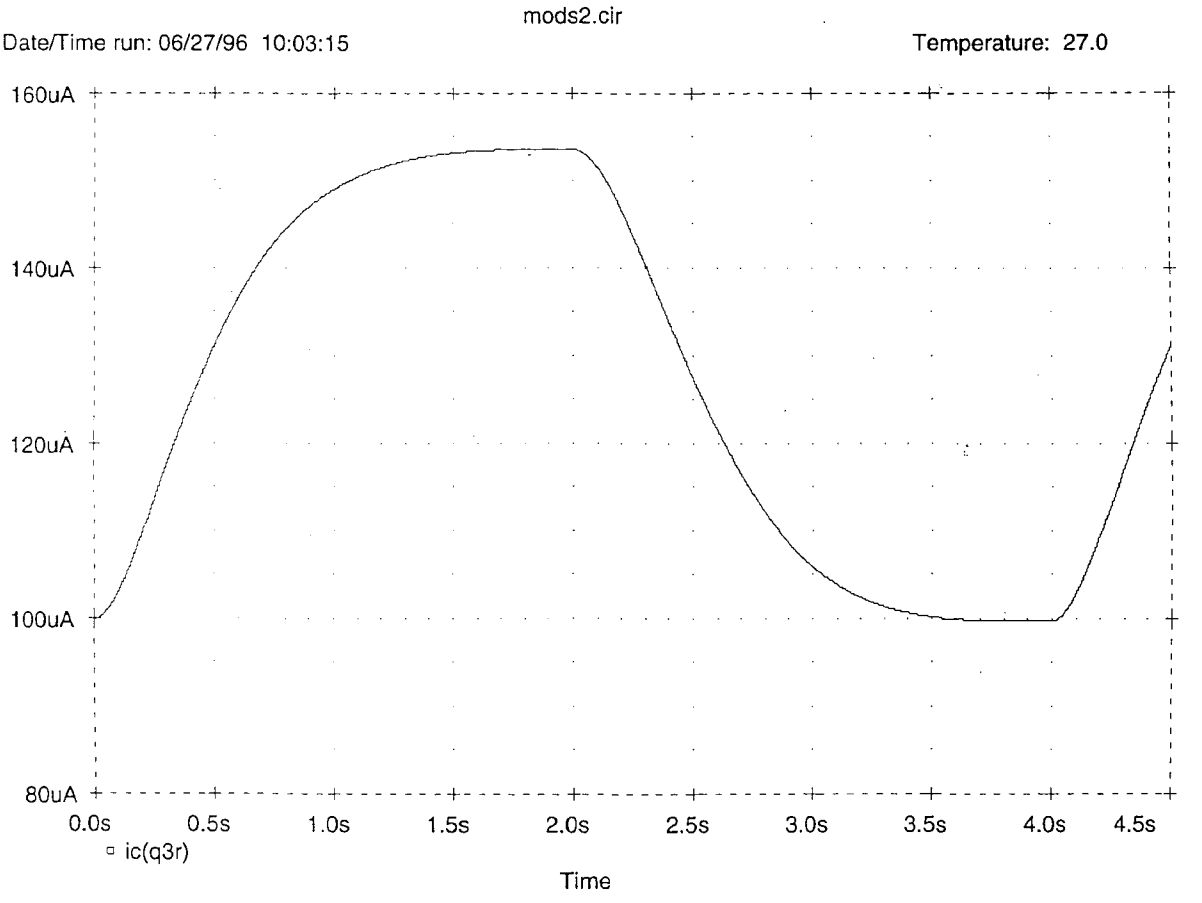


Figure 33. 2nd Order RMS Response to Sine Burst

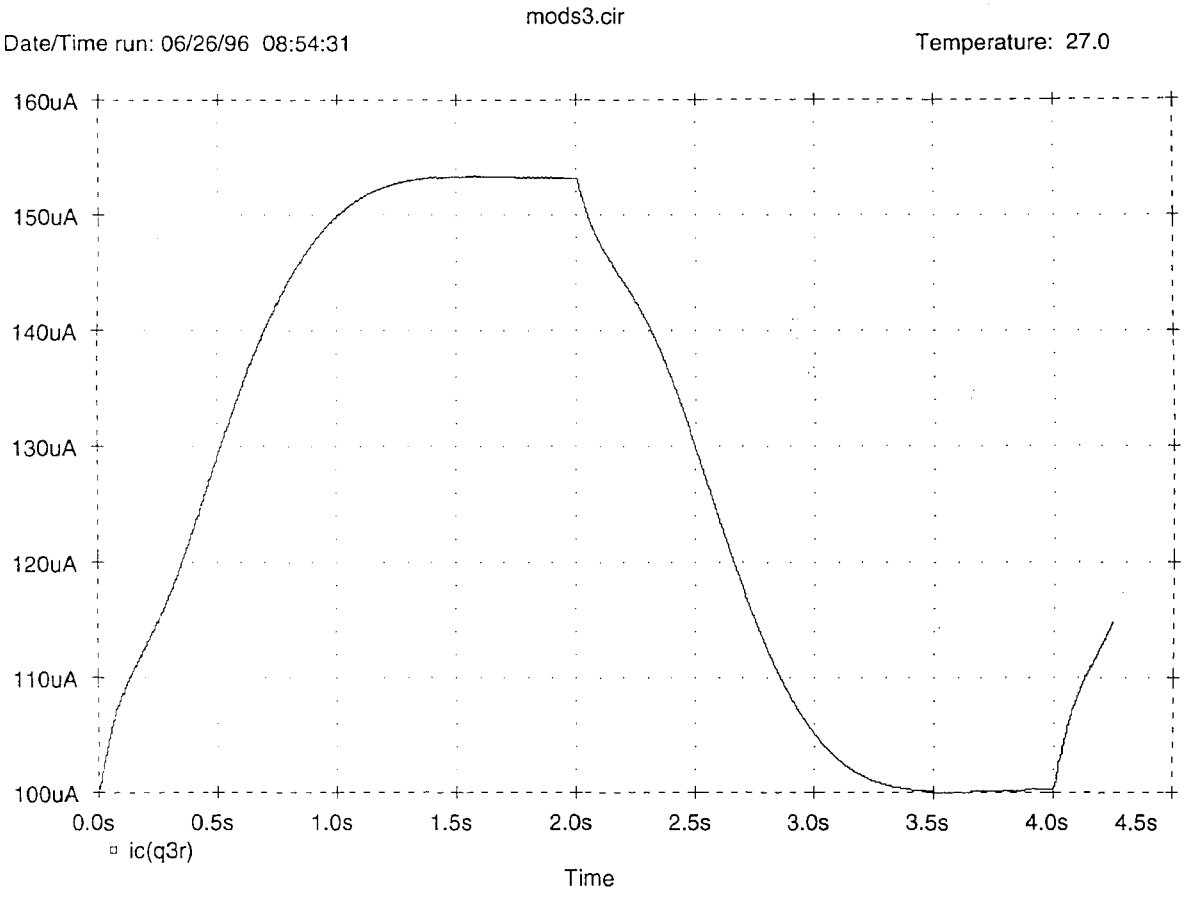


Figure 34. 3rd Order RMS Response to Sine Burst

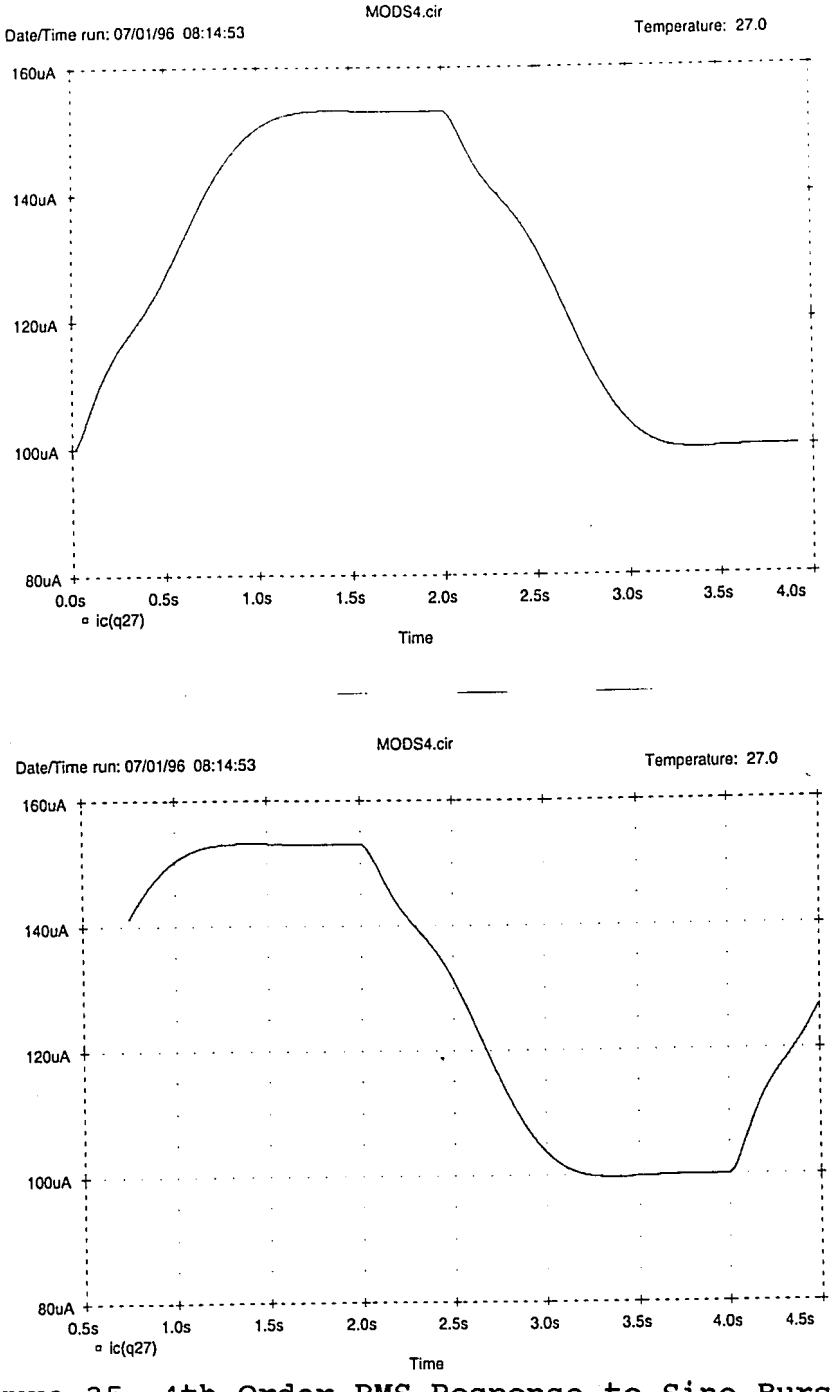


Figure 35. 4th Order RMS Response to Sine Burst

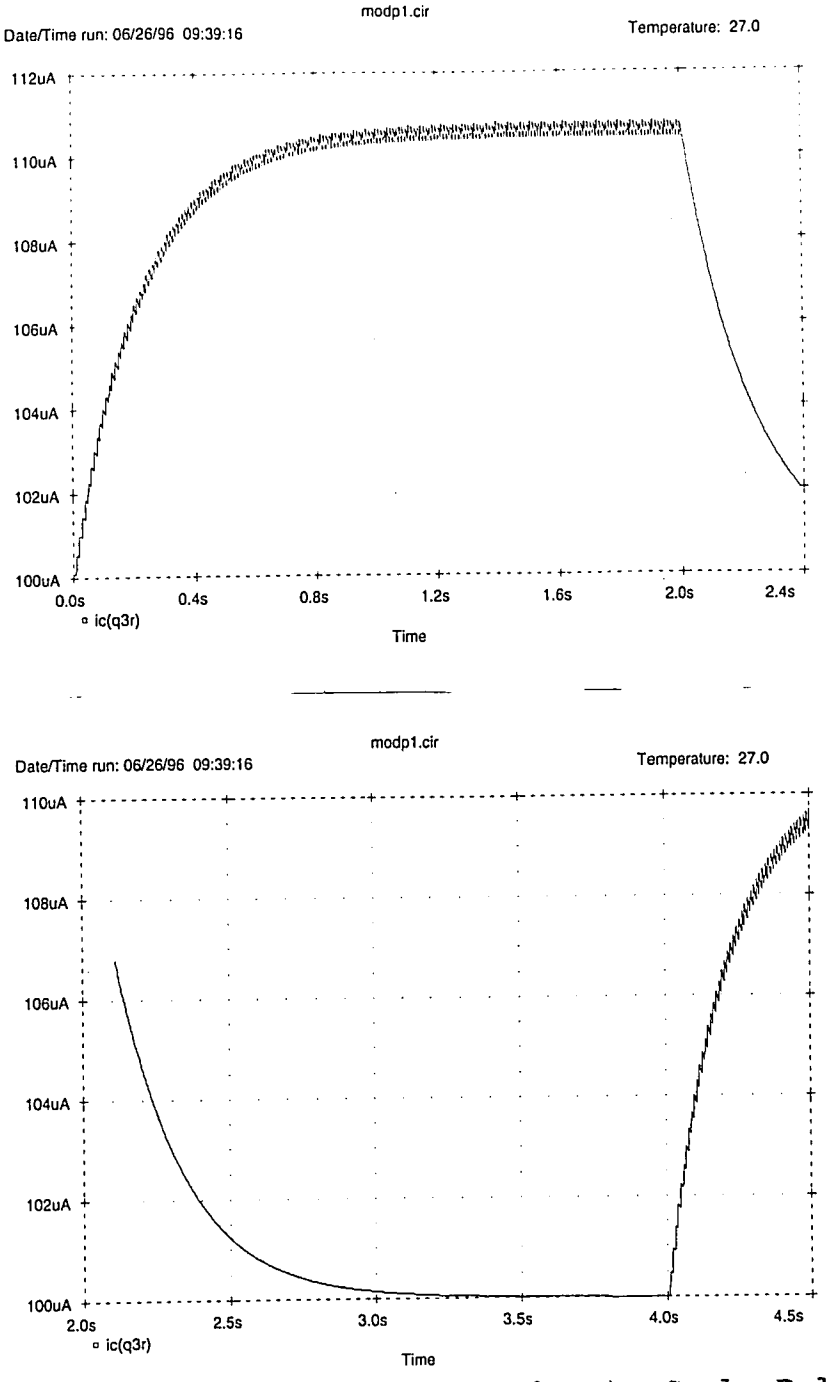


Figure 36. 1st Order RMS Response to 10% Duty Cycle Pulse Burst

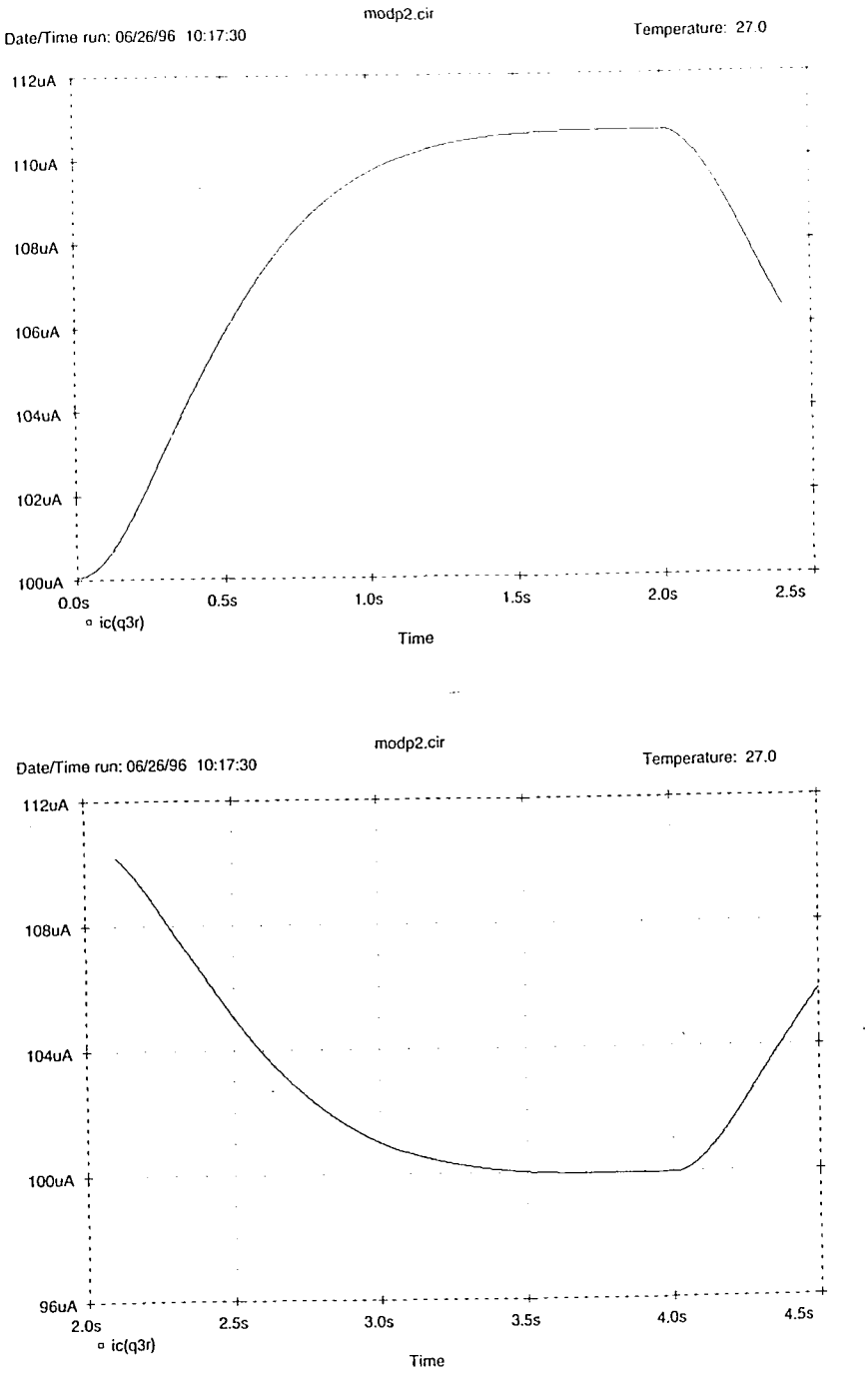


Figure 37. 2nd Order RMS Response to 10% Duty Cycle Pulse Burst

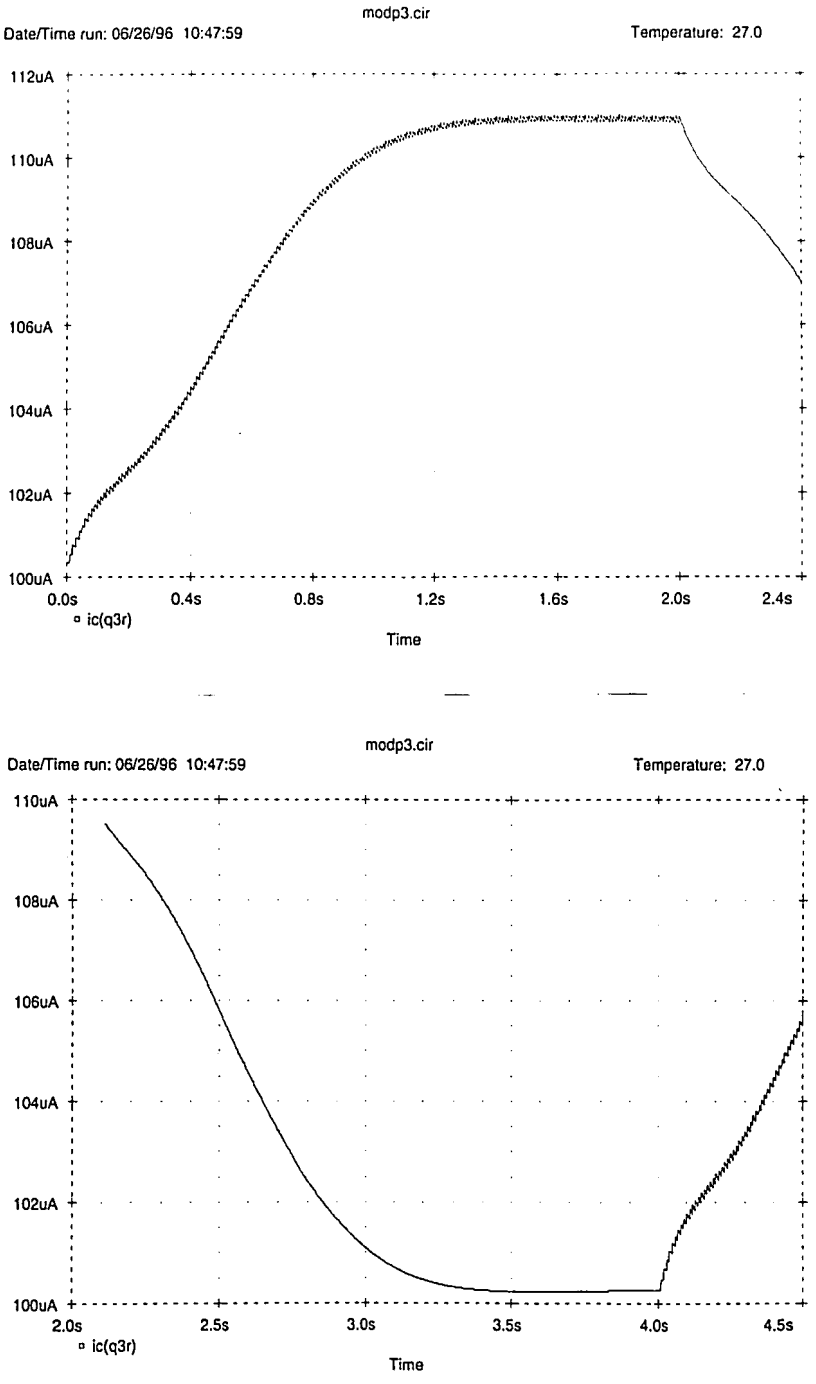


Figure 38. 3rd Order RMS Response to 10% Duty Cycle Pulse Burst

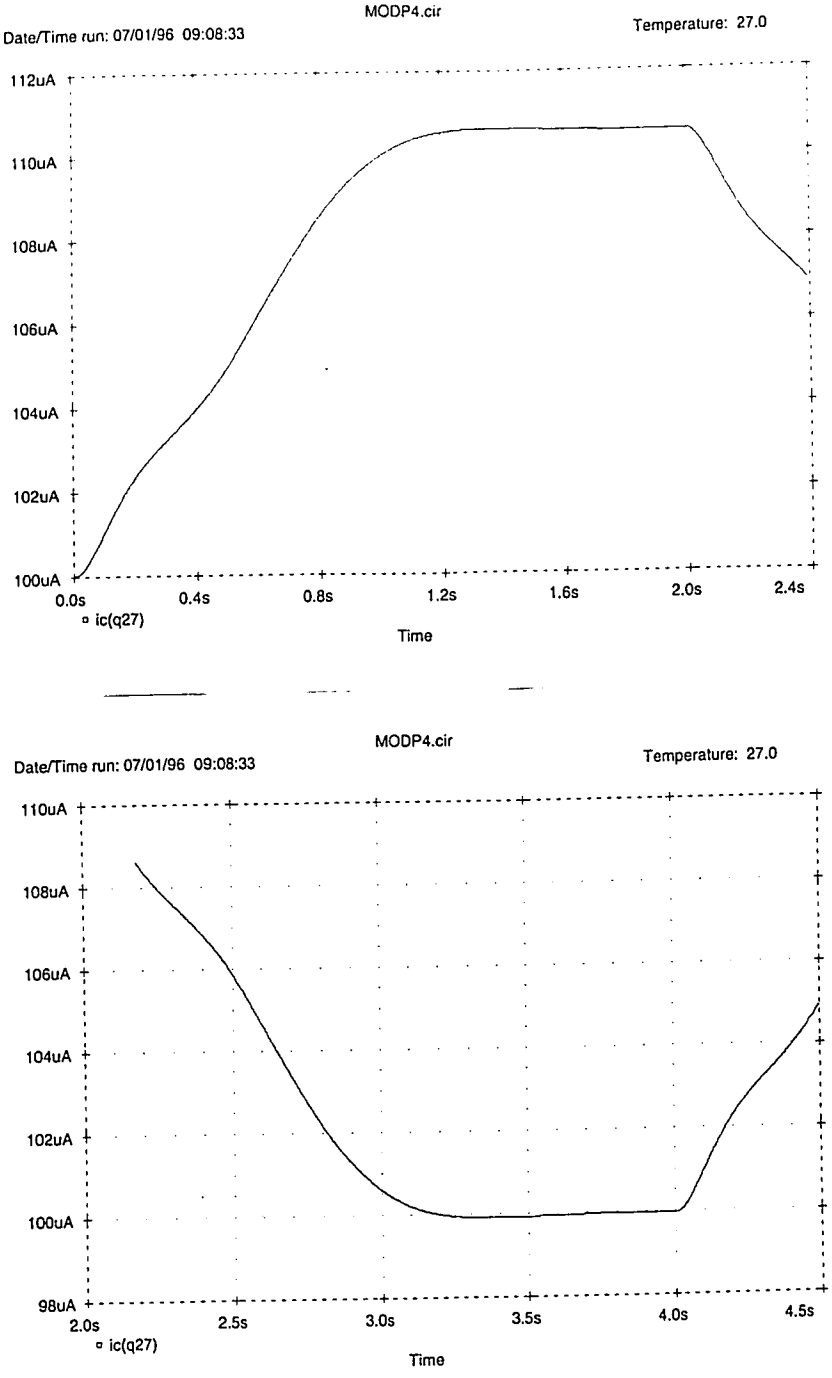


Figure 39. 4th Order RMS Response to 10% Duty Cycle Pulse Burst

The results have shown that the objective of using higher order filters to approximate a "sliding window" has been met. The higher order filters have done a better job of averaging over a fixed time period. This better averaging translates into a more accurate calculation of the RMS value of a signal over a specific time period.

Chapter 5.0: Conclusion

Throughout this work, many concepts and topics have been covered. The desire for RMS detection led to the idea of generating electronic circuits to automatically calculate the RMS value of an input waveform. Two methods of implementing the RMS calculation are the implicit and explicit method. Currently there are drawbacks to each method including bandwidth and dynamic range. It has been the goal of this work to develop a new style of explicit RMS detector. This new style detector has the ability to overcome some of the problems that current RMS detectors have. Specifically, the dynamic range issues are avoided by operating completely in the log domain. Up to this point, log domain operation was not possible because of the lack of log domain filtering techniques. Another advantage afforded by the log filters is the ability to use a higher order filter in the averaging section. The higher order generates a better approximation to the ideal sliding window.

Log domain filtering in general has been discussed as well as its application to implement a general transfer function. Not only does this explicit detector have the dynamic range of an implicit detector, but it also maintains the bandwidth of explicit detectors. This bandwidth is maintained because there is still no feedback required. The design synthesis procedure to go from transfer function to

circuitry has been covered. Second, third, and fourth order circuits were created and tested. The application of log filters to specific applications was explained.

The averaging section of the RMS detector can be improved with these higher order filters. It has been shown that the higher order terms generate a better approximation to the ideal square pulse that is desired for evaluating data.

The entire explicit, log domain RMS detector was developed and demonstrated. The input has been logged, doubled, filtered, halved, and exponentiated respectively. This chain of functions corresponds to squaring, averaging, and then square rooting, an explicit implementation of the RMS calculation.

It was shown that by increasing the order of the averaging circuit, the output was a better approximation to the ideal "sliding window". By calculating the RMS value only during this tighter time period, more accuracy can be achieved in the calculation for non-stationary signals. It is shown that improvement is made with the addition of each pole from first to fourth order. It is expected that this increase would continue for each pole added until a very close approximation to a square wave is reached.

The work done is in no way a comprehensive development of such an RMS detector. The goal was merely to show that such techniques could be applied to develop an

explicit detector. The application would require an improvement in the design of the log filters. Proper scaling of capacitors and currents would be required to make it realizable. Improvements could be made such as making the cutoff frequency tuneable. All circuits could have minor improvements to make them more robust under all conditions.

Even without these improvements, it has been shown that the concept is valid and functional. This work has successfully proposed and modeled a new type of explicit RMS detection.

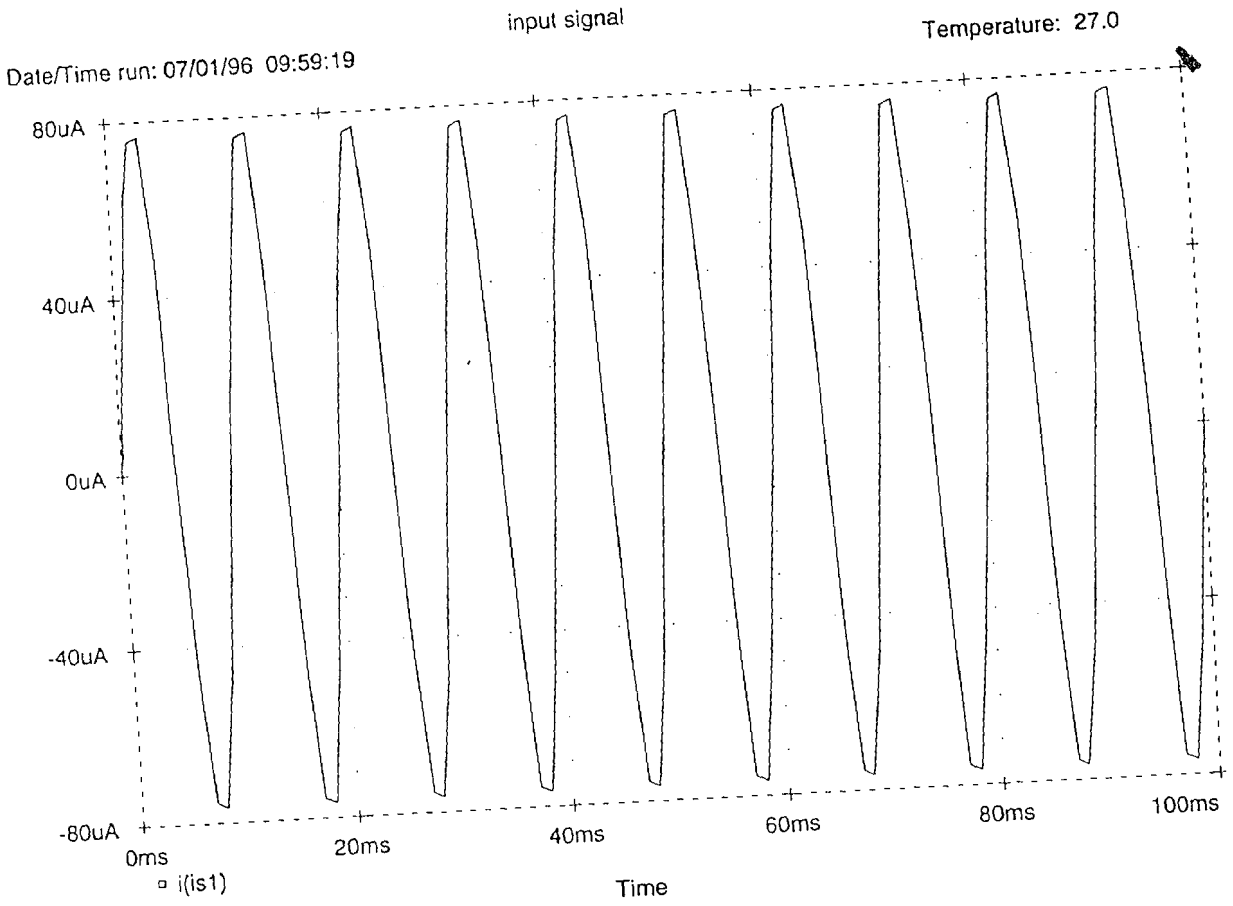


Figure 40. Sine Wave Input

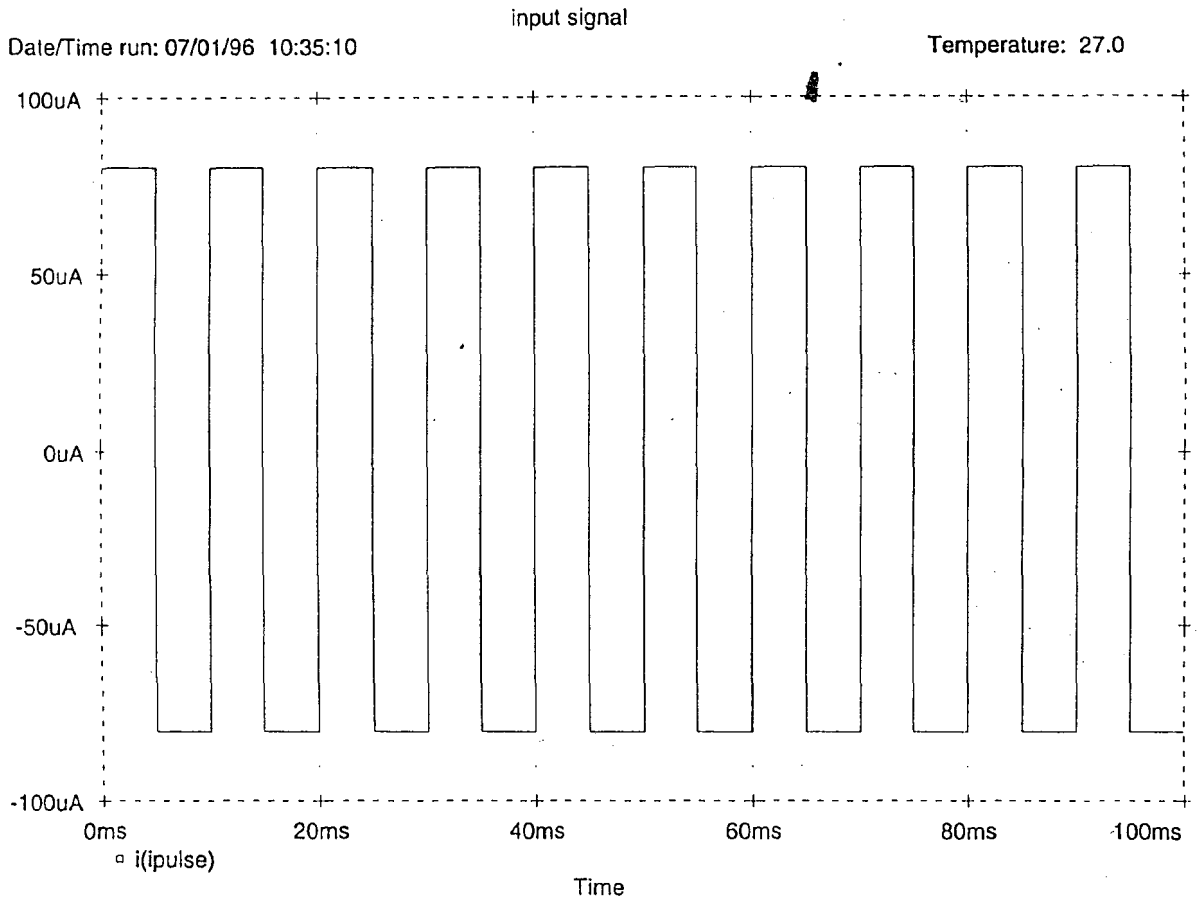


Figure 41. Square Wave Input

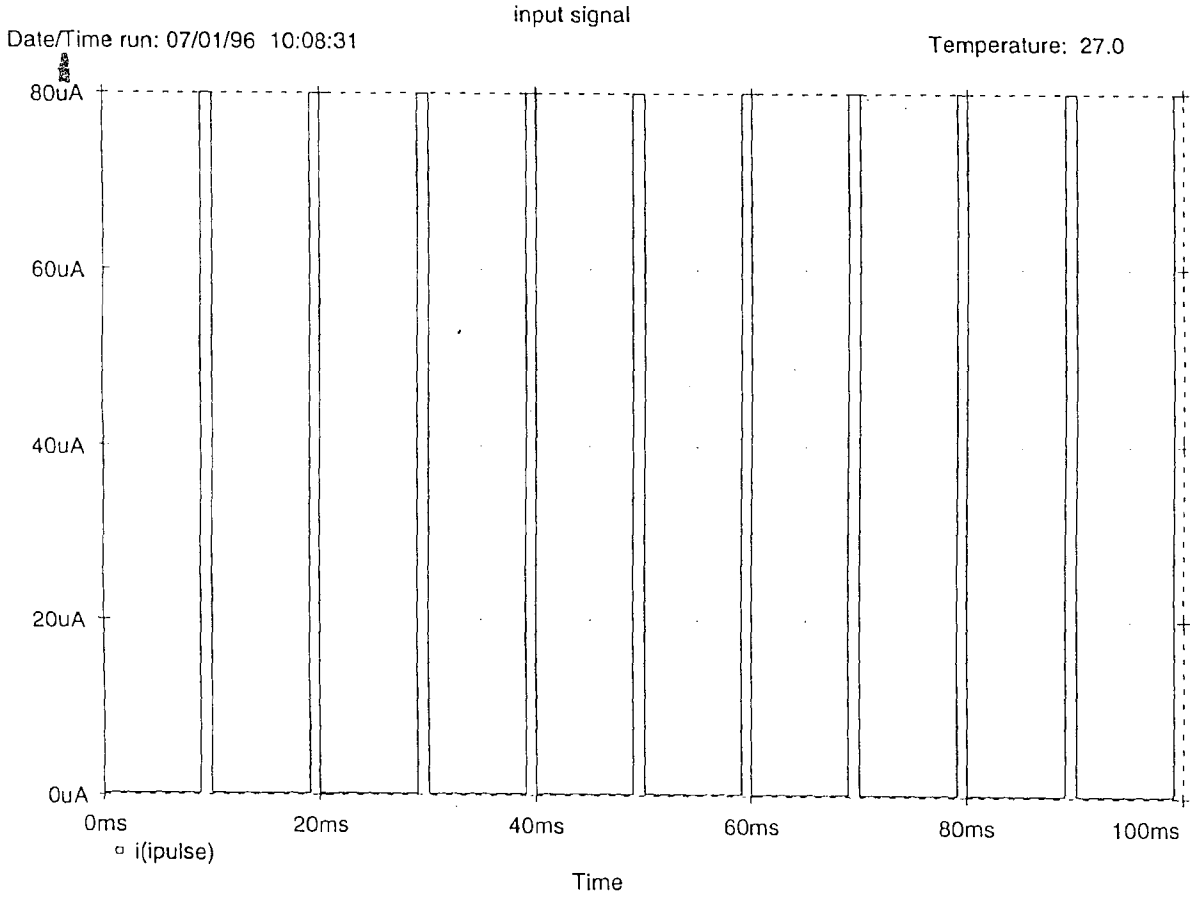


Figure 42. 10% Duty Cycle Pulse Input

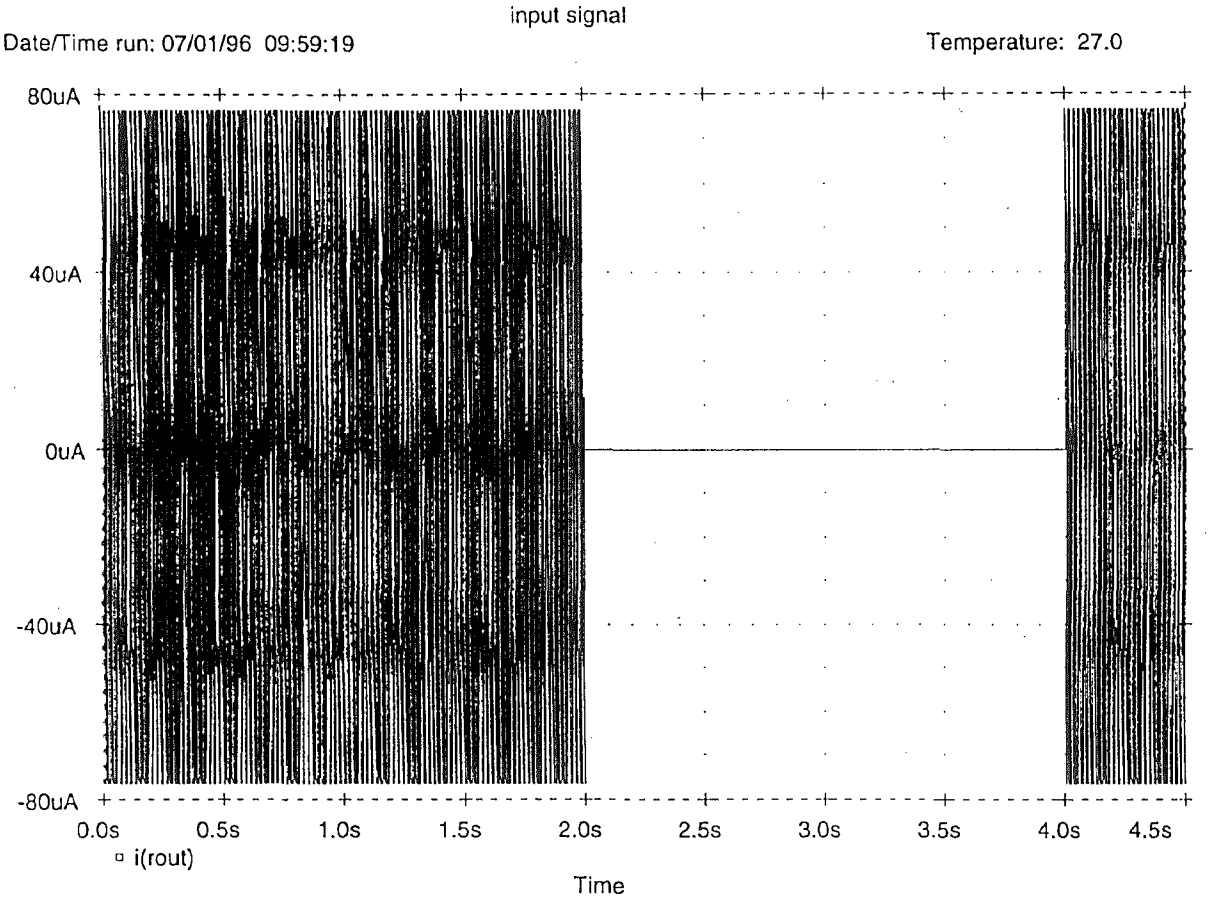
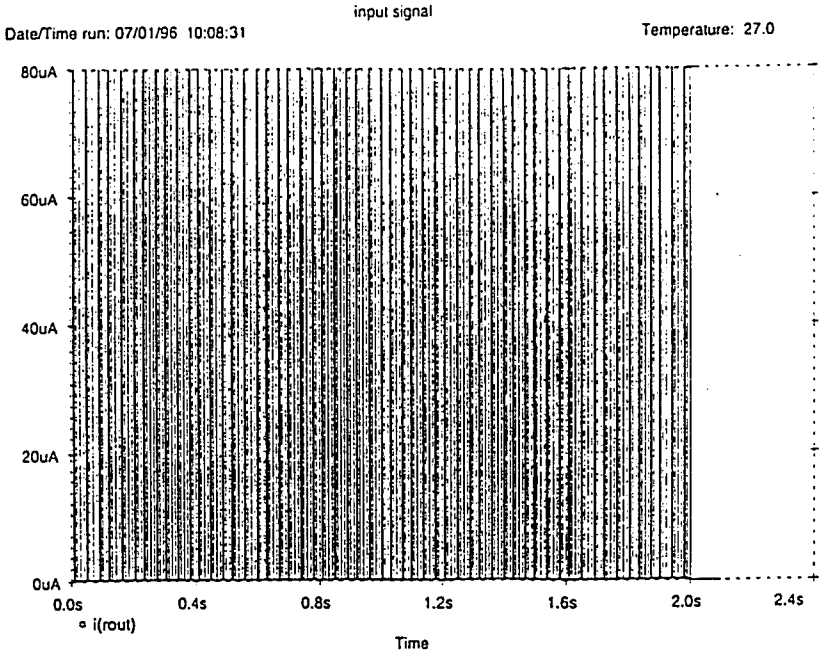


Figure 43. Sine Burst Input



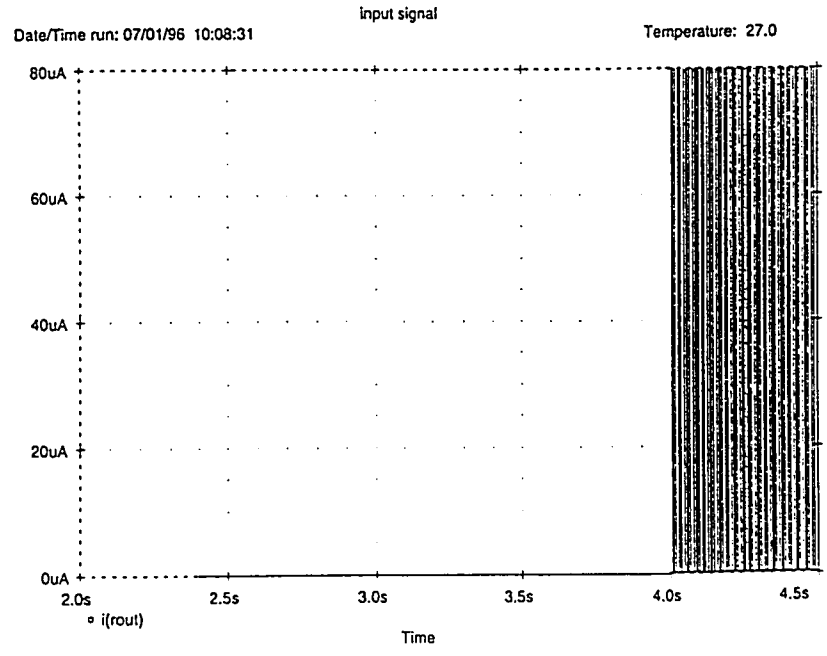


Figure 44. 10% Duty Cycle Burst Input

References

1. ADAMS, R.W.:'Filtering in the Log Domain'. Presented at the 63rd AES Conf., New York, May 1979, Preprint 1470

2. FREY, D.R.:'Log Domain Filtering: An Approach to Current Mode Filtering'. IEE Proceedings-G, Vol. 140, No. 6., 1993

Jack Romaine was born on April 24, 1971 in Williamsport, Pennsylvania to John and Ann Romaine. He graduated from Lehigh University with a BSEE in 1993. He received the Francis du Pont award for the top two ranking electrical engineering seniors and was a member of Tau Beta Pi and vice president of Eta Kappa Nu. After graduating, he went to work for Accu-Sort Systems in Telford , PA as a Research and Development Design Engineer. The job involved a broad spectrum of both analog and digital hardware design. Jack has attended Lehigh part time to complete this Master's Program. Specialization has been in signal processing with a mix of analog, digital, and image processing studies.

END OF TITLE