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# Manufacturing metrics for design : wafer-scale integration and multichip modules

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# MANUFACTURING METRICS FOR DESIGN:

# WAFER-SCALE INTEGRATION AND MULTICHIP MODULES

by

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A Thesis

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in

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## CERTIFICATE OF APPROVAL

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

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(Date)

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Director of M.S.E. Program

Chairman of E.E.C.S. Department

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# ABSTRACT

The notion of throwing a design "over the wall" to the production function has its roots in a modularized approach to manufacturing. This practice, where each department in an industrial organization optimizes its own operations with little regard for other departments, worked well in the past when the United States faced only minor competition in several industries. Today, however, in an era of global competition, integration has become a critical factor in the effort to remain competitive.

It is important to understand the manufacturing systems and engineering aspects that affect successful and economical implementation of microelectronics designs. This is particularly true in the design and selection of electronics packaging. The selections of materials, processes, and equipment for realization of a design have enormous impact on the costs, economical volumes, potential production rates and reliabilities. The impact of design choices upon the viability and manufacturing feasibility for the realization of mid-range electronic performance and functionality has been studied by comparing a multichip module design with an equivalent wafer-scale integration.

# INTRODUCTION

A great debate is currently ensuing over United States manufacturing competitiveness. Myriad issues have arisen regarding methods of improving America's industrial base: Flexible manufacturing, global marketing, improved quality control, concurrent engineering. Indeed, the present economic recession faced in the United States and in other Western nations has been described as the first manifestation of a long-term problem [1]. Ample evidence can be cited of long-term downturn in US manufacturing. One is the steadily increasing trade deficit as shown in Figure 1 [2].

Trade Balance in Manufacturing, Billions of U.S. Dollars

| Year | United States | Japan | West Germany |
|---|---|---|---|
| 1970 | 3.4 | 12.5 | 13.3 |
| 1971 | 0.0 | 17.1 | 15.0 |
| 1972 | −4.0 | 20.3 | 17.7 |
| 1973 | −0.3 | 23.3 | 28.7 |
| 1974 | 8.3 | 38.0 | 42.4 |
| 1975 | 19.9 | 41.7 | 38.7 |
| 1976 | 12.5 | 51.2 | 42.1 |
| 1977 | 3.6 | 63.0 | 46.9 |
| 1978 | −5.8 | 74.2 | 53.5 |
| 1979 | 4.5 | 72.0 | 59.2 |
| 1980 | 18.8 | 93.7 | 63.1 |
| 1981 | 11.8 | 115.6 | 61.7 |
| 1982 | −4.3 | 104.0 | 67.5 |
| 1983 | −31.0 | 110.3 | 58.7 |
| 1984 | −87.4 | 127.9 | 60.5 |
| 1985 | −107.5 | 107.7 | 59.5 |

**Figure 1**

The importance of U.S. competitiveness in microelectronics cannot be overestimated; a nation seeking to maintain supremacy in high technology cannot neglect integrated circuits (ICs), the foundation of that technology. One of the primary reasons for the current crisis in microelectronics is that the "over the wall" approach to manufacturing still exists in this industry. By this it is meant that little if any communication occurs between the manufacturing and design functions during IC product development. Though this system has been used for years, it has proven to be inefficient in terms of product development cycle time and design integrity when compared to the newer concept of concurrent engineering. Short product development cycle times are crucial in this extremely competitive industry where time to market can make the difference between profitability or huge losses.

It is believed that with manufacturing metrics knowledge designers and engineering managers can make informed choices among alternative packaging technologies for their designs before manufacturing takes place. With this data enhancements can be made to the designs to facilitate manufacturing.

The two packaging technologies modelled are wafer-scale integration (WSI) and multichip modules (MCM's). They were chosen because both have been considered for the high performance designs of tomorrow. Through analysis of the manufacturing metrics, conclusions are suggested as to the future prospects of these two technologies.

The criteria modelled have been chosen based on their importance. The approach taken toward modelling has been to start with a mathematical attempt and to resort to qualitative discussion if mathematics does not do justice to the criteria. In all, three qualitative discussions are made and two mathematical models are constructed. The mathematical models have been implemented using a spreadsheet program, Quattro Pro version 3.01. The spreadsheet format was chosen for this program because choosing between alternative packaging options involves varying many parameters based on selection criteria. This function can be readily performed on a spreadsheet. Thus, in addition to the two technologies studied in this analysis, other packaging technologies can be modelled and compared in future studies by including appropriate data in the program.

# APPLICABLE DESIGNS

Before manufacturing metrics for electronic packaging can be described, it is first necessary to discuss the silicon circuitry within the packages. This information will give the program user the range of design sizes which can be examined.

One of the major benefits of MCM and WSI technologies is that they are particularly well suited for large-area silicon circuitry. Large quantities of silicon are packaged within one module when compared to plastic dual-in-line packages or metal encapsulants. Because of this quality, packaging large sub-systems or entire systems in a module is conceivable. For example, IBM's Thermal Conduction Modules contain large percentages of CPU circuitry in IBM 308X series minicomputers and more recent models [3]. In addition, researchers at Hughes Research Labs have implemented an entire computer in a full-wafer package [4].

The range of systems that can be implemented on silicon is astounding. The preceding examples came from the computer industry. Other applications which have been suggested [5]:

1. Automotive Industry: higher reliability engine control units running at increased clock speeds;

2. Telecommunications Industry: main switches and transmission multiplexers;

3. Consumer Electronics: Video Cassette Recorders and Camcorders [6].

The design inputs in the spreadsheet for all systems analyzed are the following:

1. Number of Gates (4 transistors/gate);

2. Number of Memory Cells (1bit/cell);

3. Number of Primary I/O;

4. Clock Speed.

With these inputs, it is not necessary to know the specific details of a design. Many different systems can be modelled with the general characteristics above common to all of them. The design (primary) input menu of the program, as well as secondary input and primary output menus, are contained in the appendix. CMOS technology is the silicon processing technology chosen because all commercially successful WSI efforts and some MCM efforts have employed this technology.

What are typical values of the inputs? To determine this the nature of such systems must be understood. Figure 2 shows a schematic of a typical system. The system contains a microprocessor, random access memory, read-only memory, and various peripheral components for I/O and interrupt control:

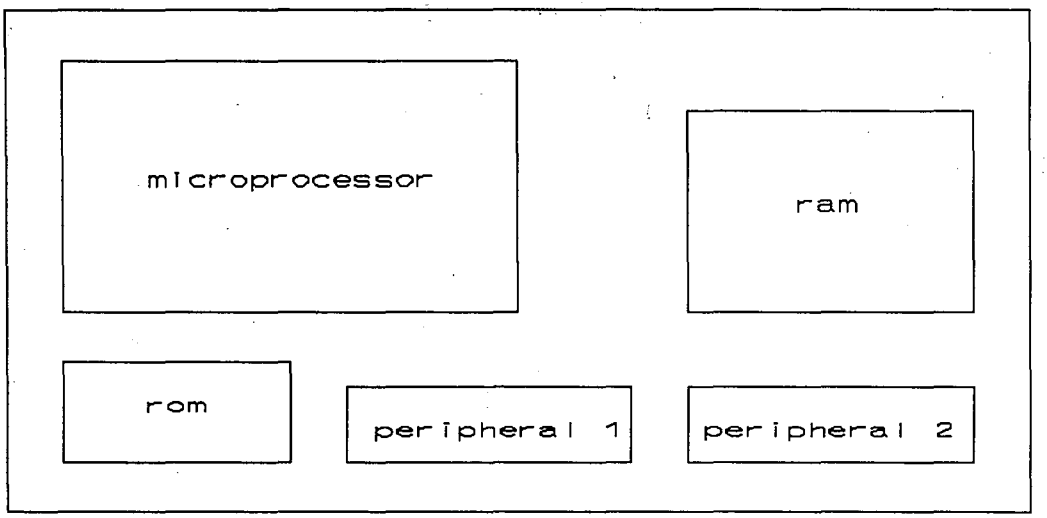


**Figure 2**

The following typical input ranges were considered:

1. Number of Gates: 25K-75K;

2. Number of Memory Cells: 512Kb-1.5Mb;

3. Number of Primary I/O: 50-100;

4. Clock Speed: 25-75 MHz;

These values were determined based on discussions with experts in the field (see acknowledgements) and acquired field data on integrated circuits. For example, the determination of the gate count range was based on microprocessor gate count knowledge. Intel's 80286 microprocessor contains approximately 275,000 transistors, which translates into 68,750 gates where each

gate has four transistors. It was determined that a processor of nearly equivalent power as the 80286 would be used in the typical design under investigation. Thus it became necessary to choose a logic gate budget close to the 80286 budget. Typical values of the inputs for further analysis of the two packaging technologies were chosen to be the range means. With these values silicon real estate computations can be made for WSI and MCM packages.

# MULTICHIP MODULES

Before discussing silicon area for MCM's, it is important to introduce this packaging technology as it pertains to manufacturing. MCM's are sealed modules with ceramic substrates for chip-to-chip interconnections. It offers the highest circuit density in packaging next to WSI. The chips can be mounted flush with the substrate or upside-down using flip-chip technology. The ceramic substrate can have many layers of conductive wiring in order to realize the level of interconnect necessary.

A large degree of variation exists regarding the types of MCM's manufactured today. Low-end applications include single-layer ceramic hybrids used in very high- volume consumer electronics applications such as camcorders and video cassette recorders. High-end applications include the liquid-cooled, large-area substrate, high-performance modules manufactured today by NEC, Fujitsu and IBM for mainframe applications.

VLSI techniques are used to fabricate the circuitry. From values of memory cell area and gate area a worst case total area estimate can be obtained for the typical design specified above.

A 1.2um design rule was chosen because it is a well established, mature technology that would display high yield within a short period of time. From the sources it was determined that 6-transistor static rams, 1-transistor read-only memories (gate array structure) and 1-transistor drams would serve adequately

for this model[7]. The following percentages were chosen for the memory types. Percentages can be changed to reflect variation in memory cell requirements:

25% ROM 50% SRAM 25% DRAM

For each of these memories, worst-case cell areas were computed. The ROM area estimation was calculated based on Figure 3 [7]. The figure shows three symbolic layouts of ROM cells. Symbolic layouts are designed to give area features without optimizing area usage. For this reason the area calculation is considered worst case.

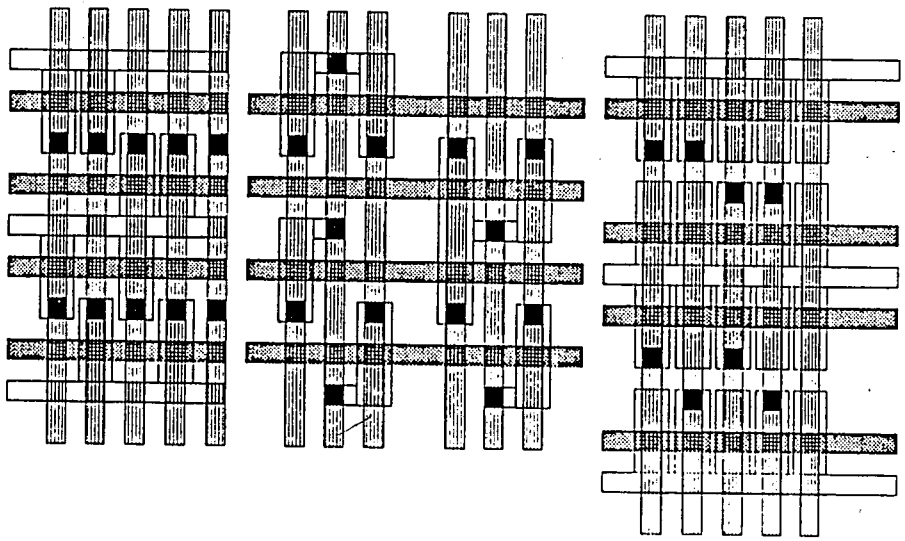

Figure 3

Figure 4 [7] shows the mask layout used to estimate SRAM cell area. The design rule was used to determine the gate length, and from this a typical SRAM area estimation was achieved.

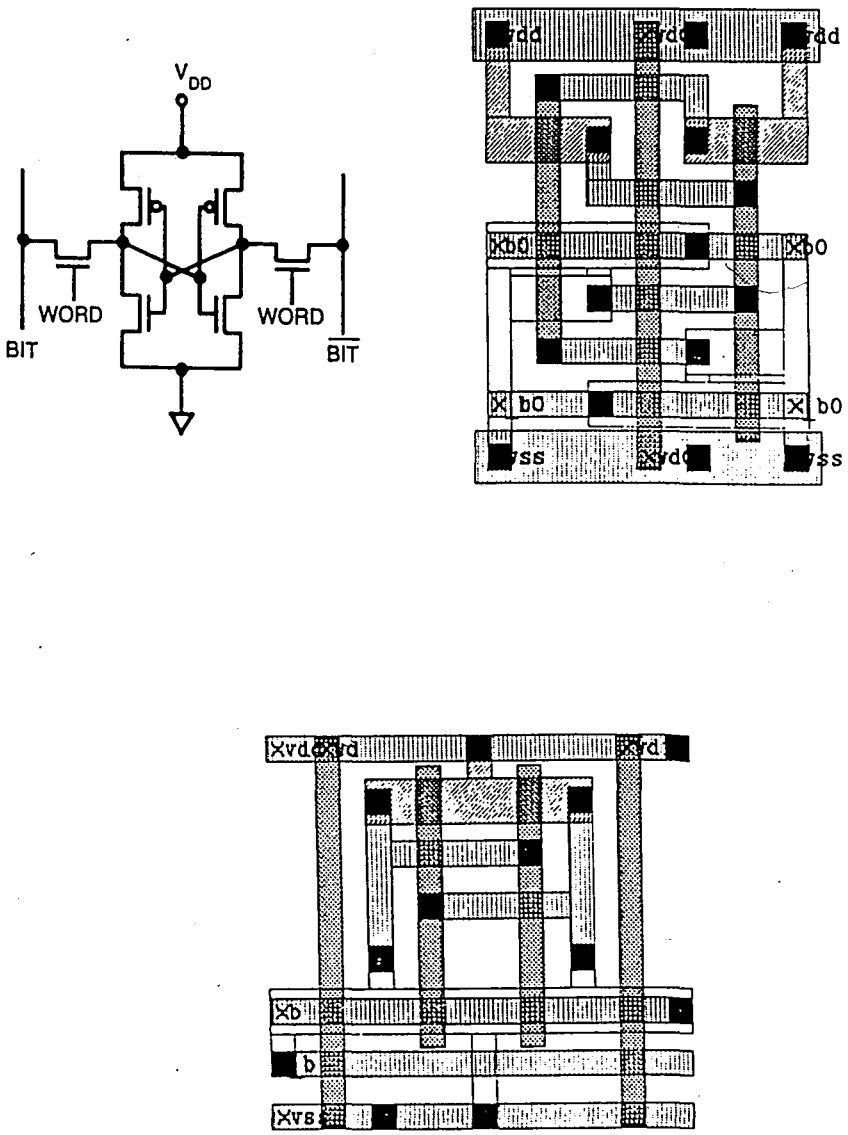


Figure 4

DRAM cell size estimation was accomplished using Figure 5 [8]. The design rule was used to compute the exact value of 43 square microns from the normalized units on the Y-axis.

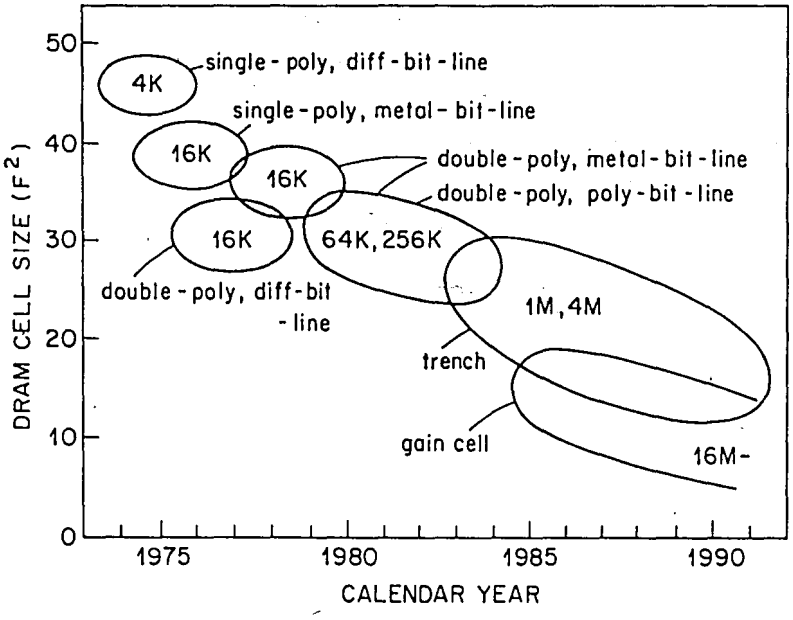


**Figure 5**

From Figures 3-5 above the following cell areas were computed:

ROM: 15 $um^2$ DRAM: 43 $um^2$ SRAM: 273 $um^2$

Thus the weighted average per memory cell is 151 $um^2$.

Figure 6 shows the mask layout used to estimate the area/logic gate. This area was computed to be 206um$^2$, where each gate contains 4 transistors.

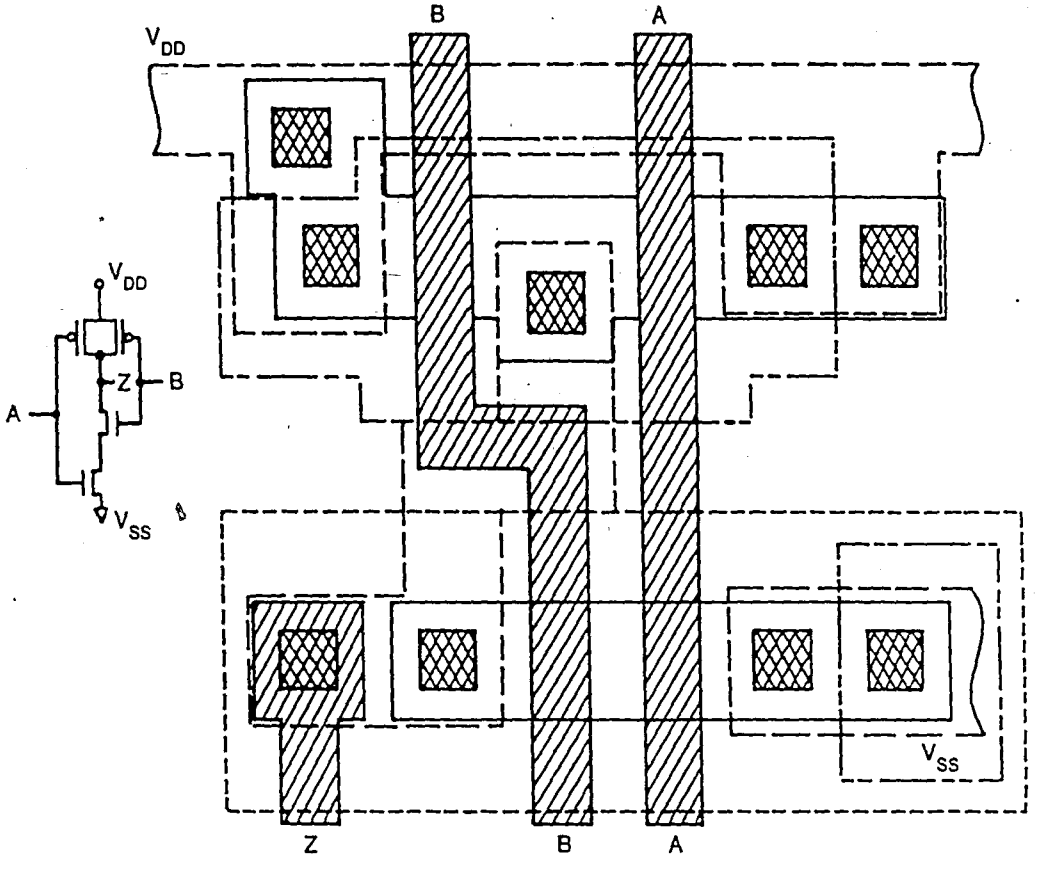


**Figure 6**

Finally, total area for the design (assuming 50% of real estate consumed with wiring) is computed as follows:

$$Area_{mcm} = [50,000*206+1,048,576*151]*2 = 3.37*10^8 um^2 \quad (1)$$

To cover this much silicon, 9 1/4" x 1/4" chips can be connected in one module as illustrated in Figure 7. The total silicon area of this configuration is $3.63*10^8$ $um^2$ which is enough for the implementation above.

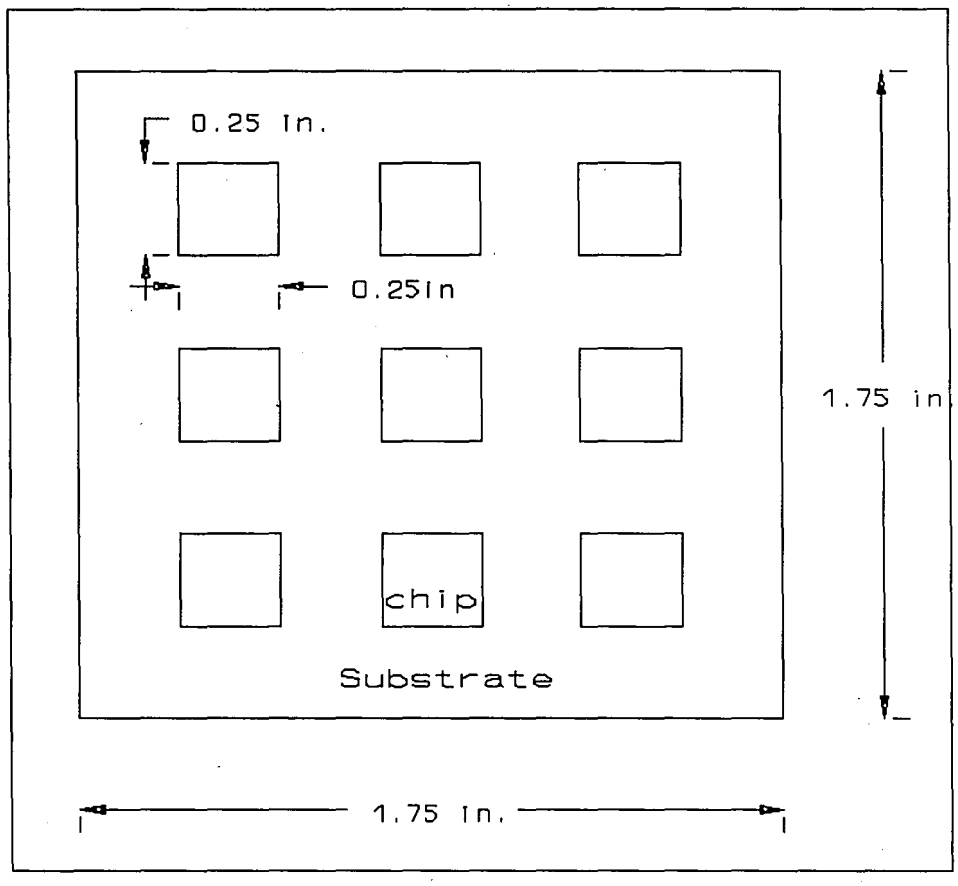


**Figure 7**

# WAFER-SCALE INTEGRATION

Wafer-scale integration is an alternative packaging option with its own tradeoffs. It is important to mention at the outset that the packaging technology discussed here is considered an incremental advancement over standard VLSI techniques instead of the more traditional full-wafer implementation. All chip-to-chip interconnections are made on the silicon itself, thus providing the highest densities possible. Because of yield limitations and other technical difficulties, however, several circuit blocks on a die are likely to be defective. Thus there is a need for redundancy in circuits to enable fabrication of enough failure-free circuit blocks to form a complete system on each wafer. Die sizes are large when compared to equivalent VLSI devices [9]. However, circuits can still be patterned using wafer steppers.

Raw material costs for WSI packaging are predicted to be less than MCM packaging cost, mainly due to the need for the interconnect substrate in MCM's. For the same function, however, die sizes in WSI are larger, thus increasing silicon costs. This tradeoff is discussed further in the cost section.

Specific information on WSI memory cell size, redundancy, packaging technology, thermal dissipation capacity and other technical data was obtained through publications and conversations with INOVA Microelectronics engineers. INOVA, previously based in Colorado Springs, CO, is to date one of the few WSI enterprises to have produced modules in high volume, primarily because

wafer approaches. They produced 1Mb SRAM devices containing over five million transistors each with a total die size of 320 square mm.

The calculation of required silicon area capacity is the same as for MCM's except for the addition of an INOVA redundancy factor of 35% which was extrapolated from INOVA product specifications. Thus the silicon area value becomes $4.55*10^8 um^2$. Several WSI sites can be easily found on a 5" diameter wafer (see Figure 8).

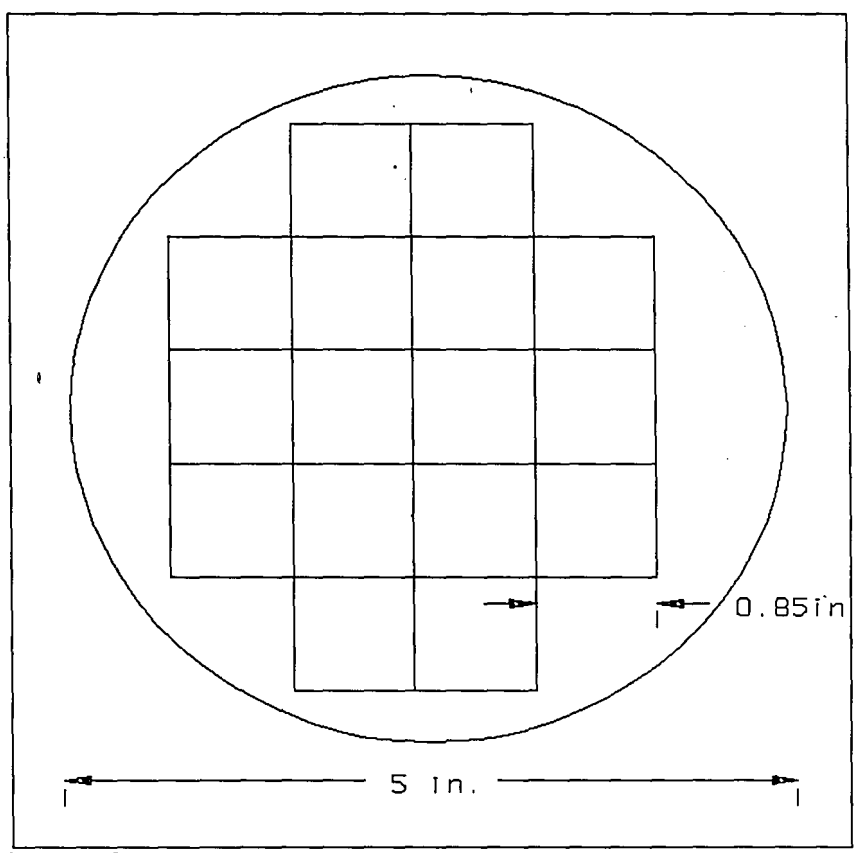


**Figure 8**

# MANUFACTURING METRICS

In this section the modelling of the manufacturing metrics is discussed, followed by results determined based on the models.

**TIME TO MARKET:** The time to market concept has become increasingly important in competitive manufacturing. In the complete sense, time to market is the period required to bring a new product from initial concept to the marketplace. For this analysis only the manufacturing development period will be considered, although the design development component will be duly addressed. Countless companies in microelectronics have failed due to an inability to introduce their latest products before their competitors. Thus comparative data on WSI and MCM time to market values is a significant metric by which they can be compared.

Mathematical modelling was attempted for two important components of time to market: Line set-up time and order turnaround time. Each component has its significance under different situations: Line set-up for an enterprise at the decision stage for investing in a new packaging line, and order turnaround time for an enterprise with an existing line that seeks to overhaul it for a new packaging module. Tasks involved for each component include quality control qualification, environmental testing and burn-in cycle set-up. The

following data was acquired for each subcomponent:

Line set-up: Sources referred to included Beckman Industrial, Fullerton, CA and INOVA. Myriad factors contributed to line set-up values, including rate of capital investment, manhours alloted to the task, and delivery times of tool suppliers.

Typical values serve to model this metric better than a mathematical equation. They are as follows:

MCM: low - 6 months; high - 1.5 years;

WSI: low - 6 months; high - 1.5 years;

Product Turnaround Time: Sources included INOVA and MCC (Microelectronics, Computer and Technology Consortium). Typical values obtained here:

MCM: 3 months;

WSI: normally 3 months from order writing to time of delivery of first parts;

Because the values for both MCM and WSI are the same, it apprears that no advantage is observed for either packaging technology under this metric. The design development cycle time, however, has not been discussed. The INOVA effort, although successful initially, failed when it attempted to design and build its next generation SRAM. INOVA engineers could not bring the new product to market before competitors captured most of the market. This

phenomenon is suggestive of a disadvantage for WSI over MCM's regarding time to market.

**COST:** Typical cost equations found in the literature include many terms which are not significant in a first order estimate. Terms such as design overhead and machine set-up costs are negligible when compared to manufacturing overhead and raw material costs. The following equations were used to model cost [10]:

Total Cost:

$$Mfg.Cost = [OH_s * Per_s + OH_p + V[C_m + C_o + (1-Y)\,C_r]]\,(1+B) \qquad (2)$$

Unit Cost:

$$Mfg.Cost = \frac{[OH_s * Per_s + OH_p + V[C_m + C_o + (1-Y)\,C_r]\,(1+B)}{V(1-D)} \qquad (3)$$

where

% of semiconductor line product going into packages: $Per_s$

cost of semiconductor mfg. overhead: $OH_s$

cost of package mfg. overhead: $OH_p$

volume of product produced: V

final product defect rate: D

cost of raw material: $C_m$

cost of operations: Co

semiconductor yield: Y

cost of rework: $C_r$

burden rate: B

Several terms require explanation. $Per_s$ accounts for the need to factor a percentage of overall semiconductor line cost into the total cost equation because only a fraction of the semiconductor line capacity is going to be used to produce silicon for MCM or WSI modules; $C_m$ refers to both silicon and packaging materials; and B refers to the sales, marketing and administrative overhead which is factored into module cost.

Typical parameter values include an investment of $100 million for a 1.2 um line, high yields, low defect counts, a burden rate of 30%, and a $Per_s$ value of 10%. Unit cost curves indicate that overhead investment cost factors in heavily at low volume, while the raw material cost is most important at high volumes. Estimating $C_m$ is difficult due to the proprietary nature of such information. It is left to the user of the spreadsheet program to supply such information to make an accurate comparison. Several factors must be considered, but primarily the raw material comparison comes down to the extra silicon cost for WSI vs. the more expensive packaging cost for MCM's. Illustrations of the packages modelled are given in the heat dissipation section.

Regardless of raw material cost, MCM's or WSI parts will be costed

relatively low at high volumes of production. For this to occur, demand must be high for the modules. The market for MCM's is predicted to rise to $7 billion from the current $50 million by 1997 [5]. Another study by Dataquest has estimated demand to be as high as $8 billion (see Figure 9). Forecasted WSI demand is less certain: Much will depend on the technology's acceptance by a sceptical customer base that is accustomed to unsuccessful WSI attempts [11].

Example cost vs. volume plots for both total and unit costs are given in the appendix. The plots are based on parameter values listed in the secondary inputs appendix section.

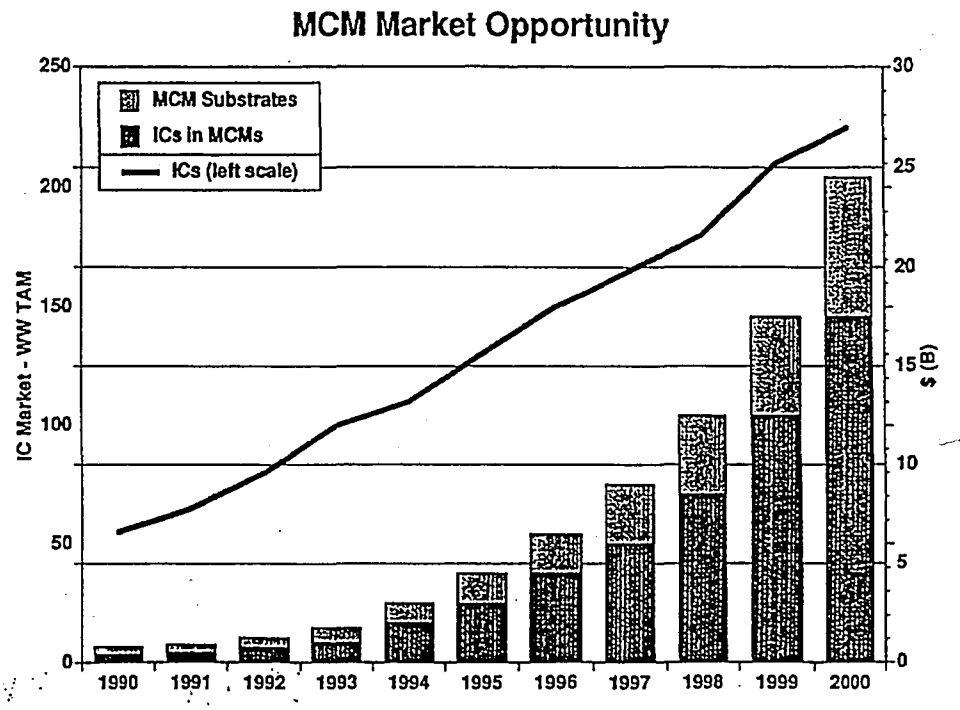


Figure 9

**PRODUCTION RATE:** From a comparative point of view, this metric is important because the packaging technology with the higher production rate generates higher net profits given that demand doesn't gate capacity.

Production rate data was acquired for MCM's and WSI lines from Beckman, INOVA and MCC:

MCM: 30,000 modules/mo. (high-volume, single product line);

WSI: 7-18K parts/mo;

Bottlenecks cited included the plasma cure and etch cycle for MCM's and the laser reconfiguration step for WSI (which involves removing wafers from the clean room and has a 1 week cycle time). Given current demands, it can be assumed that the costs of increased capacity on bottleneck processes outweighs the return on investment. From the data above, MCM's have some advantage in this metric because for the same amount of function, many more modules can be produced. Furthermore, as indicated in the cost section, the WSI future demand profile is uncertain, thus casting doubt on the need to run future WSI lines at the production rate suggested above.

Another related point is the difference in manufacturing lead time (MLT) of the two options. WSI has potentially fewer processing steps than MCM's, especially when the manufacturing of the MCM substrates is done internally instead of being vendored out. This implies reduced work in process for the WSI option, as well as fewer resources tied up with materials. If WSI

requires less processing, equipment and facilities reductions can also be forecast for the WSI option. Therefore, from an MLT point of view WSI is forecast to have an advantage.

**HEAT DISSIPATION:** Removing heat generated from electronic modules is an important metric to model. Very complex analytical tools exist to model the rate of thermal dissipation from the silicon to the outside world. Which tool is selected depends on the level of accuracy and detail required.

For this study a first order model based on the one-dimensional thermal resistance measure was devised to estimate thermal dissipation rates (in Watts) given typical material sizes and geometries [12]. In the spreadsheet specific thicknesses, areas, thermal conductivities and heat sink temperatures can be varied to determine their impact on the first order estimate. The operating temperature of the silicon is also calculated.

To compare MCM and WSI the following analysis was conducted on the spreadsheet. It was sought to determine the silicon operating temperature of the two modules. Significant differences in temperature would suggest reliability differences between the two packaging technologies.

First, the power consumed by the design operating in either module was calculated. This was based on VLSI theory for CMOS power consumption [7]. According to VLSI theory, the power consumed by a CMOS design consists of static and dynamic power. Static power is dissipated when gate are idle, or not switching. In this state a small leakage current flows from the gate, thereby consuming power. Dynamic power is dissipated when gates are switching. The amount of power dissipated by gate depends on several factors, including the

load capacitance per gate and the switching speed.

The following equations were used to model power consumption [7]:

$$P_{static}=\sum_{1}^{n} I_L * V$$

where

n = number of gates (two transistors/gate)

$I_L$ = leakage current = 0.1-0.5 nAmperes/gate

V = power supply voltage = 5 Volts

$$P_{dynamic}=nC_L V^2 f$$

where

$C_L$ = load capacitance/gate

f = clock speed

n = number of switching devices

To compute the number of switching devices, it was assumed that all the logic gates were switched every clock cycle while only a fraction of the memory cells were switched.

To compute the memory contribution to power dissipation, worst-case power consumption values for 1 Mb DRAMS, SRAMs and ROMs were acquired from IC databooks, and a weighted average was computed based on the memory type percentages listed earlier. The worst-case memory power consumption was computed to be 2.5W.

Assumptions included 50,000 gates, 1,048,576 memory cells, 0.0624 pF load capacitance per gate, 5V power supply and a 50 MHz clock speed. The worst case power consumed was computed as 10.3 Watts, which makes sense given typical worst case values of subcomponents given in IC databooks. This power value is accurate for both packaging technologies. Although the wafer-scale module incorporates 35% more silicon, this extra circuitry compensates for the circuitry lost due to particle defects, resulting in net gate and memory cell counts close to that of the MCM.

Next, thermal resistance models were devised based on typical module geometries. The theory works as follows: A temperature difference between two points (in this case between the external ambient heat sink and the silicon heat source) is the "voltage difference" which drives the "current" of heat flow in Watts. The thermal resistance impedes this heat flow and is calculated according to material geometries by the following formula:

$$R_m = \frac{L_m}{K_m A_m}$$

where

$L_m$ = material length in meters

$A_m$ = material cross-sectional area in meters

$K_m$ = thermal conductivity of material in Watts/(meter-Kelvin)

Figure 10 graphically depicts model operation:

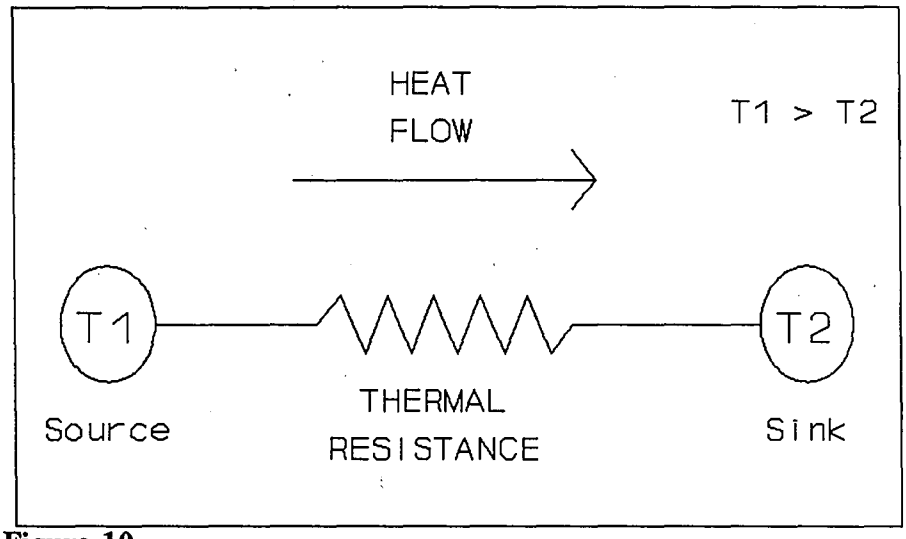


**Figure 10**

With this theory, it was possible to compute the expected silicon operating temperatures of the two modules. Both MCM and WSI modules assumed an external air temperature of 25 degrees Celsius which did not vary: The air served as a heat sink. Figure 11 shows the cross-sectional package and thermal resistance models used for MCM's:

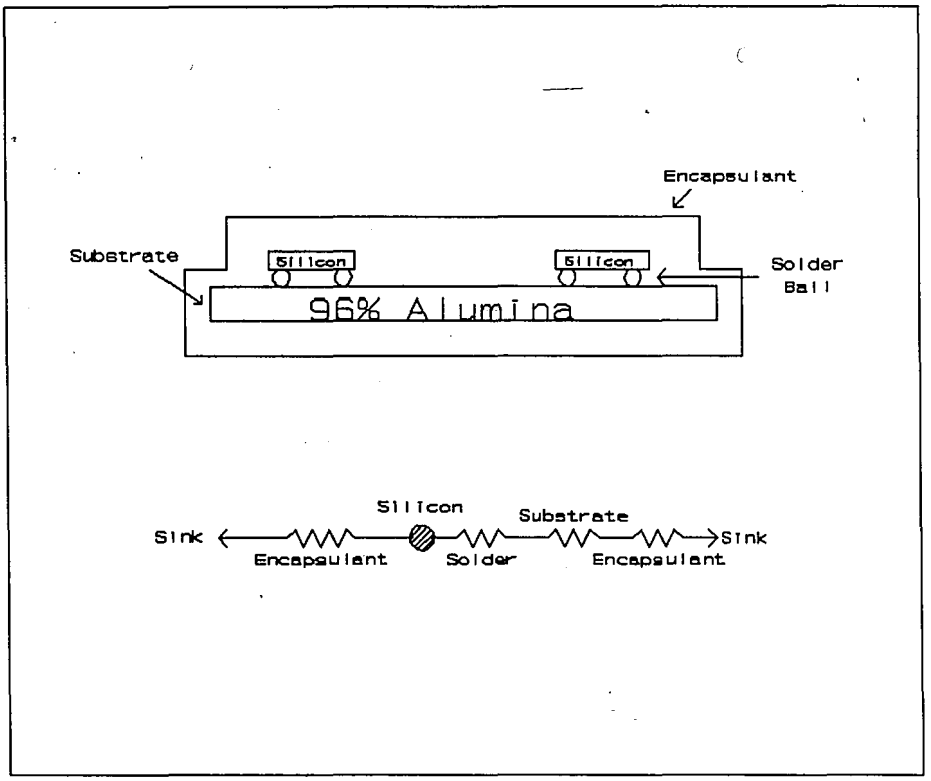


**Figure 11**

The following material values were used in the computation:

| Material | Length (m) | Area ($m^2$) | K (W/mK) |
|---|---|---|---|
| Encapsulant | 0.01 | .000363 | 12.11 |
| Substrate | 0.01 | .000363 | 29.41 |
| Solder | 0.001 | .000240 | 32.70 |

**Figure 12**

Thermal conduction was assumed to occur only in the direction perpendicular to the silicon. This approximation was considered good by experts for a first order, comparative analysis.

The solder ball area is actually 240 times that of the area per solder ball; it was assumed that a 75 pin I/O pin design would require approximately 240 solder ball connections from the silicon dies to the substrate.

I/O pin thermal conduction was neglected in the first order estimate for both MCM and WSI modules. It was assumed that the modules would be fastened very close to motherboards, thus restricting thermal conduction from the pins significantly.

Similar models for the WSI option are shown in Figure 13:

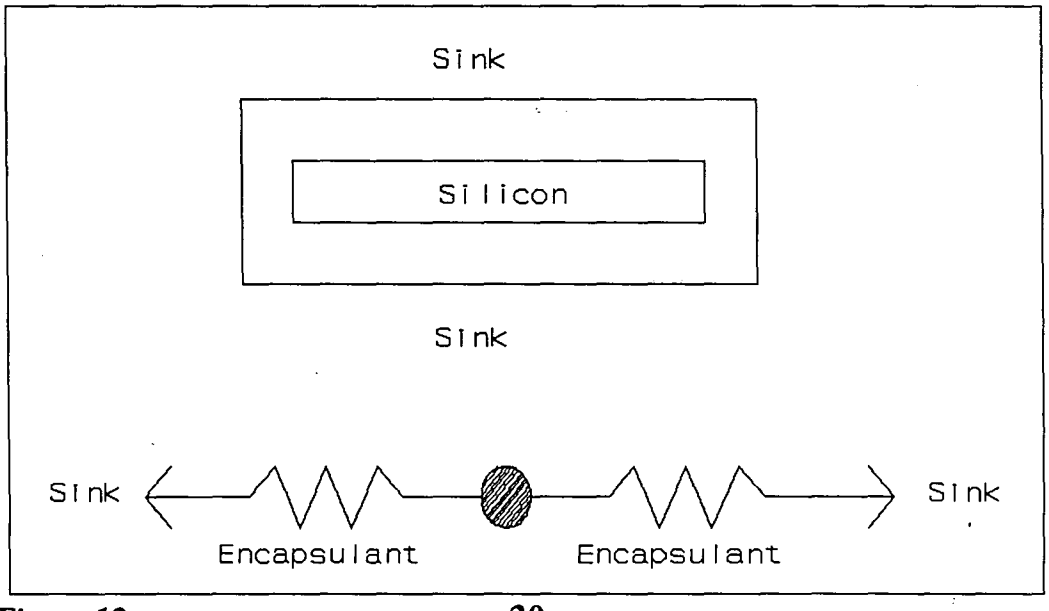


**Figure 13**

90% alumina was chosen as the encapsulant for this case. It has the following properties:

Length: 0.01 m Area: $4.55*10^{-4}$ $m^2$ K: 12.11 W/mK

For MCM's, in order to dissipate 10.3 Watts it was calculated to operate the silicon at 39 degrees C. For WSI, 34 degrees C. Both temperatures fall within typical operating temperatures [11] and are well below the maximum allowable temperatures for short-term operation [13]. Values approximately ten degrees higher than what was computed are more common. The discrepancy is accounted for by the lack of off-chip drivers in the analysis which would contribute significantly to power consumption if included. Because this is a comparative model, however, the assumption was made that off-chip drivers would contribute equally in both modules. In future research, the spreadsheet model can be upgraded to include variances in driver capability if desired.

Regarding the silicon operating temperatures computed, the temperatures are sufficiently close such that no long-term reliability differences should be deduced based on thermal issues in the first-order estimate.

**RELIABILITY:** Measuring reliability is probably the most difficult manufacturing metric to model for electronic modules due to its innate complexity. Because development in this field is revolutionary, not evolutionary, reliability cannot be taken for granted [14]. Empirical data is required to test reliability theories on particular modules. Such data has not been acquired for high-volume WSI products because very few products have existed in the field for long periods of time. For this reason a qualitative discussion is given as to why WSI is expected to be more reliable than MCM's.

Experts have cited the drastically reduced number of off-chip interconnections in WSI as a major reliability benefit. This is because on-chip thin film metal interconnections are inherently more reliabile than off-chip wire bonds, solder joints and the like. Furthermore, WSI redundancy and self-reconfigurability makes fault and failure tolerance easier than for most technologies [15].

An effort at Westinghouse Electric has attempted to forecast global module reliability for WSI vs. VLSI. The analysis uses the military reliability models found in MIL-HDBK-217. The models factor in operating temperature, design complexity, environmental factors and technology maturity [10]. Results for a design of 450,000 gates included failure rates of 0.3 failures per million hours (fpmh) for WSI vs. 10.0 fpmh for VLSI [11]. Thus an improvement factor of over 30x is predicted for WSI over VLSI.

Given that MCM's use VLSI technology and substantial off-chip interconnect, based on the above evidence is it safe to conclude that WSI is more reliable than MCM's for the typical design. How large the difference is will be determined as researchers gather data for WSI packages.

# CONCLUSIONS

The intent of this study was to excercise the modelling of manufacturing metrics to gauge the long-term feasibility of two different packaging technologies. It is clear that the first order mathematical technique has merit in that the values calculated were within expected norms. Values obtained from industry further aided the feasibility study.

Which packaging technology is chosen depends on several factors. If reliability considerations are paramount, for example, then WSI will be chosen. If profitability is the primary motive, then MCM's will be chosen because high demand has been forecasted, thus suggesting increased sales and low cost per sale. No significant first order advantage is observed under the time to market and heat dissipation metrics: Both technologies appear to function equally well under them. When design development time is considered, MCM's appear to have an edge.

On the production rate metric, MCM's appear to have some advantage. However, when manufacturing lead time is considered, WSI wins due to forecasted reduction in work-in-process. These two opposing factors must be weighed by the company considering the packaging options to determine which factor is paramount.

Given that MCM's have already established themselves in the high-performance market, MCM's are likely to penetrate the high-volume realm

before WSI does. Additional evidence for this includes the "application shock" factor mentioned earlier in that some aspects of WSI may not be easily accepted by the marketplace.

From a concurrent engineering standpoint, the metric calculations and acquired field values can be used to determine gross differences in packaging options. It is important to reiterate that the models are first-order. Thus values that are close for a given metric must be recalculated through more comprehensive techniques. Nevertheless, for the designer or engineering manager the spreadsheet tool and the knowledge acquired here can prove useful in choosing among alternative packaging technologies in microelectronics. In this study MCM's and WSI modules were compared, but it is hoped that future studies will compare other options as well.

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# APPENDIX

SPREADSHEET MODEL: ELECTRONIC PACKAGING OPTIONS

WRITTEN BY: JAWAHAR P. NAYAK

This spreadsheet model computes manufacturing metrics based on design data for alternative packaging technologies. A detailed explanation along with supporting discussions can be found in the Master's Thesis "Manufacturing Metrics For Design: Wafer-Scale Integration and Multichip Modules."

The user of this program need only vary the primary model inputs to input design criteria. The program uses this data to compute parameters for the following metrics: Package heat dissipation capability, module cost and silicon area consumed by the design.

For the designer or engineering manager with proprietary knowledge the secondary model inputs can be manipulated to reflect variations in technology and knowledge base. The numbers currently inputted are based on experience and readings on WSI and MCM's. A rationalle for the current data is given in the report.

PRIMARY MODEL INPUTS

| | |
|---|---|
| MODULE CLOCK SPEED (MHz): | 50 |
| NUMBER OF PRIMARY INPUTS: | 35 |
| NUMBER OF PRIMARY OUTPUTS: | 40 |
| NUMBER OF GATES: | 50000 |
| NUMBER OF MEMORY CELLS: | 1048576 |
| MODULES DEMANDED: | 50000 |

SECONDARY MODEL INPUTS

SILICON AREA:

| | |
|---|---|
| %ROM | 0.25 |
| %SRAM | 0.5 |
| %DRAM | 0.25 |
| %REDUNDANCY (WSI) | 0.35 |

HEAT DISSIPATION DATA:

| | |
|---|---|
| Leak. Current (nA): | 0.5 |
| Supply Voltage: | 5 |
| Load Capacitance (pF): | 0.0624 |
| Heat Sink Temp. (Celsius): | 25 |

MATERIAL DATA:

| | | WSI | MCM |
|---|---|---|---|
| Encapsulant: | A: | 0.000455 | 0.000363 |
| | L: | 0.01 | 0.01 |
| | K: | 12.11 | 12.11 |

| | | WSI | MCM |
|---|---|---|---|
| Substrate | A: | ******** | 0.00036 |
| | L: | ******** | 0.01 |
| | K: | ******** | 29.41 |

| | | WSI | MCM |
|---|---|---|---|
| SOLDER | L: | ******** | 0.001 |
| | A: | ******** | 0.00024 |
| | K: | ******** | 32.7 |

COSTING DATA:

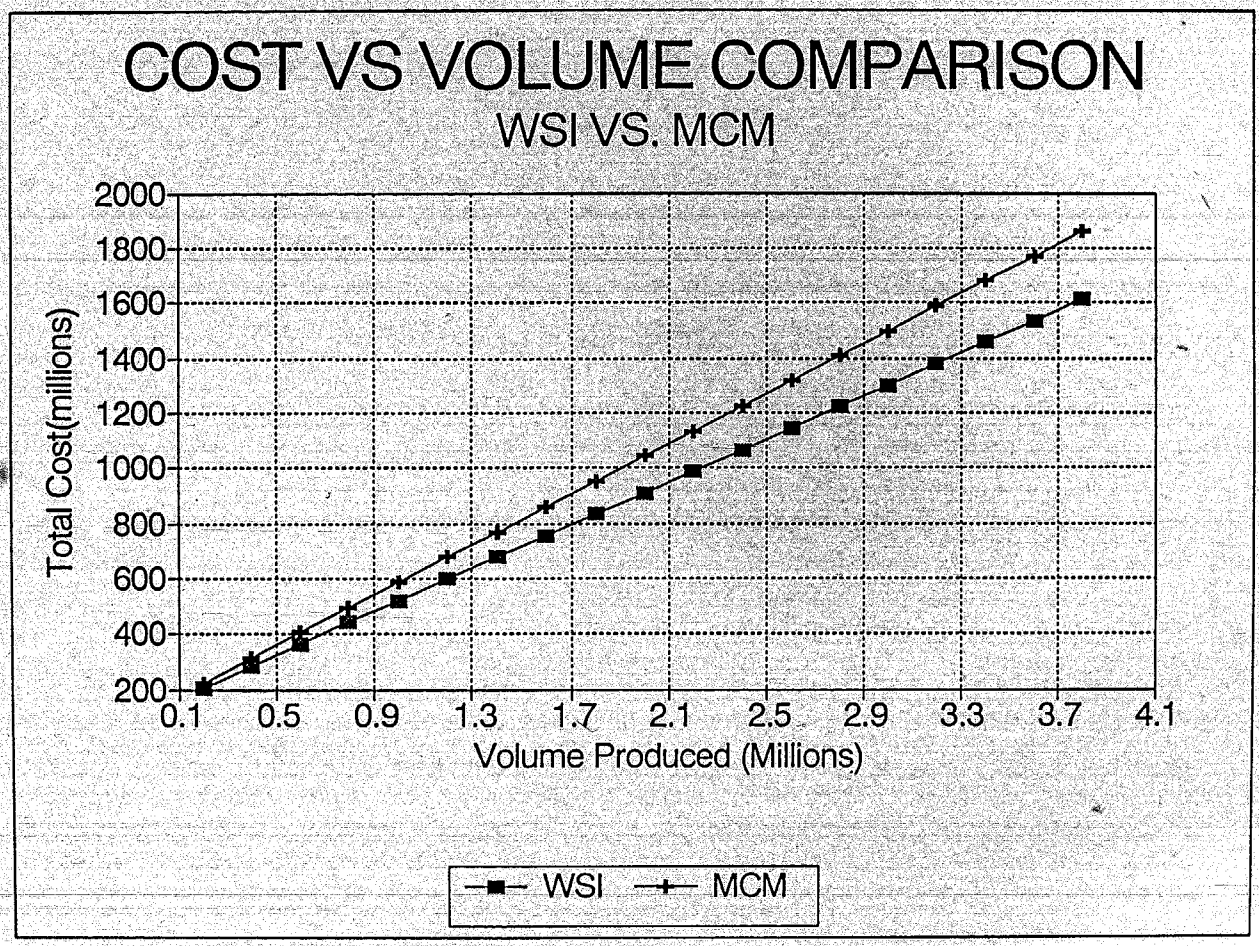
| | WSI | MCM |
|---|---|---|
| OHs: | 1E+08 | 1E+08 |
| Per% | 0.1 | 0.1 |
| OH: | 15000000 | 20000000 |
| Cm: | 300 | 350 |
| Cr: | 1 | 1 |
| D: | 0.0005 | 0.0001 |
| Y: | 1 | 0.8 |
| Co: | 0.15 | 0.15 |
| B: | 0.3 | 0.3 |

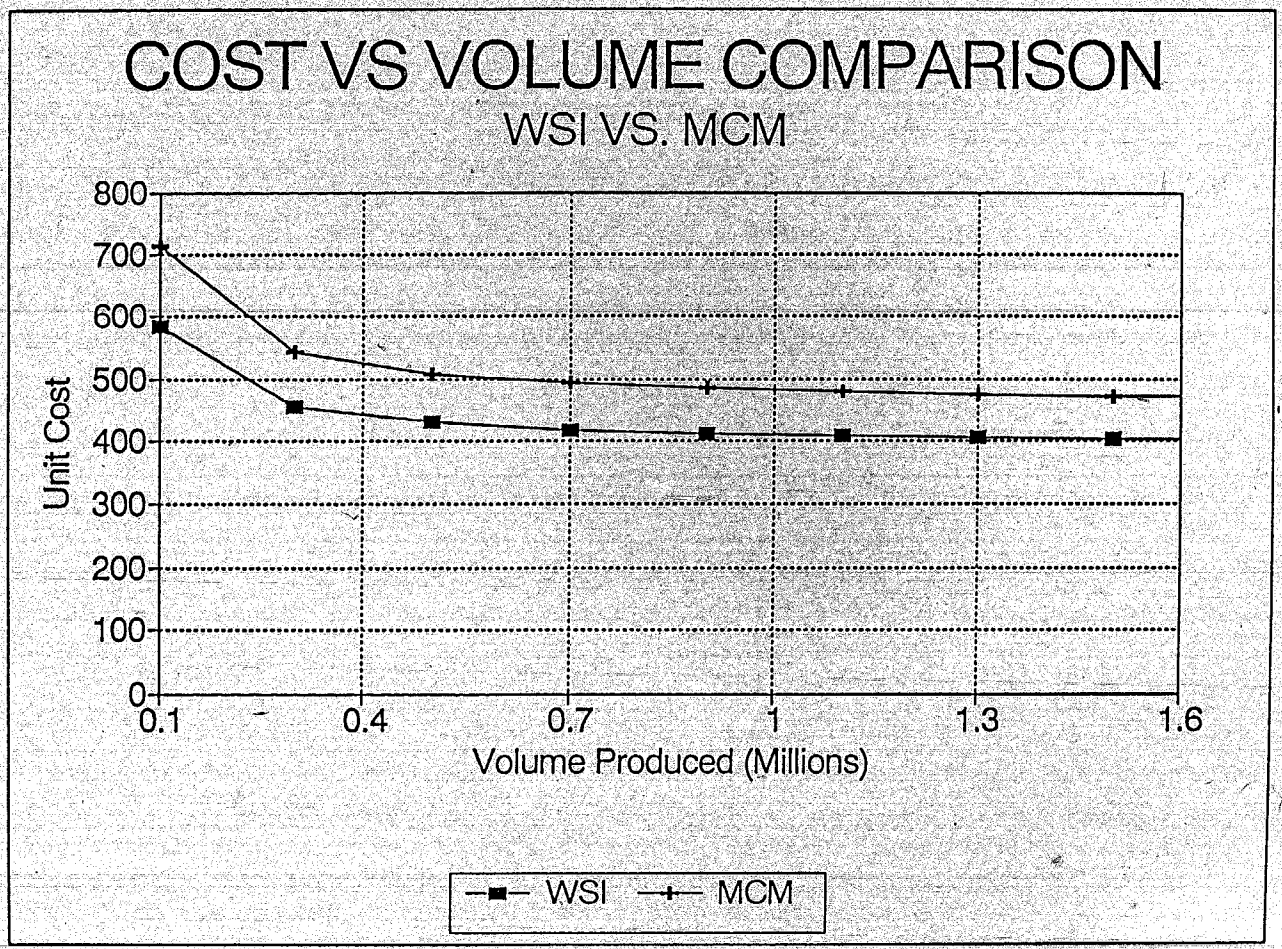
| PRIMARY MODEL OUTPUTS | WSI | MCM |
|---|---|---|
| SILICON AREA (sq. um's): | 4.55E+08 | 3.37E+08 |
| NUMBER OF MODULES NEEDED: | 50000 | 50000 |
| POWER CONSUMPTION(Watts): | 10.30582 | 10.30582 |
| OPERATING TEMP (Celsius): | 34.35184 | 38.75341 |

COST VS VOLUME:

TOTAL: Press ALT-C for TC comparison

UNIT: Press ALT-B for UC comparison


COST VS VOLUME COMPARISON
WSI VS. MCM
Total Cost(millions)
2000
1800
1600
1400
1200
1000
800
600
400
200
0.1
0.5
0.9
1.3
1.7
2.1
2.5
2.9
3.3
3.7
4.1
Volume Produced (Millions)
WSI
MCM


COST VS VOLUME COMPARISON
WSI VS. MCM
800
700
600
500
400
300
200
100
0
Unit Cost
0.1
0.4
0.7
1
1.3
1.6
Volume Produced (Millions)
WSI
MCM

# VITA

Jawahar Pundalik Nayak was born on May 18, 1968 to Pundalik and Chandrakala Nayak in Hackensack, NJ. Jawahar attended Port Reading Elementary School and Woodbridge Junior High School in NJ before graduating from Woodbridge Senior High School in June, 1986. Graduating as the Valedictorian of his class, he attended Princeton University from September, 1986 to June 1990 receiving a Bachelor of Science in Engineering (B.S.E.) degree in Electrical Engineering.

Upon graduation from Princeton, Jawahar fulfilled an MSE internship with the International Business Machines Corporation in Burlington, VT from August 1990 through December 1990, working on VLSI physical design of ASIC's. Upon completion of the internship Jawahar enrolled in the Department of Electrical Engineering and Computer Science at Lehigh University and began his graduate studies in Manufacturing Systems Engineering.

Jawahar has one publication and two conference papers to his credit. They are:

Cost and performance criteria for selection of materials and processes in microelectronics packaging (co-authored with W. Eakin and K. Gardiner). *Journal of Electronics Manufacturing*, 1 (1), 13-22.

Manufacturing Metrics For Design: Wafer-Scale Integration and Multichip Modules (co-authored with K. Gardiner). *Manufacturing Measurements - 21st Century Metrics (May 5 & 6, 1992)* Center for Manufacturing Systems Engineering, Lehigh University, Bethlehem, PA.

Manfacturing Metrics For Microelectronics Design (co-authored with K. Gardiner). *Symposium On Manufacturing Aspects In Electronic Packaging (November 8-13, 1992)* American Society Of Mechanical Engineers, Anaheim, CA.

Jawahar is a member of IEEE, SME and Sigma Xi.

END

OF

TITLE