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AUTHOR:

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TITLE:

Automated Measurement of Memory Devices

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# AUTOMATED MEASUREMENT OF MEMORY DEVICES

by

Amit Kumar Banerjee

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

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This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science.

May 20, 1993
(date)

Marvin H. White
Thesis Advisor

Alastair D. McAulay
Chairman of Department

**SONOS : The Final Frontier**

This is a thesis of the Sherman Fairchild Center; in its continuing mission to explore novel, reliable memories; to seek out scaled devices with low programming voltages; to boldly go where industry has not gone before.

Ph. D. Trek

# Acknowledgements

I would first like to express my eternal gratitude to my advisor, Prof. Marvin H. White for his valuable guidance and support. It is a rare privilege working with such a gifted researcher whose concern for his students is truly overwhelming. I am also indebted to Dr. Anant K. Agarwal whose faith in my abilities has allowed me to pursue my research ambition. He has always extended a helping hand, especially when I needed it the most.

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# Contents


**Acknowledgements** iv

**List of Figures** vii

**List of Symbols** xi

**Abstract** 1

**1 Introduction** 3

1.1 Historical Background . . . . . . . . 3

1.2 Testing of Memory Devices . . . . . . . . 5

1.3 Scope of Thesis . . . . . . . . 7

**2 The SONOS Memory Device** 9

2.1 Closed Form Erase/Write Model . . . . . . . . 12

2.2 Retention Model . . . . . . . . 18

**3 Automated Tests and Measurement** 21

3.1 Dynamic Characterization of memory transistors . . . . . . . . 21

3.2 Test Vehicles in Literature . . . . . . . . 22

3.3 The Erase-Write-Read-Idle Circuit . . . . . . . . 26

3.4 Pattern Generator . . . . . . . . 28

3.5 Motivation for Adopting HPIB . . . . . . . . 30

3.6 HPIB Interface . . . . . . . . 31

3.7 Signal Lines . . . . . . . . 32

3.8 Circuit Description . . . . . . . . 35

3.9 The Automated NVSM Test Setup . . . . . . . . 36

**4 Experimental Data** 40

4.1 Objective . . . . . 40
4.2 Erase/Write Characteristics . . . . . 40
4.3 Retention . . . . . 42
4.4 Endurance . . . . . 42
4.5 Quality of Oxides . . . . . 45

**5 Concluding Remarks** **48**
5.1 Advantages of the Automated System . . . . . 48
5.2 Testing of Arrays . . . . . 50
5.3 To the Making of a Better Device . . . . . 51

**References** **52**

**A SONOS Device Fabrication Technology** **56**
A.1 Starting Material . . . . . 56
A.2 LOCOS Oxidation . . . . . 56
A.3 Field Implant . . . . . 57
A.4 Field Oxide 6k$\AA$ . . . . . 57
A.5 Sacrificial Oxide . . . . . 58
A.6 Gate Dielectric for SONOS . . . . . 59
A.7 Polysilicon, $n^+$gate . . . . . 61
A.8 Contact Window . . . . . 61
A.9 Metallization . . . . . 62
A.10 Back Contact . . . . . 63
A.11 Some Precautions . . . . . 64

**B System Operation** **66**
B.1 Operating Procedure . . . . . 66
B.2 The Algorithm . . . . . 68

**Vitae** **73**

# List of Figures

1.1 Energy Band Diagram of some MIS devices . . . . . . . . . . . . . . 4

2.1 The cross-section of the SONOS device . . . . . . . . . . . . . . . . . . 10

2.2 The ideal energy band diagram of the SONOS device . . . . . . . . . 10

2.3 The energy band diagram and the circuit equivalent of the SONOS device during Erase and Write operations. . . . . . . . . . . . . . . . . 11

2.4 Notice the difference in the energy band diagram in Idle mode depending on the last operation, Erase or Write. . . . . . . . . . . . . . 13

2.5 The curves show the shape of typical Erase/Write curves for an n-channel SONOS device. The cross-over time between the Erase and Write curves provides a measure of the programming speed of the device for a certain programming voltage. . . . . . . . . . . . . . . . 17

2.6 A typical retention curve shows the decay in threshold voltage of a device with time. Notice the difference in the rate of decay after the Write and the Erase states. . . . . . . . . . . . . . . . . . . . . . . . 19

3.1 Flatband shifts in High Frequency C-V plots depending on the charge stored in the nitride [12]. . . . . . . . . . . . . . . . . . . . . . . . . . 23

3.2 Change in flatband voltage is measured by sample and hold [24]. . . . 23

3.3 Static I-V characteristics are used to determine threshold shift. . . . . 24

3.4 The test station for determination of erase/write and storage characteristics used by White and Cricchi. This is in the source follower category of threshold detection schemes [25]. . . . . . . . . . . . . . . . 24

3.5 Saturated drain constant current method facility [26]. . . . . . . . . . 25

3.6 The Erase/Write/Read Circuit [27,18]. . . . . . . . . . . . . . . . . . . 27

3.7 Representation of the Erase-Write-Read circuit during the different modes of operation of the device under test. . . . . . . . . . . . . . . 28

3.8 Block diagram of the Pattern Generator . . . . . . . . . . . . . . . . 29

3.9 The pulse sequence applied to the terminals of the device under test at the various modes of operation. . . . . . . . . . . . . . . . . . . . 29

3.10 Block diagram representation of the HPIB (IEEE-488) Data Interpreter [30]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 33

3.11 Circuit diagram of one of the channels in the HPIB (IEEE-488) Data Interpreter. The address is set using the dip switches. Inputs and outputs are buffered and latched TTL compatible output is provided [20]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 34

3.12 The automated test setup for nonvolatile semiconductor memories [30]. 37

4.1 The Erase/Write characteristics of the SONOS device is shown with 10V and 6V programming voltage. The gate dielectic is constituted as $x_{ot} = 20\mathring{A}, x_n = 68\mathring{A}, x_{ob} = 72\mathring{A}$. The memory window is 3V for 10V programming, but 2V for 6V programming voltage. The cross over time is almost consistent at $4\times10^{-3}$s [30,33]. . . . . . . . . . . . 41

4.2 The retention characteristics of SONOS device with 10V programming voltage was used with 29ms of write time and 150ms of erase time. The thicknesses were $x_{ot} = 20\mathring{A}, x_N = 68\mathring{A}, x_{ob} = 72\mathring{A}$. $W/L = 150\mu m/10\mu m$ [30]. . . . . . . . . . . . . . . . . . . . . . . . . 43

4.3 The threshold voltage is plotted against the number of erase/write cycles. The dielectric thicknesses are $x_{ot} = 20\mathring{A}, x_N = 73\mathring{A}, x_{ob} = 54\mathring{A}, W/L = 150\mu m/10\mu m$. 9V programming was done for 3ms write and 30ms erase [30]. . . . . . . . . . . . . . . . . . . . . . . . . 44

4.4 This is a comparison between the retention characteristics of two SONOS devices after they have been cycled a million times. The gate oxides of one device was grown in the conventional single wall oxidation furnace and the other in an ultra clean triple wall oxidation furnace (TWO). 10V programming voltage was applied with 20ms write and 150ms erase times on the TWO furnace grown device and 9V programming was done on the SO furnace grown device for 3ms write and 30ms erase times. Both devices measured $W/L = 150\mu m/10\mu m$. Notice that the single wall furnace grown device has faster rate of stored charge decay [30,33]. . . . . . . . . . . . . . . . . . . . . . 46

4.5 The growth of Si-Si$O_2$ interface trap density, $D_{it}$, is plotted as a function of the number of erase/write cycles. The dielectric thicknesses are shown in the figure. The single wall furnace grown device had dimensions of $W/L = 24\mu m/24\mu m$. 9V programming was used for 3ms write and 30ms erase pulses. The TWO furnace grown device had $W/L = 48\mu m/24\mu m$ and was programmed with 20ms write and 150ms erase pulses at 10V. The difference in the programming voltages is to maintain same field in the gate dielectrics of the two devices [33,21]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 47

A.1 Field implantation . . . . . . . . . . . . . . . . . . . . . . . . 57

A.2 After field oxidation, the $Si_3N_4$ is removed using hot nitric acid followed by etching the pad oxide with HF acid. . . . . . . . . . . . . 58

A.3 The stacked gate dielectric . . . . . . . . . . . . . . . . . . . . 59

A.4 Formation of the n+ gate using phosphorus diffusion . . . . . . . . . 60

A.5 The n+ source and drain contacts are formed using phosphorus diffusion 62

A.6 The device cross-section after the contact windows have been opened 63

A.7 The n-channel SONOS device cross-section . . . . . . . . . . . . . . 64

B.1 Schematic of the Pattern Generator showing the signal paths and the memory distribution scheme. The counter ICs are loaded from the memory ICs [18]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . 67
B.2 The flowchart of the programming of the Pattern Generator explicitly showing the code sequence used. . . . . . . . . . . . . . . . . . . . . . . . 70
B.3 The basic operations and their patterns . . . . . . . . . . . . . . . . . . 71

# List of Symbols

| | |
|---|---|
| $k$ | Boltzmann's constant ($1.38 \times 10^{-23} \frac{J}{K}$) |
| $q$ | electronic charge ($1.6 \times 10^{-19}$ C) |
| $n_i$ | intrinsic density of electrons ($cm^{-3}$) |
| $E_C$ | conduction band energy level |
| $E_G$ | energy gap ($eV$) |
| $E_V$ | valence band energy level |
| $N_C$ | effective density of states at edge of conduction band ($cm^{-3}$) |
| $T$ | temperature ($K$) |
| $V_{FB}$ | flatband voltage ($V$) |
| $V_{GB}$ | applied gate voltage with reference to bulk ($V$) |
| $V_{th}$ | threshold voltage (V) |
| $\epsilon_{ox}$ | permittivity of silicon dioxide ($3.45 \times 10^{-13} F/cm$) |
| $\epsilon_N$ | permittivity of silicon nitride ($6.64 \times 10^{-13} F/cm$) |
| $\phi_s$ | work function of the semiconductor ($V$) |
| $\phi_m s$ | work function difference between the gate metal and semiconductor ($V$) |
| $J$ | current density ($A/cm^2$) |
| $\chi_{ox}$ | electron affinity of silicon dioxide |

# Abstract

A large effort is underway to utilize the many advantages of the SONOS technology to successfully design and fabricate a low voltage programmable EEPROM or a semiconductor disk meeting stringent requirements of memory retention and endurance. This requires extensive testing of a large number of devices emulating the operations these devices will have to endure in an array while simultaneously permitting the measurement of small analog changes in the memory property to provide a better understanding of the device physics behind the operations.

A completely automated test station for performing exhaustive measurements on nonvolatile semiconductor memories, namely, SONOS (Silicon Oxide Nitride Oxide Silicon) transistors, has been designed and implemented. Time-controlled pulses are applied to the device under test which exercises the various modes of memory operation. Software has been developed to perform a series of measurements to generate Erase/Write, Retention and Endurance characteristics for SONOS nonvolatile memory transistors. The data can be transferred within different environments, permitting the usage of a large number of parameter extraction software packages. This system permits a wide variation (12 decades) in the time-controlled pulses to enable Erase-Write, Retention and Endurance measurements. The entire instrumentation may be controlled by any computer with an IEEE-488 bus access. The setup can be used to test other types of semiconductor memories and even arrays with minor modifications.

This test station requires the user only to input the test vectors. Even the instrument calibrations, previously done manually, are performed by the computer according to the test vectors. This system offers a constant viewing of the device's condition during testing. The automated gated measurements on windowed regions of the waveform and the averaging of measurements on several acquisitions increase

the accuracy of the measurements. This system is cost-effective for a small Research and Development environment. The setup has been used to study the reliability of SONOS devices and compare two different processing techniques.

# Chapter 1

# Introduction

## 1.1 Historical Background

An established method of achieving nonvolatile memory is by effecting charge storage in the traps at the interface of a multilayer insulator or in the insulator itself. This interesting approach has been utilized successfully to instill memory properties in some MIS (Metal-Insulator-Semiconductor) structures as shown in Fig.1.1, namely, MNOS (Metal-Nitride-Oxide-Silicon) and MONOS (Metal-Oxide-Nitride-Oxide-Silicon) devices.

The use of Silicon Nitride in Microelectronics evolved from its usage in regular MOSFET processing technology as a masking layer during various processing steps and it also passivates the silicon surface. Researchers knew for a long time of the high trap density of nitride which could be used to store charge. The MNOS device structure [1, 2, 3], proposed by Kahng and Sze in 1967, trap both electrons and holes which tunnel through the thin tunneling oxide under applied bias in the trap rich nitride layer. This alters the threshold voltage of the transistor. Reviews of the historical developments of the MNOS memory devices have been presented by Verwey [4], Chang [5], Nishi [6] and Maes et. al. [7]. Transient response characterization of MNOS devices are detailed in the IEEE Standards [8].

Attempts at improving the performance of these devices have led to innovations in the processing technology. The electric field in the tunneling oxide determines the tunneling probability of the carriers from the silicon to the nitride. For efficient

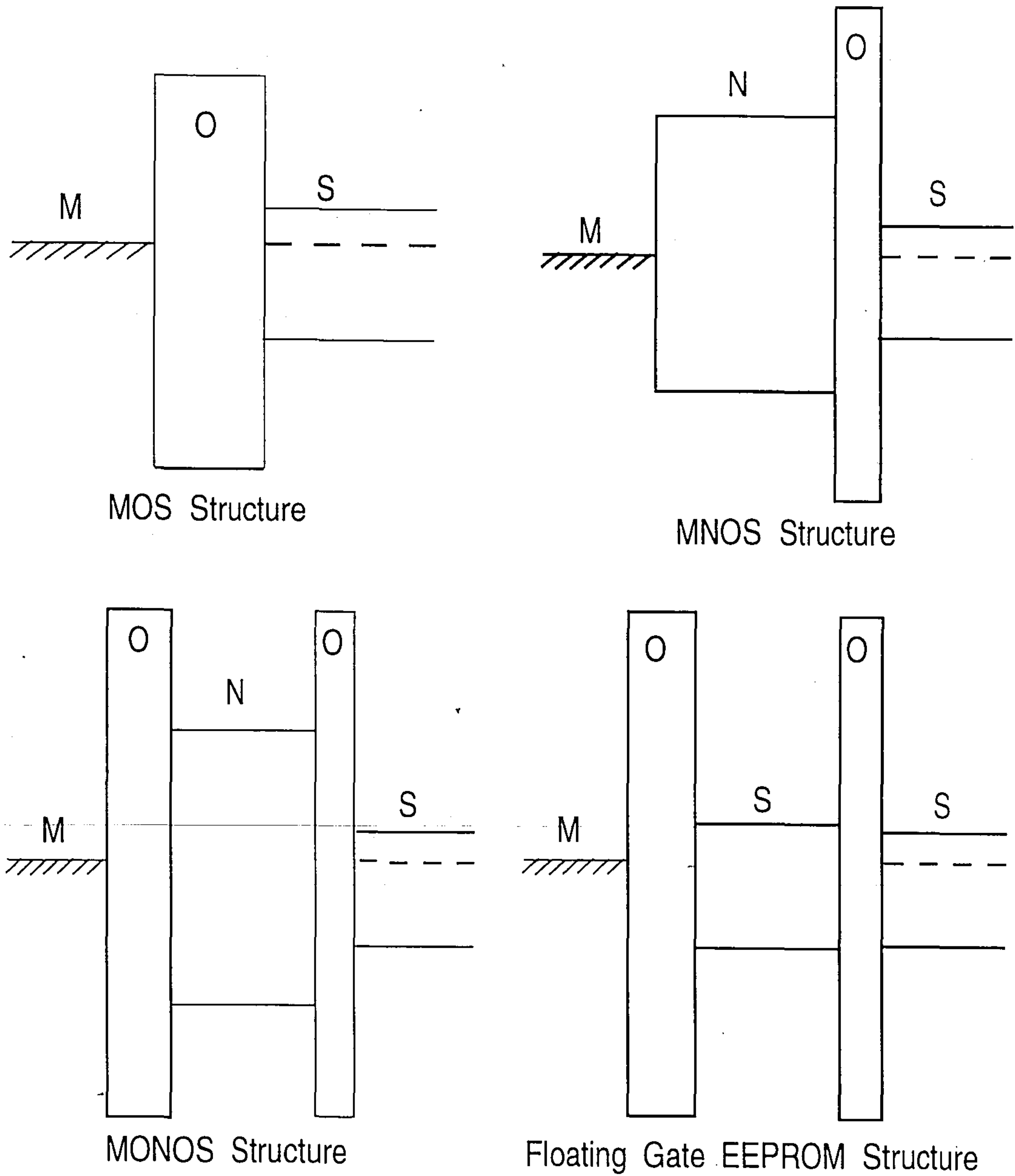


Figure 1.1: Energy Band Diagram of some MIS devices

low voltage programming, the oxide has to be thin, but still thick enough to prevent back- tunneling. This enables faster programming speeds by reducing erase and write times. However, retention of the trapped charge diminishes.

Dennard, in his constant electric field principle [9], proposed scaling all dimensions, vertical as well as horizontal, by a common factor. The applied voltages are reduced as well to maintain the electric field. Obviously, better packing density as well as lower power consumption is achieved. Since the tunneling oxide cannot be scaled down much, it is the nitride layer is the one to be scaled. Hampton and Cricchi [10] have estimated the lower limit to conform to twice the hole nitride charge centroid as 190Å. Subsequent scaling causes loss of charge to the gate electrode.

Chen [11] introduced the SONOS structure, where a blocking oxide was grown by steaming the nitride before metallization. This allowed further scaling of the nitride without the risk of injection into the nitride from the gate. Reduced gate injection leads to a wider memory window and better retention. The nitride-blocking oxide traps add to the charge trapping sites. Suzuki et. al. [12] announced a low voltage programmable SONOS device after major effort at scaling the gate dielectric layers in 1983.

Chen [11] used a programming voltage of 25V (30Å tunneling oxide, 400Å nitride, 150Å blocking oxide). Suzuki [12] programmed with only 6V (22Å tunneling oxide, 30Å nitride and 33Å blocking oxide). Chao's [13] (20Å tunneling oxide, 85Å nitride and 51Å blocking oxide) programming voltage was 8V.

## 1.2 Testing of Memory Devices

With the advent of the semiconductor memory disc, researchers have worked with various technologies. There is considerable interest in the SONOS technology to achieve this goal and also to successfully design and fabricate a low voltage

programmable EEPROM. The SONOS technology has shown great promise with low programming voltages and high endurance and reliability. A major proponent of this technology, the Microelectronics Research Center of the Sherman Fairchild Laboratory, has been the site of remarkable progress in SONOS fabrication technology. The industry is showing an ever increasing interest as this technology becomes commercially viable.

The need for a completely automated test station for the measurement of parameters of nonvolatile memory elements becomes more acute as new devices are proposed and processed. However, the testing is a tedious, time consuming process. This places severe limitations on laboratory research of such devices. Furthermore, to be accepted for commercial production, exhaustive tests must be carried out to simulate field conditions and usage.

The standard memory operations are Write, Erase, Read, Retention and Inhibit operations. To improve the memory design, arrays have to be laid out using different configurations of the peripheral circuitry, each suited for the memory device being used. The design rules for CMOS circuits have already been developed by repeated tests and experience as CMOS applications have increased rapidly over the years. Thus, the behavior of the array with the operations under different biases are predictable and can be simulated very closely to real results using commercially available software packages. Thus, a major area left for improvement is the memory device itself.

To achieve a low voltage programmable EEPROM, the memory properties of a wide variety of devices have been investigated (e.g. Floating Gate [14], Ferroelectric [14], MNOS/SONOS [15, 16, 17]. To select the most efficient design, the memory device has to be subjected to a battery of tests in order to predict device behavior in an array. The tests should reflect the biases and currents, even transients at worst possible cases, in an array.

A previous station [18] employed a pattern generator which was programmed with test patterns and delays to control the switches on the write/erase and retention circuit. The pattern generator was programmed with a small AIM-65 computer with a line display unit. The user had to wait for the TEK7854 oscilloscope to trigger to each read pulse, position the cursors and judge the time to read the output response. The data was recorded manually. Data had to be manually entered again to obtain plots and decipher the device behavior. The device suffered excessive cycling during this process. This prevented the extensive testing of many devices and increased the probability of human error. The pattern generator had to be started and reset by the operator for each measurement. The variation of a single parameter to obtain a complete curve required resetting the pattern generator, re-editing the input data and running the program again. This was followed by starting the pattern generator, waiting for the oscilloscope to trigger, positioning the cursors and recording the measurements. To take multiple measurements, the operator had to repeat these procedures numerous times.

It was apparent this testing methodology required a very long time to completely characterize a batch of wafers from one process run, not to mention the tediousness of the procedure. The chance a valuable recommendation would be offered to improve the process would come too late. This also lead to conclusions being based on a limited number of tests conducted on a small number of devices per wafer in each run. It became highly impractical to standardize the process steps depending on such measurement capabilities. Hence, the motivation for an integrated test station with only one controller was apparent.

## 1.3 Scope of Thesis

The automated system discussed in this thesis allows the operator to enter the patterns and delays on a menu driven screen using specially programmed function

keys. The instruments are controlled by the IEEE488 bus and can be accessed by any computer with an IEEE488 bus controller attachment. To obtain Erase/Write curves, the Erase (Write) time delay can be varied and a number of readings are taken for each setting. The oscilloscope adjusts its settings and takes averaged measurements. Retention measurements are done very effectively to support reliability models. Endurance tests offer a constant viewing of the device's condition at any time and prints out the threshold as cycling goes on.

Another major advantage is the cost effectiveness. A similar system procured as a component assembly will cost quite a few times more than the in house developed setup. This system is very flexible and can be modified as and when required to lend automation to other testing procedures.

The second chapter presents an insight into the operations of a SONOS device as a memory element and explains the Erase/Write characteristics with a simple analytical closed form model. The retention curve is explained in terms of charge leakages. The third chapter briefly compares the various measurement techniques used to characterize SONOS devices as well as the Erase/Write setup used previously. The salient features of the new automated test station is discussed and the individual components are presented in detail. The experimental data recorded using this setup is shown in the fourth chapter with particular emphasis on the reliability of devices with oxides grown in a triple wall oxidation furnace and a conventional single wall oxidation furnace. Finally, the concluding remarks are made in the fifth chapter to summarize this thesis and suggestions made for future work. The fabrication technology used to make the SONOS devices is shown in the appendix with figures depicting the effect of each process step. An instruction manual for the test station as well as the programming algorithm and the pattern generator programming sequence are covered in the second appendix.

# Chapter 2

# The SONOS Memory Device

The SONOS (Polysilicon-Oxide-Nitride-Oxide-Silicon) device is essentially a floating trap field effect device. The threshold voltage in the SONOS device changes due to tunneling of charge through the thin tunneling oxide and getting trapped in the nitride layer[19]. The SONOS structure and the energy band diagram is shown in Figs.2.1 and 2.2. The chief operations on n-channel SONOS devices are described as follows.

**WRITE** A positive voltage is applied to the gate, while the drain and source are grounded, creating an inversion layer. Furthermore, the electric field causes electrons to tunnel through the tunneling oxide into the nitride layer by the Modified Fowler-Nordheim tunneling mechanism. The high trap density in the nitride causes the electrons to trap and shift the threshold voltage in a positive direction and the device is then normally in a low conduction state.

**ERASE** A negative potential is applied to the gate, whereas the drain and source are grounded, and the surface is accumulated. The resultant electric field induces tunneling of holes into the nitride where they recombine with the trapped electrons and shift the threshold voltage of the device in the negative direction.

**READ** A $10\mu A$ current is forced through the drain-source junction and the gate is kept grounded. The gate to source voltage is then measured as the threshold voltage. This is an approximation valid for the small drain-source current.

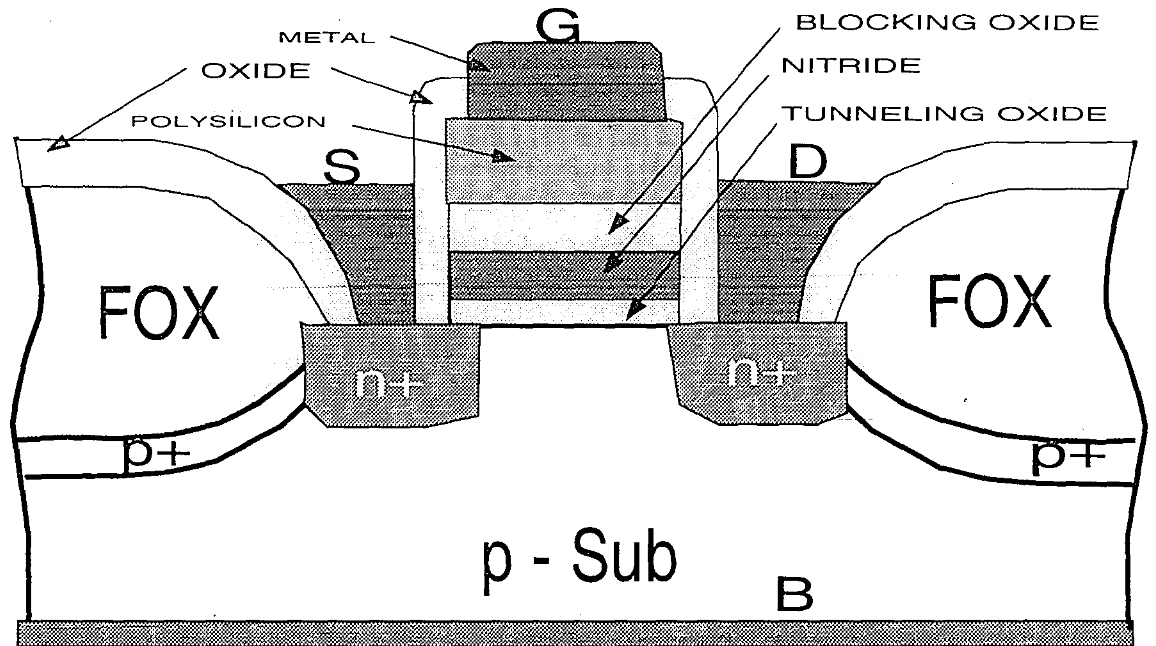


Figure 2.1: The cross-section of the SONOS device

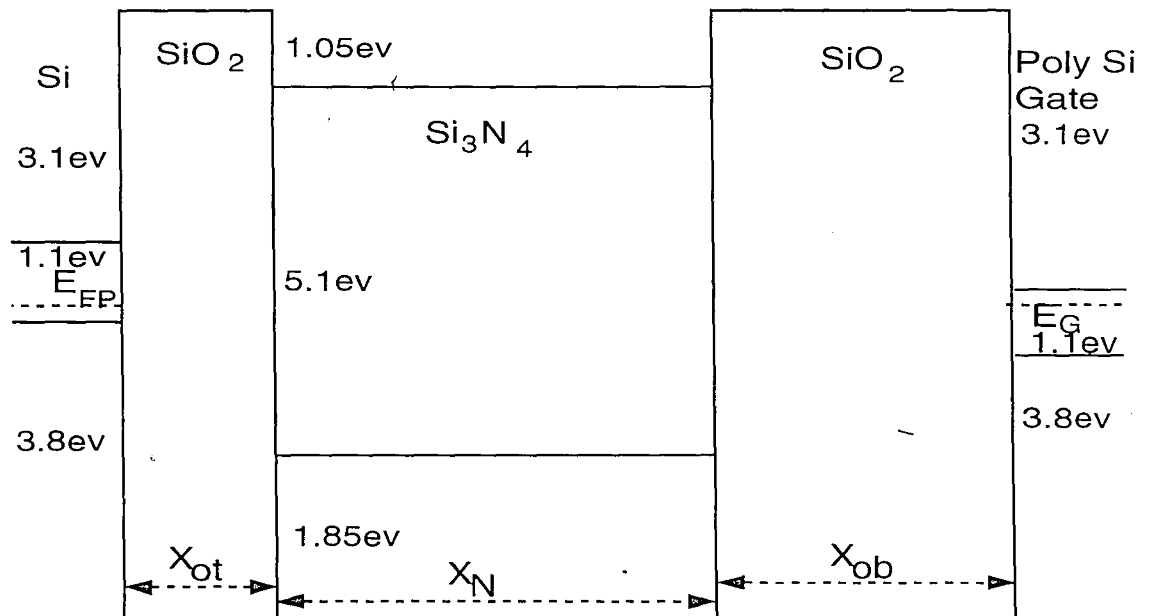


Figure 2.2: The ideal energy band diagram of the SONOS device

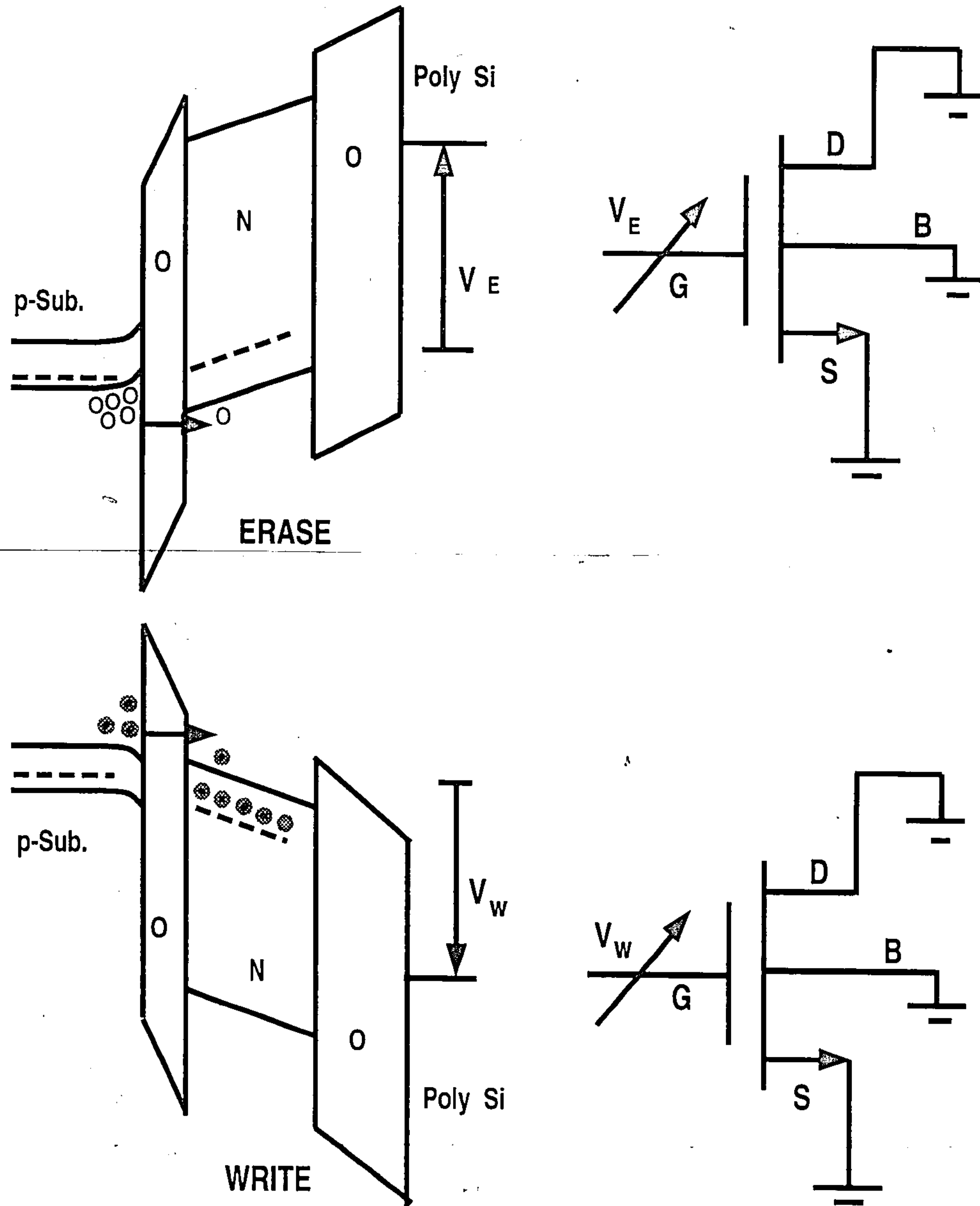


Figure 2.3: The energy band diagram and the circuit equivalent of the SONOS device during Erase and Write operations.

**IDLE** All the transistor terminals are grounded. This is the most likely state during power down condition. The idle condition energy band diagram differs with the trapped charge in the nitride layer.

## 2.1 Closed Form Erase/Write Model

This approach, despite being simple, provides a basic insight into the physical processes involved in device operation. Making the following assumptions, the model is derived.

- The traps are assumed to be located in the middle of the nitride region in the form of a sheet charge at the charge centroid.
- For the derivation of equations governing the writing of an n-channel device, the carriers being trapped in the nitride layer are considered to be only electrons. Hence, the total charge in the nitride layer, $Q_N$ is negative.
- No charge trapping occurs at the oxide-nitride interfaces.
- No current flows through the blocking oxide.

$x_N$ is the thickness of the nitride layer and $N_T$ the area trap density in the nitride layer. This gives $Q_N = -qN_T x_N$.

The continuity of the electric displacements fields over the stacked layers is maintained and this condition provides the essential boundary conditions. At the interface between the tunneling oxide and nitride layer, equating the displacements show

$$E_{ot}\epsilon_{ot} = E_{N1}\epsilon_N \tag{2.1}$$

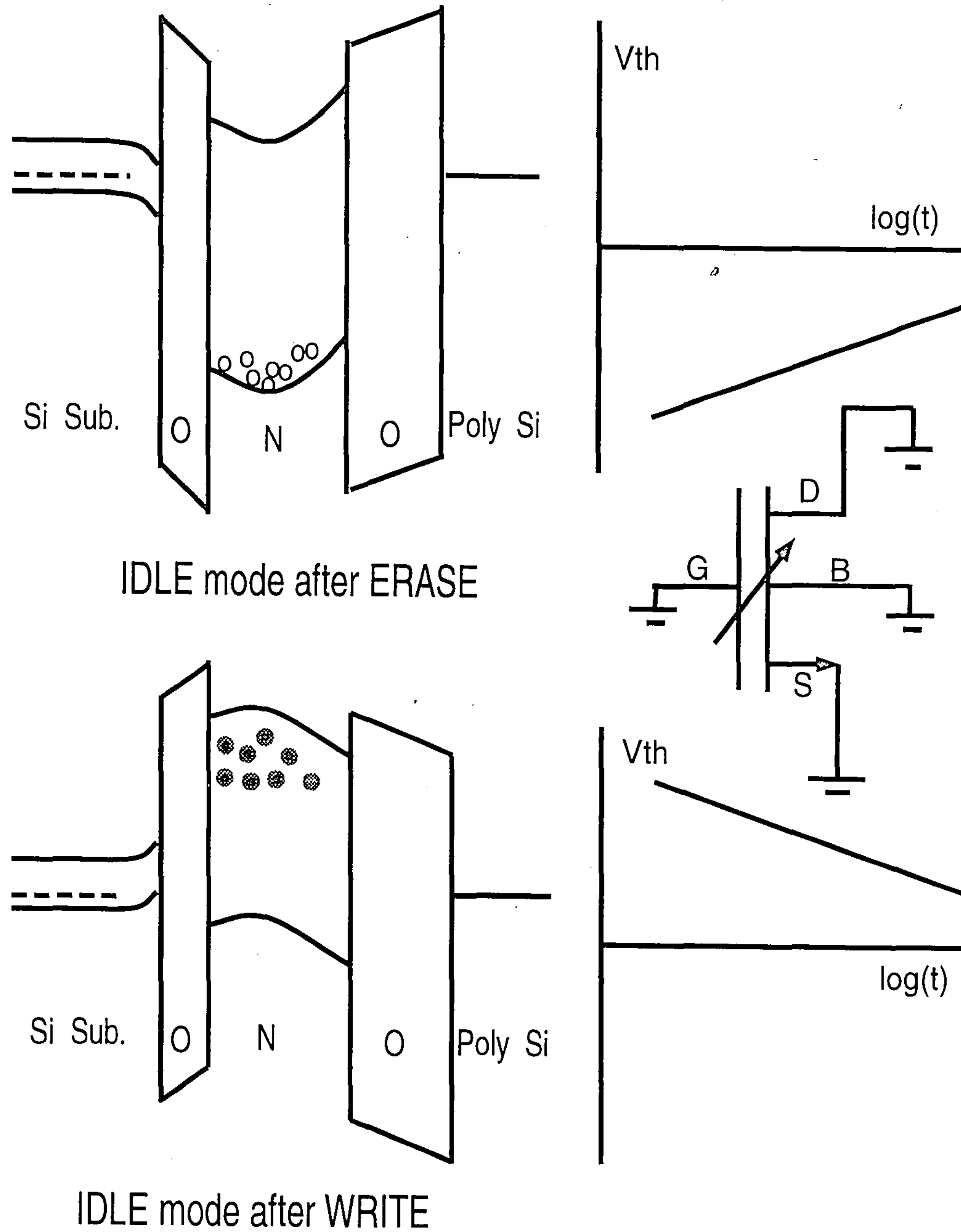


Figure 2.4: Notice the difference in the energy band diagram in Idle mode depending on the last operation, Erase or Write.

where E is the electric field and the subscript "ot" relates to the tunneling oxide, "ob" to the blocking oxide and "N" to the nitride. $\epsilon$ is the permittivity of the material. At the nitride and the blocking oxide interface,

$$E_{ob}\epsilon_{ob} = E_{N2}\epsilon_N \tag{2.2}$$

Poisson's equation in the nitride shows

$$E_{N2} = E_{N1} - \frac{Q_N}{\epsilon_N} \tag{2.3}$$

These expressions relate the quantities $E_{N1}, E_{N2}, E_{ob}, E_{ot}$. $\phi_{ms}$ and $\phi_s$ are the work functions of the gate metal and the semiconductor. Expressing the gate to bulk voltage in terms of the voltages across the oxide and nitride and the work functions,

$$V_{GB} = V_{ot} + V_{ob} + V_N + \phi_{ms} + \phi_s \tag{2.4}$$

We substitute the voltages in terms of the field and thickness of the layers to write

$$V_{GB} = x_{ot}E_{ot} + x_{ob}E_{ob} + \frac{x_N}{2}(E_{N1} + E_{N2}) + \phi_{ms} + \phi_s \tag{2.5}$$

Rearranging after using further substitution from the previous equations, $V_{GB}$ can be expressed as

$$V_{GB} = V_{ot}[1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N\epsilon_{ox}}{x_{ot}\epsilon_N}] - \frac{Q_N}{\epsilon_N}[\frac{x_{ob}\epsilon_N}{\epsilon_{ox}} + \frac{x_N}{2}] + \phi_{ms} + \phi_s \tag{2.6}$$

For a constant gate voltage, upon time differentiation

$$\frac{dV_{GB}}{dt} = 0 \tag{2.7}$$

Neglecting blocking oxide leakage current and solving for $dQ_N/dt$

$$\frac{dQ_N}{dt} = -J_0(V_{ot}) = \frac{[1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N\epsilon_{ox}}{x_{ot}\epsilon_N}]\epsilon_{ox}}{[\frac{x_{ob}\epsilon_N}{\epsilon_{ox}} + \frac{x_N}{2}]}\frac{dV_{ot}}{dt} \tag{2.8}$$

This expression represents the time rate of change of charge in the nitride layer. We can develop another expression for this current in terms of the tunneling mechanisms involved. There are several competing tunneling mechanisms that affect the charge in the nitride (through the thin tunnel oxide). The dominant mechanism is determined by the thickness of the tunneling layer and the applied electric field. The Fowler Nordheim tunneling current [20] causes the electrons in the inversion layer to tunnel through the tunneling oxide. The tunneling current expression shows the dependence on the electric field across the layer and the potential barrier.

$$J_{FN} = \frac{q^2}{8\pi h\phi_B} E_{ot}^2 \exp[-\frac{8\pi\sqrt{2m^*q}}{3hE_{ot}}\phi_B^{\frac{3}{2}}] \tag{2.9}$$

where $\phi_B = \phi_m - \chi_{ox}$ is the barrier height. We define the characteristic voltage, $V_T$ as

$$V_T = \frac{8\pi\sqrt{2m^*q}}{3h}\phi_B^{\frac{3}{2}} x_{ot} \tag{2.10}$$

and

$$J_T = \frac{q^2}{8\pi h\phi_B}(V_T/x_{ot})^2 \tag{2.11}$$

Rewriting the tunneling current expression

$$J_{FN} = J_T(V_{ot}/V_T)^2 e^{(-V_{ot}/V_T)} \tag{2.12}$$

We now equate $J_{FN}$ to $J_o$ as per our assumption that the Fowler-Nordheim tunneling is dominant and causes the change in nitride charge. On integrating both sides, we obtain

$$\int_{(V_{ot}(0)/V_T)}^{(V_{ot}(t)/V_T)} \frac{dV_{ot}}{V_T}(\frac{V_{ot}}{V_T})^{-2} e^{(V_T/V_{ot})} = \int_0^t \frac{J_T(x_{ob} + \frac{\epsilon_{ox}x_N}{2\epsilon_N})}{V_T\epsilon_{ox}[1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N\epsilon_{ox}}{x_{ot}\epsilon_N}]} dt \tag{2.13}$$

$$-\left[\exp(-V_{ot}(0)/V_T) - \exp(-V_{ot}(t)/V_T)\right] = t/\tau \tag{2.14}$$

where $\tau$ is the time constant

$$\tau = \frac{V_T \epsilon_{ox}[1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N \epsilon_{ox}}{x_{ot}\epsilon_N}]}{J_T(x_{ob} + \frac{\epsilon_{ox} x_N}{2\epsilon_N})} \tag{2.15}$$

Taking the natural log of the both sides, we have

$$V_{ot}(t) - V_{ot}(0) = V_T \ln[1 + t/\tau_c] \tag{2.16}$$

where,

$$\tau_c = \tau \exp(V_{ot}(0)/V_T) \tag{2.17}$$

$$v_{th} = \phi_{ms} + 2\phi_F + \frac{\sqrt{4\epsilon_s q N_B \phi_F}}{C_{eff}} - \frac{Q_F}{C_{eff}} - (x_{ob} + \frac{x_N \epsilon_{ox}}{2\epsilon_N})\frac{Q_N}{\epsilon_{ox}} \tag{2.18}$$

We define,

$$\Delta V_{th} = V_{th}(t) - V_{th}(0) \tag{2.19}$$

$$= -\frac{1}{\epsilon ox}[x_{ob} + \frac{x_N \epsilon_{ox}}{2\epsilon_N}][Q_n(t) - Q_n(0)] \tag{2.20}$$

$$= -[1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N \epsilon_{ox}}{x_{ot}\epsilon_N}][V_{th}(t) - V_{th}(0)] \tag{2.21}$$

Substituting gives

$$\Delta V_{th} = V_T \ln[1 + \frac{t}{\tau_c}][1 + \frac{x_{ob}}{x_{ot}} + \frac{x_N \epsilon_{ox}}{x_{ot}\epsilon_N}] \tag{2.22}$$

$$= [\frac{1}{C_{ot}} + \frac{1}{C_{ob}} + \frac{1}{C_N}] C_{ot} V_T \ln[1 + \frac{t}{\tau_c}] \tag{2.23}$$

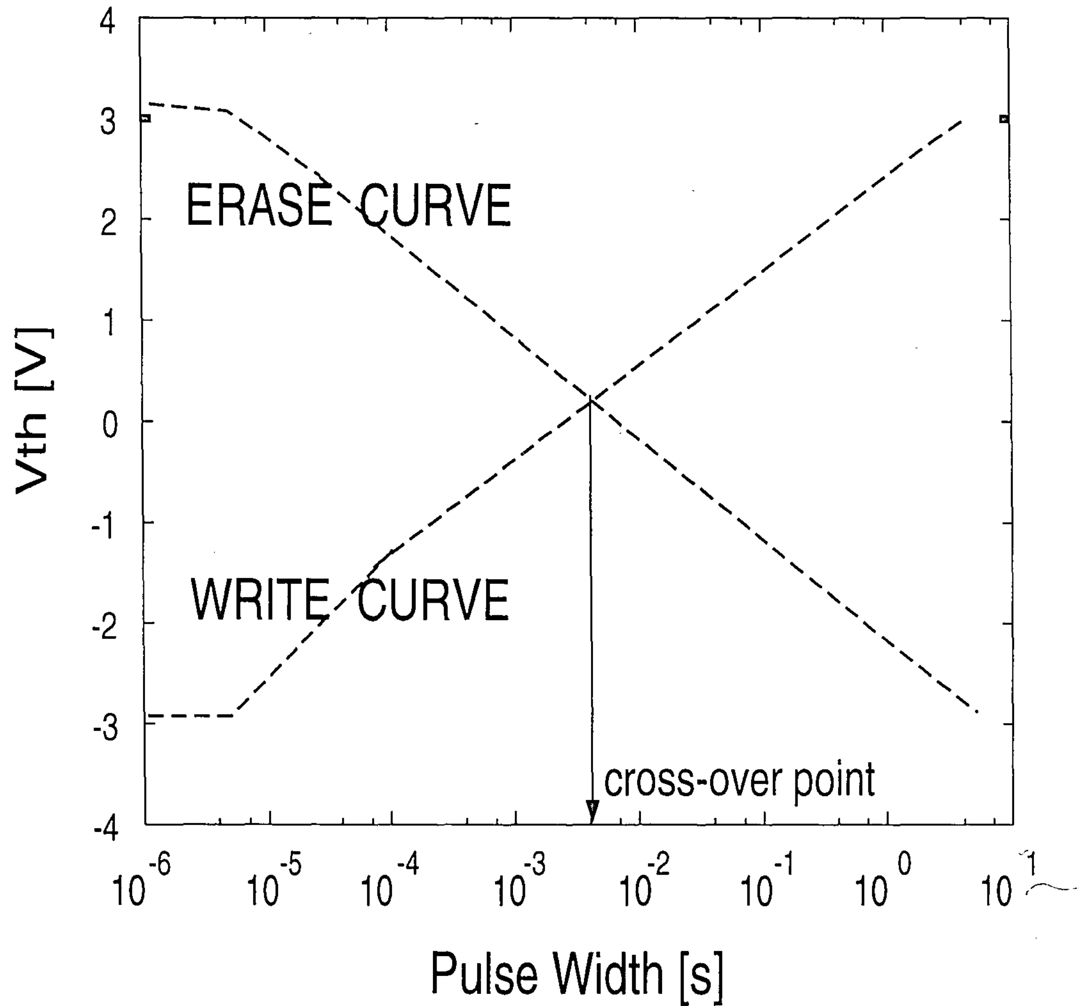


Figure 2.5: The curves show the shape of typical Erase/Write curves for an n-channel SONOS device. The cross-over time between the Erase and Write curves provides a measure of the programming speed of the device for a certain programming voltage.

The above equations depict the threshold voltage shift resulting from an erase or write operation. The tunneling of the carriers to the nitride is dependent upon the effective electric field seen across the tunneling oxide. The magnitude of this field is proportional to the programming voltage and the ratio of the tunneling oxide capacitance to the total effective capacitance of the gate dielectric. This term is scaled by a logarithmic dependence on the tunneling time constant. The shift in the threshold is visible only when the programming time exceeds the tunneling time constant. Once the programming pulse exceeds this time constant, the threshold shift varies logarithmically with time (or linearly when time is plotted on a logarithmic scale). This dependence, when sketched in the Fig.2.5 is comparable with the experimental results in chapter 4.

## 2.2 Retention Model

The following model of the threshold voltage decay is based on the assumption of an amphoteric trap model [21]. This model takes into account the loss of the trapped charge from the nitride due to

- electron charge tunneling from the nitride traps to the Si conduction band with a time constant of $\tau_{T-B}$,
- electron charge tunneling from the nitride traps to the Si/$SiO_2$ interface traps with a time constant of $\tau_{T-T}$
- and hole injection from the Si valence band to the nitride taps with a time constant of $\tau_{B-T}$.

The time constants are functions of the tunneling oxide thickness ($x_{ot}$), and the barrier height for the particular carrier.

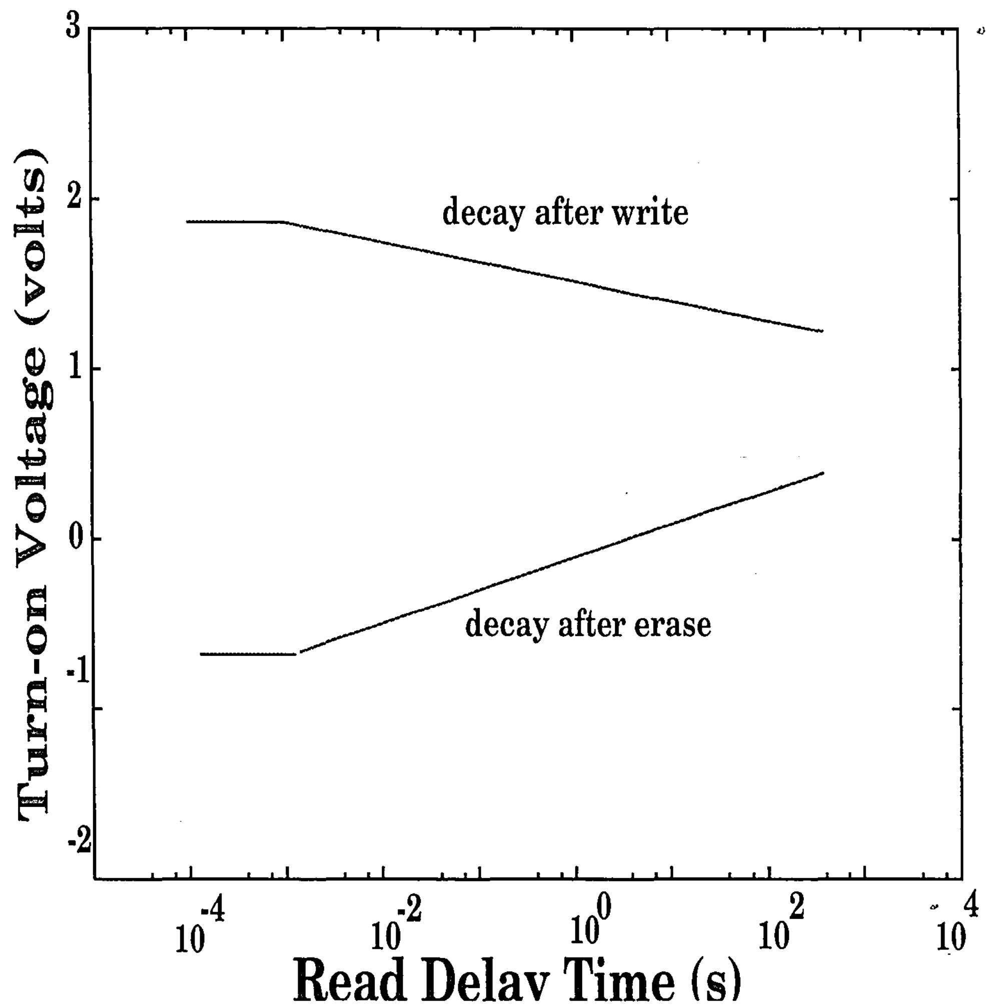


Figure 2.6: A typical retention curve shows the decay in threshold voltage of a device with time. Notice the difference in the rate of decay after the Write and the Erase states.

$$\begin{aligned}\Delta V_{th}(t) &= -qN_T \int_0^{x_n} \left( \frac{x_n - x}{\epsilon_n} + \frac{x_{ob}}{\epsilon_{ox}} \right) \\ &* \left[1 - m(x)(exp(-\frac{t}{\tau_{T-T}} + \frac{t}{\tau_{B-T}}) - exp(-\frac{t}{\tau_{T-B}})) \right. \\ &- \left. 2exp(-\frac{t}{\tau_{T-B}})\right]dx \end{aligned} \tag{2.24}$$

$$m(x) = \frac{1}{1 - \frac{e_n^0(x)+c_p^0(x)}{e_n^-(x)}} \tag{2.25}$$

$e_n^0(x)$, $e_n^-$ and $c_p^0$ are emission and capture coefficients for electrons and holes of the neutral state in the trap model. $N_T$ is the number of traps in the nitride layer. The shape of the curve showing the decay of the threshold voltage after programming the device is shown in Fig.2.6. For the retention measurements in the write state the device is Erased untill saturation and then Written for a fixed time to allow a memory window of more than a volt. The threshold voltage or the turn on voltage in this case is read after the time delay.

# Chapter 3

# Automated Tests and Measurement

## 3.1 Dynamic Characterization of memory transistors

The characterization should include the measurements exercising the standard modes of operation (erase-write-read-idle) of a memory transistor in an array.

- Erase-Write : This yields the knowledge of a device's programming ability at different programming voltages and the time taken to do so.

- Retention : This indicates the time for which the stored word will be distinguishable.

- Endurance : This gives the result of repetitive cycling effects as the electric fields are reversed in each cycle during erase and write operations.

These operations shall essentially require a switching and gating scheme to apply pulses of varying magnitude and time duration to bias the gate, source and drain with respect to the substrate. A current bias is necessary to measure the threshold voltage. These biases and time durations should be programmable.

## 3.2 Test Vehicles in Literature

Since the shift in threshold voltage in SONOS devices is treated as the memory property, some of the methods used to determine this are outlined below:

The capacitive structures also exhibit memory properties and are simpler to fabricate.

- High Frequency C-V : The shifts in the curve, Fig.3.1 depend on the programming. This test is performed easily without specialized instrumentation and has been used widely (Suzuki et. al. [12]). However, it is very slow (read delay $> 100ms$) and does not reflect the actual transient situation.
- Back-tunneling effects in MNOS capacitors were studied by Libsch [22], Roy [23], and Yun [24] using feedback operated flatband and charge monitoring schemes one of which is shown in Fig.3.2. This method is limited only by the settling time of the locking amplifier (1ms) and provides charge transport data.

The testing approaches used to test the transistor structures are enumerated below.

- The I-V method curve be used to see the threshold shift as shown in Fig.3.3. It is also a slow technique and short time retention measurements are not possible. For low voltage programming, state of memory device might be disturbed by applying high fields.
- Perhaps the technique using measurements in the most realistic modes were conducted by White and Cricchi [25]. The schematic is shown in Fig.3.4. The scheme used is referred to by the IEEE Standards as "source follower constant current method of threshold detection". Measurements are very flexible

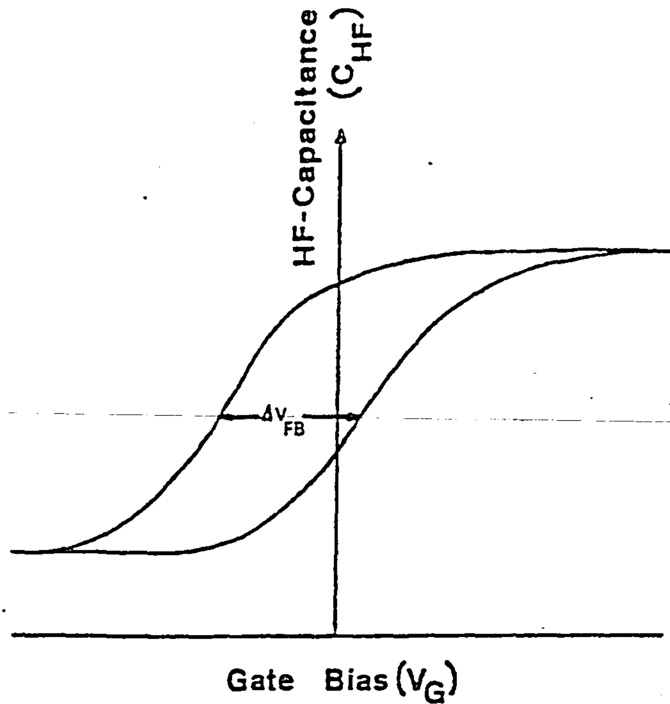


Figure 3.1: Flatband shifts in High Frequency C-V plots depending on the charge stored in the nitride [12].

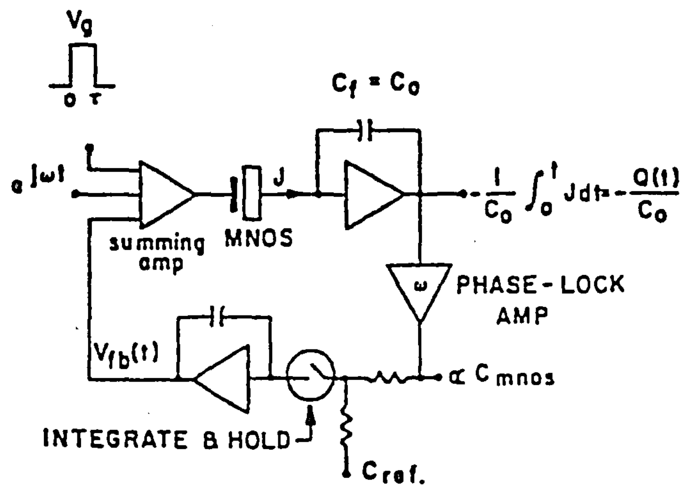


Figure 3.2: Change in flatband voltage is measured by sample and hold [24].

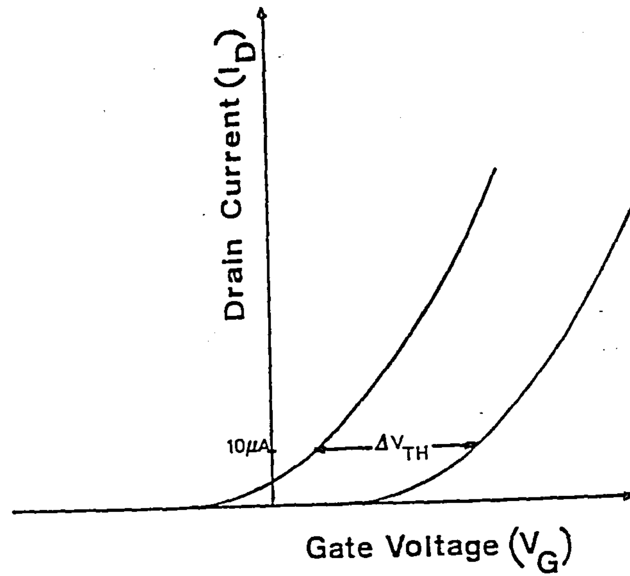


Figure 3.3: Static I-V characteristics are used to determine threshold shift.

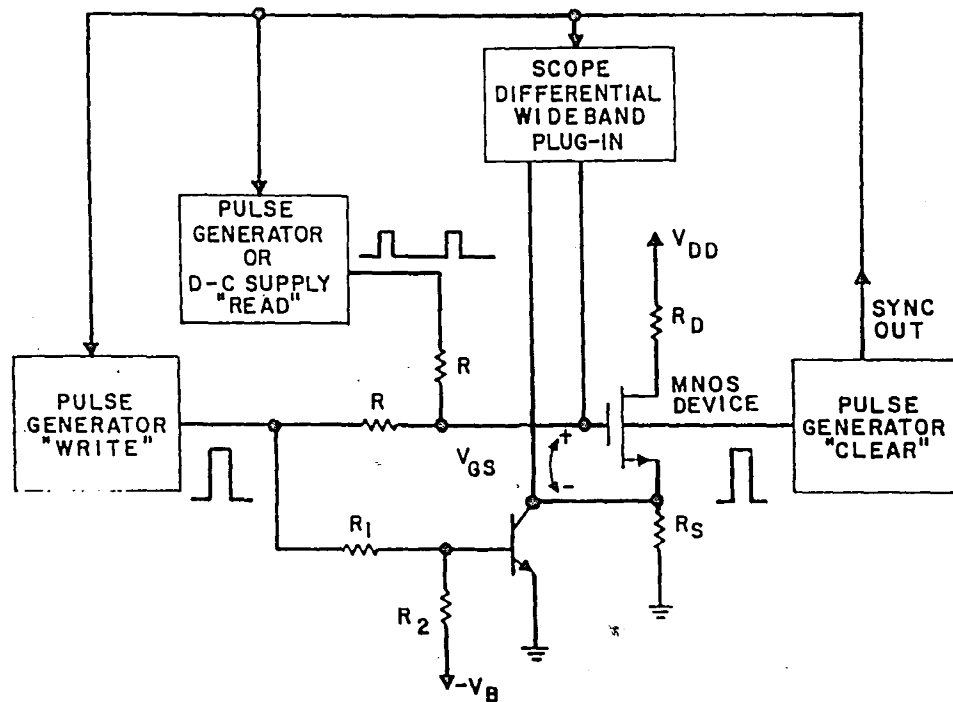


Figure 3.4: The test station for determination of erase/write and storage characteristics used by White and Cricchi. This is in the source follower category of threshold detection schemes [25].

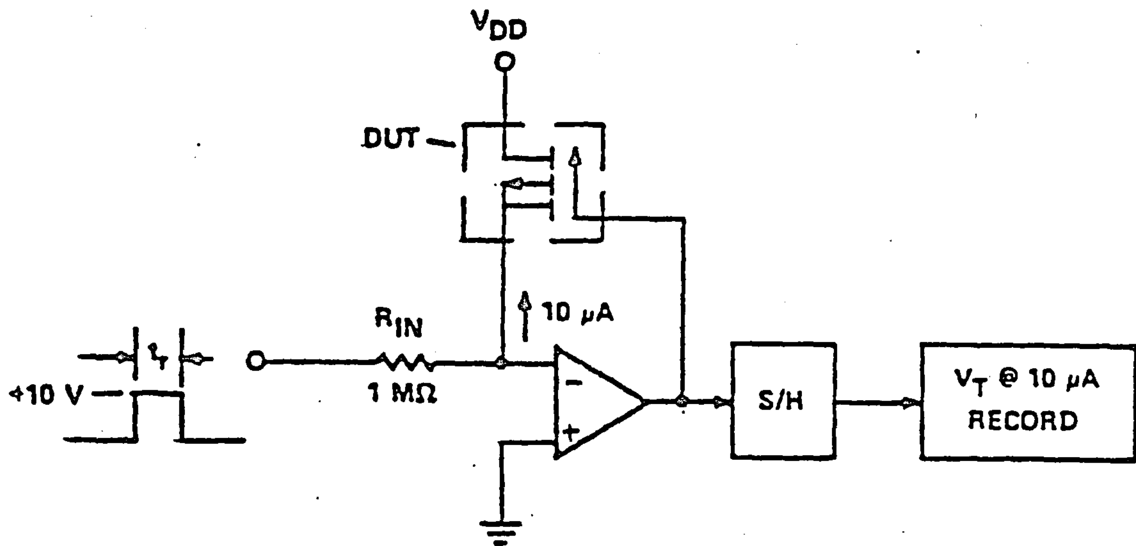


Figure 3.5: Saturated drain constant current method facility [26].

though requiring three pulse generators and being very operator dependent and difficult to coordinate and synchronize. However, the read voltage was fixed which allowed a varying current through the drain-source. The effect of substrate bias was not taken into account.

- An improved version of the "saturated drain current method" was used by Libsch [26]. The read pulse produces a constant current for the transistor and the opamp output settles at the threshold voltage. The sense current, being very small, limits the charging of stray capacitance. The opamp output saturates while doing write-erase and the initiation of the read. Fig.3.5 shows the circuit configuration.

The automated test station simulating the most real life operation of a memory device in an array is discussed with its features and motivations behind adopting the different aspects [27, 28, 29, 18, 30].

## 3.3 The Erase-Write-Read-Idle Circuit

The opamps 3 and 4 in the Fig.3.6 constitute a buffered current source required to force $10\mu$A current through the drain-source junction for reading the threshold voltage. The current sourced is $I = V_{REF}/30k\Omega$. The operational amplifiers 1 and 2 sense the current through the device under test and is used as a proportional feedback element for the voltage reference circuit. The feedback enhances the sourced current to about 10 times and thus charges the stray capacitances much faster. The circuit has been designed to operate the opamps in the linear active region, preventing saturation delays and application of high fields for greater time periods due to the opamp outputs getting saturated. Fast settling MOS analog switches are used for the switches. These switches have very low transmission resistance and very high slew rates. The controls signals of switches are TTL compatible and, hence, are utilized by the output signals of the pattern generator to obtain the various modes of memory operation of the device under test. A 5 volt drain potential is supplied externally and connected to the device through switches.

During Write and Erase operations, the switches SW1 and SW3-1 ground the drain and source of the device. Switch SW2 is used to apply either the Write or Erase programming voltage to the gate of the device. This condition is valid for the duration of the Write or Erase delay timing. In the Read mode, the gate is grounded and the source voltage adjusts to a value to support the $10\mu$A current. The negative of the source-drain voltage is the threshold potential of the device. Thus, the oscilloscope is used to monitor the source potential during the Read mode. The current source is bidirectional with high output impedance and sustains a bipolar output voltage. The read-delay is typically a few microseconds. Despite the fast settling times of the opamps used, the feedback settling time, charging of parasitic capacitances and switching of the analog switches account for the read delay. The equivalent circuit in the various modes of operation is shown in Fig.3.3. Care has been taken to keep the rise and fall times of the pulse being applied to the gate to be

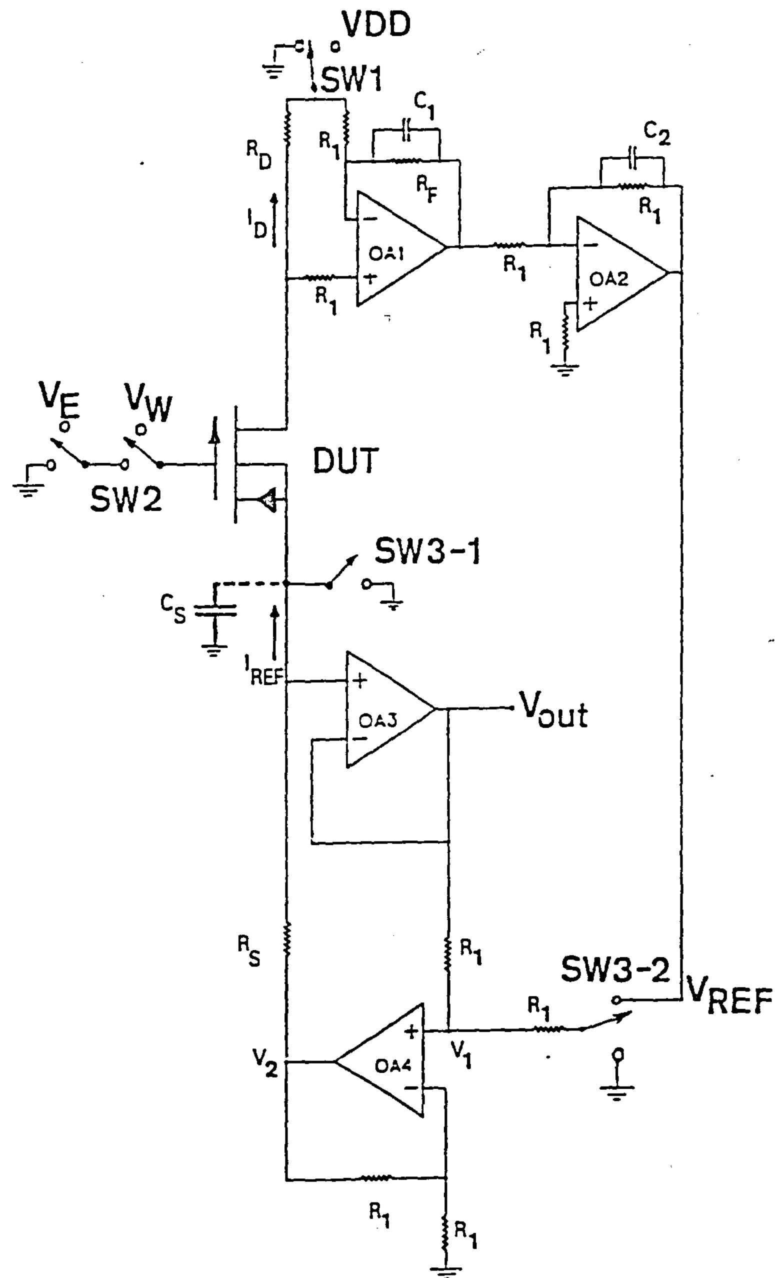


Figure 3.6: The Erase/Write/Read Circuit [27,18].

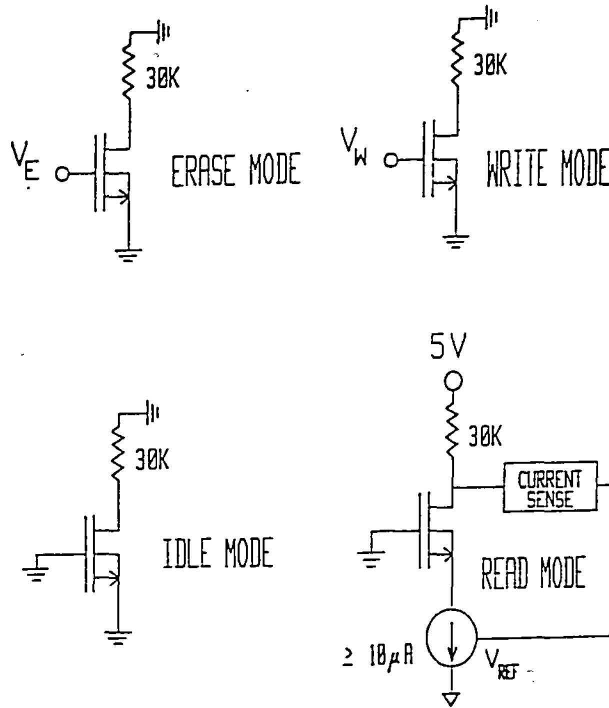


Figure 3.7: Representation of the Erase-Write-Read circuit during the different modes of operation of the device under test.

lower than $10^8$ Volts/second. This reduces possibility of high displacement currents altering the programmed status of the device.

## 3.4 Pattern Generator

hspace*.25in The pattern generator is a 8 channel synchronous, 10MHz, single board digital stimuli generator. The programming is done using a parallel TTL compatible port. A "sequence" denotes the assignment of a string of logic states for a distinct time period. The status of the output lines is called a "pattern" and the time for it is output is the "delay". The block diagram of the pattern generator is shown in Fig.3.8.

The pattern generator has two input ports of 8 bits each and a 8 bit output port.

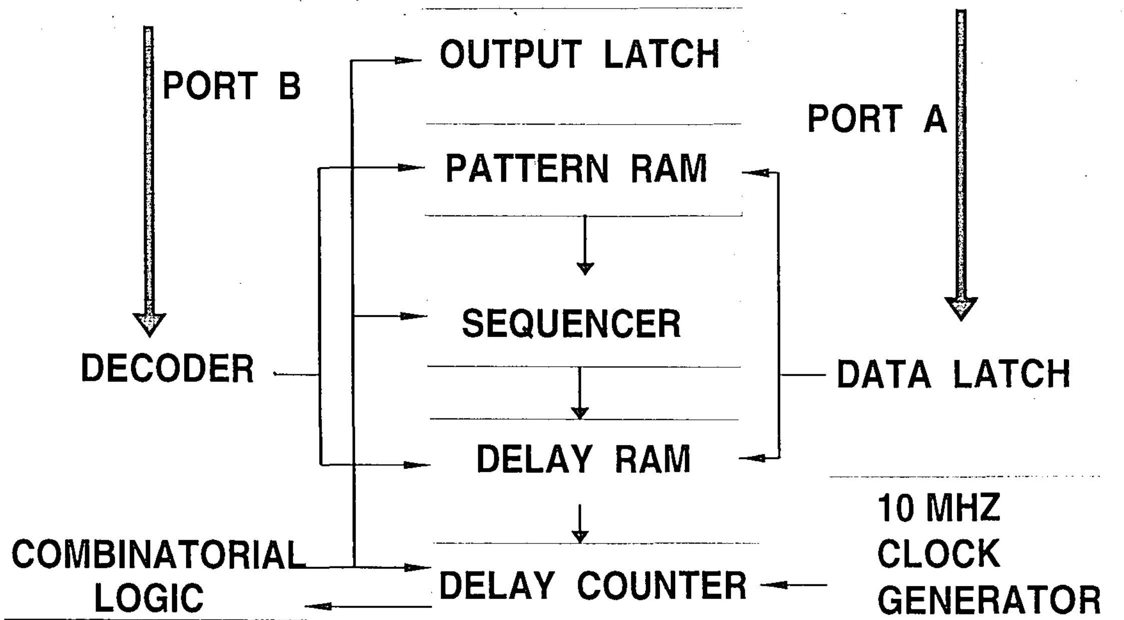


Figure 3.8: Block diagram of the Pattern Generator

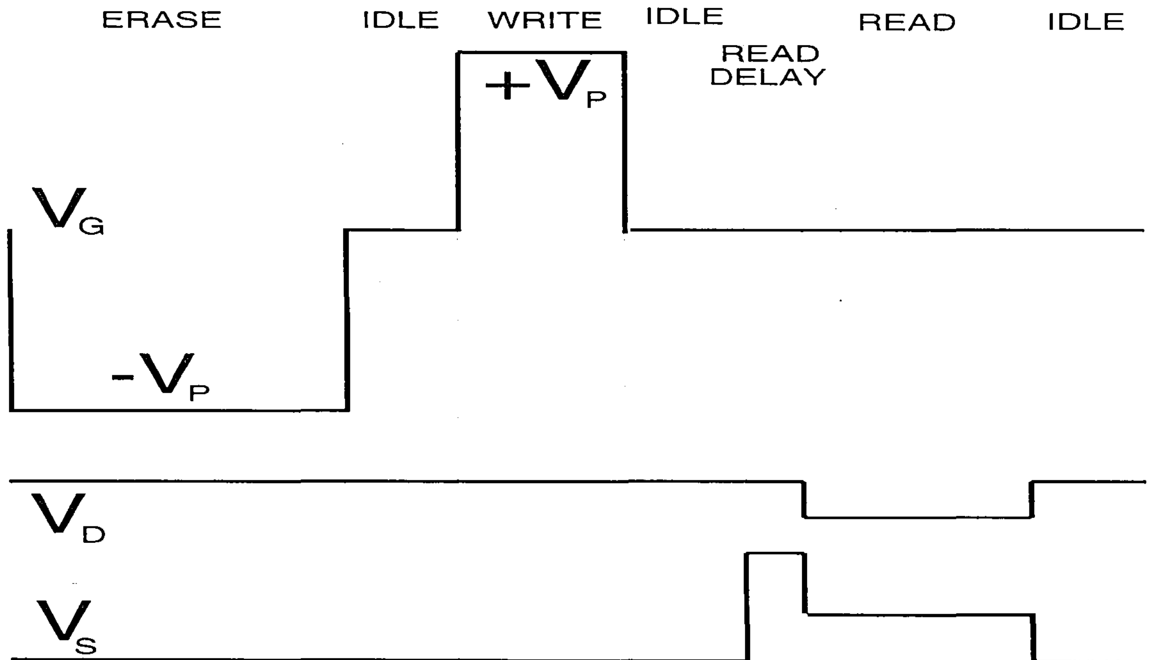


Figure 3.9: The pulse sequence applied to the terminals of the device under test at the various modes of operation.

It is controlled by a computer to program its words and timings. It is initially put in "reset" mode, clearing the output and disabling the internal clock. The computer transfers the patterns and delays in the respective RAMs. The design provides independence from the speed of data transfer. The address of the memory location to be programmed is obtained from the sequencer. The RAMs are in the write mode only during data transfer.

When a sequence of pattern and delay is to be executed, the generator is started and the 10MHz clock drives the count down of the delay loaded from the Delay RAM into a 12 decade ripple Delay Counter. The Sequencer senses the ripple out of the Delay Counter and advances to the next item in the sequence. The pattern from the Pattern Ram gets reflected at the output of the Output Latch. The sequence repeats itself after the expiration of the last delay, providing the option of repetitive sampling and W/E cycling of the memory devices. Fig.3.4 shows the voltages applied to terminals of the device at the time intervals.

## 3.5 Motivation for Adopting HPIB

Programs have already been developed for most data acquisition and parameter extraction routines used in the laboratory. The nonvolatile memory measurement program (software) can also be easily integrated into the existing routines. Thus it is desirable to have all instruments comply to the same standard. Most of the instruments used in the Microelectronics Research Laboratory are from Hewlett Packard and follow the Hewlett Packard Interface Bus (HPIB) system. The HPIB is a byte serial 8-bit parallel bus and is generally used to interface and control various instrument systems. It is consistent with the IEEE-488 with all Electrical, Mechanical and Functional specifications. The key specifications of the HPIB are enumerated below:

1. Supports up to 15 interconnected devices on one contiguous bus.
2. The network may be star or linear up to 20m of total transmission path length.
3. Byte-serial, bit parallel, asynchronous data transfer using interlocking 3-wire handshaking technique.
4. 250 to 500K baud is typical. However, this may be increased to 1M baud.
5. Primary address- 31 talk and 31 listen. Secondary address (using 2byte address)- 961 talk and 961 listen. However, on a single bus there can be only one talker and 14 listeners.
6. In multiple controller systems, only one can be active at a time. However, the system controller can assume control at any time.
7. The driver and receiver circuits are Schottky compatible.

## 3.6 HPIB Interface

To develop the pattern generator as a HPIB interfaceable system, a listener box had to be built which would listen to the HPIB controller through the HPIB bus and feed the two 8 bit words into the two ports of the pattern generator. One word is the control word which specifies the operation to be done on the other word; to store it as a pattern or a delay in addressed locations in the respective RAMs. The listener box consists of two identical boards connected to the HPIB bus but have different addresses which are set by the address switches mounted on these boards. These boards service the two ports of the pattern generator at their output. HPIB is low-true logic with positive polarity. There are 8 data lines or addresses lines, 3 hand shaking lines (DAV, NRFD, NDAC), and the ATN, IFC, EOI, SRQ and REN signals. The handshaking and signal lines are in twisted pairs with one wire to be grounded at the termination point. The description given of the HPIB interface

system and the circuit herein will be limited to the listener facility tailored to the specified requirements.

## 3.7 Signal Lines

- **Data Lines (D1 to D7)**: These data lines are gated through Schmitt inverters to reduce noise. These bidirectional lines carry TTL compatible signals and are used to send data and addresses as well.

- **ATN**: Attention line is used to distinguish between COMMAND mode and DATA mode in HPIB. When true, it causes all devices to interpret data on the bus as a controller command and activate their acceptor handshake function (controller mode) or data between addressed devices (data mode).

- **IFC**: Interface Clear initializes the HPIB system to an idle state.

- **DAV**: Data Valid indicates the condition of the information on the data lines. It is driven low by the source when the data is settled and valid and NRFD high has been sensed.

- **NRFD**: Not ready for data is used to indicate the condition of the readiness of the device to accept data. Acceptor sets its NRFD low to indicate it is not ready to accept data and releases it when ready.

- **NDAC**: Not Data Accepted shows the condition of acceptance of data by the device. The acceptor will set its NDAC low when it has not accepted data and will set it high when it has done so.

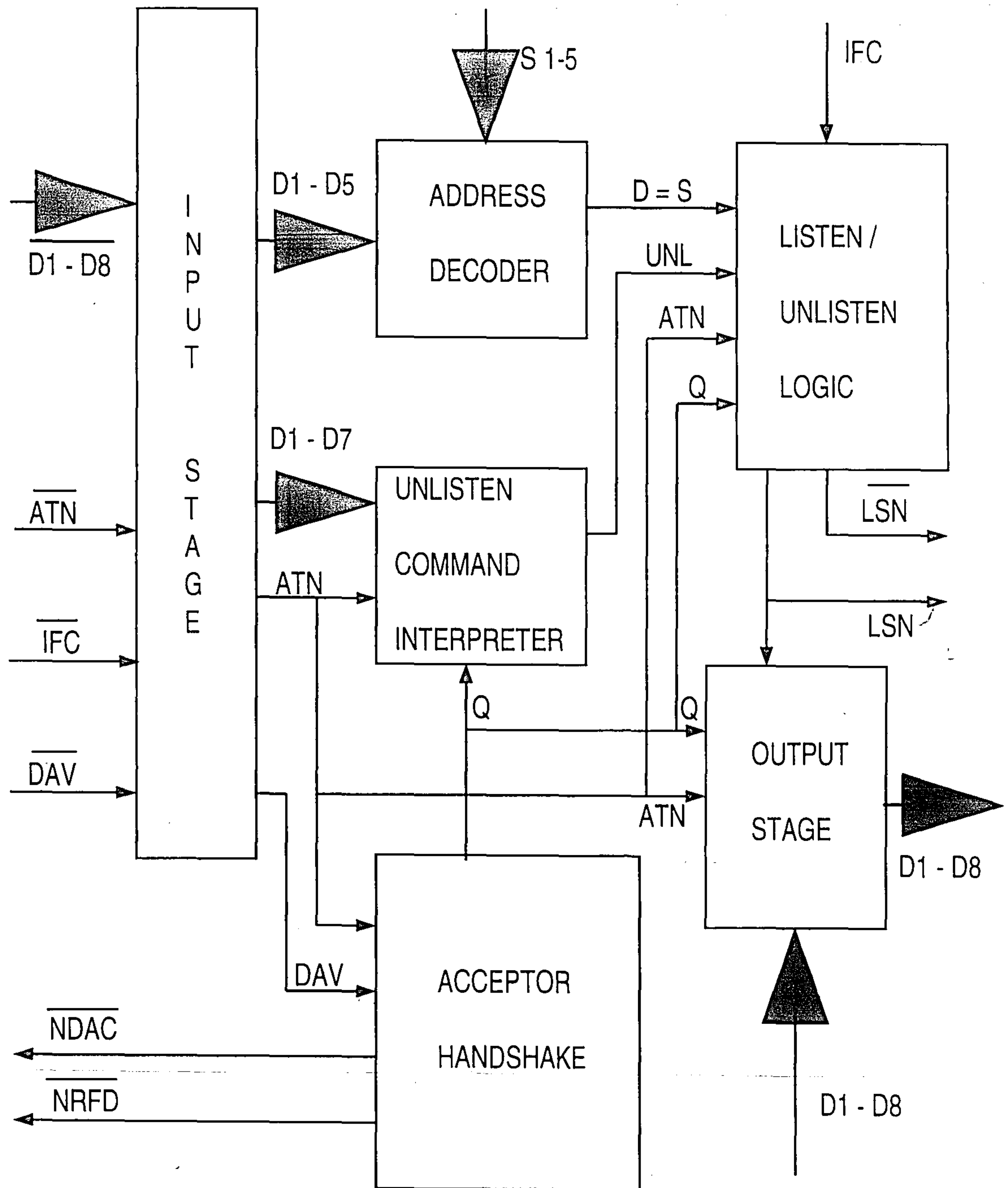


Figure 3.10: Block diagram representation of the HPIB (IEEE-488) Data Interpreter [30].

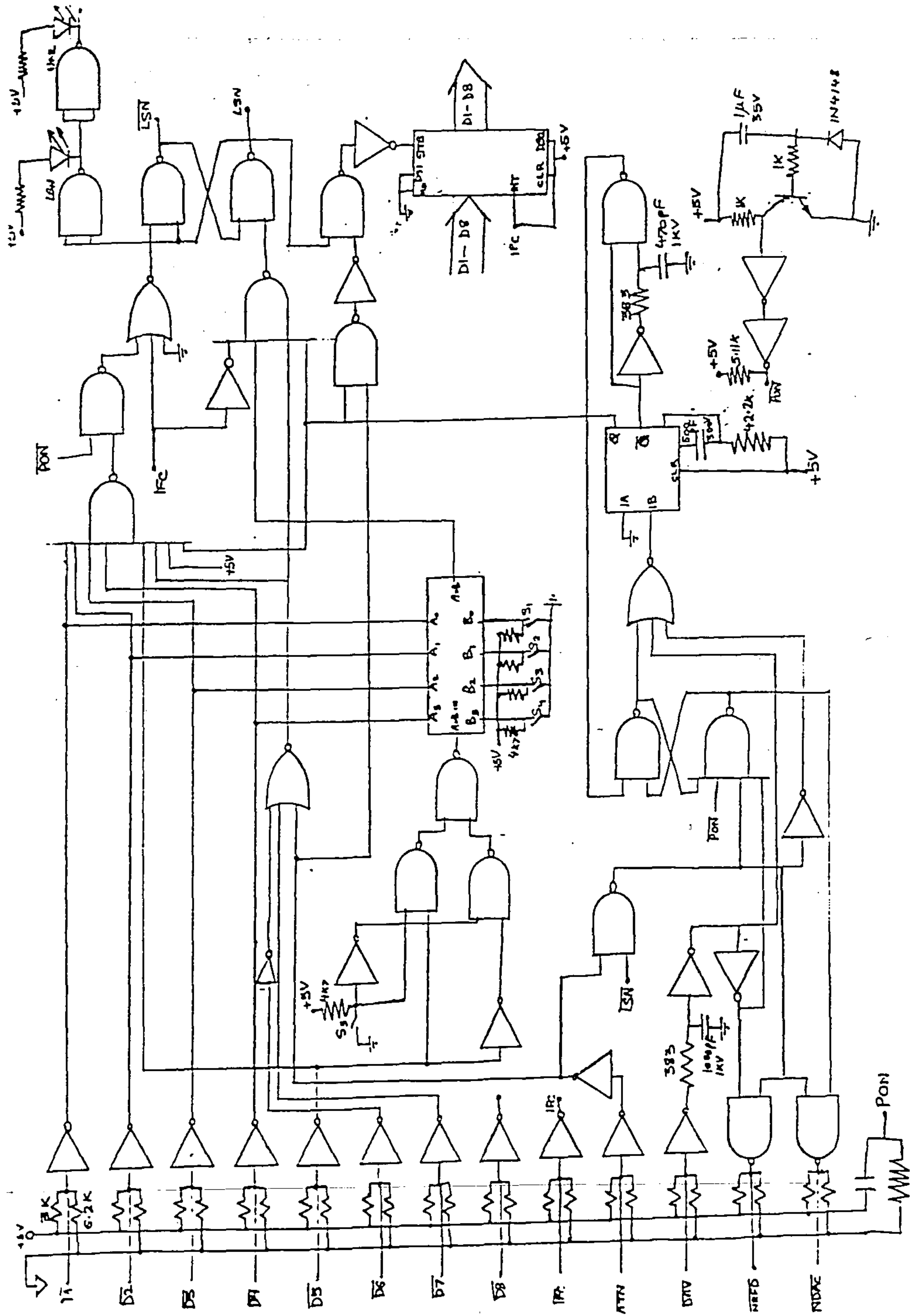

Figure 3.11: Circuit diagram of one of the channels in the HPIB (IEEE-488) Data Interpreter. The address is set using the dip switches. Inputs and outputs are buffered and latched TTL compatible output is provided [20].

## 3.8 Circuit Description

The circuit is comprised of functionally differentiable blocks as shown in Fig.3.7.

- **Input Stage**: The input stage consists of buffers and the signals are also inverted to eliminate noise and change low-true to high-true logic. The Schmidt inverters (74LS14) are used with proper pull up and pull down resistances at their inputs.

- **Address Decoder**: Five DIP switches in the circuit board are used to select an address for the device. The decimal equivalent of the five switches determine the address of the device on the interface and ranges from 00 to 30 inclusive. However, address 21 is usually reserved for the controller. The ATN line, when true, indicates that the data is to be interpreted as an address. Address 31 is used as a universal UNLISTEN command. D1 to D4 are compared with S1 to S4 at the four bit comparator (74LS185). D5 and S5 are compared using a combinational circuit which basically implements an XNOR function. The $A = B_{in}$ pin is used to have an effective five bit comparator which turns the $A = B_{out}$ high when the address matches the switch settings.

- **Unlisten Command Interpreter**: ATN line true with address 31 is the universal unlisten command which sets all listening devices to UNLISTEN mode. D6 and D7 are low in this case, and thus, have to be monitored as well. An eight input NAND gate (74LS30) is used for this purpose.

- **Listen/Unlisten Logic**: The LEDs showing the LSN or UNLSN status of the device just indicate the output of the latch. The latch is triggered by the output of the UNLISTEN command interpreter and the address comparator gated with the IFC and Power On (PON) signals.

- **Acceptor Hand Shake**: Three wire handshaking is used and allows asynchronous data transfer with the baud rate automatically adjusting to the speed

of the sender and receiver, and thus, handles even the slowest addressed device. More than one device can accept data simultaneously. All acceptors become ready for data after being addressed and set on LISTEN mode. NRFD goes high with the slowest listener. The source validates data by setting DAV low. Acceptor sets NRFD low to indicate not ready for new data. After the timing pulse Q from the timer (74LS221), NDAC is set high to indicate having accepted the data. DAV is set high by the controller to indicate that the data is no longer valid. The acceptor sets NDAC low again and NRFD high to begin another cycle.

- **Output Stage**: The output stage consists mainly of the parallel port 8212 whose enable signal is controlled through the combination of LSN, ATN and Q signals. The control pins of the 8212 have been configured for latched output.

## 3.9 The Automated NVSM Test Setup

The design goal was to implement an entirely automated test station allowing the user to control every aspect of the testing with some software menu-driven options. HPIB compatibility was achieved using a "listener" circuit which was designed to allow the pattern generator to be controlled directly by the HP9836 computer. The listener interface gets latched to the last output data as desired. Both boards were incorporated in a box to become a permanent part of the test set up. A HP54501A Digital Oscilloscope added to the facilities allowing superior measurement procedures.

First, the incorporated menu allows the operator to choose the type of measurement desired (Erase/Write/Read or Retention or Endurance). Accordingly, the proper sequence of patterns and delays are typed in. Function keys have been

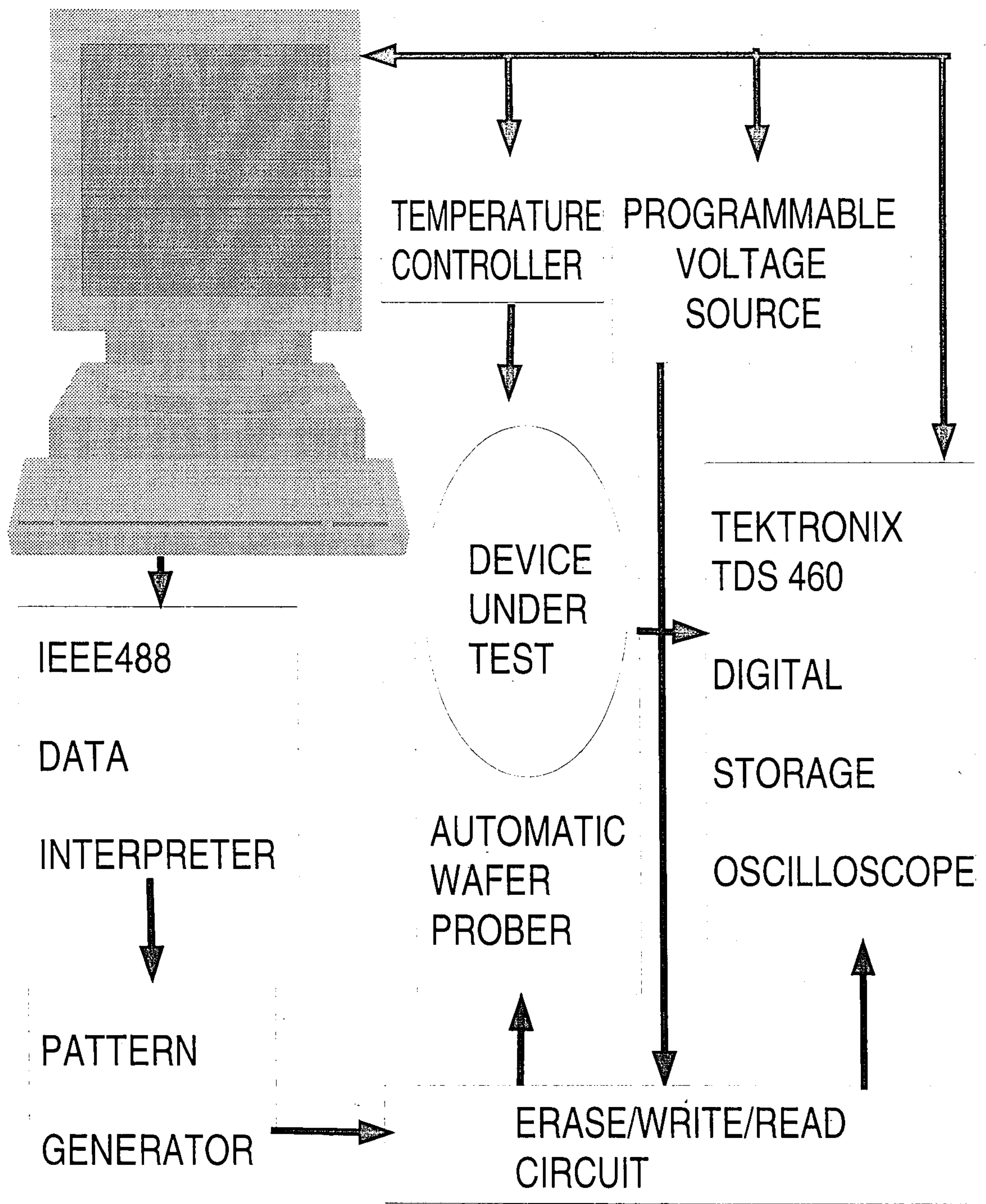


Figure 3.12: The automated test setup for nonvolatile semiconductor memories [30].

programmed to enhance user friendliness with a page menu. After the data entry stage, the program is run. The pattern generators memories are programmed with the pattern sequence and the respective delays. The pattern generator is even started remotely by the computer.

The oscilloscope is triggered with a TTL level Read operation trigger to capture the read pulse. It is programmed via the HPIB bus with the essential information about the active channels and their coupling type, offset, vertical amplifier setting; trigger source, level and slope; timebase setting; waveform acquisition mode; probe multiplication factors followed by information about the window to activate dual time base. This facilitates observing the overall waveform and simultaneously concentrating our attention to a windowed area where the cursors are set and automated measurements are carried out.

The entire waveform can be transferred over the HPIB to the computer where the required data can be found using parameter extraction routines. However, this is time consuming and will increase testing time very heavily as numerous devices have to be tested. The oscilloscope can itself very useful data about the waveform. The difference of the minimum and maximum in the windowed area is noted. If this number exceeds a preprogrammed noise threshold, the waveform is neglected as noisy and a fresh acquisition is made. When the noise threshold is not exceeded, the average of the windowed region is noted. The window then shifts to note average ground value after the pulse has receded. This offers a dynamic value of the reference level and avoids ground loop errors. The program initially allows the operator to position the window on which is altered by the computer as is required later in cases of excessive sampling anomalies.

The computer stores the threshold voltages as measured and reprogrammes the pattern generator with fresh data to allow sweeps of delay timings. The pattern generator is reset by the computer whenever not required to prevent unnecessary cycling of the device. In Erase/Write tests, the Write(Erase) time periods are stepped and

the threshold voltage noted afresh each time. When plotted, it shows what is known as the Erase-Write curve. This gives valuable information about the memory device regarding the speed and memory window. During retention measurements, the idle time between the erase and write is varied to observe the decay of charge stored as a function of time. The endurance tests can be performed by asking the computer to start the pattern generator for a calculated time determined from the cycling time and the number of cycles desired to performed on a device. This is especially attractive as the cycling time is varied, for different number of cycles, to hours and days. Additionally, the programming voltage, when supplied by a DAC (Digital to Analog Converter), can be altered by the program to observe its effect on programming capability. Measurements at different temperatures can be controlled using the temperature controller's link with the computer. The associated software has been developed to exploit the advantages that this setup offers. The data can be stored or transferred to any computer system for usage with parameter extraction routines. The system has been configured keeping in mind the future requirements. Merely, replacing the Erase/Write/Read circuit will allow testing of other memory devices and even arrays.

# Chapter 4

# Experimental Data

## 4.1 Objective

Efforts are being concentrated to achieve a low voltage programmable EEPROM. This shall require lesser power and be most suitable for battery operated applications including notebook computers. When used for space applications and other crucial purposes, reliability becomes a key issue. Erase/Write curves show the memory window and the cross-over time, an indicator of speed of programming. Retention and endurance measurements are a key to understanding the reliability of the device.

## 4.2 Erase/Write Characteristics

The Erase (Write) curve is obtained by having a fixed write (erase) time to saturate the device. The erase time is varied and the device read to obtain the threshold voltage. The threshold voltage changes as the charge stored in the nitride which depends on the time for which the pulses have been applied. The memory window increases with programming voltage as more charge tunnels through the tunneling oxide for greater fields. Speed of programming increases with the programming voltage too. The cross over time is considered an important benchmark along with the programming voltage.

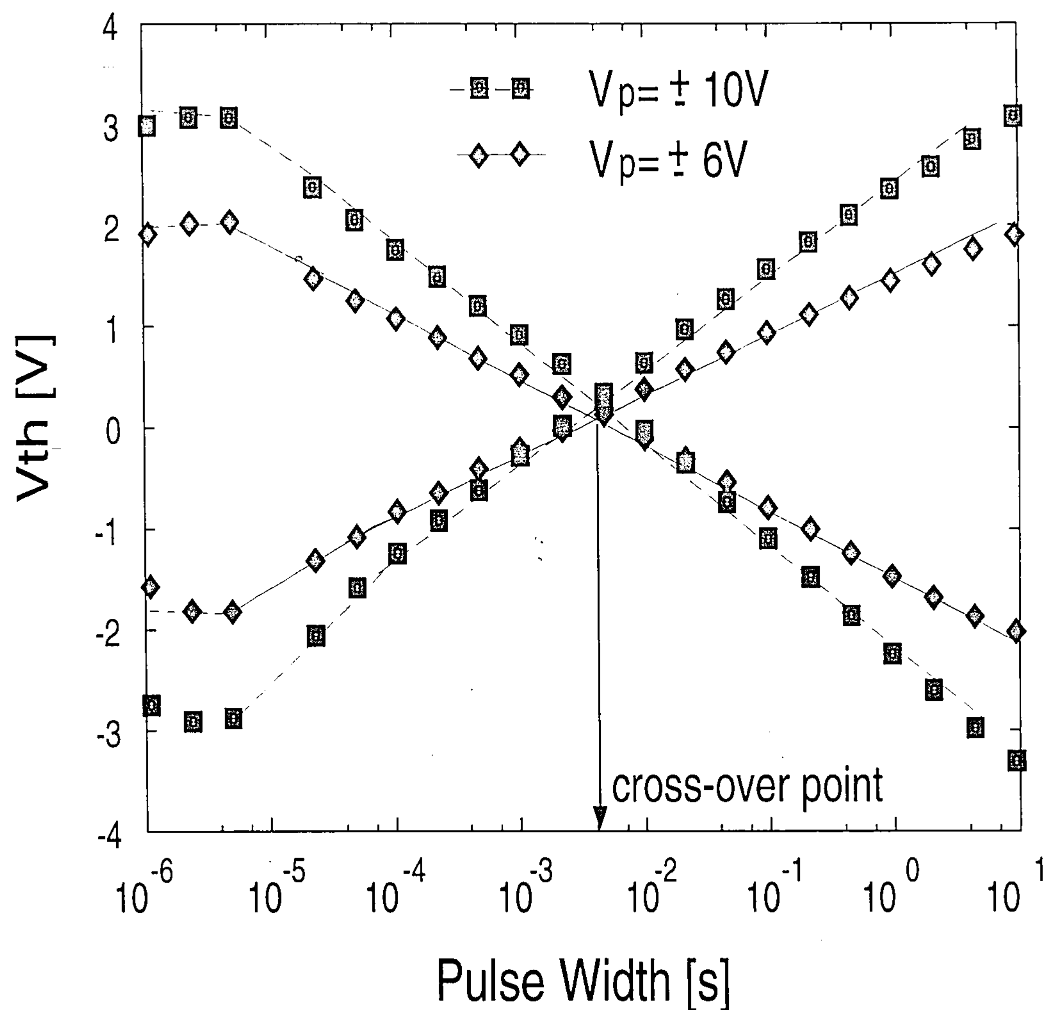


Figure 4.1: The Erase/Write characteristics of the SONOS device is shown with 10V and 6V programming voltage. The gate dielectic is constituted as $x_{ot} = 20\mathring{A}, x_n = 68\mathring{A}, x_{ob} = 72\mathring{A}$. The memory window is 3V for 10V programming, but 2V for 6V programming voltage. The cross over time is almost consistent at $4\times10^{-3}$s [30,33].

For each point in the plot, a number of points are acquired and averaged. The programming voltage can be altered from the computer using a programmable voltage source. Eq.4.1 shows the relation of the charge stored and the threshold voltage.

$$\Delta V_{th} = -(\frac{x_N}{\epsilon_N} + \frac{x_{ob}}{\epsilon_{ox}})\delta Q_N \tag{4.1}$$

## 4.3 Retention

Retention measurements are a strong indicator of the quality of the tunneling oxide (Fig.4.2). As devices are scaled, the blocking oxide and the nitride thicknesses are reduced. More charge is stored near the nitride-blocking oxide interface. Back tunneling through the blocking oxide to the gate increases. Hu has presented in detail the physics behind the loss of charge [21]. The field in the blocking oxide increases with the scaling, enhancing this process.

## 4.4 Endurance

As the Erase and Write operations are repeated, the fields in the device are reversed. This causes the built up of interface states. This causes a rise in the threshold voltage for the same programming specifications except being cycled. The quality of the tunneling and blocking oxides and the electric field determine build up of interfaces traps [31, 32, 25] which affect decay rate of stored charge shaping the endurance characteristics.

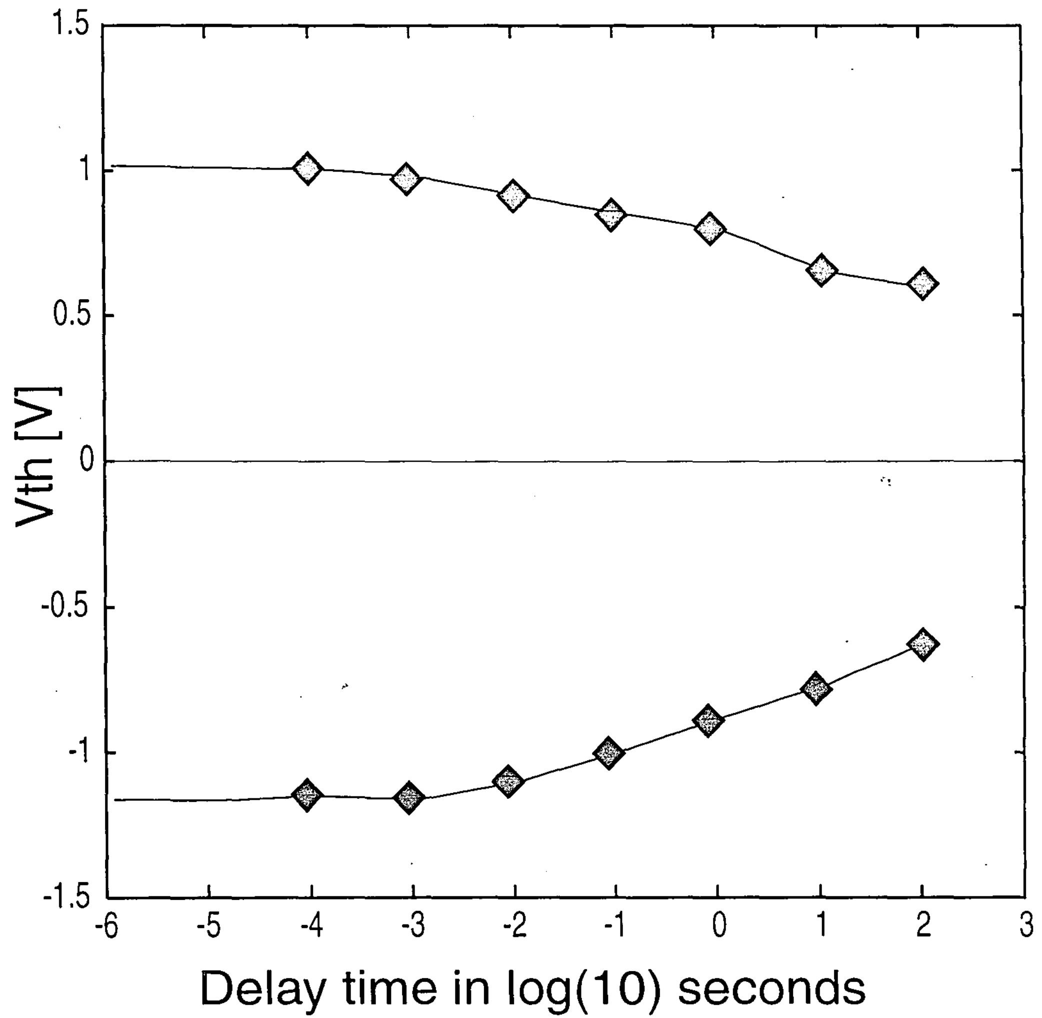


Figure 4.2: The retention characteristics of SONOS device with 10V programming voltage was used with 29ms of write time and 150ms of erase time. The thicknesses were $x_{ot} = 20\AA, x_N = 68\AA, x_{ob} = 72\AA$. $W/L = 150\mu m/10\mu m$ [30].

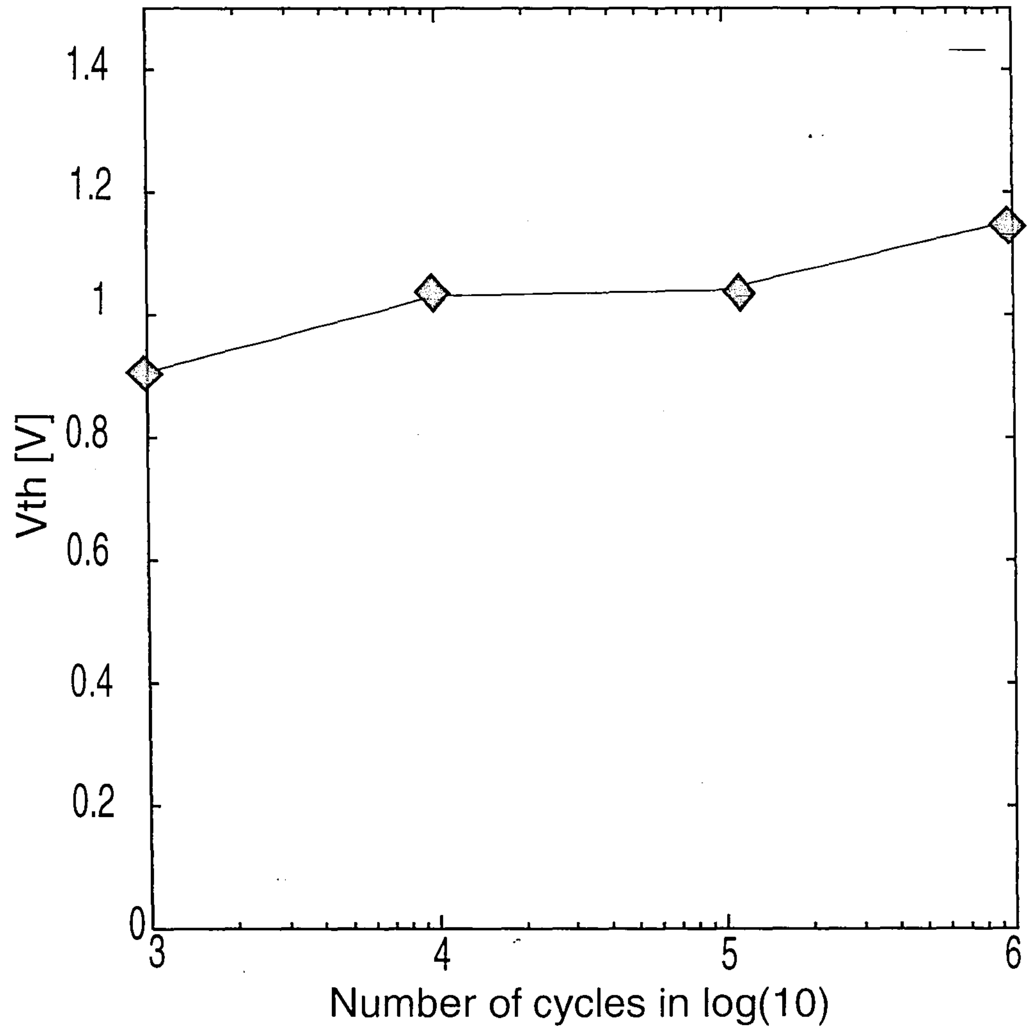


Figure 4.3: The threshold voltage is plotted against the number of erase/write cycles. The dielectric thicknesses are $x_{ot} = 20\mathring{A}, x_N = 73\mathring{A}, x_{ob} = 54\mathring{A}, W/L = 150\mu m/10\mu m$. 9V programming was done for 3ms write and 30ms erase [30].

## 4.5 Quality of Oxides

An ultra-clean/dry triple-wall oxidation process was used to grow the 20$\AA$ tunneling oxide layer to achieve high quality thin oxide and minimize the built-up of the Si/Si$O_2$ interface states due to the Erase/Write cycles. The quality of the tunneling oxide of SONOS device is a critical factor in determining the device reliability. During repetitive Erase/Write cycles, electrons and holes tunnel back and forth through this oxide layer between the Si band and the nitride traps. This causes the formation of added interface states (Fig.4.5) to a sufficient density to accelerate the back tunneling of the charge stored near the tunneling oxide-nitride interface. Consequently, the stored charge leaks faster, effecting device memory retention [33]. In addition to the back tunneling of stored charge, the formation of the interface states also deteriorates the channel mobility so that the device fails to deliver the current properly during the read mode. This affects both the ability to program the device and the retention of charge (Fig.4.5). The triple-wall oxidation furnace eliminates the diffusion of heavy metal ions, mobile alkali ions and moisture from the quartz wall of the furnace during the oxidation.

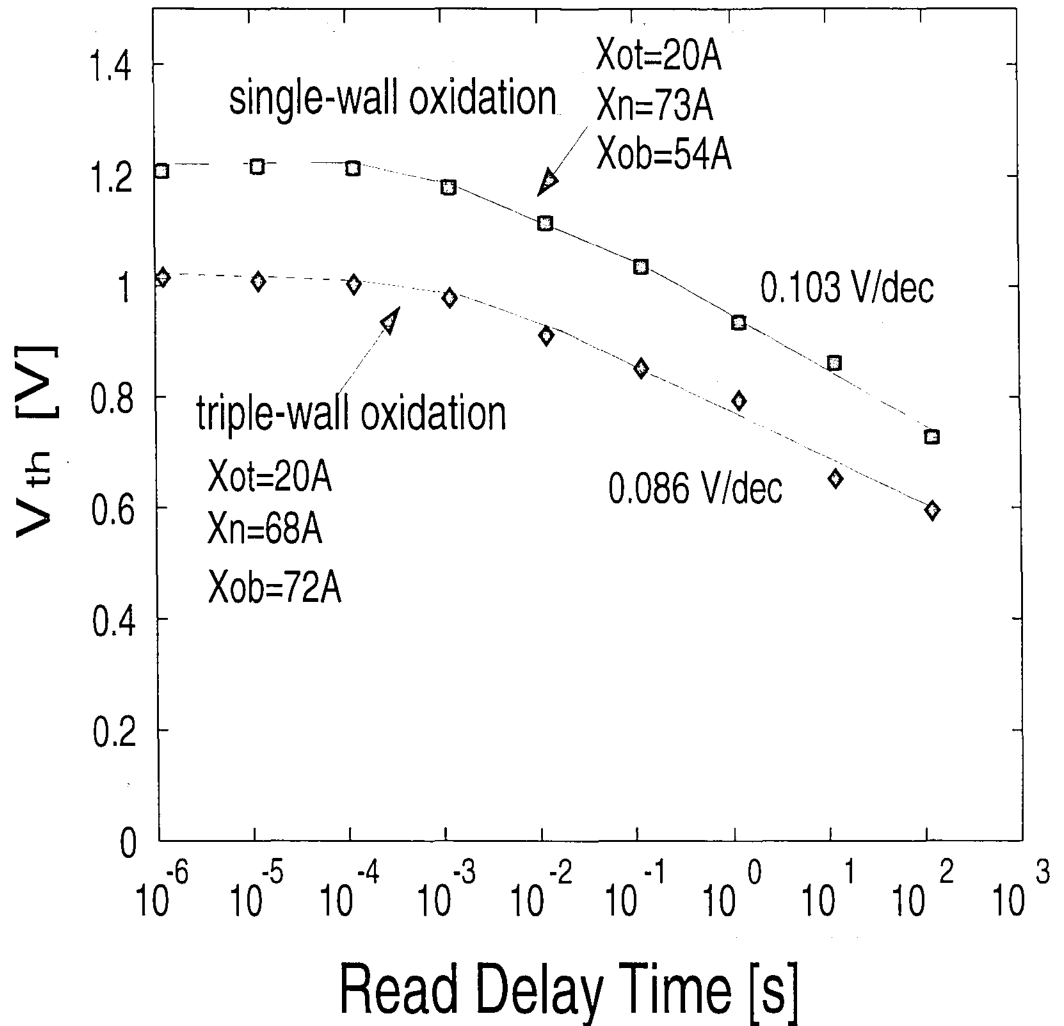


Figure 4.4: This is a comparison between the retention characteristics of two SONOS devices after they have been cycled a million times. The gate oxides of one device was grown in the conventional single wall oxidation furnace and the other in an ultra clean triple wall oxidation furnace (TWO). 10V programming voltage was applied with 20ms write and 150ms erase times on the TWO furnace grown device and 9V programming was done on the SO furnace grown device for 3ms write and 30ms erase times. Both devices measured $W/L = 150\mu m/10\mu m$. Notice that the single wall furnace grown device has faster rate of stored charge decay [30,33].

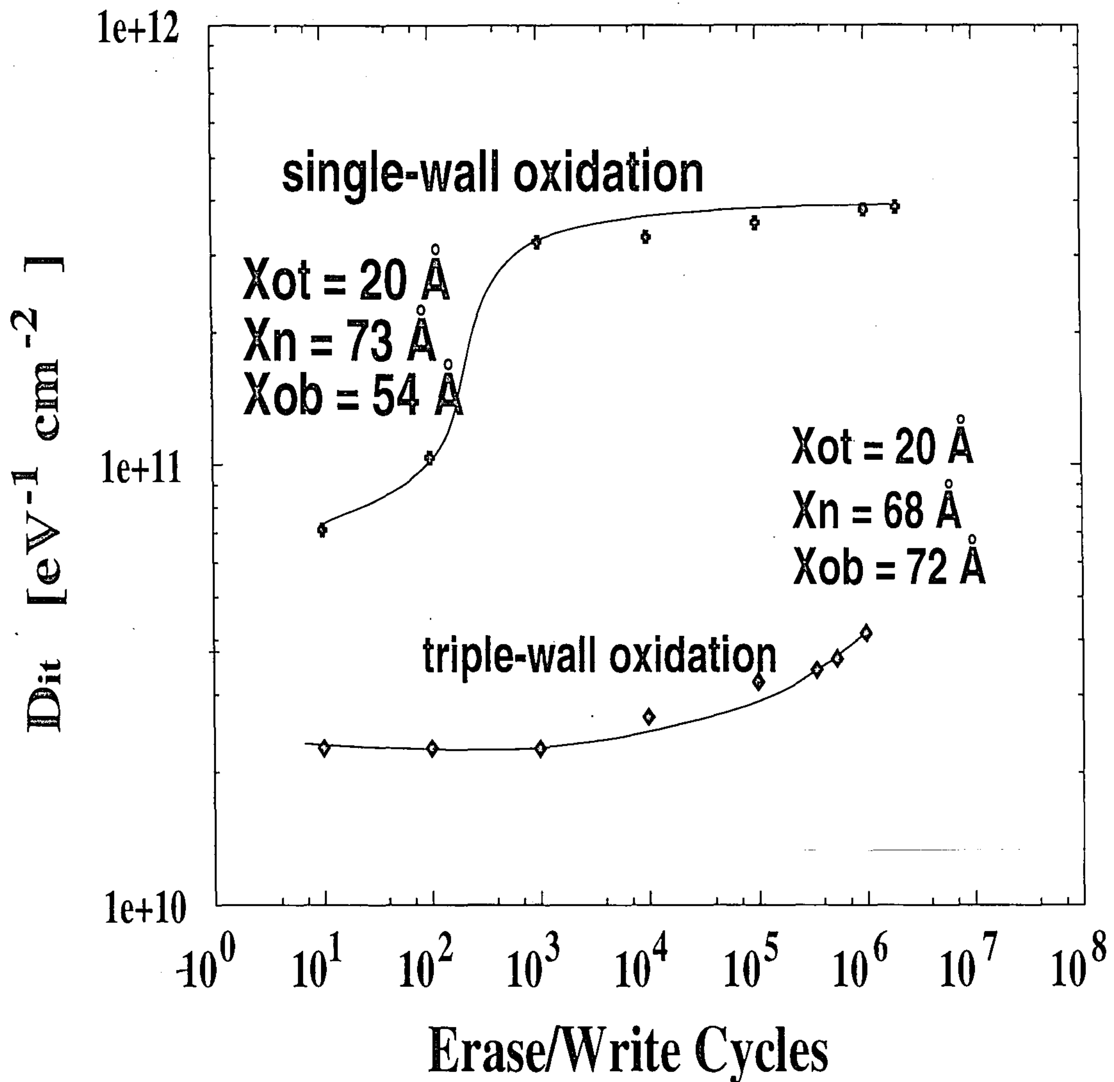


Figure 4.5: The growth of Si-Si$O_2$ interface trap density, $D_{it}$, is plotted as a function of the number of erase/write cycles. The dielectric thicknesses are shown in the figure. The single wall furnace grown device had dimensions of $W/L = 24\mu m/24\mu m$. 9V programming was used for 3ms write and 30ms erase pulses. The TWO furnace grown device had $W/L = 48\mu m/24\mu m$ and was programmed with 20ms write and 150ms erase pulses at 10V. The difference in the programming voltages is to maintain same field in the gate dielectrics of the two devices [33,21].

# Chapter 5

# Concluding Remarks

## 5.1 Advantages of the Automated System

In the past, it took considerable time to be able to trigger the oscilloscope. The read pulse is of the order of $100\mu s$ whereas the entire cycle is in the order of tens of milliseconds with nominal idle times during erase/write curves. This scenario for endurance measurements becomes worse as the idle time between the erase, write and read is increased to study the loss of charge over time. This makes it difficult to trigger to such a narrow pulse which occurs once in seconds or more. Also, the accuracy of the measurements depended heavily on the operators placing the cursors on the screen. Only one point is measured by one cursor at a time. The operator has to note down the cursor readings. The pattern generator has to be reset and started manually everytime. Programming from the AIM-65 using its one line display is cumbersome. To sum it up, it took days to obtain the erase-write curves and the retention plot for one device. During an endurance measurement, no reads were done. If the device failed or any other problem occured during the cycling time, then there was no verification or no indication of the process going on and of the condition of the device during cycling.

The new automated test system does it all by itself once started and in a matter of hours at the best. Each measurement is an average over a windowed area rather than single points. Dynamic value of the bulk potential is measured to enhance accuracy and reduce ground loop errors. Erase-write curves with sweep of the time

axis, with multiple points for each data position to average, takes a few minutes. It does the retention plots in a few minutes too. Specially, for endurance measurements, reads are done every cycle and the threshold is measured all the time. The operator can check the condition of the device under test simply by looking at the oscilloscope display. The control of the oscilloscope is put to local mode enabling it to be used for other purposes or to take independent measurements on the read pulse itself. Also, the operator can access all instruments from the computer terminal once the connections are made and power supply switched on. The pattern generator is started and reset remotely by the computer. This tries to minimize unnecessary cycling of the device. The program has been written as a subroutine of the FIDDLER software developed in house by Dr. Richard Booth and added to and improved over the years by many graduate students. This makes plotting the data a matter of just pressing the plot key.

The data can be stored as an ASCII file and transferred to the Unix environment. Many standard data processing and parameter extraction softwares are available which allow comparison of practically measured data with simulation results.

The features of the test system has made it a very flexible tool. It can be configured in many more ways to assist in automated measurements and even control of other setups. Efforts are being made to develop software for operating the test station from the SUN workstations. A very desirable set up will incorporate the automatic wafer prober when the testing shall require only placing the wafer and starting the program. The entire wafer should be tested thoroughly and all results stored for future utilisation. This shall effectively maintain the repeatability of the measurements and decrease the human error factor. With modifications, other nonvolatile semiconductor memory elements can be characterised.

This test station uses a method where the device is effectively brought to the same initial state by saturating the device (the nitride traps are all filled due to long erase or write times). Study of threshold changes due to single erase or write

operations cannot be quantified. These effects are cumulative. This problem can be solved using an Erase/Write/Read circuit which shall allow separate trigger signals for consecutive read pulses. Thus, the threshold of the device after each operation can be measured. This is essential for memory array applications of the SONOS device where the device is operated in the dynamic region to obtain faster erase and write times.

## 5.2 Testing of Arrays

The design and layout of memory arrays has already been completed. In the near future, testing of arrays will become very crucial. A lot of research has gone into developing the SONOS technology. Now armed with the knowledge, a calculated effort in the array technology combining SONOS and regular CMOS will yield promising results. Addressing the issue of testing these arrays, the automated test system will require minimal changes in the hardware. The individually addressable pins (patterns validated at a wide range of time delays) of the pattern generator will prove valuable to sequence through the array and interrogate the memory locations. The additional data will be used to study device isolation and extract parameters to quantify write or read disturbs. The Erase/Write/Read circuit's TTL compatible switching current source and potential application procedures may be still be used depending on the array design. For tests where speed and time is not the issue, the HPIB Data Interpreter's two buffered and latched output ports can be utilized directly as digital signals to access and test arrays.

In an array, the programming voltages are applied via path transistors belonging to the peripheral circuitry connecting the word and bit lines. The memory device is thus protected from wide fluctuations in the fields and also the transient spikes which occur at the testing of individual devices due to the buffering action of the adjacent circuitry.

## 5.3 To the Making of a Better Device

The potential of the automated test setup's contribution to making of better devices is already being realised. Processing of devices in a fabrication laboratory is an art learned by experience and never ceasing experimentation. However, the feedback about the effects of variations from the standard procedure has to be accurate and practical. Previously, only testing a small number of devices was possible and, thus, a strong feeling for the effects of the processing parameters was lacking. Immediate feedback is needed to ensure rapid changes in fabrication methods to work towards the goal of a low voltage programmable EEPROM. Significant conclusions will be made from studying extensively a large number of devices. One of the most important aspects of testing is to make it less cumbersome and demanding less manual operations. This reduces chances of human error. Tedious, repetitive and time consuming procedures are prime targets for automation.

On a more encouraging note, it should be remembered that a memory device used as a digital memory element allows for a relatively wide variation in the threshold voltage compared to the analog change in threshold voltage we are concerned about while testing. Also, the device in an array is not subjected to rapid transients (exceeding $10^8$ V/s) which might cause displacement currents to affect charge stored.

A very effective study of the device quality and behaviour over extended usage in a real life situation embedded in an array is found based on the erase/write curves and retention curves obtained intermittently while cycling the device to at least a million times. This is incidentaly a measurement which allows the operator to realise the advantages of an automated setup.

The variations of parameters across the wafer can be plotted in wafer maps or "schmoo plots" which lend insight into the quality of the materials and nature of depositions and growths during the numerous processing steps.

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# Appendix A

# SONOS Device Fabrication Technology

The present fabrication technology is a CMOS n-well process with LOCOS isolation. Additional steps are carried out for the memory gate dielectric [21, 23, 22].

## A.1 Starting Material

- p-substrate $< 100 >$Si 2-3 $\Omega$-cm, 3 inch diameter

## A.2 LOCOS Oxidation

- RCA clean : Wafers are cleaned before inserting into the furnace. Etching is followed using diluted hydrofluoric (HF) acid to remove any native oxide.
- pad oxide : 950°C, 12 min, wet $O_2$, 300$\AA$
- nitride: This acts as oxidation mask for field oxide. LPCVD, 750°C, 35 min, 0.3 Torr, $NH_3 : SiCl_2H_2$=100:20, 1200$\AA$
- photo: mask AD, cover the active area
- plasma etch nitride: 0.3 Torr, 125 W, $CF_4$, 2 min

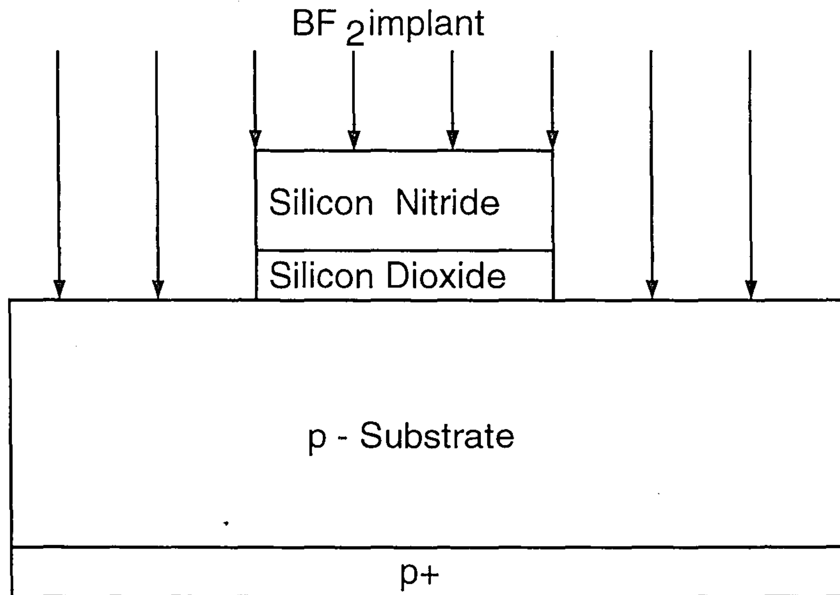


Figure A.1: Field implantation

## A.3 Field Implant

- front implant: $BF_2$, 145 keV, 5x$10^{14}cm^{-2}$
- back implant : This facilitates back contact.
  B, 32 keV, 2x$10^{15}cm^{-2}$
- strip PR: PRS-2000
- anneal : 950°C, 30 min, $N_2$
- etch oxide : BHF, 1 min

## A.4 Field Oxide 6k$\AA$

- RCA clean

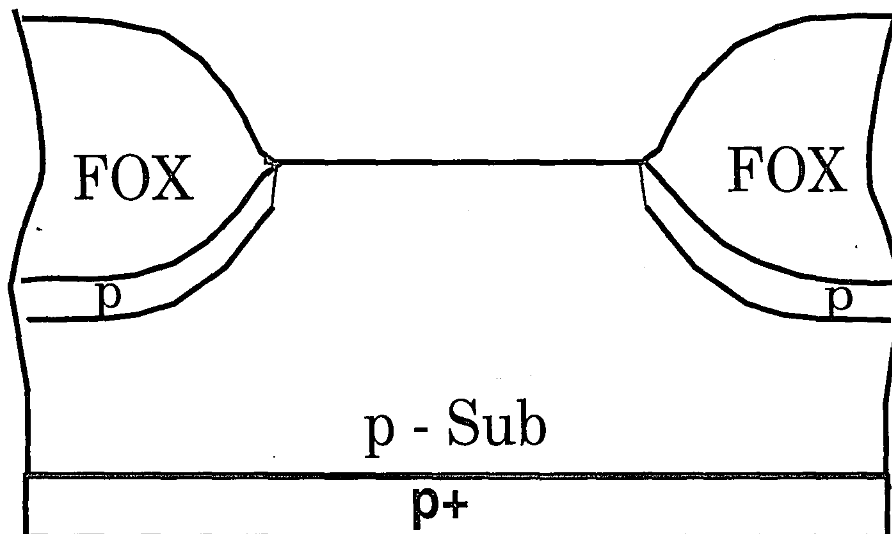


Figure A.2: After field oxidation, the $Si_3N_4$ is removed using hot nitric acid followed by etching the pad oxide with HF acid.

- wet oxidation : 1100°C, 70 min, wet $O_2$, 6k$\AA$
- etch oxide : BHF, 2 min
- etch nitride : nitride is removed from active area with hot nitric acid $H_3PO_4$, 165°C, 1 hr
- etch oxide: BHF, until hydrophobic to remove pad oxide.

## A.5 Sacrificial Oxide

The LOCOS process produces oxynitride at the edges of the active areas and forms what is known as the "bird's beak" because of its shape. This results in

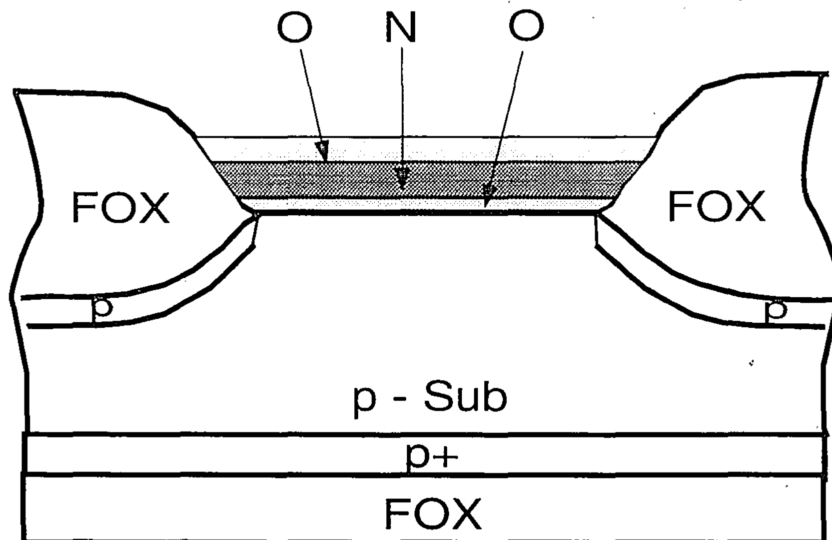


Figure A.3: The stacked gate dielectric

areas of thinner oxides on subsequent oxidation. The sacrificial oxide removes this oxynitride.

- RCA clean
- wet oxidation : 950°C, 12 min, wet $O_2$, 300Å
- etch oxide : BHF, until hydrophobic

## A.6 Gate Dielectric for SONOS

These steps are deviations from the standard CMOS process.

- RCA clean

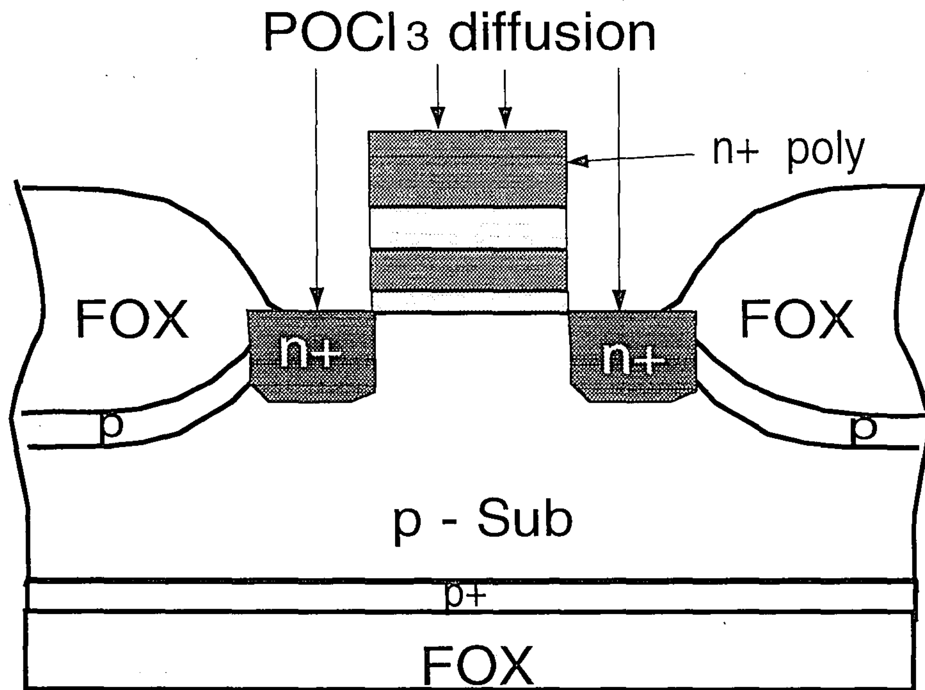


Figure A.4: Formation of the n+ gate using phosphorus diffusion

- oxide : while growing the tunneling oxide, care is taken to keep the latent $Si/SiO_2$ interface state density low. An ultra clean, triple wall oxidation furnace is used.
  triple wall oxidation, 700°C, 12 min, 1.5 l/min, $O_2$
- anneal: 700°C, 30min, 1.5 l/min, Ar, in situ
- nitride: LPCVD 0.3 Torr, $NH_3 : SiCl_2H_2$=100:33, 750°C, 8 min, 55Å
- oxide : The blocking oxide is deposited on the nitride.
  LPCVD, 0.8 Torr, $N_2O : SiCl_2H_2$=100:20, 750°C, 12 min, 60Å
- anneal : 900°C, 30 min., wet $O_2$

## A.7 Polysilicon, $n^+$gate

- LPCVD : Polycrystalline silicon is deposited. 0.8 Torr, 280 sccm $SiH_4$, 625°C, 30 min, 5k$\AA$
- photo : mask PY1, polygate definition
- plasma etch: poly, 0.3 Torr, 200 W, $SF_6$, 5 min, both sides
- chemical etch : remove the composite ONO structure left on the drain and source regions.
- strip PR : PRS-2000
- RCA clean
- diffusion : $POCl_3$, 900°C, 20 min
- drive in : $N_2$, 900°C, 30 min
- etch p-glass : BHF, 15 sec

## A.8 Contact Window

This thick oxide is grown in a wet ambient to separate the active device terminals, namely, the source, drain and gate contacts. The oxide is made thick enough to resist etching by BHF before metallization.

- RCA clean
- oxide : 900°C, 45 min, wet $O_2$, 1200$\AA$
- photo : mask CW to define contact window

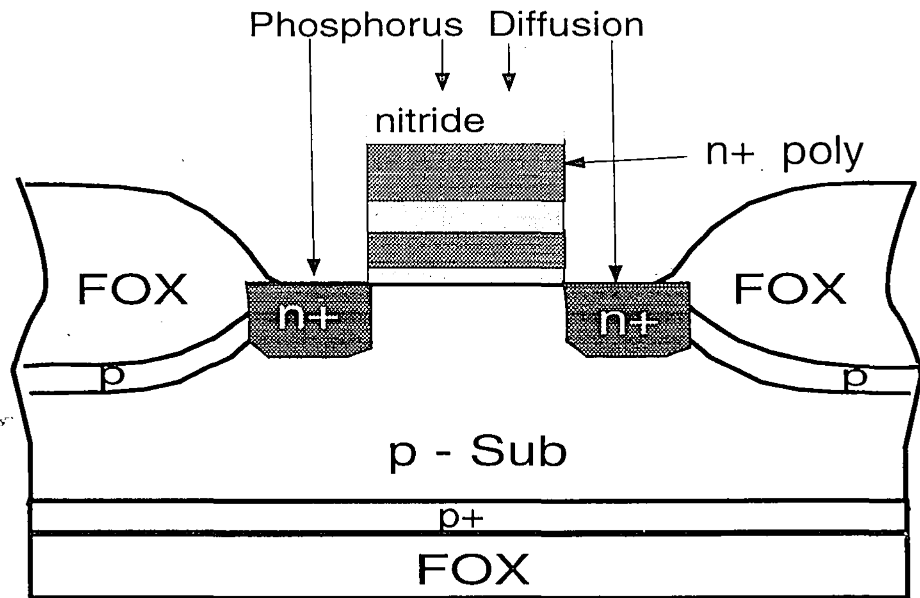


Figure A.5: The n+ source and drain contacts are formed using phosphorus diffusion

- etch oxide : BHF, 5 min, removes oxide from active areas.
- strip PR : PRS-2000

## A.9 Metallization

- RCA clean followed by HF dip, critical for making good contact.
- Al sputtering : DC sputtering system using Aluminium target with trace Silicon; front side, 7kÅ, 7 Hg, 0.4 Amp.
- photo : interconnection, mask MET
- etch Al : Phosphoric-Acetic-Nitric Acid (PAN) etch, 45°C, 2 min.
- strip PR : PRS-2000

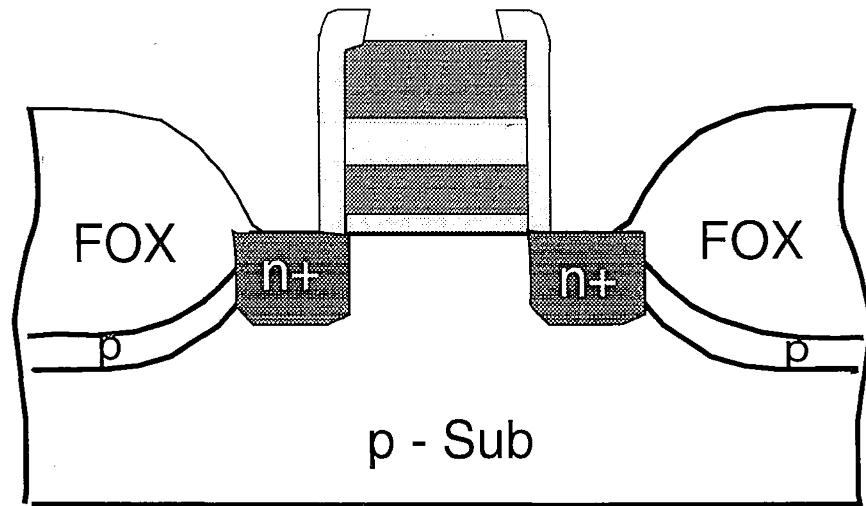


Figure A.6: The device cross-section after the contact windows have been opened

## A.10 Back Contact

This step provides the bulk contact at the back of the wafer to the p+ region.

- photo : PR on front side
- etch oxide : BHF until hydrophobic
- Al sputtering : back side, 7k$\AA$
- strip PR : PRS-2000, front side
- Organic clean: 10 min Acetone, 10 min Methanol
- anneal : PMA in forming gas, $H_2/N_2$, 475°C

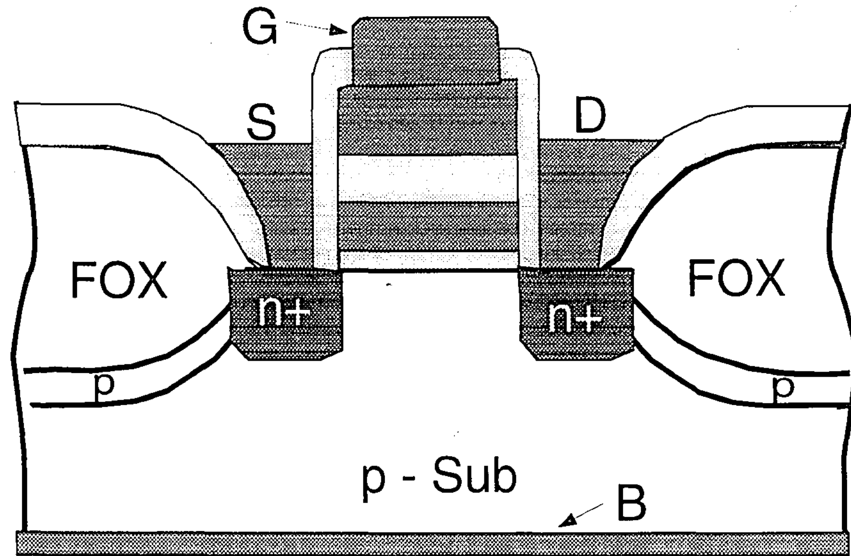


Figure A.7: The n-channel SONOS device cross-section

## A.11 Some Precautions

As aggressive efforts are being made to scale down the programming voltage, the gate dielectric constituent layers are becoming thinner and thinner. But when, for example, the tunneling oxide is of native oxide (around 10-12$\AA$) thickness, quality of the oxide becomes very important. In fact, endurance to cycling through varying electric fields lead to creation of interface and near interface states, which in their turn reduce the retention property of the device. Also tunneling through the blocking oxide decreases the retention. The $Si/SiO_2$ interface is thus a very important issue.

Care has to be taken during growth of the sacrificial oxide to reduce the "bird's beak". Etching the oxide while opening up the contact windows and before metallization is essential. Over and above, cleanliness has to be maintained to prevent

contamination. Though repetitive and tedious, cleaning procedures should be carried out thoroughly.

# Appendix B

# System Operation

## B.1 Operating Procedure

Make the power supply connections to the instruments (HPIB Interpretor, Pattern Generator, Erase/Write/Read circuit) and inspect the voltage levels at their outputs.

The probe station used should shield the device under test from electromagnetic waves.

The lengths of probes should be kept at minimum. Check for ground loop errors.

Check that the addresses of the instruments have no repetition and are set properly in the program. The HPIB connection can be checked by issuing a clear command to the oscilloscope. The Interpreter has LEDs inside to show when addressed. A programmable power supply for the Erase/Write (programming) voltages adds more flexibility.

The pattern generator should be put to "remote" mode and reset. Select the device type ("n" or "p") with the manual switches on the Write/Erase/Read circuit module front panel.

Shunt the device (the source-drain) with a 1kΩ resistor to test the system first. The Read pulse should be visible on the display of the oscilloscope. Remove resistor on satisfactory operation.

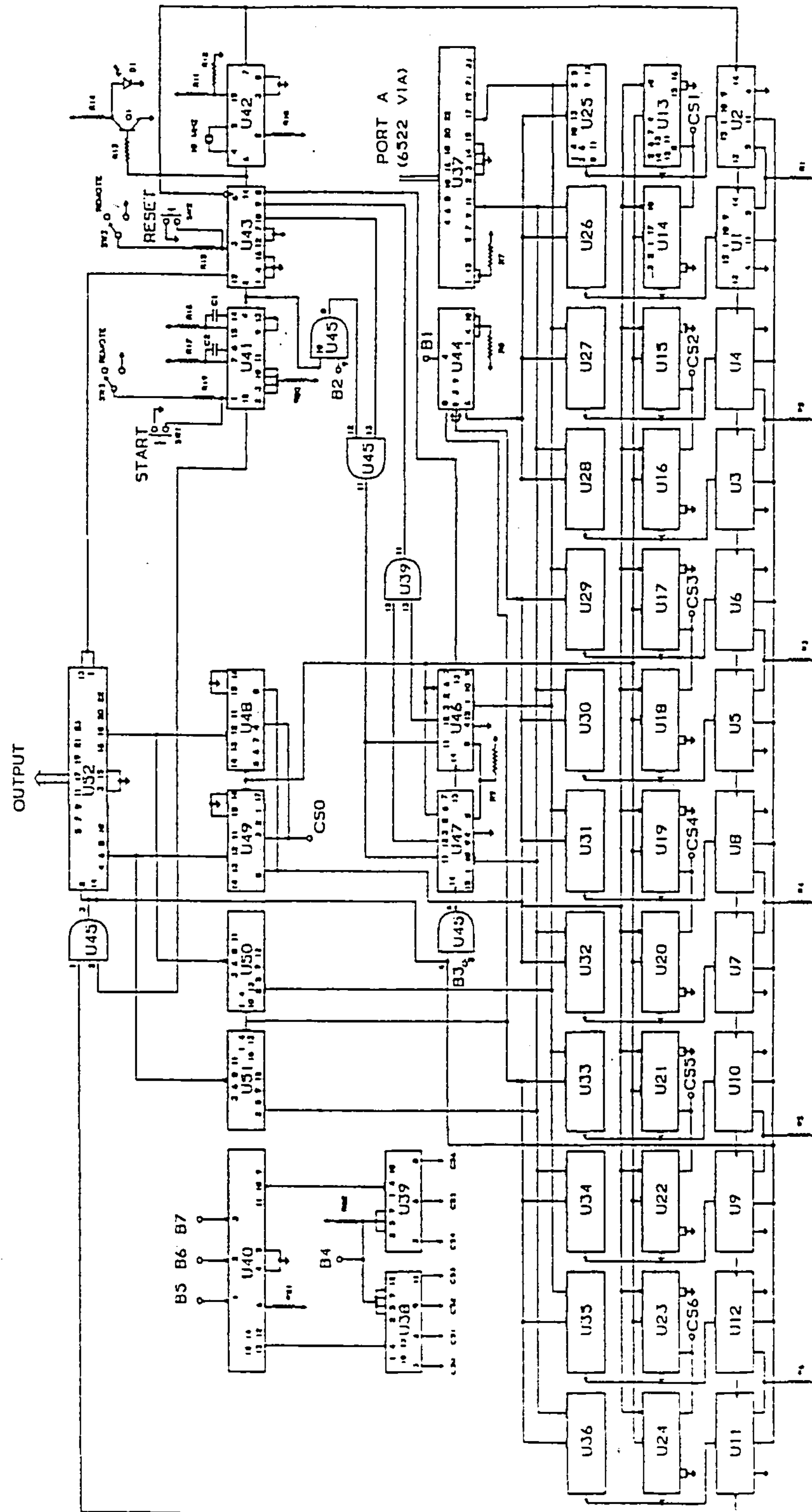


Figure B.1: Schematic of the Pattern Generator showing the signal paths and the memory distribution scheme. The counter ICs are loaded from the memory ICs [18].

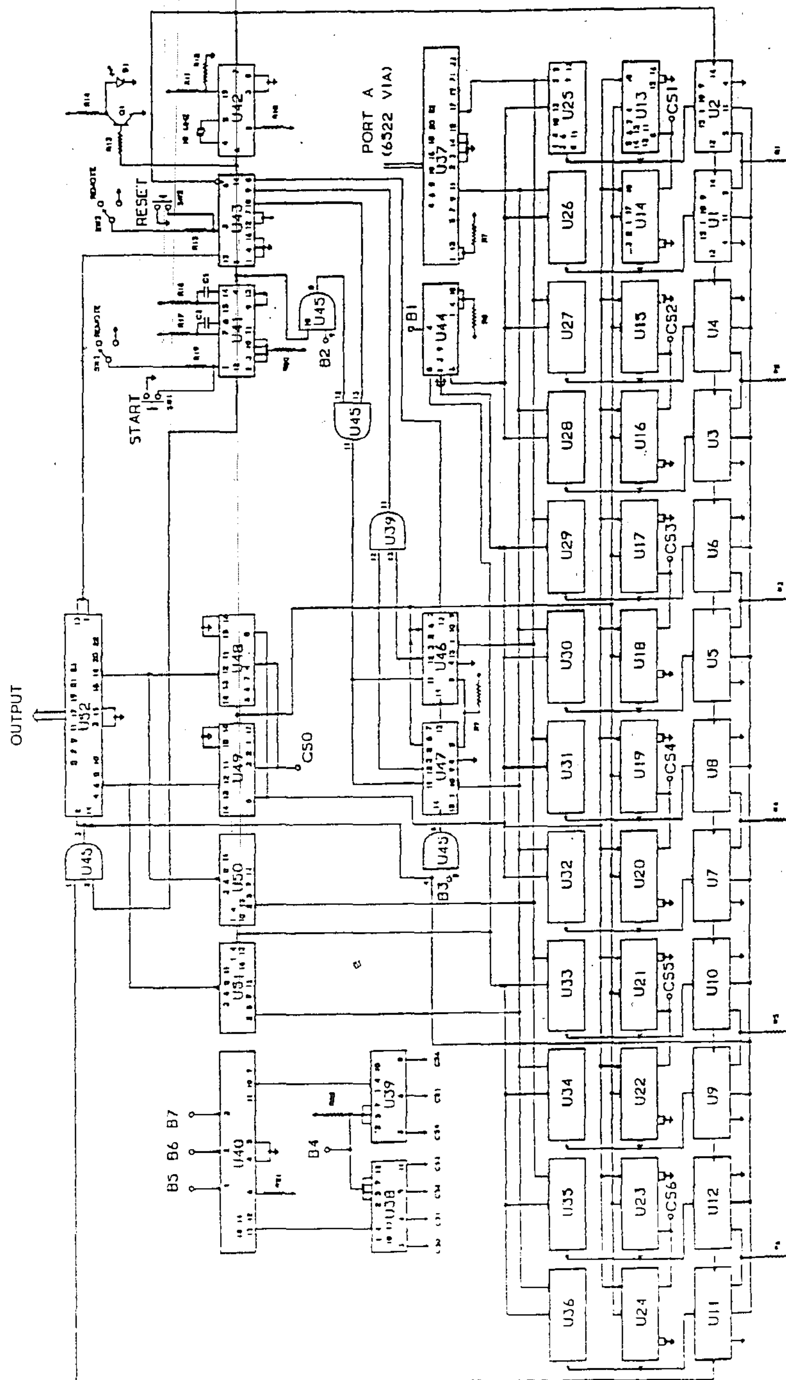

Figure B.1: Schematic of the Pattern Generator showing the signal paths and the memory distribution scheme. The counter ICs are loaded from the memory ICs [18].



INTENTIONAL SECOND EXPOSURE

Care should be taken while modifying the window position on the oscilloscope to allow maximum span for averaging. However, it should be restricted to a relatively noise free area.

For Erase-Write curves either the Erase or the Write time is kept constant and the other incremented over the range specified and then the other sweep is completed. For each of these measurements, the delay to vary should be specified to the program.

For retention measurements, first the Erase (Write) operation is carried out followed by Write (Erase). The device is Read after a varying idle time to check for loss of charge over different time periods.

The Endurance measurements take from seconds to days. The device is cycled for a large number of times. Hundreds or thousands of cycles take less than a minute. The time taken to cycle the device once is calculated by adding all the delay timings and multiplied by the number of cycles desired. The computer relinquishes the control of the oscilloscope enabling independent usage of it by operator. The pattern generator is stopped by the computer after this time. Erase write curves as well as retention programmes are run. Then cycling for longer times is resumed.

## B.2 The Algorithm

A detailed outline of programming the system is described step by step. Since the instruments can be programmed in any language using any computer with IEEE-488 bus access, the program itself is not unique to a given platform. The following details will make the steps apparent and provide an easy guideline to follow whenever attempting to program the system from different environments using different software and higher level languages.

1. The editor drives a menu with programmed function keys (hot keys) to assist in data entry and operation. Enter the following information :
   - Patterns and their respective Delays (Erase, Idle, Write, Read delay, Read). Delays are in seconds.
   - Delay to vary. For Erase (Write) curves, the Write (Erase) time is fixed and the Erase (Write) delay is stepped. The Idle time between Erase and Write is changed during Retention measurements.
   - Type of increment (linear, logarithmic or geometric)
   - Increment value and limit
   - Number of repeats for averaging for each data point
   - Noise threshold
2. Program the Pattern Generator (look for details in Fig.B.2) with the first pattern and delay sequence and start it.
3. Transfer the necessary information as follows to the oscilloscope.
   - Display type of testing on oscilloscope display. This is a check for the interface connection.
   - Set acquisition mode to normal with maximum sampling points devoted to the active channel for more preciseness.
   - Indicate active channel number (connect output from pattern generator to this channel) and set coupling type to DC with high frequency reject, vertical amplifier attenuation and offset. Also set probe attenuation factor to allow the oscilloscope to compensate the automated measurements accordingly.
   - Send information to oscilloscope about the display characteristics desired.
   - Set timebase to enable full display of the Read signal. The program gets this information from the Read delay entered. Also start the window

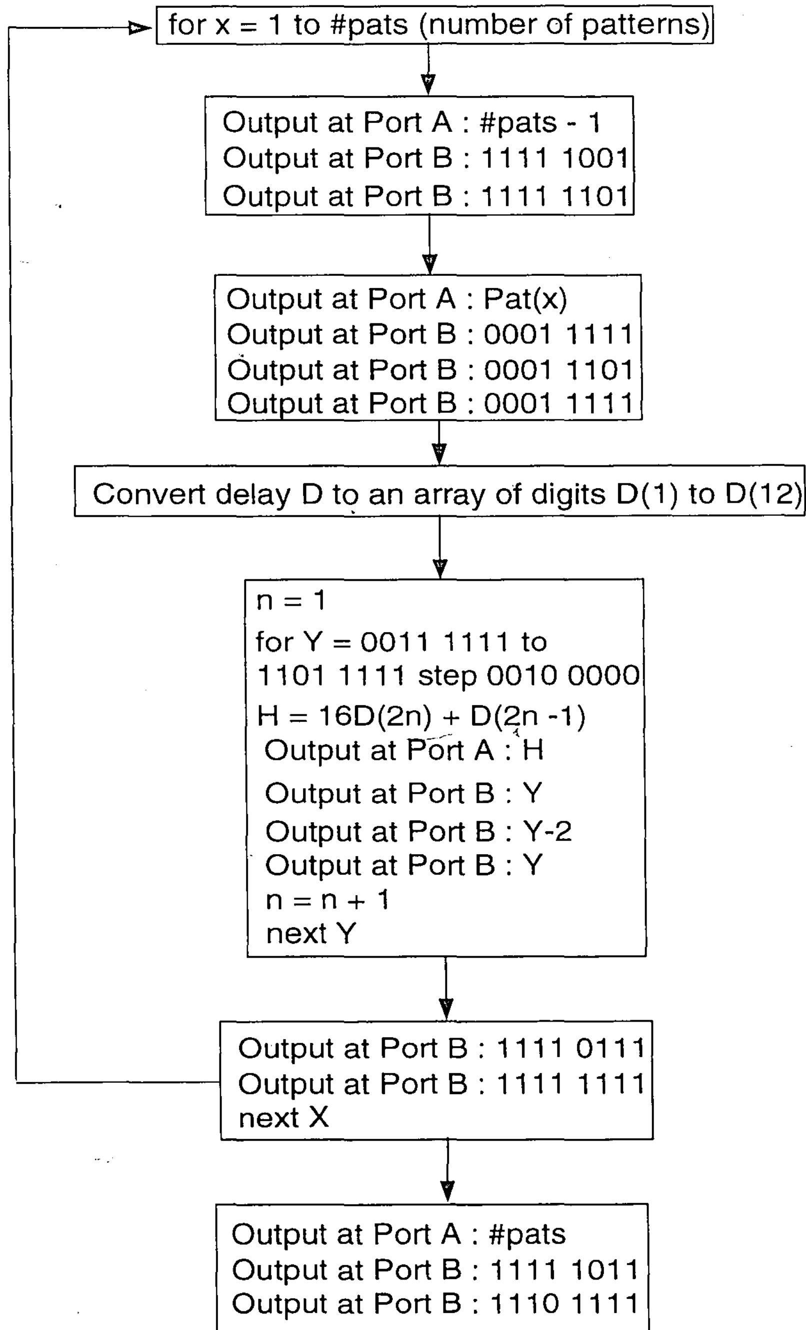


Figure B.2: The flowchart of the programming of the Pattern Generator explicitly showing the code sequence used.

| | |
|---|---|
| 0000 0010 | IDLE |
| 0000 0011 | ERASE |
| 0000 0110 | WRITE |
| 0001 0010 | READ DELAY |
| 0001 1000 | READ |

Figure B.3: The basic operations and their patterns

facility. This expands the signal within the boundaries and performs gated measurements.

- Trigger channel is selected and the triggering level is set to 3V or TTL as a TTL compatible trigger synchronous with the Read pulse is available (Check the connection from the trigger output to the oscilloscope.) and the slope as positive or rising edge.
- Activate the required automated measurement facilities of the oscilloscope.

4. Wait for the oscilloscope to trigger and acquire waveform. A window with a smaller time base is placed on the waveform at a time interval after the Read pulse to let avoid measurements in the transient region. Confirm window position from operator and note corrected window position. Window the ground level of the waveform and follow the same procedure.

5. Wait for oscilloscope to acquire fresh waveform. Obtain from oscilloscope information regarding the minimum, maximum and average of the signal within

the windowed area. The oscilloscope has automated measurement capabilities.

6. If there is a difference between the minimum and maximum values of the waveform within any of the two windows exceeds the noise threshold, then discard data and wait for fresh acquisition.

7. Otherwise, subtract the average value in the first window from the average ground level obtained from the second window and store and print it as the threshold voltage of the device for the particular erase, write and idle times used.

8. Goto step 5 and record measured data for the number of repeats. Then, increment the delay to be varied by the increment specified and go back to step 5.

9. Repeat procedure till the increment limit is reached. Reset the Pattern Generator. This is important to prevent unnecessary cycling of the device.

# Vitae

While Pink Floyd was rocking and the Beatles were rolling, Amit Kumar Banerjee was born in Dhanbad, India on November 14, 1966 to Mr. Anil Kumar Banerjee and Mrs. Monikuntala Banerjee. He joined the Motilal Nehru Regional Engineering College, Allahabad in 1985 and graduated with a Bachelor of Engineering degree in Electronics Engineering in 1989. He decided to embark on a career in research and academics when, even as an undergraduate, his work with Prof. Raj Senani, on Operational Transconductance Amplifiers, lead to his first publication. He continued working with Prof. Senani and helped in developing the laboratories of the Delhi Institute of Technology, Delhi while working there from 1989. He joined Lehigh University in the Spring of 1991 and is currently working towards his Ph.D. degree. He lives in Bethlehem with his wife, Savita, a Ph.D. student herself.

He is a recipient of Graduate Fellowship from Lehigh University and has written several research papers.

END

OF

TITLE