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Retention reliability in polysilicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile semiconductor memory devices

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Retention Reliability in Polysilicon-Oxide-Nitride-Oxide-Silicon (SONOS) Nonvolatile Semiconductor Memory Devices

by

Stephen J. Wrazien

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Chairman of Department

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This thesis is dedicated to all of you.

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Abstract

The need for radiation hard nonvolatile memory devices for use in applications such as NASA space missions, military and commercial satellites, and cellular phones has presented a great opportunity for Polysilicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile memory devices. Recent NASA space missions have demanded a level of radiation hardness not offered by conventional memory devices.

Since the advent of the nonvolatile MNOS semiconductor memory in 1967, there have been a wide variety of roles for nitride-based nonvolatile memory structures. Researchers at Northrop Grumman and Westinghouse Corporations have been involved in this work from almost its inception. Northrop Grumman has been working with Sandia National Laboratories and Lehigh University in order to refine this technology for use in applications such as satellites and automobiles. Our work focuses on the characterization of thermal acceleration effects with a goal of establishing a screening procedure to guarantee 10-year memory retention at 80 C.

SONOS memory devices have been used for several years in smart cards and satellites. Smart cards are in use extensively in Europe, and use a tiny chip with a nonvolatile memory, which can be written and erased at low voltages to store data for up to 10 years. The nonvolatile memory in smart cards can be utilized to store authentication data such as a picture, fingerprint, or other data to verify the identity of the person using the card or the authenticity of the card itself. SONOS 64k EEPROMs have been used in several satellite applications since 1992.

In this thesis we utilize the thermal excitation of electrons from traps located in the oxynitride charge storage layer in order to profile the energetic distribution of these traps. This thesis verifies the superior quality of SONOS memory devices fabricated with oxygen-rich oxynitride layers over devices fabricated with silicon-rich nitride layers. We verify the presence of an acceleration factor, which demonstrates the dependence of charge loss on temperature. This allows us to perform measurements at elevated temperatures over short periods of time in order to guarantee the memory retention of devices at lower temperatures over greater periods of time.

Chapter 1

Introduction

There are two types of Electrically-Erasable-Programmable-Read-Only-Memories (EEPROM's); floating gate devices and floating trap SONOS devices [4]. The floating gate device stores charge in a polysilicon gate electrode as free carriers with a continuous spatial distribution in the conduction band. The SONOS (Polysilicon-Oxide-Nitride-Oxide-Silicon) device stores charge in spatially isolated deep level traps (see Fig. 1.1).

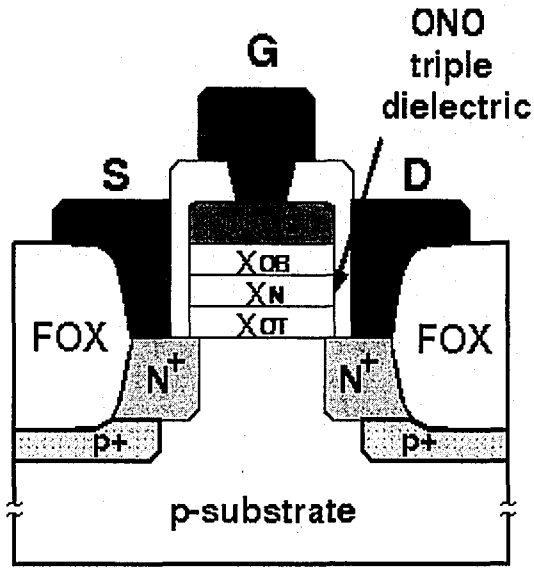

Figure 1.1 - The cross section of SONOS device structure [8].

Several characteristics of EEPROM devices include retention, endurance, and programming speed. Retention refers to the ability of the device to store and recover charge from the nitride layer after a number of write and erase cycles at a specific temperature. Endurance refers to the ability of a device to withstand repeated write and

erase cycles and still be able to retain and recover charge. Programming speed refers to the time duration of the programming voltage applied to the gate required to switch the device from the write to the erase state, or vice versa.

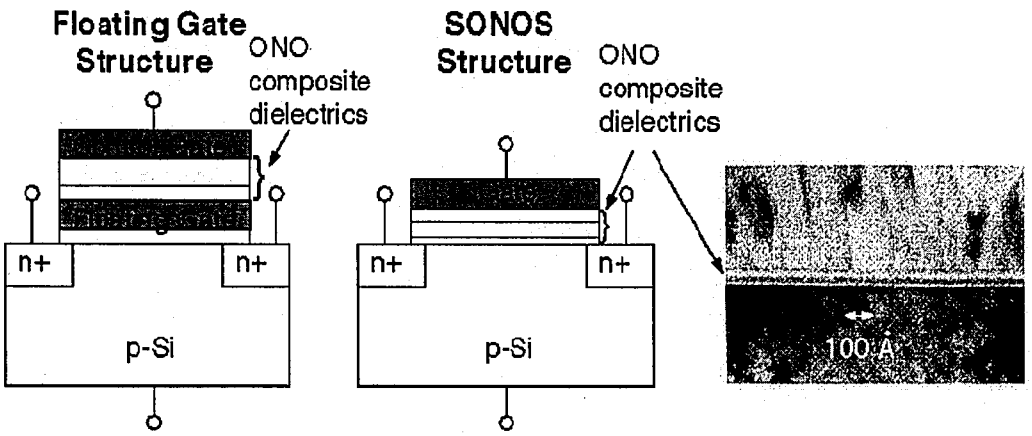

Figure 1.2 – Floating Gate versus SONOS Device Structures [6].

The requirements for future non-volatile memory devices are; endurances of 10^6 erase/write cycles, 10-year charge retention at 85 C, 5V or less programming voltage, [7]. The main barrier to meeting these goals is the challenge of achieving low power and low voltage programming while retaining speed and retention duration. The NVSM program and erase voltages currently are not compatible with aggressively scaled low-voltage CMOS devices. This makes design optimization a daunting task. Future projections predict scaled polysilicon devices as having 7 nm tunnel oxides with scaled programming voltages to produce electric fields in excess of 10 MV/cm. Today's designs for the future utilize high-voltage generating charge-pump circuits, which are difficult to integrate in device layout with memory arrays, which degrades array efficiency. High voltage devices also require additional fabrication steps and reduced yield in manufacturing high-

density NVSM's [8].

Field Programmable Gate Array (FPGA) based measurements have been used for several years to characterize the operation of SONOS nonvolatile memory devices. FPGA setups allow the user to design cost-effective test patterns, which are highly flexible since the hardware is implemented in software, fast read of the memory state, low power, high precision, and minimal disturbance of the device under test (DUT) [6].

Several different types of nonvolatile memories have stood out in the search for a technology compatible with the demands of operation in outer space. Ferroelectric RAM (FRAM) uses high currents to orient the magnetic direction of a tiny strip of magnetic material, which alters the resistance of the strip. The two magnetic directions correspond with logic one or zero [2].

The newcomers to the nonvolatile memory device scene, Nanocrystal, MRAM, and Ferroelectric technologies, suffer from the exotic nature of the materials which make are essential for their operation. Producing MRAM and Ferroelectric memories in existing fabrication facilities would contaminate the furnaces and machinery with elements such as Nickel (Ni), Iron (Fe), Cobalt (Co), and Manganese (Mn). The NROM technology seems to be the most promising of the newer technologies to hit the NVSM scene. However, this technology is very new and the research that has been conducted on NROM's is rather limited at this point. Future research should reveal whether NROM technology could be a reliable NVSM technology for the future. It is predicted that in around 5 years we should see the NROM devices on the market [3].

1.1 Floating Gate vs. SONOS

Floating gate memory, the traditional choice for many memory-intensive applications, has several major limitations with respect to cell size scaling and programming voltage [8]. Fig. 1.3 demonstrates the program (a) and erase (b) operations of floating gate devices.

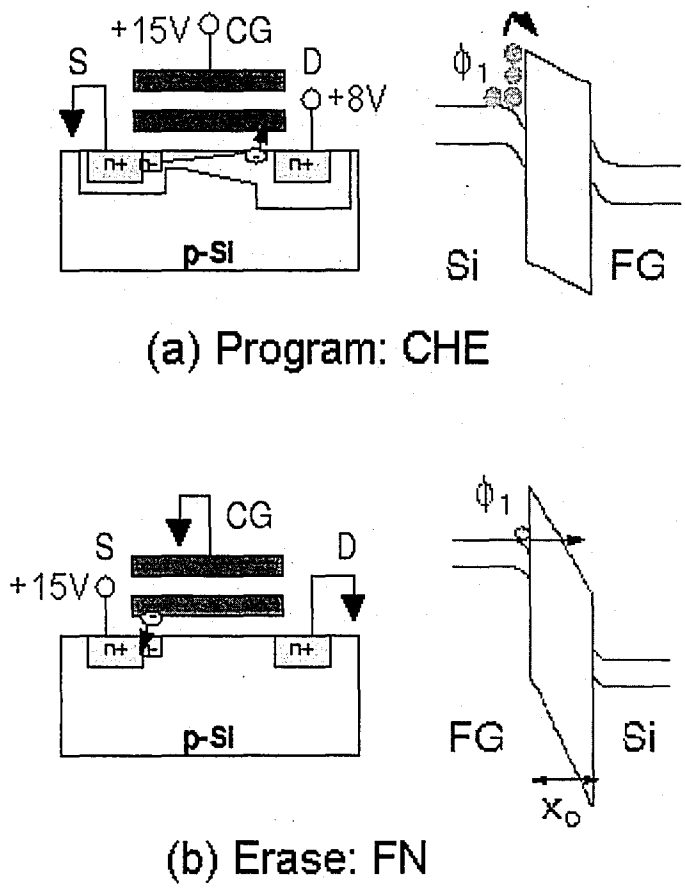

Figure 1.3 - Program/erase mechanisms of mainstream flash technologies. a) CHE for programming operation and the energy-band diagram, b) FN for erase operation and the energy-band diagram [6].

Channel Hot Electron (CHE) injection is employed for programming. Fowler Nordheim (FN) tunneling is employed for erasing the device. Applying a large lateral field along

the channel of the devices causes electrons to accelerate until they are scattered by the lattice or another carrier. The appropriate vertical field will result in "lucky" electrons, which will accumulate enough energy to cross the Si-SiO_2 barrier and inject themselves into the gate dielectric where they are stored in traps. The Carrier Hot Electron (CHE) current is defined by Tam using the equation

$$I_g = A_G E_{vertical} I_{ds} e^{-\frac{\phi_1}{\lambda_S E_{lateral}(\max)}} \quad (1\text{-}1)$$

where λ_s is the electron mean free path in silicon, A_G is the gate area, $E_{vertical}$ is the electric field in the ate dielectric, ϕ_1 is the Si-SiO_2 barrier potential, and $E_{lateral}(max)$ is the maximum electric field in the vicinity of the drain junction [9]. The following points break down the fundamental differences between the SONOS and Floating Gate technologies [6].

1) In memory operations, SONOS devices employ both electrons and holes. Floating gate devices use only electrons.
2) SONOS has a simpler structure because it only has one gate with one composite dielectric. Floating gate consists of two floating gates and two dielectrics (oxide and composite).
3) SONOS gate voltage is directly controlled. Floating gate voltage is capacitively coupled from the control gate.
4) SONOS structure is linearly scalable with programming voltage. Floating gate structure is not easily scaled.
5) SONOS structures are immune to single defect memory loss because charge is

stored in traps distributed throughout the dielectric. Floating gate structures are susceptible to single defect memory loss where a single defect in the tunnel oxide allows free charge to escape into the bulk.

6) Floating gate has thicker tunnel oxide than SONOS devices, generally around the range of 7-10 nm. This leads to better retention for floating gate devices at the expense of higher programming voltages.
7) SONOS devices operate with reduced electric fields in the tunnel oxide (Modified Fowler-Nordheim and Direct tunneling) as opposed to floating gate devices which use exclusively Fowler-Nordheim tunneling.

1.2 SONOS Device Structure and Operation

The acronym, Polysilicon-Oxide-Nitride-Oxide-Silicon (SONOS) is derived from the structure of the device. The SONOS device is basically a MOSFET (Metal-Oxide-Silicon-Field-Effect-Transistor) where the gate has been replaced by an ONO (Oxide-Nitride-Oxide) dielectric. Charge, holes or electrons, are injected into the nitride layer using direct tunneling through the tunnel oxide layer.

In our studies, SONOS nonvolatile memory devices are fabricated with a gate dielectric consisting of an 18 Å tunneling oxide, 80 Å "oxynitride" layer, and a 40 Å 'blocking' oxide underneath a phosphorus-doped polysilicon gate [5]. The gate dielectric is programmed by applying either +7 V to the gate terminal for 2.5 msec, or a –7 V pulse for 7.5 msec. The applied voltage attracts electrons or holes to the surface of the silicon depending on the polarity of the gate voltage [10].

Chapter 2

Device Reliability

2.1 Floating Gate Reliability

Charge decay mechanisms and endurance failure losses vary for different structures and types of memory devices. In Floating Gate Tunnel Oxide structures (FLOTOX), there are two mechanisms responsible for charge decay; charge loss by enhanced tunneling due to the barrier lowering at polysilicon asperities and charge loss due to thermal excitation [12,13]. Charge leakages in FLOTOX devices (Fig. 2.1) can occur due to back-tunneling of charge through the tunnel oxide to the substrate or thermal excitation of charge from traps in the nitride [14,15].

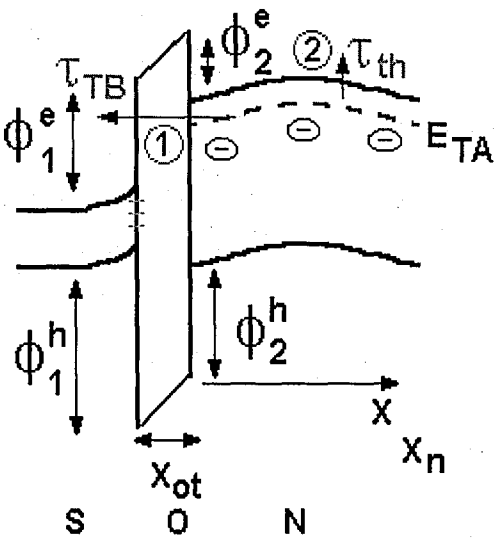

Figure 2.1 – Charge loss mechanisms in FLOTOX devices [6].

For a small number of erase/write cycles, the electric field at the injection

interface is enhanced by the hole trapping in the tunnel oxide, leading to an enlarged memory window. During each cycle, electrons pass through the tunnel oxide and traps located in the oxide capture some of these electrons. At the same time, under high local electric fields, more electron traps are generated in the oxide by dislodging electrons from covalent Si-SiO_2 bonds. As the number of erase/write cycles increases, more electrons are trapped in the oxide until the electron trapping outweighs the hole trapping. The net charge in the oxide causes a reduction in the injection field and inhibits further tunneling and CHE injection [16].

2.2 SONOS Reliability

The reliability characteristics of SONOS devices are different from those of floating gate devices. The erase/write cycling causes little charge trapping in the tunnel oxide because the tunnel oxide thickness is smaller than the mean free path of the carriers [9]. Although charge trapping will not occur in the tunnel oxide due to cycling, it will generate interface traps and deteriorate the nitride integrity. This causes a continuous reduction of data retention for SONOS structures due to their thin tunnel oxide. Another loss mechanism is stored charge back tunneling from the nitride to the silicon substrate under the influence of the internal field. Data retention, at room and elevated temperatures will be discussed in depth in the following sections of this thesis.

2.3 Retention Models for SONOS Devices

2.3.1 Historical Perspective

Since the invention of the nitride based memory structure in 1967 [17], there has been a great deal of experimental and analytical work focusing on understanding the data retention characteristics and the charge loss mechanisms. The following is a summary of charge decay mechanisms in MNOS and SONOS devices proposed in the literature [6]:

1) Lundkvist *et al.* [18] have modeled the charge decay behavior of MNOS transistors at room temperature as back tunneling of trapped charge stored in the nitride. The charge in the nitride is assumed to be stored in an area extending from the oxide-nitride interface to about 10 nm into the nitride. This trapped charge tunnels through the tunnel oxide to the silicon substrate due to the internal field present in the retention mode.
2) In order to describe the increased rate of loss of charge at elevated temperatures, Lundkvist *et al.* [19] proposed that the thermal emission of trapped charges from the nitride is another path of charge decay. It is assumed that the nitride traps are continuously distributed in energy from depth ϕ_{min} to ϕ_{max} in this model.
3) Lehovec *et al.* [20] assumed that the retention mode loss is limited by the nitride conduction through Poole-Frenkel detrapping. Using this assumption, a simple analytical expression for charge retention in MNOS devices was derived. A mono-energetic trap model was used in their work. Using a numerical data fit for the results, at a trap depth of 1.5 eV, a Poole-Frenkel coefficient of about 6×10^{-4} $cm^{1/2}V^{-1/2}eV$ and an effective escape attempt rate factor of 1.2×10^{8} sec^{-1} were

calculated.

4) Trap-assisted charge injection was revealed as a major factor in MNOS [21] and SONOS [22] device operations, particularly for thin tunnel oxides at low fields (1-4 MV/cm). Charge tunnels through part of the nitride and the entire thickness of the oxide using a nitride trap as a "stepping stone". It has been revealed that these traps are shallow and are not the same as the traps responsible for charge storage in the nitride, which are much deeper in the nitride.

5) White *et al.* [23] have explained the charge retention for thin-oxide MNOS memory transistors in terms of the direct tunneling of charges from traps in the nitride to the Si-SiO_2 interface states. · A mono-energetic donor and acceptor trap level, localized spatially at the nitride-oxide interface, was considered. They observed a slower rate of charge loss to acceptor Si-SiO_2 interface states as compared with donor Si-SiO_2 interface states. This is interpreted as a result of a larger increase in acceptor interface states near the conduction band edge as compared with donor interface states near the valence band edge.

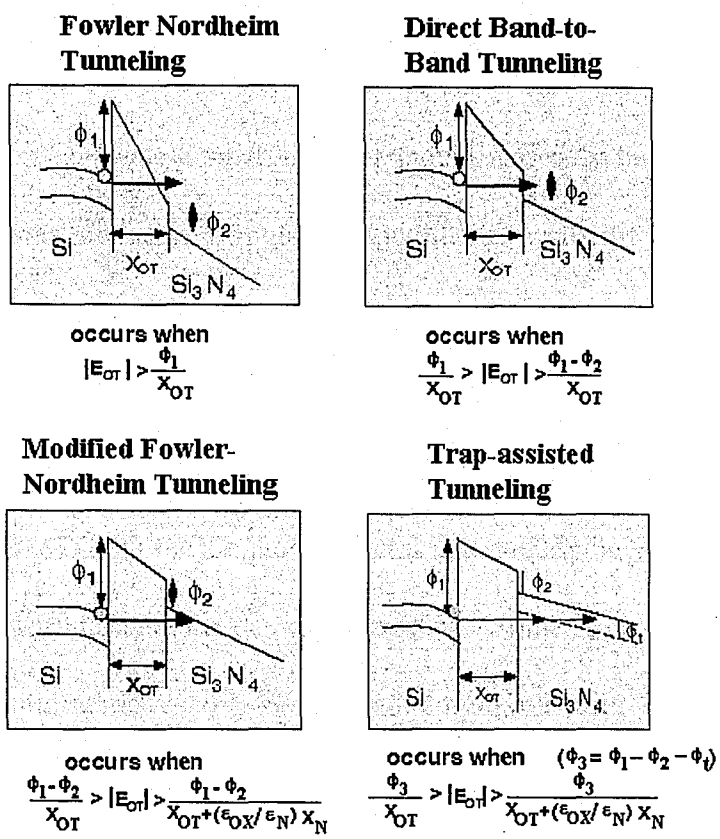

Figure 2.2 - Energy band diagrams and tunnel oxide electric field requirements for FN, DT, MFN and TAT tunneling mechanisms [8].

2.3.2 Effect of Temperature in Charge Decay

There have been contradictory findings published regarding the effect of temperature on charge decay in MNOS devices. One of the first reports showed the charge retention was independent of temperature between 25 C and 125 C [24]. A later report by Kim *et al.* [25] supported this finding. However, Lundkvist *et al.* [19] investigated the data retention within the temperature range of 24 C to 300 C and observed an increased discharge rate with increased temperature for both holes and electrons. It was concluded that the increased discharge rate was a result of thermal emission of trapped charge.

Woods *et al.* [26] noted that MNOS charge retention degraded with erase/write cycles as the operating temperature was increased. Neugebauer *et al.* [27] concluded that the charge injection process was temperature dependent and only the discharge rate of the excess hole state was increased at higher temperatures. Williams *et al.* [28] conducted a study indicating that only the discharge rate of the excess electron state was temperature dependent.

The majority of these studies were conducted on p-channel MNOS structures fabricated with an APCVD nitride and Al metal gate technology. However, there were still considerable variations in the device processing. Some structures used a thick oxide of about 50 Å, while others used a thinner tunneling oxide with a thickness of 15-35 Å. Some oxide films were formed by wet oxidation, dry oxidation, or immersion in boiling concentrated nitric acid. There were also many variations in the nitride thickness and deposition conditions. These differences, pointed out by Almeida *et al.* [29], gave rise to the variety and range of results and observations made regarding the effect of temperature on data retention [6].

2.3.3 Stress – Erase/Write Cycling

One of the methods used to determine the quality of the SONOS device and its long-term operation is stressing the device by performing a write and an erase on the device. The write and erase times are determined by the user, a 7.5 msec at 7V write and 2.5 msec at -7V erase is used with Northrop Grumman devices. The write and erase stressing of the devices is used to determine how the device will hold up after it has been

used for extended periods. When the device is programmed and erased, holes and electrons tunnel through the oxide of the device, and often disrupt the covalent bonds between silicon and oxygen atoms in the oxide layer, forming traps. As more electrons and holes tunnel, more traps, dangling bonds, will be created in the oxide of the device.

When the device is in written or erased, and is in the retention mode (all terminals connected to ground), charge from the nitride will leak out through the oxide with assistance from interface traps. Electrons and holes will tunnel through the oxide barrier to these traps at the interface and then they will continue into the silicon. As the device is stressed, the charge will leave at an increased rate, which can be seen during the retention measurement. The density of traps in the interface can be measured as D_{it} [6].

2.4 SONOS Device Fabrication

The step-by-step process of SONOS device fabrication at the Sherman Fairchild Micro-Electronics Lab is outlined in Appendix C. This section is an overview of several optimizations that must be taken into consideration in order to fabricate reliable SONOS devices. Yang *et al.* [30] conducted studies on nitride films, which were deposited at different temperatures. These studies concluded the optimum temperature for Low-Pressure-Chemical-Vapor-Deposition (LPCVD) nitride deposition for a minimum surface roughness is 680 C. Minami *et al.* [31] demonstrated that using LPCVD to form blocking oxides improved memory retention dramatically. They also demonstrated that the tunnel oxides grown at high temperature exhibit improved performance and reliability [32]. Improved retention and endurance can be obtained by using a triple-wall oxidation

furnace in place of the conventional single-wall furnace [33,34].

During LPCVD nitride deposition, Silicon dangling bonds create deep level traps in the nitride layer. The number of traps can be reduced using oxygen and hydrogen atoms as terminators for dangling bonds [8]. Trap-rich nitrides facilitate fast programming speeds [35]. An oxygen-rich nitride layer, oxynitride, can be used for improved retention and endurance [36].

Chapter 3

SONOS Device Measurements

The majority of the measurements performed on SONOS devices are the same measurements, which are performed on conventional MNOS devices. This includes the Linear Voltage Ramp (LVR), Stressing, and Charge Pumping measurements. These measurements test the quality of the device as a transistor, and can quantify the durability of the device over an extended period of use. In addition to these measurements, the memory properties of the device must be tested using the Erase/Write, Retention, and Stressing measurements. These tests will determine how well the device retains charge under extreme use and over time.

3.1 MNOS/SONOS TESTS

3.1.1 LabVIEW™

All of the measurements presented in this thesis are performed with the aid of a computer program called LabVIEW™. LabVIEW™ is a software platform developed by National Instruments. The LabVIEW™ environment utilizes a graphical programming language to control test equipment, such as oscilloscopes, electrometers, and function generators. Communication between the computer and the measurement devices is accomplished through a GPIB cable connected to the device and the printer port of the computer. LabVIEW™ can simultaneously set up several devices for a measurement. LabVIEW™ allows data to be sent back to the computer through the GPIB interface,

where it can be displayed on the computer screen and written to a file.

3.1.2 Linear Voltage Ramp (LVR)

The Linear Voltage Ramp measurement is a quasi-static C-V measurement used to determine the effective thickness of the ONO dielectric in a SONOS device. The standard LVR setup, Fig. 3.1, involves connecting the source and drain together and tying them to the bulk. A function generator, controlled by a PC using LabVIEW™, sends a ramping voltage to the bulk of the device.

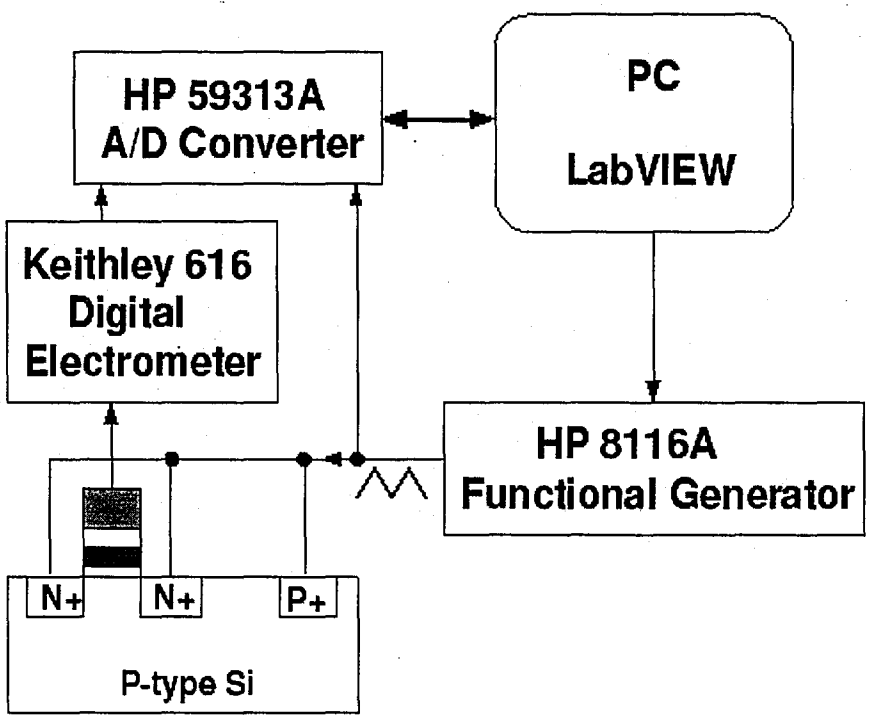

Figure 3.1 - Linear Voltage Ramp Setup [6].

The gate current is measured using an electrometer, which is controlled by a PC using LabVIEW™. The ramping voltage can be written as

$$Vgb = V_0 \pm \alpha t \tag{3-1}$$

where V_O is a DC voltage level. The measured gate current is given by

$$I_g = \frac{\partial Q_g}{\partial t} A_G = \frac{\partial Q_g}{\partial V_{gb}} \frac{dV_{gb}}{\partial t} A_G = \alpha C_{eff} A_G = \alpha \frac{\varepsilon_{ox}}{X_{eff}} A_G \qquad (3\text{-}2)$$

where $x_{eff} = x_{OT} + x_{OB} + \frac{\varepsilon_{OX}}{\varepsilon_N} x_N$ is the effective thickness of the ONO dielectric, ε_{OX} is the oxide permitivity, and A_G is the area of the gate.

The LVR measurement can be used to examine the static memory window of a SONOS device. The voltage ramp starts at a positive value where the semiconductor surface is in accumulation. The nitride traps are filled with holes. Sweeping the bulk voltage from a positive to a negative value causes the surface of the semiconductor to go from accumulation to inversion. As the surface goes to inversion, electrons are injected and trapped in the nitride. This shifts the flatband voltage negatively. Figure 3.2 shows the result of an LVR measurement on a SONOS capacitor on an N+ gridded p-type wafer, where V_{GB} is the horizontal axis.

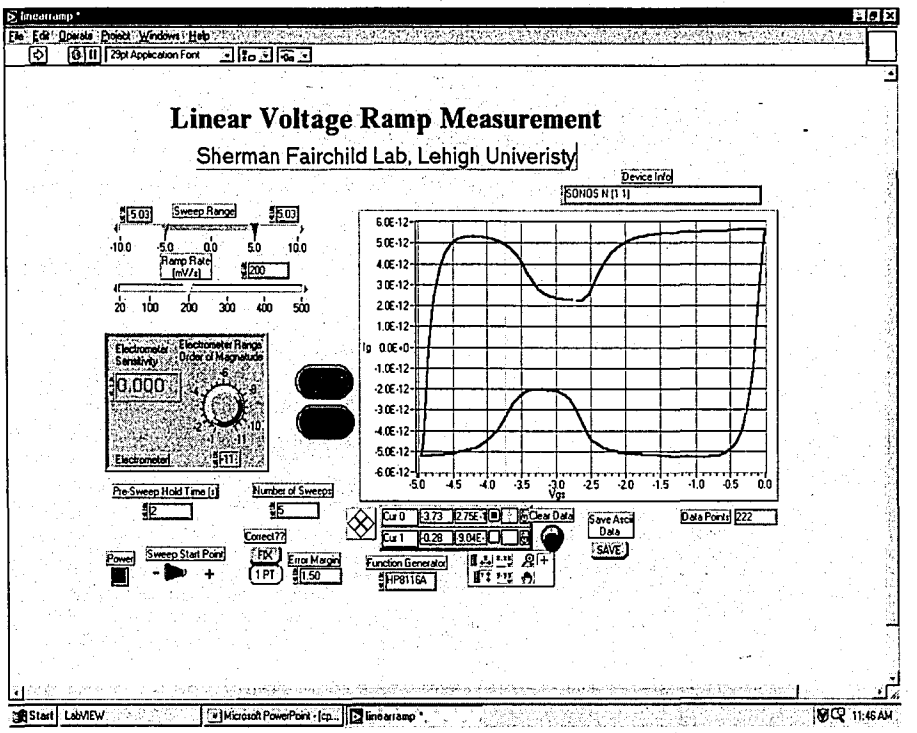

Figure 3.2 - Front panel of LVR measurement program [8].

This measurement was performed at a ramp rate of 200 mV/s. From the experimental data collected, the effective oxide thickness is extrapolated as 81 Å. Ellipsometry has shown the device oxide thickness as 79 Å, which agrees with this experimental result. The device static memory window is extrapolated as 2.5 V for a programming voltage of 4 V [6].

3.1.3 Charge Pumping

The charge pumping measurement is a widely accepted and utilized technique used to measure the interface trap parameters in MOS devices [6]. This technique is utilized on SONOS devices to measure the interface trap density before and after the device has been erased and written. Figure 3.3 demonstrates a bit-level charge pumping

setup where a SONOS device is connected in a dated diode configuration by shorting the drain and source together. A function generator is used to apply a pulse to the gate of the device, which drives the transistor surface repetitively from accumulation to inversion. The interface traps serve as recombination centers. A net recombination current is measured at the drain/source terminal.

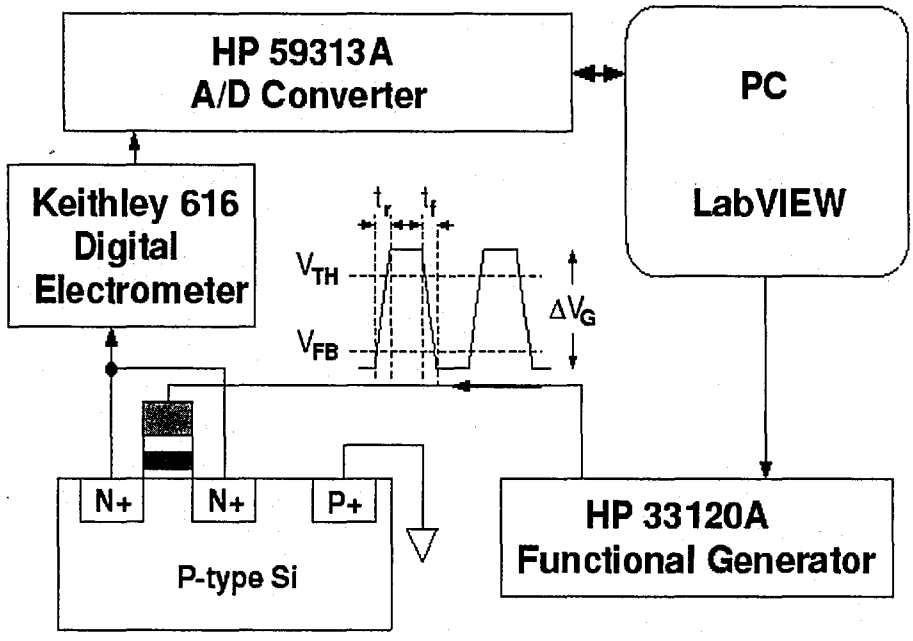

Figure 3.3 - Charge pumping setup [6].

The substrate current, I_{cp}, is proportional to the mean density of interface traps, D_{it}, and the frequency of the pumping pulse, f, shown in the following equation [37]

$$I_{cp} = 2qD_{it}fA_g kT \ln\left[v_{th} n_i \left| \frac{V_{FB} - V_{TH}}{\Delta V_G} \right| \sqrt{\sigma_n \sigma_p t_r t_f} \right] \qquad (3\text{-}3)$$

where A_G is the area of the gate, v_{TH} is the thermal velocity of the carriers, σ_n and σ_p are the capture cross sections for electrons and holes, V_{FB} and V_{TH} are the flatband and

threshold voltages of the device, ΔV_G, t_r, and t_f are the amplitude, rise time, and fall time of the pulse applied to the gate, respectively. Using this technique, the pumping current I_{cp} is measured and the interface trap density D_{it} is extracted [6].

The charge pumping measurement usually utilizes an applied pulse with a frequency in the range of 100 KHz to 1 MHz. At these frequencies, only the interface traps within 10 Å of the Si-SiO_2 interface can respond and contribute to the charge pumping current. However, if the frequency of the applied pulse decreases, the trapped carriers at the interface will have enough time to communicate with the Near-Interface-Oxide-Traps (NIOT's). Variable frequency charge pumping involves monitoring the charge pumping current over a wide range of gate pulse frequencies [38]. A plot of the charge pumped per cycle, Q_{cp}, versus the gate pulse frequency is shown in figure 3.4. This figure demonstrates how the charge pumped remains constant at high frequencies.

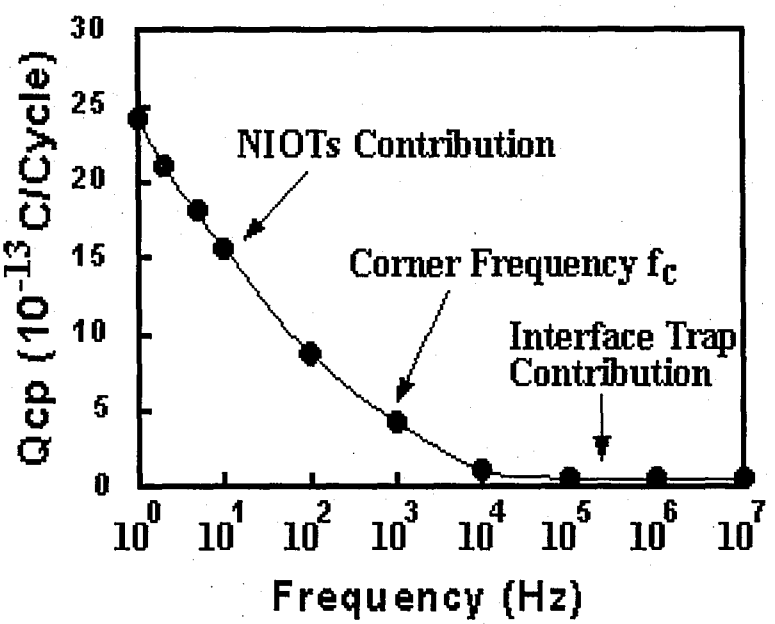

Figure 3.4 - The recombined charge per cycle Q_{cp} as a function of frequency for a thin tunnel oxide SONOS device (W=100um L=8um). The increase in Q_{cp} at low frequency is attributed to an additional charge pumping current associated with nitride traps, which are

only 1.5 nm away from the Si-SiO_2 interface [38].

As the frequency is decreased, Q_{cp} will increase due to the contribution of the NIOT's. The contribution of mono-energetically distributed NIOT's to the charge pumping per cycle, Q_{cp} (NIOT), is given by [39]

$$Q_{cp}(NIOT) = qA_g \int_{x_{min}}^{x_m(f)} dx N_T(x)[1 - e^{-\frac{1}{2\tau_{TT}(E_{TO},x)}}] \qquad (3\text{-}4)$$

where

$$\tau_{TT}(E_{TO}, x) = \frac{(m^*_{ox,e})^2 x(1+\frac{1}{2\kappa_1 x})}{2\pi^2 \kappa_2 \hbar^3 D_{it}} e^{2\kappa_1 x} \approx \tau_0 e^{2\kappa_1 x} \qquad (3\text{-}5)$$

is the trap-to-trap tunneling time constant used to describe the carrier tunneling phenomenon between interface traps and NIOT's, τ_0 is inversely proportional to D_{it} and is weakly dependent on x, $N_T(x)$ is the spatial trap density of NIOT's, x_{min} is the minimum distance at which a NIOT is distinguishable from an interface trap, $x_m(f) = -\ln(2\ln 2) f\tau_0/2\kappa$ is the maximum distance into the oxide at which a gate pulse with a frequency f can probe, $\hbar$ is the reduced Planck's constant, D_{it} is an averaged density of interface traps, and the parameters κ_1 and κ_2 are the attenuation coefficients in the oxide and semiconductor, $m_{ox,e}$ and $m_{si,e}$ are the effective masses of an electron in the oxide and semiconductor, respectively. Using the slope of the experimental curve (Fig. 3.4), the density of NIOT's

at the maximum tunneling distance x_m can be determined.

$$N_T(x_m) \approx \frac{2\kappa}{2.3qA_G}\left(-\frac{\partial Q_{cp}}{\partial \log f}\right) \tag{3-6}$$

Variations of the gate pulse frequency, f, allows a determination of the spatial distribution of NIOT's [6].

3.2 SONOS Measurements

3.2.1 Erase/Write

Applying a voltage to the gate of a SONOS device can alter the threshold voltage of the device. The transient behavior of a SONOS device is a function of the polarity, amplitude, and duration of the gate voltage pulse. The Erase/Write measurement is the measure of the programming speed of a device. The greater the amplitude of the applied voltage pulse, the quicker the device will erase or write. The typical voltage pulse duration is in the range of 1 ms to 10 ms. The erase pulse will sometimes be longer if a block or page erase system is utilized.

The shift in the threshold voltage during an erase/write operation is due to the charge injection and trapping in the nitride film. In the operation of SONOS devices, charge injection is governed by tunneling processes, which are strong functions of the electric fields in a device. This makes the amplitude of the applied programming voltage and the amount of the initial nitride charge important in determining the speed of a

SONOS memory transistor. Assuming the Modified Fowler-Nordheim (MFN) tunneling is the dominant charge injection mechanism in the operation of a SONOS device, French *et al.* [22] derived an expression to describe the dependence of the threshold voltage change on these parameters

$$\Delta V_{TH}(V_P,t_p) = \frac{x_{eff}}{E_T}\left[\frac{V_p + \left(\frac{x_{OB}}{\varepsilon_{ox}} + \frac{x_N - \bar{x}}{\varepsilon_N}\right)Q_N(0) - \phi_{GS} - \phi_S}{Xeff}\right]^2 \ln\left(1+\frac{t_p}{\tau}\right) \qquad (3\text{-}7)$$

where $x_{eff} = x_{OT} + x_N\left(\frac{\varepsilon_{ox}}{\varepsilon_n}\right) + x_{OB}$ is the effective thickness of the stacked dielectrics, $\bar{x}$ is the charge centroid in the nitride film, E_T, V_p, t_p are the magnitude and duration of the programming pulse, $Q_N(0)$ is the initial charge stored in the nitride, ϕ_{GS} is the gate-semiconductor work function difference, ϕ_S is the surface potential, and τ is the turn-on time, respectively.

The programming time, t_p, is specified by customers or applications, typically in the range of 1 ms to 10 ms for writing for writing, and 10 ms to 100 ms for erasing. For a fixed tp, the dependence of the threshold change on the programming voltage can be described by the differentiation of Eq. 3-7 with respect to Vp

$$\frac{\partial \Delta V_{TH}}{\partial V_p} = 1 - \frac{\tau}{t_p} + \frac{2}{E_T}\left[\frac{V_p + \left(\frac{x_{OB}}{\varepsilon_{ox}} + \frac{x_N - \bar{x}}{\varepsilon_N}\right) Q_N(0) - \phi_{GS} - \phi_S}{Xeff}\right] \ln\left(\frac{t_p}{\tau}\right) \approx 1 \qquad (3\text{-}8)$$

where $t_p >> \tau$ is assumed. There is a 1:1 correspondence in the change of the threshold voltage with respect to the programming voltage [6].

The erase/write characteristic for an n-channel SONOS transistor using erase and write voltages of 5, 6, and 7 volts is shown in Fig. 3.5. The transistor has a virgin threshold of 0.2 V. To perform this measurement, the drain, source, and substrate of the device are grounded. To precondition the device, a 10 second pulse is applied to the gate to erase the device. Next, a write pulse, +5 V, +6 V, or +7 V, is applied to the gate of the device. The erase operation is done in the same manner, except the gate voltages used are -5 V, -6 V, and -7 V.

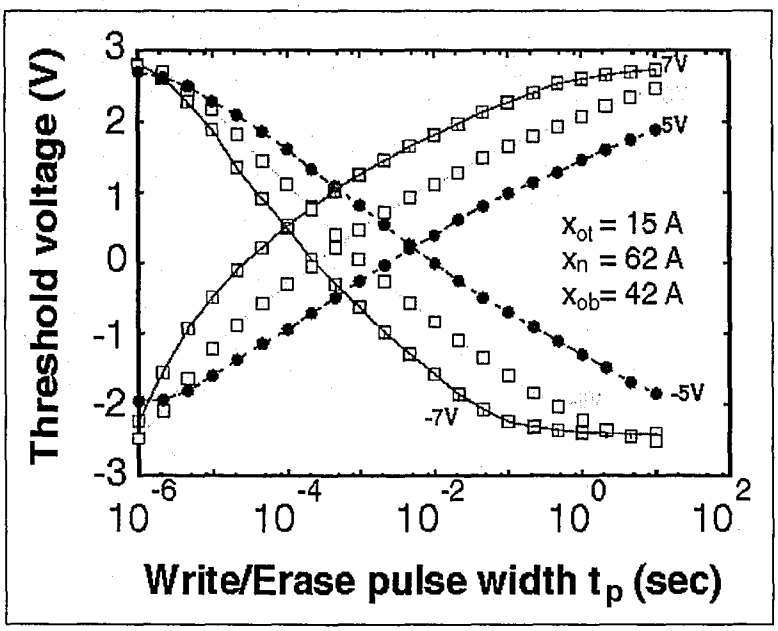

Figure 3.5 – Write/Erase curve for SONOS device performed for programming voltages of 7V (blue), 6V (teal), and 5V (red) [8].

The initial threshold voltages are –2.0 V t –2.5 V for an erased device, and 2.7 V and 2.8 V for a written device. The crossover point where the write and erase curves meet is used to characterize the programming speed of the device at that particular gate voltage. As the programming voltage is increased from 5 to 7 volts, crossover point decreases from 10 ms to 0.1 ms, a rate of 1 decade/V [6].

3.2.2 Retention

Retention measurements are used to characterize the ability of a SONOS device to store data over time. Retention is the most important characteristic for a non-volatile memory device. It is difficult to make a device with fast programming speed, good data retention, high endurance, and low voltage operation. As the tunnel oxide of the device is scaled, the device will have faster programming devices and require lower programming voltages, but will have degraded data retention and endurance.

Data retention measurements are performed at room temperature, 22 C, and 85 C. To perform the retention measurement, the device is written or erased. The read measurement is performed after a specified delay time. The read operation is repeated, and the delay time is increased by an order of 10. This process is repeated for delay times between 10^{-7} seconds to 10^{5} seconds. After the read operation is performed, the data is refreshed. During the delay when the device is in the idle mode, all terminals are grounded. An erase voltage of –7 V and a write voltage of +7 V are used for all retention measurements discussed in this thesis.

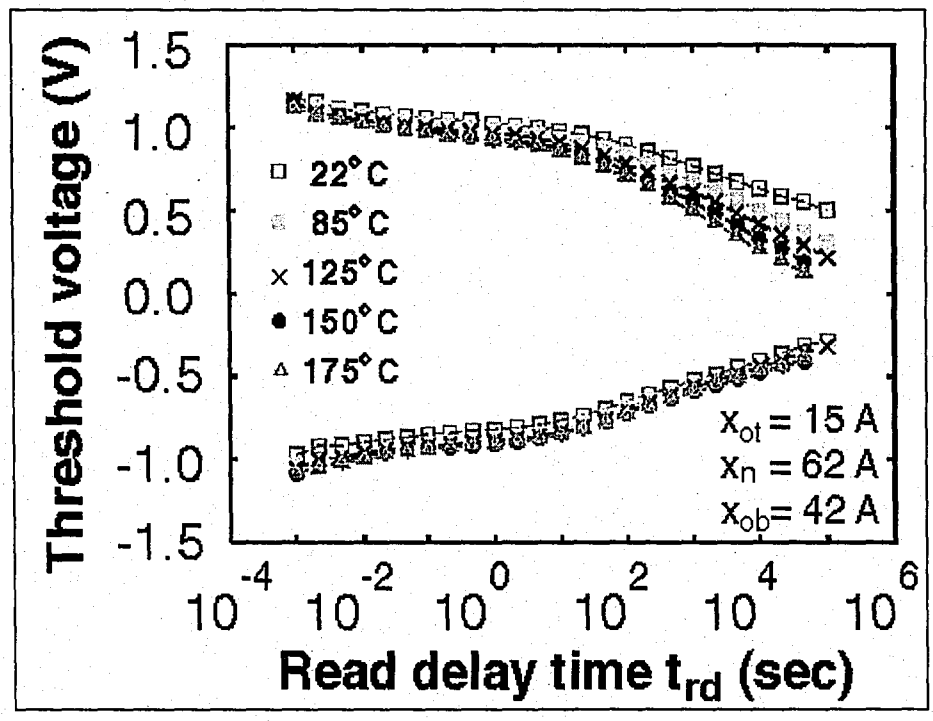

Figure 3.6 – Threshold voltage of a SONOS device versus read delay time for temperatures ranging from 22 C to 175 C [11].

The threshold voltage decay rate is small for short read delay times, up to roughly 1 second. At 1 second, the decay rate increases for both the erased and writing states. The retention measurement can be performed at elevated temperature (Fig. 3.6). There are several effects of temperature on the write state, but not the erase state. Device operation and retention at elevated temperatures is discussed in section 4.3. The retention data can be extrapolated using the last 3 or 4 data points and a straight line fit in order to characterize retention at times up to 10 years. The commercial standard for data retention is a 0.5-volt window at 10 years, at 85 C.

3.2.3 Endurance

Degradation of SONOS device data retention results from subjecting the device to a large number of erase/write cycles [27]. The high field stress a device experiences during erase/write cycling deteriorates the Si-SiO_2 interface and the nitride film. To investigate the effects of erase/write cycling on data retention, the retention characteristic is measured for a virgin device, i.e. without having been previously stressed. The charge pumping measurement is also performed in order to extract an initial interface trap density, D_{it}. The device is then subjected to 10^5 erase write cycles using a write voltage of +7 V for 2.5 ms and -7 V for 7.5 ms. The maximum oxide field reaches a value of roughly 8.5 MV/cm [6].

The retention and charge pumping measurements are performed again. This time, the threshold voltage decay rate for the erased and written states will be greater once the device is stressed. Also, the interface trap density will be greater after the device has been stressed, due to damage to the Si-SiO_2 interface and the nitride as holes and electrons tunnel through the tunnel oxide. The device is then stressed 10^6 cycles and the retention and charge pumping measurements are repeated. Most SONOS devices do not display any degradation after 10^4 erase/write cycles, so the device is only stressed 10^5 and 10^6 cycles. The device is not stressed more than 10^6 cycles since SONOS devices are meant to be programmed and store data over a long period of time, not continuously erased or written like FLASH memories [7].

Chapter 4

Characterization of Scaled SONOS NVSM Devices for Space and Military Applications

We present results on scaled Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile semiconductor memory (NVSM) devices designed specifically for high-density, EEPROM's operating in space and military environments. We describe scaling considerations and process optimization to achieve low-voltage operation (+7V write for 2.5 ms/-7V erase for 7.5 ms) with 10-year retention at 80C. We have conducted studies on 'oxynitride' films at temperatures ranging from 22-250C. An extrapolated 10-year memory window of 1.2V is obtained at 22C reducing to an acceptable 0.8V at 80C. SONOS device trap density profiles are compared for both 'oxynitride' and 'silicon-rich' nitride films.

4.1 Introduction

Since the advent of the nonvolatile MNOS semiconductor memory in 1967 [4], there have been a wide variety of roles for nitride-based nonvolatile memory structures. Researchers at Northrop Grumman and Westinghouse Corporations have been involved in this work from almost its inception [5]. Northrop has been working with Sandia National Laboratories and Lehigh University in order to refine this technology for use in applications, such as satellites and nuclear technology. Our work focuses on the characterization of thermal acceleration effects with a goal of establishing a screening

procedure to guarantee 10-year memory retention at +80 C.

In our studies, SONOS nonvolatile memory devices are fabricated with a gate dielectric consisting of an 18 A tunneling oxide, 80 A "oxynitride" layer, and a 40 A so-called 'blocking' oxide underneath a phosphorus-doped polysilicon gate [5]. The gate dielectric is programmed by applying either +7 V to the gate terminal for 2.5 msec, or a – 7 V pulse for 7.5 msec. The applied voltage attracts electrons or holes to the surface of the silicon depending on the polarity of the gate voltage [10]. Subsequently, these carriers tunnel through an ultra-thin oxide and store in "traps" within a nitride layer. Fig. 4.1 shows the write/erase operation and Fig. 13 the electric field for tunneling.

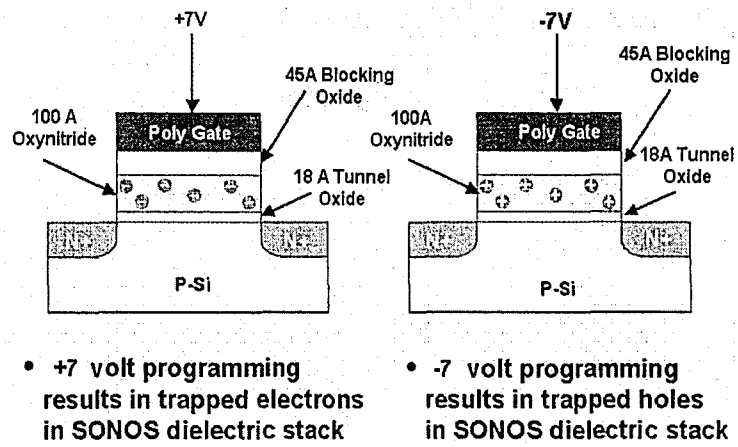

Figure 4.1 – Write/Erase Operation for a SONOS Device.

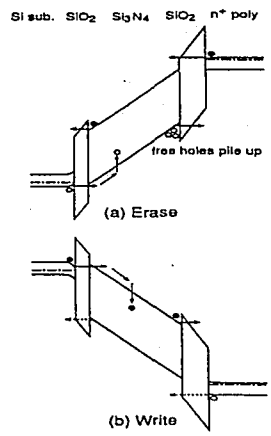

Figure 4.2 – Tunneling in a SONOS Device [10].

4.2 Silicon Rich versus Oxygen Rich "Oxynitride" Layers for Enhanced SONOS Device Performance

In order to achieve improved SONOS device memory performance, especially charge retention, oxygen-rich films called oxynitride (SiO_xN_y) have been used in the fabrication of the devices under test. Kapoor et al. investigated an oxynitride as a storage medium, replacing a silicon-rich nitride layer. The oxynitride film has a lower trap density compared to silicon-rich nitride layers, a result verified in this thesis [46]. Oxynitrides have reduced Coulombic repulsion between the trapped charges. The Coulombic repulsion between trapped charges contributes to these charges coming free from their bonds and creating interface traps, which are used as stepping-stones for charge stored in the nitride to escape to the silicon substrate.

Kapoor et. Al. concluded there was a decrease in interface trap density, which was a function of increased oxygen content in the oxynitride film. Thin oxynitride films have an improved gate dielectric compared to MNOS devices fabricated with silicon nitride films. The addition of oxygen impurities in the oxynitride reduces the traps by compensating the silicon-dangling bonds at the oxide-oxynitride interface and results in a decreased charge decay rate and current conduction and improves the MNOS memory properties [46]. Interface states must be minimal in MNOS memory devices to achieve better device performance such as lower programming voltage, shorter write\erase times, and faster access and read times [47].

4.3 SONOS Retention at Elevated Temperatures - Modeling

The decay of the charge stored in the nitride layer at room temperature has been modeled by a number of investigators, such as White and Cricchi [23], Lundkvist, Lundstrom, Svensson [18], Roy and White [40], Kamagaki and Minami [41,42], and Hu and White [34]. These models invoke back tunneling of charge from the nitride to the semiconductor substrate. An internal field due to trapped charges enhances the process of tunneling.

The characterization of charge trapped in a nitride dielectric at elevated temperatures had been investigated for SNOS devices by Sandia researchers [43,44] and researchers from Chalmers University in Sweden [19]. Recently, with the advent of scaled SONOS devices, Lehigh researchers Yang and White [11] have examined the temperature dependence with an amphoteric trap model, which attributes the electron and hole charge storage to a silicon-dangling bond.

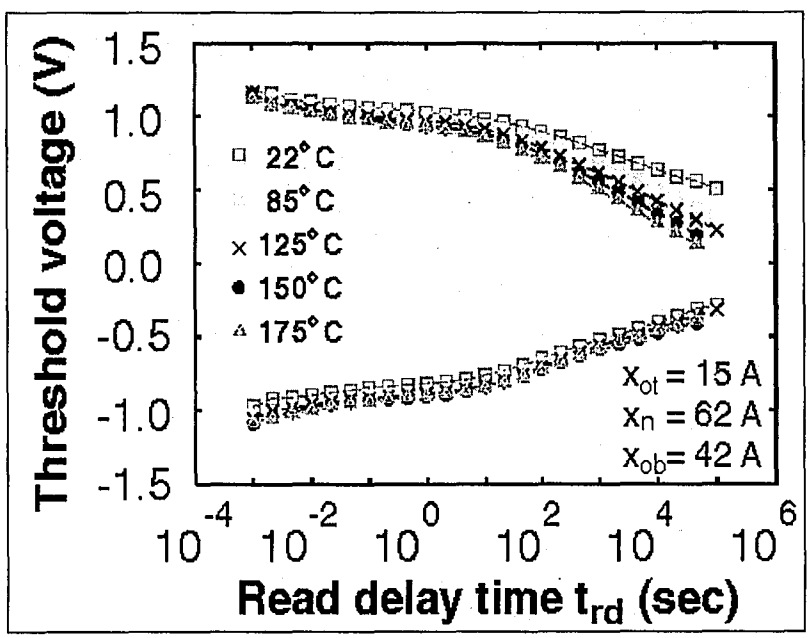

Figure 4.3 - Threshold Voltage decay vs. Temperature for a 'silicon-rich' Scaled SONOS NVSM Device. The device has experienced 10^3 erase/write cycles. The initial V_{TH} is set

with a series of erase/write pulses of ±7V, 1msec [11].

Their results, shown in Fig. 4.3, indicate the trapped 'electrons' in the nitride layer are thermally excited at elevated temperatures and 'back tunnel' through an ultra-thin tunnel oxide to the silicon. In contrast, the distribution of trapped 'holes' is influenced very little with increasing temperature. This result was explained by suggesting the activation energy for the electron traps lies closer to the conduction band edge in the silicon nitride than the activation energy for 'hole' traps to edge of the valence band in the silicon nitride as shown in Fig. 4.4.

Using this trap model, Yang and White [11] derived an expression for the charge trapped in the nitride,

$$\rho_n(x, E_{TA}, t) = -qg(x, E_{TA})f^- \qquad (4\text{-}1)$$

where E_{TA} is the energy level of the trap, f^- is the trap occupancy function for electrons, and $g(x,E_{TA})$ is the density of traps in the nitride (traps/cm^{3}eV) at a distance 'x' from the tunnel oxide-nitride interface into the nitride.

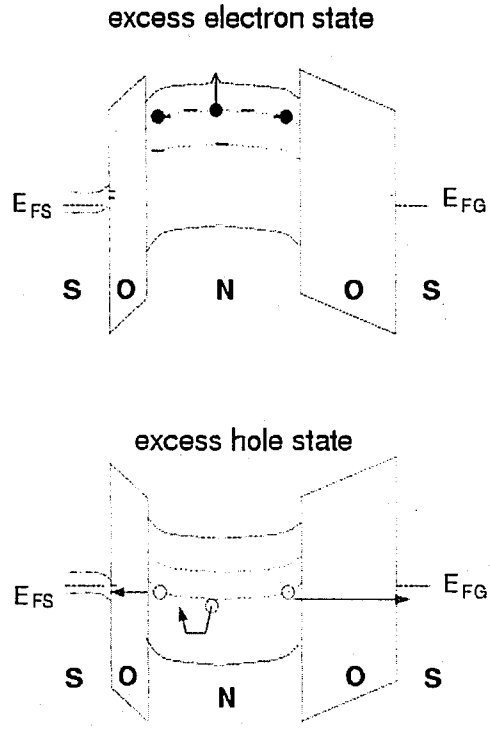

Figure 4.4 – Storage of Nitride Trapped Charge [11].

The charge stored in the nitride causes a shift in the threshold voltage of the device, ΔV_{TH}, which can be written as [11],

$$\frac{\partial \Delta V_{TH}}{\partial \log(t)} = -2.3 k_B T X_N \left(\frac{X_N}{2\varepsilon_N} + \frac{X_{OB}}{\varepsilon_{OX}} \right) g(E_{TA}) \qquad (4\text{-}2)$$

where X_N and X_{OB} are the thicknesses of the nitride and blocking oxide, respectively, while ε_N and ε_{OX} are the dielectric constants of the nitride and blocking oxide, respectively. Equation (4-3) assumes a uniform distribution of nitride traps and the activation energy responsible for the decay rate is [11]

$$E_{TA} = k_B T \ln(AT^2 t) \qquad (4\text{-}3)$$

where A is a constant given as

$$A = 2\sigma_n \sqrt{\frac{3k_B}{m^*}} \left[\frac{2\pi m^* k_B}{h^2} \right]^{3/2} \tag{4-4}$$

where σ_n is the trap capture cross-section, m^* the effective electron mass in the nitride and 'h' is Planck's constant. These relationships were used to interpret measurements of retention at elevated temperatures for retention times out to 10^5 seconds for the written state of a scaled SONOS device (Fig. 4.3). Since the thermal activation energy of electron traps is near the conduction band edge, the electrons are thermally excited from these traps and back-tunnel through the tunneling oxide. Eqn. (4-3) shows the trap energy may be probed at a given temperature by measuring the slope of the decay characteristics as a function of retention time. The capture cross-section, σ_n, may have temperature dependence.

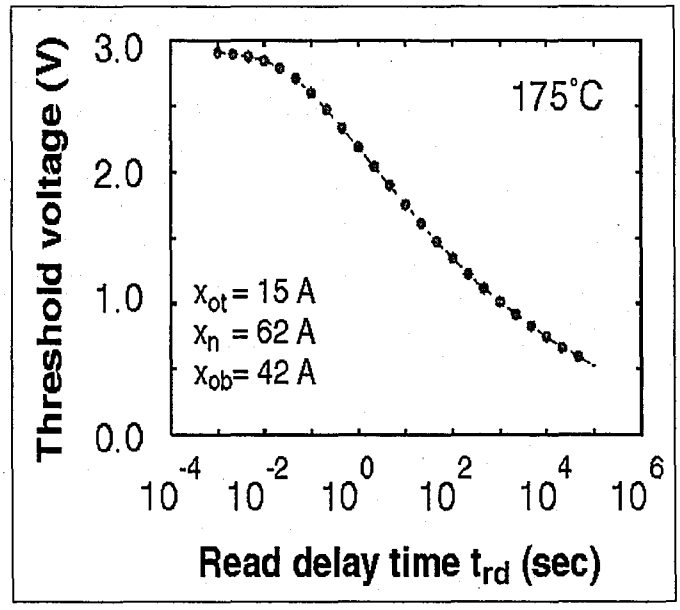

Figure 4.5 - Threshold Voltage decay versus retention time for a Scaled SONOS NVSM device at T = 175C. The device is fabricated with a 'silicon-rich' nitride [11].

Using Eqns. (4-1 – 4-4), the decay rate of the threshold voltage (Fig. 4.5) was used to extrapolate the trap profile in the nitride of the silicon-rich nitride, as shown in Fig. 17.

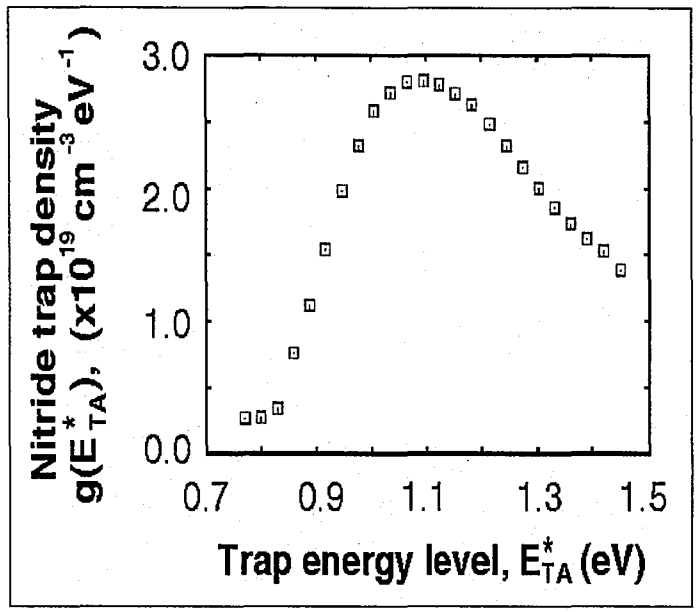

Figure 4.6 - Nitride Trap Density versus Energy for a Scaled SONOS NVSM device with a silicon-rich nitride [11].

4.4 SONOS Measurement Techniques

Retention measurements at elevated temperatures are performed at the wafer level. As in the experiments of Yang and White, we use a hot chuck, ring probe stand, oscilloscope and an analog circuit [10,45] controlled by a desktop PC. The PC controls the oscilloscope through a GPIB interface with programs written in a LabVIEW™ environment. Fig. 4.7 illustrates a block diagram of the experimental set-up for dynamic measurements. These measurements include Erase/Write, data retention and endurance measurements as a function of temperature. If we include radiation performance, then these tests are the ultimate tests for NVSM devices from a user's standpoint. The FPGA-

based measurement system in Fig. 4.8 can execute all of these measurements. The function generator is designed and simulated with XILINX Foundation Software. The bit-streams are generated and downloaded to the FPGA's through a parallel download cable. The analog detection circuit, under the control of the specific erase/write/read pulses sets the operational modes to the SONOS device under test (DUT) and determines the change of the memory-state of the SONOS nonvolatile memory transistor. The TEK460 oscilloscope digitizes the analog threshold voltage output and sends the latter to the computer (PC). The data is filtered and averaged with a LabVIEW^{TM} program on the computer and displayed on the monitor in real time.

The SONOS retention characteristics are monitored by applying programming pulses to the device, waiting a certain time t_r, and then forcing a constant current through the device and measuring the source voltage of the device as shown in the analog Detection Circuit of Fig. 4.8.

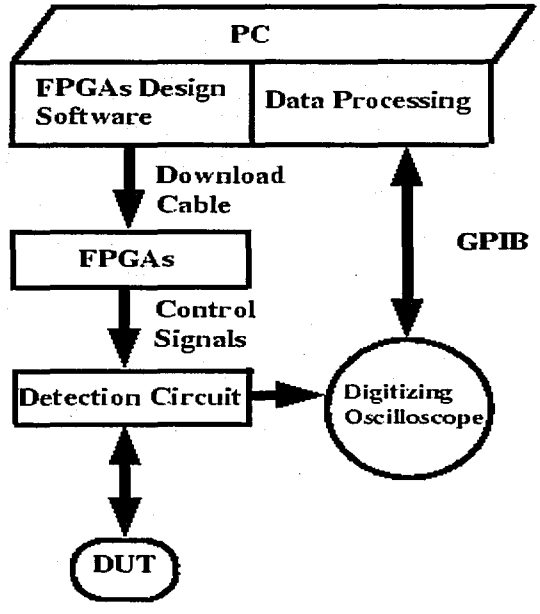

Figure 4.7 - A Block Diagram of the Experimental Setup for Dynamic Erase/Write/Read Measurements [10].

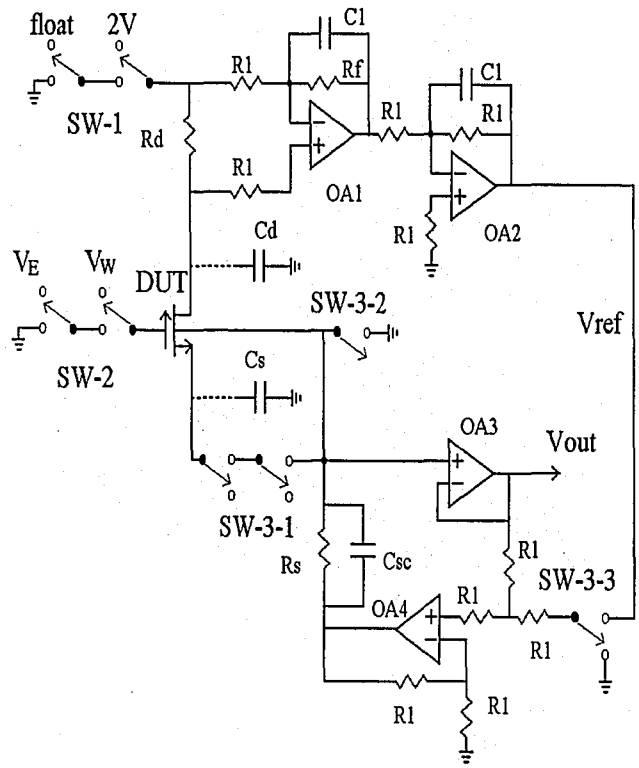

Figure 4.8 - A constant-current, threshold-voltage detection circuit implemented with switches (SW) controlled by FPGA's [10,45].

The threshold voltage is monitored at V_{OUT}. The measurements are performed on a hot chuck, which controls the temperature of the measurement environment and the wafer, as shown in Figs. 4.9 and 4.10.

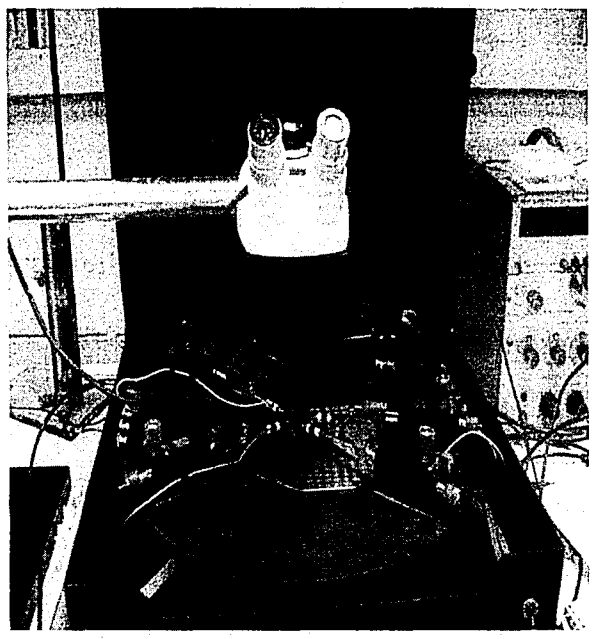

Figure 4.9 - SONOS Wafer & Hot Chuck.

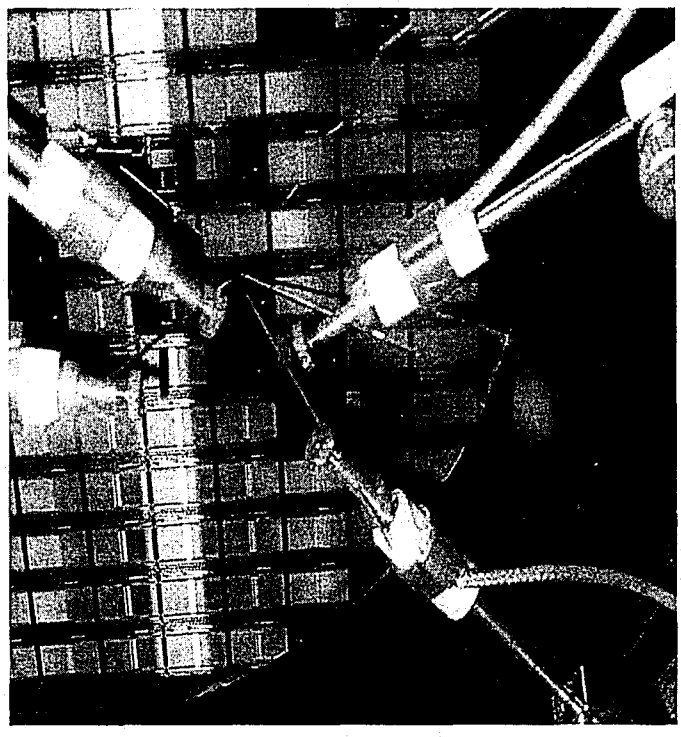

Figure 4.10 - Close-up View of Hot-Chuck Probes on Wafer.

The hot chuck is held at temperatures of 22 C, 80 C, 150C, and 250 C. The hot chuck used to collect this data has been operated routinely at temperatures up to 400 C. Due to this wear on the hot chuck, the surface where the wafer is placed is no longer planar. This created some difficulty in making good contacts with the probes onto the terminals of the device. When the device is heated and cooled, there is a degree of vibration associated with the operation of the hot chuck. When the temperature is increased to 125 C, the probes, which make contact on the device expand, and often slide off of the contact windows, scratching the device, and losing contact with the appropriate device terminals – especially for long-term retention measurements to 10^4 seconds. We compensate for these effects with special expansion probes and using smaller sections of the wafers. The smaller pieces are not affected by the hot chuck surface or by vibrations in the laboratory.

4.5 Experimental Results

In this section, we describe retention measurements at Lehigh University on SONOS devices from the Northrop Grumman Corporation 0.8 um CMOS/SONOS 1M EEPROM project. The 'oxynitride' storage dielectric contrasts with devices fabricated with a 'silicon-rich' nitride. The thermally activated SONOS retention model is applied using Eqns. (4-1 – 4-4) to the retention data of 'oxynitride' SONOS devices taken at elevated temperatures to extract the energy distribution of the electron traps in the nitride. The retention measurements are performed, as described above, at temperatures of 22, 80, 150, and 250 C. A hot-chuck probe stand regulates the temperature. The SONOS devices

are programmed with a 7V pulse applied to the gate for 2.5msec and erased with a –7V pulse applied to the gate for 7.5msec. The threshold voltage of the device is read for times ranging from 10^{-7} to 10^{3} seconds.

The threshold voltage of the device in the Write and Erase states at elevated temperatures is shown in Fig. 4.11. The results demonstrate the decay rate of the written state is affected by increasing the temperature. The Write state threshold voltage decay rate increases as the temperature increases. The Erase state decay rate is virtually unchanged. These trends are the same for both the 'oxynitride' (Fig. 4.11) and 'silicon-rich' nitride films (Fig. 4.3). In both films we observe, for Write and Erase states, a small initial shift of the threshold voltage with increasing temperature.

Long-term retention with temperature and radiation is of concern for space and military applications. The retention data has been extrapolated as shown in Fig. 4.12. At $3x10^{8}$ sec (10 years) and room temperature (22C) we have a 1.2V window. At 80C the

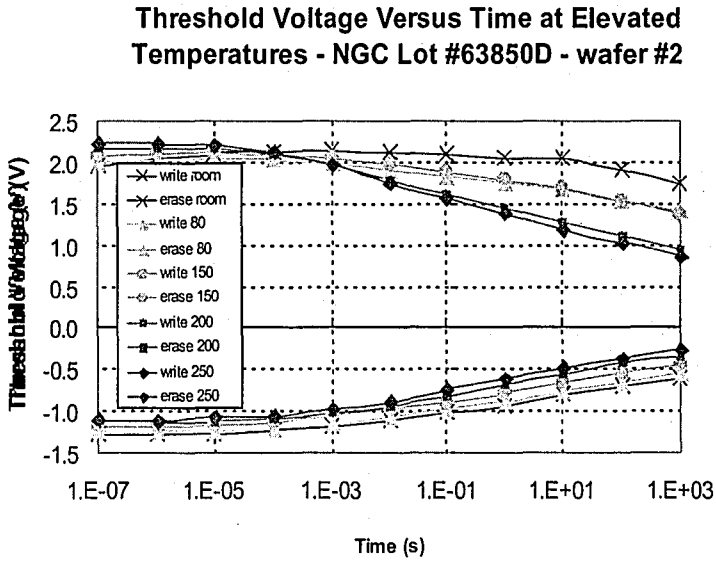

Figure 4.11 – V_{TH} vs. time at various temperatures for an Oxynitride SONOS NVSM Device. The Write (excess electron) state of the device is affected by temperature. In contrast, the Erase (excess hole) state displays very little temperature sensitivity.

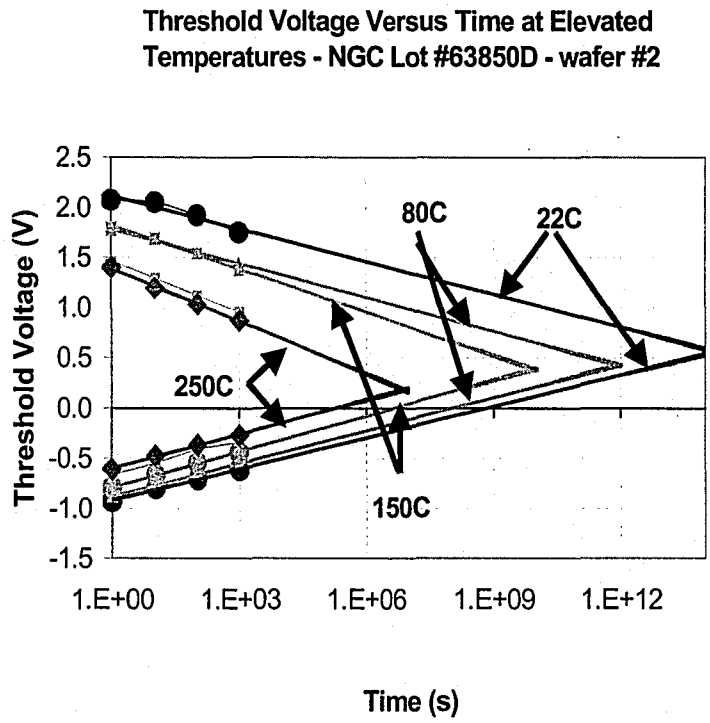

Figure 4.12 – Extrapolated V_{TH} vs. Temperature.

window has decreased to 0.8V at 10 years and at 150C the window decreases to 0.3V. The data indicates these SONOS devices should be acceptable for 7 V programming and 10 year memory retention applications for operating temperatures below +125 C. Further optimization is continuing for the 1Mb SONOS EEPROM project.

The trap density in the nitride layer of the SONOS device is determined as a function of trap energy using Eqns. 4-1 – 4-4. Eqn. 4-3 is used to calculate the energies of the traps in the nitride layer. At 250 C the trap energy ranges from 0.6 eV to 1.43 eV. The density at points along the threshold voltage curve is calculated using Eqn. 4-2. The change in threshold voltage divided by the logarithm of the change in time is calculated at each decade of time. The electron trap density, $g(E_{TA})$, is plotted versus trap energy, E_{TA}, in Fig. 4.13.

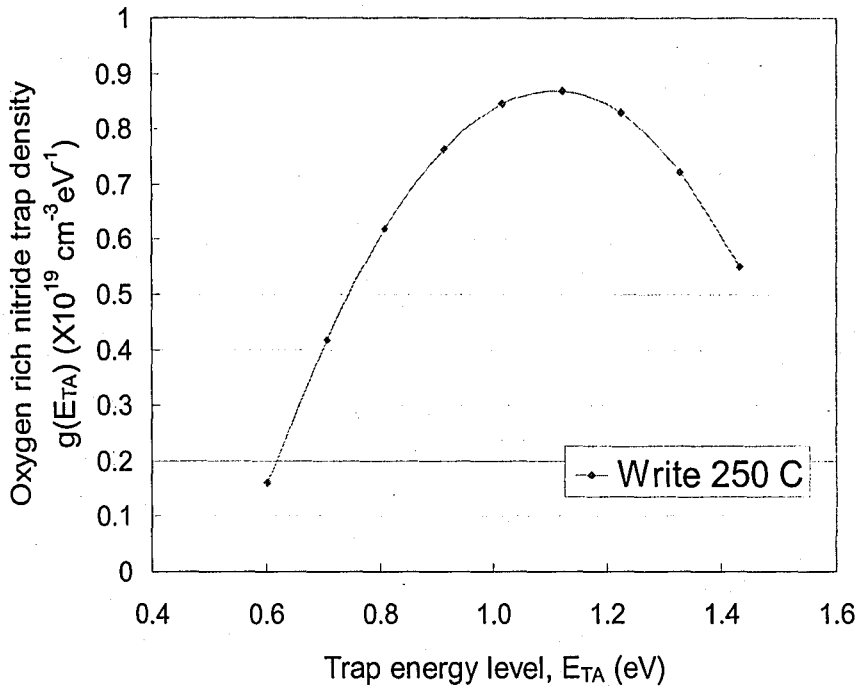

Figure 4.13 – SONOS Oxynitride Trap Density, $g(E_{TA})$, vs. trap energy, E_{TA}, for the Write (excess electron) state.

The electron trap density for the 'oxynitride' film peaks at 1.1 eV below the edge of the nitride conduction band - similar to the 'silicon-rich' nitrides film shown in Fig. 4.6. The trap density of the 'oxynitride' film is less than the 'silicon-rich' nitride film. This expected as the presence of oxygen will 'tie-up' silicon dangling bonds, which cause the memory traps in the nitride. The nitride trap density is extrapolated from the decay rate of the Write state at 250 C. This allows us to see the trap distribution within the 'oxynitride' band gap. In previous studies of elevated temperature affects, Yang and White [11] have extrapolated the electron trap density for a SONOS device with a 'silicon-rich' nitride layer at 175 C as shown in Fig. 4.6. The trap density for a silicon-rich nitride layer is roughly three times greater than the density for an 'oxynitride' layer as shown in a

comparison chart of Fig. 4.14. The 'oxynitride' and 'silicon-rich' nitride trap densities peak at the same activation energy, 1.1 eV.

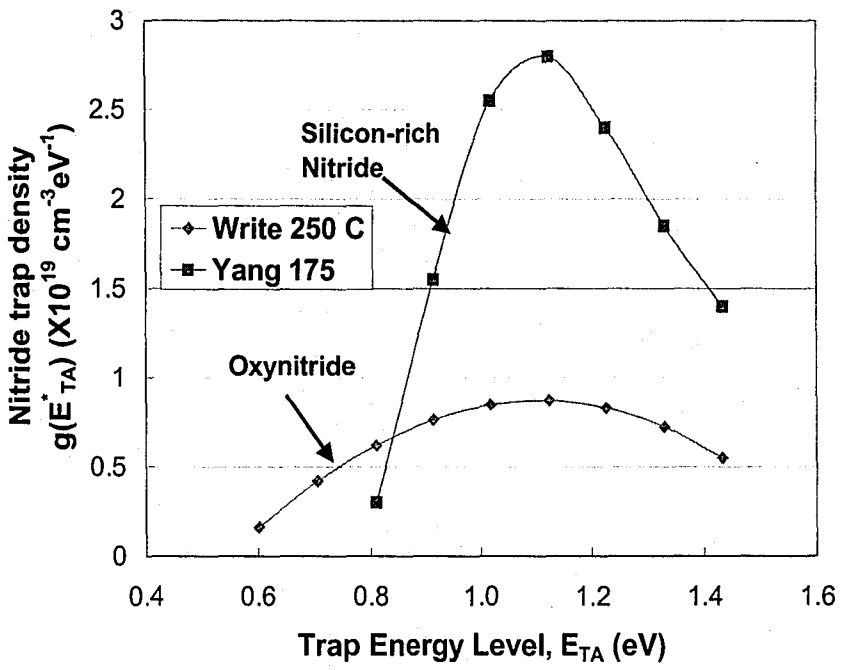

Figure 4.14 – A Comparison of Trap Densities in 'silicon-rich' and 'oxynitride' SONOS NVSM devices.

We may examine the time at which the memory window closes at the different temperatures to determine an "acceleration factor" in the rate of charge loss in the write state. We define memory window closure as the point where the write and erase states intersect. At elevated temperatures the electrons are thermally excited and escape from traps in the nitride to tunnel back to the substrate. A greater number of electrons will be excited as temperatures increase resulting in additional loss of charge. High temperatures accelerate the loss of charge and allow us to perform a screening measurement on the SONOS devices. For example, if an acceleration factor of 1000 is observed over 100

degrees, a SONOS device retaining charge at 150 C for 10^5 seconds is equivalent to a SONOS device retaining the same quantity of charge at 50 C for 10^8 seconds, roughly 10 years.

These measurements were performed on a SONOS device with a gate dielectric consisting of an 18 A tunneling oxide, 80 A oxynitride layer, and a 40 A blocking oxide. We examine Fig. 4.12 to determine the times at which the extrapolated memory windows close, see Table 4.1. The times at which the memory windows close are plotted

Temperature (C)	**Time of Memory Window Closure (sec)**
22	10^{14}
80	10^{12}
150	10^{10}
250	10^{7}

Table 4.1 – Times at which memory windows close for given temperatures for a SONOS Nonvolatile Memory Transistor with an Oxynitride Storage Layer.

on a logarithmic scale versus the temperature, Fig. 4.15. Extrapolating the window closure time versus temperature data yields a straight line, Fig. 4.16. The acceleration factor in this case is 1000 over 100 degrees.

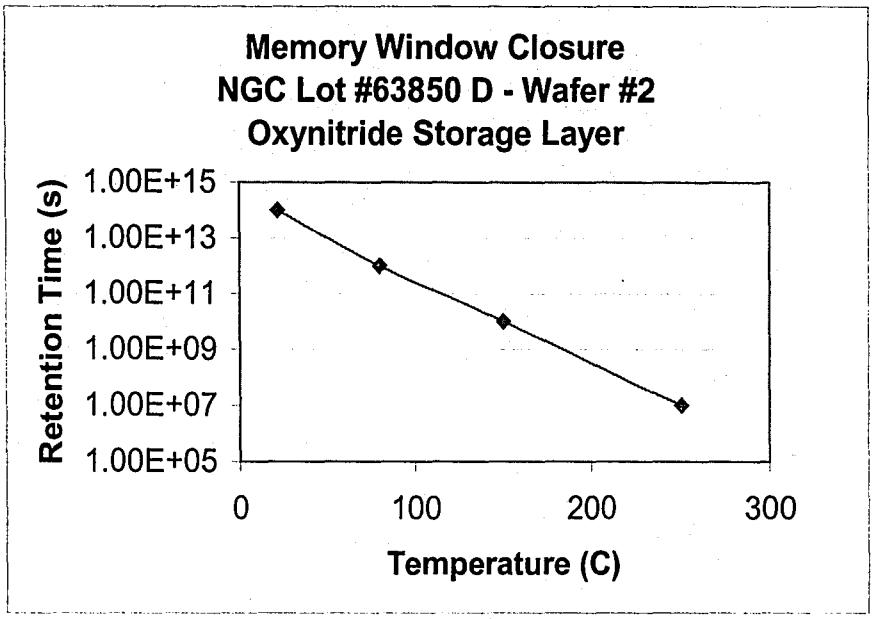

Figure 4.15 – Time in seconds of memory window closure at selected temperatures.

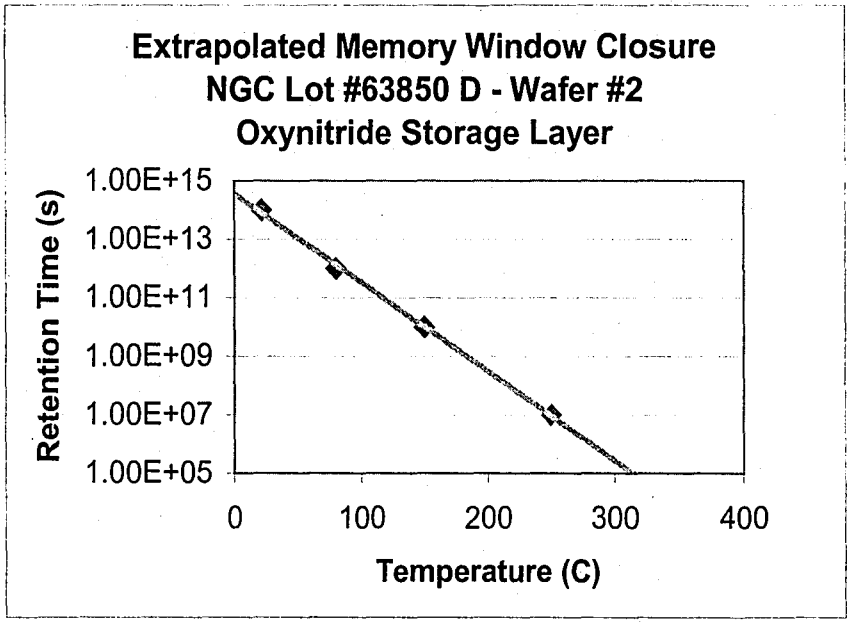

Figure 4.16 – Extrapolated memory window closure time vs. temperature.

Examining Fig. 4.16 demonstrates the logarithmic dependence on time of memory window closure on temperature. For example, at 50 C the memory window closes at 10^{13} seconds. At 150 C the memory window closes at 10^{10} seconds. Therefore, the difference

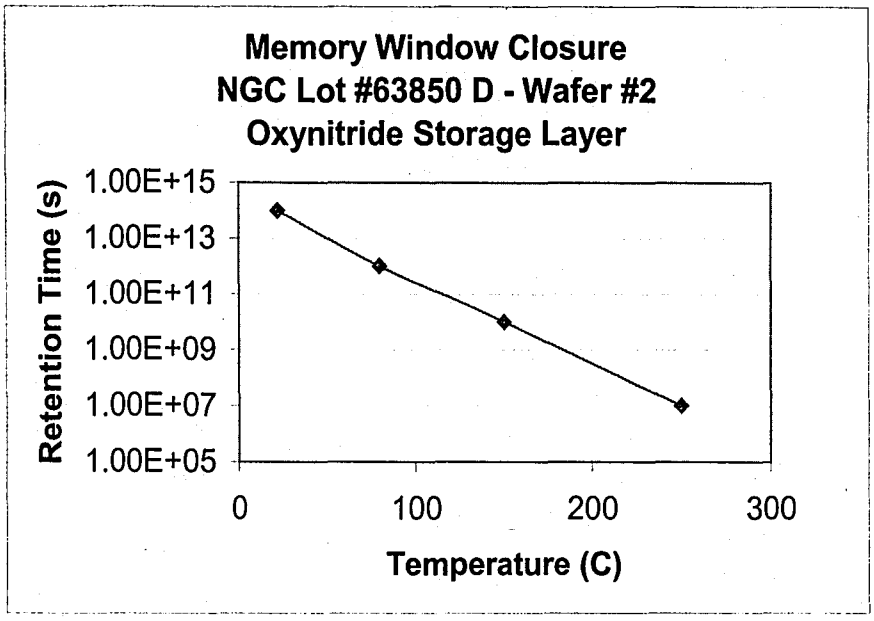

Figure 4.15 – Time in seconds of memory window closure at selected temperatures.

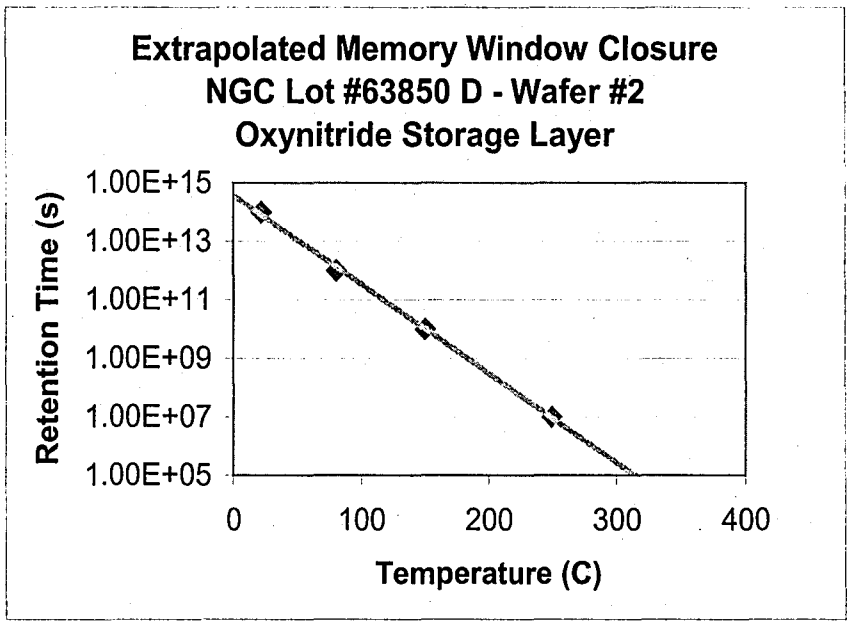

Figure 4.16 – Extrapolated memory window closure time vs. temperature.

Examining Fig. 4.16 demonstrates the logarithmic dependence on time of memory window closure on temperature. For example, at 50 C the memory window closes at 10^{13} seconds. At 150 C the memory window closes at 10^{10} seconds. Therefore, the difference

of 100 C causes the memory window to close 1000 times faster. This allows us to perform a retention measurement for a short period of time at an elevated temperature and guarantee retention at lower temperatures for greater time periods.

Chapter 5

Conclusions

This thesis addresses the retention reliability of SONOS nonvolatile memory devices at room and elevated temperatures. This chapter summarizes the crucial aspects of SONOS device charge retention investigated earlier in this thesis. Included is a brief section noting topics of future investigation regarding SONOS device reliability.

5.1 Conclusions from this Thesis

5.1.1 Modeling

- The temperature effect on the threshold voltage of scaled (7V programming) SONOS 'oxynitride' NVSM devices has been investigated. At elevated temperatures, the Write state threshold voltage decay rate, $\partial V_{TH}/\partial \log(t)$, of 'oxynitride' and 'silicon-rich' nitride SONOS devices increases with increasing temperature, while the Erase state threshold voltage decay rate remains unchanged. The nitride trap density is extrapolated from the decay rate of the Write state at 250 C. This allows us to see the trap distribution within the 'oxynitride' band gap.

5.1.2 Experimental Observations

- We see from Fig. 23 the extrapolated memory retention window at 3×10^8 sec (10 years) and 22C is 1.2V, a 0.8V window at 80C, and a 0.3V window at 150C.

- Write state temperature dependence of charge loss due to thermal excitation of electrons from traps in oxynitride charge storage layer demonstrates that with further measurements an acceleration factor of charge loss can be identified. Further measurements must be conducted to verify closure of memory windows, Fig 4.15. Present data demonstrates dependence of time of window closure on temperature, Fig. 16.
- The trap density for a silicon-rich nitride layer is roughly three times greater than the density for an 'oxynitride' layer as shown in a comparison chart of Fig. 25. The 'oxynitride' and 'silicon-rich' nitride trap densities peak at the same activation energy, 1.1 eV.

5.2 Future Considerations

- We will take longer-term retention data in the future to see if there is a change in the decay rates, since the electric fields will be modified in the device with the loss of memory charge. The retention measurement setup has already been altered to accommodate retention times up to 10^5 seconds (~1 1/8 days) in order to investigate a possible relaxation of the internal electric fields over time. Simulations could also be run in order to investigate the behavior of the electric fields for a device in the retention mode.
- Preliminary measurements on scaled SONOS NVSM devices support the validity of high temperature screening measurements in the determination of long-term retention. Future measurements must identify a consistent acceleration factor

(i.e. 50 mV memory window at 10^4 sec = 50 mV memory window at 10^7 seconds), in order to develop a quality screen for SONOS devices.

- Plasma damage has been observed in SONOS devices fabricated at Northrop Grumman. During the plasma etch procedure, electrons build up in the gate of the device, damaging the SONOS transistors to the point where they are inoperable. Two diodes connected back to back can be connected to the gate of the device. During plasma etch these diodes will periodically remove charge which has accumulated in the gate and prevent damage to the device. Retention measurements on SONOS transistors with and without these gate diodes may be performed to determine their effectiveness in preventing plasma damage.
- Doubling the density of SONOS devices by using 2-bit data storage from channel hot carrier injection can be investigated. Hot carrier injection is used to store small amounts of charge separately in the opposite ends of the nitride layer. A thicker tunnel oxide must be used to accommodate for hot carrier injection. The charge stored in each end of the nitride will correspond to a different zero or one. This effectively doubles the density of the device by allowing the user to store four different states 0 0, 0 1, 1 0, or 1 1.

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Appendix A – Trends in NVSM's (NVSMW – Monterey, CA 2001)

Table A.1 Alternatives to Floating Gate FLASH Memory Devices

Technology	Operation	Advantages	Disadvantages
SONOS	1. Tunnel electrons or holes through oxide and trap charge in ONO dielectric.	1. Simple, easily integrated into existing CMOS process. 2. Low power/ compatible with logic integration. 3. Rapid time to market < 2 yrs. 4. Low cost – dense (up to 16Mb).	1. Slow write speed (2-10ms). 2. Endurance limitation 10^5, will not effectively replace SRAM/DRAM.

NROM	1. Hot electron injection at both source and drain to store 2-bits in nitride layer. 2. "Reverse" read operation. 3. ~400 electrons/ bit. 4. Relatively new/ untested technology. 5. Charge is not vertically distributed.	1. 2 bits/cell – $2.8F^2$. 2. Simple process 16-18 masks. 3. Fast operation program:100ns erase: 250ns (800 electrons per operation). 4. Reliable – no single bit failure.	1. Not easily integrated – new concept. 2. Channel Hot Injection (CHE) – limited parallelism. 3. Small window ~1.5V. 4. Possible punchthrough. 5. Unknown charge distribution in nitride. 6. No long-term retention data. 7. No retention data at elevated cycling – possible oxide damage from hot electron injection. 8. 100-200 angstrom charge distribution – scaling limitation.
Nanocrystal	1. Discrete charge storage in gate. 2. Use Fouler-Nordheim Tunneling or electron injection. 3. 1T per bit > $4F^2$. 4. Few electrons utilized per operation.	1. Cost reduction. 2. Simple process (single poly). 3. Low programming voltage - better retention with thinner oxide. 4. Discrete storage – immune to source or drain leakage. 5. Fast access.	1. No 10X improvement (speed, cost, power). 2. Low coupling ratio. 3. Retention reliability is suspect. 4. Uniformity of crystals – V_T distribution/erratic bits.

Ferroelectric	1. Polarized charge displacement. 2. 1T/1C (similar to DRAM). 3. 1T (similar to FLASH).	1. Vast number of companies currently investigating ferroelectric NVSM's. 2. Write ~ nanoseconds. 3. High endurance (10^{13} cycles). 4. Low power. 5. Scalability. 6. Nonvolatile (analog storage/multilevel). 7. Radiation hard. 8. 1T/1C ~$10F^2$ - DRAM/FLASH. 9. 1T ~$5F^2$. 10. Possible "universal memory" if retention is good.	1. Fabrication contamination – currently using old fabs. 2. Exotic materials. 3. Limited number of cumulative bits produced. 4. 1T/1C requires high temp. anneal >700C – oxidation occurs. 5. Retention at high temperatures is unproven. 6. Sense amplifier reference fatigues. 7. Array architecture needs definition. 8. Not proven.

MRAM	1. Store data (polarization) on magnetic element. 2. CMOS reads data as low/high resistance.	1. High density. 2. High speed (35ns). 3. No refresh. 4. Nondestructive read. 5. Low voltage operations (2.7-3.3V). 6. Unlimited read/ write endurance (10^{11} cycles without degradation).	1. Difficult to maintain uniformity and reproductivity of magnetic tunnel junction (~15 angstroms). 2. Integration with CMOS – MRAM's withstand 300C max (COMS req. 400C). 3. Contamination from new materials (Ni, Fe, Co, Mn). 4. Large currents req. to program (mA). [read uA] 5. Bit disturb while switching in large arrays. 6. Large MR signal required for very high speed. 7. Deep sub-micron scalability is unknown.

Appendix B - Measurement Procedures (step by step)

B. 1 Current Versus Voltage Measurement

Goal – To plot the drain current versus applied gate voltage on a single SONOS device and to become familiar with the measurement setup using the HP- 4145, multi-meter, and LabVIEW™ interface. The I-V curve is useful in determining the threshold voltage of the device in the fresh, programmed, and erased states.

1) Setup

A) Verify that the computer is connected to the 4145 scope (bottom right) and the Keithley 7001 Switch System (top right) using the GPIB cables.

B) Place the wafer onto the probing station.

C) Locate a single SONOS device.

D) Make contact with the device at pads indicated in the chart.

Table B.1 – Current versus Voltage Measurement Pin Setup

	Source	Substrate	Gate	Drain
Pad #	9	32	33	8
Pad #	7	34	35	6
Probe #				

E) Close the lid on the probing station and watch so the lid does not close on the wafer.

F) Connect the pins on the side of the lid to the wires from the Keithley meter in this order from top to bottom: 1, 2, 4, 5.

G) On the PC, load the program "matrix.vi" in the directory \\Calvin\pcdir\labview \programs\subvis. Run the program by clicking on the white arrow in the top left of the screen.

H) On the PC, load the I-V measurement program "isvgfam" in the directory \\Calvin\pcdir\labview\programs\iv. The program will take a few seconds to load.

2) Measurement

A) Choose a title for your data measurement.

B) Set the bulk voltage to zero volts.

C) Set the Gate Voltage Range from –3.0 to 1.0 volts.

D) Set the data points to 51 for a higher resolution curve.

E) Set the Drain Voltage to 50 mV.

F) Set the Bulk Steps to 1. Setting this to a value greater than one will repeat the measurement that many times.

G) Set the Channel Definitions. (refer to chart above)

H) Run the program by clicking on the white arrow in the top left of the screen. Do not bump the table during the measurement.

I) Save your data to a file in a directory you set up for yourself.

J) Print the LabVIEW™ screen (scale window to 85% in printer settings).

K) Write the device

1) Change the Gate Voltage Range to +7V to +8V.

2) Run the program for roughly 10 seconds then click on the stop icon next to the arrow.

L) Change the title of your measurement (part A) to indicate the device has been programmed.

M) Repeat steps 2B through 2J.

N) Erase the device

1) Change the Gate Voltage Range to –7V to –8V.

2) Run the program for roughly 10 seconds then click on the stop icon next to the arrow.

O) Change the title of your measurement (part A) to indicate the device has been erased.

P) Repeat steps 2B through 2J.

Q) Open Microsoft Excel and import your data and plot it as best you can.

B. 2 Charge Pumping Measurement

Goal – To sweep the gate of the device with a square wave with specific amplitude in order to excite electrons out of traps in the Si-SiO2 interface. This will result in a

current, which will be measured. This current can be related to the charge stored in the device by dividing the current by the frequency. LabVIEW™ will extract the interface trap density, Dit, from the charge stored in the traps.

1) Setup

A) Verify that the computer is connected through the GPIB cables with the HP 33120A function generator and the Keithley 617 programmable electrometer.

B) Follow steps B – E from the I-V measurement.

C) Connect the HP 33120A to the gate of the device.

D) Connect the source and drain terminals together using the "T" connector and to Keithley 617 electrometer.

E) Place the short circuit connector onto the substrate pin to ground this terminal.

F) Load the program "sonosBASE_swp.vi" in the directory "C:\steve\SONOS LabVIEW".

2) Measurement

A) Set the amplitude to 2 volts (default).

B) Set the frequency to 1.00E+5 Hz (default).

C) Leave the rise and fall times at 1E-7 seconds (default).

D) Set samples per point to 3 or 5 if you want a more accurate measurement.

E) Set the type of device, NMOS (default) for the Northrop Grumman lot # 63850D wafers.

F) Set termination to High Z (default).

G) Set pulse generator to HP-33120A (default).

H) Set the base level range to values appropriate for the device. Start with a range from –3 to +1 volts in the forward direction. You will have to change these values in order to view the entire charge pumping curve.

I) Enter a name including the device lot #, wafer #, and any other information that characterizes the device.

J) Set the width and length of the device. For NGC lot # 63850D, W =10 um and L = 0.8 um.

NOTE: When measuring an array of devices, width becomes # of devices x width of 1 device, in order to account for the large number of devices in the array, and correctly extract I_{CP} and D_{it}.

K) Run the program by clicking on the white arrow in the top left of the screen. Do not bump the table during the measurement.

B. 3 Retention Measurement

Goal – To determine the ability of a SONOS device to retain charge over a long period of time, to investigate the retention characteristics at elevated temperature, and to determine the effect of stressing the device on the retention characteristics.

1) Setup

A) Turn on all 4-power supplies.

B) Download FPGA through the hardware debug cable.

a. Northrp1- to erase device in 7.5 ms

b. Northrop- to write device in 2.5 ms

c. In Xilinx Foundation software, choose Northrop.bit or Northrp1.bit → Download → Download design → OK

C) Verify that the computer is connected through the GPIB cables with the Tek TDS 460 oscilloscope.

D) Connect the cables from the box to the exact pad.

E) Check the connection of V_w and V_e.

a. When writing the device, V_w should be positive and V_e should be negative.

b. When erasing the device, V_w should be negative and V_e should be positive.

F) Load the program "FPGAretention_readonly.vi" in the directory "C:\steve\SONOS LabVIEW".

G) Reset SW-1 and press the middle square button to start.

2) Measurement

A) Set up windows

a. read window 1: 2.49E-4 read window 2: 3.47E-4

b. ground window 1: -3.18E-4 ground window 2: -2.41E-4

c. "read window" goes on the left side of the transition on the oscilloscope,

which is Vth. "ground window" is on the right side on the oscilloscope, which establishes ground for Vth.

B) Measurements start from 1E-7, 1E-6... to 1E+5 s.

B. 4 Erase/Write Cycling Measurement

Goal – To simulate prolonged use of the device, and determine how the device will hold up under periods of extreme use.

1) Setup

A) Connect the HP-33120A to the gate of the device.

B) Short the source, drain and bulk to ground.

C) Verify that the computer is connected through the GPIB cable with HP-33120A.

D) Load the program "stress1.vi" in the directory "C:\steve\SONOS LabVIEW".

2) Measurement

A) Set Input Stress Cycles from 1E4 to 1E6.

B) Set Write Width as 2.5 ms and Erase Width as 7.5 ms.

C) Set Write Amplitude and Erase Amplitude as 7 V.

Appendix C - SONOS Device Fabrication – (Step-by-Step)

C. 1 Starting Material

1. 3-inch p-type Si Wafers, boron-doped 13-15 Ω-cm

C. 2 N-Well Formation

1. RCA clean with HF dip
2. Oxidation, 1000 Å (dry, 1000 C, 160 min)
3. Photolithography, mask NW (N-Well)
4. BHF etch to obtain 200 Å pad oxide (14 min)
5. N-well implantation, phosphorus, 100 KeV $4.8x10^{12}cm^{-2}$
6. Plasma photo resistor (PR) strip
7. Chemical PR strip
8. RCA clean
9. Anneal, 1100 C, 60 min, N_2, 2 slpm
10. Oxidation, dry, 1100 C, 15 min
11. Anneal (N-well drive in), 1100 C for 24 hours, N_2, 2 slpm

C. 3 LOCOS Isolation

1. RCA Clean
2. LPCVD nitride 1000 Å (725 C, 0.3 Torr, 20 sccm dichlorosilane (DCS), 100 sccm ammonia, 65 min)

3. Photolithography, mask AD (Active Device)
4. Plasma etch nitride (0.3 Torr, 300 Watts, 60 sccm CF_4)
5. Chemical PR strip
6. Photolithography, mask FI (Field Implant)
7. Field implantation, boron, 40 KeV, $5x10^{14}cm^{-2}$
8. Plasma PR strip
9. Chemical PR strip
10. RCA clean
11. Field oxidation/implant activation (wet, 1000 , 180 min)
12. Field oxidation, 8000 Å (wet, 1000 C, 140 min, anneal 30 min in dry N_2)
13. Etch oxynitride over the nitride (10:1 BHF, 1 min)
14. Etch nitride, 1000 Å (hot phosphoric acid, 180 C, 60 min)
15. Etch buffer oxide, 1000 Å (10:1 BHF, 100 sec)
16. RCA clean
17. Oxidation – remove residual nitride (wet, 900 C, 20 min)
18. Etch oxide (10:1 BHF, 100 sec)
19. RCA clean (no HF)
20. Oxidation, 250 Å (wet, 900 C, 15 min)

C. 4 Channel Doping

1. Threshold adjust implant, boron 50 KeV, $1x10^{12}cm^{-2}$
2. RCA clean

3. Implant anneal (900 C, N_2, 30 min)

C. 5 Gate Formation and Polysilicon Deposition

1. Etch pad oxide (100:1 BHF, 12 min)
2. RCA clean (after HF dip to hydrophobic, do not rinse)
3. Tunnel oxide growth, 20 Å (TWO, 800 C, 30 sccm O_2 in 3000 sccm Ar, 40 min)
4. LPCVD silicon-rich nitride, 45 Å (680 C, 90 sccm DCS, 30 sccm NH_3, 7 min)
5. LPCVD nitride, 45 Å (680 C, 10 sccm DCS, 100 sccm NH_3, 13 min)
6. Optional – LPCVD oxynitride, 45 Å (680 C, 30:40:10 N_2O:NH_3:DCS, 4 Å /min)
7. LPCVD oxide, 55 Å (725 C, 10 sccm DCS, 100 sccm N_2O, 34 min)
8. Oxide steam densification (wet, 900 C, 30 min)
9. Polysilicon gate deposition, 5 K Å (625 C, 800 mTorr, 284 sccm Silane, 30 min)
10. RCA clean
11. $POCl_3$ diffusion (900 C, N_2 and O_2 flow with $POCl_3$ bubbler at 19 C, 25 min, then N_2 only for 25 min)
12. Etch P-glass (100:1 BHF, 4 min)
13. Photolithography, mask PY (Polysilicon)
14. Plasma etch polysilicon (300 Watts, 150 mTorr, 45 sccm SF_6, 60 sec)
15. Chemical PR strip

C. 6 Source and Drain Implants

1. Etch blocking oxide (100:1 BHF, 3 min)

2. Etch nitride (H_3PO_4,180 C, 3 min)
3. Etch tunnel oxide (100:1 BHF, 3 min)
4. RCA clean (with HF dip)
5. Pad oxidation, 200 Å (wet, 800 C, 28 min)
6. Photolithography, mask PP (Poly-diffusion)
7. P-Source/Drain implant, boron, 32 KeV, $5x10^{15}cm^{-2}$
8. Plasma PR strip
9. Chemical PR strip
10. Photolithography, mask NN (N-diffusion)
11. N-Source/Drain implant, phosphorus, 40 KeV, $5x10^{15}cm^{-2}$
12. Plasma PR strip
13. Chemical PR strip
14. RCA clean
15. Implant drive-in anneal (1000 C in 2 slpm N_2 for 160 min)
16. Boron/Phosphorus-silicate glass strip (10:1 BHF, 1 min)

C. 7 Contact Window

1. RCA clean (with HF)
2. Intermediate oxide, 1100 Å (wet, 950 C, 30 min, anneal 30 min)
3. Photolithography, mask CW (Contact Window)
4. Etch windows (10:1 BHF), rinse thoroughly
5. Chemical photo strip

C. 8 Pre-metal High Temperature deuterium Anneal

1. RCA clean (with HF dip to hydrophobic)
2. Anneal (700 C, 10% D_2/N_2, 2 slpm, 4 hours, PMA furnace)

C. 9 Metalization

1. DC sputter (2 hours, cool down 10 min)
2. Photolithography, mask MET (Metalization)
3. Etch aluminum (PAN etch at 43 C)
4. Chemical photo-strip

C. 10 Post-Metal Anneal (PMA)

1. Organic clean (Acetone & Methanol)
2. PMA (400 C, 10% D_2/N_2, 30 min)

Vitae

Stephen J. Wrazien was born on May 7, 1978 in Hartford, Connecticut to Mr. Carl S. Wrazien and Mrs. Barbara A. Wrazien. He attended the University of Scranton from September 1996 to May 2000 and graduated with a Bachelor's Degree in Electrical Engineering. He received admission to Lehigh University in Fall 2000 to pursue a Masters Degree in Electrical Engineering. He will continue his research assistantship at the Sherman Fairchild Laboratory in order to pursue his PhD degree in Electrical Engineering at Lehigh University. During his studies at the University of Scranton, he was inducted into the Sigma Pi Sigma and was awarded the Dr. A.J. Cawley Award for Excellence in Electrical Engineering.

Publications

Stephen Wrazien, Jon Faul and Marvin H. White, "Characterization of Scaled SONOS NVSM Devices for Space and Military Applications", Non-Volatile Memory Technology Symposium 2001, San Diego, CA, November 2001.

END OF TITLE