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Manufacturing process based quality and reliability in hybrid micro-electronic, and thick film circuits

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MANUFACTURING PROCESS BASED QUALITY AND RELIABILITY IN HYBRID MICRO-ELECTRONIC, AND THICK FILM CIRCUITS

by

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To My Mom Rajkuwar

and Dad Satish.

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Abstract

This research explores the problems in hybrid microelectronic manufacturing, in the laboratory environment. Most major problems associated with thick film ceramic microelectronic manufacturing processes involve screening of the paste and firing at the specified temperature for the given paste alloy and rheuological characteristics of the paste systems. The research explores the dispersion and spread in the paste so as to achieve the required resolution for the given rheuological condition of a silver-palladium conductor paste system. The results are used to determine a recommendation for a quality standard that can be implemented in the manufacturing environment.

Chapter 1 - Introduction

This thesis presents the work involved in the manufacturing processes and quality of hybrid microelectronic and thick film circuits. This chapter provides an overview of the thesis and the order in which it is presented. In the second chapter characteristics of metal alloys and their properties as used in paste aggregates are discussed. A detailed discussion is presented of silver, gold, platinum, palladium, and its alloy combinations as dealt with in their applications in thick film circuit manufacturing.

An analysis of the important aspects of quality involves an in depth understanding of the assembly process, the current trends in the process, and the location dispersion effects that exist within the process. These issue are addressed in the third chapter of this thesis.

The assembly process is incomplete without its proper packaging. Packaging for space, robustness, and efficiency are as important in the optimal utilization of the circuit as the development of its design for manufacturing. Chapter 4 deals with packaging in hybrid microelectronic circuits, surface mount systems, leadless passive components, leadless active components, leaded plastic components, fine pitch and ultra fine pitch components, and QFP/PQFP packages.

An overview of the standards that exist for use with microelectronic circuit manufacturing is presented, along with their direct impact in implementation, in chapter 5.

The experiment performed in the development of the code for the application with microelectronic manufacturing is presented in chapter 6. In addition, the model generated and the pastes that were used in performing those experiments are explained.

Chapter 7 discusses other processes involved in microelectronic manufacturing that were not part of the experimental process due to equipment limitations in the laboratory. These processes include electron beam coevaporation, sputtering, laser ablation, etc. An outlook to the future is also presented in the discussion in chapter 7.

Chapter 8 concentrates on the results of the study and discusses the most appropriate quality plans that can be implemented to provide a more industry-like environment in the university laboratory.

Chapter 9 discusses the implementation of the source code that was generated. To make the results more presentable the code was written in Visual Basic 4.0.

Based on the results of the experiments, suggestions for future research in manufacturing of thick film hybrid microelectronic circuits is provided as a part of chapter 10.

Chapter 2 -Metallurgy

2.1 Introduction

The metallurgy of thick film conductor paste is very complex. Certain qualities are required to be satisfied in the paste aggregate. Important qualities are adhesion (also referred to as tack strength), conductivity, resistance to corrosion, safety in handling, and cost of the element. This thesis involves experimenting to determine the factors that influence the resolution of the circuit laid out on a ceramic substrate using palladium-silver conductor paste. An understanding of the types of conductor pastes that are used and their metallurgical properties is important. Therefore this chapter presents material intended to assist with that understanding.

Most noble metals such as silver, gold, platinum, palladium and their alloys satisfy almost all of the requirements of the conductor paste aggregate. This chapter provides an overview of the metallurgical properties of metals and alloys as used in the conductor paste system as discussed by the ASM Metals Handbook**[11]**.

2.2 Silver[11]

Common name	Silver. Ag

Silver is deposited on ceramic substrates from 1 to 5 um to form a conducting layer. Silver sputtering targets are used for applications of transparent thin film, and microelectronic applications.

Density.	10.49 g/cc.
Melting Point.	961.93°C.
Coefficient of linear thermal expansion.	19068 um/m°K.
Specific Heat.	0.234 Kj/Kg°K at 0°C.
Thermal Conductivity.	418.68 W/m at 0°C.
Electrical Resistivity.	0.1059 uOhm/cm at 0°C. For an annealed wire 2.3 mm
Temperature Coefficient.	4.1x 10^{-3} /°C from 0-100°C

Corrosion. Silver does not appear to oxidize at room temperature in air. It is attacked and blackened by ozone. Sulfur attacks silver and also decreases the reflectivity of silver. The addition of noble metals has been shown to reduce this effect, especially when 50 - 70 % Pd is added to reduce the effect of the sulfur attack. Silver is resistant to acetic acid, and various other organic acids and food. It is also resistant to phenol, hydrofluoric acid, and phosphoric acid. Silver is attacked by low melting temperature molten metals like mercury, sodium, potassium and their mixtures, lead, tin, indium, bismuth, etc.

Recrystalization temperature.	20-200°C depending on purity

2.3 Gold[11]

Common name.	Proof gold if more than 99.99% pure.

Au

Gold is used for variable resistors to provide low noise, internal contacts, for adhesion and to produce a flexibile coating on vibrating and flexing components. Gold is sputtered onto selected areas of solid state devices such as silicon transistors and integrated circuit chips to provide electrical terminals for these devices. Fine diameter gold wires can then be thermocompression bonded to these terminals for electrical connections to lead frames or other external circuits. Gold and silicon or germanium make low melting eutectics. This may be done *in situ* simply by heating pure gold in contact with silicon to produce a solder that bonds the semiconductor to its base or other terminals.

Density.	19.32g/cc.
Melting Point.	1064°C.
Coefficient of linear thermal expansion.	14.2um/m°K.at 20°C
Specific Heat.	0.130KJ/Kg°K at 18°C.
Thermal Conductivity.	300 W/m at 0°C.
Electrical Resistivity.	20-22 nOhm/m at 0°C.

2.4 Commercially pure platinum[11]

99.95% Pt

Various alloying elements such as rhodium, ruthenium and iridium are alloyed to provide better corrosion properties and increased hardness.

Density.	21.46g/cc. At 25°C
Melting Point.	1769°C.
Coefficient of linear thermal expansion.	9.1um/m°K.
Specific Heat.	0.132 Kj/Kg°K at 0°C.
Thermal Conductivity.	71.1W/m at 0°C.
Electrical Resistivity.	98.5 nOhm/m at 20°C. For an annealed wire 2.3mm

Corrosion. Platinum is resistant to reducing and oxidizing acids at room temperature. It is attacked by Aqua Regia (a combination of sulfuric and nitric acid in parts 3:1) and slowly by hydrochloric acid and other oxidizing agents. It is resistant to ferric chloride at room temperature. Hydrobromic acid plus bromine attacks it at room temperature. All free halogens attack it at elevated temperature.

2.5 Commercially pure palladium[11]

99.85% Pd

Palladium finds extensive use in light duty electrical relays, where its freedom from tarnishing provides extreme reliability and noise free transmission required in voice circuits. Palladium is an important element in high temperature solder, and has low

vapor pressure. Contamination with low-melting point metals causes embrittlement. Contamination with base metals causes hardening and decreases corrosion resistance. Contamination with silicon causes loss of high temperature strength.

Density.	12.02g/cc.
Melting Point.	1552°C.
Coefficient of linear thermal expansion.	11.76um/m°K. 20°C
Specific Heat.	0.245Kj/Kg°K at 0°C.
Thermal Conductivity.	76 W/m at 0°C.
Electrical Resistivity.	108nOhm.m at 20°C.
	For an annealed wire 2.3mm

Corrosion. Generally palladium is less corrosion resistant than platinum, but more corrosion resistant than silver. In ordinary atmosphere palladium is resistant to tarnish, but some discoloration may occur during exposure to moist industrial atmospheres that contain sulfur dioxide. Adding palladium to gold or silver improves their tarnish resistance.

Resistance to specific corroding agents. At room temperature palladium is resistant to corrosion by hydrofloric, perchloric, phosphoric and acetic acids. It is attacked slightly by sulfuric, hydrochloric, and hydrobromic acids, especially in the presence of air.

Recrystalization temperature. 595°C

2.6 Gold-platinum[11]

70Au-30Pt

Gold-platinum conductor composition is used for high reliability multilayer interconnect hybrids. Gold-platinum has a good solder acceptance, thermal aged adhesion on alumina.

Density.	19.92g/cc.
Melting Point.	1228-1450°C.
Electrical Resistivity.	340 nOhm/m at 20°C.
	For an annealed wire 2.3mm
Recrystalization temperature.	1450°C

2.7 Platinum-palladium alloys[11]

Platinum-palladium alloys are used for electrical contacts without the addition of other alloys to provide for resistance to corrosion and add strength.

Electrical Resistivity.	300 nOhm.m at 40% Pd. (max)
	For an annealed wire 2.3mm
Temperature Coefficient.	0.1%/K from 40% Pd

Corrosion. An alloy containing less than 25% Pd performs the same as pure platinum in most chemical mediums. The resistance to nitric acid decreases as the palladium content increases. However, an alloy with only 2% Pt is as resistant to this reagent as a 14K gold alloy. Platinum rich alloys do not discolor when heated in air, but palladium rich alloys darken between 400-750°C.

2.8 Palladium-silver alloys[11]

Density. The densities can be calculated from the ratio of the components and the values of the same properties of the unalloyed material in g/cc.

Coefficient of linear thermal expansion. The coefficient of thermal expansion can be calculated from the ratio of the components and the values of the same properties of the unalloyed material in um/m°K.

Electrical Resistivity.	425nOhm/m at 36%Au.
	For an annealed wire 2.3mm
Temperature Coefficient.	0%/°C from 0-100°C at 40%Au

Corrosion. Alloys with more than 50% Pd resist tarnishing. Nitric acid dissolves all alloys, but they are quite resistant to hydrochloric acid, except in the presence of oxidizing agents. Cyanides attack all the alloys.

2.9 Palladium-silver-gold alloys[11]

40Ag-30Pd-30Au

Palladium-silver-gold alloys are easy to clad to other metals, and are used when high temperature resistance to corrosion is required and when other materials may present fabrication difficulties.

Chapter 3 - Assembly

3.1 Introduction

The assembly process in a thick film hybrid environment involves screening the paste onto the substrate, followed by stages in drying and firing. These steps may be repeated as many as four times depending on the number of circuit layers and the complexity of the circuit. A correction process follows involving the removal of the paste from the substrate where it exceeds the limits set in terms of its resistance, capacitance, etc. This process could involve laser trimming, or an air jet system for the removal of the paste. Assembly of surface mount components into the circuit for its satisfactory operation depends, to a large extent, on the layout of the circuit. The types of packages available and their interfacing into the circuit is as much dependent on the trace widths as on the element itself. This chapter provides the reader with a brief understanding of the mounting of a component into the circuit, for its robustness and operational integrity. Packaging is the process of providing mechanical and environmental protection for the circuit, and interconnecting the I/Os to interface with the rest of the circuit. A detailed examination of these processes is under taken in the next chapters.

3.2 Location and dispersion effects

The experiment of chapter 6 is developed based on certain parameters and stages, of which assembly is an important stage. Of the various steps involved during assembly, variables that influence the means of the process under investigation are called location effects. In certain practical situations dispersion effects or the variables that influence process variability are less of interest. Statistically designed experiments are widely used in product and process development to identify variables that effect the performance of the system.

3.3 Process description

Hallmark**[6, pg.178]** describes the processes involved and defines hybrid microelectronics as follows:

> Hybrid microelectronics is a packaging and interconnection technology for combining two or more semiconductor devices on a common interconnect substrate, typically to create a specific electrical function.

The semiconductor devices may be in the form of bare, unpackaged die or in miniature packages which mount on the interconnect substrate surface**[5]**. The interconnection pattern may include deposited resistors, capacitors, and inductors, which may even be in the form of passive components that may be mounted in chip form on the surface of the substrate.

Hybrid assemblies use both unpackaged and surface mount packaged semiconductor die. Passive components are typically in surface mount chip form. The use of unpackaged die minimizes size and weight, and reduces electrical parasitics and chip-to-chip propagation delays as discussed by Atkinson[1]. However, packaged devices are easier to pretest, easier to assemble, and do not require additional packaging of the completed hybrid circuit.

Attachment of the die to the substrate with epoxy adhesives and wire bonding is the most common method of bare die assembly. This approach as presented by Louis and Lando[10] does not require any special processing of the semiconductor die, increasing the number of devices available for hybrid assembly. However, the ability to fully pretest the die prior to assembly is limited, which adversely affects hybrid yield.

Unfilled die attach epoxies are thermally and electrically insulating[2]. By adding ceramic fillers such as Al_2O_3 or AlN to the epoxy, the thermal conductivity can be increased. If electrical conductivity is also required, Ag or Au particles are added instead of the ceramic fillers as discussed by Haskard[5]. Flexible epoxies can be formulated to minimize the stress associated with the assembly of large silicon die on an alumina substrate where the mismatch in CTE is approximately 2:1. If the subsequent assembly operations involve high temperatures (for example, solder package sealing at 350°C), epoxies may not be suitable and Au-Si eutectic bonding

may be used. Gold and silicon exhibit a eutectic melting temperature of 370°C at a composition of 6 %wt Si. For Au-Si eutectic assembly, the substrate metallization must be gold and the back side of the semiconductor die may be either silicon or gold metallized. With the die and substrate die bond pad heated to 420°C, the die is brought into contact with the gold die bond pad. A slight scrubbing action is used to break up any surface contamination, and the Au and Si interdiffuse. A eutectic liquid layer forms and grows as additional Au and Si dissolve. When the temperature is lowered below 370°C, the eutectic solidifies, forming a strong metallurgical bond. Au-Si eutectic die attach requires high temperature processing and does not provide stress relief for a large area silicon die.

Landers, Brown, et al.**[8]** in their text talk about attaching high power dissipating semiconductor die to the substrate. The die attach material often produces the highest thermal resistance in the packaging structure. High lead content solders (90%Pb/10%Sn, 95%Pb/5%Sn) are often used for the attachment of large power transistors and other high power dissipating devices. Solders have a higher thermal conductivity than filled epoxies. However, solders can fatigue and crack under the cyclic strains due to thermal or power cycling.

The electrical connection between the aluminum pads on the top of the semiconductor die and the substrate metallization are made by wire bonding**[8]**. In the wire bonding process, the wire is brought into contact with the metallized pad

and the wire is then deformed, producing a shearing action at the interface. This shearing action removes contaminants from the wire and the bond pad at the atomic level as presented by Landers, Brown et al.[8]. When sufficient cleaning has occurred, the exposed surface atoms from the wire and the bond pad, metallurgically bond to each other. Thermosonic bonding of gold wire combines heat, pressure, and ultrasonic energy in order to achieve the required deformation, although ultrasonic bonding of aluminum wire requires only ultrasonic energy and pressure.

Landers, Brown, et al.[8] discuss a second method for assembly of bare die, by the flip-chip solder attachment technique. This method implements solder bumps, which are formed on the die input/output (I/O) pads as the final step in wafer fabrication. The bumping process generates solder bumps "flipped" face down which are then used to assemble the hybrid, and the die. The contact with corresponding metal pads on the substrate is establish during the generation process where they are matched together. After this the substrate and die are heated simultaneously in a reflow oven to create the mechanical and electrical connections. Flip-chip assembly requires the smallest footprint and provides the lowest inductance (shortest) interconnection. The solder bumps can be placed as an array over the surface of the semiconductor die[5]. This allows a significantly higher number of I/O than can be achieved with perimeter I/O pads necessary for wire bonded interconnections[1]. Since special wafer processing is required, the availability of die for flip-chip assembly is limited[1].

Tape automated bonding (TAB) involves first bonding the die to a tape containing a copper lead pattern. The die are bonded to the metal leads through bumps on the die I/O pads. The bumps are fabricated in a process similar to that used for solder bumps. Landers, Brown, et al.**[8]** discuss the other methodologies and metallurgies that are used in the process examples. They are gold bump to gold plated lead with thermosonic bonding and gold bump to tin plated lead by laser solder reflow. The metal leads fan out the I/O to test pads to allow pretesting of the device prior to assembly on the substrate. The die can be assembled to the substrate in either a face-up or face-down configuration**[8]**. During assembly the die and segments of the metal lead are excised from the tape. In cases when the die is mounted face-up, the leads are typically soldered to the substrate metallization. Thermocompression outer lead bonding is used for fine pitch assembly**[8]**. In face-down bonding, the leads protrude horizontally beyond the edge of the chip and are bonded to the substrate metallization. Tape automated bonding generates bumps on the chip during the last step in the wafer processing and a custom tape for each chip I/O pattern. These factors have limited the availability of die in tape format**[8]**.

Certain other techniques which include adhesive bonded microbumps and z-axis elastomeric connectors are being used to attach and interconnect bare die**[8]**. Electrically conductive epoxy is often used to attach surface mount passive components to substrates assembled with bare semiconductor die**[8]**.

Surface mount components come in a variety of package styles including small outline transistor (SOT), small outline IC (SOIC), plastic leaded chip carrier (PLCC), quad flatpacks, and leadless ceramic chip carriers (LLCCC). These components are typically reflow soldered to the substrate metallization. The process involves screen or stencil printing the solder paste containing solder powder, flux, and a solvent onto the hybrid substrate. The components are placed with their leads in the solder paste so that they make the necessary electrical connection and provide for the mechanical bond strength of the connection with the substrate. The substrate with the surface mounted components is heated to melt or reflow the solder. The typical solder metallurgy is 62Sn/36Pb/2Ag, by weight**[8]**.

Hybrid microcircuits often combine multiple assembly techniques on a single substrate to meet electrical, mechanical, thermal, and component availability constraints see Table 3.1. This adds to the complexity of the assembly process**[1][8]**.

Table 3.1 Assembly process[8]

Interconnection substrate	**Assembly**
Thick film	Chip and wire
Thin film	Flip-chip solder attachment
Cofired ceramic or glass-ceramic packaged devices	Solder reflow of surface mount
Printed wiring board	Tape automated bonding

Chapter 4 -Packaging

4.1 Introduction

An operational electronic component not only contains the paths and traces for the electrons to flow, but provides the internal components with the rigidity in holding elements, compactness, and accommodates the roughness in handling by the end user. As much as assembly, packaging drives the circuit layout, including the width of the traces. A basic understanding of packaging technology is required for this research. A package provides mechanical and environmental protection for the circuit. It also provides I/Os to interface with the next level of system interconnections, and also acts as a heat dissipator and spreader. In determining hybrid packaging requirements, a number of factors must be considered including cost, reliability, electrical performance, end-use environment, and thermal management. A number of package styles are in use currently including leadless passive components, leadless active components, leaded plastic components, fine pitch and ultra-fine pitch technology, QFP/PQFP packages, and JEDEC packages.

Hybrids assembled with unpackaged die typically require some type of packaging or protection of the die. In high reliability applications such as military and medicine, the assembled substrate is sealed in a hermetic ceramic or metal package[9]. The

internal cavity of the package provides a benign environment (typically nitrogen or vacuum) for the hybrid circuit.

In other applications, plastic packaging is used[10][4]. The plastic is typically either molded around or coated and cured on the circuit. In some cases, liquid resins are applied directly over the bare die and cured[10]. In others, the assembled substrate is mounted in a plastic cavity package and silicone is poured over the substrate and cured. A number of variations are possible. Plastic packaging does not provide a hermetic environment because moisture permeates through the plastic. However, the adhesion between the plastic and the hybrid surfaces prevents condensation of water, which minimizes the potential for corrosion[10]. Hybrid circuits assembled with packaged surface mount components typically do not require additional packaging.

4.2 Hybrid microelectronics

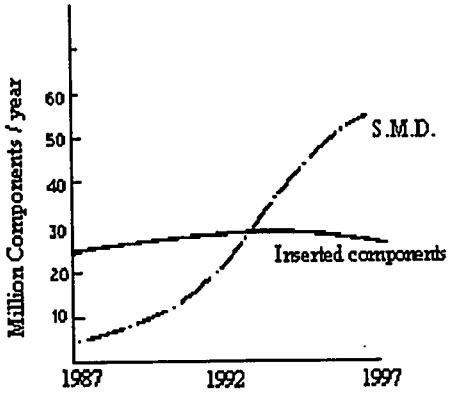
Hybrid microelectronics encompass substrate, assembly, and packaging options which can be combined to optimize the critical parameters for a given application. Electrical performance, size, weight, thermal characteristics, reliability, environmental requirements, design cycle time, and cost are all variables which factor into the decision to use hybrid microelectronics.

4.3 Surface mount technology[5][13][8]

Surface mount technology provides discreet advantages in passive element packaging some of which are noticeable with large-scale integration.

4.3.1. Related to the individual component: Large-scale integration of chips and high switching rates demand short leads of roughly equal lengths. This requirement can only be met with the close-pitch design of QFPs (quad flat packages) and TABs (tape automated bonding packages).

4.3.2 Related to the assembly as a whole: The number of functions per component, and consequently per assembly, has grown almost exponentially over the years since the introduction of surface mount technology. A fine-pitch-technology board is many times smaller than a board with the same functions but populated with through hole components only. Electronic devices like the controls for a camcorder, the circuitry of a cellular telephone, or a pacemaker are unthinkable without SMT. Figure 4.1**[13]** provides a forecast of trends in the use of surface mount components.



Forecast of electronic component usage (from Surface Mount Technology, BPA Ltd, Dorking RH4 1DF, UK)

Figure 4.1 Forecast of trends in SMT[13]

4.3.3. Related to circuit manufacture: Automatic insertion of fine-pitch wired components, even if it did exist, would pose insurmountable problems if they were to be directly attached and wirebonded to the circuit board (chip-on-board, COB)[1].

The details of surface mount and fine pitch technology (SMT/FPT) components, materials, and processes need to be known with the perspective of troubleshooting. Correcting or preventing problems requires a good understanding of the cause-and-effect relationships concerning these problems.

Packaging is to a very large extent decided by the type of component, either passive or active. Further, each of these can be packaged in two distinctly different surface mount packages - leadless and leaded. The largest number of leadless components are classified as passives - resistors, capacitors, inductors, etc. Another major group

of leadless components is leadless chip carriers. The newest packaging group is also essentially leadless, ball or column grid array packages (BGA/CGA). Although most of the packages with leads are active components, some passive components, such as resistor networks, can also use these packages**[8]**.

There has been a significant increase in the number of new SMT/FPT packages in recent times**[5][13]**. There exist certain variations in the multi-leaded packages, such as the popular small outline, quad flat package, grid array packages, and two terminal leadless package for passive components. Based upon history and technical papers given at leading conferences, there is no doubt that there will be many more new variations, as well as volume growth in the older types, in the future.

4.4 Leadless passive components[8]

Most of the solder paste technology and passive components currently used for SMT/FPT assemblies are a development of hybrid or thick film circuit technology. These components are similar in construction to through-hole components, but with different solderable terminations. This class of components includes multilayer ceramic capacitors, tantalum capacitors, and thick film resistors on ceramic bodies. They usually have rectangular shapes with a 2:1 length to width ratio which facilitates vibratory feeding**[8]**.

The fragile materials used in their construction cause many problems. The difference in the thermal coefficients of expansion (TCE), thermal conduction, and the relative strength of the materials are a major concern in the design of the casing.

Because of the TCE differences and the relatively brittle nature of the ceramic body, the ceramic capacitor can suffer both from mechanical cracks and from thermal shock stress induced cracks[8][9]. Thermal shock stress induced cracks arise from the soldering process, either by machine or by hand. Thermal gradients resulting from low thermal conduction can exacerbate normal thermal energy applications, resulting in low levels of thermal stress[9].

The mechanical cracks arise most frequently from pick and place machines or from hand assembly operation. Proper machine maintenance is necessary on the pick-up heads, to control the placement pressure.

Both thermal and mechanical cracks in ceramic capacitors can result in latent or catastrophic failure modes. Careful handling, such as not bending the printed circuit board (PCB) or applying soldering irons directly to the component, should be exercised during manufacturing and handling to prevent cracks[8].

Haskard[5] pointed out that tantalum capacitors also have potential TCE mismatch problems, due to the materials used in their construction, and they should receive

the same concern and care during soldering operations. Further, tantalum capacitors are polarized components and are sensitive to the placement orientation on the PCB. The tantalum package end that has the beveled edge is the positive (+) end. This must be matched to the correct soldering pad or land, usually also marked with a + sign. Polarized parts, that have an arrow or other markings, can cause a severe problem if they are not placed in the correct orientation.

4.5 Leadless active components[8]

The leadless ceramic chip carrier (LCCC) was one of the earliest forms of integrated chips**[8]**. It had solderable connections on all four sides, leading to the generically used term of "quad pack" for SMT packages of this form. Due to the requirement for a substrate that had a similar thermal coefficient of expansion (TCE), these packages have not been used abundantly. Unless implemented in an environment with a good TCE and temperature match, there can be considerable stress induced in the solder joints. This stress causes a solder joint reliability concern in applications that have many temperature cycles over an extended range. Due to the hermeticity and thermal conductance of the leadless ceramic chip carrier (LCCC), it proved to be a generally successful package for high reliability applications**[9]**. Applications varied from military and telecommunication, to small volume special functions where reliability and size were more important than minimum cost**[8]**.

Ball grid array (BGA) packages have become very popular for SMT during the last few years because of the slightly smaller footprint of the package for a given pin count. Since they are leadless packages, they too need a PCB with a compatible TCE for optimum reliability, as well as small geometry capability to handle the via and interconnect density of the grid array solder joints.

The plastic BGA intrinsically achieves this TCE match with certain PCBs. Landers, Brown, et al.[8] refer to one match as FR-4 (or equivalent) PCB, which has found significant acceptance for items such as cellular telephones and portable computers. Since these systems in general operate in temperature ranges that are limited by the user, there is less stress in the leadless solder joints and the reliability is acceptable. PCB area savings and process yield are the major advantages in using the BGA package[8].

For applications that are more demanding, either in thermal dissipation or temperature range/cycles, ceramic grid array packages can be used. They are produced with either ball or column grid arrays[5]. The solder column connections are approximately 75 mils tall, providing more compliancy than the solder ball connections. This compliancy reduces the probability of a crack formation, produces a slightly improved lifetime of the solder joints, and results in a higher reliability of the electronic system[4]. A compatible TCE substrate would be required to further minimize problems with cracked solder joints.

4.6 Leaded plastic components[8]

To solve the cracked solder joint and cost problems with ceramic chips, plastic leaded surface mount components were developed. The first small package, reportedly nicknamed SO for Swiss Outline, was developed for transistors and integrated circuits (IC's) used in electronic watches. An extension of the same into 14 and 16 leads is referred to as "Small Outline." Presently, SO is used to refer to a surface mount package with leads on two sides.

The thin liquid crystal display (LCD) requires a very thin package with a high lead count (40-60) to scan the calculator keyboard and drive the display. It implements it by using a plastic package, similar to the SO, but with leads on four sides, and is generally called a quad flat pack.

The leads of both the SO and quad flat pack are extended out from the body, either straight or with two right angle bends. This slightly resembled a sea gull in flight and resulted in the term "gull wing" leads[8]. The low profile of both packages left a very small space under the package which prevents easy cleaning, very important for many high reliability applications[9].

The plastic leaded chip carrier (PLCC), which had leads formed in a "J" shape, does away with some of the disadvantage with leadless chip components. Their body is

slightly thicker than the quad flat pack to improve reliability and space for the forming of the lead underneath. The "J" lead[8] produced a compliant connection between the package and the solder joint on the substrate, making it more reliable in a system required to endure many extreme temperature cycles. The IC also, occupies a smaller area on the PCB than the quad flat package. Because of the facility to tuck the end of the lead into a recessed cavity in the body, it is protected from bending, hence making testing and socketing easier[2].

A subtle advantage of the plastic chip carrier is that it has a compatible footprint with a ceramic chip carrier. Long term solder joint reliability can be achieved over commercial temperature ranges (0-80°C) with 20 pin LCCC's on an epoxy-glass circuit board[8].

The "gull wing" and "J" leads form a complementary set. The "J" lead does not perform well on a small outline 150 mil wide body, and because of the larger PCB area usage for the same body size and lead count, the "gull wing" is not practical for large memory systems with hundreds of memory packages on a PCB because of the area utilization for extended leads and solder joints[8].

The "I" lead was developed as a compromise to the difficulty of forming the "J" lead and the PCB space requirements of the "gull wing" lead. Despite some of its advantages, this lead form does not have the same level of acceptance or

standardization in the industry, except for the very recent Column Grid Array (CGA) package. Its major drawbacks are a slightly weaker solder joint and less lead compliancy than the "gull" or "J" leads[9]. They still find applications in custom packages and applications where through hole components are being used in SMT applications, as well as for the CGA package.

Similarly, there is a problem for the very high pin count packages[1][13]. The leads must be placed closer together, requiring them to be narrower and thinner, hence making the "J" lead form impractical. Thus, the "gull wing" lead form is used for a lead pitch, or center-to-center spacing, of less than 50 mils. Fine pitch technology overcomes these disadvantages.

4.7 Fine pitch and ultra-fine pitch technology[13]

Most SMT production uses 50 mil pitch packages. The processes that use packages in the 20-40 mil (0.5-1.0 mm) range were achieved with a basic SMT process, but with tighter process controls. This modified process, called fine pitch, is well established and there is a significant volume of IC packages with lead pitches in this range, both SO's and Quad's. However, there is also a growing need for an even denser packaging technology, one with high pin counts requiring a pitch that is smaller than 20 mils. This smaller lead pitch is necessary to facilitate lead counts in the 300 to 1000 range. The technology to achieve this appears to be significantly

different, and thus is given a different name, Ultra-Fine Pitch Technology, even though it was still a "surface mount" technology[8].

4.8 Definitions

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) first defined FPT as "the interconnection technology for fabrication and assembling IC packages with leads from 0.1 mm to 0.5 mm (4-20 mils)" (SMC-TR-001). This helped to distinguish where a different technology is needed from the "standard SMT." With this definition FPT was usually an individual placement and attachment process, compared to the mass placement and reflow solder attachment of SMT.

This definition helped greatly, but has been somewhat insufficient. Since the basic process used for 50 mil pitch components proved to be marginal for 1.0-0.5 mm (40-20 mil) pitch IC's, a revised process with tighter control has evolved and was usually referred to as a "fine pitch" process.

A printed circuit board consortium known as the "October Group" recognized this need and proposed that FPT be used to describe IC packages with a pitch of 1.0-0.5 mm (40-20 mils), and UFPT be used for pitches of less than 0.5 mm (20 mils). The former, FPT, requires a tighter control on the components, the substrate, and the attachment process (particular solder paste printing), but usually is also an individual placement and mass reflow process.

The latter category, UFPT, is usually a process of placement and attachment of one IC at a time. This technology then includes IC packages that have leads that are not pre-formed (such as carrier ring packages), chip scale packages (where the packages is equal to or slightly larger than the silicon chip), and the chip mount technologies (CMT) featuring tape automated bonding (TAB), flip chip, and chip-on-board (COB). It also includes thin film mounting technologies similar to what has been used in the past for Wafer Scale Integration (WSI). Assemblies manufactured with these technologies are usually referred to as multi-chip modules or MCM's

4.9 QFP/PQFP packages[13]

The primary driver for FPT/UFPT is the need for more input/output (I/O) connections. The 16 and 32 bit microprocessors, need higher pin counts on multiple memory address and data buses. It is not unusual to need 100+ leads. Application Specific IC's (ASIC's), that provide hundreds of logic gates in one package with pin counts of up to 300 pins, are common.

IC packages of larger than one inch on a side, in addition to taking up considerable space on the PCB, have subtle reliability problems due to the differences in the TCE of the plastic, silicon, and metal used in the IC package[9]. Moisture absorption during handling exacerbates the TCE problem, and is generally referred to as a

"popcorn effect." Depending upon the amount of exposure to ambient moisture, a bake of the IC package may be required before undergoing a soldering process[13].

Thus, to minimize the PCB area utilization and the potential package TCE reliability problem, leads are made smaller and closer together (fine pitch) allowing a smaller body, up to the minimum size allowed by the silicon chip and the IC package fabrication technique. The smaller IC package results in a lower stress build-up at the interfaces of the different materials, particularly the interface between the metal used to mount the silicon chip and the bottom plastic layer. The most common package used to achieve high pin count in a small area is the quad flat package[13].

JEDEC standards resulted in the bumpered corners and thicker body, known as the Plastic Quad Flat Package (PQFP) to distinguish it from the metric family of quad flat packages (QFP). The PQFP family has fewer members and tighter standards, and slightly better reliability during the reflow soldering process due mostly to a thicker plastic body. The QFP family is thinner with more variations in the package size to allowing it to minimize its practical size to match the silicon chip, with the lead pitch being the dependent variable to achieve the required lead count with the minimum size. As lead pitches drop to 0.4 mm and with package sizes of up to 40 mm on a side, the lead count can range up to 376. More recent standards have a closer lead pitch between the two versions of the quad flat packages.

Once the process for the fine pitch, high pin count package is developed, then other package forms can be used for low pin count memory and logic IC's. The thin small outline package (TSOP) with leads only on the ends for high density memory packaging (typically used in plug-in memory cards, such as PCMCIA modules), or the SSOIC/VSOIC (shrink or very small outline IC) packages for 20-56 pin count logic or interface circuits are typical. Generally SMT allowed a 2:1 reduction in packaging density from through-hole processing. FPT can usually achieve another 2:1 reduction from SMT. UFPT or MCM's, with their focus on minimizing interconnection distances, can usually achieve another 2:1 reduction from FPT**[14]**.

4.10 Package standards

IC and other component packages that have lead pitches of 50 mils could then be considered as "standard" SMT. SMT and FPT differ fundamentally on the principle of placement and soldering. This is because the tolerance requirements of the alignment and coplanarity of the IC package leads to the lands on the PCB, as well as the properties of the solder paste and printing, are very critical for high yielding mass placement and reflow technology**[8]**. Table 4.1 gives a summary of some common packages.

Table 4.1 List of major JEDEC packages [13]

PINS	SOIC 150	SOIC 300	PLCC	SO - J	PQFP
8	X				
14	X				
16	X	X (50 MIL)			
18			X (DRAM)		
20		X (25 &50 MIL)	X	X (1&4 MEG)	
24		X (25 &50 MIL)		X	
28		X (50 MIL)	X	X	
32			X (EPROM)		
44			X		
48		X (25 MIL)			
52			X		
56		X "			
68			X		
84			X		X
100					X
132					X
164					X

Table 4.1 also gives a list of the major packages that have been standardized by the Joint Electronic Device Engineering Council (JEDEC) of the Electronic Industry Association (EIA) (many more are standardized, but not as frequently used). This list is primarily the 50 mil pitch SOIC and PLCC. It also includes some of the 25 mil pitch SSOIC and PQFP packages. This list also includes rectangular PLCC's for memory application, where the silicon chip is relatively large and has a rectangular shape for use in DIP packages. The memory SO packages, with "J" leads, save approximately 25% of the board area when compared to "gull wing" packages**[8]**. These "SOJ" packages are also used in other applications, such as resistor networks.

The SSOIC/VSOIC package style (25 mil pitch) is included in the Table 4.1. It uses a body size that is slightly larger than the 24-28 pin count 50 mil pitch versions, but with 48 and 56 pins, respectively. The body thickness is the same, but the stand-off height of the package body is higher to provide for cleaning. There is also a 20 and 24 pin version with a body size that is approximately one-fourth of the 50 mil pitch

package area, and thus is sometimes called a Quarter Size Outline Package (QSOP)[8].

As discussed earlier, the plastic quad flat package (PQFP) resulted from an effort to design and produce a set of high lead count IC packages. These cover the range from 84 to approximately 200 leads, and for these the "J" lead is not practical. Trying to use the "J" lead form for fine pitch creates more problems with the lead thickness and minimum spacing than can be solved cost-effectively. Thus, the "gull wing" is the lead most highly preferred. It is easily produced in any size, thickness, and spacing. The JEDEC committees in the U. S. have standardized this package family with leads on 25 mil centers and a protrusion (bumper) on each corner to protect the leads. Table 4.2[8] lists some of the other QFP standard packages (Lead count by package size and lead pitch).

Table 4.2 Worldwide metric QFP standard packages [8]

Body\Pitch	1	0.8	0.65	0.5	0.4
10 X 10		44	52	64	80
14 X 14	52	64	80	96	120
14 X 20	64	80	100		
20 X 20				144	176
28 X 28		120-128	144-160	208	256
32 X 32			184	240	296
36 X 36				272	336
40 X 40			232	304	376

Chapter 5 - Standards

5.1 Introduction

The first point of consideration, of course, is that the component performs the proper electrical and/or mechanical function for the application. There are a number of standards that provide for uniformity within product families. The need to recommend a standard based on the outcome of the research requires the understanding of the standards that are available. For each of the activities performed as a part or whole of the process, in manufacturing a hybrid micro electronic circuit applicable standards are helpful. Industry organizations, such as Electronic Industries Association (EIA) and The Institute for Interconnecting and Packaging Electronic Circuits (IPC), provide leadership for development and coordination of standardization. These standards are for both electrical and mechanical properties of electronic components and for mechanical properties of the other items such as printed circuits, connectors, sockets, etc.

Standards are constantly evolving and at any point in time reflect the maturity of a technology. There are a number of package types that are not completely standardized or have dimensional values that have too wide a range to be easily used.

5.2 Standards organizations[8][2]

The major organization for component standardization is the Joint Electronic Devices Engineering Council, or more commonly referred to as JEDEC. Table 5.1**[13]** lists some of the standards and their publication numbers. JEDEC is part of EIA and issues specifications and standards for electronic components. JC-11 is the committee for standardization of IC packages, and thus has a major role in establishing the details necessary for problem free manufacturing of SMT/FPT.

Table 5.1 List of pertinent standards that include SMT/FPT components [13]

COMPONENT	STANDARD
Integrated Circuit	EIA JEDEC Pub. 95
Discrete Semiconductors	EIA JEDEC Pub. 100
Resistors/Capacitors	EIA PDP-100
Chip Capacitors	EIA RS-198
Tantalum Capacitors	EIA RS-228
Tape and Reel	EIA RS-481
Solder Test Methods and techniques	PC-S-805/J-STD-002

5.3 Planarity and solderability

Since SMT requires two coplanar surfaces to be held together with a metallurgical connection of solder, with little or no mechanical structure, special care must be taken in handling. The basic definition of coplanarity becomes dependent upon the ability of the solder to "bridge the gap" between the two surfaces. The solder alloy, the flux and solvent used in the paste, the reflow medium, and the solderability of the component and the PCB all have some impact on this desired performance**[1]**.

A general value for acceptable planarity of the component leads is no more than 4 mils off the seating plane. This value results from the typical capability of the component production equipment to form the leads and the ability of the surface tension of SN63 solder to bridge up to this gap. Greater separation between the package lead and the PCB than this increases the statistical probability of open solder joints.

The issue of solderability of the component and the PCB is a multi-faceted one. It includes the metal finish on the package lead, the metallization on the PCB lands, the solder alloy, the flux, the solder paste solvents, and the reflow or wave soldering system used to form the solder interconnection.

The standard **PC-S-805/J-STD-002** specifies that the solder can be either dipped or plated, and should contain 60-70% tin. If solder plating is used, a post-plating reflow should be performed. Recommended solderability test methods are given in **J-STD-002** and **Mil-Std-202**, with further guidelines of using 16 hours of steam aging and a solder pot temperature of 230°C to better simulate worst case SMT/FPT manufacturing requirements[7].

5.4 Handling considerations

To properly use the benefits of automation, the SMT/FPT components should be supplied in a carrier consistent with the feeders on the manufacturing pick and place machine. The industry standard defining the specification for tape and reel is the **EIA RS-481**. This handling method provides the highest quantity of parts in the smallest shipping volume[2]. It also helps in providing the largest number of different parts in the smallest volume for inventory storage and on the manufacturing pick-and-place equipment. Further, it helps to minimize handling damage on small components with fragile leads, thus decreasing losses due to planarity or lead skew problems.

For fine pitch components, the common shipping method is a waffle or matrix tray. These trays are especially designed to protect the fragile leads. The pick and place systems are adapted to handle these trays. The feeder table moves concurrently with the pick up head to provide the component for pick up and placement, and the tray feeder appropriately discharges the empty tray and presents a full one.

5.5 Component procurement requirements

When preparing a component procurement specification, there are several major points to remember. The document must accurately reflect the users need and the ability of the vendor to supply in a cost effective manner. Most vendors' standard

component specifications, as influenced by JEDEC or other comparable standards, are sufficient for general use.

There may be applications where special requirements must be identified. The information given in Table 5.2 is useful as a check list in preparing the procurement specification. It lists the major categories of consideration.

Table 5.2 Component procurement requirements

1. *Physical dimensions or outline drawings*

Body dimensions and tolerances

Lead dimensions and tolerances

Seating plane

2. *Standard test definition*

Electrical

Mechanical

3. *Process temperature capability*

Temperature profile

4. *Chemical requirements*

Symbol permanency

Solvent resistance

5. *Handling and shipping*

6. *Physical requirements*

Lead metallization

Solderability

Package integrity

Flame retardant

Symbolization

5.6 Standards documentation

Detailed documentation on standards can be obtained from

EIA: Electronic Industries Association

IPC: The Institute for Interconnecting and Packaging Electronic Circuits

Chapter 6 - Experiment

6.1 Introduction

The experiment developed and performed is a factorial experiment to determine factors affecting thickness and to attribute the cause of spread in the paste after firing the circuit and the circuit is ready for the next operation or assembly as a component into a more complex system of which it is a part. Both conductor and resistor paste were tested. Data sheets of the paste used as a part of the experimental process have been generated in part with the information relevant to the experiment performed.

6.1.1 Product information

6.1.1.1 Silver conductor paste

Silver conductor paste has a high conductivity and has expansion and shrinkage carefully matched to most common dielectrics. It is used for internal conductor structures and external ground planes. Table 6.1[5] lists conductor properties for a silver conductor paste. This information was supplied by the manufacturer.

Table 6.1 Typical conductor properties - silver conductor paste[5]

Viscosity[1]:	250 Poise
Solids Content:	69%
Fineness of Grind:	<20 micron
Print Thickness:	0.04 inch
Dry:	6-10 min
Fired:	3-5 min
Coverage[2]:	120 cm^2/g
Line Resolution:	5 mil (127 m) Line/Space
Resistivity[3]:	<1.5 Ohm.m/sq

Notes:
[1] Measured using Wells-Brookfield HBT cp51 viscometer, 9.6s-1, 25C.
[2] Calculated value.
[3] Normalized to 1 mil (25.4 micron) fired thickness.

Thinning:

Thinning of the paste is not generally recommended, since it is supplied with a suitable rheuology for screen printing. Ferroflo Thinner 0800 may be used to replace solvent lost through evaporation.

Printing:

325 or 400 mesh stainless steel screens with 15 mil emulsion thickness are recommended.

Drying:

The paste should be dried at room temperature for 15-60 minutes, or in conventional drying ovens at a maximum temperature of 70°C for 5-10 minutes.

Firing:

The paste is designed to cofire with silver conductor paste dielectric tape, when used for both buried and external layers in the silver conductor paste multilayer structure.

Paste storage and shelf life:

The paste should be stored in tightly capped containers, in a cool, dry place away from direct sunlight. Properly stored material will have a shelf life in excess of 12 months.

6.1.1.2 Mixed Metal Materials (MMM) system

Mixed Metal Materials (MMM) system is a unique thick film composition, for which patents have been applied. The material has been formulated for use in the via

connection between buried silver-based conductors, and external gold based conductors in the silver conductor paste multilayer structure. Table 6.2[5] lists conductor properties of the MMM system. This system eliminates Kirkendall voiding effects and results in a highly reliable interconnect.

The MMM construction takes advantage of silver's high conductivity for buried layers, with external layers of gold based materials, to produce high reliability, hermetic ceramic packages to be used in the most hostile of environments.

IMPORTANT: When using Mixed Metal Materials (MMM) system, the termination on the internal (silver) side of the MMM structure should be a catch pad, and on the external surface Au paste should be used. These catch pads should have radii a minimum of 1 mil (25micron) greater than that of the via.

Table 6.2 Typical conductor properties - MMM system[5]

Viscosity[1]:	10000 Poise
Solids Content:	87%
Fineness of Grind:	25 micron
Coverage[2]:	80 cm^2/g
Via Definition[3]:	100 micron

Notes:
[1] Measured using Wells-Brookfield HBT SC4-14/6 viscometer 1s-1, 25C.
[2] Calculated value.
[3] Minimum recommended via diameter which may be produced with standard via processing conditions.

Thinning:

Thinning of the paste is not generally recommended, since it is supplied with a suitable rheuology for application. Ferroflo Thinner 0800 may be used to replace solvent lost through evaporation.

Printing:

Two or 3 mil (50 or 75 micron) thick brass or stainless steel stencils are recommended.

Drying:

The paste should be dried at room temperature for 30-60 minutes, or in conventional drying ovens at a maximum temperature of 70°C for 5-10 minutes.

Firing:

The paste is designed to cofire with silver conductor paste dielectric tape, when used as a via fill for connecting silver to gold in the silver conductor paste MMM multilayer structure.

Paste storage and shelf life:

The paste should be stored in tightly capped containers, in a cool, dry place away from direct sunlight. Properly stored material will have a shelf life in excess of 12 months.

6.1.1.3 Palladium-silver conductor paste

Palladium-silver conductor paste is used as a solderable cofiring conductor on the external surface of multilayer constructions manufactured with the silver conductor paste system. Table 6.3**[5]** lists properties of palladium-silver conductor paste systems.

Palladium-silver conductor paste is a high conductivity product, which is carefully expansion matched to the silver conductor paste dielectric. It displays excellent solder wettability, adhesion and leach resistance.

Palladium-silver conductor paste has excellent compatibility with silver conductor paste dielectric and all of the products in the silver conductor paste ASB (All Silver Based) materials system.

Table 6.3 Typical conductor properties - palladium-silver paste[5]

Print Thickness:	12 mil
Dry:	15-20min
Fired:	8-12 min
Resistivity[1]:	10 Ohm m/sq.
Line Resolution:	5 mil (127micron) Line/Space
Solderability[2]:	1
Solder leach resistance[3]:	30
Initial:	>22N

Notes:
[1] Normalized to 1 mil (25.4 m) fired thickness.
[2] Dip seconds to reach >95% coverage, Sn62 solder, 215°C.
[3] Number of 1 second dips to reach <80% wetting, Sn62, 215°C.

Thinning:

Thinning FX 34-113 conductor paste is not usually recommended, since the paste is supplied at the correct viscosity for screenprinting. Ferroflo Thinner 0800 may be used to replace solvent lost through evaporation.

Screen printing:

325 mesh stainless steel screens with 12 mil emulsion thickness are recommended.

Drying:

The paste should be dried at room temperature for 15 to 60 minutes, or in conventional drying ovens at a maximum temperature of 70C for 5-10 minutes.

Firing:

The paste is designed to cofire with other dielectric tapes.

Paste storage and shelf life:

The paste should be stored in tightly capped containers, in a cool, dry place away from direct sunlight. Properly stored material will have a shelf life in excess of 12 months.

6.1.1.4 Resistor paste

The resistor paste is a silver and lead based resistor paste system and has a sheet resistance of 10k ohm. Table 6.4 lists the properties of the resistor paste used in the experiment.

Table 6.4 Typical resistor properties[5]

Viscosity[1]:	155 Kcps
Print Thickness:	dried: 20 microns, fired: 10 microns
Dry:	6-10 min
Fired:	10 min at 850°C
Coverage:	90-120 cm^2/g
Resistivity:	10.1K ohms/sq. on 1mm x 1mm

Notes:

[1] Brookfield HBT spindle number: SC4-14 speed: 10 rpm.

Thinning:

Thinning of the paste is not generally recommended, since it is supplied with a suitable rheuology for screen printing. Emflow 202 may be used to make up slovent loss.

Printing:

Use 250-325 mesh stainless steel screen to achieve a dried print thickness of 20 ± 2 microns.

Drying:

The paste should be dried at room temperature for 2-5 minutes, then in a conventional drying oven at a maximum temperature of 150°C for 10 minutes.

Firing:

Optimum results are obtained by firing at a peak temperature of 850°C for 10 minutes with a total cycle time of 36 minutes.

Paste storage and shelf life:

The paste should be stored in sealed containers, at 25°C.

6.1.1.5 Etchant solutions for pastes [5]

Etchant solutions are used to etch away the paste traces laid on the substrate, they are used in applications where the substrate needs to be cleaned, for reuse or as part of rework wherein some particular trace is erased from the circuit. Table 6.5 lists some solutions used to etch common pastes.

Table 6.5 Etchant solutions

Gold pastes	Temperature 55-60 degrees celcius 50 gms iodine 30 gms potassium iodide 400 ml ethanol and 50 ml DI water
Gold-palladium pastes	Temperature 20-30 degrees celcius 100 ml conc. Nitric acid 200 ml DI water
Silver pastes	Temperature 35-50 degrees celcius 35 gms ferric nitrate 40 ml DI water 10 ml conc. Nitric acid
Palladium-silver pastes	Temperature 35-50 degrees celcius 35 gms ferric nitrate 40 ml DI water 10 ml conc. Nitric acid

6.2 Types of experiments

The experimental design implemented in this research is a factorial design. Since data was generated through tests there were no probabilistic techniques used. A brief review is provided of the styles and methodologies of experimental design.

Rifle Shot Experiment.

The analysis of available data may point strongly to only one or two suspected variables. In such a case it is common to avoid extensive experimentation by focusing on the suspected variables. Such studies are known as Rifle Shot experiments.

Unbridled Experiment.

In the absence of strong suspicion about several variables being dominant, the trial approach takes the form of an Unbridled experiment. In this form a batch of products is followed through the successive processes under a plan which provides for making measurements of many of the suspected materials and processes.

6.3 Purpose

This experiment studies the thickness and spread in the screened paste after the firing operation is complete as seen in Figure 6.1 and Figure 6.2. The arrow marks in the figure indicate the area of spread. The hypothesis for the experiment is "width spread of the screened paste trace is not a function of time and temperature within the normal firing range." Spread in the trace after firing can cause a number of problems with the circuit, some of which are:

- limiting the distance between the traces laid out on the substrate which otherwise might result in a short circuit. Too much spread can cause the traces to touch and short circuits to form.

- forcing large spaces between traces which can lead to larger substrates and heavier circuits.
- adding to future processing by forcing trimming of components.

The thickness of a trace is another important parameter. The resistance of a resistor paste is a function of the thickness, the length, and width of a trace. Thus, it is one of the important factors that needs to be controlled and maintained in the manufacturing of a thick film circuit.

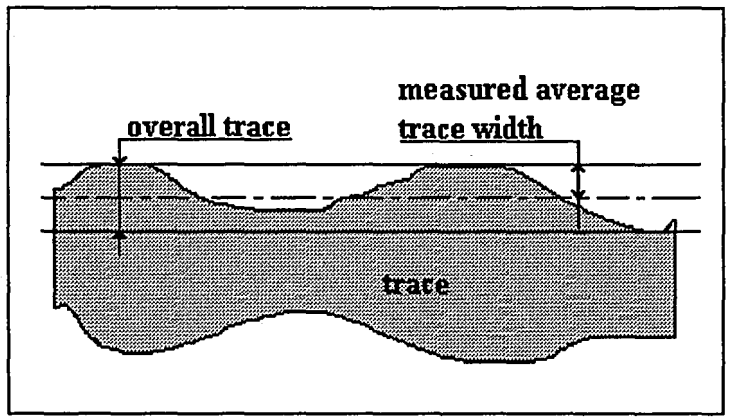


Figure 6.1 Width spread

Figure 6.1 shows a drawing of the trace and points within, as perceived in the experiment. The figure exaggerates the spread from the actual width of the trace. In the figure the shaded region is the trace. The two solid parallel lines represent the overall spread over the width of the trace. In this experiment, the average peak has been measured, (marked between the center line and any of the solid lines.). The act

of averaging is performed by observation and estimation. Figure 6.2 shows an actual image of overall trace spread as viewed from the microscope.

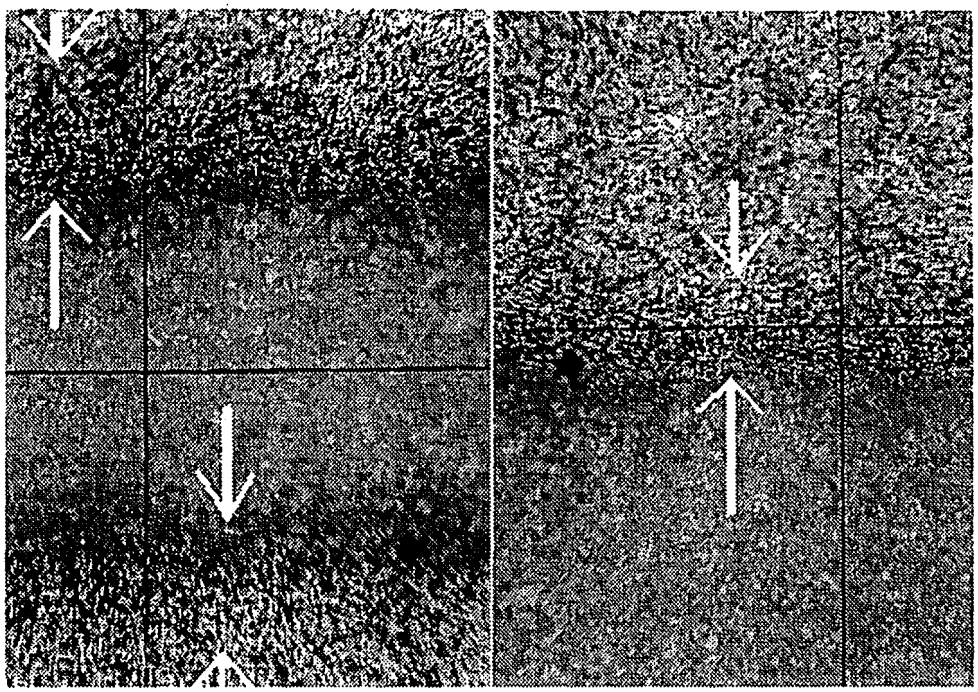


Figure 6.2 Width spread pictured from the microscope (zoom: 33 times)

The equipment used in the laboratory to perform the experiment include:

Thick film screen printer	Presco Model: MSP873.
Screen size	320 mesh stainless steel, 8 inches x 11 inches, 10 lb tension force.
Drying oven	Vitronics Model: SMD-310
Firing oven	RTC Model: LA-306H
Substrate	Alumina, 97%. Camber 2°
Microscope	Micro Dynascope Model: 5E

6.4 Experimental setup

Screen printer: The screen is mounted onto the screen holder. Areas of the screen that are not intended to be screened with paste are masked with cellophane tape on the underside. Height adjustment is made on the Z axis using the adjusting screw on the left side. The snap height is maintained at the default value. The air supply to the system is set at the required level and the electric power is turned on.

Drying oven: The Vitronics oven is a convection/infrared system. To start it the power supply and computer are turned on. The computer is interfaced with the control system of the oven. At startup the computer loads the control information, allows the user to select a new profile, and sets the temperature in °C for each zone. For these experiments the following settings were used:

zone 1: 275 **zone 2:** 350 **zone 3:** 350 **zone 4:** 350

zone 5: 260 **zone 6:** 300 **zone 7:** 300

belt speed: 4 inches/min

Firing oven: The RTC oven is an infrared furnace system, with radiant heating. To use it the compressed air supply must be attached to the system. The air flows are adjusted to distribute the compressed air to every zone. The air flow into each of the areas is measured by flowmeters, in LPM. The knobs at the base of the flowmeters can be used to vary the flow rate in each individual zone. For these experiments the following settings were used:

Exhaust venturi	Entrance baffle	Zone 1 N_2	Zone 2-3 N_2	Seal N_2	Exit baffle	Cooling
8	14	28	28	10	14	28

The power supply is turned on and the heating elements at the top and the bottom in each of the individual zones are turned on. The temperature in each zone is adjusted to the required value, in °C.

Depending on the trial being tested the temperature settings were changed. The settings used for each of the levels the experiment performed are shown.

1. **High - Zone 1:** 650 **Zone 2:** 850 **Zone 3:** 900
2. **Low - Zone 1:** 650 **Zone 2:** 850 **Zone 3:** 850

The experiment is ready to start as soon as the system temperature stabilizes.

Microscope: There are no specific settings for the microscope. The 20X lens is used. The microscope and the associated lights are turned on. Finally the computer interface is turned on and the "Measure Graph 1-2-3" software is started.

6.5 Procedure

The paste is screened onto the substrate. Next, the paste is allowed to settle in open air for 20 minutes. The substrate is then run through the drying oven (Vitronics oven) which heats the substrate to 250-300°C, as it passes through the 7 zones. The zones are split into a preheating zone 1, and three additional zones. Each of the

following three zones are split into top and bottom with separate controls. The drying process drives out the volatile materials and moisture contained in the paste. The process takes about 12 minutes. The drying process is followed by firing in the radiant heating oven at about 850°C and held at that temperature for 10 min. The radiant heating RTC oven provides three zones of control. In each zone, the top and bottom heaters can be turned on and off independently. The substrate is then allowed to cool and the thickness and spread are measured under the microscope that is connected to a computerized data collection system.

6.6 Experimental design

The experimental design is developed based on Douglas Montgomery's *Statistical Process Control in Manufacturing*[12]. The process variables evaluated are shown in Table 6.6 and include temperature of firing in degrees Centigrade(°C), time for firing in seconds and method of heat application (both top and bottom or top only). The uncontrollable variables are thickness of the paste laid out on the substrate and spread of the trace laid out as a part of the circuit. The experiment assumes that there are no three way interactions. The experiment varies the controllable parameters, such as time through the firing oven, heat application, and temperature of firing, in order to determine their effects on the response variables thickness and spread, to achieve high resolution, better line width and spacing. Table 6.7 shows the experimental settings. Table 6.9 and Table 6.10 show the individual readings taken for the experiment.

Table 6.6 Location and dispersion effects

Main effects	Response variables
Temperature (**A**) in °C.	Thickness (of paste) (**D**) in inch.
Time (**B**) in seconds.	Width spread(**E**) in inch.
Heat (**C**)top heater, or both top and bottom on.	

$2^{(3)} = 2^8$ factorial design.

Table 6.7 Experimental settings

	High +	**Low-**
Temperature	900	850
Time (belt speed)	3.1 inch/min	2.7 inch/min
Heat	both	top

During the experiment the belt speed is changed to vary the time parameter. The speed is set so that it takes the required number of minutes to travel from the start of the furnace heating zones and the end not inclusive of the cooling region. The temperature settings are changed by adjusting the zone control units. Finally, the heat application is varied by turning on and off the top and bottom heating elements.

The process variables in this experiment concentrate only on the firing process. The drying process is disregarded.

Table 6.7 shows the conditions under which each of the trials was run. A " +" indicates a high on the effect and "-" indicates a low on the effect. The high and the low effects were previously defined in Table 6.7.

Table 6.8 Highs and lows in the effects

		A	B	AB	C	AC	BC	ABC
I	**1**	-	-	+	-	+	+	-
a	**2**	+	-	-	-	-	+	+
b	**3**	-	+	-	-	+	-	+
ab	**4**	-	+	+	-	-	-	-
c	**5**	+	-	+	+	+	+	+
ac	**6**	-	-	-	+	-	+	-
bc	**7**	+	+	-	+	+	-	+
abc	**8**	-	+	+	+	-	-	+

6.7 Experimental results and discussion - spread

In Tables 6.9 and 6.10 the experimental results from the tests conducted on conductor paste and resistor paste respectively are shown. The highs(+) and lows(-) are representative of the levels discussed in Table 6.7.

Table 6.9 Experimental results - conductor paste

Time	Temp	Heat	Spread	Thickness
+	+	+	0.033	0.006
-	+	+	0.030	0.006
+	-	+	0.031	0.004
-	-	+	0.033	0.006
+	+	-	0.030	0.005
-	+	-	0.033	0.006
+	-	-	0.031	0.006
-	-	-	0.033	0.006

Table 6.10 Experimental results - resistor paste

Time	Temp	Heat	Spread	Thickness
+	+	+	0.054	0.015
-	+	+	0.050	0.012
+	-	+	0.052	0.015
-	-	+	0.054	0.015
+	+	-	0.050	0.015
-	+	-	0.054	0.016
+	-	-	0.052	0.015
-	-	-	0.054	0.016

The ANOVA shown in Table 6.11 decomposes the variability of spread into contributions due to various factors. The contribution of each factor is measured having removed the effects of all other factors. The P-values test the statistical significance of each of the factors. Since no P-values are less than 0.05, none of the

factors have a statistically significant effect on spread at the 95.0% confidence level.

Table 6.11 Analysis of variance for spread - conductor paste

Source	Sum of Squar	Df	Mean Square	F-Ratio	P-Value
MAIN EFFECTS					
A:Heat	0	1	0	0	1
B:Temp	5.00E-07	1	5.00E-07	0.11	0.7952
C:Time	0.000002	1	0.000002	0.44	0.6257
INTERACTIONS					
AB	0	1	0	0	1
AC	0.0000045	1	0.0000045	1	0.5
BC	0.000002	1	0.000002	0.44	0.6257
RESIDUAL	0.0000045	1	0.0000045		
TOTAL (CORRECTED)	0.0000135	7			

There is no significant effect from the three main effects: time, temperature, and application of heat on the spread. In the first interaction plot shown in Figure 6.3, the effect of heat does not depend on the level chosen for temperature. It is noted that the two lines, 1 and 2, are approximately parallel, indicating a lack of interaction between the factors heat and temperature. Figure 6.4 shows the second interaction plot. The plot indicates an interaction effect between heat and time. However, the values are not statistically significant.

In the third interaction plot shown in Figure 6.5, there is interaction between temperature and time, but once again the values are not statistically significant.

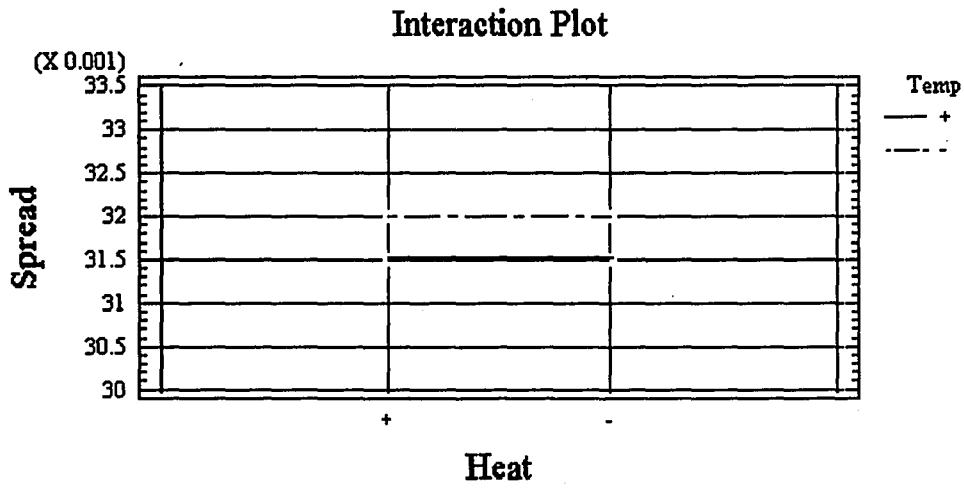


Figure 6.3 Interaction plot heat against temperature - conductor paste

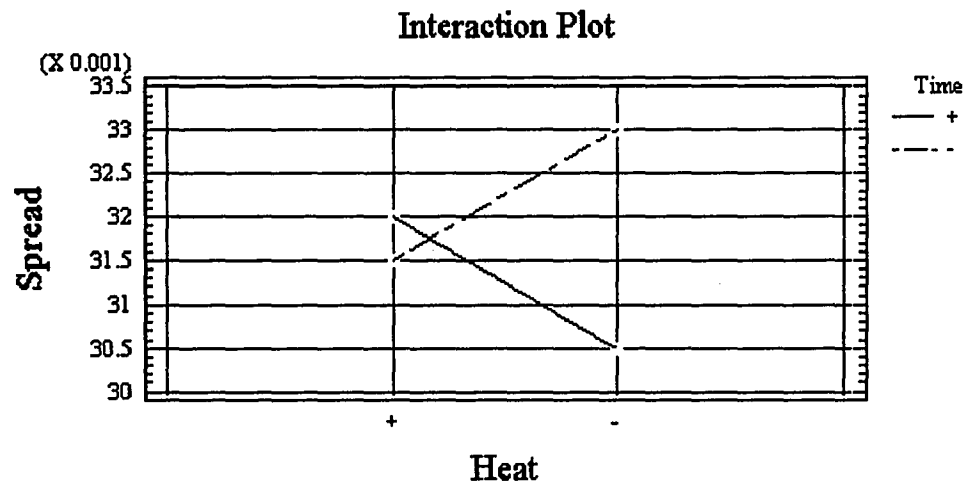


Figure 6.4 Interaction plot heat against time - conductor paste

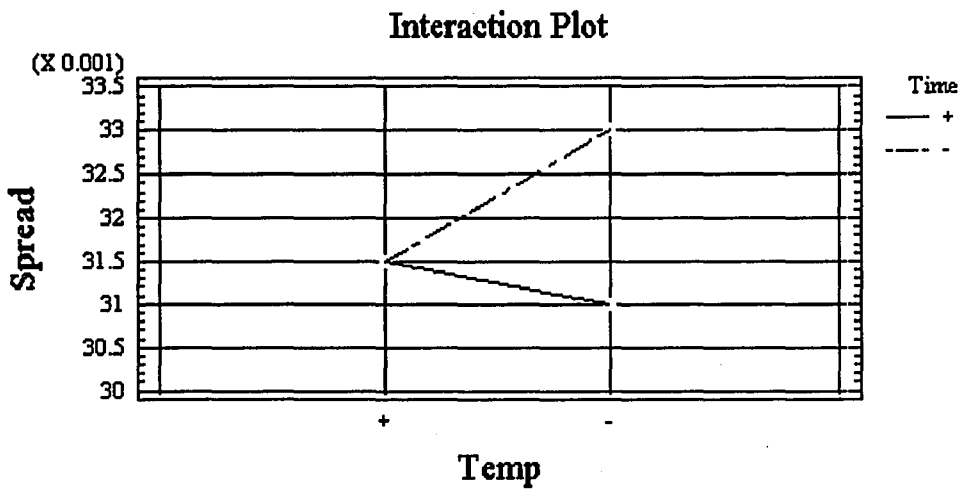


Figure 6.5 Interaction plot temperature against time- conductor paste

A second experiment was performed using resistor paste. The results are shown in Table 6.10. The design of the experiment is the same as the experiment for the conductor paste. Since the two experiments are performed independently at different time periods they cannot be integrated unless blocked. Table 6.12 shows the resulting ANOVA table.

The ANOVA for spread of resistor paste is shown in Table 6.12. Since none of the P-values are less than 0.05, none of the factors or interactions have a statistically significant effect on spread at the 95.0% confidence level.

Table 6.12 Analysis of variance for spread - resistor paste

Source	Sum of Squares	Df	Mean Square	F-Ratio	P-Value
MAIN EFFECTS					
A:Heat	0	1	0	0	1
B:Temp	0.000002	1	0.000002	0.25	0.7048
C:Time	0.000002	1	0.000002	0.25	0.7048
INTERACTIONS					
AB	0	1	0	0	1
AC	0.000008	1	0.000008	1	0.5
BC	0.000002	1	0.000002	0.25	0.7048
RESIDUAL	0.000008	1	0.000008		
TOTAL (CORRECTED)	0.000022	7			

In the first interaction plot shown in Figure 6.6, slight interaction trends are shown. However they are not statistically significant. Similarly, Figure 6.7 for heat and temperature, shows a slight interaction as seen in the graph but its value as calculated in the ANOVA table indicates that the interaction is not statistically significant. The third interaction plot shown in Figure 6.8, determines the heat and temperature interaction. Statistically there is no significant interaction for these parameters.

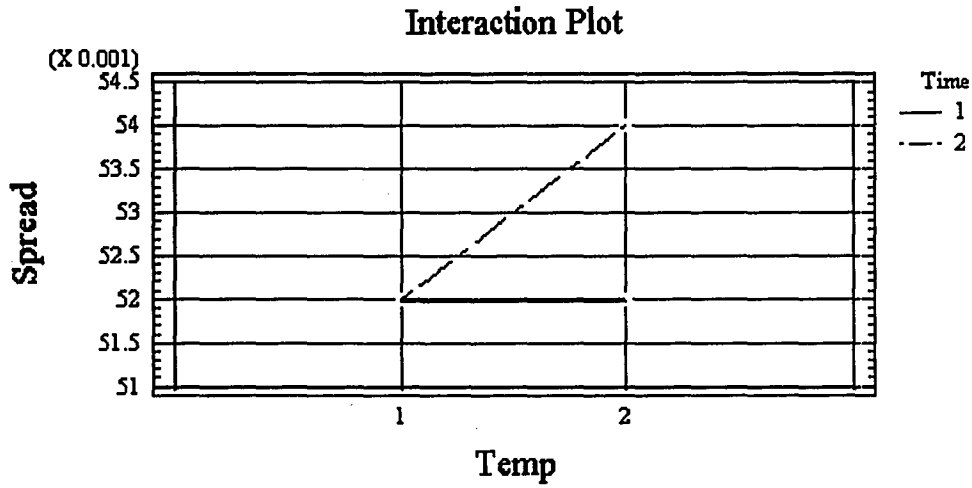


Figure 6.6 Interaction plot temperature against time- resistor paste

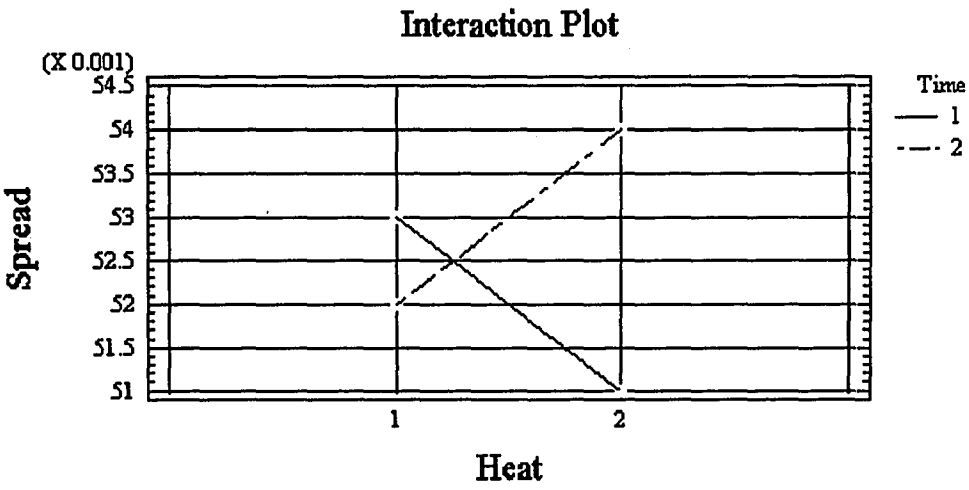


Figure 6.7 Interaction plot heat against time - resistor paste

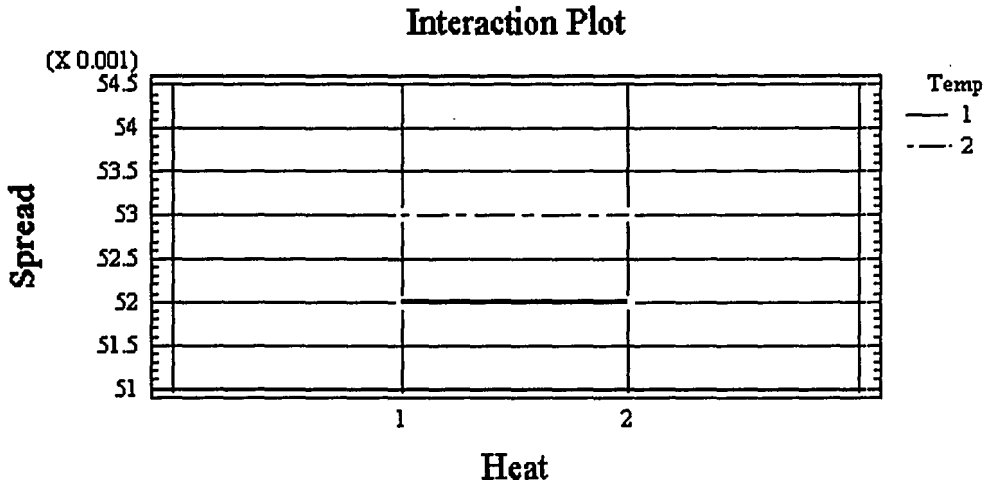


Figure 6.8 Interaction plot heat against temperature - resistor paste

Although the graphs indicate that there exists some slight interactions, the ANOVA clearly indicates that there is no significant interaction. Montgomery**[12]** mentions that the interaction plots at times indicate different results than the ANOVA and must be used only as an aid to analyze the results.

6.8 Summary of spread

The interpretation of results from the ANOVA tables indicate that the main effects time, temperature and heat do not have a significant effect on the spread. The interaction plots between temperature and time, indicate that this interaction does not have a statistically significant effect on the spread at the 95% confidence level.

6.9 Experimental analysis and discussion - thickness

The analysis of the thickness is performed separately with the same assumption that there are no three way interactions. The ANOVA table for the conductor paste is generated and presented in Table 6.13 and the one for resistor paste is presented in Table 6.14.

Table 6.13 Analysis of variance for thickness - conductor paste

Source	Sum of SqDf		Mean Square	F-Ratio	P-Value
MAIN EFFECTS					
A:Heat	1.25E-07	1	1.25E-07	0.11	0.7952
B:Temp	1.25E-07	1	1.25E-07	0.11	0.7952
C:Time	1.13E-06	1	0.000001125	1	0.5
INTERACTIONS					
AB	1.13E-06	1	0.000001125	1	0.5
AC	1.25E-07	1	1.25E-07	0.11	0.7952
BC	1.25E-07	1	1.25E-07	0.11	0.7952
RESIDUAL	1.13E-06	1	0.000001125		
TOTAL (CORRECTED)	3.88E-06	7			

The ANOVA Table 6.13 decomposes the variability of thickness into contributions due to various factors. The P-values test the statistical significance of each of the factors. Since no P-values are less than 0.05, none of the factors or interactions have a statistically significant effect on thickness at the 95.0% confidence level.

Table 6.14 Table Analysis of variance for thickness - resistor paste

Source	Sum of SqDf		Mean Square	F-Ratio	P-Value
MAIN EFFECTS					
A:Heat	3.13E-06	1	0.000003125	2.78	0.344
B:Temp	1.13E-06	1	0.000001125	1	0.5
C:Time	1.25E-07	1	1.25E-07	0.11	0.7952
INTERACTIONS					
AB	1.13E-06	1	0.000001125	1	0.5
AC	3.13E-06	1	0.000003125	2.78	0.344
BC	1.13E-06	1	0.000001125	1	0.5
RESIDUAL	1.13E-06	1	0.000001125		
TOTAL (CORRECTED)	1.09E-05	7			

In the ANOVA Table 6.14, no P-values are less than 0.05. Therefore, none of the factors or interactions have a statistically significant effect on thickness at the 95.0% confidence level.

6.10 Summary of thickness

The main effects time, temperature and heat have any statistically significant effect on the thickness of the trace. The interaction effects between time and temperature, time and heat, and temperature and heat also have no statistically significant effect on the thickness.

6.11 Overall summary

In both the experiments it is clear that the main effects time, temperature, and heat do not influence the spread and thickness of the traces on the substrate. The

interaction of the controllable variables also, has no statistical significance. Manufacturers literature provides information on the trace width, and the resolution possible. Since these vary with paste type, it is possible that paste type will influence the variables. Furthermore, observation of paste rheuology during the experiments shows that this factor may also effect spread and thickness.

Chapter 7 - Process

7.1 Introduction

Most modern manufacturing facilities implement the state-of-the-art in manufacturing hybrid microelectronic circuits. The process advanced so quickly that modern equipment is usually not available in university laboratories. Early research in thick and thin film related to superconducting and buffer layers. Later it developed into the use of substrates such as $SrTiO_3$ and $LaAlO_3$ for high frequency applications. As such most literature on super conducting to some extent covers thin and thick film research and development. To some extent this literature takes a look at some of the processes that can be implemented but due to lack of resources in the laboratory could not be put to practice. The processes discussed have been adopted from the section of the Metals Handbook**[11]** called Properties and Selection: Alloys and Special-Purpose Materials.

The main deposition techniques currently used are:

- Electron Beam Coevaporation.
- Sputtering from either a composite target or multiple sources.
- Laser ablation (also called pulsed laser deposition).

Chemical deposition has been the slowest of the methods to come on line, but recent results suggest that in time it may become competitive.

7.2 Electron beam coevaporation[5]

This is one of the earliest techniques to have given successful results in terms of deposition. This procedure typically requires separate sources for each component of the circuit, much like the process for manufacture of thick film, when screening elements on the substrate. This multi-source evaporation creates problems with accurate rate control of each of the sources (especially if a large oxygen pressure is present) as well as geometrically induced composition variation. Applications involving the study of experiments performed in this thesis have particularly related to flat substrates with a camber of 2°(degrees) and substrates of size 4 inch x 4 inch. (One important feature is that since these are line compounds, stoichiometry is very important). Oxidation of the sources is less of a problem here than in sputtering. This allows greater possibilities of *in situ* film growth. Certain alloys allow patterning of deposited films by photolithography after which an anneal produces the required properties.

7.3 Sputtering[5]

Film deposition by sputtering can be done with either a single composite target or with multiple sources.

Composite target sputtering avoids geometric compositional variation as well as a need for good rate control. The main drawback involves the difficulty in obtaining the desired composition in the film (which does not necessarily match the target composition). This can be addressed either by adjusting target composition or by varying sputtering conditions such as location of substrates. The latter results because of bombardment of the film surface by negative oxygen ions. By moving the substrates to the side, stoichiometric films were obtained.

Multiple target sputtering has greater flexibility to vary composition but has drawbacks due to oxidation of the barium target and rate control. In the end composite sputtering seems to have the advantage.

7.4 Laser ablation (or pulsed laser deposition)[5]

Laser ablation uses a composite target of the desired composition that is exposed to a focused laser beam from a pulsed excimer laser. The area vaporizes and is projected in a narrow forward plume to the substrate. Laser ablation may need a post annealing, but high quality *in situ* films are generated.

7.5 Future outlook

Laser ablation and composite target sputtering seem to be the most promising deposition methods with Electron Beam codeposition also being competitive, especially for *in situ* films.

Chapter 8 - Quality Plan

8.1 Acceptance sampling

Any acceptance sampling application must distinguish whether the purpose is to accumulate information on the immediate product being sampled or on the process which produced the immediate product at hand. Based on this principle two sampling plans have been laid out[12][9][7]. This chapter reviews the plans and policies of acceptance and rejection, as applied in manufacturing. The procedures are adaptable to an electronic manufacturing environment. Suggestions are provided in the latter part of the chapter.

Type A: Sampling to accept or reject the immediate lot of product at hand.

Type B: Sampling to determine if the process which produced the product at hand was within acceptable limits.

The type of sampling will determine the appropriate probability to be used in characterizing the performance of the plan. In addition the type of data generated will also play a role. In acceptance sampling, data can be of these types:

- Acceptance go no-go information

  Defectives-usually measured in proportion or percent defective. This refers to acceptability of limits of products for a wide range of characteristics.

Defects-usually measured by actual count or as a ratio of defects per unit. This refers to number of defects found in the units inspected, and hence can be more than the number of units inspected.

- Variable measurement information

  Variables usually measured by the mean and standard deviation. This refers to the distribution of a specific measurable characteristic of the product inspected.

8.2 Acceptance sampling procedures

Sampling plans are of two types: attributes plan and variables plan**[12][7]**.

Attributes Plan: In these plans a sample is taken from the lot and each unit classified as conforming or non-conforming. The number of non-conforming is then compared with the acceptance number stated in the plan and a decision is made to accept or reject the lot. Attribute plans can be classified with one of two basic criteria:**[14]**.

1. Plans can meet specified sampling risks and provide protection on a lot-by-lot basis. Such risks are:

   a. A specified quality level for each lot (in terms of percent defective) having a selected risk (say 0.01) of being accepted by the consumer. The specified quality level is known as the lot tolerance percent defective ($p2$); the selected risk is known as consumer's risk (β)

   b. A specified quality level for each lot such that the sampling plan will accept a stated percent (say 95 percent) of the submitted lots having

this quality level. This specified quality level is termed the acceptable quality level (AQL). The risk of accepting a lot of AQL quality ($p1$) is known as the producer's risk (α)

2. Plans which provide a limiting average percentage defective items for the long run. This is known as the average outgoing quality level (AOQL).

Variables Plan: In these plans, a sample is taken and a measure of a specific quality characteristic is made on each unit. These measurements are then summarized into a simple statistic (e.g., sample mean) and the observed value compared with an allowable value defined in the plan. A decision is then made to accept or reject the lot. When applicable, variables plan provide the same degree of consumer protection as attributes plan while using considerably smaller samples.

Attributes plan are generally applied on a percent defective basis. That is, the plan is instituted to control the proportion of accepted product which is defective or out of specification. Variables plan for percent defective are also used in this way. Such plans provide a sensitivity greater than attributes but require that the shape of the distribution of individual measurements must be known and stable. The shape of the distribution is used to translate the proportion defective into specific values of process parameters (mean, standard deviation) which are then controlled.

Variables plan can also be used to control process parameters to given levels when specifications are directed towards the process average or the process variability and

not specifically to percent defective. These variables plan for process parameters do not necessarily require detailed knowledge of the shape of the underlying distribution of individual measurements.

Sampling plans used in reliability and in the sampling of bulk products are generally of this type. Published plans in the reliability area, however, usually require detailed knowledge of the shape of the distribution of lifetimes.

8.3 Types of sampling plans

In single-sampling plans, the decision to accept or reject a lot is based on the results of a single group of units drawn from the lot. In double-sampling plans, a smaller initial sample is usually drawn, and a decision to accept or reject is reached on the basis of this smaller first sample if the number of defectives are either quite small or quite large. A second sample is taken if the results of the first are not decisive. Since it is necessary to draw and inspect the second sample only in borderline cases, the average number of pieces inspected per lot is generally smaller with double sampling. In multiple sampling plans, one, or two, or several still smaller samples of n individual items are taken until a decision to accept or reject is obtained.

8.4 Sampling schemes and systems[7]

While simple sampling plans are often employed solely in sentencing individual lots, sampling schemes and systems are generally used in acceptance control applications

involving a steady flow of products from the producer**[14]**. The ANSI/ASQC Standard A2 (1987) defines a sampling plan as "... a specific plan that states the sample size or sizes to be used also states the associated acceptance and non-acceptance criteria on the amount of 100 percent inspection and sampling."**[14, pg 25.8]**. The definition and nomenclature Subcommittee of the ANSI Z-1 Committee on Quality Assurance defined a sampling system as a "Unified collection of one or more sampling schemes"**[14, pg 25.79]**. Thus n=134, c=3 is a sampling plan; Code J, 1.0 percent AQL is a sampling scheme; and **MIL-STD-105D**, or its civilian version ANSI/ASQC Z1.4, is a sampling system.

A collection of given sampling procedures depends upon the extent and nature of quality history. Thus, with a supplier having an average quality history, it may be beneficial to start a single sampling plan, switch to an AQL scheme after moderate quality history has been obtained, and then to skip-lot, supplier certification, or control chart procedures when extensive excellent history has been generated.

8.5 Plan suggestion

Exponential distribution **(MIL-STD-690B, MIL-STD-781C)**.

MIL-STD-690B is concerned with "process qualification" Military Standard (1960). This standard provides plans that evaluate the ability of the process to produce electronic parts that meet specified failure rate requirements. It presents three sets

of plans based on failure rates expressed as a percentage per thousand hours of operation (Table I, II, and IV).

The standard is intended as a tool for assessment of:

1. Qualification of the process at the initial failure rate level.
2. Extension of qualification to lower failure rate levels.
3. Maintenance of failure rate level qualifications.
4. Lot conformance failure rate inspection.

Operating characteristic curves for the qualifying plan are provided and confidence levels are also specified. The plans involved are similar in operation to the time terminated sampling plans presented in **(H108)**. The *Reliability Handbook* **H108**, presents a set of life test and reliability plans based on the exponential model for time to failure. The plans contained therein are intended for use when mean time to failure is specified in terms of acceptable mean life and unacceptable mean life. MIL-STD-781C provides a standard set of acceptance testing plans for both pre-production reliability qualification and reliability acceptance in production. This standard was developed for electronic equipment as contrasted to Military Standard 690B developed for electronic parts. MIL-STD-781C is devoted to test conditions and procedural considerations. The plans are expressed by mean time between failures. Appendix C of the standard presents the following plan:

1. Fixed length test plans.

2. Probability ratio sequential tests.

3. Short run high risk probability ration sequential test plan.

4. All equipment reliability test.

Expected test time curves are presented for probability ration sequential test plan. The sequential tests operate in a manner similar to the ones in **H108**. The fixed length tests are similar to the time terminated tests of **H108**. The plans in MIL-STD-781C are indexed by producer's risk α, consumer's risk β, and discrimination ratio θ_0/θ_1. Operating characteristic curves are given for the sequential tests, equipment and fixed length tests.

Chapter 9- Visual Basic Code

9.1 Application of code[15]

The code has been written to develop a user interface to the experimental and manufacturer's data. It helps to present in a comprehensive manner the results of the experiment along with data collected from journals and papers. The GUI presents the user with a screen to enter various types of information. Figure 9.1 shows the GUI at the startup of the program, when the user selects **New** from the **File** menu.

The code is available through the Industrial and Manufacturing Systems Engineering (IMSE) Department at Lehigh University.

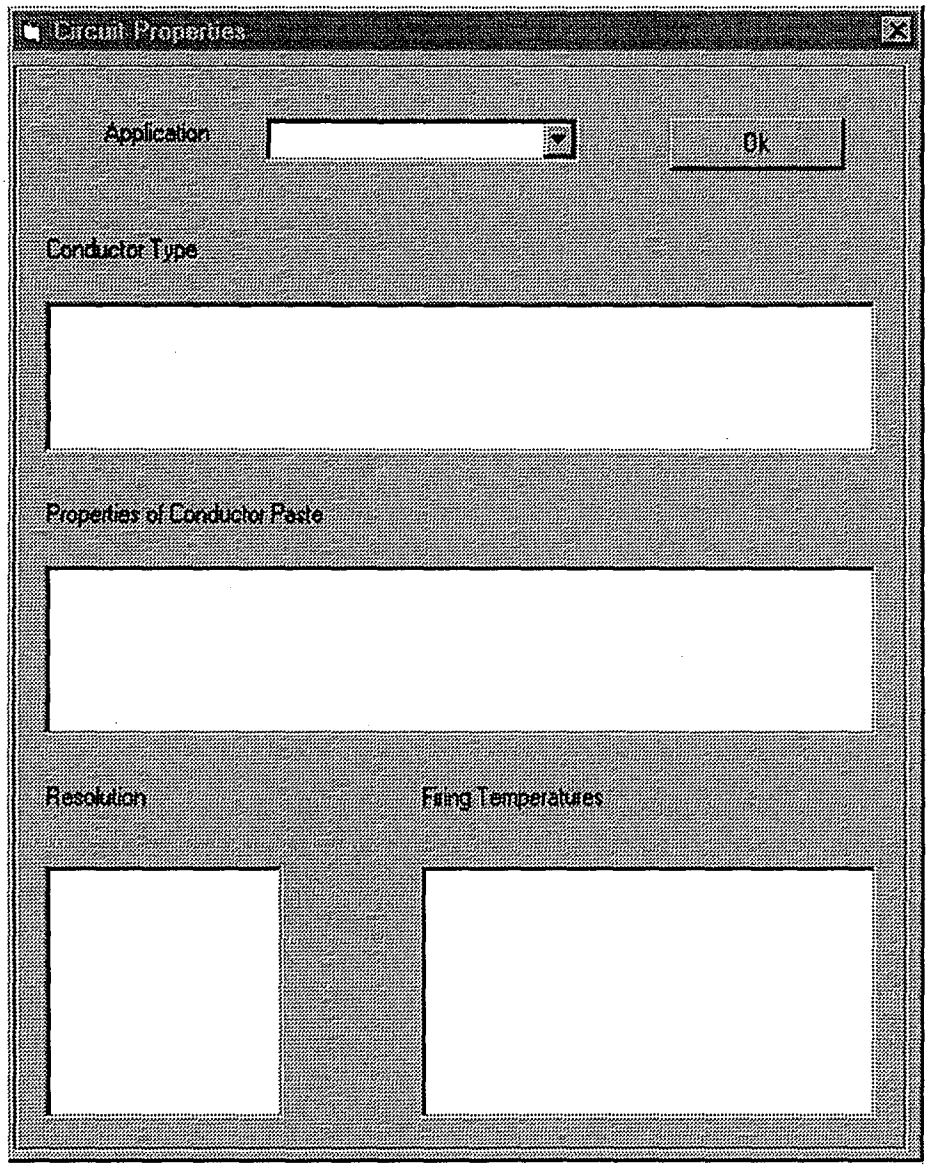


Figure 9.1 Visual Basic application-circuit form

The user selects the application to which the circuit is to be applied e.g. automotive, high density multilayer circuit, single layer double sided circuit, etc. Based on the user selection, the code loads the most typical conductor paste material used in the application. It also provides the user with the information on the expected resolution that can be obtained, conductor paste's metallurgical properties, and firing temperature.

Figure 9.2 show the response when trying to **Save** a file. The files are in "*.TFC" (Thick Film Circuit) file format.

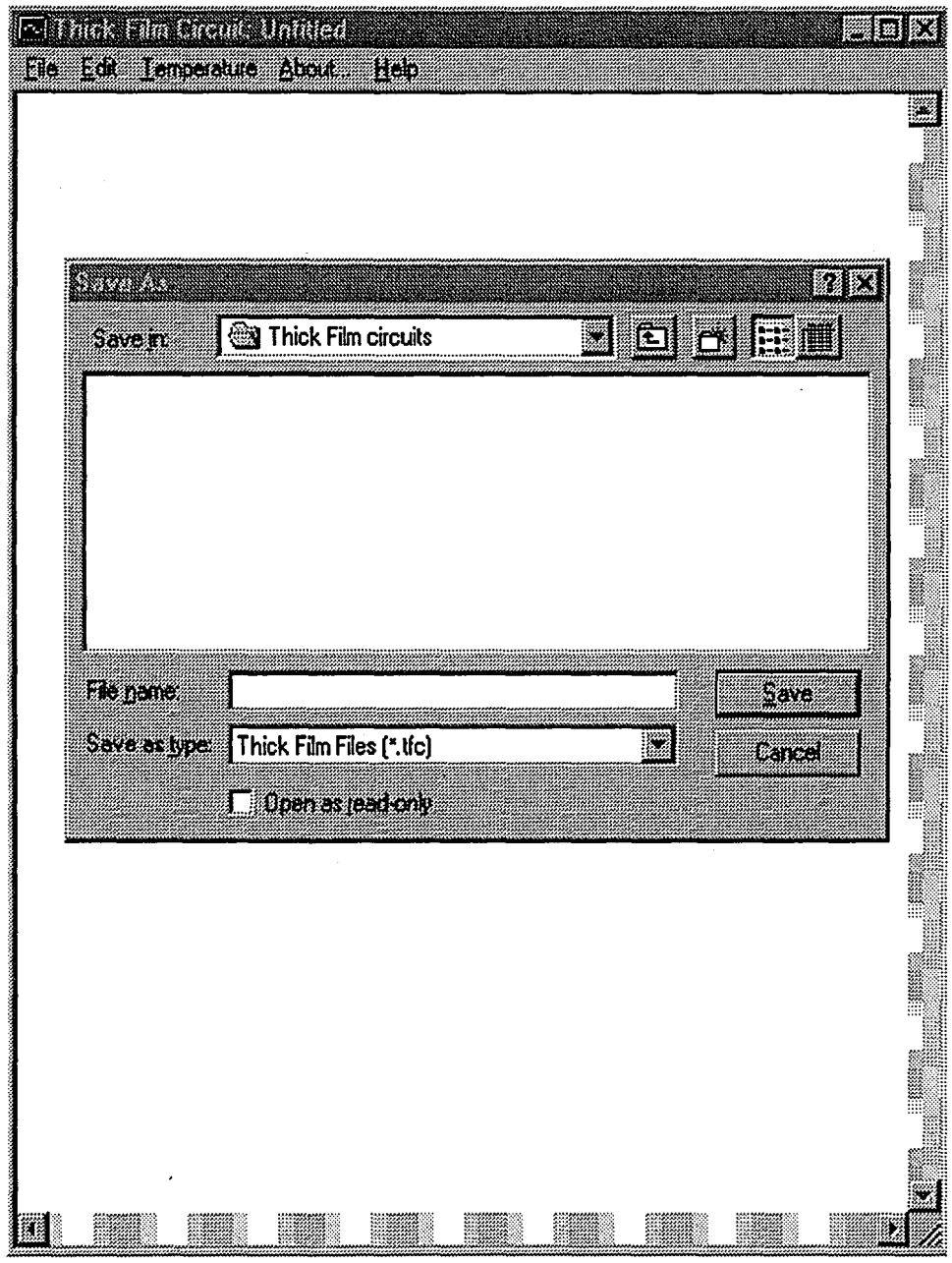


Figure 9.2 Visual Basic application-Save file

The **Temperature** option allows the user to change temperature from Fahrenheit to Celsius and vice versa as seen in the Figure 9.3.

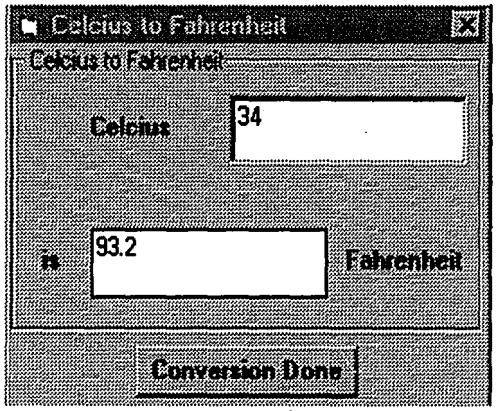


Figure 9.3 Visual Basic application-celcius to fahrenheit conversion

There is a **Help** menu as shown in Figure 9.4 that provides the basic information needed to run the program for new users. And the **About** in Figure 9.5 tells the user about the creator of the program.

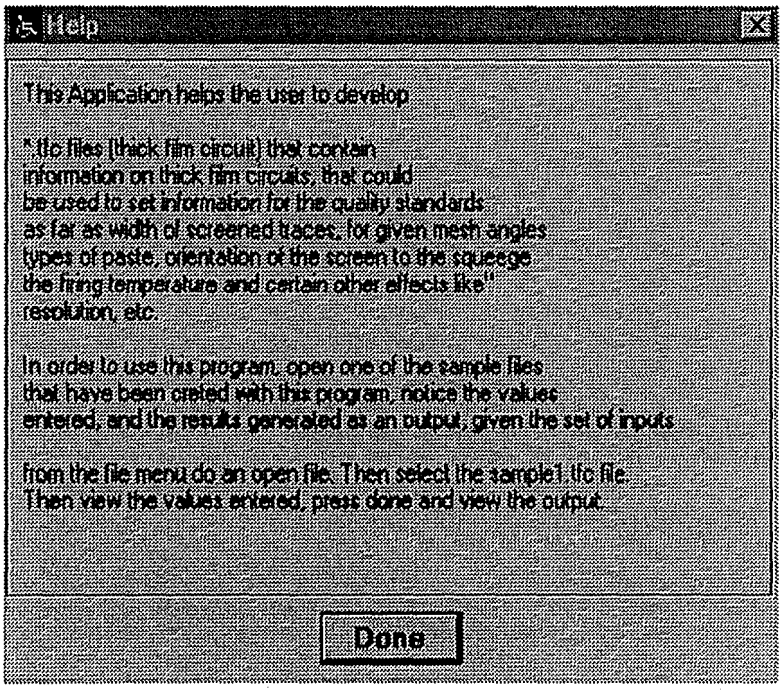


Figure 9.4 Visual Basic application-Help file

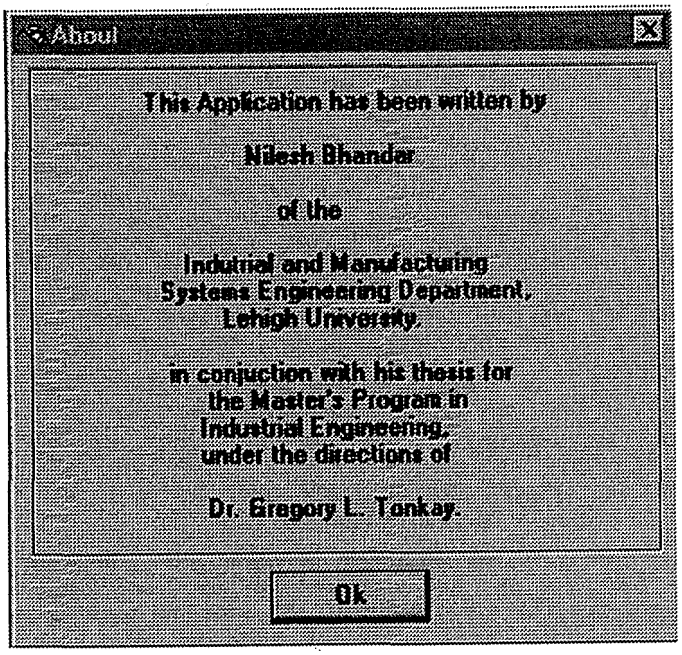


Figure 9.5 Visual Basic application-About file

This application loads the table data from an Excel application file of the following kind:

Application.xls

Automotive
High density multilayer circuits
Single layer/Double sided

Automotive.xls

Pt/Pd/Ag
Pd/Ag
Pt/Ag

hdmc.xls

Ag
Pd/Ag
Au

Ag
Pd/Ag
Au

slds.xls

Ag
Pd/Ag

thickfilm.xls

Conductor Metal	Firing Temp	Coverage
Pt/Pd/Ag	850C	~70 cmsq/gram
Pd/Ag	850C	~70 cmsq/gram
Pt/Ag	850C	~75 cmsq/gram
Ag	850C	~70 cmsq/gram
Au	850C	~65 cmsq/gram
Pt/Au	850C	~50 cmsq/gram
Au multisys	850-925C 10 min	~50 cmsq/gram

* All firing temperatures are on Alumina Substrates

Resolution	Film thickness	Resistivity
250u lines and spaces	11-15 u	<=40 mohms/sq at 12 u
125u lines and spaces	10-14 u	<=15 mohms/sq at 12 u
250u lines and spaces	10-12 u	<= 5 mohms/sq at 11 u
250u lines and spaces	11-15 u	<= 3 mohms/sq at 12 u
175u lines and spaces	6-8 u	<= 8 mohoms/sq at 8 u
250u lines and spaces	11-15 u	<= 100 mohms/sq at 13 u
200u lines and spaces	9-13 u	<= 4 mohoms/sq at 12 u

Chapter 10 - Future Outlook

10.1 Introduction

This thesis presents the results of a study designed to determine the parameters influencing the manufacturing of thick film and hybrid microelectronic circuits. The designed experiment provides the analysis of multiple factors such as time, temperature, and application of heat as controllable parameters and the thickness of the conductor laid out and width spread as the uncontrollable parameters. The deductions from the experiment provide a sound conclusion that the temperature, time, and application of heat do not influence the width spread.

10.2 Scope for future work

This study did not find the parameters that influence the width spread of thickness of the trace. In conducting the experiments, behavior of the pastes and screening processes suggested that future studies should be conducted. Specifically there seemed to be a difference in the rheuology of the resistor and conductor paste that affected both thickness and width spread. Additional experiments should be conducted with different rheulogical combinations of the same pastes. The screening process probably also affects the thickness and width spread. Parameters of

screening such as mesh size, mesh angle, snap-off distance, force, etc. could be varied. Additional types of pastes and screening speed could also affect the process.

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Vita

Nilesh Bhandar was born on the 30th day of August, 1974 in Bombay, India, to Dr. (Mrs) Rajkuwar Bhandar and Satish Bhandar. He graduated with a Diploma in Mechanical Engineering from M.H.S.S. Polytechnic in Bombay with the highest honors when he stood first in the State of Maharashtra. Before he joined the highly esteemed Lehigh University he finished his Bachelors in Mechanical Engineering from Victoria Jubilee Technical Institute, of Bombay University with an honors.

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TITLE