Single-Event Effect Pe… ance of a Commercial ReRAM

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Abstract: *We show heavy ion test results of a commercial production-level ReRAM. The memory array is robust to bit upsets. However, the ReRAM system is vulnerable to SEFI.*

INTRODUCTION

Non-volatile memories are widely used in space systems for data and code storage. However, options for radiation-tolerant memories are limited. The commercial demand for high-density mass-storage electronic devices has driven the rapid development of floating-gate flash memories to its scaling limits. The International Technology Roadmap for Semiconductors named Reduction-Oxidation Random Access Memory (ReRAM) as a promising candidate to replace flash [1]. The ReRAM structure consists of a metal-oxide insulator (TaO_x, HfO_x, TiO_x, etc.) between a top and bottom electrode. In TaO_x systems, an applied electric field creates an electrochemical reaction which dissociates anions (O^{-2}) at the top or bottom electrode. The oxygen vacancies can migrate across the insulator to form a conductive link between the electrodes. An electric field of opposite polarity breaks the conductive link.

The ReRAM is naturally hardened against ionizing radiation, since it does not store charge. Previous studies have shown that the ReRAM structure can be hardened up to several Megarad(Si) of total ionizing dose (TID) and up to 10^{14} ions/cm^2 of proton fluence [2]−[4]. However, there is currently no knowledge on the single-event effect (SEE) performance of ReRAM. Furthermore, the existing published data have only evaluated test structures or memory arrays. The circuit level response can include unique error modes with significant impact to device operation [5]−[7]. In this study, we investigate the SEE performance of a commercial production-level ReRAM.

DEVICE DETAILS

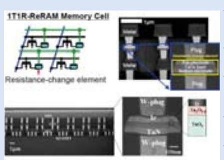

Fig. 1. Schematic of the ReRAM array architecture, and cross section images of the array and ReRAM cell [8].

- Panasonic MN101L 16 bit microcontroller with embedded ReRAM
- Industry's first mass production-level ReRAM
- 1T1R array architecture, with CMOS access transistor to each ReRAM stack
- Resistive memory stack: $Ir/Ta_2O_{5-\delta}/TaO_x/TaN$
- Conduction through electron hopping via oxygen vacancies
- Fabricated back-end-of-line in a 180 nm CMOS process

Table I.
MN101L ReRAM electrical characteristics and reliability specifications.

Function	Description
Memory Size	64 KB
Program Endurance	Program area (62 KB): ≥ 10^3 Data area (2 KB): ≥ 10^5
Programming Voltage	1.8 to 3.6 V
Reading Voltage	1.1 to 3.6 V
Data Retention	10 years at 85°C

EXPERIMENTAL DETAILS

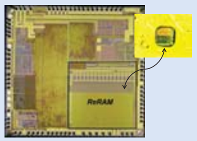

Fig. 2. MN101L microphotograph showing the ReRAM array and peripheral circuits. The inset picture shows the collimator revealing only the ReRAM. *(Image courtesy of NASA Jet Propulsion Laboratory)*

- Acid etched TQFP080-P-1212F plastic case and exposed the entire die surface
- Collimator exposed only the ReRAM
- Created a "window" in a kovar lid using an Ultra-Tech ASAP-1® surface preparation machine. Kovar collimator approximately 10 mils (254 μm), which stops the majority of the test facility heavy ion energy spectrum.
- The collimator shields other components of the microcontroller aside from the ReRAM, such as the static random access memory (SRAM), logic circuits, and analog circuits.

Fig. 3. Hea… TAMU. T… Panasonic…

Irradiation Facilities

- 15 MeV/amu heavy ions at Texas A&M University (TAMU), in air
- 16 MeV/amu heavy ions at Lawrence Berkeley National Laboratory (LBNL), in vacuum
- 590 nm pulsed-laser at the Naval Research Laboratory

Table II.
Heavy ion species, energy, LET and range at TAMU and LBNL.

Ion	Total Energy (MeV)	LET (MeV·cm²/mg)	Range in Si (μm)
Ar (TAMU)	642	7.27	256
Kr (TAMU)	1225	24.98	165
Xe (TAMU)	1955	49.29	148
Kr (LBNL)	886	30.9	113
Cu (LBNL)	659	21.2	108

Test Condition…

- Used Panasonic's evaluation board as te…
- Vcc = 3.3 V, Frequency = 8 MHz or DC
- Test modes:
  - Static
  - Continuous read
  - Continuous read/compare/write
  - Continuous write
- Data patterns: 00, FF, 55, and AA
- Actively monitored the light emitting diod… that is connected to the I/O address regi… probes. The indicator signals the functio… microcontroller.

RESULTS

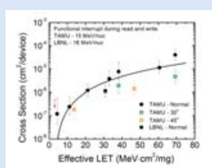

Fig. 4. SEFI cross section vs. effective LET for the MN101L microcontroller. Irradiation was performed on the ReRAM circuit.

- No single-event upset (SEU) from static test.
- Single-event functional interrupt (SEFI) was the dominant error mode.
  - Most susceptible during continuous read or write
  - Most events caused the microcontroller to stop reading/writing immediately
  - SEFI also observed following some static runs
  - Static mode SEFI not observed if DUT is reinitialized, which clears address buffers
  - No column, page, or block errors as commonly observed in flash memories
- Similar cross sections for read and write test mode.
- Angular effects due to beam shadowing from the kovar collimator. Degraded beam produced cross section >5× relative to angular beam at same effective LET.

Fig. 5. Address locations of various SEE modes … memory space.

- Bit upsets characteristics:
  - Include single-bit and multiple-bit ups…
  - Error address locations distributed thr… microcontroller memory bank, and
  - 8 SEUs in the ROM.
- 1 locked mode event possibly due to S… device security function, 1 part failed f… krad(Si)).

RESULTS

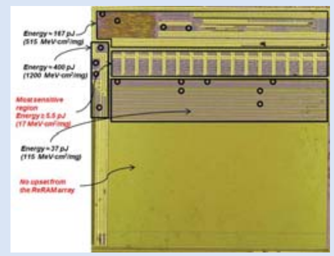

Fig. 6. Microphotograph of ReRAM array and peripheral circuits on the MN101L microcontroller. The different regions are identified according to their upset sensitivity to pulsed-laser.

Fig. 7. Microphotograph of the sense amplifier circuit of the ReRAM. Sensitive spots are identified.

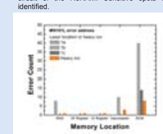

Fig. 8. Error memory address locations for errors observed during heavy ion testing, and errors from the sense amplifier circuit during pulsed-laser test.

- Probed the ReRAM array and surrounding peripheral circuits with a 20× lens with a beam diameter of 1.7 μm to identify the sensitive regions.
  - Different sensitive regions are shown on the left with respective upset energy thresholds.
  - No errors were found from the ReRAM array.
- Most sensitive region, which consists of sense amplifier circuit, was investigated further with a 100× lens, with a beam diameter of 0.9 μm, and the energy was fine-tuned to determine the upset energy threshold (Fig. 7).
- Energy threshold at Location 1 (Fig. 7) was comparable to heavy ion results.
  - Read mode: 5.5 pJ (17 MeV·cm²/mg); Write mode: 8.6 pJ (26.5 MeV·cm²/mg)
- SEFI memory addresses and error characteristics from laser test are similar to those from heavy ion test.
  - Stops reading/writing,
  - Continuously reading out errors from the ROM,
  - Stuck reading at end of Bank0 (FFFF), and
  - Continuously reading errors from other address locations beside the ROM.

DISCUSSION

Bit errors are an important part of the SEE response for floating-gate non-volatile flash memories, particularly for multiple-level cell devices, where multiple-bit upsets make up a significant portion of the overall radiation-induced bit upset rate [5]. The scaling potential of ReRAM raises additional questions about its multiple-bit upset sensitivity, which worsens with diminishing device dimensions. The results presented here show that the ReRAM array in the MN101L microcontroller is extremely robust against heavy ion irradiation. We did not observe any ion-induced bit upsets during either the static or dynamic test modes. The access transistors in the 1T1R architecture are susceptible to SEUs. However, the test results showed that the memory array is hardened against errors due to access transistor upsets, likely owing to the bipolar operating nature of the ReRAM. The "set" and "reset" states require polar opposite potentials for operation. The access transistor controls the voltage potential at one electrode, while the bit line controls the potential at the other electrode. Switching between states requires a change in the voltage potential at both terminals. Therefore, a SEU from the access transistor alone is insufficient to cause an incorrect write/read to the ReRAM, provided that the signal on the bit line remains uncorrupted.

SEFI dominated the SEE response. Pulsed-laser testing identified the sense amplifier circuit as a sensitive region for SEFIs. SEU in the sense amplifier circuit caused some of the microcontroller hang-ups. The SEFI error cross sections are similar for the read and write mode. The response differs from SEFIs occurring in flash memories, where the cross sections from program or erase are typically different than that from the read mode [5], [7]. This is partly due to the similar voltage levels required for a read or write operation in ReRAM technology. The lower voltage level required to perform erase or write eliminates the need for charge pumps and reduces the circuit complexity. The elimination of charge pumps is particularly beneficial for the part's radiation tolerance. Charge pumps are especially susceptible to total ionizing dose and destructive single-event effects.

Many factors aside from radiation would need to be considered for actual space flight applications. Here, we evaluate the on-orbit event rate of the SEFIs. We used a maximum likelihood method to determine the Weibull fit for the cross section of normal incident irradiation as shown in Figure 2 [9]. The Weibull fit parameters for the best fit are: LET_{th} = 2 MeV·cm²/mg, saturating cross section = 6.6 × 10^{-4} cm², W = 370, and S = 2. The corresponding heavy ion event rate for an orbit similar to the international space station is approximately 1.6 × 10^{-5} upsets per day during solar minimum. The fact that the ReRAM array is immune to upsets makes the ReRAM technology promising for space applications. The suitability of ReRAM technology for space flight will be partly determined by the application tolerance to the SEFI error rate, which depends on the SEE sensitivity of the CMOS peripheral circuits.

CONCLUSION

We have investigated the single-event effect performance of the embedded ReRAM in the MN101L microcontroller. We observed a total of 15 SEUs from the heavy ion test, which included single-bit and multiple-bit upsets. A pulsed-laser test confirmed that the SEUs did not originate from the ReRAM array. Therefore, the ReRAM array is immune to ion-induced upsets up to LETs as high as 70 MeV·cm²/mg. We also found that the CMOS access transistors, although theoretically susceptible to SEUs, do not necessarily lead to upsets in the array. We believe that this is due to the operating principal of the ReRAM cell, where polar opposite potentials are required to set or reset the memory.

Single-event functional interrupt dominated the SEE response of the MN101L. Pulsed-laser testing showed that the sense amplifier contained vulnerable circuits sensitive to SEU, which can lead to functional interrupt of the microcontroller. However, the pulsed-laser may be limited by penetration range. So there are likely other CMOS structures in the peripheral circuits that are susceptible to heavy ions.

Nevertheless, the SEFI error rate for this device is relatively low. However, the consequence is significant, since each SEFI requires a reset or power cycle for recovery. The ReRAM cells appear to be intrinsically hardened against heavy ion-induced ionization effects. The effects of scaling on the radiation hardness are yet to be seen; the progression of this technology depends on its scaling potential. Regardless, the performance of the ReRAM technology in the space environment will be largely determined by the SEE susceptibility of the peripheral control circuits. The lack of charge pump circuits serves to reduce power and minimize size, while also enhancing the device's radiation tolerance to TID and destructive SEE.

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REFERENCE

1. ITRS, "International Technology Roadmap for Semiconductors," 2001 and 2011 Editions: http://www.itrs.net/Links/2001ITRS/FEP.pdf, http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ERD.pdf
2. M. J. Marinella, S. M. Dalton, P. R. Mickel, P. E. Dodd, M. R. Shaneyfelt, E. Bielejec, G. Vizkelethy, and P. G. Kotula, "Initial assessment of the effects of radiation on the electrical characteristics of TaOx memristive memories," IEEE Trans. Nucl. Sci., vol. 59, pp. 2987 – 2994, Dec. 2012..
3. H. J. Barnaby, S. Malley, M. Land, S. Charnicki, A. Kathuria, B. Wilkens, E. DeIonno, and W. Tong, "Impact of alpha particles on the electrical characteristics of TiO2 memristors," IEEE Trans. Nucl. Sci., vol. 58, pp. 2838–2844, Dec. 2011..
4. J. S. Bi, Z. S. Han, E. X. Zhang, M. W. McCurdy, R. A. Reed, R. D. Schrimpf, D. M. Fleetwood, M. L. Alles, R. A. Weller, D. Linten, M. Jurczak, and A. Fantini, "The Impact of X-Ray and Proton Irradiation on HfO2/Hf-Based Bipolar Resistive Memories," IEEE Trans. Nucl. Sci., vol. 60, pp. 4540 – 4546, Dec. 2013.G. Chaumont, "Dose rate effect on bipolar transistors," presented at the JEDEC meeting, Tempe, AZ, Feb 15th 2011.
5. S. Gerardin, M. Bagatin, A. Paccagnella, K. Grürmann, F. Gliem, T. R. Oldham, F. Irom, and D. N. Nguyen, "Radiation effects in Flash memories," IEEE Trans. Nucl. Sci., vol. 60, pp. 1953 – 1969, Jun. 2013..
6. T.R. Oldham, S. Mohammed, P. Kuhn, E. Prinz, H. Kim and K.A. LaBel, "Effects of heavy ion exposure on nanocrystal nonvolatile memory," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2366-2372, Dec. 2005.
7. T. R. Oldham, M.R. Friendlich, A. B. Sanders, C. M. Seidleck, H. S. Kim, M. D. Berg, and K. A. LaBel, "TID and SEE response of advanced Samsung and Micron 4G NAND flash memories for the NASA MMS mission," IEEE Radiation Effects Data Workshop Record, pp. 114-122, Jul. 2009.
8. http://www.semicon.panasonic.co.jp/en/products/microcomputers/mn101l
9. R. Ladbury, "Statistical properties of SEE rate calculations in the limits of large and small event counts," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2113 – 2119, Dec. 2007.

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