Radiation Hardness Study on SiC Power MOSFETs

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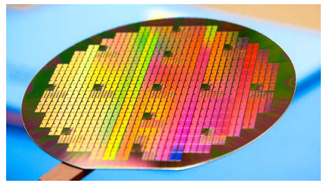
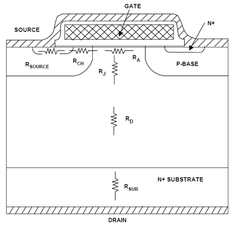
Introduction

As an emerging technology, silicon carbide (SiC) power MOSFETs are showing great potential for higher temperature/power rating, higher efficiency, and reduction in size and weight, which makes this technology ideal for high temperature, harsh environment applications such as downhole, medical, avionic, or even space applications. Radiation tolerance therefore becomes a critical aspect of the device performance in such environments.
In this work, we explored radiation hardness of SiC devices to total ionizing dose (TID), neutron-induced single-event burnout (SEB), and heavy-ion induced single-event effects (SEE).

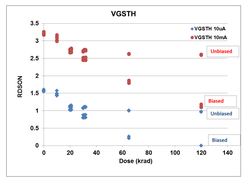


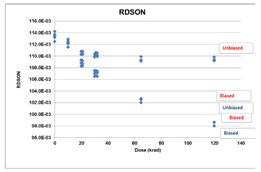


Previous Work

Total Ionizing Dose (TID):

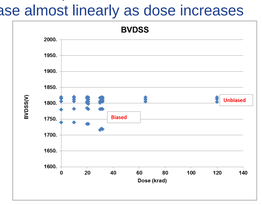
200 keV X-ray source was used to irradiate GE SiC MOSFETs under different bias conditions up to 120 krad (Si). The results indicate that compared with silicon, SiC is very tolerant to TID. This finding is in good agreement with previous reports on other SiC commercial off-the shelf (COTS) parts [1]

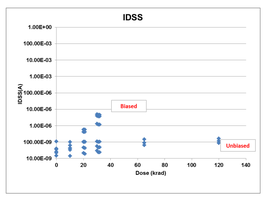




- ❖ Threshold voltage (Vth) decreases as dose increases. The recovery is very slow
- ❖ For unbiased samples, Vth shift seems to saturate @-0.5V after 65 krad(Si)
- ❖ For biased samples, Vth shift seems to decrease almost linearly as dose increases

- ❖ On-state resistance (Rdson) as dose increases, basically showing the same trend as threshold voltage

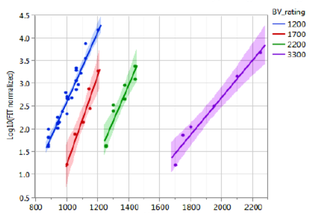




- ❖ Breakdown voltage (BVDSS) and drain leakage current (IDSS) are almost unchanged for unbiased samples
- ❖ Some degradation is observed on samples under bias, but is relatively small

Neutron Induced SEE:

Terrestrial Cosmic Radiation (TCR) induced single-event failures were also studied. These findings were reported briefly in an earlier publication [2]. SiC MOSFETs with different blocking voltage ratings were subjected to neutron irradiation to simulate accelerated TCR conditions. The results indicate that the failures in time (FIT) rate varies with different voltage ratings, and a different derating factor needs to be applied. Importantly, no gate degradation was observed



Comparison of Terrestrial Cosmic Radiation induced failure rates for 1.2kV, 1.7kV, 2.2kV and 3.3kV rated SiC MOSFETs. All results normalized to total MOSFET active area of Aact =7.2cm^2. The results were taken at room temperature and at sea level

Heavy-Ion Single-Event Effects (SEE)

Heavy-ion single-event effects are studied on GE SiC power devices in this part. Previous studies on COTS SiC devices demonstrated that parts started showing single-event degradation at very low drain-source voltage (Vds) bias conditions [3-4].

Ion	Split	JFET width	Rated Voltage	Min V_{DS} Latent Gate Damage*	Min V_{DS} Latent only*, PIGS > 1 mA	Onset V_{DS}: I_D, I_G Degradation $I_G = I_D$	$I_D > I_G$	Min V_{DS} Sudden SEE
1110 MeV Ag	1.2kV Production		1200	50 < V_{DS} < 75		200 ≤ V_{DS} < 225	350 < V_{DS} < 400	500 < SEB ≤ 600

*PIGS: Post-irradiation gate stress; I_G: gate current; I_D: drain current.

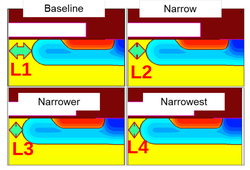
Design splits:

Based on the baseline test results, in this work we have implemented several design changes to improve the single event radiation performance.

1) Wafer splits (Epi and Gate Oxide thickness)

Split #	Splits
SS	Standard (Std) Epi + Std Gate Oxide
	Std Epi + Std Gate Oxide
DS	Dual Epi + Std Gate Ox
	Dual Epi + Std Gate Ox
ST	Std Epi + Thicker Gate Oxide
	Std Epi + Thicker Gate Oxide
DT	Dual Epi + Thicker Gate Oxide
	Dual Epi + Thicker Gate Oxide

2) JFET width splits



Sentaurus TCAD* simulation

- 2.5D (cylindrical geometry)
- Iso-thermal model

TCAD Transient simulation

Simulation Results:

Max electric field vs. time during SEE simulation of Single epi vs. Dual Epi

Max electric field vs. time during SEE simulation of different JFET width split

- ❖ **Dual epi can improve the rad hard performance, but only at higher drain bias >2000 V**
- ❖ **Transient electric field reduces as JFET width decreases, which could improve the latent gate damage**

*TCAD: Technology computer-aided design

Single-Event Radiation Test Results and Discussion

Part Preparation
- Open can package with MOSFET exposed .
- 1-mil parylene-C deposited to prevent arcing.
- Typical sample size of each part type: ~20 pieces

Power MOSFET Single-Event Effect Testing
Test conditions:
–Gate-source voltage (VGS) held at 0 V (off-state);
–Drain-source voltage (VDS) incremented before each run;
–Post-irradiation gate stress (PIGS) test performed and breakdown voltage (BVDSS) measured after each run.
–Gate bias during gate stress (PIGS) test on thicker gate split is scaled such that the field across the gate oxide is the same as for thinner split
Failure criteria:
–Maximum bias yielding no degradation: no change in PIGS or BVDSS pre- vs. post-irradiation;
–Onset bias for current degradation: lowest bias yielding measurable change in gate (I_G) or drain (I_D) current during run;
–Threshold bias for sudden SEE: catastrophic failure (ΔI_D> 20 mA and BVDSS< 1 V (shorted), or ΔI_G> 1 mA) immediately upon beam exposure.

Summary of Power MOSFET SEE Test Result

Ion	Split	JFET width	Min V_{DS} Latent Gate Damage*	Min V_{DS} Latent only*, PIGS > 1 mA	Onset V_{DS}: I_D, I_G Degradation $I_G = I_D$	$I_D > I_G$	Min V_{DS} Sudden SEE
1110 MeV Ag	1.2kV Production		50 < V_{DS} < 75		200 ≤ V_{DS} < 225	350 < V_{DS} < 400	500 < SEB ≤ 600
	SS	L1	50 ≤ V_{DS} < 75	< 200?	350 < V_{DS} ≤ 450	450 ≤ V_{DS} < 500	1000 < SEE < 1100
		L2	125** < V_{DS} ≤ 150	150 < V_{DS} ≤ 175	n/a	450 < V_{DS} < 500	1000 < SEE < 1100
		L3	125 < V_{DS} ≤ 150	200 < V_{DS} ≤ 400	n/a	400 < V_{DS} < 450	1200 < SEE (very close)
		L4	150 < V_{DS} < 175		n/a	400 < V_{DS} < 450	
	DT	L1	75 < V_{DS} ≤ 100		300 < V_{DS} ≤ 350	400 < V_{DS} < 450	1000 < SEE < 1100
		L2					
		L3	125 < V_{DS} ≤ 150	125 < V_{DS} ≤ 150	n/a	400 < V_{DS} < 450	1000 < SEE < 1100
		L4					
	ST	L1			300*** < V_{DS} ≤ 350		1100*** < SEE ~1200?
		L2	100 < V_{DS} ≤ 125	100 < V_{DS} ≤ 125	n/a	400 < V_{DS} < 450	1100*** < SEE < 1200
		L3	125 < V_{DS} ≤ 150	125 < V_{DS} ≤ 150	n/a	400 < V_{DS} < 450	1000 < SEE < 1100
		L4					
	DS	L1	75 < V_{DS} ≤ 100	100 < V_{DS} ≤ 125	300 < V_{DS} ≤ 350	400 < VDS ≤ 450	1000 < SEE ≤ 1100
		L2					
		L3	125 < V_{DS} ≤ 150	200 < V_{DS} ≤ 225	n/a	400 < V_{DS} < 450	1000 < SEE ≤ 1200
		L4	150 < V_{DS} ≤ 175	250 < V_{DS} ≤ 275			

* After fluence = 5.E+05 cm-2

Results and Discussion

1) The onset Vds for sudden SEE is significantly improved by 2X, from 500~600V (previous result on the production 1.2kV MOSFETs) to 1000~1200V. This is largely due to the improved epi design. The results indicate that the Vds for sudden SEE roughly scales linearly with Epi thickness (or breakdown voltage rating)
2) A latent gate damage is observed at lower Vds, ranging from 125V to 300V. The gate strength is weakened during the irradiation and an increase in gate leakage is observed during the gate stress test afterwards. This is slightly improved compared to the previous result on the 1.2kV production MOSFETs. If the gate is swept to the equivalent oxide field, the thick oxide split does NOT show any improvement in gate latent damage, indicating the latent gate damage could be governed by the gate oxide field.
3) Different JFET widths show an impact on all the gate-related failures. It better protected the gate from the latent damage as well as damage during the beam run. Simulation indicates this is most likely due to reduction of the field across the gate during irradiation.
4) The degradation of Id (Id>Ig) before sudden catastrophic failure is also observed at low Vds (400~500V) during irradiation. Note the onset Vds on the production 1.2kV is at about 350~400V. Although the thicker epi is able to improve the Vds for sudden catastrophic SEE, the onset of the minimum Vds does not seem to improve as much as expected, which indicates that this could be material limited.
5) The extra Epi does not seem to have any significant impact on the radiation hardness. This is because our design targets a higher drain bias; however, most of the radiation-induced failure happened at <1000V regime where this epi has minimal impact according to the simulation.

Acknowledgement

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References

[1] A. Akturk et al. “Radiation Effects in Commercial 1200 V 24 A Silicon Carbide Power MOSFETs”, IEEE Trans. Nucl. Sci. Vol. 59, No. 6, (2012)
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[4] S. A. Ikpe, et al., "Long-term reliability of a hard-switched boost power processing unit utilizing SiC power MOSFETs," in 2016 IEEE International Reliability Physics Symposium (IRPS), 2016, pp. ES-1-1-ES-1-8.

imagination at work

To be presented by Xingguang Zhu at the International Conference on Silicon Carbide and Related Materials (ICSCRM 2017), Washington, DC, September 17-22, 2017.