Journal of Astronomical Telescopes, Instruments, and Systems

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Kazuhiro Sakai, Joseph S. Adams, Simon R. Bandler, Douglas A. Bennett, Kent D. Irwin, John A. B. Mates, "Development of space-flight compatible room-temperature electronics for the Lynx x-ray microcalorimeter," *J. Astron. Telesc. Instrum. Syst.* **5**(2), 021013 (2019), doi: 10.1117/1.JATIS.5.2.021013.

Development of space-flight compatible room-temperature electronics for the Lynx x-ray microcalorimeter

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Abstract. We are studying the development of space-flight compatible room-temperature electronics for the Lynx x-ray microcalorimeter (LXM) of the Lynx mission. The baseline readout technique for the LXM is microwave SQUID multiplexing. The key modules at room temperature are the RF electronics module and the digital electronics and event processor (DEEP). The RF module functions as frequency converters and mainly consists of local oscillators and I/Q mixers. The DEEP performs demultiplexing and event processing, and mainly consists of field-programmable gate arrays, ADCs, and DACs. We designed the RF electronics and DEEP to be flight ready, and estimated the power, size, and mass of those modules. There are two boxes each for the RF electronics and DEEP for segmentation, and the sizes of the boxes are 13 in. × 13 in. × 9 in. for the RF electronics and 15.5 in. × 11.5 in. × 9.5 in. for the DEEP. The estimated masses are 25.1 kg/box for the RF electronics box and 24.1 kg/box for the DEEP box. The maximum operating power for the RF electronics is 141 W or 70.5 W/box, and for the DEEP box is 615 W or 308 W/box. The overall power for those modules is 756 W. We describe the detail of the designs as well as the approaches to the estimation of resources, sizes, masses, and powers. [DOI: 10.1117/1.JATIS.5.2.021013]

Keywords: microcalorimeter; microwave SQUID multiplexing; readout electronics.

Paper 18100SS received Nov. 1, 2018; accepted for publication Apr. 1, 2019; published online Apr. 26, 2019.

1 Introduction

The Lynx mission concept is one of four flagship missions being studied for consideration in the 2020 Astrophysics Decadal Survey.[1] It has three science pillars: it aims to unveil the otherwise "invisible" Universe with the power of unique state-of-the-art instruments that will enable us to observe the earliest black holes directly, reveal galaxy formation drivers, and understand the high-energy processes of stellar evolution.

The Lynx x-ray microcalorimeter[2] (LXM), one of three instruments the spacecraft carries, is an imaging spectrometer, which will provide 3-eV spectral energy resolution over the 0.2 to 7 keV energy band for $5' \times 5'$ field of view (FOV) with $1''$ pixels. This will match the angular resolution of the x-ray optics in Lynx, which will be $<1''$ maintained out to $10'$ off-axis with an effective area greater than 2 m^2 at 1 keV improving x-ray sensitivity by 100-fold from the Chandra x-ray Observatory.

The baseline readout technique for the LXM is microwave SQUID multiplexing.[3–5] In microwave SQUID multiplexing, hundreds of sensor signals are fed into RF-SQUIDs that are inductively coupled to superconducting microwave resonators spread over a frequency range of several gigahertz and are read out using a single pair of coaxial cables. This technique is the essential readout scheme for the LXM detector with more than 7000 sensors. Figure 1 shows the simplified system block diagram for the LXM from the readout perspective.[2] The detector is at the 50 mK stage along with the SQUID multiplexers, while cryogenic 4 to 8 GHz high-electron-mobility transistors (HEMT) at the 4.5 K stage are used to amplify the signals from the multiplexers. At room temperature, there are boxes with RF electronics inside that receive the amplified signal and perform a frequency conversion from a microwave frequency to an intermediate frequency. The downconverted signal is digitized and processed in the DEEP boxes. The DEEP also generates a frequency comb that is upconverted in the RF electronics and fed into the SQUID multiplexer. Finally, the DEEP is also responsible for generating bias voltages/currents and flux-ramp signals[4] for the TES arrays, SQUID multiplexers, and HEMTs, and these are fed into the cryostat through a junction box attached outside the cryostat. The RF electronics and DEEP are controlled by the Main ELectronics (MEL), which also control the cryocooler electronics and ADR controller.

In this study, we present a design for the RF electronics and DEEP that meets the notional requirements of each subsystem using technology that should be available in the near future. These designs are based on several currently available state-of-the-art readout systems developed for ground applications. We then derive an initial estimate of the power, size, and mass of the electronics based on the design. It should be noted that strict requirements for Lynx do not exist at this point in time; thus, the requirements we use are merely estimates. Also, several requirements that would exist for a mature

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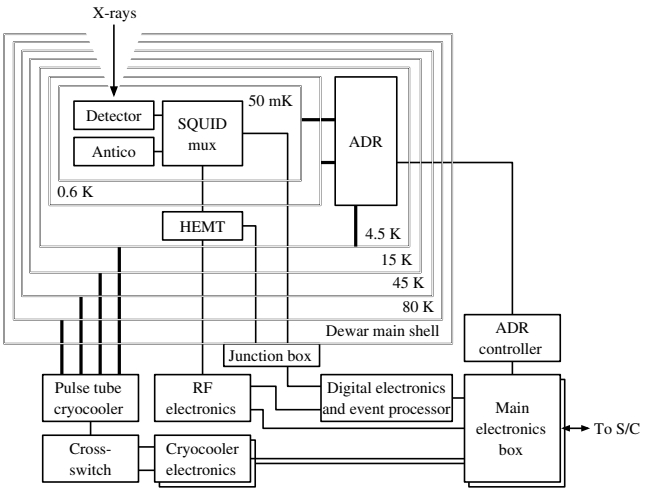

Fig. 1 Simplified system block diagram for the LXM subsystem.[2] The overlaid boxes represent the redundancy in the system but specifically the number of boxes for the subsystem.

system, such as thermal loading and radiation hardness, are not addressed in this study. We hope to address them in future work.

2 Microwave SQUID Multiplexing Readout System Overview

The LXM detector consists of the main array and two subarrays[2] (Fig. 2). The main array covers a $5' \times 5'$ FOV with $1''$ pixels, and it will provide 3-eV energy resolution over the 0.2 to 7 keV energy band. At the center of this $5'$ FOV main array, there is an enhanced main array that covers a $1' \times 1'$ FOV with $0.5''$ pixels, which will provide 1.5 eV energy resolution over the same energy band. The ultra-high-resolution array that provides 0.3 to 0.4 eV energy resolution from 0.2 to 0.75 keV will be placed beside the main array and cover a $1' \times 1'$ FOV with $1''$ pixels. The pixels for the main array and enhanced main array are thermally multiplexed using a 5×5 hydra[6,7] technique to reduce the number of sensors.

Based on the resonator frequency spacing in the SQUID multiplexer, the required number of HEMTs is defined for each array.[2,8] Table 1 shows the number of sensors for each type of array along with the resonator width and spacing, as well as the number of HEMTs for each array, which is approximately given by the number of sensors times the resonator spacing divided by the HEMT bandwidth. Assuming the use of 4-GHz bandwidth HEMTs, the required number of HEMTs are 10, 6, and 6 for the main, enhanced main, and ultra-high-resolution arrays, respectively. Although the total number of HEMTs is 22, these will not be used simultaneously. The two observation modes[2] of LXM limit the simultaneous use of HEMTs to 16 at maximum, which is either for the main array plus the enhanced main array or the ultra-high-resolution array.

Table 1 The summary of three TES arrays and the required number of HEMTs.

	Main array	Enhanced main array	Ultra-hi-res array
Number of sensors	3456	576	3600
Number of pixels	86,400	12,800	3600
Hydra	5×5	5×5	—
Sampling frequency (flux-ramp frequency)	500 kHz	2 MHz	300 kHz
Resonator width	2 MHz	8 MHz	1.2 MHz
Resonator spacing	10 MHz	40 MHz	6 MHz
Number of HEMTs	10	6	6

Current ground applications/prototypes are utilizing high-speed, high-resolution ADCs and DACs with bandwidths of ~1 GHz. Thus, we divide each four GHz HEMT into four sub-bands to match the bandwidth of the ADCs and DACs. Figure 3 shows the simplified system schematic of the microwave SQUID multiplexing readout system in this design. The box labeled "Cryostat" in the left side of the schematic is showing the microwave SQUID multiplexer and the cryogenic HEMT amplifier. A more detailed description of the cryogenic setup and the microwave SQUID multiplexer are discussed elsewhere.[9]

The box labeled "1 GHz RF block" in the RF electronics box in Fig. 3 represents the 1-GHz bandwidth RF block. For the 4-GHz bandwidth HEMT, there will be four 1-GHz RF blocks, but the schematic is only showing one block for simplicity. The 1-GHz RF block consists of two I/Q mixers (I/Q modulator and demodulator), a local oscillator (LO), and a splitter. This block performs frequency conversion from the intermediate frequency to a microwave frequency and vice versa. The I/Q modulator takes a frequency comb spread over ± 500 MHz

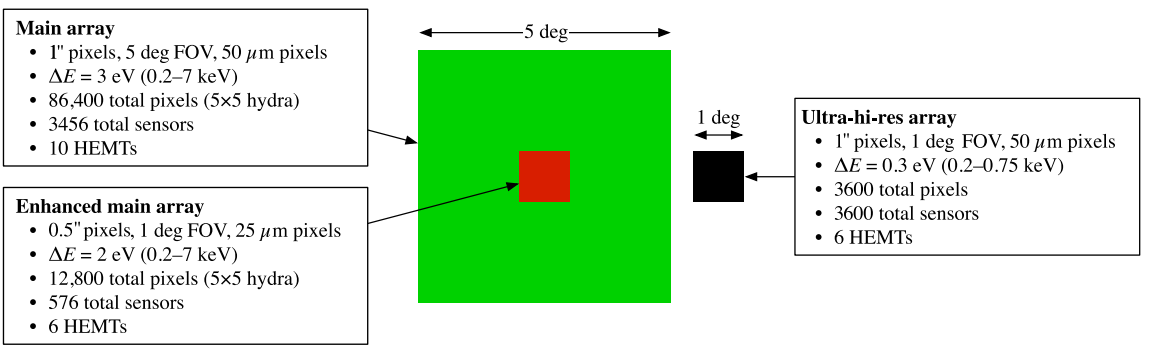

Fig. 2 The baseline focal plane layout of the LXM.[2] It consists of the main array (green), the enhanced main array (red), and the ultra-high-resolution array (black).

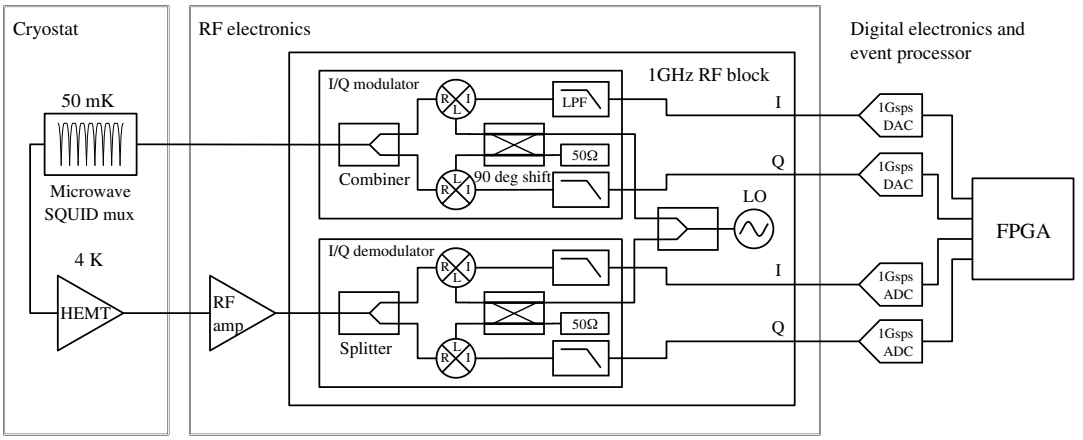

Fig. 3 Simplified system schematic of the microwave SQUID multiplexing readout system. The schematic is only showing one 1-GHz RF block out of four per HEMT for simplicity.

range for in-phase and quadrature signals generated in DEEP, and upconverts it within the range of 4 to 8 GHz. The upconverted 1-GHz bandwidth frequency comb is mixed with three other 1-GHz bandwidth frequency combs and fed into the SQUID multiplexer in the cryostat. The flux-ramp modulated output signal from the SQUID multiplexer is first amplified by the cryogenic 4 to 8 GHz bandwidth HEMT amplifier and pulled out to the outside cryostat. A room-temperature RF amplifier is used to boost the signal further, and the signal is divided into four 1 GHz sub-bands using splitters and fed into the I/Q demodulators. Band-pass filters may be required between the splitter and I/Q demodulator. The I/Q demodulator downconverts the input signal and generates $\pm$500-MHz baseband in-phase and quadrature signals.

The box labeled "digital electronics and event processor" in the figure is showing digital electronics to read out 1-GHz bandwidth signal in the DEEP. There are two 1-Gsps DACs and two 1-Gsps ADCs for in-phase and quadrature signals, and they are connected to a field-programmable gate array (FPGA). The FPGA is responsible for (A) generating a frequency comb to feed into the SQUID multiplexer, (B) demultiplexing the sensor signals, and (C) performing optimal filtering for triggered x-ray pulses. Although it is not shown in the figure, the DEEP is also responsible for generating bias voltages and flux-ramp signals for the TES arrays and SQUID multiplexers.

Note that the 1-GHz RF block is a notional partition used to make the various estimations in the following sections easy, and thus it does not necessarily reflect an actual hardware design. In other words, if 2-Gsps ADCs/DACs are used in the actual design, it is reasonable to expand the RF block bandwidth to 2 GHz.

3 RF Electronics

As described in the previous section, the RF electronics box consists of RF amplifiers and 1-GHz RF blocks. In the current baseline design, there will be two RF electronics boxes for segmentation, and each box will interface to half the total number of HEMTs, that is $5 + 3 + 3$ HEMTs per box for the main, enhanced main, and ultra-high-resolution arrays. Therefore, for each RF electronics box, there are 11 of RF amplifiers and 44 of 1-GHz RF blocks.

For RF electronics, there is no flight qualified commercial-off-the-shelf components available, so we may have to build the module using radiation-hardened parts from scratch, or to space-qualify commercially available nonspace-grade components at NASA. Designing and building one from scratch is beyond the scope of this study, as the main goal of this work is to estimate the power, size, and mass of the system. Therefore, we will assume the use of commercial components, and we will utilize their specifications for the estimate.

Table 2 shows a summary of the assumed commercial components and the required numbers for those components. The I/Q modulator and demodulator, AM4080A and AD4080B, have the baseband frequency bandwidth of 300 MHz as default and this must be customized to expand the bandwidth to 500 MHz.

For these components, we estimated the power and mass in Table 3. For the calculation of power, we used the maximum

Table 2 The summary of RF components and the required numbers.

	Manufacture	Part number	Qty per HEMT	Qty per box	Total qty
RF amplifier	Mini-circuits	ZX60-83LN+	1	11	22
Splitter/combiner (four-way)	Pasternack	PE2031	2	22	44
LO	Polyphase microwave	Phase-locked oscillator module	1	11	22
I/Q modulator	Polyphase microwave	AM4080A	4	44	88
I/Q demodulator	Polyphase microwave	AD4080B	4	44	88

Table 3 The power and mass estimates for the RF components.

	Max operating qty	Unit power (W)	Max operating power (W)	Total qty	Unit mass (kg)	Total mass (kg)
RF amplifier	16	0.30	4.8	22	0.025	0.6
Splitter/combiner (four-way)	32	0.00	0.0	44	0.243	10.7
LO	16	0.75	12.0	22	0.111	2.4
I/Q modulator	64	0.75	48.0	88	0.152	13.4
I/Q demodulator	64	0.75	48.0	88	0.152	13.4
Power card (80% efficiency)	2	—	28.2	2	0.9	1.8
Housing	—	—	—	2	4.0	8.0
Total			141.0			50.2
Total per box (two boxes)			70.5			25.1

operating quantity, which was calculated from the maximum HEMTs simultaneously used (16 HEMTs), instead of the total quantity. The power shown for the power card is a power loss assuming 80% efficiency. The total power for the RF electronics is 141 W or 70.5 W per box. We estimated the size of the RF electronics box as 13 in. × 13 in. × 9 in., and for this size, the estimated mass for the housing is 4 kg. For the mass calculation, we multiplied the unit mass with the total number and added the housing mass of 4 kg. The total mass for the RF electronics is 50.2 kg or 25.1 kg per box.

4 Digital Electronics and Event Processor

As described in Sec. 2, the DEEP box mainly consists of FPGAs, ADCs, and DACs for reading out the SQUID multiplexer. It also includes bias and flux-ramp signal generators for the TES arrays and SQUID multiplexers. There will be two identical DEEP boxes for segmentation, as is the case for the RF electronics.

4.1 *ADC and DAC*

The effective number of bits (ENOB) of ADC and DAC needs to be well considered so as not to be the dominant noise source. The conservative requirement to the ENOB comes from the quantization noise as well as the clipping noise, which is an additional noise term due to the clipping when the amplitude of superimposed tones exceeds the maximum range of the ADC and DAC. The SNR is given as[10]

$$\mathrm{SNR} = 6.02b - 10\log_{10}(N) - 20\log_{10}(\mu) + 10\log_{10}\left(\frac{f_s}{2\times \mathrm{BW}}\right) + 7.78\ \mathrm{dB},$$

where b is the ENOB, N is the number of multiplexed signals, f_s is the ADC and DAC sampling frequency, BW is equivalent to the flux-ramp frequency, $\mu = A_{\mathrm{clip}}/\sigma$, where $\pm A_{\mathrm{clip}}$ is the full range of ADC in volts, and σ is the standard deviation of each tone. For the Lynx arrays, $N \times \mathrm{BW}$ is kept the same, and thus the SNR will be the same for a given ENOB for all arrays. For a given number of bits, there is an optimal μ and for $b = 10$ $\mu = 4.5$ and $b = 11$ and $\mu = 5.0$, and we used these values to calculate the SNR for 10- and 11-bit cases. For 10-bit ENOB, the SNR is 65 dB, and for 11-bit ENOB, the SNR is 70 dB. The typical SNR of the HEMT with 3 K noise temperature is 70 dB, so the requirement to ENOB for Lynx is set to 11 bits.

In this study, we do not specify any particular ADC because there is no such a commercially available space-grade ADC that satisfies the ENOB requirement at this time. There are some nonspace grade ADCs with the ENOB of 11 bits or higher, such as Texas Instruments ADS54J40, which is a dual-channel 14-bit 1 Gsps ADC with 1.35 W/channel power dissipation. For this study, we only assume the number of bits and power for ADC as 14 bits and 1 W at 1 Gsps. For the DAC, Texas Instruments DAC5670-SP is available, which is a dual-channel 14-bit 2.4 Gsps (or 1.2 Gsps per channel) space-grade DAC. The power dissipation for this DAC is 2 W or 1 W/Channel at 1 Gsps.

4.2 *FPGA Design*

Although the 1-GHz RF block is the common design for three TES arrays, the FPGA firmware design of DEEP needs to be tailored for each TES array since the number of multiplexed channels per HEMT is different. The main design of the firmware is the same as in Ref. 11 with a few exceptions. In this design, we use a polyphase filter bank (PFB) channelizer[12] on both the tone generation and the channelization, and the FFT size of the PFB channelizer depends on the type of array. Table 4 shows the summary of three TES arrays along with the FFT size.

Figure 4 shows the FPGA firmware block diagram. The 500-MHz clocked part on the left is a parallel PFB coarse channelizer that takes a 1-Gsps I/Q data stream from the ADC and splits it into 128/32/256 channels. The other 500-MHz clocked part on the right is another parallel PFB channelizer that generates the frequency comb. The 250-MHz clocked center parts are four demodulators that perform the flux-ramp demodulation and one event processor that performs triggering and optimal filtering.

Table 4 The summary of three TES arrays and the required number of each component.

	Main array	Enhanced main array	Ultra-hi-res array
Number of sensors	3456	576	3600
Sampling frequency (flux-ramp frequency)	500 kHz	2 MHz	300 kHz
Resonator width	2 MHz	8 MHz	1.2 MHz
Resonator spacing	10 MHz	40 MHz	6 MHz
Number of resonators per 1-GHz RF block	100	25	166
FFT size per RF block	128	32	256

4.2.1 *Tone generation and channelization*

The channelizer consists of PFB blocks and FFT blocks. The PFB in this design is implemented as an eight-tap finite impulse response (FIR) filter. All blocks in the channelizer are driven with a 500-MHz clock, and two PFBs and two FFTs are in parallel to process the 1-GHz I/Q data streams. The FFT size is equal to the number of resonators (or sensor channels) per 1-GHz bandwidth rounded up to the next power of two: e.g., 128 for the main array, 32 for the enhanced main array, and 256 for the ultra-high-resolution array.

Since the resonator spacing and the FFT bin frequency width do not match, the PFB channelizer needs to handle an arbitrary frequency tone. Figure 5 shows the frequency response of the PFB. The solid line shows the single-bin frequency response, and dashed lines show the responses of neighboring bins. To prevent the signal leakage and the scalloping loss, the pass-band of this PFB is limited to the red-shaded range, which is $\pm 30\%$ of the FFT bin width from the bin center, and therefore, one PFB channelizer only covers 60% of 1-GHz bandwidth. There is an additional PFB channelizer to cover the rest of the bandwidth. For the tone generation, it is followed by a frequency shifter that shifts the signal frequency by the half of the FFT bin width, and the frequency-shifted signal is summed with the signal from the first PFB channelizer, as shown in the bottom half of Fig. 4. For the coarse channelization, the additional channelizer receives the I/Q signals that are frequency shifted by the same amount.

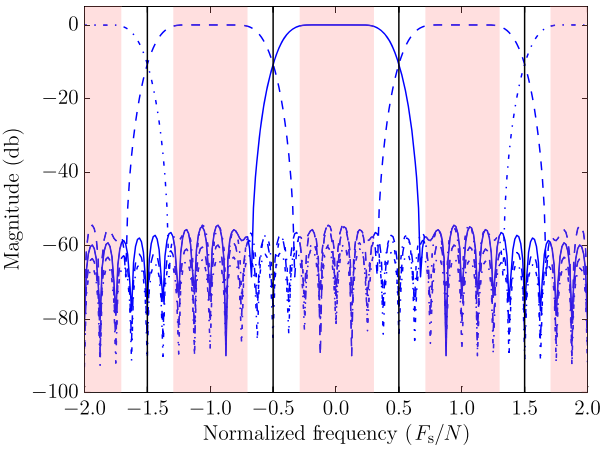

Fig. 5 The frequency response of the PFB. The solid line shows the single-bin frequency response and dashed lines show the frequency responses of neighboring bins (± 1 and ± 2 bins). The red-shaded regions are pass-bands, which is $\pm 30\%$ of the bin width from the bin center.

The signals from the two PFB channelizers are interleaved and serialized as a single $1/N_{\mathrm{FFT}}$ GHz signal stream for each channel, where N_{FFT} is the number of the FFT size, and given to a channel select, which is a multiplexer that the following demodulators can select a channel from. On the other side, another channel select receives signals from the demodulators and sends it to a deserializer. The deserializer parallelizes the incoming signals to the parallel FFTs.

4.2.2 *Microwave SQUID multiplexer demodulator*

The demodulators, which are shown at the center part in Fig. 4, are to demodulate the flux-ramp modulation. These are four identical blocks and run in parallel driven with a 250-MHz clock. One demodulator can process up to $N_{\mathrm{FFT}}/4$ channels, and it receives the channelized I/Q data streams from the PFB channelizer and extracts the sensor signal for each channel.

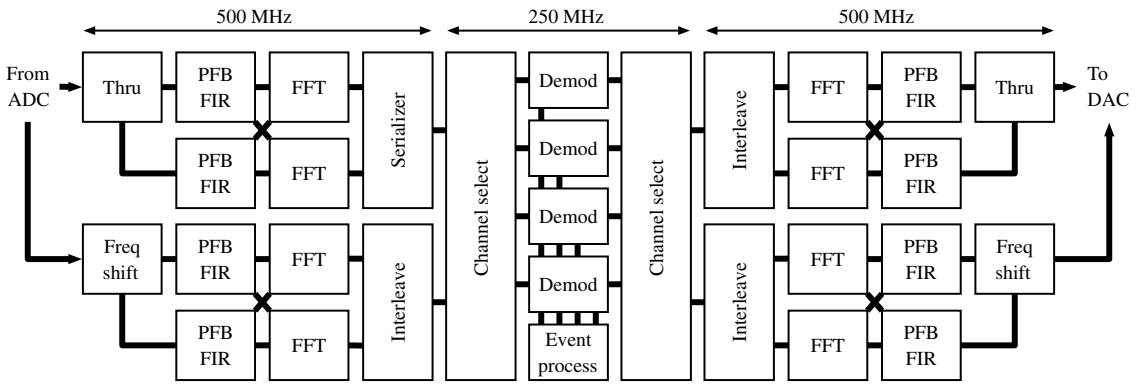

Fig. 4 The FPGA firmware block diagram. The 500-MHz clocked part on the left is a parallel coarse channelizer that takes 1-Gsps I/Q data stream from ADCs and splits into 32/128/256 channels. The other 500-MHz clocked part on the right is a parallel dechannelizer that generates the input frequency comb. The 250-MHz clocked center parts are four demodulators that perform the flux-ramp demodulation and one event processor that performs triggering and optimal filtering.

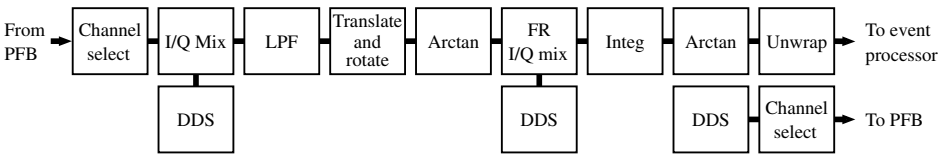

Fig. 6 The block diagram for the 250-MHz clocked flux-ramp demodulator.

Figure 6 shows the block diagram of the demodulator. The demodulated sensor signals are fed into the event processor, which is described later.

Following the diagram in Fig. 6, the signal from the coarse channelization comes from the left into the channel select. Since this signal is in an intermediate frequency, it needs to be mixed down to zero intermediate frequency at the first I/Q mixer stage in the demodulator for fine-tuning. The LO for the mixer is implemented using a direct digital synthesizer (DDS). There are two independent DDSs (one for I and one for Q) to allow to compensate for phase deviations from the ideal 90-deg phase difference for I and Q of the analog demodulators in the RF electronics.

In addition to the DDSs used for the LO, there are two additional DDSs that generate the same frequency I/Q tones as for the I/Q mixer. Those tones are passed to the PFB channelizer for the tone generation via the channel selector. The channelizer DDSs are also independent synthesizers to allow for phase adjustment to compensate for phase deviations of the I/Q modulators in the RF electronics.

The fine-tuned I/Q baseband signals are then low-pass filtered using a 16-tap FIR filter to reject spurious tones outside the bandwidth of the resonator. At this point, the baseline signals draw an arc in the I/Q complex plane, and the angle of the arc represents the sensor signal with the flux-ramp modulation.[11] We use a coordinate rotation digital computer[13] (CORDIC) block to calculate the arc angle, but the arc needs to be first centered at the origin and rotated to the positive x-axis. The arc center is fit in advance and subtracted to translate the arc to the origin. Another CORDIC is then used to rotate the arc, and the angle is calculated using the CORDIC taking the arctangent of the I/Q signals.

Finally, the demodulation of flux-ramp modulation is performed. This process involves another I/Q mixing with sinusoids generated by a DDS, masking a transient caused by the flux-ramp reset, integrating the mixed signals over the integer number of mixing frequency periods, and calculating the angle of the I/Q signals after the integration taking the arctangent using a CORDIC.[11] At this point, the data rate is reduced to the flux-ramp frequency per each channel. One final step in the demodulation stage is phase unwrapping to linearize the periodical phase signal from the last CORDIC.

4.2.3 *Event processing*

The event processor, which is shown at the bottom center in Fig. 4, captures demodulated sensor signals from four demodulators and extracts the incident x-ray photon energy. It is also driven with the 250-MHz clock. Figure 7 shows the block diagram of the event processor.

The event processor triggers on x-ray pulses and extracts the pulse records from the stream of the sensor signal. The trigger block consists of a derivative, which calculates the difference from the previous data point for each channel, and an edge trigger, which triggers when the incoming signal crosses the given threshold in the given direction (up or down). With the combination of these two, this block behaves as a simple slope trigger for the incoming signal from the demodulator. For the triggered signal, the rise-time of the pulse is measured and used to differentiate the 5×5 hydra pixel for the main array and the enhanced main array. Furthermore, the pixel differentiated signal is decimated by a factor of 4 using a cascaded integrator-comb filter.[14] The pixel differentiation and the decimation are not performed for the ultra-high-resolution array. The signal is then supplied into a pretrigger delay, which is a circular buffer implemented using a block RAM, and the stored signal is taken out from the other side after a certain amount of delay.

The optimal filtering block performs optimal filtering and event grading. We are assuming Suzaku and Hitomi-style grading.[15,16] There are three event grades, high resolution (HR), medium resolution (MR), and low resolution (LR), based on two-time differences: Δt_{p}, which is the time between the previous trigger and the current trigger, and Δt_{n}, which is the time between the current trigger and the next trigger. For each Δt_{p} and Δt_{n}, two thresholds are given, and if an event occurs with both Δt_{p} and Δt_{n} exceeding the strict thresholds, the event is graded as HR. If both Δt_{p} and Δt_{n} are less than the relaxed thresholds, the event is graded as LR. All other events are graded as MR. For HR and MR events, optimal filtering is performed. For LR events, optimal filtering is not performed, but the signal is integrated for a certain number of data points after the offset of the signal is subtracted. These calculations are speculatively executed in parallel, and at the same time the event is graded based upon Δt_{p} and Δt_{n}. Once the event is graded, the corresponding result is selected, and other two

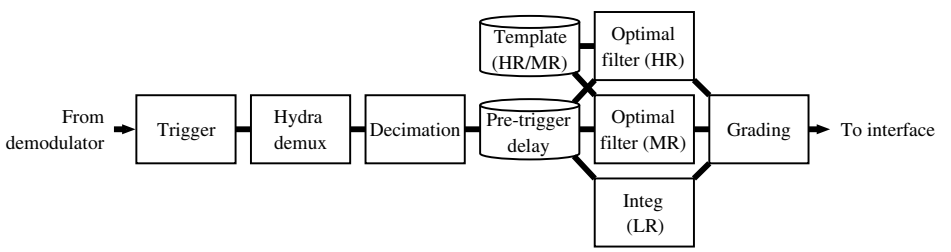

Fig. 7 The block diagram for the 250-MHz clocked event processor. The pixel differentiation (hydra demux) and the decimation are only for the main array and the enhanced main array.

results are discarded. Moreover, because these calculations are continuously executed without a dead time for the incoming x-ray pulse events, the upper limit on count rate in the readout hardware will be equal to the theoretical limit, which is the inverse of the shortest LR record length.

Each HR and MR optimal filtering performs three optimal filtering at the same time, one with an event record delayed by one data point, one with an event record with no delay, and one with an event record advanced by one data point. These three values are later used to interpolate the maximum pulse height after fitted with a quadratic function. This interpolation is not assumed to be performed in the firmware for this study.

The templates for optimal filtering are stored in a block RAM to perform multiple filtering in parallel, and the maximum number of templates that can be stored in the block RAM is hence limited. For the 5×5 hydra arrays, 25 templates are assumed for each hydra pixel, and they are shared with all the TESs within the 1-GHz RF block. For the nonhydra array, one template per TES is assumed. For HR events, a full-length template is used, while a quarter-length template is used for MR events. The template length, or record length, for each array, is chosen so that the record length is longer than $10\tau_0$, where τ_0 is the TES pulse decay time constant. The record length for LR is 1/16 of the full length. Table 5 summarizes the sampling rate and record length for each TES array type.

Table 5 Sampling rate and record length for each array type.

	Main array	Enhanced main array	Ultra-hi-res array
TES τ_0	2.7 ms	0.67 ms	0.32 ms
Sampling rate	500 ksps	2 Msps	300 ksps
Rate after decimation	125 ksps	500 ksps	—
Record length			
HR	4096 pts/32.8 ms	4096 pts/8.2 ms	1024 pts/3.5 ms
MR	1024 pts/8.2 ms	1024 pts/2.0 ms	256 pts/0.8 ms
LR	256 pts/2.0 ms	256 pts/0.5 ms	64 pts/0.2 ms
Pretrigger length			
HR	255 pts/2.0 ms	255 pts/0.5 ms	63 pts/0.2 ms
MR	63 pts/0.5 ms	63 pts/0.1 ms	15 pts/50 μs
LR	31 pts/0.2 ms	31 pts/60 μs	7 pts/23 μs

Table 6 The summary of available resources for FPGA candidates.

	UltraScale+ MPSoC	UltraScale+ RFSoC	Virtex-5Q	Virtex-5QV
	Space grade	Commercial grade	Defense grade	Space grade
Part number	RT-ZU19EG	XCZU27DR	XQ5VSX240T	XQR5VFX130
LUTs	523k	425k	150k	82k
Flip-flops	1045k	851k	150k	82k
DSPs	1968	4272	1056	320
36k block RAM blocks	984	1,080	516	298
UltraRAM blocks	128	80	—	—
Processors	ARM v8 Cortex-A53 ARM v7 Cortex-R5 Mali-400 GPU Soft IP	ARM v8 Cortex-A53 ARM v7 Cortex-R5 Soft IP	Soft IP	Soft IP
Integrated RF-ADC/RF-DAC	—	Eight 12-bit 4 Gsps ADC Eight 14-bit 6.5 Gsps DAC	—	—

Table 7 Estimated resource usage per 1-GHz process block.

	Main array	Enhanced main array	Ultra-hi-res array
FFT size per process unit	128	32	256
Family		Virtex-5	
LUTs	57k	23k	101k
Flip-flops	63k	31k	109k
DSPs	223	211	223
36k block RAM blocks	131	115	195
Family		UltraScale+	
LUTs	66k	41k	97k
Flip-flops	91k	50k	140k
DSPs	223	211	223
36k block RAM blocks	136	109	183

4.3 *FPGA Resource Estimation*

For a high-performance signal processing and computation in space, the space-qualified Xilinx Virtex-5QV has been used with success in many projects since 2011. Although it will still be used in some of the near-term missions planned to launch around 2020, the resource availability of Virtex-5QV is quite limited if compared with the recent newer-generation resource-rich FPGAs. To replace Virtex-5QV for the next decade, Xilinx is now space qualifying the Zynq UltraScale+ MPSoC, and it is expected to be rolled out in 2019. For the Lynx mission, we are baselining using the space-qualified MPSoC, RT-ZU19EG, and in this section, we estimate the resource and power usage for the firmware described in the previous section. In addition to MPSoC, the estimation is performed for Xilinx UltraScale+ RFSoC and defense-grade Virtex-5Q for comparison. The RFSoC is an FPGA Xilinx recently released, and it has the same architecture as MPSoC but has some integrated high-speed ADCs and DACs. It is well suited to the microwave SQUID multiplexing readout, but it is not expected to be space-qualified. The defense-grade Virtex-5Q has a flight legacy at NASA, and it is a backup option to MPSoC. The space-grade

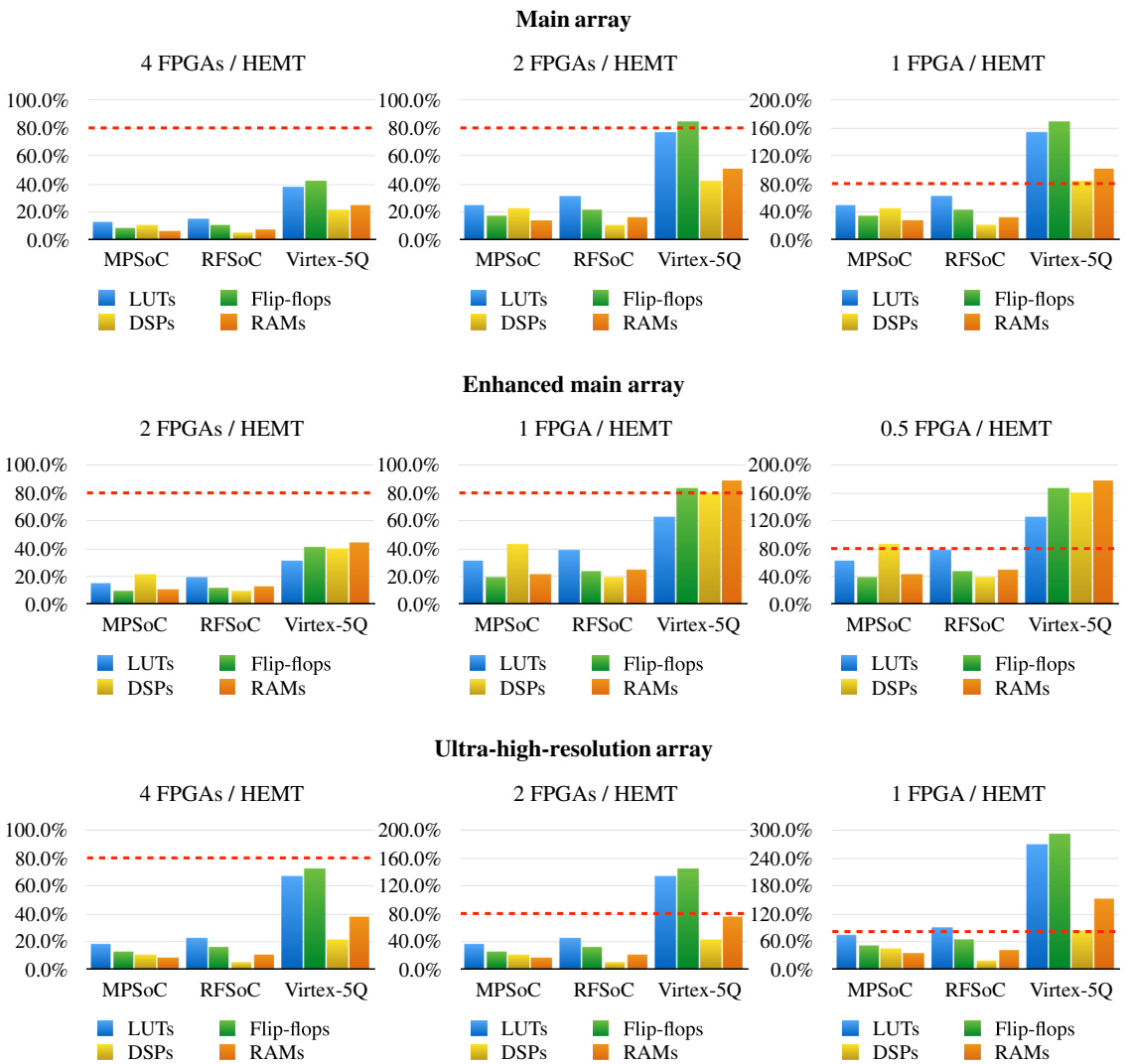

Fig. 8 The FPGA resource usages for the various number of FPGAs per HEMT. The dashed line in the plots shows the 80% threshold.

Virtex-5QV does not have enough resources, and it is excluded from the estimation. Table 6 summarizes the available resources for MPSoC, RFSoC, Virtex-5Q, and Virtex-5QV.

For a better resource estimation, we have developed most of the firmware and synthesized using Xilinx ISE and Vivado and checked the resource usage for a single 1-GHz RF block. Table 7 shows the estimated resource usage on look-up tables (LUT), flip-flops, digital signal processing (DSP) cores, and 36k-bit block RAM blocks for the Virtex-5 family and the UltraScale+ family. We used the Xilinx ISE Design Suite 14.6 for Virtex-5 and the Xilinx Vivado Design Suite 2016.4 for UltraScale+. Note that this is not a resource usage after the actual mapping on specific device resources, so the estimation is still approximate. Moreover, the I/O pin availability was intentionally left out in this study, as we have not chosen the specific ADCs and DACs at this stage.

The required number of FPGAs per HEMT was calculated based on the number of 1-GHz RF blocks that can be fitted into a single FPGA. Figure 8 shows the total resource usages on MPSoC, RFSoC, and Virtex-5Q for the various number of FPGAs per HEMT. During this study, one UltraRAM, which is only available in MPSoC and RFSoC, was treated as eight 36k-block RAM blocks. The top, middle, and bottom rows show the usages for the main array, enhanced main array, and ultra-high-resolution array, respectively. The dashed line in the plots shows the 80% threshold.

For the main array, if using MPSoC or RFSoC, a single FPGA is required per HEMT, alternatively, if using Virtex-5Q, four FPGAs are required per HEMT. Similarly, for the enhanced main array, the required number of FPGAs per HEMT is 1 for the MPSoC case, 0.5 for the RFSoC case, and 2 for the Virtex-5Q case. Finally, for the ultra-high-resolution array, it is on FPGA per HEMT for the MPSoC case, two for the RFSoC case, and four for the Virtex-5Q case.

Table 8 Estimated FPGA power for each type of array.

	Main array	Enhanced main array	Ultra-hi-res array
Number of HEMTs	10	6	6
	UltraScale+ MPSoC space grade (RT-ZU19EG)		
FPGAs per HEMT	1	1	1
Total FPGAs	10	6	6
FPGA unit power	16 W	12 W	20 W
Total FPGA power	160 W	72 W	120 W
	UltraScale+ RFSoC commercial grade (XCZU27DR)		
FPGAs per HEMT	1	0.5	2
Total FPGAs	10	3	12
FPGA unit power	16 W	21 W	11 W
Total FPGA power	160 W	63 W	132 W
	Virtex-5Q defense grade (XQ5VSX240T)		
FPGAs per HEMT	4	1	4
Total FPGAs	40	6	24
FPGA unit power	11 W	16 W	13 W
Total FPGA power	440 W	96 W	312 W

4.4 *Power and Mass Estimation*

Based on the estimated resource usage, we calculated the FPGA unit power using the Xilinx Power Estimator. The power estimation largely depends on the toggle-rate, which is signal transitions per clock cycle, but it is not easy to accurately estimate the rate. According to Xilinx, 12.5% is the default value, and most of the logic-intensive designs work at around this rate, while 20% can be used for the worst-case estimate.[17] For arithmetic-intensive designs, 50% represents the absolute worst case. For this study, we used 25% of toggle-rate for the 500-MHz clocked devices as they are more arithmetic-intensive modules, and 12.5% of toggle-rate for the 250-MHz clocked devices as they are a mix of logic and arithmetic operations. For the I/O interface to the external ADC and DAC, we assumed 500-MHz double data rate low voltage differential signaling for each 1 Gsps ADC and DAC with the bit widths of 14 bits.

Table 8 shows the estimated FPGA unit power for each type of array together with the required number of FPGAs and the total FPGA power. Note that the actual number of RFSoC FPGAs for the enhanced main array will be one greater than shown due to the need to round up to an integer number of FPGAs per box, but for the power estimation, we did not round up the number as the power nearly scales with the resource usage not the number of FPGAs.

In addition, the power for the bias and flux-ramp generator needs to be estimated. For the TES bias, one 12-bit low-speed DAC per HEMT is assumed, and for the flux-ramp signal, one 12-bit medium-speed (<10 Msps) DAC is assumed. The logic to generate these signals is very simple and does not require much FPGA resource. Although it may be possible to include the logic into the Xilinx FPGA, we assume a separate PCB with a single Microsemi RTAX2000 FPGA for each box. The estimated power is 4 W per board.

Table 9 shows the estimated power for the DEEP in two observation modes: (A) an observation with the main and enhanced main arrays and (B) an observation with the ultra-high-resolution array. For ADC and DAC power, 16 W per HEMT was assumed for eight of each 1-Gsps ADC and DAC, 1 W for each, as described in a previous section. The power shown for the power card is a power loss assuming 80% efficiency. Using the MPSoC baseline design, the estimated maximum power dissipation for the DEEP is 615 W or 308 W/box. The same for the RFSoC case is 284 W or 142 W/box, and for the Virtex-5Q case, it is 995 W or 498 W/box.

The housing for the DEEP is a modular housing with a backplane, with the standard PCB size of 8 in. × 10 in. The number of PCBs per box for the MPSoC baseline design is 14:1 PCB for the bias and flux-ramp generator, 11 PCBs for the signal processing FPGA and ADC/DAC (5 for the main array, 3 for the enhanced main array, and 3 for the ultra-high-resolution

Table 9 Estimated power for the DEEP in two observation modes.

	Observation mode A:	Observation mode B:
	Main and enhanced main arrays	Ultra-hi-res array
Number of HEMTs	10 + 6	6
	UltraScale+ MPSoC space grade (RT-ZU19EG)	
FPGA power	160 W + 72 W	120 W
ADC/DAC power	160 W + 96 W	96 W
Bias/flux-ramp power	4 W	4 W
Power card (80% efficiency)	123 W	55 W
Total power	615 W	275 W
Total power per box (two boxes)	308 W	138 W
	UltraScale+ RFSoC commercial grade (XCZU27DR)	
FPGA power	160 W + 63 W	132 W
ADC/DAC power	Included in FPGA power	Included in FPGA power
Bias/flux-ramp power	4 W	4 W
Power card (80% efficiency)	57 W	34 W
Total power	284 W	170 W
Total power per box (two boxes)	142 W	85 W
	Virtex-5Q defense grade (XQ5VSX240T)	
FPGA power	440 W + 96 W	312 W
ADC/DAC power	160 W + 96 W	96 W
Bias/flux-ramp power	4 W	4 W
Power card (80% efficiency)	199 W	103 W
Total power	995 W	515 W
Total power per box (two boxes)	498 W	258 W

array), and 2 PCBs for the power card. For the signal processing PCB, one FPGA per PCB was assumed. The mass estimate for the standard PCB is 0.7 kg, but an additional thermal conductive layer needs to be added to the signal processing PCB and the power card PCB, which makes 30% increase in PCB mass (0.9 kg). The housing size was estimated as 15.5 in. × 11.5 in. × 9.5 in. with a mass of 10.2 kg. The backplane mass was estimated at 1.5 kg. Table 10 shows the summary of the size and mass for the DEEP, and the estimated total mass is 48.2 kg or 24.1 kg/box. Figure 9 shows the summary of the estimated number of each component, and the estimated size, mass, and the maximum power for each RF electronics and DEEP box.

Table 10 Estimated size and mass for the DEEP.

	Qty	Size	Unit mass (kg)	Total mass (kg)
Bias/flux-ramp PCB	2	8 in. × 10 in..	0.7	1.4
Signal processing PCB	22	8 in. × 10 in.	0.9	19.8
Power card PCB	4	8 in. × 10 in.	0.9	3.6
Backplane	2	—	1.5	3.0
Housing	2	15.5 in. × 11.5 in. × 9.5 in.	10.2	20.4
Total				48.2
Total per box (two boxes)				24.1

5 Future Work

5.1 *Tone Tracking*

Microwave SQUID multiplexers utilize warm readout electronics to digitally generate a comb of RF tones to probe the individual microwave SQUID channels. The noise performance and stability of microwave SQUID multiplexing systems can be enhanced with tone tracking electronics, which actively adapt the probe frequency to follow the changing resonance frequencies due to both the flux-ramp modulation and the x-ray pulses.

Most existing warm electronics, including the one in this study, read out superconducting resonators using RF probe tones that are fixed at the central frequency of the phase-modulated resonances. Even for an RF system that only generates tones in less than an octave of bandwidth, nonlinearities in broadband components in the signal path will generate unwanted third-order intermodulation products that will fall directly in-band. The theoretical number of third-order tones generated in an N tone system is $2N(N-1)$. For example, in a readout generating 2000 tones, nearly 8 million third-order intermodulation products will be produced, with the power in these tones growing as the cube of the power in the fundamental tones. For large multiplexing factors and sufficiently high power, the intermodulation products become an irreducible pseudonoise floor. Certain intermodulation products can also produce unwanted crosstalk.

More advanced room-temperature electronics can instead track the shifting resonator frequencies and maintain each probe tone on resonance using a closed feedback loop operating independently on each tone.[18] Tone tracking can reduce the transmitted power as much as 20 dB, greatly diminishing third-order modulation products, because, when perfectly on

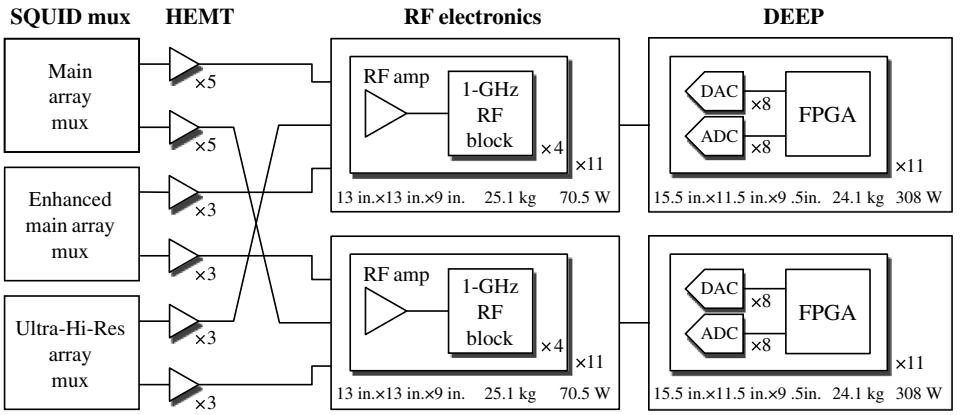

Fig. 9 The summary of the estimated number of each component, and the estimated size, mass, and the maximum component power for each RF electronics and DEEP box. The power card and bias/flux-ramp generator card are omitted in the DEEP box diagram.

resonance, most of the power is reflected off the resonator, rather than transmitted forward to the amplifier.

The advanced tone-tracking algorithms that have been implemented in the SLAC Microresonator RF electronics[18] have low computational resource needs in electronics FPGAs or ASICs, and are therefore compatible with a satellite platform, although this has not been baselined for the Lynx readout. This reduction has potential advantages improving noise, reducing crosstalk, and allowing for a reduction in bias power to the broadband components in the readout chain, improving the engineering margins for a satellite system.

5.2 *Resource Reduction*

It is interesting to consider different methods in which the resource requirement of this system can be reduced in future studies. These resources will include, but not be limited to, size, mass, and power. For example, to reduce mass and size, we can consider higher-bandwidth components. In this study, we notionally split the 4-GHz bandwidth to four 1-GHz subbands and performed several estimates. We are optimistic about the availability of higher-bandwidth components, such as a 2-GHz ADC, that are, or can be, space-qualified in the near future. In this case, it would be possible to reduce the number of LOs, I/Q modulators/demodulators, ADCs, and DACs by half. Although the estimated power for the RF electronics and DEEP would not be reduced greatly, it would be a significant mass and size reduction for the RF electronics. In addition, the reduction in the number of ADCs and DACs would help to simplify the design of the signal processing PCB which would, as a result, lower the design costs and improve the reliability.

Another example is if the UltraScale+ RFSoC can be space qualified. As discussed in Sec. 4.4, the DEEP power would then be reduced almost by half, and it would lower the total power consumption from 756 to 425 W.

5.3 *Thermal Loading and Radiation Hardness*

As strict requirements for the Lynx do not exist at this point, the thermal loading and radiation hardness of the designed system are not addressed in this study. The component power values used in this study are typical values taken from their datasheets or official power estimators. The component temperature was assumed at room temperature. In the FPGA firmware design, no mitigations were incorporated for single-event phenomena, such as single-event upsets and single-event transients. At this point, these are beyond the scope of this paper, but we hope to address them in future work.

6 Summary

For the Lynx mission, the microwave SQUID multiplexing is the baseline readout technology, and to read out three types of TES arrays of LXM with this multiplexing technology, we have studied the feasibility of space-flight compatible readout system development. The room temperature system consists of the RF electronics, which performs the frequency conversion, and the DEEP, which performs demultiplexing and event processing, the heart of the readout system. For the DEEP, we baselined using Xilinx MPSoC FPGAs. There will be two RF electronics boxes and two DEEP boxes for segmentation, and the size of the boxes are 13 in. × 13 in. × 9 in. for the RF electronics and 15.5 in. × 11.5 in. × 9.5 in. for the DEEP. The masses are 25.1 kg/box for the RF electronics box and 24.1 kg/box for the DEEP box. The maximum operating power for the RF electronics is 141 W or 70.5 W/box when operating the main array and the enhanced main array at the same time. The same for the DEEP box is 615 W or 308 W/box. The total power becomes 756 W.

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