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A TID and SEE Characterization of Multi-Terabit COTS 3D NAND Flash

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Abstract: Single-event effects and total ionizing dose testing is described for a 32-layer NAND flash memory, in both SLC and MLC configurations, with special considerations for unique three-dimensional test results.

Introduction

Results of a comprehensive SEE and TID test of Micron 32-layer 3D NAND flash devices are presented. The device is intended for use in an upcoming NASA solid-state recorder design, and includes sixteen 32-layer dice, each 256 Gb, for a total of 4 Tb of multi-level cell (MLC) flash memory in each BGA package. For enhanced reliability, the devices will be operated in a single-level cell (SLC) configuration, though test data is presented in both configurations. SEE test data were obtained on the same design but with a 4-die package in which only the top die could be exposed to heavy ion irradiation.

Device Under Test

Table I. Device characteristics

MFG:	**Micron**
P/N:	**MT29F1T08CMHBB and MT29F4T08CTHBBM5**
Type:	**32-Layer MLC NAND Flash 256 Gb die (with 4 or 16 die per package)**
LDC:	**201816**
Process:	**CMOS**

Fig. 1. Decapsulated 3D NAND device.

Test Setup

As in many of our recent tests, an ARM Cortex-M0 microcontroller (240 MHz) setup was used to directly communicate with the NAND flash devices, which were operated asynchronously at approximately 10 MHz. Calibrated laboratory power supplies provided 3.3V and 1.8V power, and both data and power were logged on a laptop computer. Various test setup components are shown below in Fig. 2.

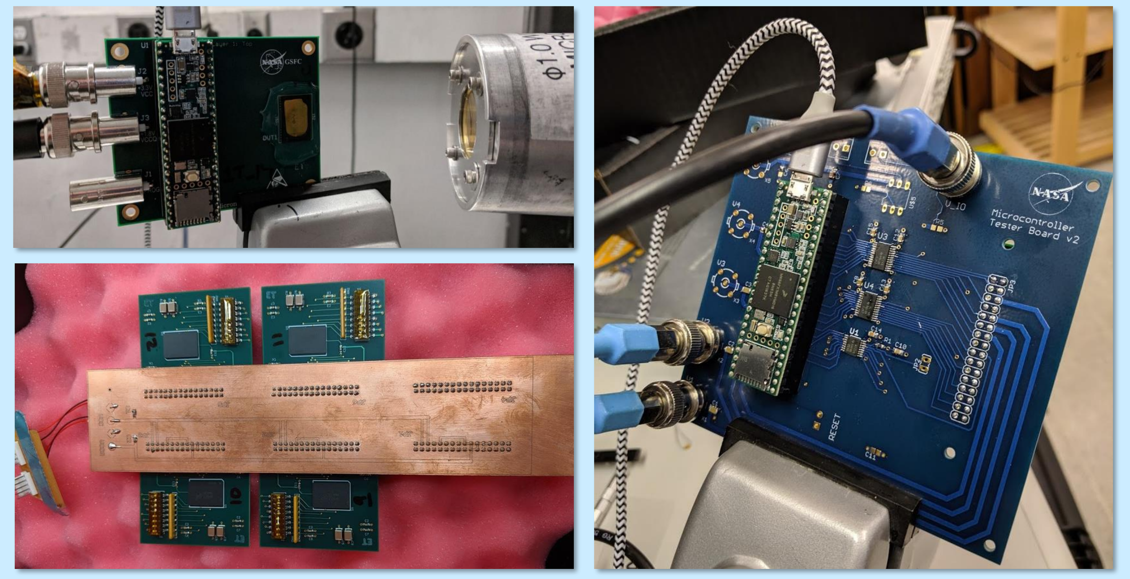

Fig. 2: Test setup components, including the integrated microcontroller/flash board built for heavy-ion irradiation (top-left); the test motherboard used for TID characterization (right); and the bias board used for standby TID irradiations (bottom-left).

Acronyms

BGA = Ball Grid Array	REAG = Radiation Effects & Analysis Group
CMOS = Complementary Metal Oxide Semiconductor	SEE = Single-Event Effects
DUT = Device Under Test	SEFI = Single-Event Functional Interrupt
GSFC = Goddard Space Flight Center	SEL = Single-Event Latchup
LDC = Lot Date Code	SEU = Single-Event Upset
LET = Linear Energy Transfer	SLC = Single-Level Cell
MeV = Mega Electron Volt	TAMU = Texas A&M University Cyclotron
MLC = Multi-Level Cell	TID = Total Ionizing Dose

Single-Event Effects

Heavy Ions: SEU, SEFI, SEL

Single-event upset data was collected with the 15-MeV/amu tune at Texas A&M, and the 10-MeV/amu tune at Lawrence Berkeley National Laboratory. Data are shown in Fig. 3, with a comparison of single-level cell (SLC) and multi-level cell (MLC) operation.

Particularly at lower LET, the device shows a higher sensitivity to single-event upsets when operated in MLC mode, where Vth margins are reduced to "store" two bits of information in one floating gate transistor.

Single-event latchup was not observed during testing at 62°C and an LET of 58.8 MeV·cm²/mg.

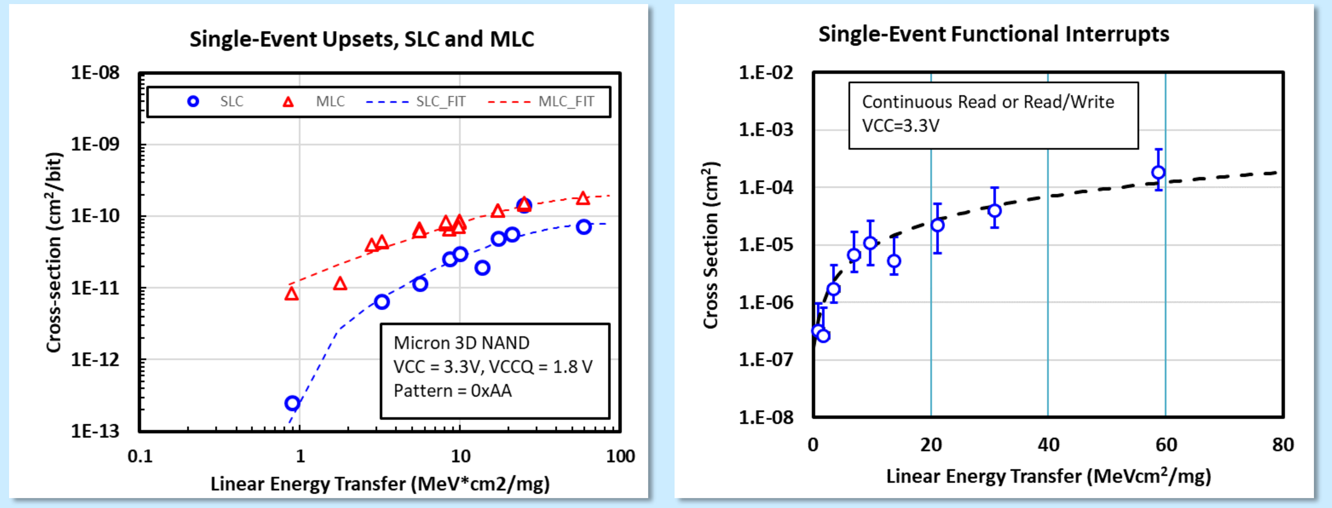

Fig. 3. SEU (left) and SEFI (right) cross-sectiosn with Weibull curve fits

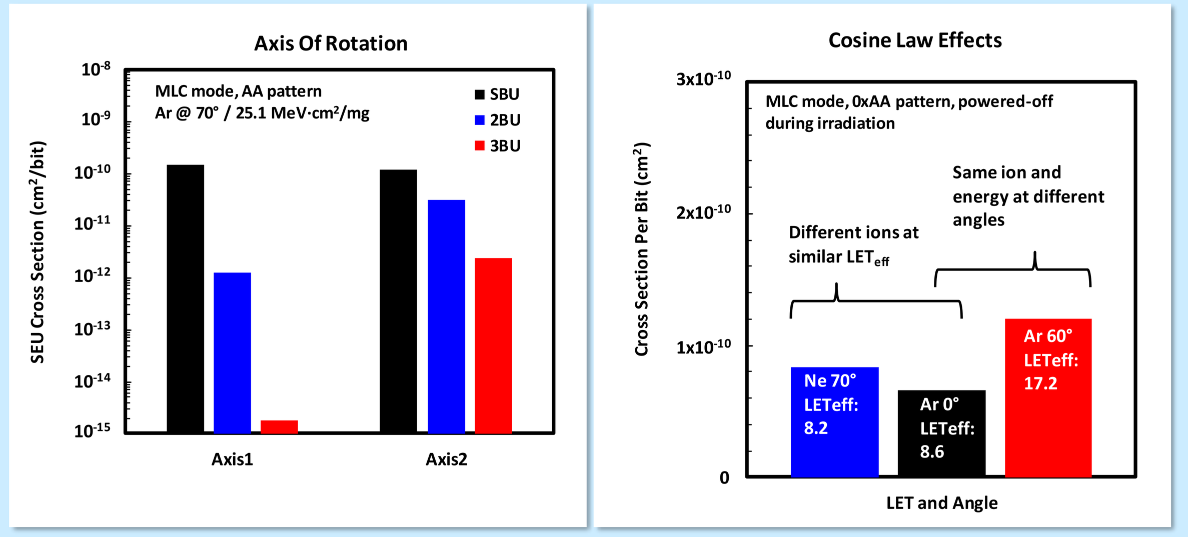

Fig. 4. Effects of angular rotation on SEU cross section, with different axes of rotation (left) and different effective LETs (right).

Angular Heavy-Ion Effects on SBU/MBU

A strong angular dependence on single-bit and multi-bit upsets is shown in Fig. 4 (left). Argon ions striking the die down the long-axis of the device at a 70° angle created a high number of multi-bit upsets, including those with at least three upset bits per byte (red).

Fig. 4 (right) shows the relationship between angle of incidence and effective LET (calculated as 1/cos(θ)). These irradiations are taken along "Axis 1" from the left figure, to minimize the effect of MBU, and only count the number of bytes in error. The red and black bars suggest higher LET_{eff} results in higher cross section (as expected), though the blue and black bars hint at a three-dimensional effect: the 70° strike upsets more cells than expected given its somewhat lower LET.

Pattern Dependence

Memories irradiated in SLC mode showed a strong dependence on data pattern (Fig. 5); cells in an erased state ('1') were rarely upset, while those in a programmed state ('0') were more susceptible. In MLC mode, no data pattern dependence was observed. Data is charted in Fig. 5.

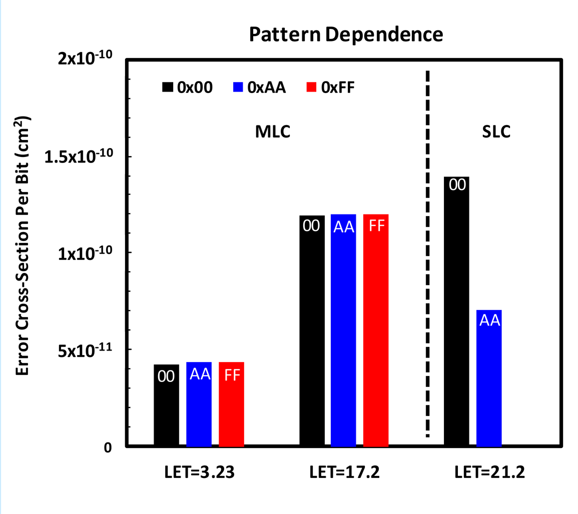

Fig. 5. Data pattern dependence for SLC and MLC modes.

Three-Dimensional (Multi-layer) Upsets

In addition to the simple SBU/MBU analysis within each byte shown in Fig. 4, data can also be presented showing particle tracks in the three-dimensional volume of the memory. In this manner, it is possible to observe multi-cell upsets from individual heavy ions.

For example, four prominent ion strikes in Fig.6 (left) consist of ~32 single-bit upsets each, distributed on the same byte address of 32 different pages as the particle traverses the vertical structure. The ion tracks in Fig. 6 (right) show the angular irradiations. Both are from SLC-mode operation.

MLC plots are omitted for space, but show similar 3D upset tracks, with a much higher level of background noise due to the higher intrinsic error rate.

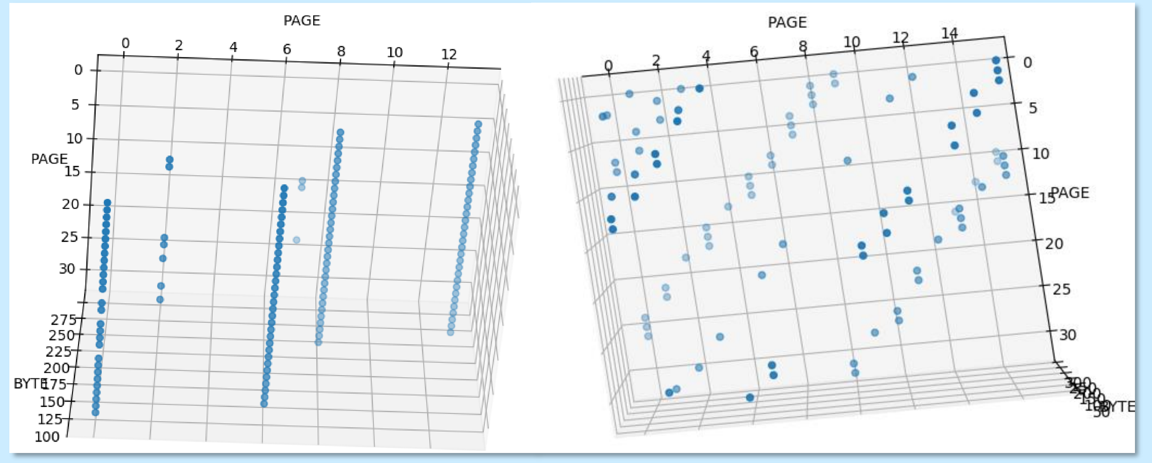

Fig. 6. Three-dimensional upset tracks for normal-incidence (left) and angled (right) heavy-ion testing in SLC mode.

Total Ionizing Dose

Erase Circuitry

NAND flash TID failures are typically attributed to higher-voltage charge pump transistors in the erasure circuitry [1-4]. Fig. 7 shows an irradiation performed with dynamic SLC Erase-Program-Read cycles actively run during exposure. The byte error rate of each cycle remains relatively low until approximately 40 krad(Si), where it rapidly jumps to 100%.

At the same time, the I_{CC} during erase operations was carefully monitored for changes (an external V_{PP} supply was not used). The erase current increased with dose as expected, with an odd (and repeatable across devices) discontinuity near 30 krad.

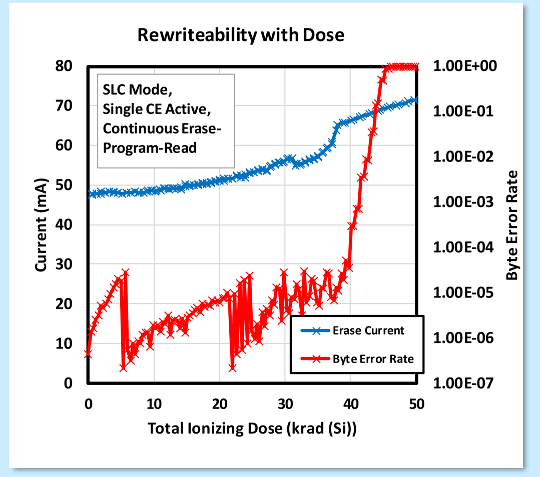

Fig. 7. Erase operation supply current and post-write raw bit error during continuous E-P-R cycling for a single device.

Readback Circuitry

Ionizing radiation deposits charge in the oxides of a floating gate cell with much the same results as programming a cell; in either case, the threshold voltage of the transistor is altered. Without periodically refreshing/reprogramming the memory, the threshold voltages will shift far enough to change the value stored.

Fig. 8 shows an irradiation under constant read-only cycling for SLC and MLC modes. With lesser margins, MLC mode shows a faster increase in error rate with accumulated dose.

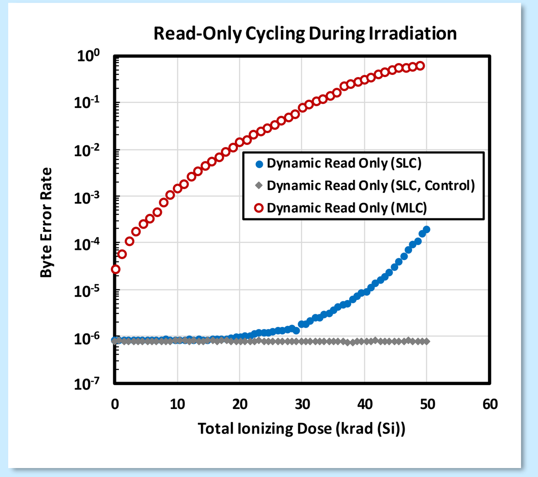

Fig. 8. Proportion of read-only bytes in error for SLC and MLC devices, along with a control curve for the SLC device.

Error Distribution by Page

A non-uniform distribution of errors is evidenced by the histograms in Fig. 12, showing the number of errors per page at 25 krad and 50 krad for a single device operated in SLC mode.

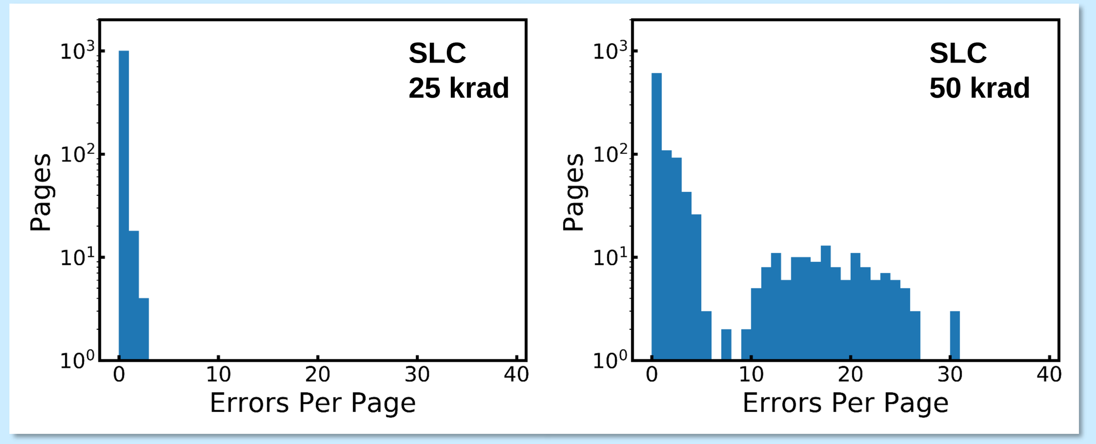

Fig. 12. Distribution of errors per page in SLC mode.

Three-Dimensional TID Response and Directionality

Extracting three-dimensional dependence of TID errors by the same means used for 3D SEU mapping produced a starkly non-uniform result through the material that will require further analysis. A pair of representative plots are shown in Fig. 13 to illustrate this effect. Irradiation in opposite directions to 50 krad (top) and 45 krad (bottom) in SLC mode shows no clear directional dependence to the relative distribution of errors. Each plot is 10 blocks with page numbers shuffled to show estimated physical layer on the y-axis (x-axis is non-physical). Analysis of both the raw test data and the test software did not show any systemic test setup failure that would account for this distribution.

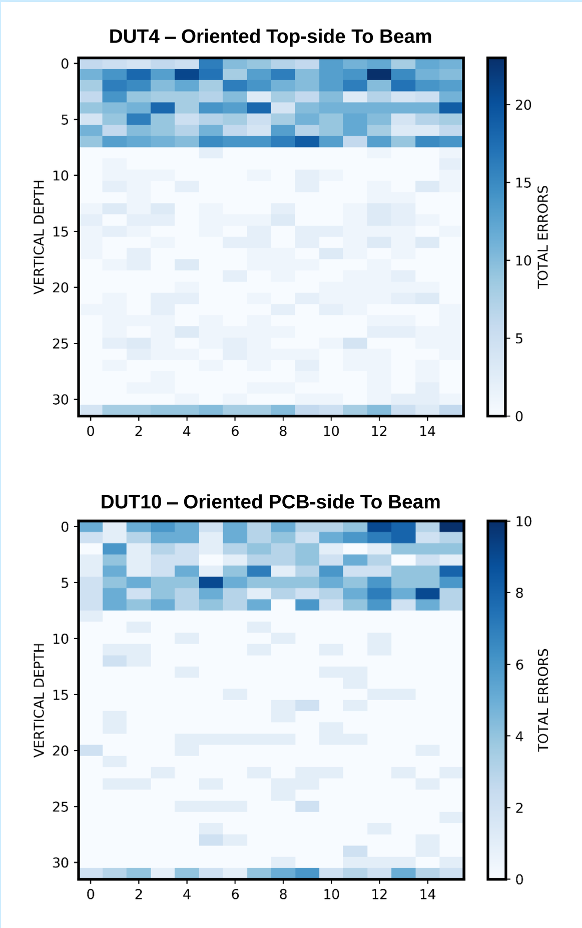

Fig. 13. Typical distribution of errors shown for two devices irradiated in opposite directions (to slightly different doses; 50 krad top, 45 krad bottom).

Dose-Step Irradiations vs Dynamic

The effects of testing with a continuous reading cycle during irradiation compared to irradiating the part in a ground or biased (standby) configuration are presented in Fig. 9. The devices actively read during irradiation show a faster increase in error rate with dose compared to the biased (standby) parts or the unbiased (grounded) parts. Reference the control part in Fig. 8 to observe that no apparent read-disturb issues are observed at this level of repeated readback.

Since the high-voltage charge pump circuits are most vulnerable to TID, a comparison is made in Figs. 10 and 11 between typical dose-step irradiation (both biased and grounded) and a continuous cycling of Erase-Program-Read operations during irradiation. While multiple effects are involved (e.g., accumulated number of erase cycles, time between measurements, short-term annealing) the worst-case failure occurs when the high-voltage erase circuitry is active during irradiation and may warrant additional study.

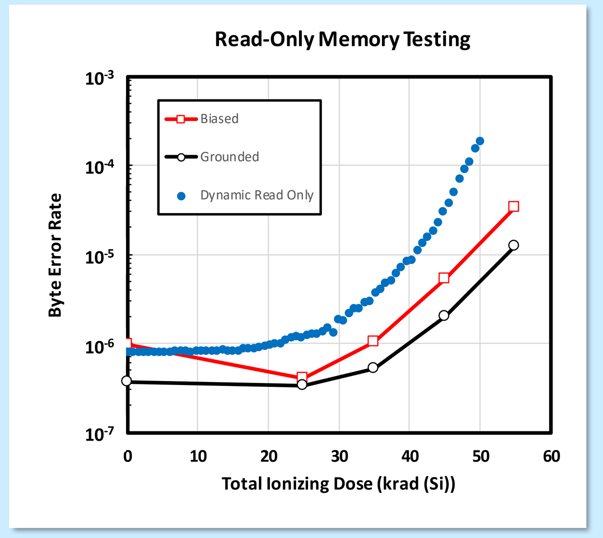

Fig. 9. Proportion of read-only bytes in error for biased, unbiased, and dynamic operation during irradiation.

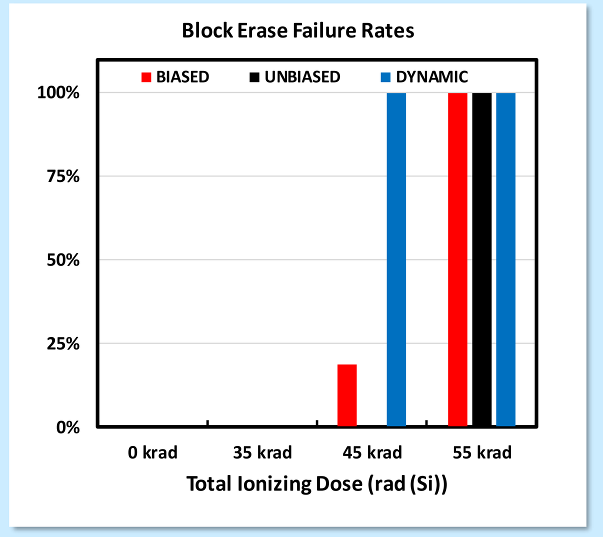

Fig. 10. Block erase failure dose points by biasing type.

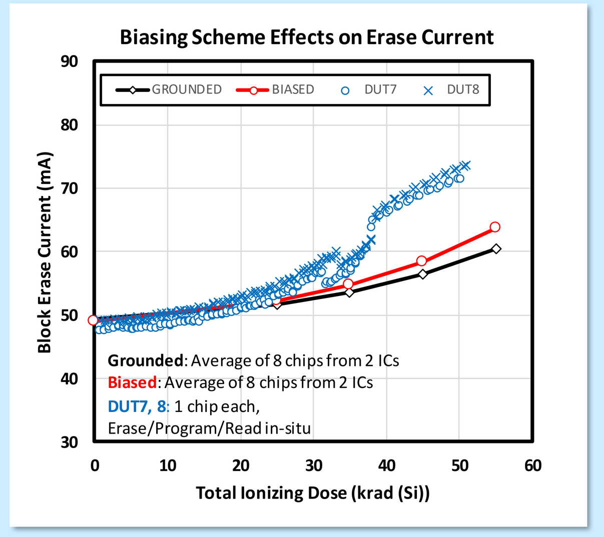

Fig. 11. Erase operations dynamically performed during irradiation compared to a typical dose-step test.

Acknowledgments

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