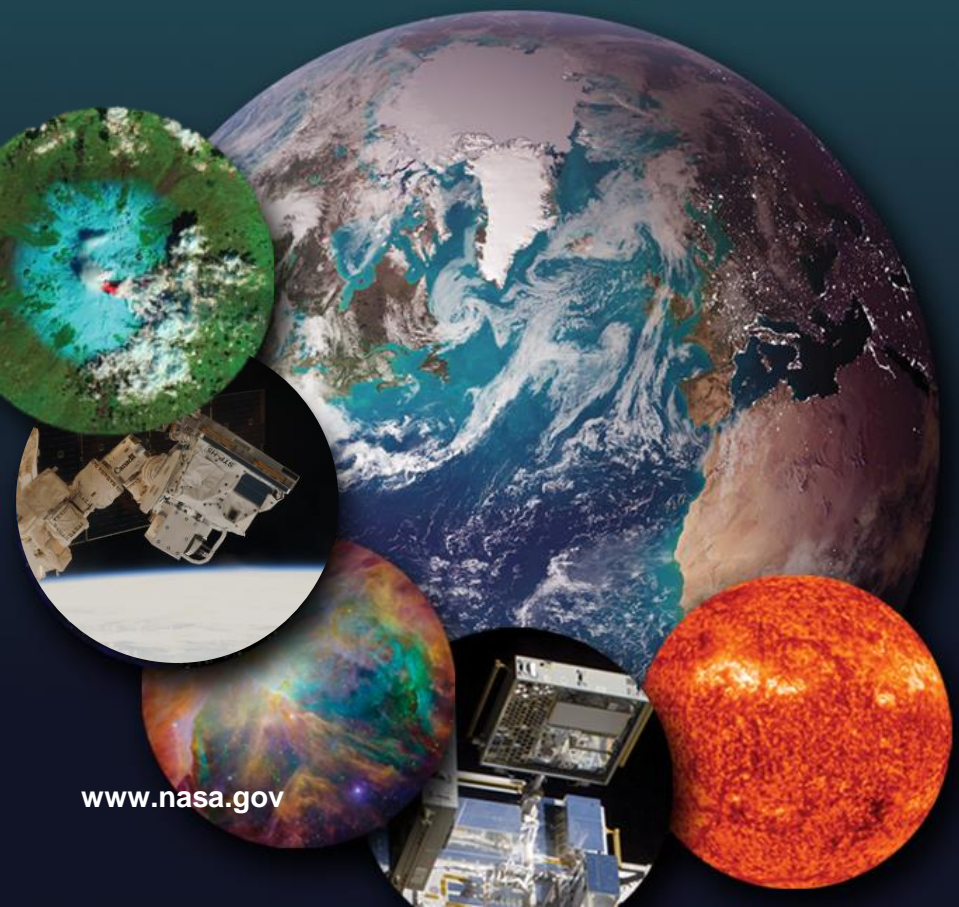National Aeronautics and Space Administration

SpaceCube v3.0 Mini
NASA Next-Generation Data-Processing System for Advanced CubeSat Applications

SpaceCube

Cody G. Brewer
Science Data Processing Branch
Software Engineering Division
NASA - Goddard Space Flight Center
Greenbelt, MD, USA

The Twelfth Space Computing Conference

July 2019

www.nasa.gov

Acronyms

Acronym	Definition
BL-TMR	BYU-LANL TMR
cFE	Core Flight Executive
cFS	Core Flight System
CHREC	Center for High-performance Reconfigurable Computing
CPU	Central Processing Unit
CSP	CHREC/CubeSat Space Processor
DSP	Digital Signal Processor
ELC	ExPRESS Logistics Carrier
EM	Engineering Model
FF	Flip-Flop
FLT	Flight
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GMSEC	Goddard Mission Services Evolution Center
GOPS	Giga-Operations Per Second
ISA	Instruction Set Architecture
LEO	low-Earth Orbit
MGT	Multi-Gigabit Transceiver
MIPS	Million instructions per second
NSF	National Science Foundation
ORS	Operationally Responsive Space
PCB	Printed Circuit Board
RE	Recuring Engineering
SBC	Single-Board Computer

Acronym	Definition
SEL	Single-Event Latchup
SEM	Soft Error Mitigation
SSIVP	Spacecraft Supercomputing for Image and Video Processing
STP-Hx	Space Test Program Houston
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TRL	Technology Readiness Level
UVSC	Ultraviolet Spectro-Coronagraph

Outline

1 Introduction and Background

2 SpaceCube Mini

- SpaceCube Introduction
- SpaceCube Approach
- Mini Design Philosophy
- SmallSat CubeSat Challenges

3 Fault-Tolerant Design

- Xilinx Space-grade Devices
- Kintex UltraScale
- Soft-Core Processors
- Configuration Schemes & Operation

4 Software and Deployment Examples

- cFE/cFS
- Deployment Configurations
- Specifications

5 Conclusion

INTRODUCTION AND BACKGROUND

Science Data Processing Branch Embedded Processing Group (EPG)

EPG Group Specializes in Embedded Development
- Hardware acceleration of algorithms and applications
- Intelligence, autonomy, and novel architectures
- Flight software integration for development platforms
- Advanced architectures and research platforms

Advanced Platforms for Spaceflight
- SpaceCube v2.0 and v2.0 Mini
- SpaceCube v3.0, v3.0 Mini
- SpaceCube Mini-Z and Mini-Z45

Key Tools and Skills
- **Flight Software**: cFE/cFS, driver integration, flight algorithms
- **GSE**: COSMOS, GMSEC, system testbeds
- **FPGA Design**: Hardware acceleration, fault-tolerant structures
- **Mission Support**: Supporting flight cards, algorithm development
- **On-board Autonomy and Analysis**: deep-learning frameworks, unique architectures

SpaceCube v2.0

5

SpaceCube Introduction

What is SpaceCube?

A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs

High performance reconfigurable science / mission data processor based on Xilinx FPGAs

– Hybrid processing … CPU, DSP, and FPGA logic

– Integrated "radiation upset mitigation" techniques

– SpaceCube "core software" infrastructure (cFE/cFS and "SpaceCube Linux" with Xenomai)

– Small "critical function" manager/watchdog

– Standard high-speed (multi-Gbps) interfaces

SpaceCube is Hybrid Processing...

6

SpaceCube Heritage

Closing the gap with commercial processors while retaining reliability

- **57+ Xilinx device-years on orbit**
- **26 Xilinx FPGAs in space to date (2019)**
- **11 systems in space to date (2019)**
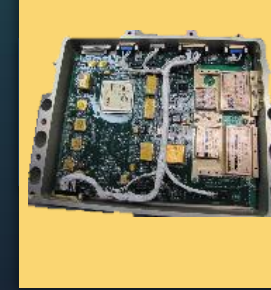
SpaceCube is Mission Enabling...

SpaceCube v1.0
STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5
SMART (ORS)

SpaceCube v2.0-EM
STP-H4, STP-H5
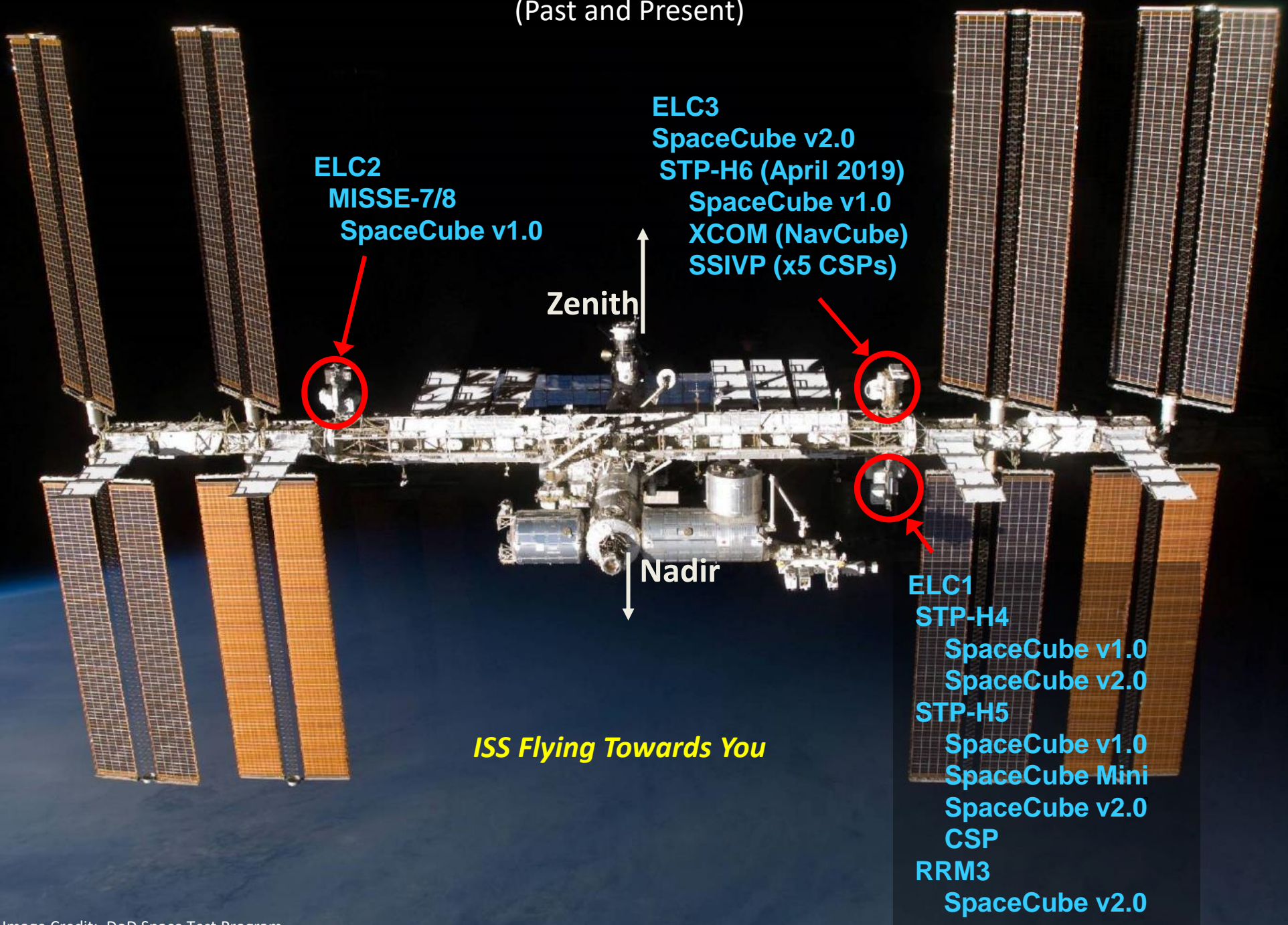
SpaceCube v2.0-FLT
RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini
STP-H5, UVSC-GEO

SpaceCube on the ISS

(Past and Present)

ELC2
MISSE-7/8
SpaceCube v1.0

ELC3
SpaceCube v2.0
STP-H6 (April 2019)
SpaceCube v1.0
XCOM (NavCube)
SSIVP (x5 CSPs)

Zenith

Nadir

ISS Flying Towards You

ELC1
STP-H4
SpaceCube v1.0
SpaceCube v2.0
STP-H5
SpaceCube v1.0
SpaceCube Mini
SpaceCube v2.0
CSP
RRM3
SpaceCube v2.0

Image Credit: DoD Space Test Program

SpaceCube Approach

01 The traditional path of developing radiation-hardened flight processor **will not work** …
they are always one or two generations behind

02 Use latest radiation-tolerant* processing elements to achieve massive **improvement** in "MIPS/Watt" (for same size/weight/power)
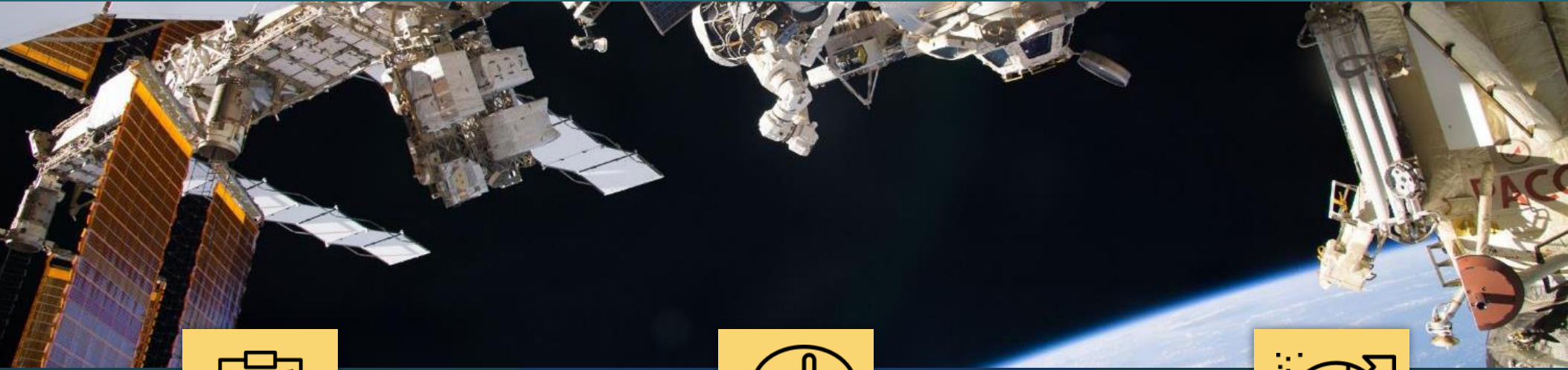
03 Accept that radiation induced upsets may happen occasionally and just deal with them appropriately …
any level of reliability can be achieved
via **smart system design!**

*Radiation tolerant – susceptible to radiation induced upsets (bit flips)
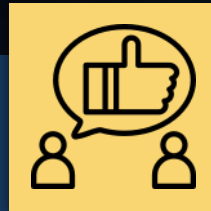but not radiation-induced destructive failures (latch-up)

SPACECUBE MINI

Goals, Motivations, Challenges

Goals

Develop reliable, high-speed hybrid processor using SpaceCube design approach to **enable next-generation instrument and CubeSat capability**

Motivations

Many commercial CubeSat processor offerings primarily target benign LEO orbits and do not strongly address **radiation concerns and parts qualification**

Need exceptional capability to support **complex applications** such as artificial intelligence

Challenges

Managing PCB area restrictions for rad-hard components, balancing cost, educating mission designers for key reliability differences

SpaceCube v2.0 Mini

Overview of SpaceCube v2.0 Mini

- **TRL9 flight-proven** processing system, miniaturized version of SpaceCube v2.0 Processor Card for CubeSats
- 1U CubeSat (10 × 10 × 10 cm) size
- Typical power draw: <10 W
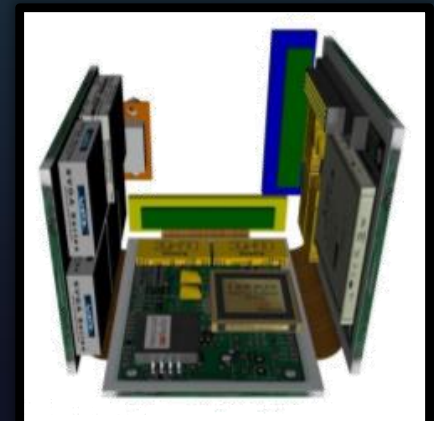- Scalable design allows daisy-chaining of Mini cards with Gigabit interface

SpaceCube v2.0 Mini Unfolded

Flight Deployment

Missions and Heritage

- Launched Feb 2017 to ISS on STP-H5/ISEM as mission manager card for several DoD experiments
- Instrument processor for Ultraviolet Spectro-Coronagraph (UVSC) Pathfinder to be launched to GEO on STPSat-6

SpaceCube Mini-Z (CSPv1)


Original CSPv1

Overview of SpaceCube Mini-Z

- Collaborative development with **NSF CHREC** at University of Florida for Zynq-based 1U Board
  - Selective population scheme between commercial and rad-hard components
  - Rapid deployment prototyping
  - Convenient pre-built software packages with cFS
- **Re-Envisioned** to support quality-of-life upgrades and enable specific NASA mission needs
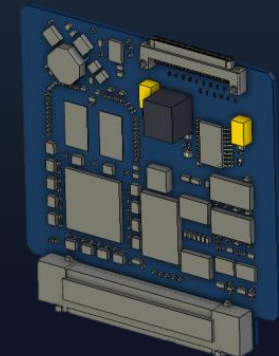

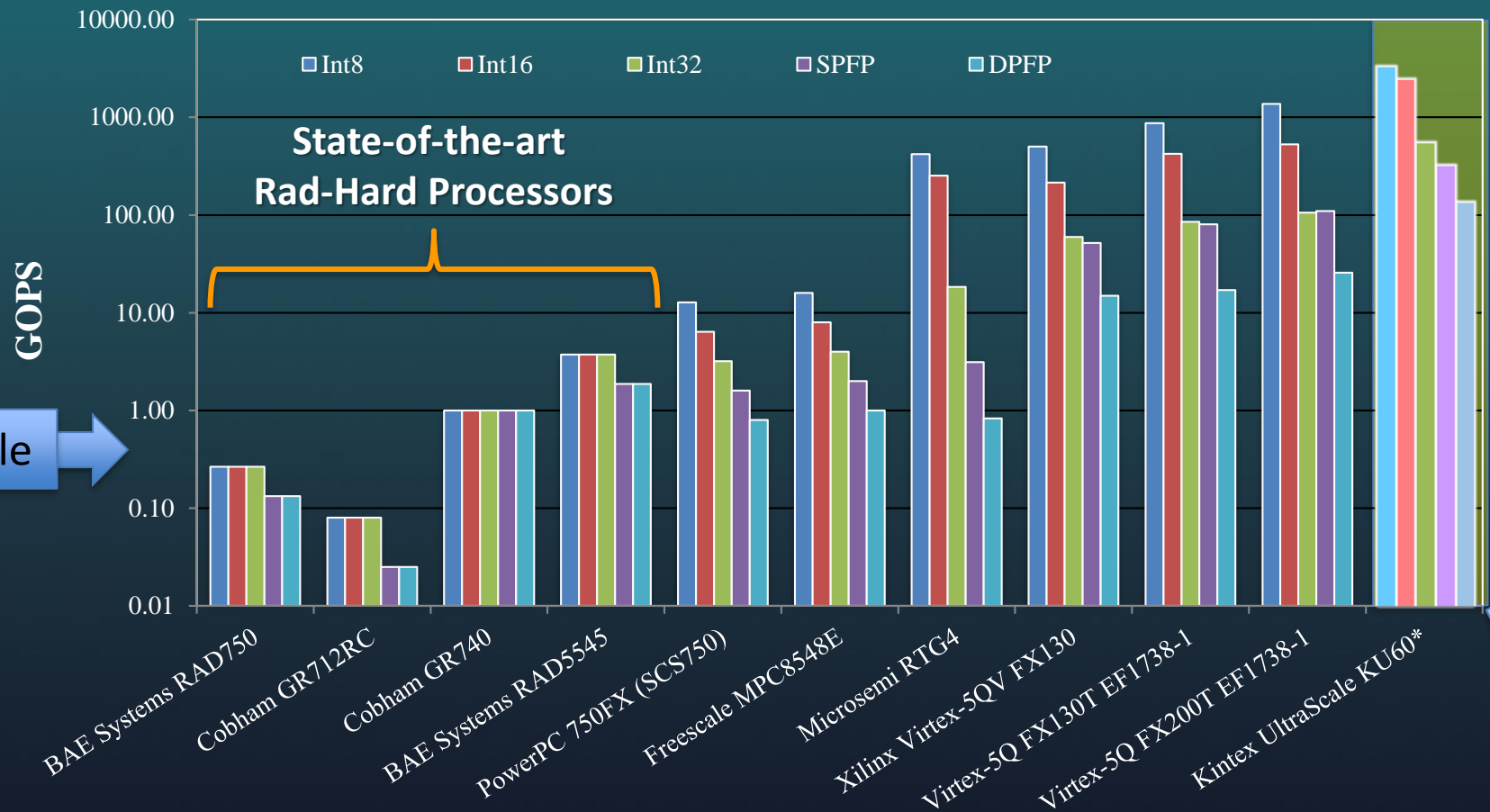CSPv1 Development Board
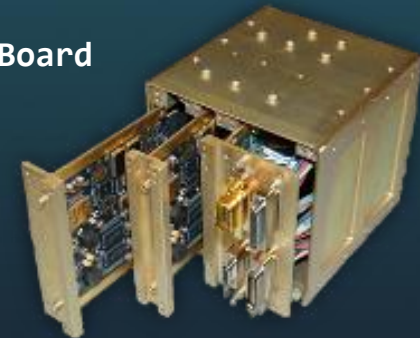
STP-H5/CSP Flight Unit

Missions and Heritage

- Launched Feb 2017 to ISS on STP-H5/CSP featuring 2 CSPv1 cards performing image processing
- Launched May 2019 to ISS on STP-H6/SSIVP featuring 5 CSPv1 for massive parallel computing
- Featured on many more…

NASA SpaceCube Mini-Z

Performance

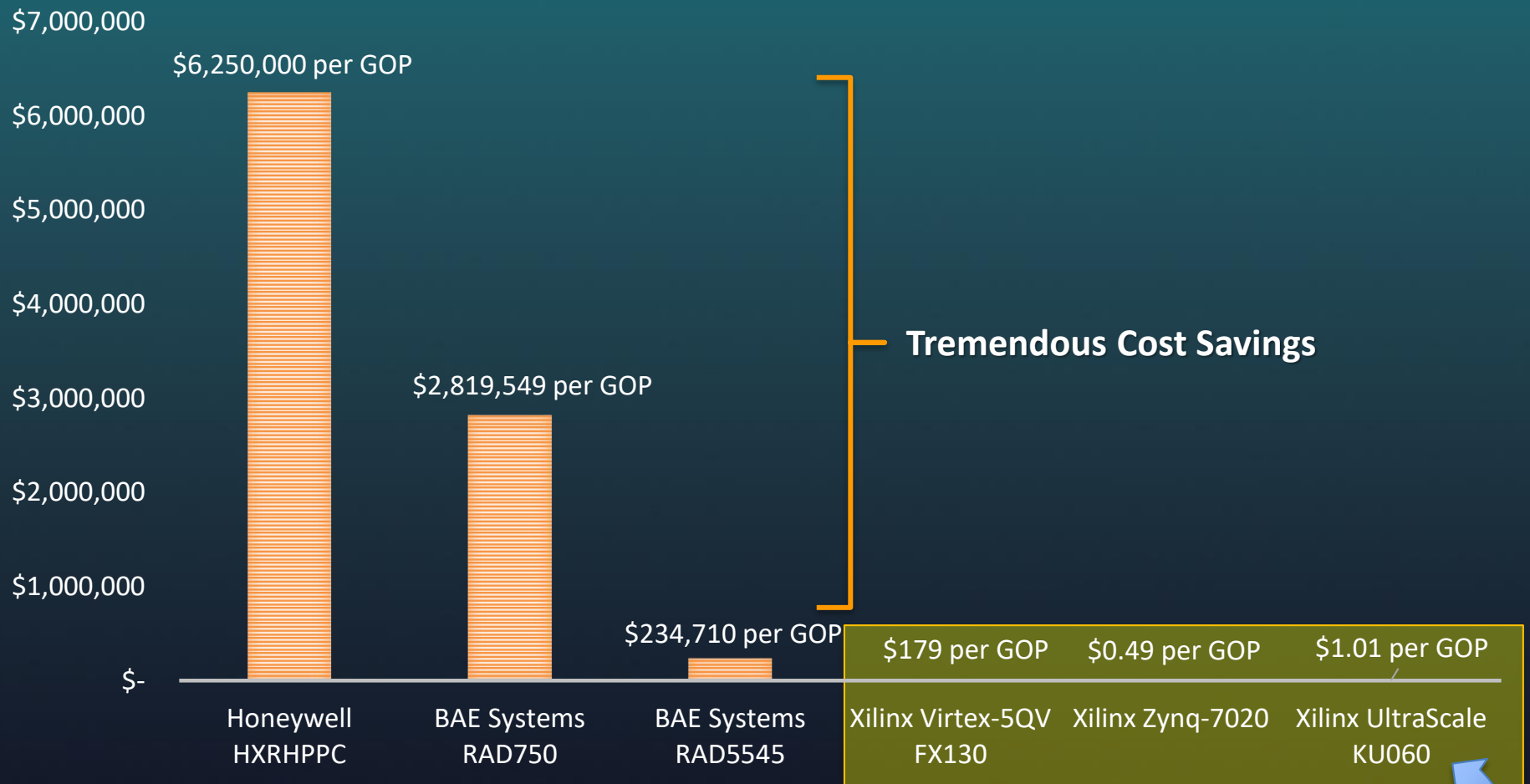

State-of-the-art Rad-Hard Processors

Note Log Scale

Lovelly, T. M. and George, A D., "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics,"AIAA Journal of Aerospace Information Systems, Vol. 14, No. 3, Mar. 2017, pp. 184-197. doi: 10.2514/ 1.I010472

Device used in SpaceCube v3.0 Mini

*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

Affordability

COST TO ACHIEVE '1' GOP*

$6,250,000 per GOP — Honeywell HXRHPPC

$2,819,549 per GOP — BAE Systems RAD750

$234,710 per GOP — BAE Systems RAD5545

Tremendous Cost Savings

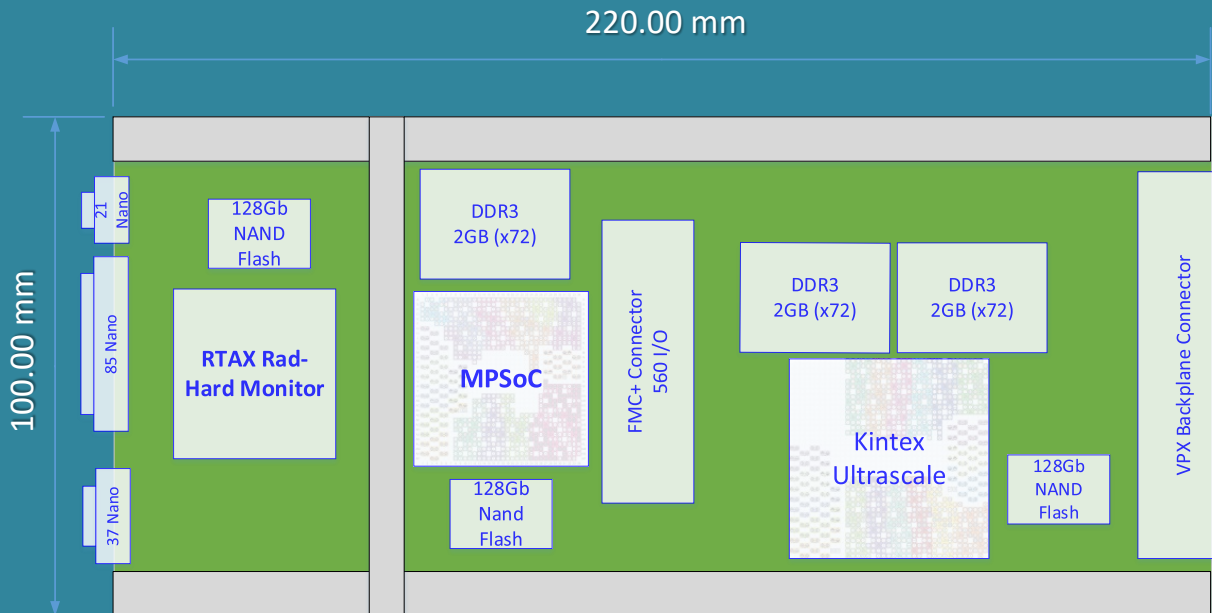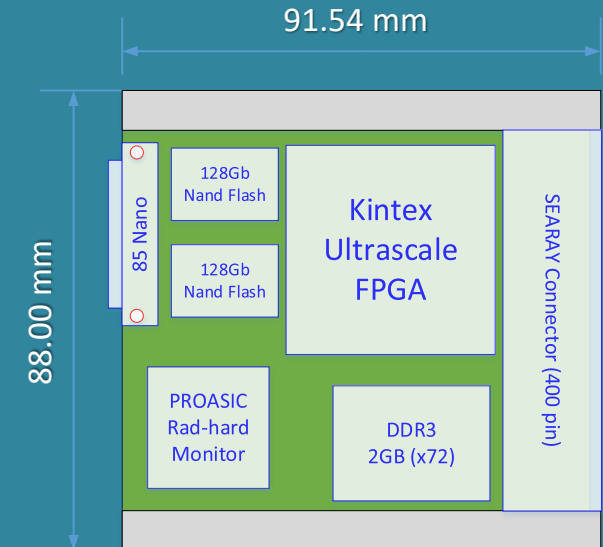| $179 per GOP	$0.49 per GOP	$1.01 per GOP
Xilinx Virtex-5QV FX130	Xilinx Zynq-7020	Xilinx UltraScale KU060

Devices used in SpaceCube Family

*Represents Average Estimated Price Over Survey Data. Device Cost is Proprietary and Quantity Dependent. Contact Vendor for Additional Details. Kintex Results based on previous chart GOPS assumption and industrial-grade device

SpaceCube v3.0 Mini - NASA Goddard Space Flight Center – July 2019

Mini Design Philosophy

SpaceCube v3.0 Processor Card

220.00 mm

100.00 mm

- 21 Nano
- 85 Nano
- 37 Nano
- 128Gb NAND Flash
- RTAX Rad-Hard Monitor
- DDR3 2GB (x72)
- MPSoC
- 128Gb Nand Flash
- FMC+ Connector 560 I/O
- DDR3 2GB (x72)
- DDR3 2GB (x72)
- Kintex Ultrascale
- 128Gb NAND Flash
- VPX Backplane Connector

SpaceCube v3.0 Mini

91.54 mm

88.00 mm

- 85 Nano
- 128Gb Nand Flash
- 128Gb Nand Flash
- PROASIC Rad-hard Monitor
- Kintex Ultrascale FPGA
- DDR3 2GB (x72)
- SEARAY Connector (400 pin)

Same Approach, Smaller Size
SpaceCube design approach applied to smaller form-factor

Key Design Reused
Much of UltraScale design and interface remain same between cards including DDR Pinout
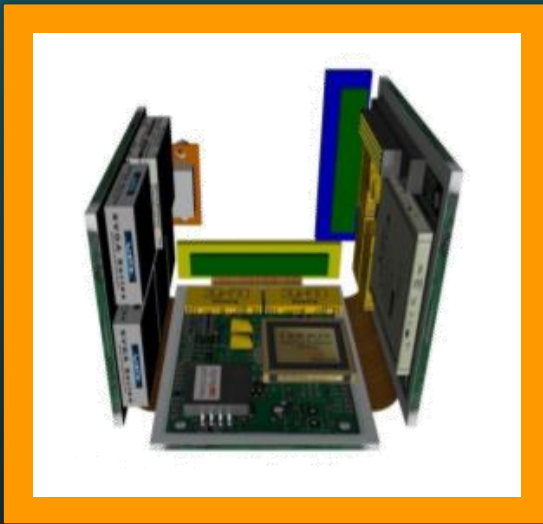
Supervision Requested
Radiation-hardened monitor architecture and code reusable

Trade in, Trade Out
EEE parts trades, analysis, and circuits extensively leveraged from main card design

Mini Form Factor Lessons Learned

SpaceCube v2.0 Mini
Lessons Learned

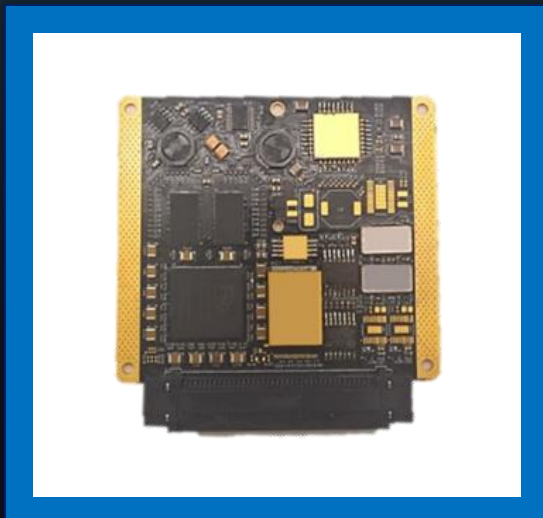

CSPv1
Lessons Learned

Manufacturability
Difficult to manufacture due to rigid-flex and laser-drilled microvias. Tied to single vendor design.

Monitor Design
Aeroflex rad-hard monitor was effective, however, limited by FPGA resources preventing more robust design

CubeSat Connector
Samtec SEARAY connector provided flexibility and performance, same connector used with SpaceVNX (VITA 74.4)

Backplane Advantage
Backplane allows swapping of individual card as advances/improvements are made and can easily incorporate new components

17

SmallSat/CubeSat Processor Challenge

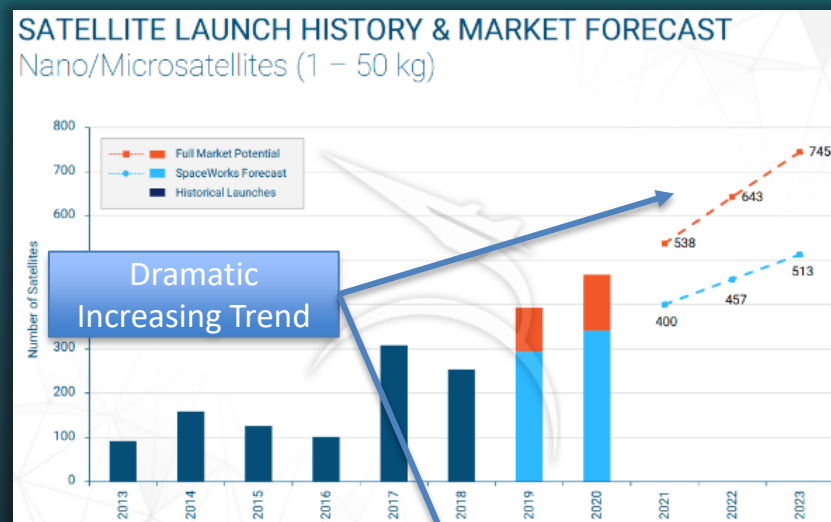**Massively Expanding Commercial Market for SBCs**

- Tons of commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc...)

**Mission Developers Seeking Commercial Hardware**

- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat "Kit" types of cards

Not Designed With Harsh Orbit Considerations Beyond LEO

- Many vendors have performed limited radiation testing and largely support missions in more benign LEO orbits
- Mission is radiation test approach
- Little-to-no additional radiation testing or parts qualification
- No recommendations for fault-tolerant configurations of offered SBCs

SATELLITE LAUNCH HISTORY & MARKET FORECAST
Nano/Microsatellites (1 – 50 kg)

Dramatic Increasing Trend

"2019 Nano/Microsatellite Forecast, 9th Edition," SpaceWorks Enterprises, Inc., Jan 2019.
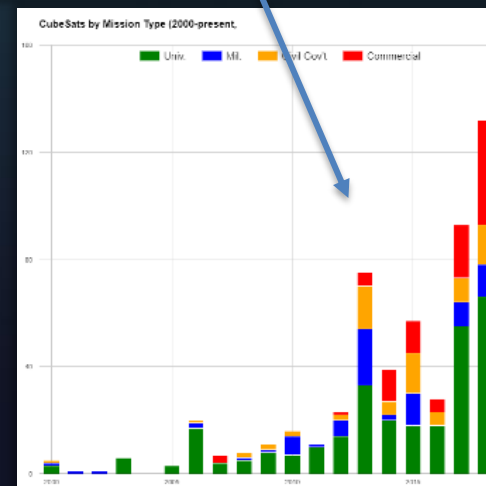
M. A. Swartwout @ The CubeSat Database

FAULT-TOLERANT DESIGN

Xilinx Space Devices Compared

	SpaceCube v1.0		SpaceCube v2.0	SpaceCube v3.0	
	XQR4V **(RT, 1.2V)**		**XQR5V** **(RHBD, 1.0V)**	**XQRKU060** **(RT, 1.01V)**	**KU060 vs. V5**
Resource	**FX60**	**FX140**	**FX130**	**KU060**	
Logic Cells	56,880	142,128	131,072	726,000	5.54x
CLB FF	50,560	126,336	81,920	663,360	8.10x
Max Distributed RAM (Kb)	395	987	1,580	9,180	5.81x
Total Block RAM (Kb)	4,176	9,936	10,728	38,000	3.54x
BRAM/FIFO ECC (36 Kb)	--------	--------	--------	1,080	N/A
DSP Slices	128	192	320	2,760	8.63x
MGT			18 @ 4.25 Gbps	32 @ 12.5 Gbps	5.23x
TID (krad)	300	300	1,000	120	(0.12)
SEL	>125	>125	>125	~80	(0.64)
Flow	V-Flow (QML-V)		B-Flow (QML-Q) V-Flow (QML-V)	B-Flow (QML-Q) Y-Flow (QML-Y Compliant)	N/A
Package	35 x 35 mm	40 x 40 mm	45 x 45 mm	40 x 40 mm	(0.78)

"Xilinx's Adaptive FPGAs for Space
Applications" White Paper

Xilinx Kintex UltraScale XQRKU060

- First 20 nm FPGA for Space
  - Designed for SEU mitigation (>40 patents)
  - Deploys same commercial silicon mask set
  - Uses Vivado UltraFast Development

- Ruggedized 1509 CCGA
  - 40 mm x 40mm package
  - Footprint compatible A1517

- Product Space Test Flows
  - B-Flow (QML-Q Equiv.) and Y-Flow (QML-Y Compliant)

> Lee, D., Allen, G., Swift, G., Cannon, M., Wirthlin, M., George, J. S., Koga, R., and K. Huey, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," IEEE Radiation Effects Data Workshop, July 13-17, 2015.

- Commercial Radiation Testing Results
  - Improved Xsect compared to 7 series
  - No observed classical SEL signatures

> Berg, M., Kim, H., Phan, A., Seidleck, C., Label, K., and M. Campola, "Xilinx Kintex-UltraScale Field Programmable Gate Array Single Event Effects (SEE) Heavy-ion Test Report," NASA Electronic Parts and Packaging, 2017.

Fault-Tolerant Soft-Core Processing

Xilinx TMR MicroBlaze[1]

- Built-in Xilinx TMR solution for newer FPGAs
- Includes TMR SEM IP Core
- Vivado IP integrator for easy project creation

BL-TMR MicroBlaze[2]

- BYU-LANL TMR Tool (BL-TMR) provides automated TMR application
- Fault Injection on MicroBlaze performed for SpaceCube v2.0

BL-TMR RISC-V[3]

- RISC-V is a promising new ISA processor gaining popularity for Intel and Xilinx FPGAs
- Neutron radiation test of Taiga RISC-V
- 27% decrease in operational frequency, for 33x improvement in cross section

Resource Utilization of TMR Designs on KU040

Resource	Unmitigated MicroBlaze	Xilinx TMR MicroBlaze	BL-TMR MicroBlaze	BL-TMR RISC-V[3]
LUTs	3.29%	9.81%	15.58%	0.80 %
CLB FF	1.63%	4.77%	4.89%	0.20 %
BRAM/FIFO ECC (36 Kb)	12.50%	37.50%	37.50%	1.00 %
DSP Slices	0.31%	0.94%	0.94%	0.20 %
FMax	-----	0.95x	0.88x	0.73x

BL-TMR v6.3, MicroBlaze v11, 32-bit 5-stage, FPU, 32 Kb I/D, Vivado 2019.1,

[1]Microblaze Triple Modular Redundancy (TMR) Subsystem v1.0, https://www:xilinx:com/support/documentation/ip documentation/tmr/v1 0/pg268-tmr:pdf, Xilinx, 10 2018.
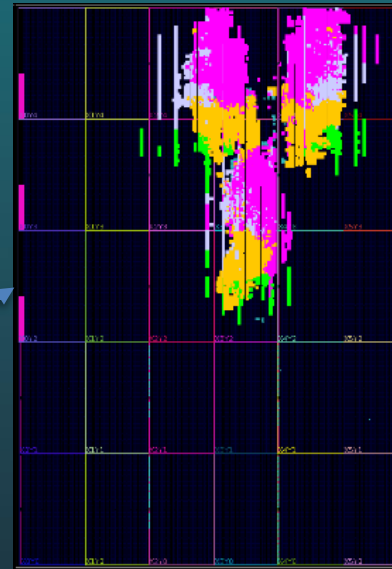
[2]http://reliability.ee.byu.edu/edif/

[3]A. Wilson and M. Wirthlin, "Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processors on Xilinx SRAM-based FPGAs," 12th Space Computing Conference, July 30 – August 1, 2019.
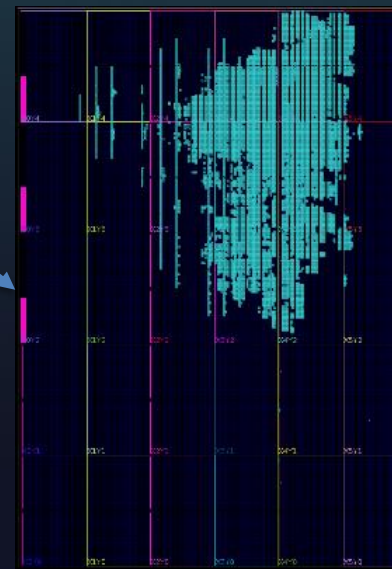
TMR Floorplan Design on KU060

Different Granularity of TMR
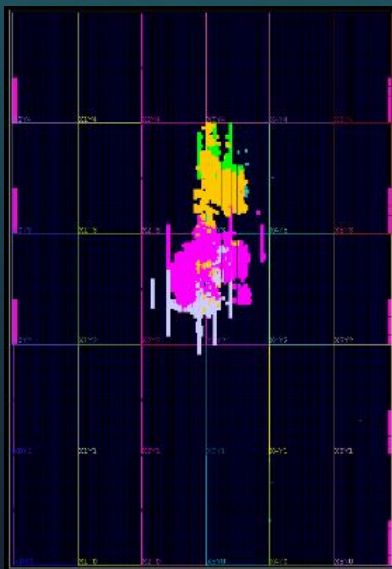
Microblaze (magenta)
Interconnects/AXI (yellow)
Caches (green)
Local memory (light)

Unmitigated MicroBlaze

Xilinx TMR MicroBlaze

BL-TMR MicroBlaze

BL-TMR tool completely flattens design and removes hierarchical information about the design

SCv3.0 Mini Booting Configuration
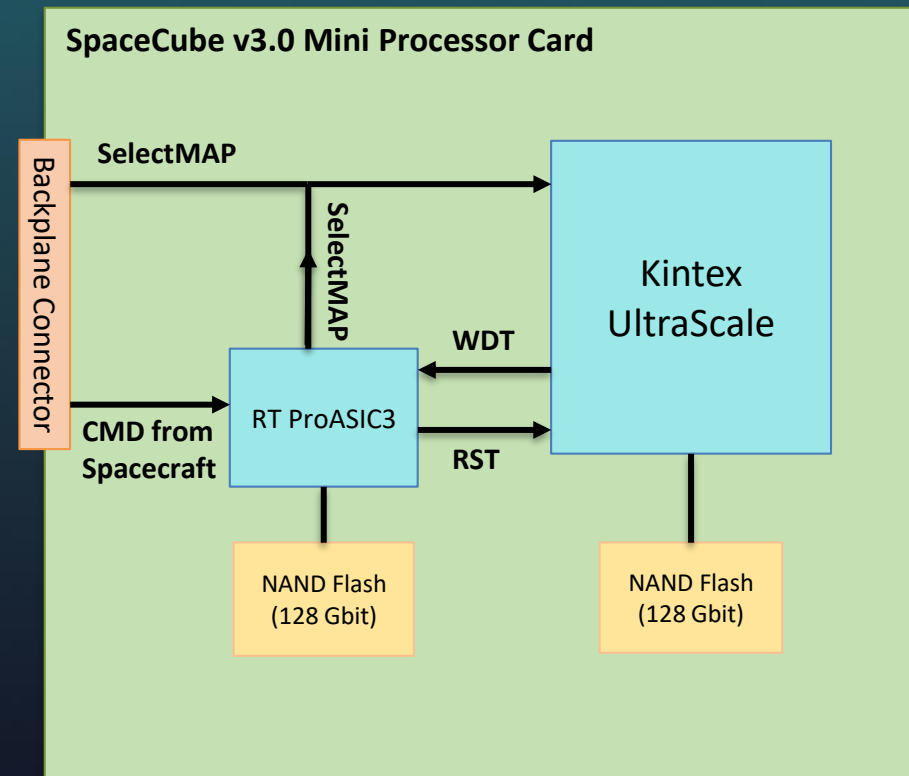
Selectable Configuration

- Kintex configured via SelectMAP from **backplane** or on-board **RTProASIC3** supervisor
- Dozens of configuration files stored with redundant copies across multiple internal dies

Robust RTProASIC Monitor

- Verifies configuration files are valid via page-level CRC checks
- Can reconstruct valid configuration file from several corrupted ones
- Internal FSM ensures Kintex programming and boot sequence is completed correctly
- Automatic program retry

Flexible Configuration

- Can be reconfigured via command from spacecraft to RTProASIC
- Can change configurations in-flight to support dynamic mission requirements

SpaceCube v3.0 Mini Processor Card

Backplane Connector

SelectMAP

SelectMAP

CMD from Spacecraft

RT ProASIC3

WDT

RST

Kintex UltraScale

NAND Flash (128 Gbit)

NAND Flash (128 Gbit)

# SCv3.0 Mini Fault-Tolerant Architecture

Stand-Alone Operation (RT-ProASIC)

- Scrubs Kintex configuration during operation via either:
  - Blind scrubbing (consistent time interval)
  - Smart scrubbing (readback scrubbing to check configuration and correct errors as they are detected)
- Scrubs configuration files in NAND flash memory

SpaceCube v3.0 Mini Processor Card
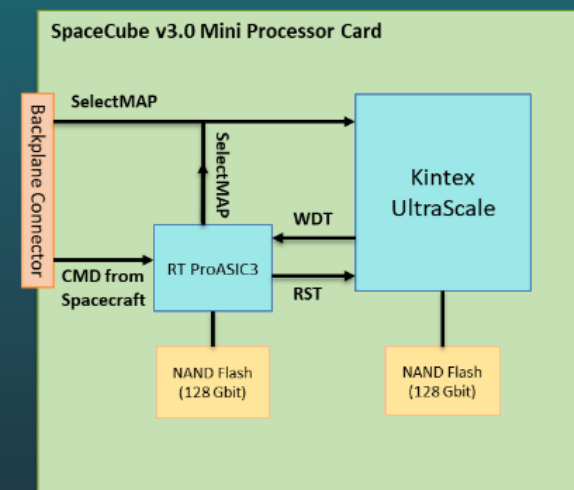
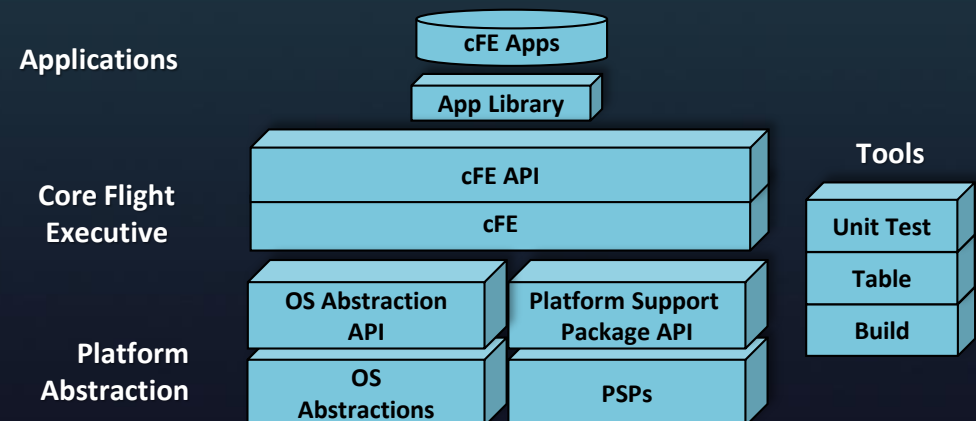## Companion-Card Operation (GSFC CubeSat Bus)

- Combines reliability of RTG4 with high performance of SCv3Mini to form flexible, reusable SmallSat/CubeSat bus
- RTG4 configures and monitors Mini over the backplane
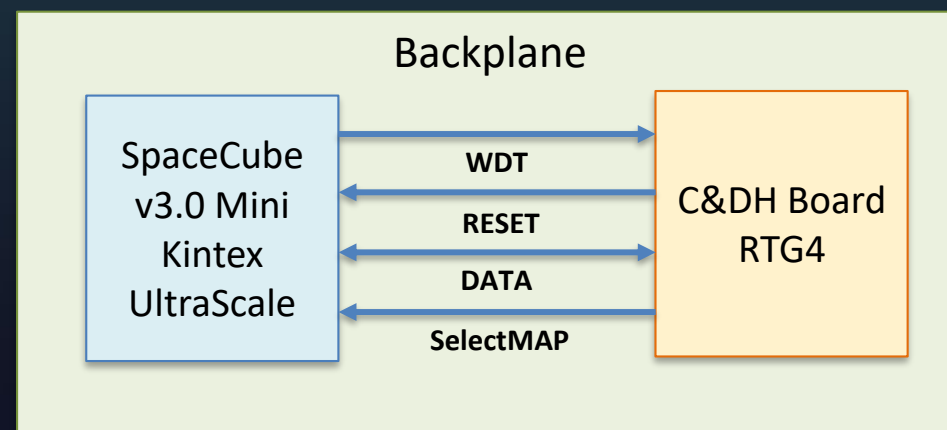
SOFTWARE AND DEPLOYMENT EXAMPLES

Core Flight System (cFS) Overview

- SpaceCube includes software packages supporting cFS
- cFS is NASA **multi-center** configuration controlled **open source** flight software **framework**
  - Layered architecture with standards-based interfaces
  - Provides development tools and runtime environment for user applications
  - Reusable Class A lifecycle artifacts: requirements, design, code, tests, and documents
- Framework is ported to platforms and augmented with applications to create **cFS distributions**
  - Highly reliable software with more than decade of flight heritage
  - **Worldwide community** from government, industry, and academia

Applications	cFE Apps / App Library
Core Flight Executive	cFE API / cFE
Platform Abstraction	OS Abstraction API / Platform Support Package API / OS Abstractions / PSPs
Tools	Unit Test / Table / Build

Benefits of cFS

- **Portable**: Write once, **run anywhere** cFS framework has been deployed
  - Framework has been ported to many popular hardware platform/operating system platforms including MUSTANG, SpaceCube, and CSPv1
- **Open Source**: **15** Goddard apps released as open source that provide common command and data handling
  - Stored command management and execution
  - Onboard data storage file management
- **Lowers Risk**: Reduces project cost and schedule risks
  - High quality **flight heritage applications**
  - Focus resources on mission-specific functionality
- Framework provides seamless application transition from technology demonstration efforts to flight projects
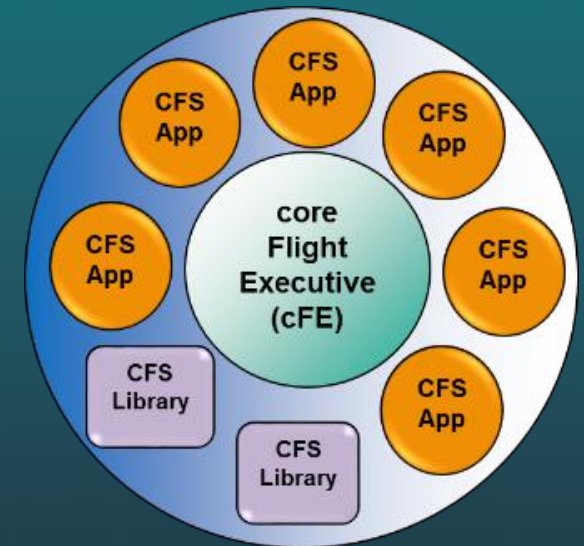
cFS Integration

- SpaceCube v2.0 is currently flying with cFE 6.4 with the Linux OSAL
  - Many open source applications have been used on the SpaceCube (including SC, SCH, LC, HK, HS, FM)
- Platform support packages exist for SpaceCube v2.0 and SpaceCube Mini
  - cFS applications exist to control the SpaceCube Mini Aeroflex, SpaceCube v2.0 Aeroflex, SpaceCube v2.0 Analog Card

SpaceCube v3.0 Mini - NASA Goddard Space Flight Center – July 2019
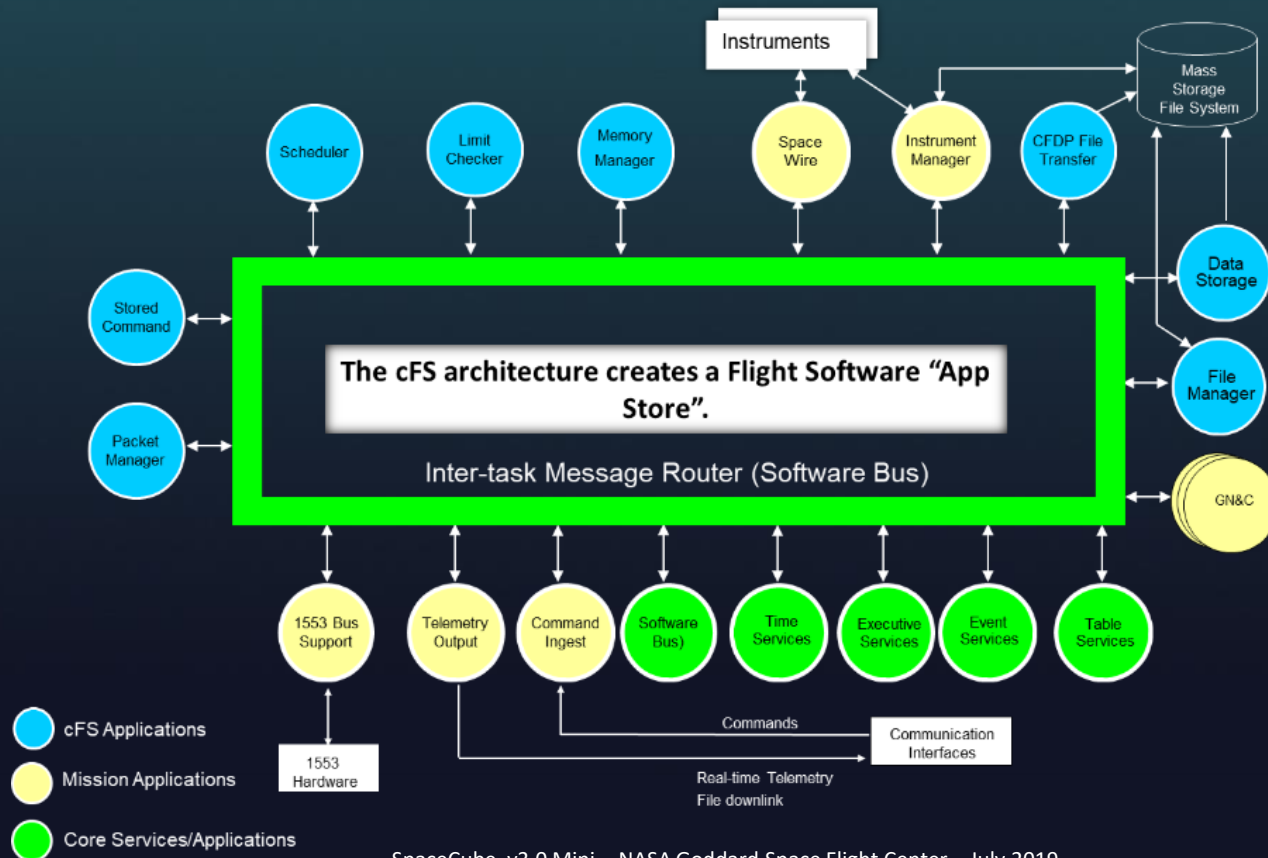
SpaceCube Development Kit

SpaceCube provides software packages for mission development

SpaceCube includes support for several popular OS (Linux, RTEMS, FreeRTOS) and allows for end-to-end flatsat testing with ground station software such as Ball Aerospace's COSMOS and NASA's IRC

Deployment Configurations

- Small form factor makes SpaceCube Mini **versatile** for many use cases and multiple mission classes

Instrument Processing Unit
- Provides high-speed interface to instruments supporting 12 Multi-Gigabit Transceivers and over 70 LVDS pairs
- Convenient small enclosure for tight integration

High-Performance Processor
- Featured as the high-performance processor on NASA GSFC's highly reliable CubeSat Bus DellingrX
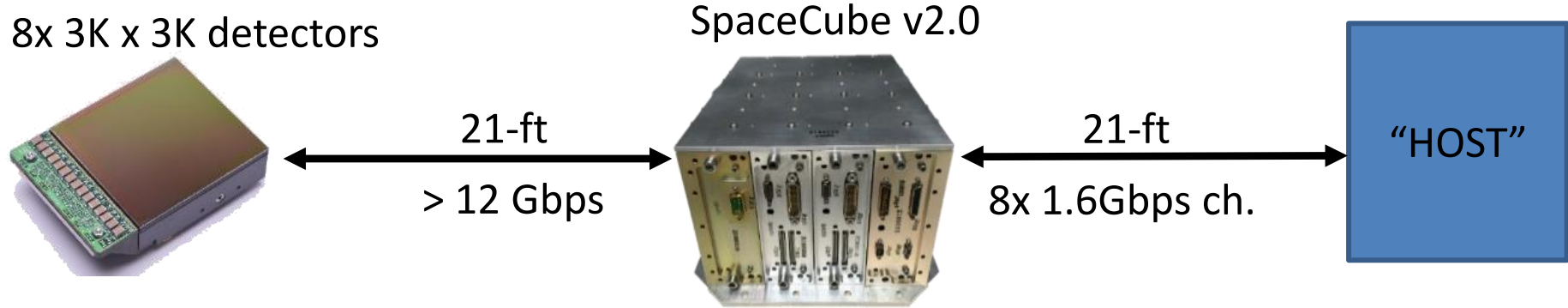- Supports latest Xilinx FPGA development tools including high-level synthesis, reVISION, and Partial Reconfiguration

AI "Edge Node" System
- Can combine SCv3.0 Mini with Mini-Z or Mini-Z45 to provide on-board autonomy and analysis dedicated co-processing node
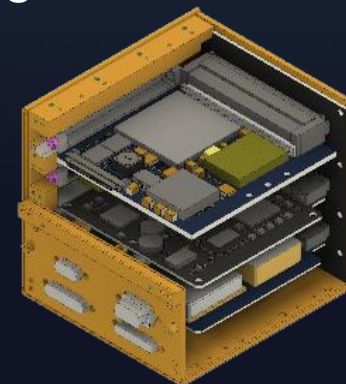
NEODaC Instrument Example

8x 3K x 3K detectors

SpaceCube v2.0

21-ft
> 12 Gbps

21-ft
8x 1.6Gbps ch.

"HOST"

- Near Earth Objects Detection and Characterization (**NEODaC**)

- SerDes output drivers over **21-ft**

- SpaceCube FPGAs being used to interface with detectors, host on-board data processing and compression

- Successful multi-detector readout with SpaceCube completed during TVAC

- SpaceCube Mini can be used in similar role, but supporting **faster rates**

Xilinx GTX Driver: 1.6Gbps
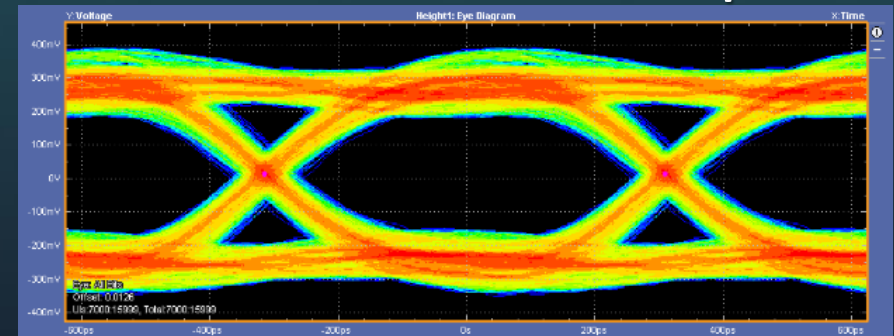
SerDes Link Test Results

Transmitter Swing (mV)	Transmitter % Pre-emphasis	Test Duration	Bit Error Count	BER (*)
500	0	6hr	32	9.2E-13
500	8	18hr	0	9.6E-15
800	0	4hr	4	1.7E-13
800	25	20hr	0	8.7E-15
1300	17	20hr	0	8.7E-15
1300	0	19hr	52	4.7E-13

- *Note: BER calculation assumes at least 1 error*
- *58-hours of error-free transmission*

32

AI "Edge Node" System

## Artificial intelligence co-processors for on-board autonomy or analysis

- Run machine-learning models on flight-qualified single-board computers networked together for fault tolerance, flexibility, and performance
- Currently deep learning models and applications rely on HPC resources like GPUs not broadly for spaceflight
- State-of-the-art radiation-hardened computers are **unable** to run modern neural networks
- Published research for running deep learning models on flight systems

SpaceCube AI Co-Processor

- SpaceCube v3.0 Mini combined with SpaceCube Mini-Z or Mini-Z45
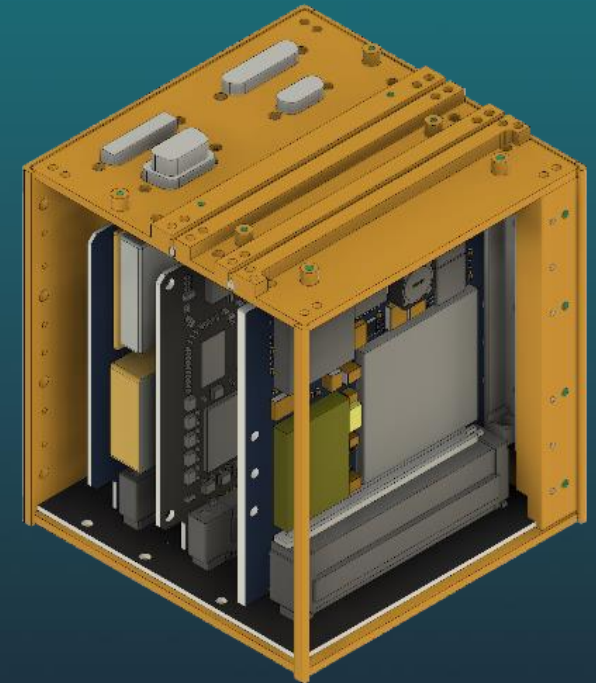
AI Co-Processor 1U Box
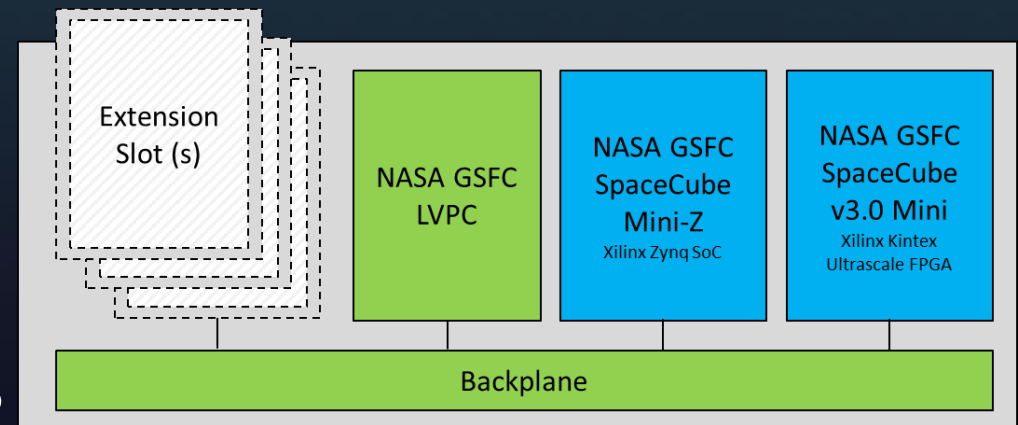
Expandable Design

Advanced Applications Example: Semantic Segmentation

- ## Computer Vision / Machine Learning Process
  - Learns to assign label to all pixels of image
  - Pixels with same label share semantic characteristics
  - Output roughly resembles input

- ## Space Applications
  - **Science**: Earth observations and remote sensing
  - **Defense**: reconnaissance and intelligence gathering

S. Sabogal, A. D. George, and G. Crum, "ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs," 12th Space Computing Conference, July 30 – August 1, 2019.

	Roads		Low Vegetation		Automobiles
	Buildings		Trees		Clutter

SpaceCube for Advanced Applications

Resource-Intensive Applications

- Advanced deep-learning algorithms, such as semantic segmentation, are computationally expensive and prohibitive on traditional rad-hard processors

ReCoN (Reconfigurable CNN accelerator)

- ReCoN is designed for scalability and parameterization of CNNs and used for semantic segmentation demonstration
- Generated using Vivado High Level Synthesis (**HLS**)
- Parallel computations are scalable, and certain accelerator sizes **can only be supported on larger devices** such as the Kintex UltraScale in SpaceCube Mini
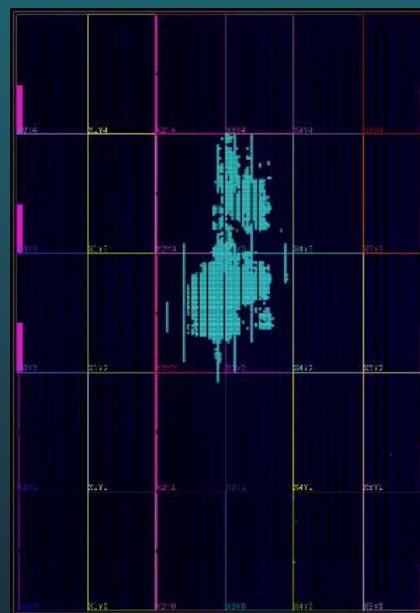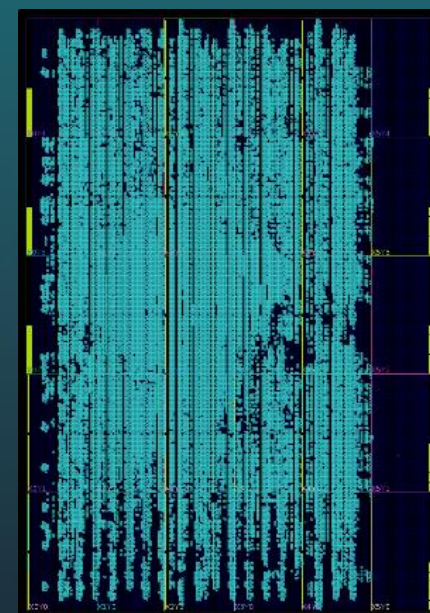
MicroBlaze   ReCoN Accelerator

Resource Utilization of TMR Designs on KU060

Resource	MicroBlaze Stand Alone Reference	ReCoN$_{16}$
LUTs	2.41%	18.85%
CLB FF	1.19%	21.61%
BRAM/FIFO ECC (36 Kb)	6.94%	6.11%
DSP Slices	0.22%	84.64%

SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus Dellingr-X
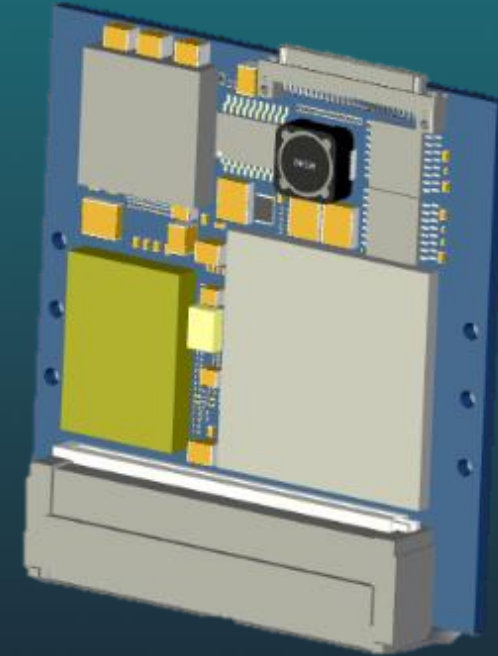
High-Level Specifications

1x Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 30x 3.3V GPIO
  - 2 RS-422/LVDS
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG

91.54

88.00

85 Nano

Kintex UltraScale KU060

SEARAY Connector (400 pin)

RTProASIC3 Supervisor

CREDIT CARD

4768 0989 8978 2378

VALID 07/2014   EXP 08/2020

36

SpaceCube Mini-Z45 Specification

Overview

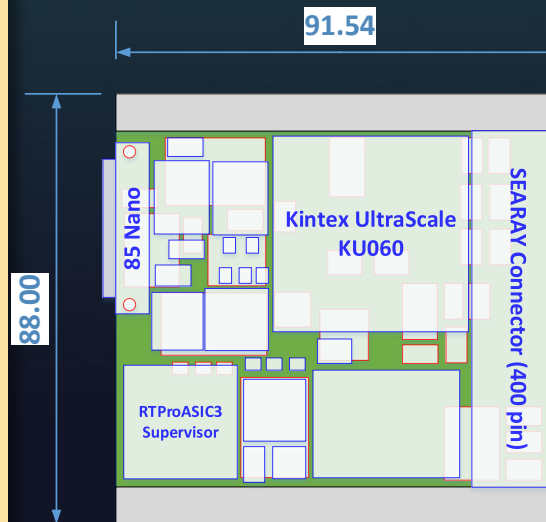- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory
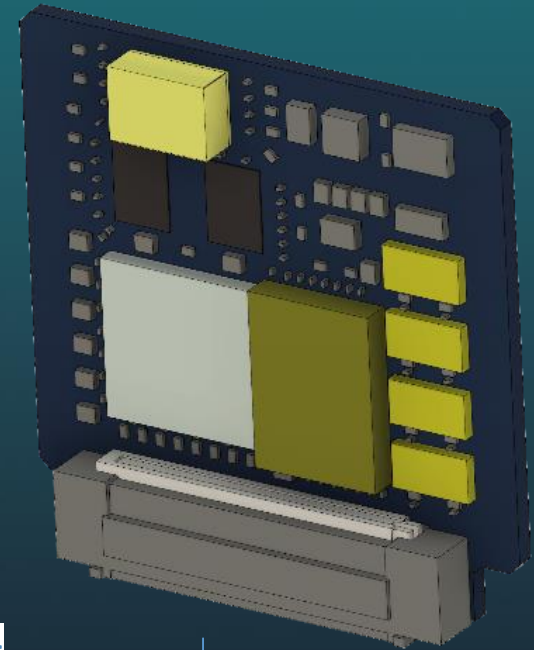
High-Level Specifications

1x Xilinx Zynq 7000 System-on-Chip

- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (Voltage Selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG

91.54

88.00

SEARAY Connector (400 pin)

Zynq 7000

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- Prototype demonstration 9/19
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Space Computer (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot

SpaceCube v3.0 Architecture

High-Level Specifications

1x Xilinx Kintex UltraScale

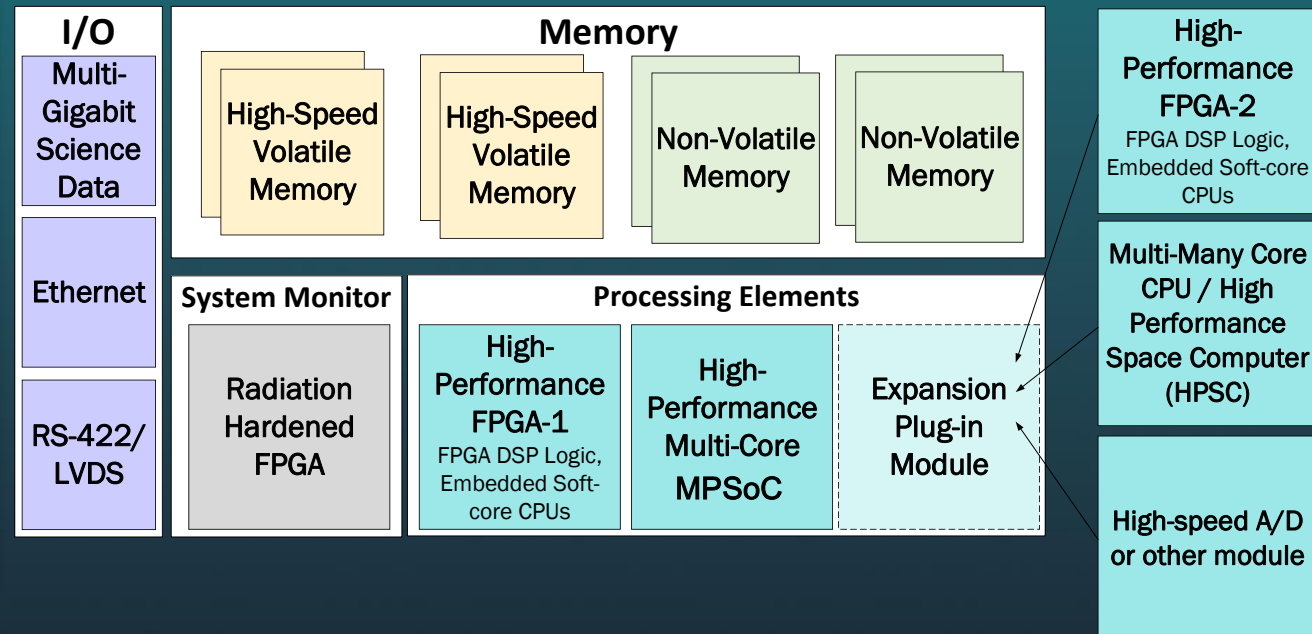- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 82x LVDS pairs or 164x 1.8V single-ended I/O
  - 30x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces:
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces:
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring

SpaceCube "Spin-offs" and Technology Infusion

SpaceCube designs have expanded to support variety of missions and projects

9 Mission-Unique SpaceCube I/O Cards in various stages of integration and test

- SSCO Video Distribution Unit
- GRSSLi (Code 590)
- NavCube (Code 590)
- GEDI Digitizer design
- Complex PWB design using 1mm pitch CCGAs
  - TESS, GEDI, Mustang, OSIRIS-REx
- Proposal development
  - CycloPPS (Code 550 and Code 600)
  - DTN (Code 450)
  - DFB (Code 600)
  - Various others
- NICER/GEDI Ethernet Circuitry
- NSF CHREC Space Processor
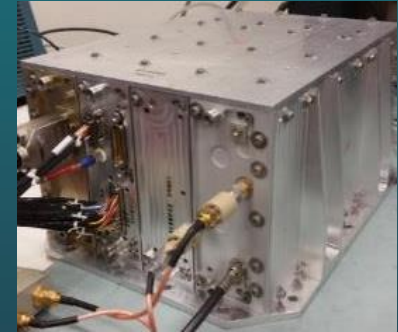
"NavCube"
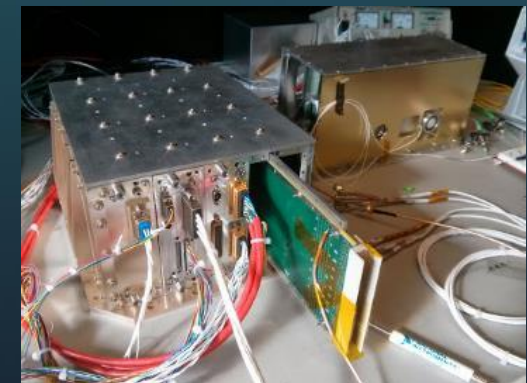
GRSSLi Lidar
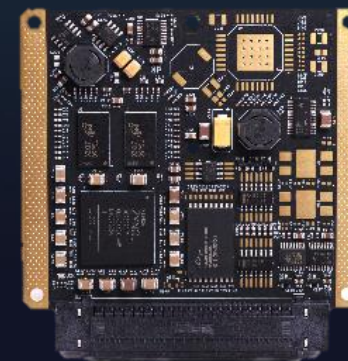
Conclusion

SpaceCube is a MISSION ENABLING technology

- Delivers exceptional computing power in number of form factors

- Cross-cutting technology for Comm/Nav, Earth and Space Science, Planetary, and Exploration missions

- Being reconfigurable equals BIG SAVINGS

- Past research / missions have proven viability

- Designs support AI applications for autonomy and analysis onboard

- Successful technology transfer to industry through commercialization

SpaceCube Publications

- A. Geist, C. Brewer, M. Davis, N. Franconi, S. Heyward, T. Wise G. Crum, D. Petrick, R. Ripley, C. Wilson, and T. Flatley, "SpaceCube v3.0 NASA Next-Generation High-Performance Processor for Science Applications," 33rd Annual AIAA/USU Conf. on Small Satellites, SSC19-XII-02, Logan, UT, August 3-8, 2019.

- A. Schmidt, M. French, and T. Flatley, "Radiation hardening by software techniques on FPGAs: Flight experiment evaluation and results," IEEE Aerospace Conference, Big Sky, MT, March 4-11, 2017.

- A. Schmidt, G. Weisz, M. French, T. Flatley, C. Villalpando, "SpaceCubeX: A framework for evaluating hybrid multi-core CPU/FPGA/DSP architectures," IEEE Aerospace Conference, Big Sky, MT, March 4-11, 2017.

- D. Petrick, N. Gill, M. Hassouneh R. Stone, L. Winternitz, L. Thomas, M. Davis, P. Sparacino, and T. Flatley, "Adapting the SpaceCube v2.0 data processing system for mission-unique application requirements," IEEE Aerospace Conference, Big Sky, MT, June 15-18, 2015.

- T. Flatley, "Keynote 2 — SpaceCube — A family of reconfigurable hybrid on-board science data processors," International Conference on ReConFigurable Computing and FPGAs (ReConFig14), Cancun, Mexico, Dec 8-10, 2014.

- D. Petrick, A. Geist, D. Albaijes, M. Davis, P. Sparacino, G. Crum, R. Ripley, J. Boblitt, and T. Flatley, "SpaceCube v2.0 space flight hybrid reconfigurable data processing system," IEEE Aerospace Conference, Big Sky, MT, March 1-8, 2014.

- D. Petrick, D. Espinosa, R. Ripley, G. Crum, A. Geist, and T. Flatley, "Adapting the reconfigurable spacecube processing system for multiple mission applications," IEEE Aerospace Conference, Big Sky, MT, March 1-8, 2014.

- T. Flatley, "Keynote address I: SpaceCube: A family of reconfigurable hybrid on-board science data processors," NASA/ESA Conference on Adaptive Hardware and Systems (AHS), June 25-28, 2012.

- M. Lin, T. Flatley, A. Geist, and D. Petrick, "NASA GSFC Development of the SpaceCube Mini," 25th Annual AIAA/USU Conf. on Small Satellites, SSC11-X-11, Logan, UT, August 8-11, 2011.

SmallSat / CubeSat Publications

- J. Manning, E. Gretok, B. Ramesh, C. Wilson, A. D. George, J. MacKinnon, G. Crum, "Machine-Learning Space Applications on SmallSat Platforms with TensorFlow," 32nd Annual AIAA/USU Conference on Small Satellites, SSC18-WKVII-03, Logan, UT, Aug 4-9, 2018.

- S. Sabogal, P. Gauvin, B. Shea, D. Sabogal, A. Gillette, C. Wilson, A. D. George, G. Crum, and T. Flatley, "Spacecraft Supercomputing Experiment for STP-H6," 31st Annual AIAA/USU Conf. on Small Satellites, SSC17-XIII-02, Logan, UT, Aug 5-10, 2017.

- C. Wilson, J. MacKinnon, P. Gauvin, S. Sabogal, A. D. George, G. Crum, T. Flatley, "µCSP: A Diminutive, Hybrid, Space Processor for Smart Modules and CubeSats," 30th Annual AIAA/USU Conf. on Small Satellites, SSC16-X-4, Logan, UT, August 6-11, 2016.

- C. Wilson, J. Stewart, P. Gauvin, J. MacKinnon, J. Coole, J. Urriste, A. D. George, G. Crum, A. Wilson, and M. Wirthlin, "CSP Hybrid Space Computing for STP-H5/ISEM on ISS," 29th Annual AIAA/USU Conf. on Small Satellites, SSC15-III-10, Logan, UT, August 8-13, 2015.

- B. LaMeres, S. Harkness, M. Handley, P. Moholt, C. Julien, T. Kaiser, D. Klumpar, K. Mashburn, L. Springer, G. Crum, "RadSat – Radiation Tolerant SmallSat Computer System, "29th Annual AIAA/USU Conf. on Small Satellites, SSC15-X-8, Logan, UT, August 8-13, 2015.

- S. Altunc, O. Kegege, S. Bundick, H. Shaw, S. Schaire, G. Bussey, G. Crum, J. Burke, S. Palo, D. O'Conor, "X-band CubeSat Communication System Demonstration," 29th Annual AIAA/USU Conf. on Small Satellites, SSC15-IV-8, Logan, UT, August 8-13, 2015

- D. Rudolph, C. Wilson, J. Stewart, P. Gauvin, G. Crum, A. D. George, M. Wirthlin, H. Lam, "CSP: A Multifaceted Hybrid System for Space Computing," Proc. of 28th Annual AIAA/USU Conference on Small Satellites, SSC14-III-3, Logan, UT, August 2-7, 2014.

- S. Palo, D. O'Connor, E. DeVito, R. Kohnert, G. Crum, S. Altune, "Expanding CubeSat Capabilities with a Low Cost Transceiver," Proc. of 28th Annual AIAA/USU Conference on Small Satellites, SSC14-IX-1, Logan, UT, August 2-7, 2014.

Thank you! Questions?

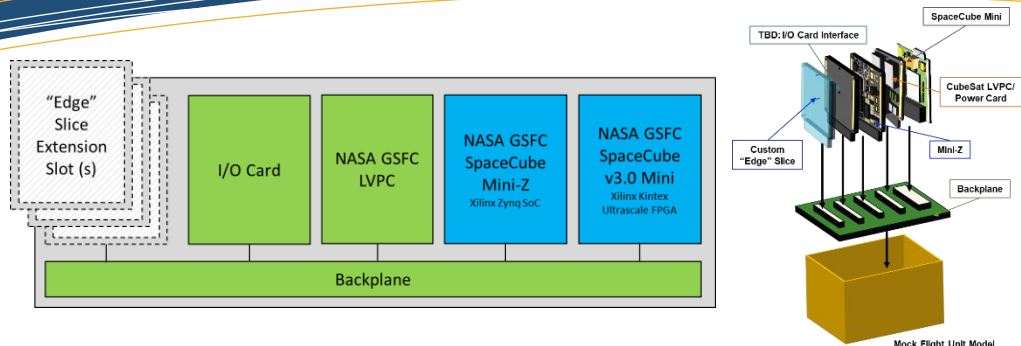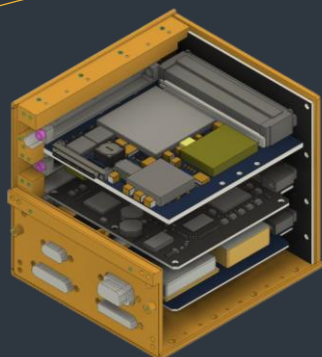alessandro.d.geist@nasa.gov

spacecube.nasa.gov

Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)

Icons courtesy https://www.flaticon.com/packs/marketing-management-2

SpaceCube v3.0 Mini - NASA Goddard Space Flight Center – July 2019

Artificial Intelligence CubeSat Co-Processor

Experimental ISS Testbed in CubeSat Form-Factor

Mock Flight Unit Model

The ISS Artificial Intelligence (AI) and Machine Learning (ML) CubeSat Co-Processor baseline system features the NASA Goddard SpaceCube v3.0 Mini (Kintex UltraScale FPGA), the NASA Goddard SpaceCube Mini-Z (Zynq SoC), the GSFC Low Voltage Power Converter, and customizable I/O card to support mission and instrument unique interfaces. The backplane is extendable for "Edge" processor slices which can feature the Cubic Aerospace Edge Processor (NVIDIA TK1 CPU/GPU SoC), Lucid Circuit Astrum (AI Microchip), or Intel Movidius Myriad X (VPU). Combined with a high-resolution imager, dynamic vision sensor, or other state-of-the-art instruments, this platform would be able to act as an in-flight AI processing unit to execute new AI algorithms in a space environment.

Baseline Specification

Processing

• Processing System (PS)	Dual-Core ARM-Cortex A9
	• L1 Cache 32KB I / D per core, L2 Cache 512 KB, on-chip Memory 256KB
	• Up to 667 MHz (-1) and 866 MHz (-3)
• Softcore MicroBlaze(s)	3 Preset Configurations
	• Microcontroller (400 MHz / 540 DMIPS)
	• Real-Time Processor (302 MHz / 405 DMIPS)
	• Application Processor (256 MHz / 232 DMIPS)
• FPGA Programmable Logic	811K (726K + 85K) System Logic Cells
	42.9Mb (38 Mb + 4.9 Mb) Block RAM
	2,980 (2,760 + 220) DSP Slices

Supported Interfaces

• External Interfaces	12x Multi-Gigabit Transceivers
	48x LVDS pairs or 96x 1.8V single-ended I/O
	24x LVDS pairs or 48x 1.8V, 2.5V, or 3.3V single-ended I/O
	30x 3.3V GPIO
	12x 1.8V, 2.5V, or 3.3V GPIO
	2x RS-422/LVDS
	1x SpaceWire Port
	I2C/CAN/GigE/SPIO/GPIO/SPW
• Debug Interfaces	2x RS-422 UART
	JTAG

Memory	2x 16 GB + 1x 4 GB NAND Flash
	1x 2 GB + 1x 1 GB DDR3 SDRAM
Mechanical	CubeSat 1U (105 mm × 95 mm × 170 mm w/ 1 "Edge" slice)
	Up to 2.19 kg (depending on Edge Slice)
Thermal	Conduction cooled
Power Consumption	24.46 W (Baseline), 50 W (K1 Slice), 26 W (Astrum Slice)

*Values presented are notional estimates, baseline configuration does not include additional features of "edge" slices

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New Computing Frontier

GPUs and custom AI devices have vast potential for accelerating applications in the artificial intelligence domain, however, many have not been evaluated for flight (FPGA will serve as baseline/control)

New Mission Enabling

Develop key software functions for adaptive machine learning, multi-point measurements, constellation management, and collaborative satellite ecosystems

Key Scenarios

Demonstrate autonomy, decision making, inter-platform collaboration, detection / identification and tracking

For more information on any of our solutions please visit us on the web at: spacecube.nasa.gov

Science Data Processing Branch

Gary Crum / Embedded Group Lead
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Artificial Intelligence Testbed for ISS

Experimental ISS Testbed To Evaluate AI/ML Technology Platforms

New Computing Frontier

GPUs and custom AI devices have vast potential for accelerating applications in the artificial intelligence domain, however, many have not been evaluated for flight (FPGA will serve as baseline/control)

New Mission Enabling

Develop key software functions for adaptive machine learning, multi-point measurements, constellation management, and collaborative satellite ecosystems

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For more information on any of our solutions please visit us on the web at: spacecube.nasa.gov

Legend:
- Supporting Cards
- GPU SoC
- AI Microchip
- FPGA
- Enclosure
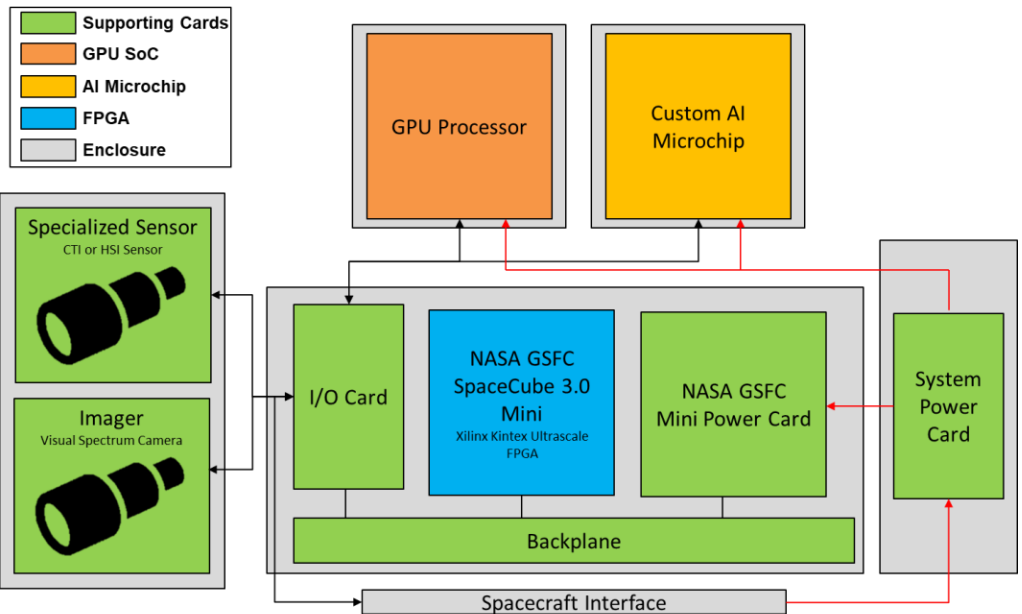
The ISS Artificial Intelligence (AI) and Machine Learning (ML) Testbed features the NASA Goddard SpaceCube v3.0 Mini (Kintex UltraScale FPGA), the Cubic Aerospace Edge Processor (NVIDIA TK1 CPU/GPU SoC), and the Lucid Circuit Astrum (AI Microchip). Combined with a high-resolution imager, the platform would be able to act as an in-flight AI testbed to prototype new algorithms in a space environment.

System Requirements

1. Run the state-of-the-art AI algorithms on all three platforms, and show comparisons in performance, power, and resiliency to radiation effects

2. Provides flight heritage and verification for three technologies that may be included in future NASA solicitations

3. Provide the capability to upload new software applications to use the in-flight experiment time to test additional applications of interest and scenarios. This upload feature would be convenient to make adjustments and modifications to code when investigating autonomy reacting to ground commands (Operator's Intent) and experimental prototyping for conveying decisions (Human-readable, decision-making understanding of AI decisions)
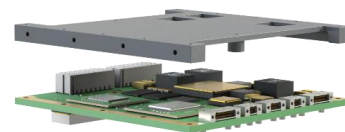
Science Data Processing Branch

Code 587

Tom Flatley / Principal Investigator
thomas.p.flatley@nasa.gov

SpaceCube v3.0 Mini

Next-Generation Data-Processing System for Advanced CubeSat Applications

In order to provide a high-performance processor to perform on-board data analysis, conduct fault mitigation and management, and provide spacecraft autonomy for future missions, the Science Data Processing Branch at NASA GSFC has developed a new CubeSat-sized processor named SpaceCube v3.0 Mini.

CubeSat Form Factor

Apply SpaceCube design approach to provide next-generation processor in CubeSat form factor

SpaceCube Compatibility

Maintains compatibility with main line SpaceCube v3.0

High-performance Processor (HPP)

NASA GSFC's new CubeSat framework is under development as the DellingrX mission, where the SpaceCube v3.0 Mini assumes the role of the high-performance processor

For more information on any of our solutions please visit us on the web at: spacecube.nasa.gov

The SpaceCube family consists of cross-cutting, in-flight reconfigurable hybrid data processing systems. The Mini is another addition to the SpaceCube family, a series of NASA developed space processors that established a hybrid-processing approach combining radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs. Just as its predecessor card the v2.0 Mini, the design methodology for the SpaceCube Mini series leverages the design of the larger processor card in the SpaceCube family, and reduces the core functionality to fit within a CubeSat form-factor design.

In "Achieving Science with CubeSats," the Space Studies Board at the National Academies emphasized that NASA must assign a high priority to develop the capability to implement large-scale constellation missions for multi-point science measurements and expanded spatial and temporal coverage. To enable these types of multi-satellite missions, high-performance onboard computing is necessary to provide autonomous behavior to reduce operations cost, as well as, provide robustness, fault management, and resource conservation of the entire constellation. There are many proposals to apply the benefits of ground-based artificial intelligence (AI) algorithms to space autonomy, however, AI structures are too computationally intensive to run on current CubeSat platforms. To enable the next CubeSat revolution, advanced CubeSat applications and complex formation-flying missions need CubeSat processors to offer higher-performance processing while remaining affordable and highly reliable.
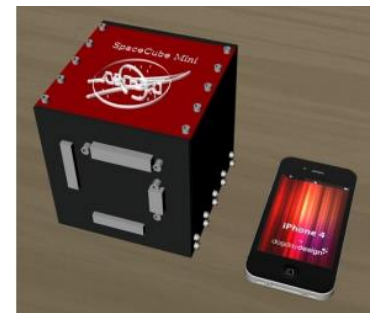
CubeSat Size Comparison to Phone
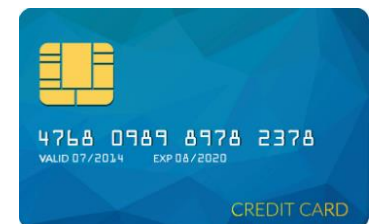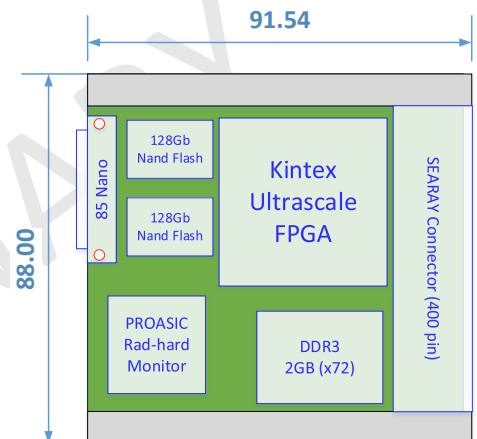
Specification

Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 30x 3.3V GPIO
  - 2x RS-422/LVDS
  - 1x SpaceWire Port
  - SelectMAP
  - (Optional) 24 LVDS pairs or 48x 1.8V single-ended I/O
- Debug Interfaces
  - 2x RS-422 UART
  - JTAG

Science Data
Processing Branch

Code 587

Alessandro Geist / Principal Engineer
alessandro.d.geist@nasa.gov

SpaceCube v3.0 Mini

Next-Generation Data-Processing System for Advanced CubeSat Applications

About SpaceCube v3.0 Mini

The SpaceCube family consists of cross-cutting, in-flight reconfigurable hybrid data processing systems. The Mini is another addition to the SpaceCube family, a series of NASA developed space processors that established a hybrid-processing approach combining radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs. Just as its predecessor card the v2.0 Mini, the design methodology for the SpaceCube Mini series leverages the design of the larger processor card in the SpaceCube family, and reduces the core functionality to fit within a CubeSat form-factor design.

For more information on any of our solutions please visit us on the web at:

spacecube.nasa.gov

Contact Us

Science Data
Processing Branch

Code 587

Alessandro Geist / Principal Engineer
alessandro.d.geist@nasa.gov

This Datasheet is Subject to Change Without Notice

Specifications

Processing		
	Softcore MicroBlaze(s)	3 Preset Configurations
		• Microcontroller (400 MHz / 540 DMIPS)
		• Real-Time Processor (302 MHz / 405 DMIPS)
		• Application Processor (256 MHz / 232 DMIPS)
	FPGA Programmable Logic	100 MHz CLK
		726K System Logic Cells
		9,180 KB Block RAM
		2,760 DSP Slices

Supported Interfaces		
	External Interfaces	12x Multi-Gigabit Transceivers
		48x LVDS pairs or 96x 1.8V single-ended I/O
		30x 3.3V GPIO
		2x RS-422/LVDS
		1x SpaceWire Port
		SelectMAP Interface
		(Front Panel) 24 LVDS pairs or 48x 1.8V single-ended I/O
	Debug Interfaces	2x RS-422 UART
		JTAG

Memory	
	2x 16 GB NAND Flash
	2 GB DDR3 SDRAM

Radiation Performance	TID:	Est. 60+ krads (Si)
	SEE:	TBD Upsets/Day (LEO) TBD (GEO)
		Radiation-Hardened Monitor

Development Tools		
	Mini Evaluation Board*	JTAG programming support
		10/100/1000 Ethernet
		GPIO breakout
		4x SpaceWire breakouts
		2x Camera Link breakout
	Software BSP	Basic SCv3 Mini BSP includes FPGA Cores for all board interfaces, as well as, light-weight Linux supporting CFS

Mechanical	
	1U CubeSat form factor (< 10 cm x 10 cm)
	250 grams max weight
	29mm thickness with populated parts

Thermal	
	Conduction cooled

Power Consumption	
	10-17 Watts
	(Application/Utilization Dependant)

Temperature Ratings†	
	SCv3-EM Operational: 0 to 70 °C
	SCv3-Flight Operational: -35 °C to +85 °C
	SCv3-Flight Survival / Storage: -35 °C to +85 °C

*Mini Eval Board Still In Development
† Pending Finalized BOM

SpaceCube v3.0

Next-Generation High-Performance Processor for Science Applications

Next Generation Design

SpaceCube v3.0 features the latest cutting-edge processing technology for space systems including the new Xilinx Ultrascale and Zynq Ultrascale+

3U SpaceVPX

SpaceCube v3.0 is built around the new industry standard SpaceVPX form factor. This design ensures compatibility with more vendors and reduces costly vendor lock-in.

Expandable

The FMC+ expansion slot is designed to seamlessly integrate new devices with the core processing elements, such as, high-speed ADC/DAC cirucits, GPU's and more!

HPSC Compatible

Ready for the High-Performance Space Computer (HPSC). SpaceCube v3.0 includes high-speed interfaces, power, and thermal solutions to pair the HPSC with our high-performance FPGA's to meet the most extreme performance and relaiabiilty needs.

For more information on any of our solutions please visit us on the web at: spacecube.nasa.gov
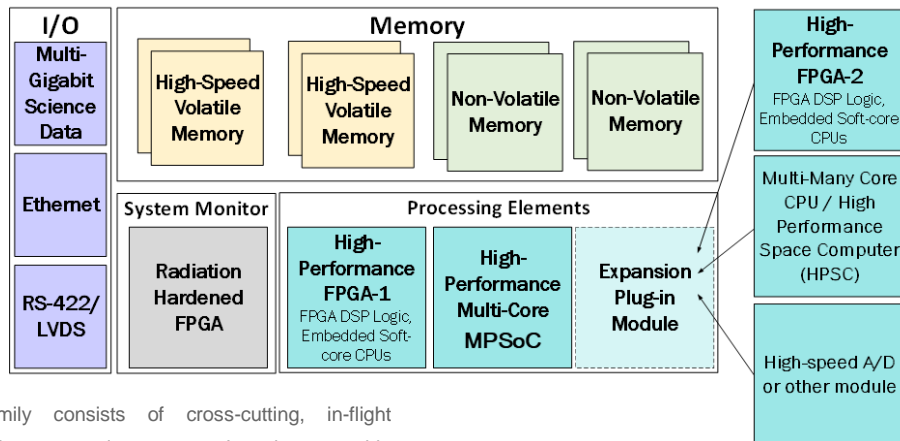
The SpaceCube family consists of cross-cutting, in-flight reconfigurable hybrid data processing systems. In order to provide a robust solution to a variety of missions and instruments, the Science Data Processing Branch at NASA GSFC has pioneered a hybrid-processing approach that combines radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs. This approach provides anywhere from 10x to 100x improvements in on-board computing capability while lowering relative power consuption and cost. The SpaceCube v3.0 is the next generation SpaceCube design and functions as the next evolutionary step for upcoming missions while providing a flexible and mature architecture to adopt HPSC upon release.

Specification

Xilinx Kintex UltraScale

- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
    - 24x Multi-Gigabit Transceivers
    - 82x LVDS pairs or 164x 1.8V single-ended I/O
    - 30x 3.3V single-ended I/O,
    - 4x RS-422/LVDS/SPW
- Debug Interfaces
    - 2x RS-422 UART / JTAG

Xilinx Zynq MPSoC

- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
    - I2C/CAN/GigE/SPIO/GPIO/SPW
    - 12x-16x Multi-Gigabit Transceivers
- Debug Interfaces:
    - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces:
    - SpaceWire
    - 2x 8-channel housekeeping A/D with current monitoring

Mezzanine Card

- FMC+ compatible
- 1.8V, 3.3V, 12V power rails
- Multi-Gigabit interfaces, LVDS, and GPIO

Applications

Real-Time instrument processing

Autonomous Operations / Robotic Servicing

Mission-critical computing

Real-time Event / Feature Detection

Gigabit interfacing

On-board classification

Intelligent data compression

Real-time situational awareness

Data volume reduction

Inter-platform collaboration

High speed data routing

Multi-processor computing

Adaptive processing applications

Science Data / Image Segmentation

Software Degined Radio

Deep Learning / Convolutional Neural Networks

Science Data Processing Branch
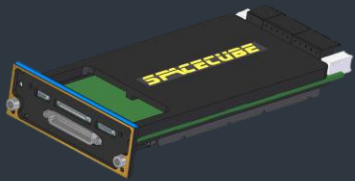
Alessandro Geist / Principal Engineer
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SpaceCube v3.0

Next-Generation High-Performance Processor for Science Applications

About SpaceCube v3.0

The SpaceCube family consists of cross-cutting, in-flight reconfigurable hybrid data processing systems. The v3.0 is the next main design in the SpaceCube family, a series of NASA developed space processors that established a hybrid-processing approach combining radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs.The SpaceCube v3.0 functions as the next evolutionary step for upcoming missions while providing a flexible and mature architecture to adopt HPSC upon release.SpaceCube v3.0 features the latest cutting-edge processing technology for space systems including the new Xilinx Ultrascale and Zynq Ultrascale+

For more information on any of our solutions please visit us on the web at:

spacecube.nasa.gov

Contact Us

Science Data Processing Branch

Code 587

Alessandro Geist / Principal Engineer
alessandro.d.geist@nasa.gov

This Datasheet is Subject to Change Without Notice

Specification

Processing		
	Processing System (PS)	Quad-Core ARM Cortex-A53 Processor (1.3GHz)
		L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB (ECC)
		Dual-Core ARM Cortex-R5 processor (533MHz)
		L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core (ECC)
	Softcore MicroBlaze(s)	3 Preset Configurations
		Microcontroller (400 MHz / 540 DMIPS)
		Real-Time Processor (302 MHz / 405 DMIPS)
		Application Processor (256 MHz / 232 DMIPS)
	FPGA Programmable Logic	1,230K (726K + 504K) System Logic Cells
		49Mb (38 Mb + 11 Mb) Block RAM
		27 Mb UltraRAM
		4,488 (2,760 + 1,728) DSP Slices

Supported Interfaces		
	External Interfaces	36x (24x + 12x) Multi-Gigabit Transceivers
		82x LVDS pairs or 164x 1.8V single-ended I/O
		30x 3.3V GPIO
		4x RS-422/LVDS
		1x SpaceWire Port
		I2C/CAN/GigE/SPIO/GPIO/SPW
		2x 8-ch Housekeeping ADC
	Mezzanine Card	FMC+ Compatible
		1.8V, 3.3V, 12V Power Rails
		24 Multi-Gigabit Transceivers
		58x LVDS pairs or 116x 1.8V single-ended I/O
		20x 3.3V GPIO
		26x Configurable MIO
	Debug Interfaces	4x (2x + 2x) RS-422 UART
		JTAG

Memory	3x 16 GB NAND Flash
	3x 2 GB DDR3 SDRAM

Radiation Performance	TID:	Est. 60+ krads (Si)
	SEE:	TBD Upsets/Day (LEO) TBD (GEO)
Rad-Hard Monitor FPGA		Performs Scrubbing and Power Sequencing

Development Tools		
	Evaluation Card*	JTAG programming support
		10/100/1000 Ethernet
		MIO breakout
		TBD SpaceWire breakouts
		Camera Link breakout
	Software BSP	Basic SCv3 BSP includes FPGA Cores for all board interfaces, as well as, light-weight Linux supporting CFS

Mechanical	SpaceVPX 3U-220
	250 grams max weight
	29 mm thickness with populated parts

Thermal	Conduction cooled

Power Consumption	23-55 Watts

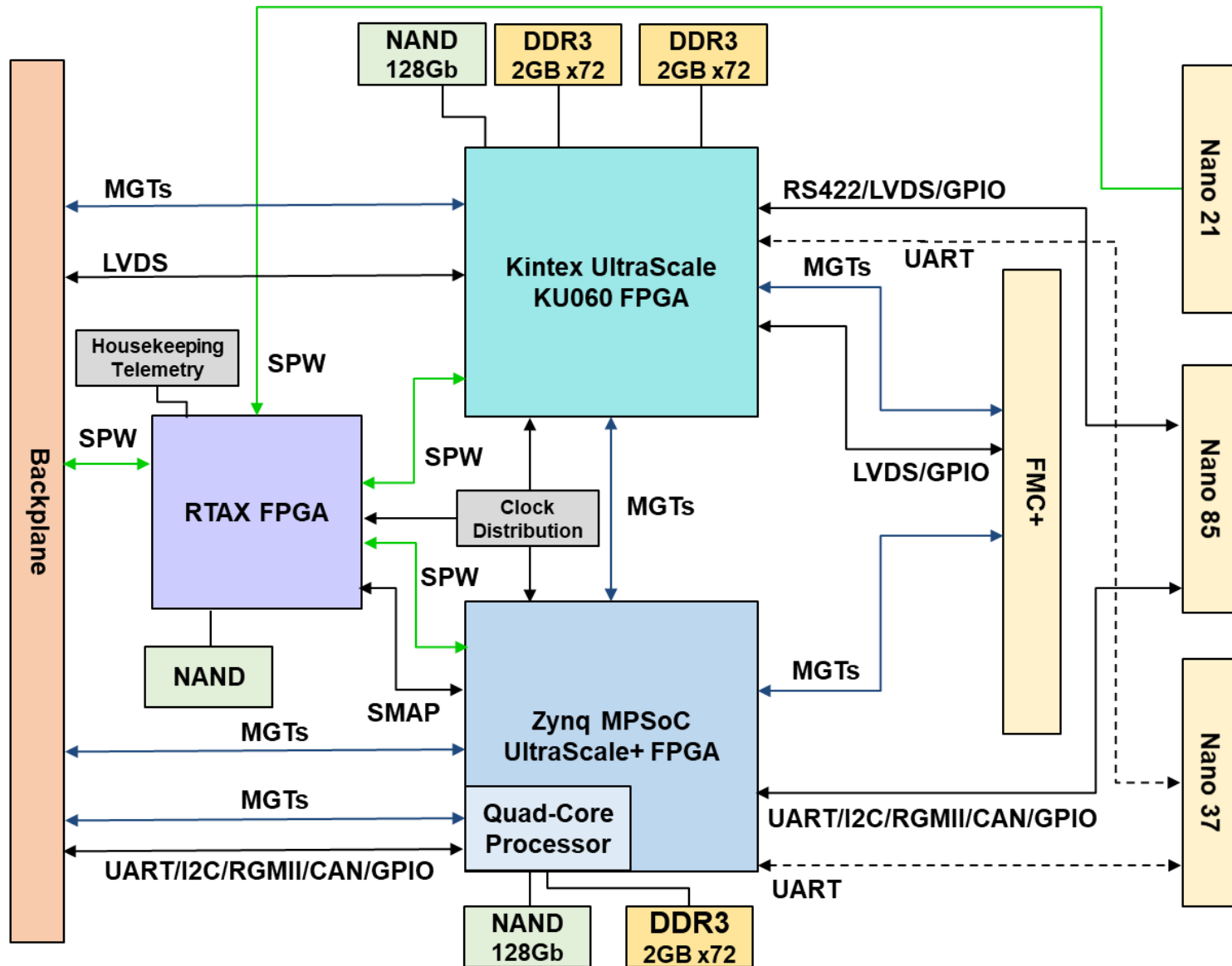| Temperature Ratings†	SCv3-EM Operational: 0 to 70 °C
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PRELIMINARY

SpaceCube v3.0 3U SpaceVPXLite Processor Card

SpaceCube v3.0 Mini (1U CubeSat Form Factor)

Goddard Space Flight Center