SIGNAL SENSING BY THE ARCHITECTURE OF EMBEDDED I/O PAD CIRCUITS

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Abstract- In this study, the detecting structures in an embedded CUP wafer, which are called sensors, are investigated through a contactless sensing analysis. These novel sensing structures, which were designed using the ADS 2009 platform and the design rules for the TSMC 0.18-μm CMOS process, were placed under bonding pads. However, signals would still pass through these I/O sensing structures (i.e., ESD devices or circuits) and become coupled up to the pads of the top-layer metal as square, sinusoidal, or ESD pulse waveforms are injected. Through the resulting sensing relationship, we could then judge whether or not the bottom circuit is a good candidate for EMI consideration. Eventually, it was found that during an ESD occurred situation, a strong signal coupling can be sensed by the ESD protection circuits, especially by gate-coupled ESD protection circuitry.

Index terms: Circuit under pad (CUP), electrostatic discharge (ESD), electromagnetic interference (EMI), gate-coupled circuit, gate-grounded nMOS (GGnMOS), human-body model (HBM).

I. INTRODUCTION

The integration scale and performance of ULSI are continuously improving, allowing for miniaturization through the addition of more transistors to a silicon chip. As a result, circuit designs are becoming significantly more dense and complicated. Nevertheless, as more than 100 million gate counts per die are now required for the 750 to 1000 pads in the input/output (I/O) and power/ground ports [1], The layout area occupied by these bonding pads in a chip is getting larger. Therefore, a more effective shrunken pad-part area in a chip would provide an interesting solution. Furthermore, by using such a bond-pad area, ESD protection circuitry or other circuitry can be arranged under these bonding pads. This pad structure, which is called "circuit-under pad; CUP", have been investigated in some previous technical studies [2-5]. However, they must still maintain good wire bond reliability [6-10]. In contrast, in the 0.5-μm 5-V/18-V design rules of UMC-Fab [11], the authors indicated that only using the top-layer metal as a pad metal that is connected to the circuits through vias is legitimated, while a non-top-layer metal underneath the pad window is not allowed. Given these contrasting reports, interested designers will understandably be interested to know which view is accurate.

As shown in Table 1, over time the pad size has become smaller and smaller, and the pitch-to-pitch space has become closer. When a pad dimension cannot be shrunk any further, the next option is to consider the area beneath a pad for further reductions. Unfortunately, the electrical influence of any changes must be considered carefully under a CUP situation. Therefore, some signals pass through circuit under a pad area, and the influences on the top metal will be shown in this work.

Table 1: Trends of a pad dimension

Roadmap	2005	2007	2009	2011	2013	2015
Pad Size X∗Y (μm^2)	35×65	30×55	25×45	25×45	20×35	15×25
Pad Pitch (μm)	40~100	40~100	30~80	30~60	30~60	30~60

II. EXPERIMENTAL DETAILS

2.1 Device structures designed by the ADS

The geometric dimensions of a bonding pad can be determined using the Momentum toolkit (for schematics and layouts) of the ADS (Advanced Design System) 2009 platform [12]. Therefore, by using the ADS, we can obtain the signal relationship between a CUP and a top-layer metal as an input signal is injected, which is similar to what occurs in capacitor-sensor detection [13, 14].

First, we defined the pad sizes and some required parameters according to the TSMC 0.18-um design rules (Table 2). The pad sizes were set to be 96-μm×96-μm, 65-μm×75-μm, and 66-μm×53-μm, respectively. The second subject was defined as the sheet resistance for each material layer. In this work, a SiO_2 layer was placed between metal-1(M1) and the next layer of metal, metal-2(M2). In addition, the metal and substrate were the common aluminum and silicon materials, respectively.

A CUP pad and corresponding layer locations as determined by the ADS layout are defined and shown in Fig. 1. According to some previous studies [6, 8, 9], a top-layer metal should be able to pass shear and pull testing, and a minimum thickness for this metal layer is required. Accordingly, the thickness of any metal layer in this work was set to be 5-μm.

Table 2: The sheet resistance of different materials

	Si	Al	SiO_2
96 μm×96 μm	10 Ω/sq.	0.02 Ω/sq.	100 MΩ/sq.
75 μm×65 μm	10 Ω/sq.	0.02 Ω/sq.	100 MΩ/sq.
66 μm×53 μm	10 Ω/sq.	0.02 Ω/sq.	100 MΩ/sq.

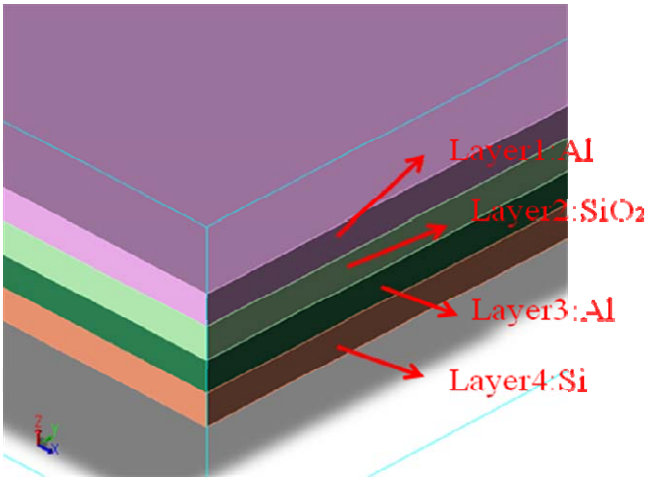


Figure 1. Layers composition of a bonding pad by the ADS layout

2.2 Pulse triggering emulations

As shown in Fig. 2(a), the external square excited waveform was similar to an output signal from a transmission-line pulse (TLP) tester [15, 16], and the V_{peak}, frequency, and pulse width are defined as 1V, 0.5-MHz, and 100-ns, respectively. Secondly, as shown in Fig. 2(b), the amplitude of a sinusoidal signal was set as 1-V and the frequency was set as 100-MHz, which is similar to a normal input signal. In Fig. 2(c), the third image shows a piece-wise linear (PWL) waveform, for which the rising time was set to be 10-ns, the amplitude was set at 2-kV, and the voltage for a falling time of 160-ns was set at 736-V; this waveform is similar to a human-body model (HBM) pulse [17]. Meanwhile, in the real HBM evaluation test, a Keytek Zapmaster machine was used. These three waveforms were injected into a MOS, a gate-grounded nMOS (GGnMOS) [18, 19], or gate-coupled circuit [20, 21] as shown in Fig. 3(a), 3(b), and 3(c), respectively. Because each I/O pad and power pad need to have an ESD protection device or circuit [22-24], these units may be used in an embedded CUP structure.

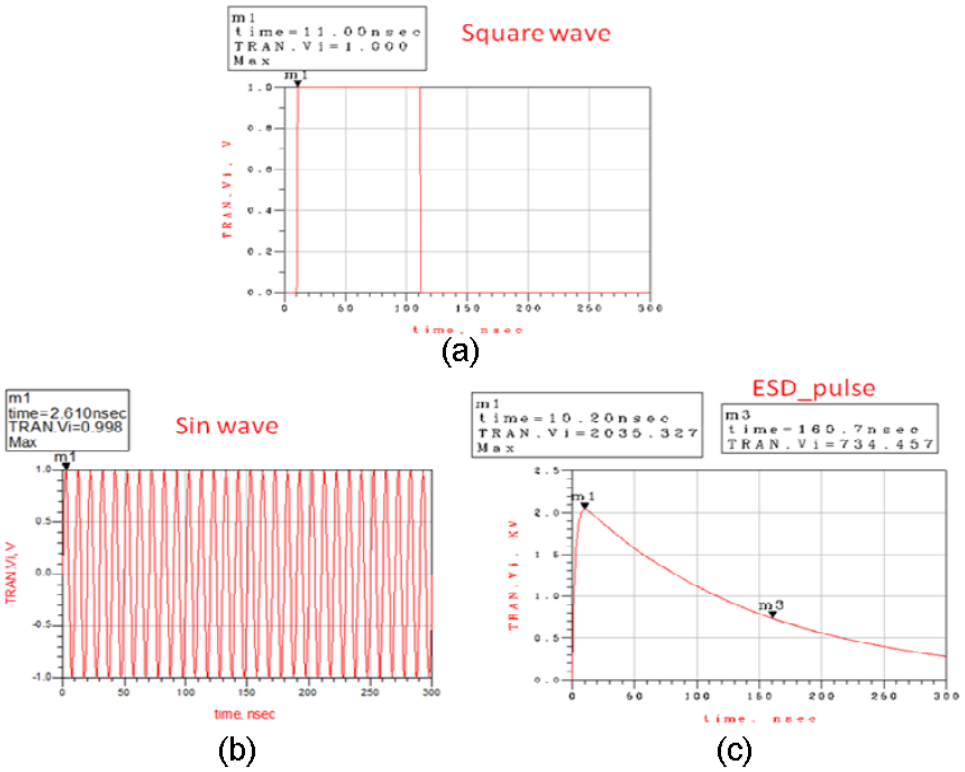
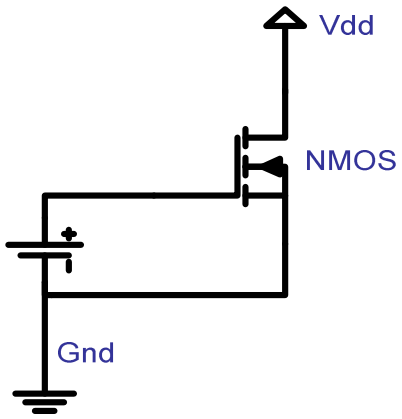
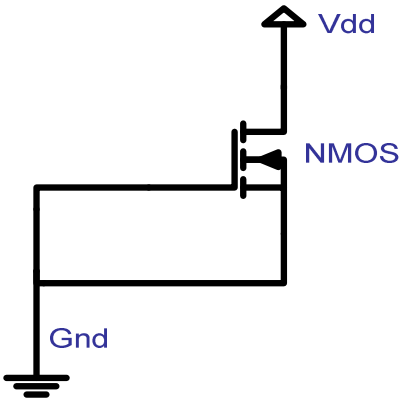


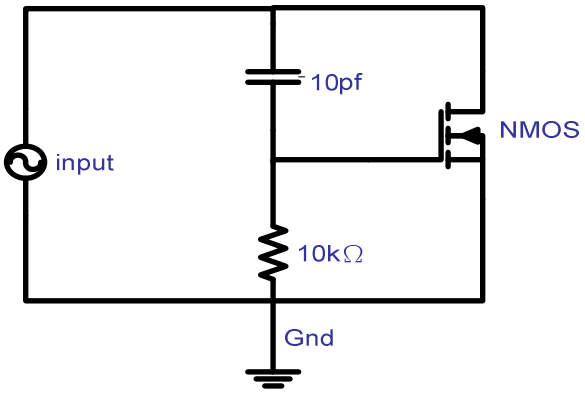
Figure 2. Some emulation waveforms for an embedded CUP structure



(a). MOS



(b). GGnMOS



(c). Gate-coupled circuit

Figure 3. An ESD protection unit with an (a)MOSFET, (b)GGnMOS, or (c)gate-coupled circuit

III. EXPERIMENTAL RESULTS AND DISCUSSION

Each external signal that flowed through the MOS, GGnMOS, or gate-coupled circuit would pass through the bottom metal and couple up to the top grounded terminal, as shown in Figs. 4~6, respectively. Thereafter, the signal in the coupled top metal was monitored and analyzed.

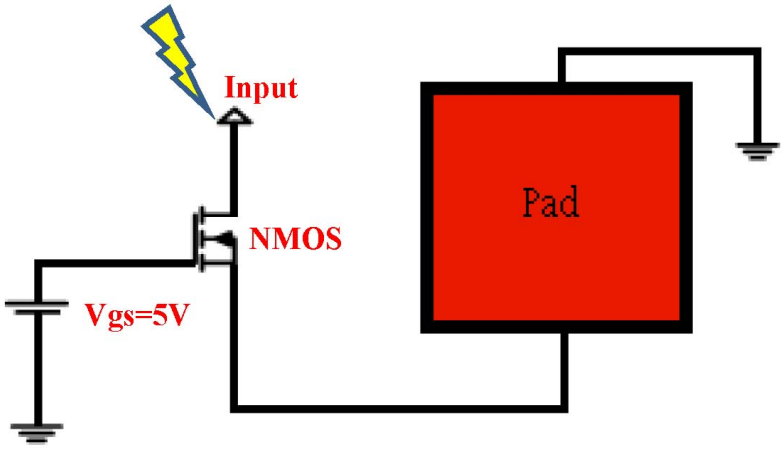


Figure 4. The signal sensing structure with an nMOS device

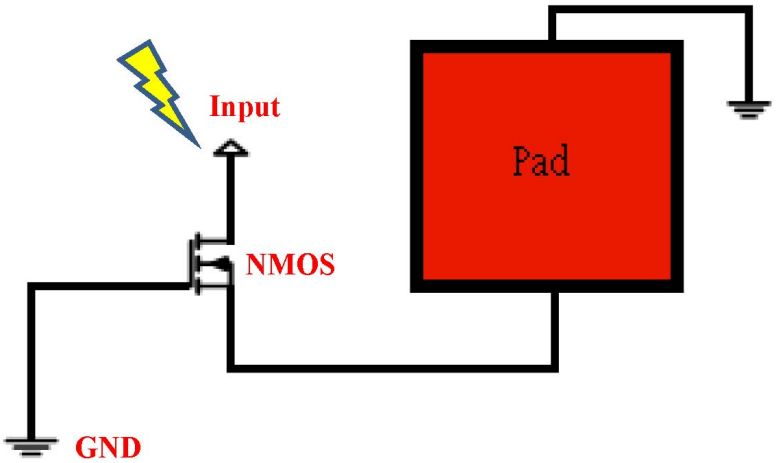


Figure 5. The signal sensing structure with a GGnMOS device

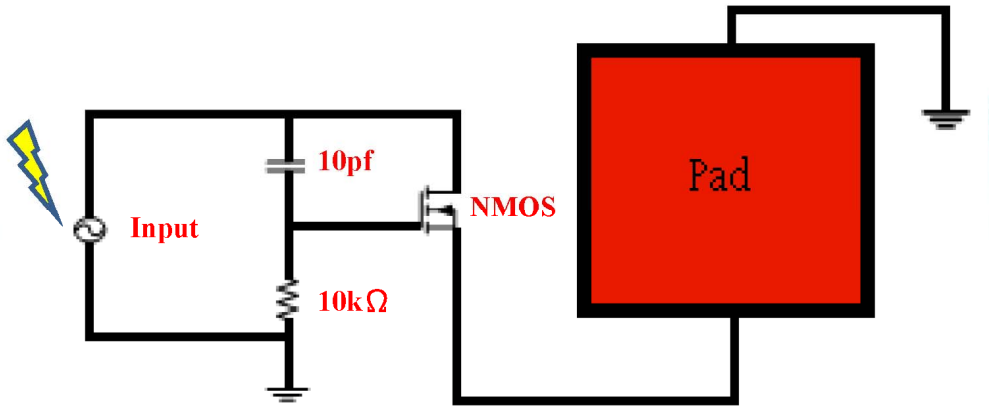
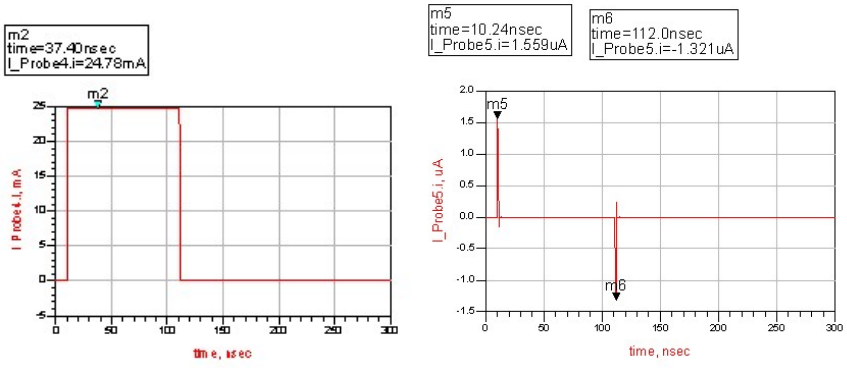
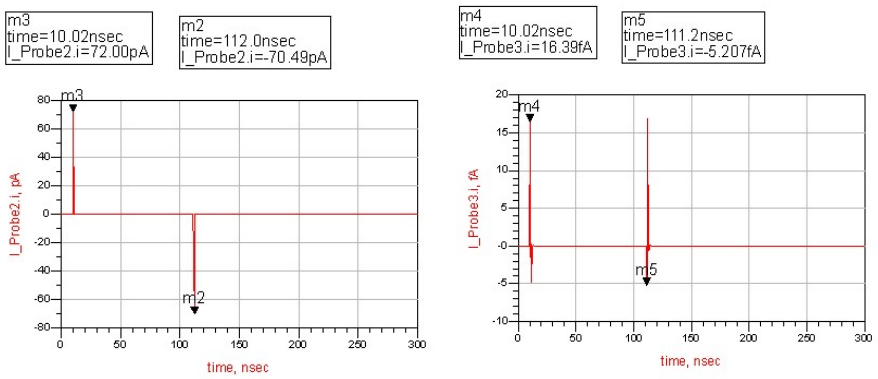


Figure 6. The signal sensing structure with a gate-coupled circuit

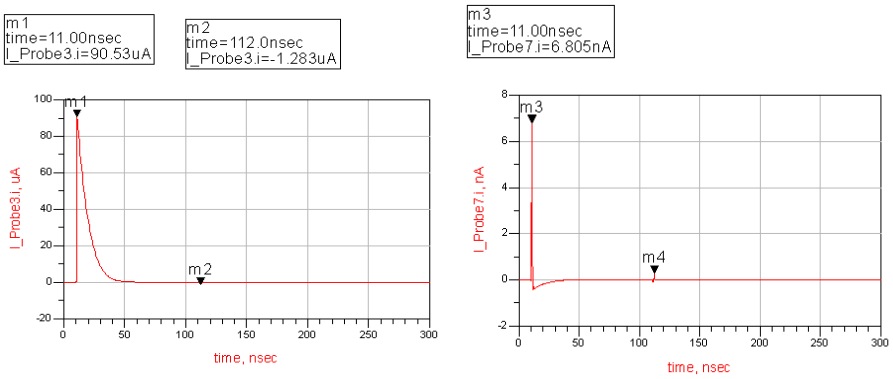
As shown on the left-hand side of Fig. 7(a), when a square pulse was fed into an MOSFET ESD element, due to the function of this pad being similar to a capacitance, the MOS turned-on phenomenon could be detected on the top metal (shown on the right-hand side of Fig. 7(a)). Similar activity occurred as a square waveform flowed into the GGnMOS, because a GGnMOS device is identical to an open device, so that the coupled signal of a GGnMOS is shown on the right-hand side of Fig. 7(b). Finally, the input signal and coupled signal of the top-metal as a square waveform was fed into a gate-coupled circuit are shown on the left-hand and right-hand sides of Fig. 7(c), respectively.



(a) MOS



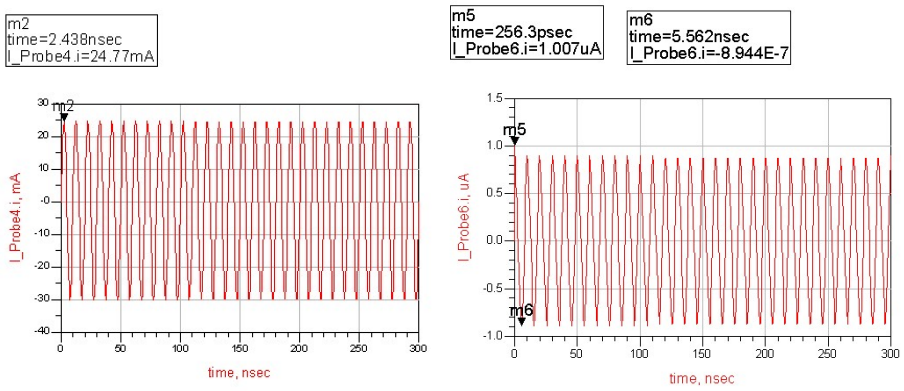
(b) GGnMOS



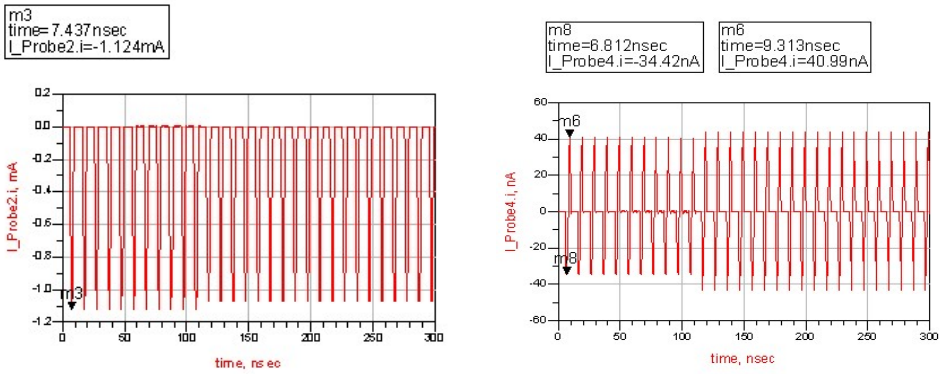
(c) Gate-coupled circuit

Figure 7. Left-hand side waveforms are square wave inputs and coupled signals (right-hand side waveforms) on the top-layer metal as for (a)MOS, (b)GGnMOS, and (c)gate-coupled circuit, respectively

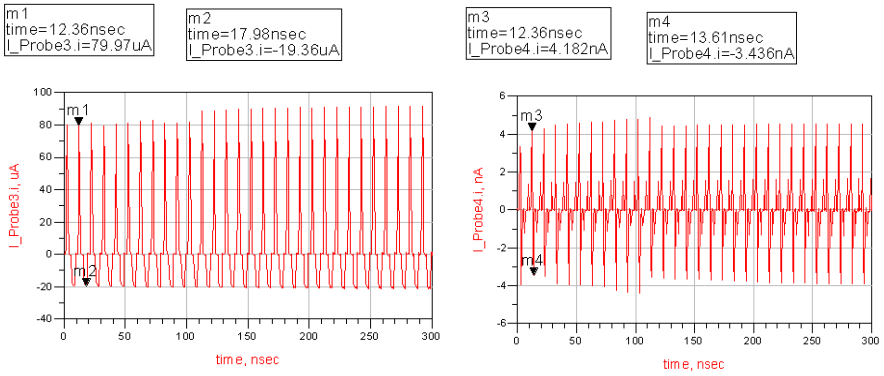
When a sinusoidal waveform was fed into these three circuits, as shown in Figs. 4~6, the MOS output response value was at about the μA order when the input signal was nearly 24.77-mA, as shown in Fig. 8(a). As shown in Fig. 8(b), the GGnMOS output value was very small, at about the nA order, when the input signal was near the 1-mA range. The input signal and the coupled signal of the top-metal as a sinusoidal pulse was fed into a gate-coupled circuit are shown in Fig. 8(c), respectively. The output sensing current of a gate-coupled circuit is also very small, at about the nA order.



(a) MOS



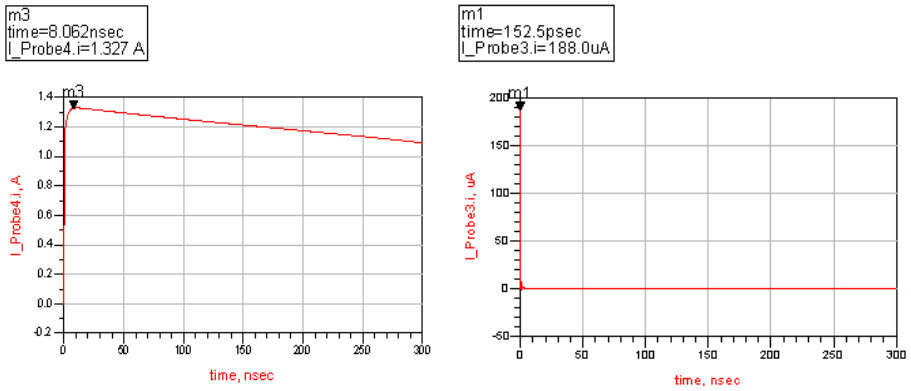
(b) GGnMOS



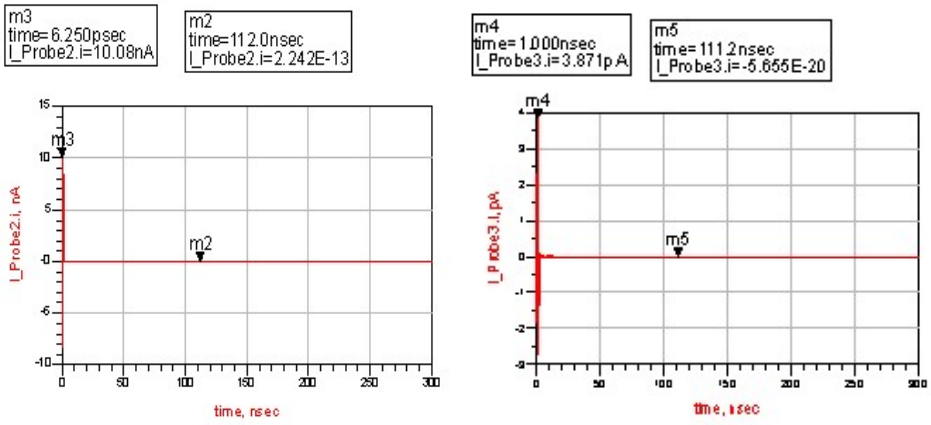
(c) Gate-coupled circuit

Figure 8. Left-hand side waveforms are sinusoidal wave inputs and coupled signals (right-hand side waveforms) on the top-layer metal as for (a)MOS, (b)GGnMOS, and (c)gate-coupled circuit, respectively

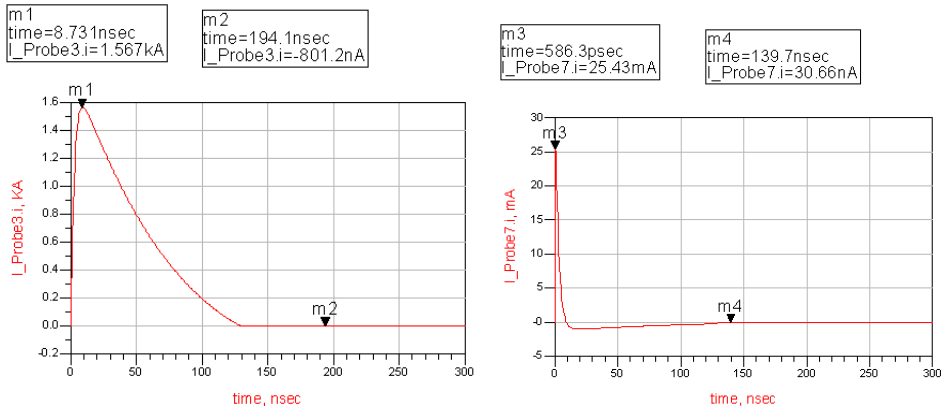
The final experiment consisted of feeding an ESD pulse into these three circuits again. The output response value of an MOS device is in the range of about 190-μA when the input signal is nearly 1.33-A, as shown in Fig. 9(a). As shown in Fig. 9(b), the output sensing value of a GGnMOS is still very small, at about the pA order, when the input signal is nearly 10-nA. The input signal and the coupled signal of the top-metal-layer when an ESD pulse was fed into a gate-coupled circuit are shown in Fig. 9(c), respectively. Here, the output detecting value of the gate-coupled circuit was clearly at about the 30 mA order.



(a) MOS



(b) GGnMOS



(c) Gate-coupled circuit

Figure 9. Left-hand side waveforms are ESD pulse inputs and coupled signals (right-hand side waveforms) on the top-layer metal as for (a)MOS, (b)GGnMOS, and (c)gate-coupled circuit, respectively

In general, the external square or sinusoidal signals coupled into the top-metal-layer are very small, as shown in Tables 3 and 4. In contrast, as shown in Table 5, when an ESD pulse was fed into the circuit, the coupled signal was very obvious on the top-metal. Meanwhile, from Tables 3~5, we can see that the coupled signals of the top-metal-layer in a GGnMOS were very small, which is due to the fact that a GGnMOS device cannot be re-modeled and turned-on as a parasitic BJT structure in the ADS even under an ESD stress condition. Furthermore, as indicated in Tables 3~5, when a pad size becomes smaller, the amplitude of the coupling signal will be stronger due to a smaller parasitic capacitance.

Table 3: Coupled currents on the top-layer metal as a square signal injected

Pad Area (μm^2)	MOS (nA)	GGnMOS (pA)	Gate-coupled (nA)
#1: 96×96	1510	15.89	6.805
#2: 75×65	1599	16.39	7.5
#3: 66×53	1822	19.2	8.128

Table 4: Coupled currents on the top-layer metal as a sinusoidal signal injected

Pad Area (μm^2)	MOS (nA)	GGnMOS (pA)	Gate-coupled (nA)
#1: 96×96	865.9	39.77	4.182
#2: 75×65	990	40	4.6
#3: 66×53	1000	48	5.028

Table 5: Coupled currents on the top-layer metal as an ESD pulse injected

Pad Area (μm^2)	MOS (μA)	GGnMOS (pA)	Gate-coupled (mA)
#1: 96×96	188	3.754	25.42
#2: 75×65	219.7	3.87	27.36
#3: 66×53	250.3	4.535	28.47

Furthermore, by same token as indicated in Tables 3~5, the peak currents of the top-metal-layer for a square, sinusoidal, or ESD pulse fed into an MOS, GGnMOS, or gate-coupled circuit are shown again in Figs 10~12. As shown in Fig. 10, when an ESD pulse was fed into an MOS device, the strongest coupling signal was obtained, while the sensing signal was very small for ordinary signal inputs such as square-wave or sinusoidal-wave signals. As for a GGnMOS device, it can be seen from Fig. 11 that a small coupling peak current (only of the pA order) was detected regardless of which kind of input signal was fed into it, which is due to the fact that a GGnMOS device cannot be re-modeled and turned-on as a parasitic BJT structure by the ADS. However, as shown in Fig. 12, when the ordinary input signals were fed into a gate-coupled circuit, the peak coupling signals were small, whereas when ESD event occurred, the sensing signal was at about ten times the mA range. In addition, as an ESD pulse was injected, good consistent data in terms of simulation and measurement in a gate-coupled circuit were yielded, as shown in Fig. 13. These data were measured by a high-frequency digital oscilloscope (Tektronix TDS3054B) and a current transformer.

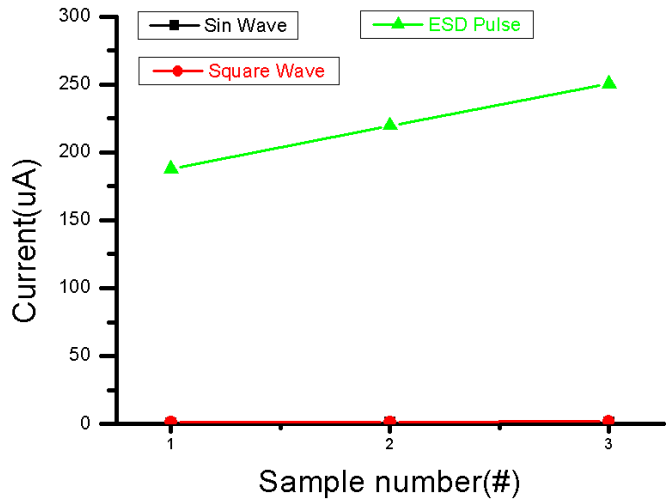


Figure 10. Peak sensing currents on the top-layer metal as for an MOSFET device

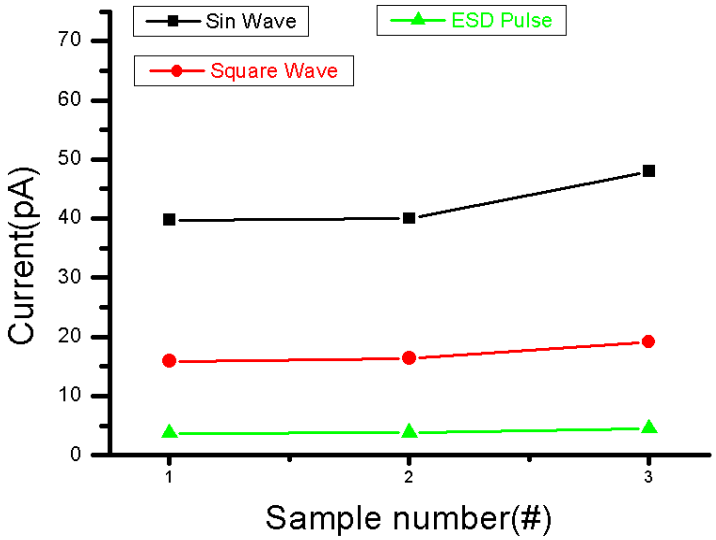


Figure 11. Peak sensing currents on the top-layer metal as for a GGnMOS device

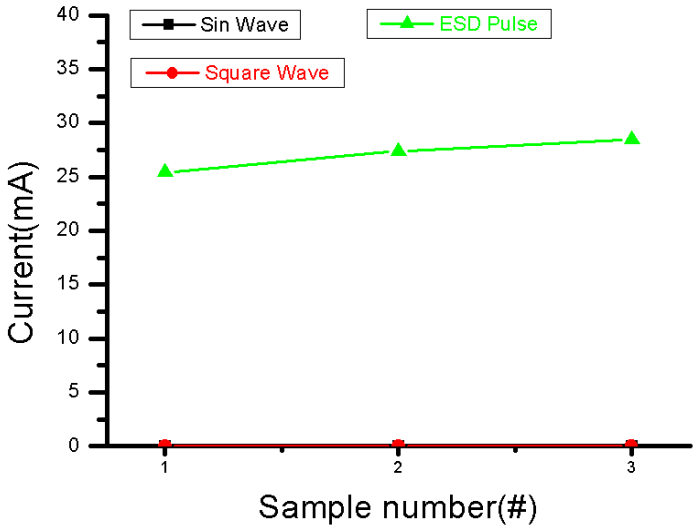


Figure 12. Peak sensing currents on the top-layer metal as for a gate-coupled circuit

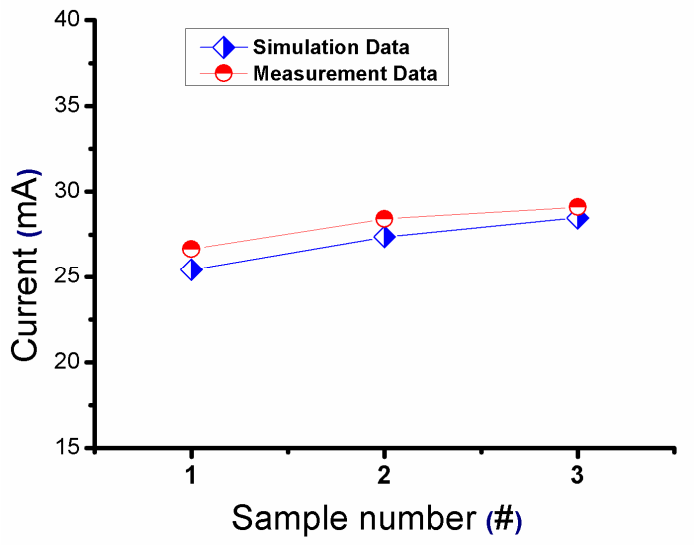


Figure 13. Comparison of peak sensing currents on the top-layer metal as for a gate-coupled circuit and an ESD pulse injected

VI. CONCLUSIONS

By using the Momentum toolkit (for schematics and layouts) of the ADS 2009 platform, a contactless sensing analysis for CUP structures can be implemented. A sensing capacitor combined with the top-metal can be used as a contactless detector to detect or measure internal

circuits and greatly improve the detection speed and measured time. In addition, from the EMI view of integrated circuits, the external signals or noises can be coupled into a top-metal-layer and then mixed with a normal signal in this top-metal through an MOS, GGnMOS or gate-coupled circuit. It was also found that during an ESD noise event, there is a strong coupling sensed by any ESD protection unit, especially for gate-coupled ESD protection circuitry. In conclusion, as demonstrated by the contactless sensing analysis in this study, it would be better not to use any CUP construction, especially for a gate-coupled circuit underneath a bonding pad.

ACKNOWLEDGMENT

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