A holistic DC link architecture design method for multiphase Integrated Modular Motor Drives

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Abstract—This article describes a holistic DC link architecture design method that considers the end-application of the drive and its corresponding constraints e.g. the maximum battery ripple current for a battery-supplied inverter. Also, the levers that are available to comply with the design criteria are presented e.g. the use of interleaved carrier waves. This holistic approach will result in a feasible and performant Integrated Modular Motor Drive from an application point of view. Finally, a platform is presented that was developed for feasibility and performance assessment of various DC link architectures obtained from the holistic design approach. The platform comprises a fifteen phase integrable modular motor drive for an Axial Flux Permanent Magnet Synchronous Machine. It allows non-intrusive reconfiguration of the DC link architecture and implementation of various control strategies and interleaved PWM schemes.

Keywords—DC link capacitor, Integrated Motor Drive, interleaved, inverter, modular, multiphase

I. INTRODUCTION

The need for increased reliability and power density of electric drivetrains in novel application areas like automotive and Industry 4.0, strongly determines the research efforts in this field nowadays. To cope with these needs, the Integrated Modular Motor Drive (IMMD) concept was proposed in literature. IMMD is an overarching term that denotes a group of power electronic integration concepts where the machine and/or drive electronics are discretized into modules to form a multiphase motor-drive combination. The emergence of new power-electronic technologies, characterized by their high energy efficiency, their high power density and their high operating temperatures, has made the integration of the power electronic converter in the motor housing a viable possibility. Fig. 1 shows an illustration of this concept for an Axial Flux Permanent Magnet Synchronous Machine (AFPMSM). Attractive features of IMMDS include:

- Improved fault-tolerant capabilities thanks to the use of a multiphase winding [2].
- Economy-of-scale effects because of the inherent modularity.
- Lower individual component ratings due to the higher power processing partitioning of the multiphase winding [1].

However, the realization of these attractive features gives rise to several design aspects that are not found in conventional motor drives [1], [3]. For example, the drive electronics should be able to operate over a sufficiently long lifetime in an environment with high temperatures, levels of mechanical vibrations and electromagnetic fields that originate from the close proximity of the motor. Therefore, the IMMD concept has been the subject of numerous articles that describe methods to cope with one or more extraordinary design aspects. The majority of the articles focusses on miniaturizing the drive electronics, since power density is an important driver for research in IMMD concepts. In particular,
the DC link architecture often constitutes the focus of these articles since this part takes up a large portion of the IMMD volume [4]. Measures to obtain a reduction of this volume might lead to an increased volume in other parts of the drivetrain such as external filters or heatsinks. This motivates the need for a holistic DC link architecture design method that considers the complete drivetrain (as presented in Fig. 3) when evaluating design choices. To the authors' best knowledge, a holistic DC link architecture design method has not yet been reported in the literature on Integrated Modular Motor Drives.

The DC link architecture design comprises:
1. Selection of the DC link filter circuit topology. Fig. 2 gives a non-exhaustive set of candidate topologies.
2. Sizing of the circuit capacitances and inductances in the selected circuit topology
3. Selection of the capacitor and inductor technology

Hence this is a multi-criteria, multi-degrees-of-freedom design problem. In combination with the extraordinary design specifications in IMMD applications, this might force the designer to introduce simplifications for the first iteration of the design process. In the reported experimental IMMD realizations of [5], [6] and [7], the DC link architecture design was simplified to a single-criterion, multi-degrees-of-freedom design problem. Their design's performance with respect to other criteria was however not mentioned. Often the used criterion only considers constraints imposed by the IMMD and not by other parts of the drivetrain. Although the authors reported that the integration of their IMMD concepts was feasible, this does not necessarily mean that their design satisfies the design constraints on other design criteria that are applicable to a certain end-application. Therefore it is not possible to assess the feasibility of the mentioned IMMD realizations from an application point of view. To illustrate this, consider the sizing of a DC link capacitor in a battery-supplied inverter. Using only the peak DC link voltage criterion, which is imposed by the semiconductor breakdown voltage [5], might result in a large battery ripple current rms value. This can drastically reduce the lifetime of the battery pack [8].

To fill this gap in literature on IMMD design, this article proposes a holistic multi-criteria, multi-degrees-of-freedom approach based on physical arguments for the design of the DC link architecture in IMMDs. The proposed method empowers the designer to obtain a feasible IMMD design from an application point of view. In subsection II.A the workflow of the design method will be described, then in subsection II.B, possible design criteria will be discussed, and in subsection II.C, the degrees of freedom that are at the disposal of the designer are presented. Finally in section III, the platform is presented that was developed for feasibility and performance assessment of various DC link architectures obtained from the holistic design approach outlined in this article.

II. HOLISTIC DC LINK ARCHITECTURE DESIGN METHOD

A. Method

This subsection describes a method to design the DC link architecture for an IMMD comprising a multiphase two-level Voltage Source Inverter (VSI). The proposed method considers the design problem as a holistic multi-criteria, multi-degrees-of-freedom design problem. This means that DC link architecture design choices are evaluated on the basis of their impact on the complete drivetrain, which comprises power source, front-end converter, external filter, IMMD and load as shown in Fig. 3. This allows the designer to obtain a DC link architecture that results in a feasible IMMD design from an application point of view, since application-specific criteria are taken into account.

Fig. 4 presents a graphical representation of the proposed method. The method requires as input both knowledge of the IMMD end-application and the preliminary drivetrain hardware configuration i.e. the hardware configuration without the DC link architecture. Knowledge of the end-application consists of performance requirements on the drivetrain that originate from the end-application, such as the required acceleration and deceleration capability, continuous and peak torque, and rated and maximum speed. This knowledge is used to design the complete hardware configuration of the drivetrain except the DC link architecture.
This part of the drivetrain design falls beyond the scope of this article, and is considered as input to the DC link architecture design. However, if no feasible DC link architecture design can be found, the designer might have to alter the hardware configuration. The knowledge of the end-application and hardware configuration is then used to determine the DC link architecture design criteria and design levers as will be discussed in subsequent paragraphs.

The design criteria on the DC link architecture can be divided into two groups: criteria that originate directly from the end-application and criteria that indirectly originate from the end-application via the design choices made in other parts of the drivetrain. These design choices constitute the hardware configuration as mentioned in Fig. 4. Every criterion can either be subjected to constraints or optimization or both. For example, in an application where the power source features very slow dynamics but a certain minimum acceleration performance is required, the DC link architecture should contain enough energy storage elements to deliver the peak power for acceleration. The acceleration performance is a criterion that originates from the end-application, and that is subjected to a lower bound. In drivetrains with battery-supplied inverters on the other hand, the battery lifetime depends on the battery ripple current rms value [8]. Therefore, the DC link filter design should use the maximum battery ripple current rms value, specified by the manufacturer, as a constraint [10]. The battery ripple current rms value is a criterion that originates from the hardware configuration that includes a battery in this specific case. Other design criteria mentioned in Fig. 4 will be discussed in subsection II.B.

To satisfy the constraints on the design criteria or if necessary, optimize some of the design criteria, the designer has several degrees of freedom, called ‘levers’ hereafter. These levers represent degrees of freedom available to meet the constraints or optimize the design criteria of the DC link architecture without altering the given hardware configuration. In [11], interleaved PWM carrier waves are used as a lever to reduce the inverter input current harmonics. An extensive discussion of other levers mentioned in Fig. 4 will be given in subsection II.C.

Eventually, the designer should make an appropriate choice for every design lever. For every choice of the design levers, the numerical values of the design criteria can be calculated using appropriate models, and they are then compared to the design constraints and/or checked for optimality. Every set of design levers that meets these requirements will result in feasible IMMD realizations from an application point of view. If no choice satisfies the constraints, the designer should consider adapting the hardware configuration.

Heuristically choosing design levers, calculating the design criteria and comparing them to the design constraints, and/or checking for optimality, requires a large number of design criteria evaluations. To reduce this number, the designer can leverage on guidelines and models that describe a relation between the design levers and their effect on the design criteria. In literature on IMMDs, the effect of using interleaved PWM carrier waves on the DC link ripple current has been extensively covered [10][11][12]. However, for other design levers, especially the DC link architecture circuit topology, this relation is less well documented. Given the large number of candidate DC link architecture circuit topologies, this documentation constitutes a study on its own, and will be the subject of future research. This article only describes the holistic design method and a platform to evaluate several choices of the design levers.

B. Design criteria

This subsection gives the most common DC link architecture design criteria found in IMMD applications. As already mentioned, the design criteria can be divided in two groups: the ones that directly originate from the end-application and the ones that indirectly originate from the end-application via design choices in other parts of the drivetrain. The references in this subsection provide more information on the implications of these criteria on the DC link architecture design aspects.

The criteria that originate from the end-application often include:

1. The expected lifetime of the drivetrain including the DC link filter [13][14].
2. The ambient temperatures the drivetrain has to be capable to operate in [15].
3. The level of mechanical vibrations that the IMMD should be capable to withstand [3].

4. The accelerating and decelerating performance of the drivetrain [16].

The criteria originating from the hardware configuration include:

1. The internal DC link filter volume.
2. The peak DC link voltage. The breakdown voltage of the semiconductor switches imposes an upper bound on this criterion. The DC link capacitor should provide a low-inductive commutation path for the current to prevent the peak DC link voltage from exceeding the breakdown voltage due to the semiconductor switching [5].
3. The DC link voltage ripple amplitude. To avoid EMC issues, the amplitude of the high-frequent voltage ripple generated by the high-frequent switching operation should not exceed a certain limit [17].

These are the criteria originating indirectly from the end-application since they originate from the design choices made in the hardware configuration. These criteria apply to every IMMD design.

In addition, there are criteria that only apply to certain specific hardware configurations:

1. In battery-supplied IMMDs, the battery ripple current should be considered as an additional criterion. According to [8], the battery ripple current rms value has a negative impact on the expected lifetime of the battery pack, and should therefore not exceed the limits specified by the battery manufacturer. The DC link capacitor should deliver the high-frequent current ripple instead of the battery [10], [13].

2. In grid-connected passive rectifier supplied IMMDs, the input power fluctuation due to the rectifier’s operating principle or due to power quality issues of the grid [9], [18] constitutes a criterion. The DC link filter should have enough energy storage capacity to compensate these fluctuations.

3. In IMMDs with unidirectional power-flow power supplies, the DC link voltage increase in case of an instantaneous power reversal is a design criterion. Instantaneous power reversal can occur during braking or in case of an emergency shutdown of all semiconductor switches [9]. The DC link capacitor should be sized so that it can absorb the reversed power and limit the DC link voltage rise.

C. Design levers

This subsection will discuss the design levers that are at the disposal of the IMMD designer to optimize the design criteria or satisfy the constraints on the design criteria that apply to his application and hardware configuration. There exist two groups of design levers, the first group was already mentioned in section I and comprises all elements that constitute the DC link architecture design. The second group comprises aspects related to the control of the multiphase two-level VSI.

The first group comprises, amongst other levers, the selection of the DC link filter circuit topology. In [19], it was already demonstrated that the interconnection between the individual modules has an impact on the DC link capacitor current due to the parasitic inductance of the interconnections. An interconnection with a low parasitic inductance could decrease the DC link capacitor rms current by 30%. Therefore the circuit topology is considered an important design lever. The designer has several options for the circuit topology: either a centralized, external or decentralized, internal filter or a combination of both, mainly capacitive elements or also inductors, a special low-inductance interconnection between the modules or a standard low-cost interconnection. Possible candidate circuit topologies were already given in Fig. 2. To illustrate how the DC link filter circuit topology can be used as a lever to meet the constraint on the volume criterion, consider the choice for a circuit topology with a combination of both a centralized, external filter and decentralized, internal filter. The internal filter can be chosen sufficiently small since its only function will be to provide a low-inductive commutation path for the current that is switched by the semiconductor switches. Whereas the external filter will act as a filter between front-end converter and IMMD, this filter can be chosen larger in order to meet the application requirements, and can be located where more volume is available.

Besides selection of the DC link filter circuit topology, the first group of design levers also comprises the sizing of the capacitors and inductors, and selection of their technology. Both of these levers often go hand-in-hand. For example, if electrolytic capacitors are selected because of their high capacitance per volume, their current capabilities in terms of maximum rms current will be the most stringent design constraint. Therefore, sufficient electrolytic capacitors have to be paralleled to reduce the current stress per capacitor. Often the total capacitance then provides more filtering than is required to meet the constraints on the other criteria. If, on the other hand, ceramic or film capacitors are chosen, the current capabilities are no longer a limiting factor and they should be sized according to the governing criteria of the end-application and hardware configuration [19]. Also the high operating temperatures in IMMDs play an important role in the selection of the capacitor technology [3]. Film or ceramic capacitors are an attractive option due to their higher temperature rating which reduces the cooling requirements.

The second group deals with the control aspects of the multiphase two-level VSI that can be adapted without altering the existing hardware configuration:

- A higher switching frequency can be used to reduce the size of the passive components in the IMMD [3].
- The carrier waves of different PWM signals can be interleaved in order to reduce DC link and capacitor ripple current. This was successfully demonstrated in [10][11][12][20]. This is mainly an important aspect in battery-supplied inverters since the remaining useful lifetime of the battery is directly affected by the DC link ripple current rms value. It is also important in inverters that use electrolytic capacitors in the DC link, since they have a high equivalent series resistance and thus a low current capability compared to other capacitor technologies.
- The PWM scheme and dead time can also be considered as levers. Choosing a PWM scheme with
a larger DC link voltage utilization allows to reduce the DC link voltage level which is determined by the maximum back-emf. It is assumed that the maximum back-emf is determined by the maximum required operating speed of the drivetrain. A lower DC link voltage level will result in a smaller DC link capacitor. The dead time introduces additional harmonics in the spectrum of the DC link current, and should therefore also be considered as a lever.

If these levers do not suffice to comply with all constraints, the designer has no other option than to adapt the hardware configuration. For example, wide bandgap switches could be used instead of conventional silicon based semiconductors. This allows a higher switching frequency and thus a reduction of the DC link capacitor volume [3].

III. EXPERIMENTAL DC LINK ARCHITECTURE VALIDATION PLATFORM

This section will describe the experimental platform that was developed to implement various DC link architecture designs and compare their performance with respect to several design criteria such as IMMD volume or DC link ripple current rms value. The goal of this comparison is to fill the gap in literature on IMMDs concerning the selection of an appropriate DC link filter circuit topology. However, due to the large number of candidate circuit topologies, this will be the subject of future research. This paragraph will only deal with the description of the platform, with a focus on how it allows to implement various DC link filter circuit topologies and which control aspects of the multiphase two-level VSI can be varied in this platform.

The platform is given in Fig. 6. It consists of a variable DC voltage source (not shown on this figure), fifteen half-bridge inverter modules, an AFPMSM [21], and a dSPACE Microlabbox (not shown on this figure) containing a real-time processor and FPGA. For the commissioning of the validation platform, the DC link voltage was set to 48 V, and a DC link filter topology as given in Fig. 5 was implemented, which comprises fifteen 1 mF electrolytic capacitors and no inductors. The capacitors were connected in series to allow fast reconfiguration via plug-and-play connectors. Additional external capacitors or inductors can also easily be connected between the two DC link terminals. The AFPMSM was loaded with an 7.5 kW induction motor that was operated in speed mode. The AFPMSM was torque controlled via a multiphase field oriented control [20][22]. The motor parameters are given in Table I. The half-bridge modules use mosfets (TI CSD19506KCS) and a bootstrap gatedrive IC to control the mosfets. The switching frequency was set to 50 kHz and the dead time to 1 μs. The use of a multiphase winding offers the designer the possibility to use interleaved carrier waves. The influence of the use of interleaved carrier waves was investigated experimentally by varying the phase shift between the PWM carrier waves. Fig. 7 gives the DC link ripple current for the situation without and with optimal interleaved carrier waves [11]. A comparison indicates that the DC link ripple current rms value can be reduced by 40% in the worst-case motor operating point i.e. from 0.12 A to 0.074 A. The Microlabbox allows to quickly validate the performance for various settings of the switching frequency, dead time, PWM scheme and interleaving strategy. The plug-and-play connectors of the DC link capacitors and the multiphase two-level VSI control via a dSPACE Microlabbox make this platform suited to compare the performance of various DC link architectures for IMMDs.

IV. CONCLUSION AND FUTURE RESEARCH

This article has presented a DC link architecture design method for IMMDs that considers the design problem as a multi-criteria, multi-degrees-of-freedom design problem. In contrast to IMMD designs described in literature, where only one design criteria is considered to design the DC link architecture, this article presents a holistic approach that takes into account all criteria from both the end-application and hardware configuration. This is a necessary condition to obtain a feasible IMMD realization from an application point of view. Finally, the experimental platform that is developed to validate various DC link architecture designs is presented. This platform comprises a fifteen phase half-bridge inverter that features a reconfigurable DC link filter. Moreover, the control strategy of the multiphase two-level VSI is implemented on a dSPACE Microlabbox, this enables fast validation of several control strategies. This platform will be used to compare the effectiveness of various DC link architecture designs and control strategies of the multiphase

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TABLE I. MOTOR PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power [kW]</td>
<td>4</td>
</tr>
<tr>
<td>Rated speed [rpm]</td>
<td>2500</td>
</tr>
<tr>
<td>Pole pairs [1]</td>
<td>8</td>
</tr>
<tr>
<td>Rated phase current [A_{base}]</td>
<td>10</td>
</tr>
<tr>
<td>Stator phase resistance [mΩ]</td>
<td>65</td>
</tr>
<tr>
<td>Stator inductance (L_{st}-L_{d}) [mH]</td>
<td>2.54</td>
</tr>
</tbody>
</table>
two-level VSI in optimizing some design criteria and/or meeting the constraints on other criteria for a given end-application and hardware configuration. However, due to the large number of candidate DC link architectures, and multiphase two-level VSI control strategies, this study falls beyond the scope of this article and will constitute the subject of future research.

REFERENCES


Fig. 6. Experimental IMMMD: (1) Axial Flux Permanent Magnet Synchronous Machine (2) Copper DC link bus bar (3) Electrolytic DC link capacitor (4) Half-bridge inverter module (not integrated yet)

Fig. 7. DC link current without interleaved carrier waves (κ=0°) and with optimal interleaved carrier waves (κ=140°) for an AMPMSM operating at the worst-case motor operating point i.e. T=15 Nm and \( \dot{Q} \)=500 rpm, using multiphase field-oriented control with a DC link voltage of 48 V.