Design of Agile Signal Conditioning Circuits for Microelectromechanical Sensors

By

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Conception d'un circuit de conditionnement de signal agile pour capteurs microélectromécaniques

Parisa VEJDANI

RÉSUMÉ

Les systèmes microélectromécaniques (MEMS) sont utilisés dans des nombreuses applications pour détecter les paramètres physiques et les convertir en signal électrique. Généralement, la sortie des transducteurs à base de MEMS ne convient pas pour être traitée directement dans le domaine numérique ou analogique. L'ordre de grandeur peut être aussi petit que des femto farad en détection capacitive ou des micro volts en détection résistive. Par conséquent, les exigences du conditionnement de signaux à haute sensibilité sont essentielles. Le bruit et la capacité d'entrée sont des paramètres importants de la détection capacitive. La source de bruit dominante dans le circuit de conditionnement MEMS est le bruit de scintillement et la technique de hachage est l'un des meilleurs moyens afin d'éliminer le scintillement. Trois techniques de hachage différentes sont utilisées : un amplificateur à hacheur simple (SCA), un amplificateur à hacheur double (DCA) et un amplificateur à hacheur simple à deux étages (TCA). De plus, leur sensibilité et leur consommation de puissance basée sur le gain total et la capacité de détection sont extraites. Nous montrons que la distribution du gain entre les deux étages du DCA et du TCA a un effet significatif sur la sensibilité et que la sensibilité et la consommation de puissance changent considérablement en fonction de cette distribution. À faible détection capacitive, le DCA pourrait atteindre la sensibilité la plus élevée en raison de sa capacité à réduire simultanément le bruit de fond et la capacité du capteur d'entrée. En outre, un nouveau DCA est proposé pour atteindre la plus grande sensibilité et la plus faible consommation de puissance. Dans ce DCA, deux tensions d'alimentation sont utilisées et le deuxième étage est composé de deux chemins parallèles qui améliorent le rapport signal sur bruit et fournissent deux réglages de gain. Ce circuit est fabriqué en technologie CMOS de $0.13~\mu m$. Les résultats de mesures ont montré une consommation de $2.66~\mu W$ pour la tension d'alimentation de 0.7V et de $3.26~\mu W$ pour la tension d'alimentation de 1.2V. Le DCA à simple trajet a un gain de 34 dB, une bande passante de 4 kHz et un bruit de fond de $25~nV~/~\sqrt{Hz}$. Le DCA à double trajet a un gain de 38 dB, une bande passante de 3 kHz et un bruit de fond de $40~nV~/~\sqrt{Hz}$. Afin de pouvoir détecter le signal près de la fréquence DC, un autre circuit a été proposé, dans lequel une bande passante configurable et une fréquence de bruit de coin sous les μHz. Ce circuit est composé de trois étages et trois fréquences de hacheur sont utilisées pour éliminer le bruit de scintillement des trois étages. Le circuit simulé est conçu dans une technologie CMOS de $0.13~\mu m$ avec des tensions d'alimentation de 0.4 V et 1.2 V. La consommation totale est de $6.7~\mu W$. Un gain de 68 dB et des bandes passantes de 1, 10, 100 et 1000 Hz sont obtenues. Le seuil de bruit en entrée est de $20.5~nV~/~\sqrt{Hz}$ et la conception atteint un bon facteur d'efficacité énergétique de 4.0. En mode capacitif, le bruit de fond est de 3.6 zF pour un capteur ayant une capacité de 100 fF.

Mots clés: hacheur, faible bruit, faible consommation, fréquence de coupure basse, amplificateur à double hacheur, sensibilité à la capacité, sensibilité élevée

Design of Agile Signal Conditioning Circuits for Microelectromechanical Sensors

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ABSTRACT

Microelectromechanical systems (MEMS) are used in many applications to detect physical parameters and convert them to an electrical signal. The output of MEMS-based transducers is usually not suitable to be directly processed in the digital or the analog domain, and they could be as small as femto farads in capacitive sensing and micro volts in resistive sensing. Consequently, high sensitivity signal conditioning circuits are essential. In this thesis, it is shown that both the noise and input capacitance are important parameters to ensure optimal capacitive sensing. The dominant noise source in MEMS conditioning circuits is flicker noise, and one of the best methods to mitigate flicker noise is the chopping technique. Three different chopping techniques are considered: single chopper amplifier (SCA), dual chopper amplifier (DCA), and two-stage single chopper amplifier (TCA). Also, their sensitivity and power consumption based on the total gain and sensing capacitance are extracted. It is shown that the distribution of gain between the two stages in the DCA and TCA has a significant effect on the sensitivity, and, based on this distribution, the sensitivity and power consumption change significantly. For small sensor capacitances, the highest sensitivity could be achieved by a DCA because of its ability to decrease the noise floor and the input sensor capacitance simultaneously. A novel DCA is proposed to reach higher sensitivity and reduced power consumption. In this DCA, two supply voltages are utilized, and the second stage is composed of two parallel paths that improve the SNR and provide two gain settings. This circuit is fabricated in the GlobalFoundries 0.13 µm CMOS technology. The measurement results show a power consumption of 2.66 µW for the supply voltage of 0.7 V and of 3.26 µW for the supply voltage of 1.2 V. The single path DCA has a gain of 34 dB with bandwidth of 4 kHz and input noise floor of 25 nV/√Hz. The dual path DCA has a gain of 38 dB with bandwidth of 3 kHz and input noise floor of 40 nV/√Hz. To be able to detect the signal near DC frequencies, another circuit is proposed which has a configurable bandwidth and a sub-µHz noise corner frequency. This circuit is composed of three stages, and three chopping frequencies are used to mitigate the flicker noise of the three stages. The simulated circuit is designed in the GlobalFoundries 0.13 µm CMOS technology with supply voltages of 0.4 V and 1.2 V. The total power consumption is of 6.7 µW. A gain of 68 dB and bandwidths of 1, 10, 100 and 1000 Hz are achieved. The input referred noise floor is of 20.5 nV/√Hz and the design attains a good power efficiency factor of 4.0. In the capacitive mode, the noise floor is of 3.6 zF for a 100 fF capacitance sensor.

Keywords: Chopping, high sensitivity, low noise, low power, low corner frequency, dual chopper amplifier.

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LIST OF ABREVIATIONS

ADC	Analog to Digital Converter
BW	Bandwidth
CAGR	Compound Annual Growth Rate
CIS	Contact Image Sensor
CMOS	Complementary Metal Oxide Semiconductor
DCA	Dual Chopper Amplifier
FM	Frequency Modulation
FVC	Frequency to Voltage Converter
LPF	Low Pass filter
MEMS	Micro Electro-Mechanical Systems
PEF	Power Efficiency Factor
PVT	Process, Voltage and Temperature variations
PWM	Pulse-Width Modulation
SAR	Successive Approximation Register
SCA	Single Chopper Amplifier
SNR	Signal to Noise Ratio
TCA	Two-stage Chopper Amplifier
THD	Total Harmonic Distortion
VLSI	Very Large-Scale Integration

LIST OF SYMBOLS AND UNITS

Z	Zepto
f	Femto
n	Nano
m	Mili
μ	Micro
k	Kilo
M	Mega
V	Volt
W	Watt
Hz	Hertz
F	Farad
dB	Decibel
P	Power
I	Current
R	Resistor
C	Capacitance
T	Temperature
S_F	Sensitivity Factor
g_m	Transconductance
W	Width of transistor
L	Length of transistor

C_{ox}	Oxide capacitance
V_n	Thermal noise
C_{gg}	Input capacitance of transistor
f	Frequency
f_{chop}	Chopping frequency

INTRODUCTION

Background and motivation

Sensors are becoming more and more prevalent in a wide range of applications touching our daily lives. They are a crucial component in environment sensing (Maruyama, Taguchi, Yamanoue, & Iizuka, 2016; X. Wang et al., 2017), medical equipment (Lopez et al., 2018; Yazicioglu, Kim, Torfs, Kim, & Hoof, 2011), smart homes (Byun, Jeon, Noh, Kim, & Park, 2012; Vujović & Maksimović, 2015), automotive electronics (Altaf, Zhang, & Yoo, 2015; Cooley, Wallace, & Antohe, 2002; Hilt, Gupta, Bashir, & Peppas, 2003; Luo et al., 2008; Vasilyev, Rewienski, & White, 2006), and smart portable electronics (Charlot, Sun, Yamashita, Fujita, & Toshiyoshi, 2008; Rashidi & Mihailidis, 2013; Shi et al., 2009; Yazdi, Mason, Najafi, & Wise, 1996). For example, smartphones include sensors such as face ID, barometer, three-axis gyro, accelerometer, proximity sensor, ambient light sensor and modern cars easily contain more than 100 sensors used for several functions such as basic operation (engine temperature, oil pressure), information and driving help (parking aid, tire pressure measurement), comfort (air conditioning, defogging), safety (airbag deployment, yaw rate sensing) and optimization (exhaust gas monitoring), etc. (Wilcox & Howell, 2005; J. Zhao, Jia, Wang, & Li, 2007).

Among different kinds of sensors, MEMS (Micro-ElectroMechanical Systems) -based sensors are implemented broadly nowadays. They have the advantage of small size, low cost, low power consumption, and high reliability. This kind of sensor had a significant growth during the past years.

The growth of revenues from MEMS systems in different applications from 2014 to 2024 is shown in Figure 0.1. As displayed, consumer electronics, automotive, and medical sensors have larger growth. In 2024, MEMS market revenues will come mostly from consumer electronic applications, estimated to reach US$13B. Moreover, automotive applications are

estimated to reach US$6B, and medical sensors are estimated to reach US$5B worldwide (Yole, 2017).
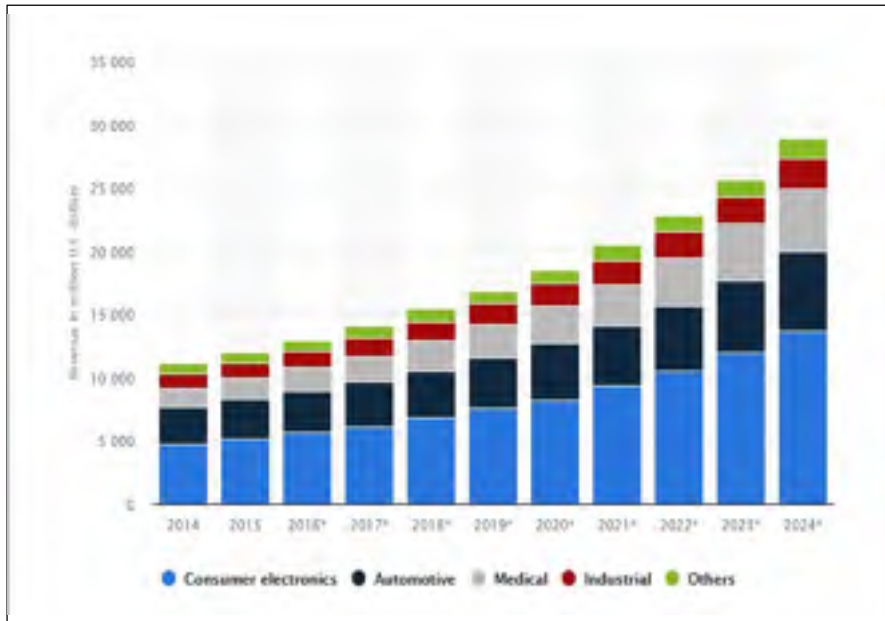
Figure 0.1 Revenues from the global micro-electromechanical
systems (MEMS) market from 2014 to 2024, by application,
taken from (Yole, 2017)

To compare the growth of MEMS systems with other kinds of sensors, segmented revenues are shown from 2015 to 2021 in Figure 0.2. As shown, it is estimated that the market for MEMS and sensor devices will grow from US$49B in 2018 to US$66B in 2021. Such a figure is an impressive 12% compound annual growth rate (CAGR). Also, it is shown that the revenue of MEMS and contact image sensors (CIS) are remarkable in comparison with others. This revenue was US$10.5B for MEMS in 2015, and it is estimated to jump to US$21B in 2021. Moreover, new applications of MEMS sensors are also emerging with use in smart homes and buildings recently. The sensor market has a CAGR of 13.4% in smart homes and buildings from 2016 to 2022, and it is predicted to be US$1.7B U in 2022 (Muller, Gambini, & Rabaey, 2012).

MEMS sensors can respond to physical parameters such as radiation (Augustyniak et al., 2013; Buchner et al., 2007; Musca et al., 2005), pressure (Ge, Wang, Chen, & Rong, 2008; Mohan,
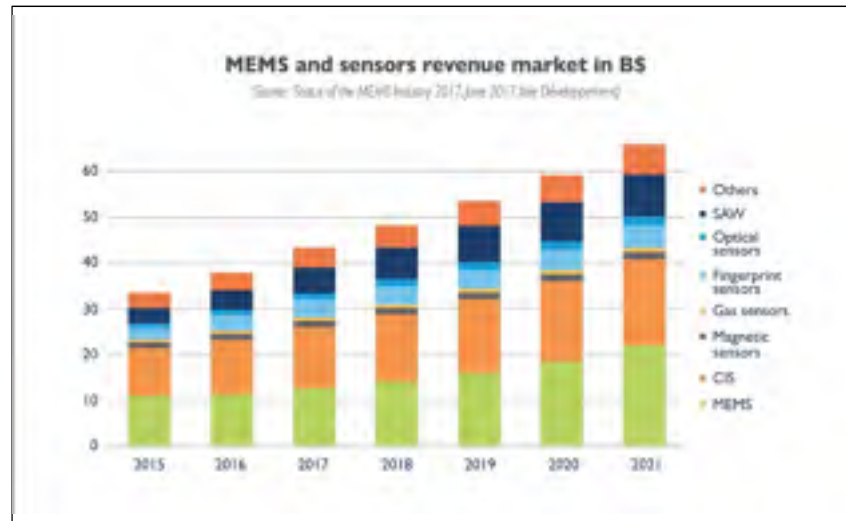
Figure 0.2 MEMs and sensors market anticipation,
taken from (Yole, 2017)

Malshe, Aravamudhan, & Bhansali, 2004; Palasagaram & Ramadoss, 2006; Y. Zhang, , movement (Fitzmaurice, 1993; B. Lee, Bang, Kim, & Kim, 2011; Mehra, Werkhoven, & Worring, 2006; Rohs et al., 2007), flow (Kao, Kumar, & Binder, 2007; E. Meng & Yu-Chong, 2003; Nguyen, Paprotny, Wright, & White, 2015; Shibata, Niimi, & Shikida, 2014; Y.-H. Wang, Lee, & Chiang, 2007), chemical (Holthoff, Heaps, & Pellegrino, 2010; Lavrik, Sepaniak, & Datskos, 2004; Saxena, Plum, Jessing, & Baker, 2006), or temperature (Khazaai, Haris, Qu, & Slicker, 2010; Que, Park, & Gianchandani, 1999; Sinclair, 2000).

Problems and challenges statement

The output of MEMS sensors usually are not proper for signal processing such as analog to digital conversion. Accordingly, signal conditioning circuits should be integrated at the outpout of the sensors before further signal processing. These circuits preserve the integrity of the sensor's signal and properly amplify it while maintianing the signal to noise radio and minimizing distortion. Accordingly, signal conditioning circuits are implemented to amplify the signal with low added noise in order to make the signal ready to process in an analog or digital fashion. The frequency range of detected signals in MEMS-based sensors are up to a few kHz, and in biomedical applications it can be as small as a few Hz. For example, the

frequency of brain waves can be small as 0.5 Hz and the amplitude can be as small as 5 µV. As a result, removing the flicker noise of the signal conditioning circuit is the most important challenge in these applications. In additon of the flicker noise, the thermal noise should be minimized to be able to detect the signal properly. Also, in capacitive sensors, the effect of input capacitance of signal the conditiong circuit should be considered, as it can negatively impact sensitivity. Accordingly, the signal conditioning circuit should be optimized for flicker and thermal noise, and for low input capacitance. At last, the power consumption should be minimized to be able to allow for the sensor to be deploed in battery-operated environments, where sensors are often needed. However, there is a tradeoff between decreasing the noise, power consumption, and input capacitance of the circuit, and this thesis aims at investigating this tradeoff and proposing signal conditioning circuit architectures that can provide a good tradeoff.

Signal conditioning circuit overview

The schematic of a typical sensor is shown in Figure 0.3. As shown, it consists of two main parts: MEMS transducer and signal conditioning circuit. The physical parameters such as temperature, pressure, position, movement, and vibration are detected and converted to an electrical signal in a MEMS transducer and then transferred to a signal conditioning circuit for amplification and filtering. Since the output signal produced by a sensor is usually not suitable to directly process in the digital or analog domain, signal conditioning is a method of preparing an analog signal for further processing. The signal conditioning usually involves amplification and filtering. The goal of the filtering stage is eliminating the noise from the signal of interest and the aim of the amplifier is to increase the performance of the circuit. MEMS sensors have different electrical characteristics. The principle of operation of the sensor determines the nature of sensor output, which in turn determines the signal conditioning circuit requirement. Thus, depending on the sensor output, a circuit can be designed in different configurations to extract the sensor output (Master, 2010).
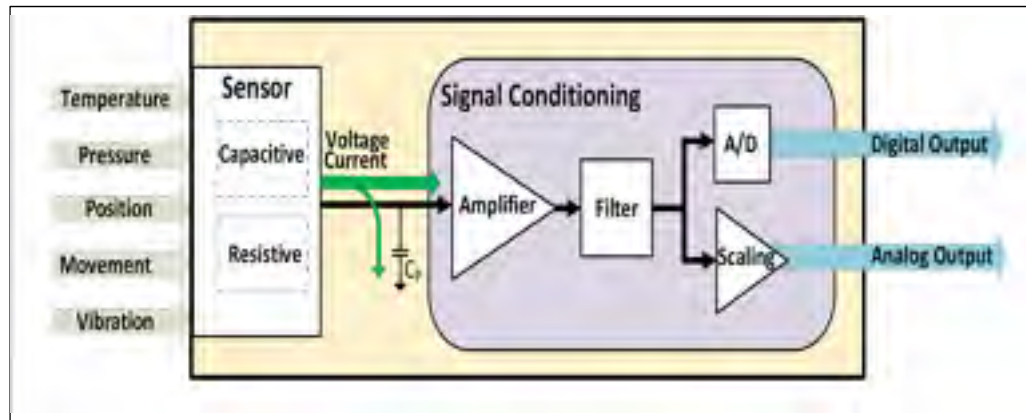
Figure 0.3 Schematic of a typical sensor

To detect the signal in the transducer, a capacitive bridge, or a resistive bridge could be implemented to convert the physical parameters to the electrical signal. The output of resistive sensors usually varies from few hundreds of μV to tens of mV, and the output of the capacitive sensor can be as small as femto farad. Usually capacitive sensors are preferred to resistive ones because of their high sensitivity, low power consumption, and high reliability. In the capacitive (resistive) sensing, there is a nominal value for the capacitance (resistance) and with a physical variation, the value of the capacitance (resistance) is changed. By measuring this variation, the amount of physical parameter change will be defined. Performance of the MEMS sensors is dependent to both the MEMS transducer design and the signal conditioning circuit design. In this work, design of the signal conditioning part will be investigated. This circuit should be precise enough to be able to integrate with different MEMS transducers.

A capacitive sensor and its integration with a signal conditioning circuit is shown in Figure 0.4. The output voltage of this transducer equals to:

$$V_o = \frac{\Delta C}{C_0} V_m \tag{0.1}$$

Where, C_0 is the nominal capacitance sensor, V_m is the excitation voltage and ΔC is the capacitance variation.

However, when this transducer is connected to a signal conditioning circuit, the input
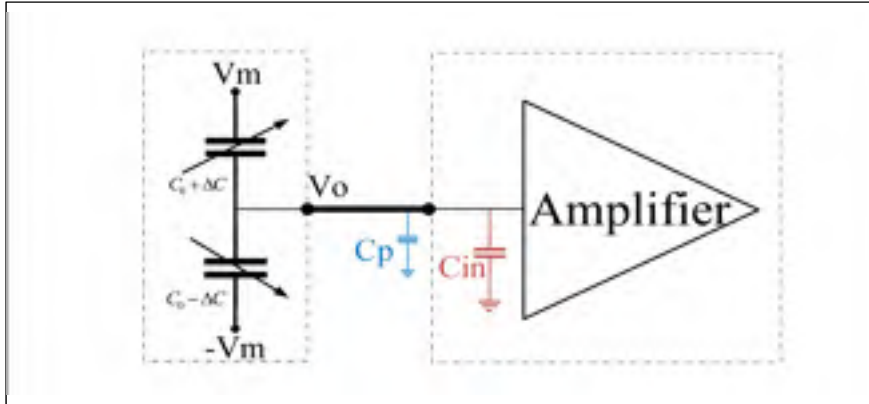
Figure 0.4 Capacitive sensing and its integration with signal conditioning circuit

capacitance of the signal conditioning circuit will be affected on the performance of the transducer. As a result, the output voltage of capacitive sensor equals to:

$$V_o = \frac{2\Delta C}{2C_0 + C_P + C_{in}} V_m \tag{0.2}$$

where C_p is the parasitic capacitance of wiring, and C_{in} is the input capacitance of signal conditioning circuit. With the proper integration of the MEMS transducer with signal conditioning circuit, the C_p could be removed, but the value of C_{in} is dependent on the signal conditioning circuit design. For small sensor capacitances, the value of the input capacitance of a signal conditioning circuit is important, and it should be considered in the design of signal conditioning circuit. The voltage produced by the capacitive sensor is transferred to the signal conditioning circuit. Consequently, the value of this voltage should be larger than the input noise of signal conditioning circuit to be detectable. Thus, another important factor that should be considered in the design of a high sensitivity circuit is the input noise level of the signal conditioning circuit. It should be noticed that decreasing the noise level could be possible at the cost of increasing the input capacitance. As a result, the noise level of the signal conditioning circuit should be decreased while keeping the input capacitance low. Moreover,

the power consumption and area are the two other factors that should be considered for sensors in portable devices.

To reach these characteristics, many different signal conditioning circuit architectures are possible. An appropriate choice of architecture is beneficial to detect the signal with enough sensitivity and gain and make it ready for processing.

Research goals and objectives

The goal of this research is to investigate novel signal conditioning circuits to enable the readout of several MEMS-based transducers. These circuits will have to feature low power consumption and noise reduction techniques, and also be agile (i.e., reconfigurable) to accommodate various capacitive and resistive MEMS transducer types.

The following research objectives were tackled during this Ph.D.:

- Design a best-fit signal conditioning circuit based on the sensor characteristics and required gain;
- Enable energy efficient operation by targeting ultra-low power consumption to enable the use of multiple sensors in portable devices with a longer battery life and better performance;
- Minimizing the noise in order to be able to detect the smallest variation in the sensors;
- Minimizing the input capacitance in order to prevent the loading effect on the capacitive sensors and maintain the sensitivity; and
- Improving the SNR of the signal conditioning circuit to maintain the input signal integrity;

Our Approach

In order to achieve the above-mentioned goals and objectives, various signal conditioning circuits are investigated and compared. For our desired application, a chopper technique is preferred to reach the small noise floor. Then, different chopping techniques, such as single

chopper amplifier (SCA), two-stage chopper amplifier (TCA), and dual chopper amplifier (DCA), are considered for capacitive and resistive sensors.

First, the power consumption, the input noise floor, and the sensitivity of different chopping techniques are analysed for different gains and sensor capacitances. Then, a methodology is proposed to choose the proper chopping technique and design a circuit to reach the highest sensitivity or the desired sensitivity with minimum power consumption in each gain and sensor capacitance. It is shown that the input capacitance of the signal conditioning circuit is important to achieve the best capacitance sensitivity, and this factor is considered in the analysis of the sensitivity of different chopping techniques for the first time. It is shown that the minimum sensitivity factor is achievable by the DCA structure. The DCA has the freedom of distribution of gain between the two stages. As a result, based on the value of sensor capacitance, DCA can be designed in a way that minimizes both the input noise floor and the input capacitance.

Based on the methodology, a novel circuit is designed to improve the sensitivity performance and minimize the power consumption in the signal conditioning circuit. In this design, a dual-path dual-chopper amplifier with two different supply voltages is proposed and fabricated in the GlobalFoundries 0.13μm CMOS technology. A low-noise low-supply voltage amplifier is implemented at the first stage. In this amplifier, high current and low supply voltage are implemented to minimize the power consumption and the noise at the same time. Then, the second stage includes two paths of two high gain amplifiers and each of them is chopped separately. Enabling of one path or two paths together is possible in this design to reach configurable gain. It is shown that utilising the dual paths helps to reach a higher gain and a higher SNR. A four-input g_m-C filter is utilized to add the signals from the two paths, which helps to reduce the switch-nonidealities which are produced in the two paths too.

In the last design, a signal conditioning circuit with the three stages and the triple-chopping is designed and simulated in the same 0.13 μm CMOS technology. The first stage is used to reach the low noise and low-input capacitance amplifier. The amplifier of this stage has a high current and low supply voltage to reach the low noise floor and the low power consumption. The

second and third stages are a resistive feedback amplifier and a capacitive feedback amplifier to attain low noise low pass filtering with a tunable bandwidth. The miller effect in the capacitive feedback amplifier helps to reach a bandwidth as small as 1 Hz without the need of a very large capacitance. A small bandwidth contributes to a lower integrated input noise and improves SNR. Since three blocks are chopped, there is no significant flicker noise in this circuit. The corner frequency of this circuit is 0.5 µHz and allows for near-DC high precision operation.

Main Contributions and Novelties of the Thesis

To the best of the author's knowledge, the first signal conditioning circuit which considers the effect of input capacitance on the methodology design is presented in this research work. Based on the above objectives and methodologies, the main contributions of this work are:

- Proposing a methodology to design an optimized signal conditioning circuit with a chopping technique based on the sensor capacitance and the required total gain. This methodology helps to design a circuit to reach the maximum possible sensitivity, or reach the desired sensitivity with the minimum power consumption.

- Design and fabrication of dual path-dual chopper amplifier. A low-noise and ultra-low power circuit is achieved. The power efficiency factor (PEF) of this circuit is 11 for the single-path circuit and 13 for the dual-path circuit, which indicates a good trade-off of noise and power consumption. The small power consumption of this circuit is 2.66 µW from the 0.7 V supply and 3.26 µW from the 1.2 V supply voltage. The noise floor achieved is of 25 nV/√Hz.

- Design and simulation of a low-power low-noise signal conditioning circuit with sub-µHz noise corner frequency and tunable bandwidth. This circuit has a low noise and a low power consumption. Simulation results show that with this circuit, a corner frequency of 0.5 µHz with a noise floor of 20.5 nV/√Hz is achievable. This structure helps to measure the signal around DC frequency. In addition, the bandwidth is tunable, and it can be set based on the application. A bandwidth as small as 1 Hz is achievable in this circuit, which helps to reduce the integrated input noise and improve the SNR. The power efficiency factor of 4 and SNR of 115.7 dB for the bandwidth of 100 Hz is achievable with this circuit.

Thesis Organization

The thesis has been divided into 6 chapters. The first chapter summarizes the literature review and the recent implemented architectures for relevant signal conditioning circuits. The most common implemented signal conditioning circuits are categorized, and their advantages and disadvantages, as well as common features, are be discussed.

Chapter 2 explains the important factors in the design of a signal conditioning circuit for MEMS. An overview of chopping technique is explained. A brief discussion of the papers that compose this thesis is done in this chapter, and their relevance to the Ph.D. work is described.

Chapter 3 is a methodology paper. In this paper, which was published in the Journal of Low Power Electronics and Applications in 2017, three different chopping techniques are considered, and their sensitivity and power consumption are extracted based on the required gain and sensor capacitance. Moreover, the proper chopping technique and the way of designing a chopping circuit to reach the optimum performance in each gain and sensor capacitance is shown in this paper.

In chapter 4, a dual-path dual-chopper amplifier with two supply voltages is designed and fabricated in the GlobalFoundries $0.13\mu m$ CMOS technology. This chapter is a paper that was published in IEEE Transactions on Circuits and Systems I: Regular Papers in 2019.

In chapter 5, a low-noise low-power signal conditioning circuit with configurable bandwidth and sub-μHz noise corner frequency for use in resistive and capacitive MEMS sensors that requires minimal capacitive loading is designed and simulated. This chapter is a paper that was submitted to IEEE Sensors Letters in 2019.

Finally, the overall results and the contributions are discussed in chapter 6. The conclusion and suggestions for future work are presented at the end of the thesis.

CHAPTER 1

LITERATURE SURVEY

1.1   Different electrical readout techniques

One of the most important parts of any sensor is a readout system capable of monitoring physical changes and converting them to an electrical signal. In this section, we discuss the details of sensor readout techniques that can be classified broadly as capacitive sensing and resistive sensing.

1.1.1   Capacitive sensing

Capacitive sensing is the dominant sensing mechanism in micro-electro-mechanical systems (MEMS) inertial sensors, since it has the advantages of low temperature coefficients, low power consumption, low noise, low cost and the potential of compatibility with integrated circuit (IC) fabrication technology. A simple configuration of capacitance is defined as shown in equation (1.1):

$$C = \varepsilon_r . \varepsilon_0 \frac{A}{g}$$

(1.1)

Where ε_r is the permittivity of the dielectric, ε_0 is the permittivity of vacuum, A is the overlapping area, and g is the distance. Capacitive sensors are designed to detect a signal based on changing the size of a gap (Baxter, 1997), overlap area (Baxter, 1997), or dielectric properties (Heidari, 2010).

In capacitive sensors based on changing the gap distance, the position is encoded as capacitance between two or more separate electrodes in the sense element. These capacitive sensors can be configured in different ways. One is a single variable capacitor where the

capacitive sensors are designed such that they have two fixed plates and one movable plate in the middle. With an external acceleration the movable plate is displaced from its nominal position. The physical sizes of the gaps between the plates are changed and contributes to two different values of capacitance. The principal design objective of this capacitive sensor is to efficiently convert mechanical displacements and hence capacitive changes into an electrical signal. The other configuration is a capacitive half bridge where one capacitor with a positive positional dependency and other with negative positional dependency are connected at a common mode. Typically the change in capacitance is first converted to a voltage and then it can be further processed with various signal-conditioning blocks or an analog to digital converters (ADC). Capacitive sensing is widely used in pressure sensors, liquid-level gauges, accelerometers and humidity sensors, and proximity and position sensors (1998; Lazarus, Bedair, Lo, & Fedder, 2010; H. Lee, Chang, & Yoon, 2009; Lin et al., 2008; Yazdi, Ayazi, & Najafi, 1998; Y. Zhang, Howver, Gogoi, & Yazdi, 2011).

1.1.2   Piezoresistive sensing

In piezoresistive sensors, the resistivity is changed by the application of a physical stimulus, and the resulting resistance variation is measured to detect the value of physical stimulus. The change in resistance equals to:

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \tag{1.2}$$

where R is the initial resistance, ΔR is the change in resistance, π_l and π_t are the longitudinal and transverse piezoresistive coefficients, respectively, and σ_l and σ_t are the lateral and transverse stresses, respectively. The resistance can change in response to stimulus in two different categories: changes to the geometry or changes to the conductive properties of the resistor. Typically, a Wheatstone bridge circuit is implemented in resistive sensing as shown in Figure 1.1.
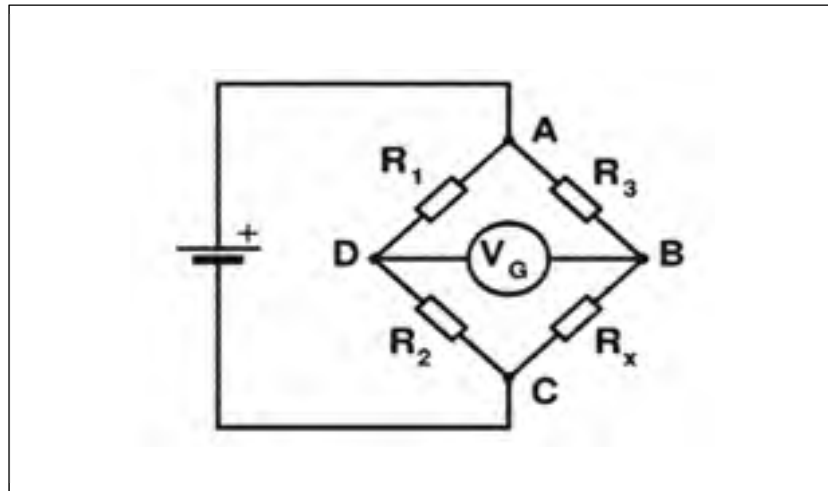
Figure 1.1 Wheatstone circuit taken from (Mutyala,
Bandhanadham, Pan, Pendyala, & Ji, 2009)

The output voltage is directly related to the change in the resistance with respect to the initial resistance R. The resistance change in the Wheatstone bridge is measured by the excitation voltage or current, and high excitation voltage or current is necessary for high bridge sensitivity, which results in high power consumption (Thanachayanont & Sangtong, 2007).

Piezoresitive sensors have a simple structure. They are tolerant to high shock conditions. They have low measurement uncertainty, and low nonlinearity and hysteresis error. However, they have more power consumption compared to capacitive sensors and they are more sensitive to temperature variations.

1.1.3   Comparison between methods by principle of output measurement

The advantages and disadvantages of capacitive and resistive sensors are shown in Table 1.1. Between the above-mentioned methods, capacitive sensing is preferred since it has the advantages of low temperature coefficients, low power dissipation, low noise, low-cost fabrication, and compatibility with VLSI technology scaling.

Table 1.1 Comparison of different readout techniques

	Advantages	**Disadvantages**
Capacitive sensing	• High sensitivity • Low temperature dependence • Capable of measuring very low frequency signals • Low power circuit interface • High temperature range • Compatibility with VLSI technology	• Low frequency range • More complex interface circuit
Resistive sensing	• Simple interface • High shock tolerance • Medium frequency range	• Low sensitivity • Higher power consumption • Temperature dependence •

1.2 Literature survey of signal conditioning circuits

After detecting a signal in a sensor, the signal should be amplified in a signal conditioning circuit. Figure 1.3 shows the classification of signal conditioning circuits based on their outputs. As shown in this figure, output can be analog, semi-digital, and digital. Analog output can be achieved by discrete time or continuous time architectures. In a discrete time architecture, switched capacitor amplifiers are usually implemented. For continuous time amplification, an input stimulus is converted to a voltage or current and then amplified. Architecture such as chopping can be utilized in continuous time amplification to improve the performance of the circuit. Another category of amplification of the signal is based on the architecture that produces a semi-digital output. This category includes pulse-width

modulation and frequency modulation. To produce a digital signal at the output, an analog signal can be converted to digital signal using an analog to digital converter or digitalizing a semi-digital signal.

In the design of a signal conditioning circuit, power, noise, and sensitivity are the three most important challenges that should be considered. Regarding the application, the output signal can be digital, analog or semi-digital. In the following, the methods to produce these kinds of outputs are briefly described, and at the end, the advantages and disadvantages of each will be explained.
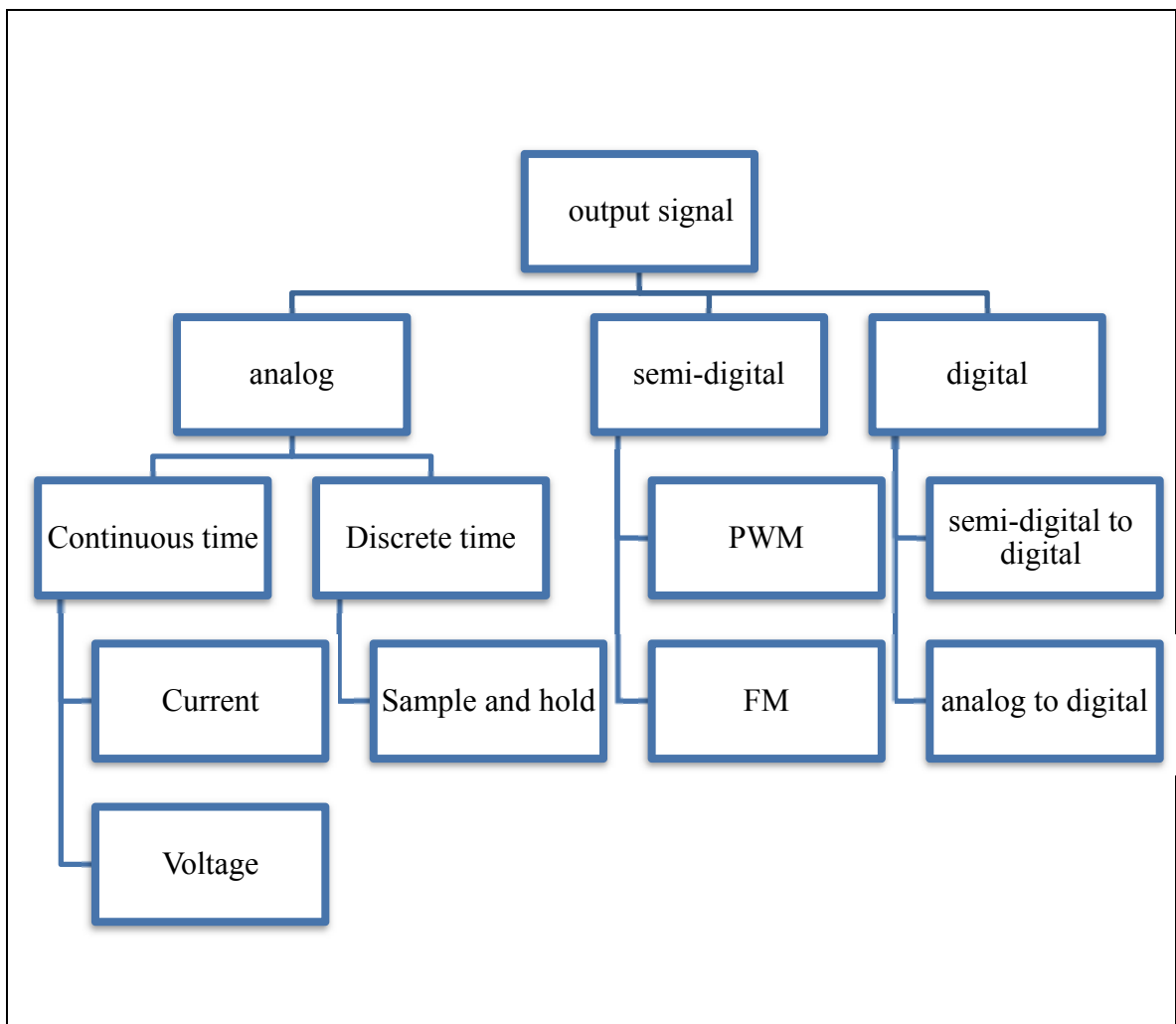
Figure 1.2 Classification of signal conditioning circuit based on the output type

1.2.1 Techniques to produce an analog output signal

An analog output signal from a signal conditioning circuit can be obtained by either continuous time or discrete time methods. Switched capacitor circuits are used in discrete time methods to amplify the detected signal. In the continuous time architecture, a detected signal is amplified in either voltage or current mode. Because of the low frequency range of the input signal, chopper modulation is often implemented in continuous time methods. Some of the state-of-the-art design of signal conditioning circuits with analog outputs are described in the following sections.

1.2.1.1 Discrete time signal conditioning circuit

A switched capacitor circuit can be implemented in a signal conditioning circuit to move the charge in the sensor to the output. In the switched capacitor circuit, the sensing and reference capacitors are charged with opposite polarity voltages, which causes charge to propagate due to the voltage created by the difference of the capacitances to the output. A model of switched capacitor circuit is shown in Figure 1.3.
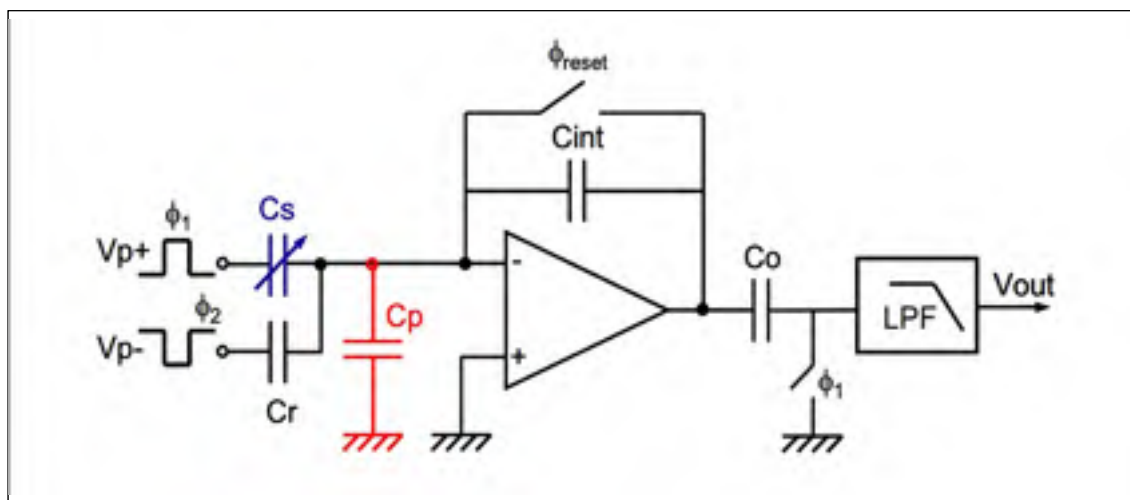
Figure 1.3 Switched capacitor circuit, taken from (Yazdi, Kulah, & Najafi, 2004)

$$V_{out} = V_P \frac{\Delta C}{C_{int}}$$

<div align="right">(1.3)</div>

Where ΔC is the capacitance difference between C_s and C_r are the sensing capacitance and reference capacitance, respectively, V_p is the excitation voltage, and C_{int} is the capacitance of the feedback capacitor.

The switched capacitor circuit provides a virtual ground and robust dc biasing at the sensing nodes. As a result, the sensing node is insensitive to parasitic capacitances and undesirable changes (Reddy, 2011). Moreover, the switched capacitor circuit is insensitive to the temperature (Aezinia, 2014). This architecture is implemented in works such as (Chavan & Wise, 2000; Kajita, Un-Ku, & Temes, 2002; Kulah, Junseok, Yazdi, & Najafi, 2003; M. Lemkin & Boser, 1999; M. A. Lemkin, 1997; Lu, Lemkin, & Boser, 1995; Ogawa, Oisugi, Mochizuki, & Watanabe, 2001; Ranganathan, Inerfield, Roy, & Garverick, 2000; Smith, Nys, Chevroulet, DeCoulon, & Degrauwe, 1994). The main disadvantages of a switched capacitor is a high noise floor, which is caused by high kT/C noise at low capacitance, high thermal noise if resistive MOS switches are implemented, and noise folding (Jiangfeng, Fedder, & Carley, 2004). In addition, they need a precise design of non-overlapping clock (Aezinia, 2014).

To reduce the kT/C in switched capacitor circuit, correlated double sampling (CDS) is utilized (Du et al., 2015; Du et al., 2017; Ranganathan et al., 2000) . Although CDS reduces the kT/C noise, noise folding and the thermal noise of resistive MOS switches still exist. In conclusion, the discrete time method is not preferred for high resolution signal conditioning due to its noise performance being worse than other methods.

1.2.1.2   Continuous time signal conditioning circuit

In continuous time sensing, there are two ways to measure the signal at the output: continuous time voltage sensing and continuous time current sensing. In voltage sensing, the physical

sensed signal is converted to a voltage and then amplified, while in the current sensing mode, the physical sensed signal is converted to a current and then amplified.

At low frequencies, flicker and offset are the dominant sources of noise in CMOS technology, and to achieve high sensitivity, it is important to remove them properly. Two methods are implemented in continuous voltage sensing to remove the flicker noise: auto zeroing and chopping. In auto zeroing, flicker noise is removed but the noise floor is increased because of noise folding (Enz & Temes; Rong Wu, Huijsing, & Makinwa, 2013). As a result, chopping is generally preferred in low-noise continuous time voltage sensing. The architectures of circuits using current sensing and voltage sensing are explained in the following sections.

1.2.1.2.1   Continuous time current-mode signal conditioning circuit

A current-mode signal conditioning circuit converts the capacitance difference to a current (Singh, Saether, & Ytterdal, 2009). A block diagram of a capacitance-to-current signal conditioning circuit is shown in Figure 1.4. In this figure, C_m and C_r represent the sensor capacitance and fixed capacitance, respectively. Both of these capacitances have the same nominal value. At zero, the charging current (I_b) splits equally between these two capacitances,
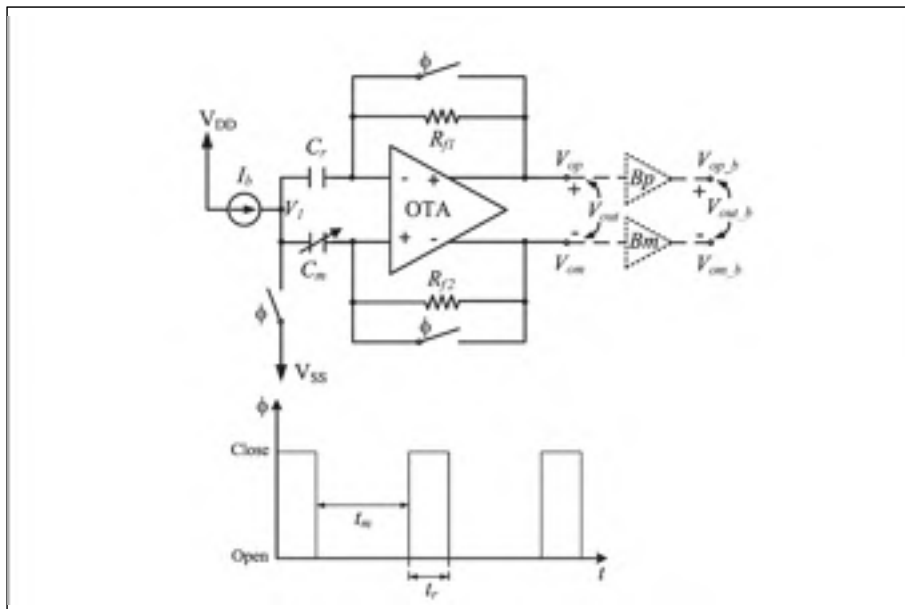
Figure 1.4 Block diagram of a capacitance-to-current signal
conditioning circuit taken from (Singh, Saether, & Ytterdal, 2009)

but with changes in the value of C_m the distribution of current between the two paths is altered. The current is converted to a voltage by a resistive feedback amplifier. The output voltage of this amplifier is proportional to

$$|V_{out}| = V_{op} - V_{om} = R_f.i = R_f.i = R_f I_b \frac{\Delta C}{2C + \Delta C} \tag{1.4}$$

Where R_f is the resistive feedback, C is the nominal capacitance, and ΔC is the difference between the sensor capacitance (C_m) and reference capacitance (C_r).

The advantages of current mode sensing is that adding signals as currents is simple. A current-mirror-like scheme can be applied for improving the sensitivity while also simplifying the circuit (Haider et al., 2008). However, the disadvantage of this scheme is that nonlinearity can be produced by current leakage from the switches. Moreover, the parasitic capacitance at the common node electrode should be significantly smaller than the sensing capacitance to prevent degrading the performance (Banitorfian & Soin, 2011; Marcellis, Carlo, Ferri, & Stornelli, 2009; Pennisi, 2005; Scotti, Pennisi, Monsurrò, & Trifiletti, 2014; Singh et al., 2009).

1.2.1.2.2 Continuous time voltage-mode signal conditioning circuit with chopper stabilized amplifier

A chopper-stabilized amplifier is generally preferred in continuous time voltage-mode signal conditioning method. In a chopper stabilized amplifier, the desired signal is modulated to a higher frequency, amplified, and then demodulated (Bakker, Thiele, & Huijsing, 2000; Enz & Temes, 1996; Enz, Vittoz, & Krummenacher, 1987). In this fashion, the DC offset and flicker noise are decreased significantly (Enz et al., 1987). Figure 1.5 shows the chopping amplifier with its ideal waveform. To remove the flicker noise effectively, the chopper frequency should be larger than the flicker noise corner frequency.
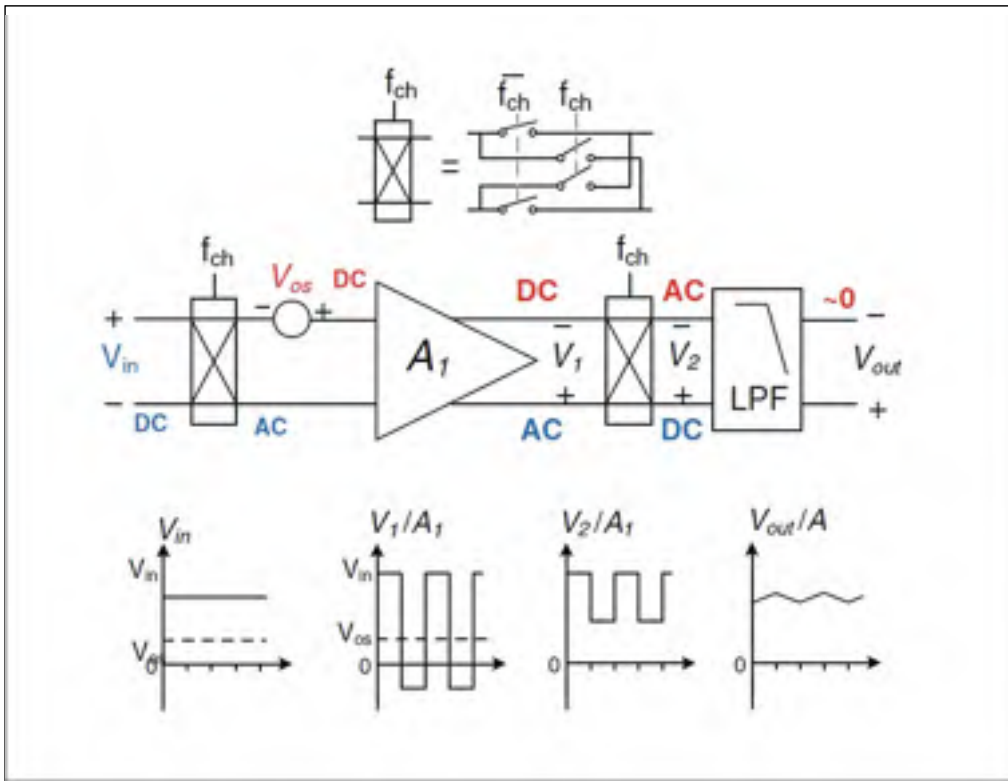
Figure 1.5 Chopping principle, taken from (Rong Wu,
Huijsing, & Makinwa, 2013)

Although the chopping amplifier suppresses flicker noise, it is not an energy efficient technique. In (Fang, Qu, & Xie, 2006; Qu, Fang, & Xie, 2008; H. Sun et al., 2011), dual chopper amplifier (DCA) is implemented. In (H. Sun et al., 2011), a dual chopper amplifier design is proposed to minimize the power consumption and noise by chopping the sensed signals at two different clock speeds, the design of which is shown in Figure 1.6. The first clock is at a high frequency to remove the flicker noise while the second clock is at a significantly lower frequency to keep the unity gain bandwidth low. The optimized gain of the first amplifier to reach the minimum power consumption is given in Equation 1.5:

$$G_{H-opt} = \sqrt{\frac{3f_L C_L (W_H / L_H)^{\frac{1}{2}}}{f_H C_H (W_L / L_L)^{\frac{1}{2}}}} . \sqrt{G} \qquad (1.5)$$
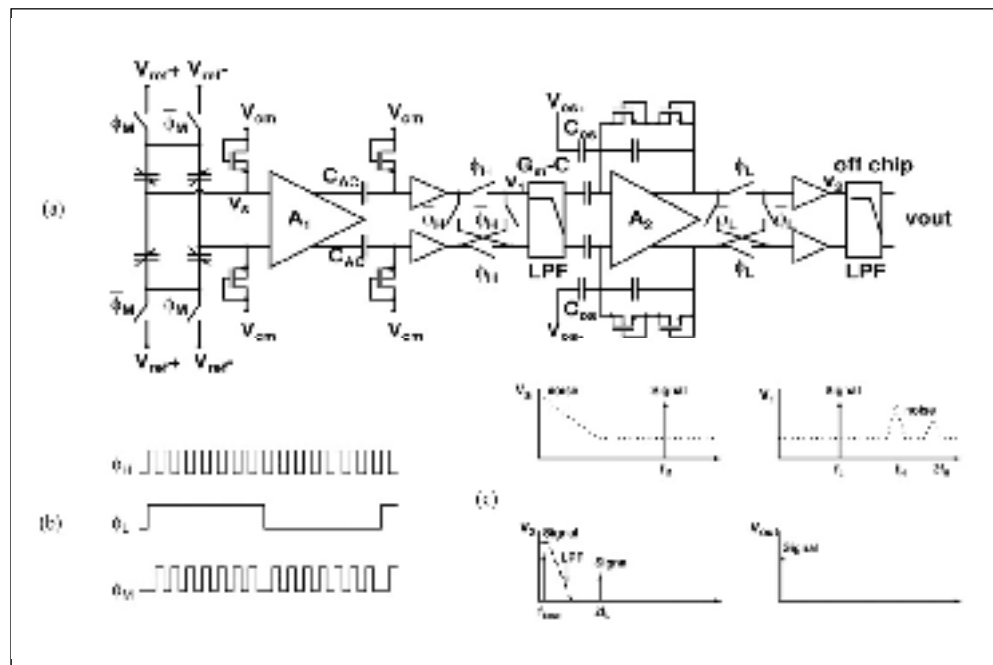
Figure 1.6 Dual chopper amplifier proposed in (H. Sun et al., 2011)

Where f_L and f_H are the second chopping frequency and first chopping frequency, respectively, C_L and C_H are the load capacitances of the second amplifier and first amplifier, respectively, W_L/L_L is the ratio of the width to length at the input to the transistor of the second amplifier, W_H/L_H is the same ratio but in the first amplifier, and G represents the total gain of the circuit. In the equation (1.5) it is assumed that the noise from the first amplifier is dominant over the noise from the second amplifier, and so the noise produced by the second amplifier is not considered in that formula. This circuit is optimized for the parasitic capacitances, while the effect of the capacitance of the input transistor is not considered in the optimization. The effect of this transistor will degrade the performance of the sensor capacitance while the sensing capacitance is small.

As explained above, in a DCA two different frequencies are implemented to chop at two stages. Thus, there is a freedom of distribution of gain between the two stages that contributes to a reduced power consumption compared to a single chopper amplifier design. The drawbacks of this chopping technique is that clock non-idealities, such as charge injection and residual offset,

can degrade the performance. To remove clock non-idealities and improve the performance, a careful design of the clock is essential. Implementing properly designed switches, such as dummy or complementary switches, will improve the performance. Moreover, this chopping technique can be combined with other techniques such as the capacitively coupled technique (Denison et al., 2007; Fan, Huijsing, & Makinwa, 2012; Fan, Sebastianen, Huijsing, & Makinwa, 2010; Fan, Sebastiano, Huijsing, & Makinwa, 2011; P. Sun, Zhao, Wu, & Fan, 2012; R. Wu, Makinwa, & Huijsing, 2009), a ripple reduction loop (Kusuda, 2009, 2010; P. Sun, Zhao, Wu, & Fan, 2012; Yazicioglu, Merken, Puers, & Hoof, 2008), correlated double sampling (Belloni, Bonizzoni, Fornasari, & Maloberti, 2010; Belloni, Bonizzoni, Maloberti, & Fornasari, 2010; Enz & Temes, 1996; Shiah & Mirabbasi, 2014), the auto-zeroing technique (Witte, Makinwa, & Huijsing, 2007), and the multi-path chopping technique (Fan, Huijsing, & Makinwa, 2013; Fan, Huijsing, & Makinwa, 2012).

As a result, the combination of a DCA with other techniques could be an effective way to reach a low-power, high-sensitivity signal conditioning circuit.

1.2.2   Semi-digital signal conditioning circuit

A semi-digital output can be achieved with pulse-width modulation (PWM) or frequency modulation (FM). The principle of these two conditioning architectures are described in the following sections.

1.2.2.1   Frequency modulation based signal conditioning circuit

Capacitance-to-frequency converters have simple and straightforward structures. They usually use relaxation oscillators (Coskun et al., 2013; J. Zhang, Zhou, & Mason, 2007) or ring oscillators (Kyriakis-Bitzaros, Stathopoulos, Pavlos, Goustouridis, & Chatzandroulis, 2011; J. Zhang et al., 2007) to convert the capacitance to the frequency. Moreover, crossed-coupled oscillators (M. Shamsul Arefin et al., 2014; M. S. Arefin, Redouté, & Yuce, 2016b; Hua, Yan, Hassibi, Scherer, & Hajimiri, 2009; Wang, Weng, & Hajimiri, 2013) can be implemented to provide highly stable and lower phase-noise output frequencies for specific applications.

A block diagram of a capacitance-to-voltage circuit with frequency modulation (FM) is shown in Figure 1.7. A voltage-controlled oscillator (VCO) is implemented to convert the capacitance or inductive variation to the frequency. A sine-to-square circuit (STS) is implemented to convert the frequency variation to a time variation, and a frequency-to-voltage converter (FVC) circuit is used to convert the ΔT_{VCO} to the voltage changes. The FVC is implemented to convert an oscillation into a measurable voltage (M. Shamsul Arefin et al., 2014). The two main approaches for the implementation of FVC blocks are counter-based circuits (Hou, 2004; Kyriakis-Bitzaros et al., 2011) and integrator-based circuits (Bui & Savaria, 2008; Djemouai, Sawan, & Slamani, 2001).
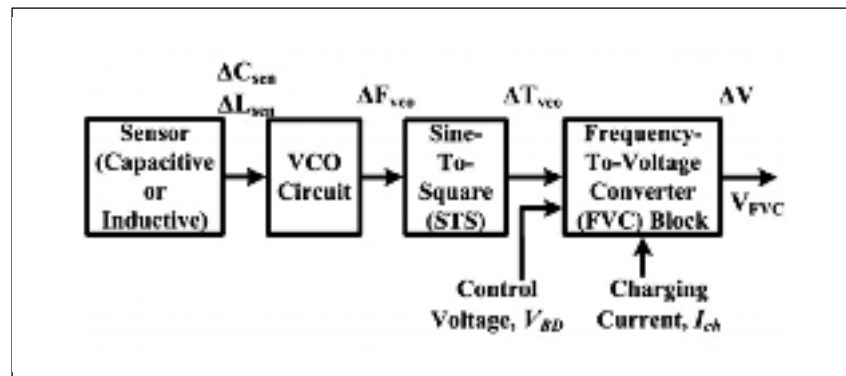
Figure 1.7 Block diagram of capacitive (or inductive)
sensor to voltage with FM circuit taken from (M. S. Arefin,
Redouté, & Yuce, 2016)

The benefits of using frequency-based modulation are reduced phase, flicker, and white noises at higher frequencies (Ko, Tseng, & Lu, 2006; Mohammadi, Yuce, & Moheimani, 2012; Wang et al., 2013). However, FM circuits consume more power than current-to-voltage converter circuits (Bui & Savaria, 2008; Djemouai et al., 2001). Moreover, non-idealities such as parasitic capacitances, and feedback through air and track paths result in undesirable oscillations and degrade the performance of the overall circuit (Awad, 1988; Tyagi & Sumathi, 2017; Yili, Song, Nakayama, & Watanabe, 2000).

1.2.2.2   Pulse-width modulation based signal conditioning circuit

Pulse-width modulation (PWM)–based capacitive sensors are based on relaxation oscillators whose output period is proportional to the variation of the sensor capacitance. The operating principle of PWM circuits is reported in (Heidary & Meijer, 2008; Heidary, Shalmany, & Meijer, 2010; Tan, Shalmany, Meijer, & Pertijs, 2012), and Figure 1.8 shows a diagram of a signal conditioning circuit that converts capacitance to a pulse-width signal. In this structure, two phases are implemented. At phase $\varnothing_1$, V_{drive} is connected to a supply voltage, and the output of the integrator steps down because of the amount of charge $V_{int}C_x$ is transferred to C_{int}, and then rises smoothly since a sinking current $I_{int,n}$ discharges from C_{int}. To detect the moment that V_{int} returns to its initial value, a comparator is used. At that moment, the phase triggers to the phase $\varnothing_2$. During $\varnothing_2$, V_{drive} is pulled to V_{ss} and a sourcing current $I_{int,p}$ charges C_{int} as in the previous phase, but with an opposite polarity. This process will repeat N times, and the time period of this process is (Y. He, 2014) given by

$$T = \frac{2NV_{dd}C_x}{I_{int}} \tag{1.6}$$
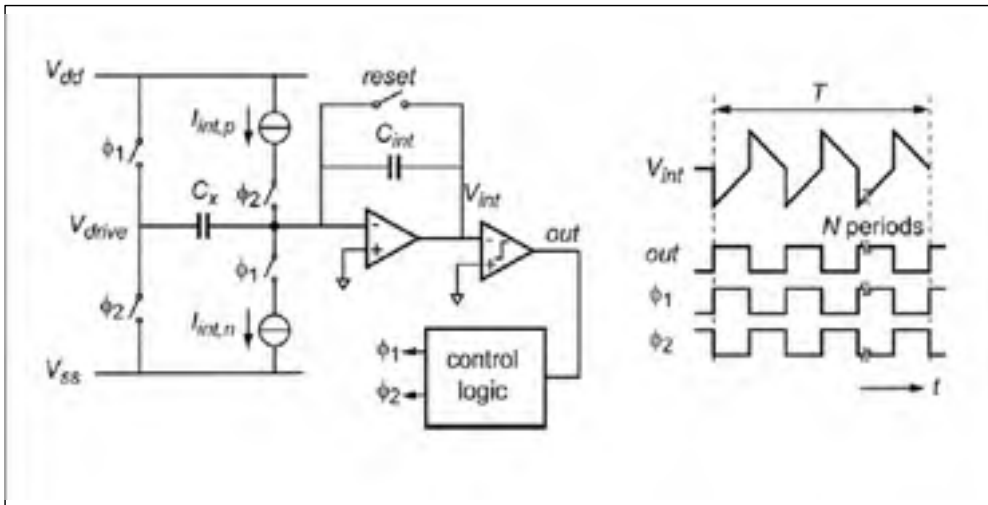
Figure 1.8 Typical ring oscillator for the measurement of a
capacitive sensing element in pulse-width modulation, taken
from (Y. He, 2014)

Where T is the clock cycle, V_{dd} is the supply voltage, and C_x is the sensor capacitance. By counting the clock cycles the sensor capacitance of C_x will be defined.

Pulse-width modulation can be designed to have relatively high resolution and handle a very large input capacitance range (Heidary & Meijer, 2008; Meijer & Iordanov, 2001). Interfaces that are based on relaxation oscillators are operated asynchronously and thus do not require a clock signal. Period-modulation-based capacitive sensor interfaces can be quite flexible, and, by using a sample digital divider, they can be simply converted to measurement time by counting the duration of multiple output periods (Heidary et al., 2010; Xiujun & Meijer, 2002). However, the power consumption is high in this implementation and are therefore not suitable for use in energy-constrained applications (Pertijs & Tan, 2013). To reduce the power consumption, the pulse-widthmodulation is combined with other techniques such as negative-feedback loops (Heidary & Meijer, 2008; Meijer & Iordanov, 2001), piece-wise charge transfer techniques (Y. He, Chang, Pakula, Shalmany, & Pertijs, 2015), and chopping and three-signal auto-calibration techniques (Tan et al., 2012). The output of PWM is strongly dependent on MOSFET transconductance, parasitic capacitance, and resistance values (M. S. Arefin, Redouté, & Yuce, 2016a; Bruschi, Nizza, & Piotto, 2007).

1.2.3   Digital output

To produce a digital output, analog-to-digital converters (ADCs) can be implemented to convert the voltage to a digital signal. These ADCs include successive approximation register (SAR) analog-to-digital converters (Brenk et al., 2011; Hsieh & Hsieh, 2018; Hwang, Park, Song, & Jeong, 2018; Mao, Li, Heng, & Lian, 2018; Sadollahi, Hamashita, Sobue, & Temes, 2018; D. Zhang, Bhide, & Alvandpour, 2012; Zou, Xu, Yao, & Lian, 2009) and $\Delta\Sigma$ modulators (Jung, Duan, & Roh, 2017; Park, Cho, Na, & Yoon, 2018; Rout & Serdijn, 2018; Sanyal & Sun, 2017). Successive approximation register (SAR) ADCs have low power consumption and moderate resolution (Hariprasath, Guerber, Lee, & Moon, 2010; Liu, Roermund, & Harpe, 2017; Tai, Hu, Chen, & Chen, 2014). $\Delta\Sigma$ modulators are suitable for high resolution applications, but have low energy efficiency (Paavola et al., 2007; Shin, Lee, & Kim, 2011;

Tan et al., 2013). Semi-digital-to-digital converters include frequency-to-digital convertors (Brookhuis, Lammerink, & Wiegerink, 2015; Cardes et al., 2018; Chiu, Hong, & Wu, 2013; Elhadidy, Shakib, Krenek, Palermo, & Entesari, 2015) and time-to-digital convertors (Danneels, Coddens, & Gielen, 2011; S. Lee et al., 2007). Time-to-digital convertors have a simple structure (e.g., counters), but usually they do not have a high resolution as their iterative discharging process requires 2^N cycles for N-bit resolution (Sanyal & Sun, 2017). The frequency-to-voltage convertors that VCO has implemented suffer from non-linearity problems and have a high sensitivity to process, voltage, and temperature (PVT) variations (Sanyal, Li, & Sun, 2018). Digital output can also be achieved by using the combination of frequency-to-voltage converters and ADCs (Elhadidy, Elkholy, Helmy, Palermo, & Entesari, 2013; Gaggatur, Dixena, & Banerjee, 2016; Helmy et al., 2012; Matsumoto & Esashi, 1993).

1.2.4   Comparison of different application areas

In this section, a review of different application areas and the requirements of sensor circuits implemented in those areas is given. As discussed previously, MEMS applications work in a low frequency range of up to a few kHz, and circuits applied here also need to have high resolution and a low-power signal conditioning circuit is necessary to detect small variations in the sensors. Each architecture for signal conditioning circuits has its benefits and limitations, and the most important of these are shown in Table 1.2. Among these architectures, the chopping technique is a well-suited option for low noise and low frequency applications.

Moreover, the power consumption of the chopping technique could be decreased significantly with the proper design of a dual chopper amplifier. The limitation of the chopper technique is that it is sensitive to clock non-idealities, and the input capacitance of the circuit can degrade the sensitivity performance. With a combination of the dual chopper technique with other techniques such as a ripple reduction loop, multi-path circuits, switch non-idealities can be decreased. Furthermore, the dual chopper amplifier gives us the freedom to design a circuit with a minimum input capacitance that also contributes to maximize the sensitivity during capacitive sensing.

Table 1.2 Summary of advantages and disadvantages of
different signal condition circuit

	Advantages	**Disadvantages**
Switched Capacitor	• Insensitive to parasitic capacitance	• High noise floor because of the noise folding • Need higher bandwidth • Need techniques to suppress offset and low frequency
Chopper stabilized amplifier	• Eliminating offset and flicker noise • Power reduction with DCA	• Non-idealities problem: charge injection, clock feed-through and jitter.
Pulse width modulation	• Robustness against environmental noise , • Dynamic range is not limited by the supply voltage or currents • Relatively high resolution • Handle very large input capacitance range	• Output affected by temperature and process variations • High power consumption
Frequency modulation	• Less prone to amplitude noise • Having lower phase, flicker, and white noises at higher frequencies	• Output affected by large temperature and process variations • High power consumption

CHAPTER 2

DESIGN CONSIDERATIONS OF SIGNAL CONDITIONING
CIRCUITS FOR CAPACITIVE AND RESISTIVE SENSORS

The goal of this work is designing a signal conditioning circuit to be applicable for MEMS sensors. This circuit should be able to read signals from both capacitive and resistive sensors. At the MEMS transducer, a physical stimulus is converted to an electrical signal, and the electrical signal is amplified in the signal conditioning circuit. To have a proper MEMS sensor, the transducer, signal conditioning circuit, and their integration should work well to have a high performance circuit. The design of the MEMS transducer is not the scope of this work. However, by considering the characteristics of the MEMS transducer, the signal conditioning circuit is designed to maximize the performance.

The detected signal from the MEMS transducer could be as small as atto Farads in the capacitive sensor, and as small as micro volts in the resistive sensor for a frequency range of up to a few kHz. As a result, the signal conditioning circuit must have the capability of reading a low-amplitude low-frequency signal, and then amplify it properly to be suited to more processing. As a result, the input noise of the signal conditioning circuit should be smaller than the detected signal by the MEMS transducer. On the other hand, when a signal conditioning circuit is added to the capacitive sensor, it adds some parasitic capacitance to the transducer, and, based on the value of sensor capacitance, this parasitic could degrade the performance. The smaller sensor capacitance, the more important the input capacitance of signal conditioning circuit is.

In other words, the signal could not be readable even with a very low noise signal conditioning circuit that has a large input capacitance. As a result, both the input noise and the input capacitance should be minimized. As the frequency range of signal conditioning circuit is from DC to few kHz, the dominant noise is the flicker noise. The formula of flicker noise for a CMOS transistor equals to:

$$V_f = \frac{k_f}{C_{ox}WLf} \tag{2.1}$$

In the oxide capacitance, W and L are the width and the length of the transistor, respectively and k_f is the flicker noise coefficient. With increasing dimension of the transistor, flicker noise is decreased. However, to have a low input noise in low frequencies, a technique should be implemented to suppress the flicker noise completely. Among the different techniques to remove the flicker noise, the chopping technique is preferable. In this technique, the signal is modulated to the higher frequency, amplified and then demodulated to the baseband as shown in Figure 2.2. As a result, flicker noise can be suppressed completely.
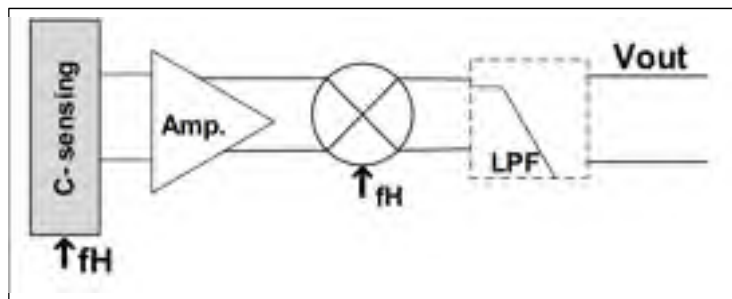
Figure 2.1 Single chopper amplifier structure

There are many constraints that should be considered in the design of a chopper amplifier. The most important of them is choosing the proper chopper frequency. To prevent the flicker noise down-folding, the chopping frequency should be larger than the corner frequency (Nielsen, 2004). Figure 2.3 shows the percentage of increasing noise floor regarding the ratio of chopping frequency to corner frequency. As shown, the chopping frequency should be at least ten times larger than the corner frequency to have less than a 10% increase in the noise floor. On the other hand, the chopping frequency should be in the bandwidth range not to degrade the signal amplitude. As a result, larger chopping frequency demands larger bandwidth that contributes to more power consumption.
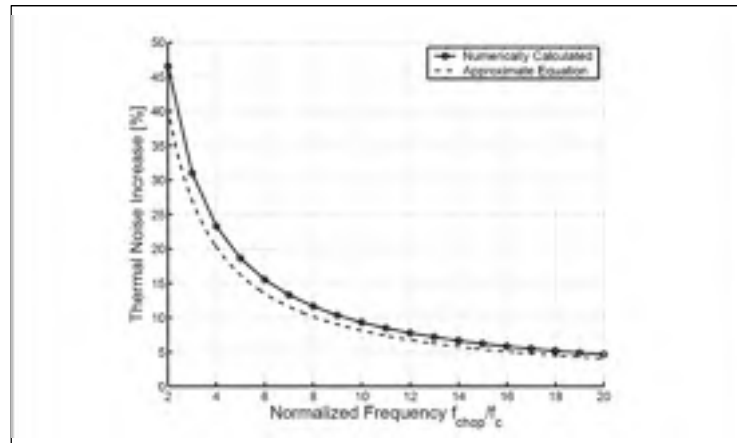
Figure 2.2 Thermal noise increase based on
normalized frequency f_{chop}/f_c, taken from
(Nielsen, 2004)

In addition of flicker noise, a careful design should be done to minimize the thermal noise. The thermal noise of a CMOS transistor equals to:

$$V_n = \frac{4kT}{g_m} \tag{2.2}$$

where k is Boltzmann's constant, T is the absolute temperature, and g_m is the transconductance, which can have a value that is different in the subthreshold and saturation region. At the saturation region, to reduce the thermal noise, transconductance of transistor should be increased which means more current and larger ratio of W/L. However, a larger ratio of W/L contributes to a larger dimension for the transistor and will increase the input capacitance. Because of the limitation in power consumption and input capacitance of a single-chopper amplifier, a dual-chopper amplifier is proposed as shown in Figure 2.4. As shown in this architecture, two different chopping frequencies are implemented to chop two amplifiers. In the dual-chopper amplifier, the signal is chopped with a high frequency modulator, then amplified, and subsequently, it will be chopped with another chopping frequency to send it to the lower frequency, and then will be amplified again at the second amplifier. At last, it is demodulated to the baseband. This structure gives a greater degree of freedom, and with the

proper distribution of the gain between the two stages, it can be optimized for noise, power consumption, and power-noise factor.
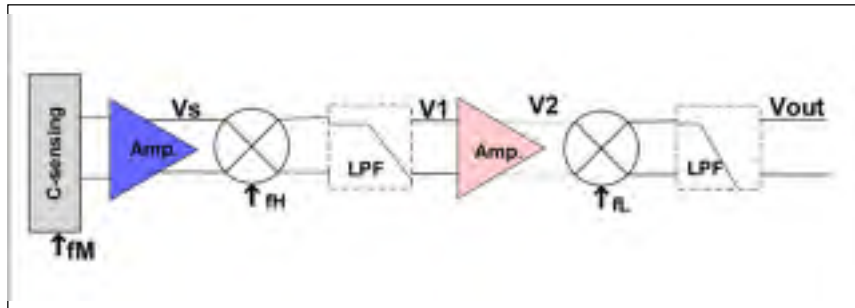
Figure 2.3 Dual chopper amplifier structure

2.1 Chopping amplifier signal conditioning circuit in resistive sensors

In the design of a signal conditioning circuit, in resistive sensors, the input noise of the circuit is important with regards to the performance. However, the input capacitance is not an issue in this kind of sensing. As a result, to have a high resolution circuit, the input noise should be reduced as much as possible.

Another factor that should be considered in the design is power consumption. There is a trade-off between noise and power consumption. Distribution of the gain between the two stages in DCA gives us a greater degree of freedom, and it could contribute to a smaller power consumption than the SCA. Thus, regarding the total gain, there is an optimal distribution of gain between the amplifiers in DCA to reach the minimum noise, power consumption, or power-noise factor. Figure 2.5 shows the normalized power-noise factor in DCA based on the variation of the gain of the first amplifier. The overall gain of the DCA is considered to be 40 dB, and $G_{H\text{-}opt}$ is the gain of the first amplifier to reach the minimum power-noise factor. As shown, based on the value of the gain, the contribution of each stage in total noise and power consumption is different, and it could change the result significantly.
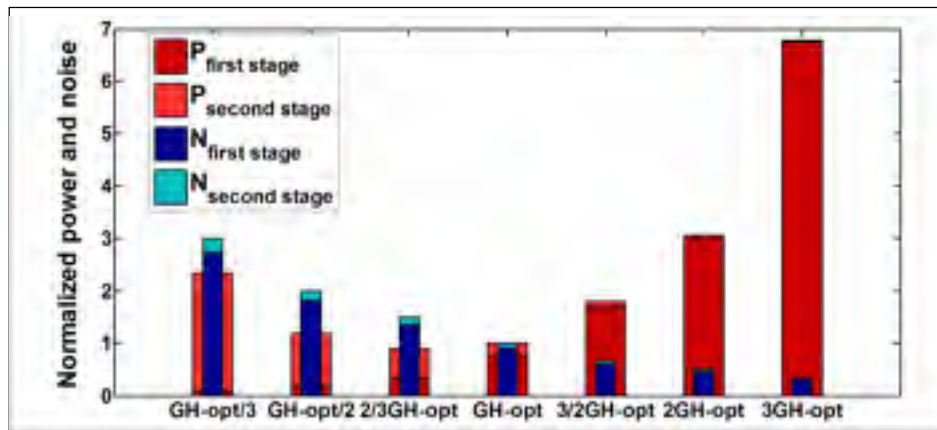
Figure 2.4 Normalized power consumption and input-referred
noise of each stage of the DCA vs. the gain of first stage
(overall gain set to 40 dB).

In addition to the distribution of the gain, the ratio of chopping frequencies is important on the
DCA performance. Figure 2.6 compares the performances of the single- and the dual-chopper
amplifiers by plotting the ratio of the power-noise product of the SCA and the power-noise
product of the DCA vs. the overall gain, G, and R_f given by

$$R_f = \frac{f_H}{f_L} \tag{2.3}$$

Where f_H is the chopping frequency of the first amplifier, f_L is the chopping frequency of the
second amplifier. The region where the SCA has a better power-noise product than that of the
DCA is outlined in blue in Figure 2.6. Conversely, in the region where the ratio is above 1, the
DCA attains a better power-noise product than the SCA. When R_f is low, the SCA always
exhibits a better performance independent of the value of G. When R_f and the overall gain is
increased, the DCA provides a better performance. In this region, the power-noise product of
the DCA will be improved over that of the SCA by a factor of G, the overall gain. As such,
with an appropriately designed R_f, the DCA yields increasingly better power-noise
performance as the total gain is increased.
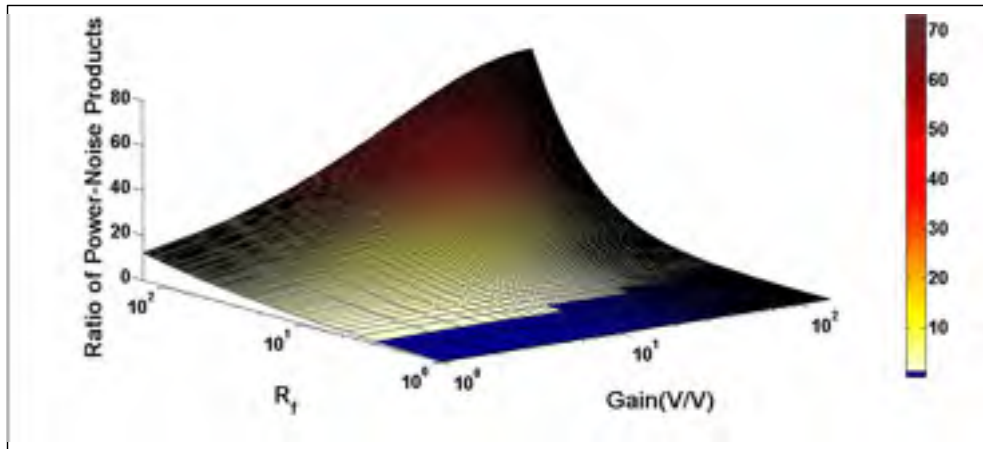
Figure 2.5 Preferred chopping technique (SCA or DCA) depending on
the overall required gain and R_F value.

2.2   Design of signal conditioning circuit for capacitive sensing

The design of a signal conditioning circuit for the capacitive sensing is more challenging. In this design, the input capacitance of the signal conditioning circuit should be considered, as it makes the design of the circuit more complicated. In this kind of signal conditioning, the circuit should be optimized for the noise, input capacitance and power consumption. As explained, to remove the flicker noise, a chopping technique is the best choice. Also to be able to remove the flicker noise properly, chopping frequency should be chosen carefully and it should be at least 10 times larger than the corner frequency. A large chopping frequency necessitates a larger bandwidth for the circuit which demands a higher power consumption. However, the corner frequency of a MOS transistor has a direct relationship with transconductance of the transistor and inverse relationship with the dimension of the transistor. To reduce the corner frequency, dimension of the transistor should be increased, as it causes a larger input parasitic capacitance, and it degrades the performance of the capacitive sensing. As a result, the chopping technique will remove the flicker noise, but there is a trade-off between the noise floor, the power consumption, and the input parasitic capacitance. A careful design is necessary to remove the flicker noise and optimize the power consumption and the sensitivity at the same time. As a result, it is important to find the best chopping technique and the best way of designing based on the required specifications for the capacitive sensing.

In our work, different analyses, simulations and measurements are done to propose a low-noise, low-power, and high-sensitivity signal conditioning circuit which is applicable in both capacitive and resistive sensors and the results are explained in three papers, which are reproduced in the following chapters.

The first paper (chapter 3), which is published at the Journal of Low Power Electronics and Applications, discusses the methodology of designing the chopping circuits. In this paper, three chopping techniques of single-chopper amplifier (SCA), dual-chopper amplifier (DCA), and two-stage single-chopper amplifier (TCA) are considered, and the sensitivity factor and power consumption for these three chopping techniques are calculated. The parameters related to the sensitivity factor are determined in this work. It is shown that the input noise and the input parasitic capacitance are the important factors to define the sensitivity. Sensitivity for different total gains and sensor capacitances are extracted in each chopping technique. Moreover, the minimum sensitivity for each technique based on the gain and the sensor capacitance is calculated. Then, a methodology to reach the maximum sensitivity in each chopping technique is described. As shown, designation of the amplifier and distribution of the gain in the TCA and DCA are the important factors to reach the highest sensitivity or the minimum power consumption for the desired sensitivity. It is shown that the DCA has the highest sensitivity and is the most suitable for a small sensor capacitance and large required gain.

Based on these results, a DCA structure is chosen to reach the lower noise floor and the lower power consumption at the same time. In addition, some other techniques are combined with DCA to improve the performance.

To reach the higher SNR and the lower power consumption, a novel circuit is proposed and fabricated in the 0.13 μm CMOS technology. Its measurement result is presented in a paper that is published in the IEEE Transactions on Circuits and Systems: TCAS-I Regular Papers (chapter 4). In this circuit, a dual-chopper and a dual-path signal conditioning circuit is presented to reach ultra-high sensitivity and ultra-low power consumption. The noise performance and the SNR improvement are explained in detail in this paper.

At the first stage of this circuit, an amplifier with low supply voltage and high current is implemented. This structure results in a lower noise floor and a lower power consumption at the same time. The second stage is designed to work in a single-path or a dual-path mode. In the dual path mode, a higher gain and a higher SNR are achievable. The amplifiers at the second stage are chopped to remove the flicker noise. These two paths are added together by an adder, which is a four-input fully differential g_m-C filter. A g_m-C filter is used at the end to remove the up-converted flicker noise and harmonics. The noise performance, frequency response, SNR, and THD of this circuit for single-path and dual-path are presented, and these results are compared to other works. It is shown that the power consumption of this circuit is significantly lower than the similar works. Moreover, the input capacitance of the circuit is minimized to be suitable for high-sensitivity fully-integrated capacitive mode sensors.

To be able to detect the small signal at the sub-milli Hertz range and having a low power consumption, an architecture is proposed in the third paper (chapter 5), which is submitted in the IEEE Sensors Letters. In this work, a circuit is presented wherein three different chopping frequencies are implemented to remove the flicker noise of the three different stages. The first stage of this circuit is a low-supply voltage and high-current amplifier to reach a low-noise floor and a low-power consumption. The second stage is a resistive feedback amplifier that is chopped, and the third stage is a capacitive feedback amplifier. The amplifier of this stage is chopped as well. With benefiting the Miller effect at the third stage and utilising capacitive bank at the feedback, a configurable bandwidth is achievable. This design helps to decrease the integrated input noise and improve SNR. Moreover, with this design, there is no need to use an extra g_m-C filter, which adds extra flicker noise. Appropriate chopping frequencies and proper distribution of the gains between three stages are important to reach a low-noise, low-power, and high-sensitivity circuit. Moreover, with utilising the nested chopper at the input of this circuit, the charge injection effect will be reduced. With the help of this circuit, corner frequency of 0.5 µHz is achievable and near-DC high precision operation is possible. In addition, the first amplifier is designed to have a low capacitance, which contributes to ultra-high sensitivity in capacitive sensors.

CHAPITRE 3

ANALYSIS OF SENSITIVITY AND POWER CONSUMPTION OF CHOPPING TECHNIQUES FOR INTEGRATED CAPACITIVE SENSOR INTERFACE CIRCUITS

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Abstract

In this paper, parameters related to the sensitivity of the interface circuits for capacitive sensors are determined. Both the input referred noise and capacitance of the input transistors are important for capacitive sensitivity. Chopping is an effective technique for signal conditioning circuits because of its capability of reducing circuit noise at low frequencies. The capacitive sensitivity and power consumption of various chopping techniques including the dual chopper amplifier (DCA), single chopper amplifier (SCA), and two-stage single chopper amplifier (TCA) are extracted for different values of total gain and sensor capacitance. The minimum sensitivity for each technique will be extracted based on the gain and sensor capacitance. It will be shown that designation of the amplifier and distribution of gain in the TCA and DCA are important for sensitivity. A design procedure for chopper amplifiers that illustrates the steps required to achieve either the best or the desired sensitivity while minimizing power consumption will be presented. It will be shown that for a small sensor capacitance and large total gain, the DCA has the best sensitivity, while for a large sensor capacitance and a lower gain, the SCA is preferable. The TCA is the desired architecture for an average total gain and a large sensor capacitance. Moreover, when the power consumption is the key requirement and

the maximum sensitivity is not the goal; the TCA works best due to its potential to decrease the power consumption.

Keywords: chopper amplifier; capacitive sensor; high sensitivity; low power

3.1   Introduction

Consumer electronics are increasingly making use of multiple integrated sensors to enhance their functionalities. Microelectromechanical systems (MEMS) have enabled the design of sensors with very high sensitivities, enabling a range of sensing applications (Huang et al., 2015). Sensors that convert a physical stimulus into a capacitance are widely used for different purposes including detecting motion, pressure, and acceleration (Han & Shannon, 2009; Hao et al., 2014; Liu, Hsiung, & Lu, 2012; Meng & Dean, 2016). Capacitive sensing has the benefits of a low temperature coefficient, low power dissipation, and low noise. Additionally, the devices can be easily integrated with CMOS circuits, and they are compatible with VLSI technology scaling (Hafizi-Moori & Cretu, 2015; Jiangfeng, Fedder, & Carley, 2004b; Tavakoli & Sarpeshkar, 2003).

Typical capacitive sensor output signals are in the microvolt range and have bandwidths ranging from DC up to a few kilohertz (Witte, Makinwa, & Huijsing, 2007). Amplifying such signals requires low noise and low offset amplifiers. Due to this frequency range, flicker noise is the dominant noise source in CMOS technology. There are two methods to remove the flicker noise: auto-zeroing and chopping (Enz & Temes, 1996). Auto-zeroing is a sampling technique that removes flicker noise; but causes noise folding. Chopping is a continuous-time modulation technique in which the signal and offset are modulated to high frequencies. As a result, the chopping technique achieves low noise at low frequencies. Chopping techniques have been applied widely in recent publications to remove flicker noise and DC offsets (Belloni, Bonizzoni, Fornasari, & Maloberti, 2010; Fan, Huijsing, & Makinwa, 2012a; Hongzhi, Fares, Deyou, Kemiao, & Huikai, 2008; Jiangfeng, Fedder, & Carley, 2004c; Ong & Chan, 2014; Pertijs & Kindt, 2010; Qu, Fang, & Xie, 2008; Sun et al., 2011; Yaul &

Chandrakasan, 2016). One or more chopping frequencies can be applied when using chopping. An amplifier with a single chopping frequency is a single chopper amplifier (SCA) that can also be implemented as a two-stage chopper amplifier (TCA). In this system, the signal is modulated to a higher frequency, amplified and then demodulated to the baseband. When two different chopping frequencies are used, the system is a dual chopper amplifier (DCA). This technique can simultaneously remove flicker noise and reduce power consumption (Hongzhi et al., 2008; Sun et al., 2011).

Figure 3.1 shows a signal conditioning circuit that is connected to a differential sensor capacitance, C_0 that can vary by ΔC in the presence of a stimulus. An important factor that must be considered in systems with capacitive sensors is parasitic capacitances at the sensing nodes that include the input capacitance of the signal conditioning circuit, C_{gg}, and the interconnect parasitic capacitance, C_P.
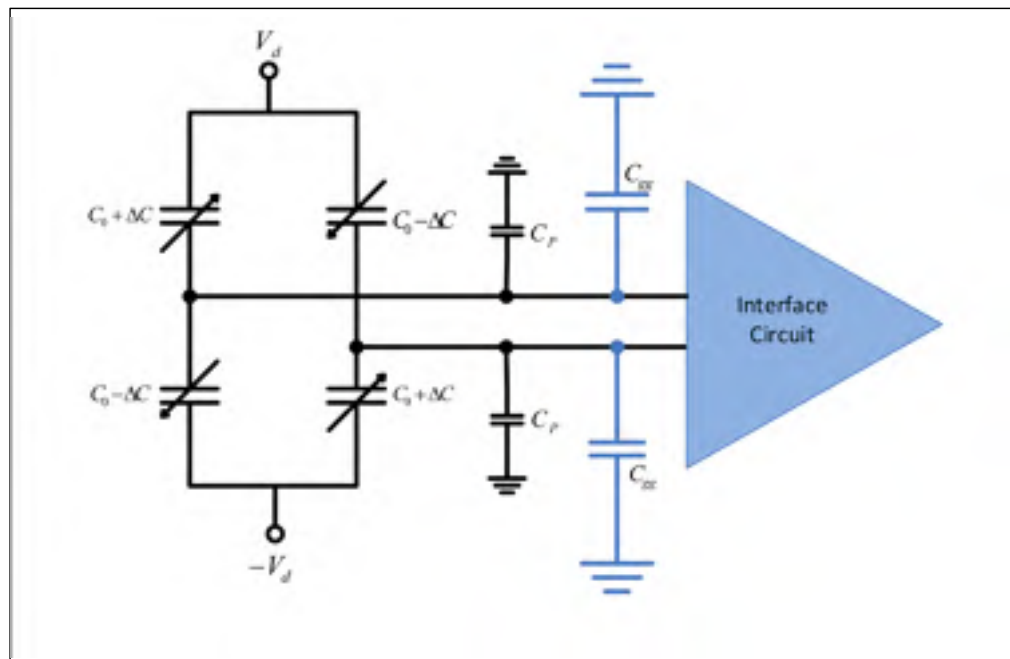
Figure 3.1 Connection of differential sensor capacitance to an interface circuit with parasitic capacitances.

The sensed signal is sensitive to loading caused by parasitic capacitances at this node, which can degrade the circuit performance. In this paper, the effect of input capacitance of such an interface circuit on the sensitivity performance is investigated.

Power consumption is another important factor when sensors are used in portable devices (Shiah & Mirabbasi, 2014). Adding this requirement means the power must be minimized while maintaining satisfactory sensitivity in the interface system. There is a tradeoff between the noise level and the power consumption, which poses a design challenge when trying to simultaneously obtain low noise and low power consumption.

This paper presents an analysis of sensitivity and power consumption when using the three chopping techniques of the SCA, TCA and DCA. These architectures are described in Section 3.2. Parameters related to the sensitivity of these systems are presented in Section 3.3, where a sensitivity factor used to extract the minimum detectable capacitance variation in the sensor capacitance is introduced. The sensitivity of the different chopping techniques is analyzed in Section 3.4. In each chopping technique, the achievable sensitivity and power consumption are extracted based on the total desired gain, the sensor capacitance, and the minimum sensitivity. Section 3.5 compares the sensitivity of the three techniques and the preferred chopping technique is identified based on design constraints. Section 3.6 provides a method to select the appropriate circuit architecture based on a sensor's capacitance and desired total gain. Finally, conclusions are presented in Section 3.7.

3.2   Architecture of the three different chopping techniques

The system diagrams of the SCA, DCA and TCA are shown in Figure 3.2. In the SCA, the detected signal from the capacitive sensor is chopped at frequency f_L, which is chosen to be higher than the $1/f$ noise corner frequency. After amplification, the signal is downconverted to the baseband and then filtered. In the TCA, the detected capacitive sensor signal is chopped at frequency f_L, which is chosen to be higher than the $1/f$ noise corner frequency of the first and second stages, and is then amplified by the first and second stages. After amplification, the
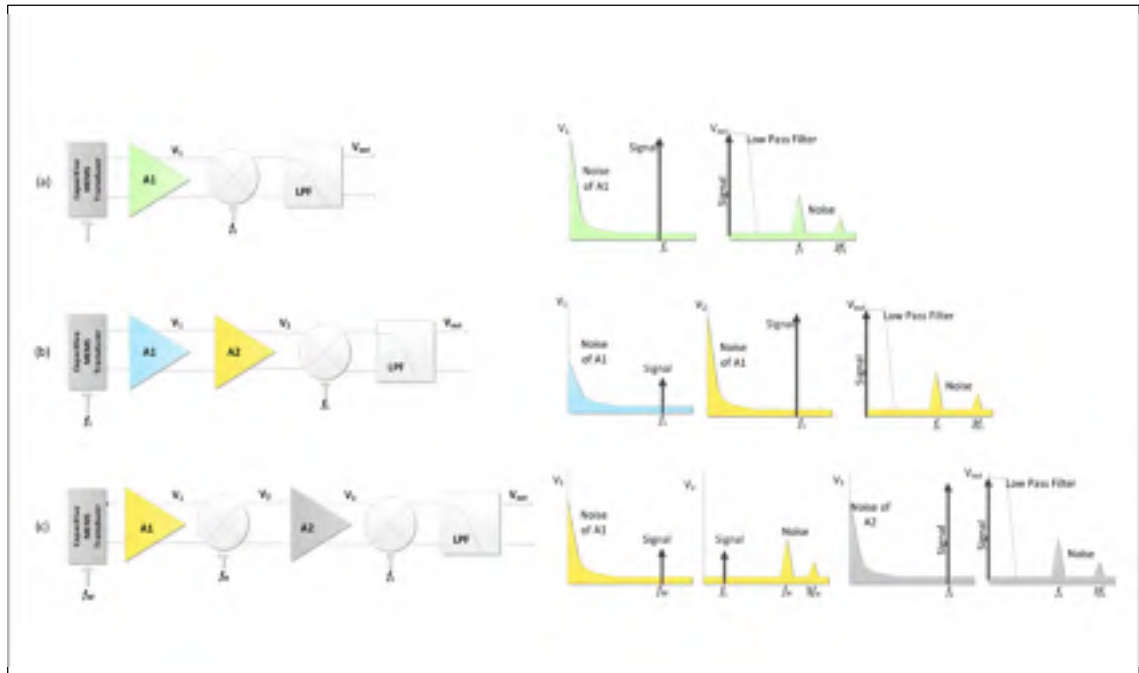
Figure 3.2 Diagram of the (a) single chopper amplifier, (b) two stage single chopper amplifier, and (c) dual chopper amplifier with a capacitive transducer connected to the input. The frequency domain signal and noise representation for each system is also presented.

signal is downconverted to the baseband and at last, the harmonics will be filtered. In the DCA, the sensed signal is modulated by frequency f_M, which is a frequency that is generated by the mixing of two chopper frequencies, f_H and f_L. After chopping with frequency f_M and amplification by the first stage A_1, the signal is then chopped with frequency f_H. In this step, the 1/f noise of the first stage can be filtered, as it is shifted to the odd harmonics of frequency f_H. Finally, the signal is amplified by the second stage A_2, and is then chopped by frequency f_L, which is higher than the 1/f noise corner frequency of the second stage. With this latest chopping operation, the signal has been downconverted to the baseband and the 1/f noise of the second stage is moved to the odd harmonics of f_L and can be filtered for further processing. This dual chopping technique has advantages that will be highlighted in Section 3.3.

3.3 Parameters related to the sensitivity of the chopping technique

In the following sections, the effective parameters for the sensitivity of the chopping amplifiers are shown and a sensitivity factor is defined to be able to compare the capacitive sensitivity of the signal conditioning circuits.

3.3.1 Noise and corner frequency

One of the important effective factors on sensitivity is the noise. The dominant noises sources in MOS transistors are thermal and flicker noise, which are given as (Gray & Meyer, 1990):

$$V_n^2 = \frac{4KT\gamma}{g_m} \tag{3.1}$$

$$V_f^2 = \frac{K_f}{C_{ox}WLf} \tag{3.2}$$

where V_n is the thermal noise voltage, V_f is the flicker noise voltage, g_m is the transconductance of the MOS transistor and K is Boltzmann's constant. In (3.2), K_f is the flicker noise constant and W and L are the width and length of the transistor, respectively.

The goal of the chopping technique is to remove the flicker noise such that small signals at low frequencies can be detected. To remove the flicker noise, a suitable chopping frequency must be chosen. In addition, the chopping frequency should be in the bandwidth of the amplifier to prevent suppression of the signal. A chopping frequency which is smaller than the noise corner frequency cannot remove the flicker noise properly. On the other hand, using a large chopping frequency requires a large amplifier bandwidth, which results in a higher power consumption. As a result, choosing the proper chopping frequency is important to optimize both the power consumption and the noise. Once the noise corner frequency is extracted, the appropriate chopping frequency can be selected.

The noise corner frequency is the frequency at which the thermal noise and flicker noise become equal (Fang, 2006a). Based on the relation of the thermal noise and flicker noise, the noise corner frequency can be extracted as:

$$f_c = \frac{K_f}{4KT\gamma} \times \frac{g_m}{W.L.C_{ox}}$$ (3.3)

As shown in (3.3), both dimensions of the transistor and its transconductance affect the noise corner frequency. Larger dimensions and a smaller transconductance result in a lower noise corner frequency. If the chopping frequency is 10 times larger than the corner frequency, then the flicker noise is 10% of the thermal noise and can be neglected (Fang, 2006a). In this analysis, a chopping frequency that is 10 times larger than the noise corner frequency is considered, and the amplifier bandwidth is chosen to be a slightly larger than the chopping frequency as shown below to optimize the power consumption:

$$10 \times f_c < f_{chop} < BW$$ (3.4)

where f_{chop} is the chopping frequency and BW is the 3-dB bandwidth of the amplifier.

3.3.2   Input capacitance

The other determining factor on the capacitance sensitivity is the parasitic capacitance of the input transistor. Based on the value of the sensor capacitance and capacitance of the input transistor, the sensitivity can be decreased. The gate capacitance of a MOS transistor is equal to (Gray & Meyer, 1990):

$$C_{gg} = W.L.C_{ox} + W.L_{ov}.C_{ox}$$ (3.5)

where W and L are width and length of the transistor, C_{ox} is the thin-oxide field-capacitance per unit area, and L_{ov} is the gate overlap length.

Considering equations (3.5), (3.2) and (3.3), it is observed that the noise corner frequency and the flicker noise have an inverse relationship with the gate capacitance. If the dimensions of the input transistor are increased to decrease the flicker noise and the corner frequency, the input capacitance will increase. This effect can have a negative effect on the sensitivity, as will be shown in section 3.3. In an amplifier, the equations for the bandwidth and gain can be written as follows:

$$BW \cong \frac{1}{R_o . C_L}$$

(3.6)

$$G = \alpha \cdot g_m \cdot R_o$$

(3.7)

where C_L is the load capacitance, R_o is the output impedance, and g_m is the transconductance of the input transistor. The coefficient α is included in (3.7) because the exact gain depends on the amplifier topology. In fully differential amplifiers, α is equal to 1, and in other types such as two stage amplifiers and folded cascode amplifiers, it is larger than 1. Substituting the equations for bandwidth (3.6) and the noise corner frequency (3.3) into equation (3.4), we obtain:

$$10 \times \frac{K_f}{4KT\gamma} \times \frac{g_m}{W . L . C_{ox}} < \frac{1}{R_o . C_L}$$

(3.8)

We can rewrite (3.8) as:

$$W \cdot L \cdot C_{ox} > 10. \frac{K_f}{4KT\gamma} . g_m . r_o . C_L$$

(3.9)

In (9), $g_m . r_o$ is the gain or part of the gain, and the left hand side can be considered as the capacitance of the input transistor (C_{gg}) if the value of $W \cdot L_{ov} \cdot C_{ox}$ is negligible. If not, the input capacitance is larger than this value. As a result, the input capacitance and gain are related such that:

$$C_{gg} > 10 \cdot \frac{K_f}{4KT\gamma \cdot \alpha} \cdot G \tag{3.10}$$

This equation highlights the fact that the input capacitance and the gain are dependent on each other. For a given gain, the input capacitance is larger than the value in (3.10). As the gain is increased, the input capacitance will also increase, and this can degrade the sensitivity.

3.3.3   Sensitivity factor

A sensitivity factor is introduced to extract the minimum variation in the sensor capacitance. A smaller sensitivity factor translates to a greater sensitivity for the sensing interface.
The detected voltage signal from the capacitive sensor should be larger than the input noise floor of the circuit, as shown by:

$$v_n \times \sqrt{BW_{system}} < \frac{\Delta C_{min}}{2C_0 + C_p + C_{gg}} V_{dd} \tag{3.11}$$

where V_n is the noise floor voltage, C_0 is the sensor nominal capacitance, C_p is the parasitic capacitance of the interconnects, C_{gg} is the capacitance of the interface circuit, ΔC_{min} is the minimum detectable variation at the sensor capacitance, V_{dd} is the excitation voltage, and BW_{system} is the desired bandwidth of the system and is defined by the application. Equation (3.11) can be rewritten as:

$$v_n \times \sqrt{BW_{system}} < \frac{\Delta C_{min}}{(2C_0) \times (1 + C_{gg}/2C_0)} V_{dd} \tag{3.12}$$

Here, it is assumed that the parasitic capacitance of the interconnect can be neglected. This is a viable assumption in monolithically integrated sensors where very high levels of sensitivity are required and interconnect parasitics are minimal. In this analysis, a loading factor K_c is defined as:

$$K_c = \frac{C_{gg}}{2C_0} \tag{3.13}$$

Based on (12) and (13), the following relationship can be derived:

$$v_n \times (1 + K_c) < \frac{\Delta C_{min}}{(2C_0) \times \sqrt{BW_{system}}} V_{dd} \tag{3.14}$$

In this equation, C_0, V_{dd}, and BW_{system} are constants. As a result, $\frac{\Delta C_{min}}{2C_0}$, which is the ratio of the smallest detectable capacitance variation to the nominal capacitance, depends on the noise and the loading factor. A sensitivity factor can then be defined as:

$$S_F = v_n \times (1 + K_c) \tag{3.15}$$

As such, both the noise floor and the loading factor are influential in detecting the minimum variation in the sensor capacitance. Thermal noise has a direct effect on the sensitivity factor as it is multiplied by $(1 + K_C)$. Therefore, the value of the loading factor is important. If it is much smaller than 1, the thermal noise is the sole factor for determining the sensitivity factor; however if it is comparable with 1, it will affect the sensitivity factor.

In this paper, the sensitivity factor is applied to extract the minimum detectable variation of capacitance in the SCA, TCA, and DCA configurations for different gains and sensor capacitances.

3.3.4   Power-sensitivity factor

To achieve a design suited to low-power operation, the effect of both sensitivity factor and power consumption should be considered. It is possible to achieve a very small sensitivity factor in a system, but this may demand high power consumption. As a result, a power-sensitivity factor is defined as:

$$PS_F = P \times S_F \tag{3.16}$$

where P is the power consumption of the system. Based on the application, the system is designed to attain the minimum power-sensitivity factor, or the smallest possible value of sensitivity factor considering a constraint on the power-sensitivity factor.

3.4 Sensitivity of the SCA, TCA, and DCA

In this section, the sensitivity factor of the SCA, TCA and DCA are extracted based on the total gain and sensor capacitance. To design a chopper amplifier, it is important that the relation between the bandwidth and the noise corner frequency given in (4) is respected. As a result, a *reference amplifier* with a particular gain and a valid relationship between the bandwidth and the noise corner frequency is considered to compare the performance of different chopping techniques for different gains.

3.4.1 Reference amplifier

It is assumed that the reference amplifier has a gain of G_0 and the current and dimensions of the input transistors maintain a valid relationship between the bandwidth and the noise corner frequency.

The characteristics of the chopping amplifiers for different gains are extracted based on characteristics of the reference amplifier. It is assumed that all amplifiers used in the chopping systems in this paper have a bandwidth of at least ten times larger than their noise corner frequency. There are different methods of changing the current and dimensions of the transistors to achieve an amplifier gain such that:

$$G = K \cdot G_0 \tag{3.17}$$

where G is the amplifier gain which is K times the gain of the reference amplifier. The possible ways of changing the gain while maintaining the condition set in (4) are listed in Table 3.1 along with the effect they have on different circuit metrics.

Table 3.1 Different methods of changing the gain of the SCA w.r.t. the reference amplifier.

Case	G	Length	Width	Vn	Cgg	Gm	Ro	fc	BW	Power
1	K	K	1	K	K	$\frac{1}{K}$	K^2	$\frac{1}{K^2}$	$\frac{1}{K^2}$	$\frac{1}{K^2}$
2	K	1	K	$\frac{1}{K}$	K	K	1	$\frac{1}{K}$	$\frac{1}{K}$	K
3	K	$\sqrt{K}$	$\sqrt{K}$	1	K	1	K	1	1	1
4	K	$\sqrt[4]{K}$	$\sqrt[4]{K^3}$	$\frac{1}{\sqrt{K}}$	K	$\sqrt{K}$	$\sqrt{K}$	$\frac{1}{\sqrt{K}}$	$\frac{1}{\sqrt{K}}$	$\sqrt{K}$

In all of these cases, the load capacitance C_L is kept constant. It is noted that any second order non-idealities are neglected in Table 3.1 Moreover, the minimum allowed value of length and width of the transistors depend on the technology considered for the design.

Figures 3.3 and figure 3.4 show the effect of changing the gain on the sensitivity factor for two values of the loading factor in the reference amplifier (k_c =0.01 and 1). The sensitivity factor and gain of these figures are normalized based on the sensitivity factor and gain of the reference amplifier. In each figure, the sensitivities for the four possible cases in Table 1 are considered to achieve the desired gain. As shown in Figure 3.3, with increasing gain, the thermal noise and input capacitance vary as shown in Table 3.1. C_{gg} is changed by a factor of K in all of the cases which implies that the loading factor is increased by a factor of K. As a result of the gain variation, the loading factor is changed from 0.001 to 0.1, having a negligible impact on the sensitivity factor in this case as it remains much smaller than 1. Variation of the thermal noise depends on the considered case. As shown in Figure 3.3, with increasing K, the sensitivity factor is increased in case 1, decreased in cases 2 and 4, and almost constant in case 3. The trend in the sensitivity factor is thus the same as the trend of the thermal noise. This means that the effect of the loading factor on the sensitivity factor is negligible and the sensitivity factor is affected solely by the thermal noise.
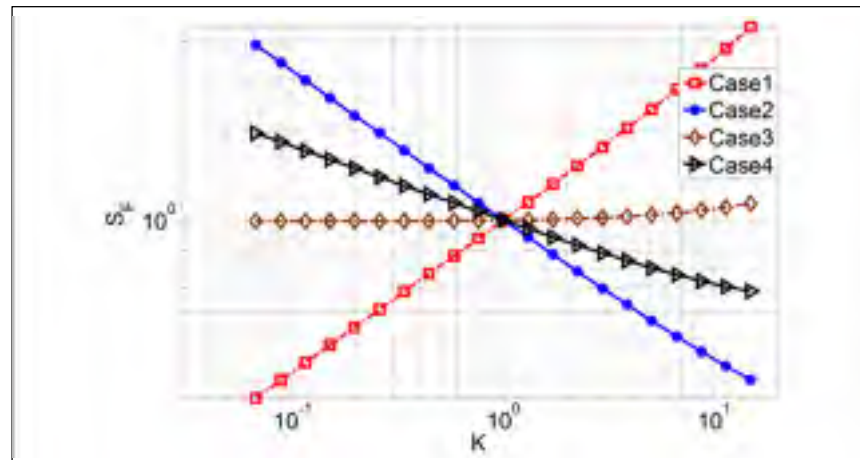
Figure 3.4 Sensitivity factor of the chopper amplifier normalized
by the reference amplifier for a loading factor of 0.01.
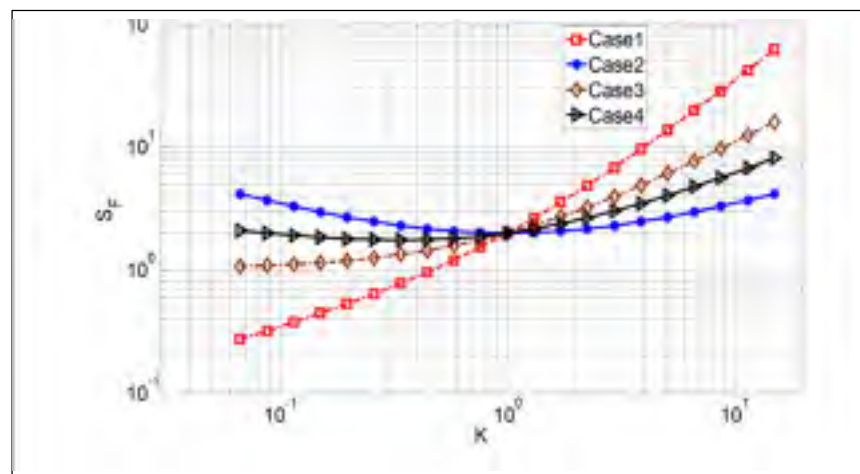
Figure 3.3 Sensitivity factor of the chopping amplifier
normalized by the reference amplifier for a loading factor of 1.

The sensitivity factor based on varying K for a loading factor of 1 in the reference amplifier is shown in Figure 3.4. In this case, the loading factor varies from 0.1 to 10. As a result, it affects the sensitivity factor. As shown in Figure 4, with increasing K, the sensitivity factor is increased in case 1 but in cases 2, 3 and 4, there is an optimum value. This stems from both the thermal noise and loading factor variation with K. In case 1, both the thermal noise and loading factor are increased by increasing K, causing an ascending trend in the sensitivity factor. However, in cases 2, 3, and 4, the loading factor is increased but thermal noise is decreased. Since the

effect of loading factor in this case is not negligible; an optimum value of K to achieve the lowest sensitivity factor can be observed. Accordingly, when the loading factor is 1, the effect of the loading factor on the sensitivity factor cannot be neglected.

To be able to compare the sensitivity factors of the different chopping techniques in the following analysis, the total gain of the circuit is considered to be set to G_t, and the gain of the reference amplifier is considered to be of G_0. Equation (3.18) shows the relation between G_0 and G_t implying that the total gain is G_0 times larger than the gain of the reference amplifier.

$$G_t = G_0^2 \tag{3.18}$$

In the following sections, the sensitivity factor and power consumption of the three chopping techniques considered in relation to the reference amplifier will be analyzed.

3.4.2   Single chopper amplifier

In the SCA, the signal is chopped at the frequency f_{chop}. After modulation, the signal is amplified by the amplifier. Next, the signal is demodulated to the baseband where it will be filtered by a low pass filter. For an SCA gain of G_t, K is made to be equal to G_0. Out of the four cases in Table 3.1, cases 1, 2, 4 can be applied in the SCA to vary the gain. Case 3 cannot be applied because achieving a large gain by changing the dimensions and keeping the power constant is not possible. The sensitivity factor of the SCA is given by:

$$S_{F,k} = V_{n,SCA}\left(1 + K_{c,SCA}\right) \tag{3.19}$$

where $V_{n,SCA}$ is the thermal noise of the amplifier and $K_{C,SCA}$ is the loading factor of the amplifier. The sensitivity factor for cases 1, 2 and case 4 based on the reference amplifier are given below in (3.20), (3.21) and (3.22), respectively.

$$S_{F,SCA1} = G_0 \cdot V_{n,0}(1 + G_0 \cdot K_{c0}) \tag{3.20}$$

$$S_{F,SCA2} = \frac{V_{n,0}}{\sqrt{G_0}}(1 + G_0.K_{c0}) \tag{3.21}$$

$$S_{F,SCA4} = \frac{V_{n,0}}{\sqrt[4]{G_0}}(1 + G_0.K_{c0}) \tag{3.22}$$

where $V_{n,0}$ is the reference amplifier noise floor voltage and K_{C0} is the reference loading factor. The sensitivity factor of the SCA versus the total gain is shown in Figure 3.5 for three sensor capacitances of 100 fF, 250 fF, and 800 fF and for cases 1, 2, and 4.

As shown, increasing the gain increases the sensitivity factor and the increase is larger for a smaller sensor capacitance because it has a larger loading factor. Comparing these three cases, $S_{F,SCA2}$ has the lowest sensitivity factor, since the thermal noise is smaller in case 2.
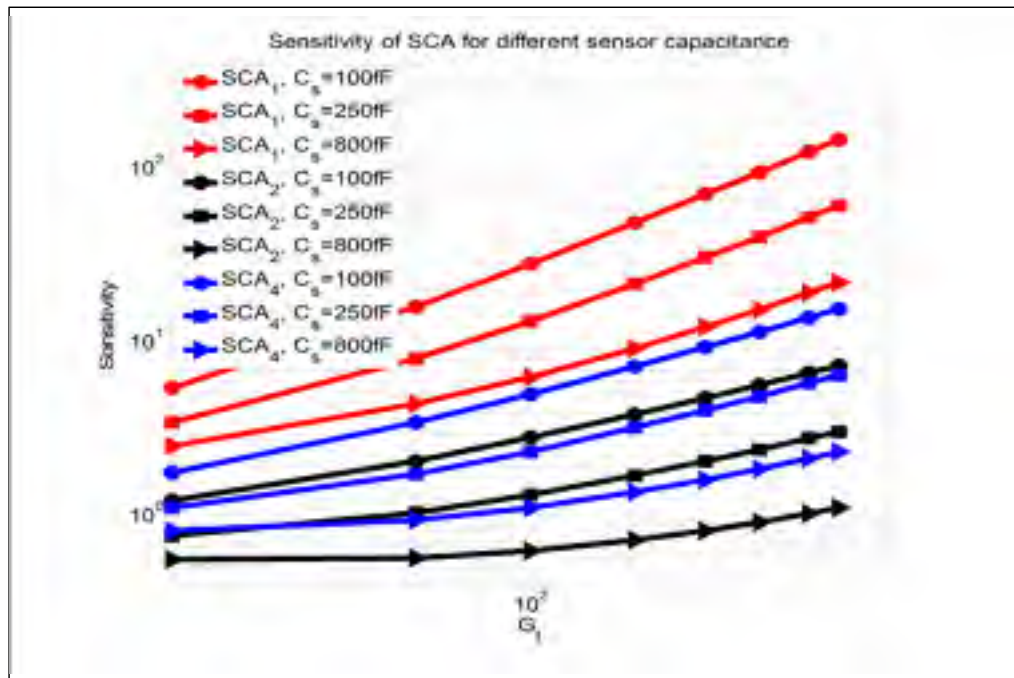
Figure 3.5 Sensitivity factor of SCA for different total gains for sensor capacitance of 100fF, 250fF, and 800fF.

The power consumption is independent of the sensor capacitance and in cases 1, 2 and 4, it is equal to:

$$P_{SCA,2} = 1/_{G_0^2} \cdot P_0 \qquad (3.23)$$

$$P_{SCA,2} = G_0 \cdot P_0 \qquad (3.24)$$

$$P_{SCA,4} = \sqrt{G_0} \cdot P_0 \qquad (3.25)$$

From these equations, it can be concluded that although *SCA₂* has better sensitivity, it consumes more power. The power-sensitivity factor for the SCA in cases 1, 2 and 4 is given by:

$$PS_{F,SCA2} = 1/_{G_0} \cdot V_{n,0}(1 + G_0 \cdot K_{c0}), \qquad (3.26)$$

$$PS_{F,SCA2} = \sqrt{G_0} \cdot V_{n,0}(1 + G_0 \cdot K_{c0}) \qquad (3.27)$$

$$PS_{F,SCA4} = \sqrt[4]{G_0} \cdot V_{n,0}(1 + G G_0 \cdot K_{c0}). \qquad (3.28)$$

From these equations, it can be concluded that increasing the gain will increase the power-sensitivity factor in cases 2 and 4 but in case 1 it depends on both the value of the gain and the loading factor. The power-sensitivity in case 2 is larger than in case 4. Moreover, a smaller sensor capacitance results in a larger power-sensitivity factor outlining the limitations of the SCA topology to accommodate small sensor capacitances.

3.4.3 Two-Stage single chopper amplifier

In the TCA, the signal is also chopped by the frequency *f_chop*. After modulation, the signal is amplified by the first and second amplifiers. Next, the signal is demodulated to the baseband

where it will be filtered by a low pass filter. Since both amplifiers in the TCA are operating at the same frequency, it is important to select a chopping frequency that is at least 10 times larger than both noise corner frequencies of the amplifiers. To analyze the performance of the TCA with the same total gain as the SCA, it is assumed that the first amplifier and the second amplifier have the gain of G_1 and G_2 that are varied from 1 to G_t (G_0^2) as outlined in (3.29) and (3.30).

$$G_1 = K \times G_0 \tag{3.29}$$

$$G_2 = 1/K \times G_0 \tag{3.30}$$

G_1 and G_2 are the gain of the first and second amplifiers and K (distribution of gain between two stages) should be in the range shown in (3.31) to have the total gain of each amplifier range from 1 to G_0^2.

$$^1/_{G_0} \leq K \leq G_0. \tag{3.31}$$

The second amplifier in the TCA has a constant load capacitance of C_L, but the load capacitance of the first amplifier is the input capacitance of the second amplifier. As a result, changing the dimensions of the second amplifier to change the gain will affect the characteristics of the first amplifier. A larger gain in the second amplifier will result in a larger input capacitance, and a larger load capacitance for the first amplifier. This will decrease the bandwidth of the first amplifier. As a result, the effect of changing the load capacitance of the first amplifier should be considered when distributing the gain between the two stages. The TCA is designed in such a way that the bandwidths of both amplifiers are at least 10 times larger than the noise corner frequency. The characteristics of the possible methods to change the gain of the first amplifier by the factor of K when compared to the reference amplifier and the gain of the second amplifier by a factor of *1/K* are shown in Tables 3.2 and 3.3; respectively.

Table 3.2 Different methods of changing the gain of the TCA first amplifier w.r.t. the reference amplifier.

Case	G	Length	Width	Vt	C_{gg}	G_m	R_o	F_c	BW	Power
1	K	K	1	K	K	$1/K$	K^2	$1/K^2$	G_0/K	$1/K^2$
2	K	1	K	$1/K$	K	K	1	1	$G_0 \cdot K$	K
3	K	$\sqrt{K}$	$\sqrt{K}$	1	K	1	K	$1/K$	G_0	1
4	K	$\sqrt[4]{K}$	$\sqrt[4]{K^3}$	$1/\sqrt{K}$	K	$\sqrt{K}$	$\sqrt{K}$	$1/\sqrt{K}$	$G_0\sqrt{K}$	$\sqrt{K}$

Table 3.3 Different methods of changing the gain of the TCA second amplifier w.r.t. the reference amplifier.

Case	G	Length	Width	Vt	C_{gg}	G_m	R_o	F_c	BW	Power
1	$1/K$	$1/K$	1	$1/K$	$1/K$	K	$1/K^2$	K^2	K^2	K^2
2	$1/K$	1	$1/K$	K	$1/K$	$1/K$	1	1	1	$1/K$
3	$1/K$	$1/\sqrt{K}$	$1/\sqrt{K}$	1	$1/K$	1	$1/K$	K	K	1
4	$1/K$	$1/\sqrt[4]{K}$	$1/\sqrt[4]{K^3}$	$\sqrt{K}$	$1/K$	$1/\sqrt{K}$	$1/\sqrt{K}$	$\sqrt{K}$	$\sqrt{K}$	$1/\sqrt{K}$

As shown in Tables 3.2 and 3.3, different combinations of cases for the first and second amplifiers are possible to attain the required gain from each amplifier. However, only case combinations where the chopping frequency fulfills (3.4) for both amplifiers can be considered. With these conditions, only the combinations of cases in Table 3.4 are suitable. The first case index in this table represents the applied case in the first amplifier and the second index shows the applied case in the second amplifier. Because of the limitation in the noise corner frequencies and the chopping frequency, all of these cases are valid for K larger than 1.

Table 3.4 Different case combinations (first amplifier and second amplifier) for changing TCA total gain.

Case	21	22	23	24	12	32	33	34	41	42	43	44
C_{gg}	K	K	K	K	K	K	K	K	K	K	K	K
V_n	$\frac{1}{K}+\frac{1}{K^3 G_0^2}$	$\frac{1}{K}+\frac{1}{KG_0^2}$	$\frac{1}{K}+\frac{1}{K^2 G_0^2}$	$\frac{1}{K}+\frac{1}{K^{1.5} G_0^2}$	$K+\frac{1}{KG_0^2}$	$1+\frac{1}{KG_0^2}$	$1+\frac{1}{K^2 G_0^2}$	$1+\frac{1}{K^{1.5} G_0^2}$	$\frac{1}{\sqrt{K}}+\frac{1}{K^3 G_0^2}$	$\frac{1}{\sqrt{K}}+\frac{1}{KG_0^2}$	$\frac{1}{\sqrt{K}}+\frac{1}{K^2 G_0^2}$	$\frac{1}{\sqrt{K}}+\frac{1}{K^{1.5} G_0^2}$
f_{chop}	K^2	1	K	$\sqrt{K}$	1	1	1	$\sqrt{K}$	K^2	1	1	$\sqrt{K}$
P	$2K$	$K+\frac{1}{K}$	$K+1$	$K+\sqrt{K}$	$\frac{2}{K}$	$1+\frac{1}{K}$	2	$1+\sqrt{K}$	$\frac{1}{K}+\sqrt{K}$	$K+\sqrt{K}$	$1+\sqrt{K}$	$2\sqrt{K}$

This means that in the TCA, the gain of the first amplifier should be larger than the gain of the second stage. As a result, it is impossible to implement a small gain in the first stage to realize a small loading factor. Between these cases, the maximum sensitivity is achieved by applying case combination 21. However, the power consumption for this case combination is the largest. The sensitivity factor of the TCA for total gains of 60 dB and 40 dB and two different sensor capacitances of 100 fF and 500 fF versus K are shown in Figure 3.6. Since the second amplifier does not have a sizable effect on the sensitivity factor of the TCA, the sensitivity factors based on the possible cases for the first amplifier are shown. As shown at this figure, at the same gain and sensor capacitance, case 2 has a smaller sensitivity factor than case 4. With increasing K, the trend in sensitivity factor is dependent on both the gain and the sensor capacitance. At a gain of 40 dB and a sensor capacitance of 500 fF, the sensitivity factor decreases for an increasing K. This is because the effect of the loading factor is negligible and when the gain of first amplifier is increased; the thermal noise is decreased resulting in a decreasing trend in the sensitivity factor. However, for some larger total gain or smaller sensor capacitance, the loading factor is not negligible when the gain of the first amplifier is increased. This results in an optimum value based on the value of K. At a gain of 60 dB and a sensor capacitance of 100 fF, where the effect of the loading factor is dominant over the thermal noise on the sensitivity factor. As a result, increasing the gain of the first amplifier causes the sensitivity factor to have an increasing trend.
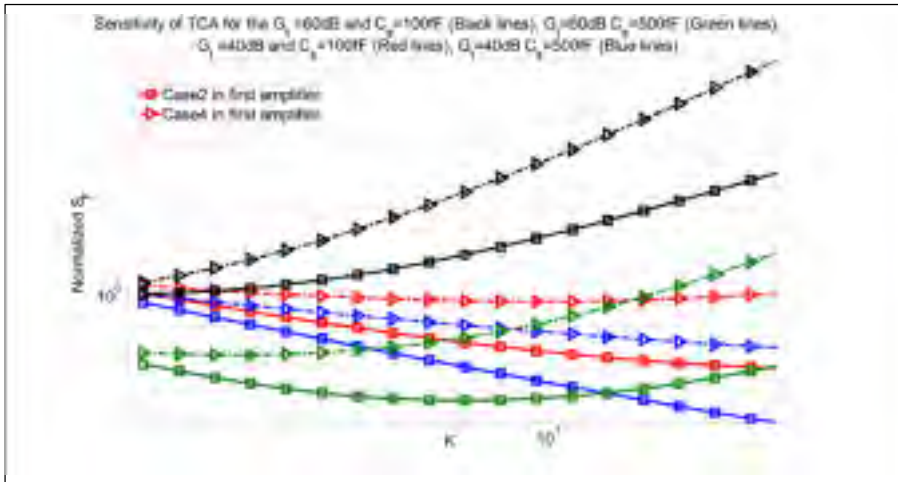
Figure 3.6 Normalized sensitivity factor of the TCA for different
total gains and sensor capacitances.

Note that minimum power consumption is achieved when K equals 1, which occurs when both amplifiers have the same gain. Comparing the power consumption in different cases shows that case 4 in the first amplifier results in a lower power consumption, although its sensitivity factor is larger.

The minimum sensitivity factor of the TCA for different total gains and different sensor capacitances is shown in Figure 3.7 (a) and the ratio of gain of the first amplifier to the total gain related to the minimum sensitivity of TCA is shown in Figure 3.7 (b). For each gain and sensor capacitance, the sensitivity factor is based on the possible gain adjustment cases, the range of K is considered, and the minimum sensitivity factor is extracted. As a result, for each gain and sensor capacitance, the value of K and the applied cases can be different. As shown in Fig. 3.7 (b), at a smaller G_t, the ratio of the first amplifier gain to the total gain is 1 which means that the minimum sensitivity factor is reached when all the amplification is done at the first stage and the second stage has the gain of 1. Note that this case corresponds to the SCA, since all gain is achieved using only one stage and the second gain stage is not necessary. As the total gain is increased, the ratio of gains starts to decrease based on the value of sensor capacitance. For a smaller sensor capacitance, the ratio starts to drop at a smaller gain, but for

the larger sensor capacitance, the ratio stays at 1 and then starts to drop at a larger gain. This is justified by the loading factor.

Increasing the gain increases the power consumption, and the power consumption for a large sensor capacitance is higher. This is because in this condition, all amplification is done by the first amplifier which results in a larger power consumption. Systems with a smaller sensor capacitance can have lower power consumption because the amplification is distributed between the two stages.

(a)

(b)
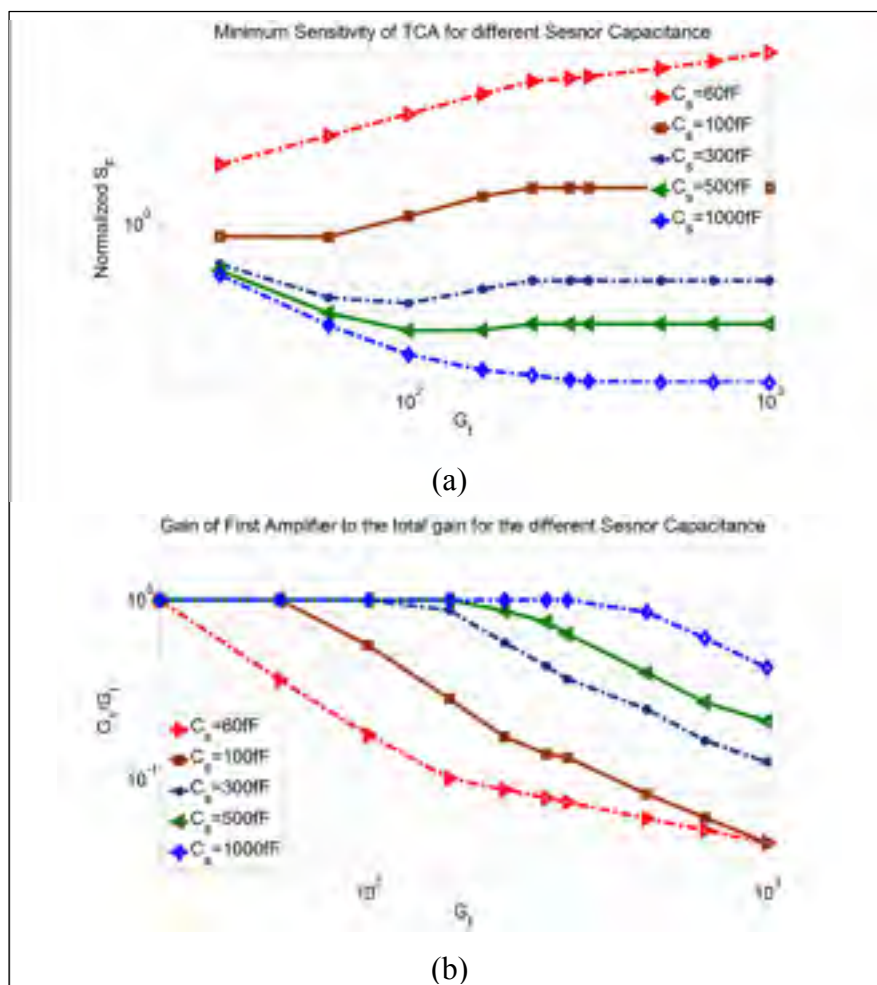
Figure 3.7 Minimum Sensitivity factor in the TCA for (a) different total gains and sensor capacitances and (b) ratio of first amplifier gain to total gain related to minimum sensitivity factor.

3.4.4 Dual chopper amplifier

In the dual chopper amplifier, two different and independent chopping frequencies are applied. Each chopping frequency is defined by the corner frequency of the related amplifier. This characteristic gives an extra degree of freedom when distributing the gain between the two stages which makes it possible to have a smaller sensitivity factor. As with the TCA, the capacitance of the input pair of the second amplifier is the load capacitance of the first amplifier. As a result, changing the gain distribution between the two stages changes the load of the first amplifier, which affects its bandwidth and power consumption. If the first and second amplifiers have a gain of G_1 and G_2, respectively, as described in (3.29) and (3.30), there are different ways to change their gains and all of the combinations in Tables 3.2 and 3.3 can be applied to reach the desired gain. The sensitivity factor of the DCA for sensor capacitances of 100 fF and 500 fF for gains of 40 dB and 60 dB are shown in Figures 3.8 (a) and 3.8 (b). In these two figures, the sensitivity factor based on K and three possible cases for the gain modification of the first amplifier are shown. Since the effect of the second amplifier on the sensitivity factor is small, it is not considered here. This is the case because the total gain can be distributed to ensure that the gain of the first amplifier is high enough to suppress the thermal noise of the second stage, or that the gain of the second amplifier is high enough to result in a small thermal noise from the second stage.

As shown in Figure 3.8 (a), increasing K decreases the sensitivity factor for cases 2 and 4 and increases it for case 1. With increasing K, the thermal noise is decreased in cases 2 and 4 and increased in case 1, but the loading factor is increased in all cases. At this total gain, the effect of the thermal noise is dominant rather than the loading factor. As a result, the sensitivity factor has the same trend as the thermal noise. At a gain of 40 dB and a sensor capacitance of 500 fF, the minimum sensitivity factor is reached when K is maximized. In other words, all amplification is done in the first stage and the second stage has a gain of 1. This condition simplifies to the SCA. For a gain of 40 dB and a sensor capacitance of 100 fF, the minimum sensitivity factor is reached with the minimum possible K and applying case 1 for the first amplifier. The equation of sensitivity factor in this case is shown in given by:

$$Sens_{DCA} = \sqrt{K + \frac{1}{KG_0{}^2}}(1 + Kk_C),$$

(3.32)

A minimum K means the gain of the first amplifier is equal to 1 and all amplification is done in the second stage. For a small sensor capacitance (i.e., 100 fF), the effect of the loading factor is more important and the first amplifier acts as a buffer to keep the parasitic capacitance at the sensor node low, while being able to drive the larger capacitance of the second amplifier that implements the required gain.

(a)

(b)
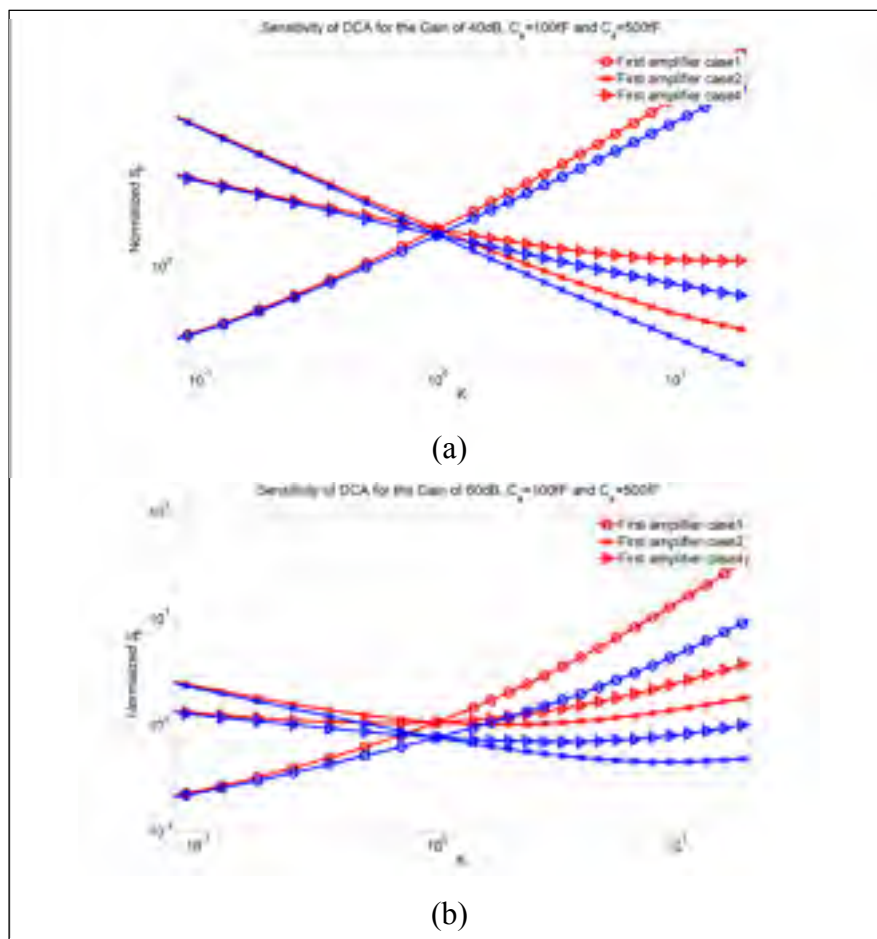
Figure 3.8 Normalized sensitivity factor of the DCA for the gains of (a) 40 dB and (b) 60 dB for sensor capacitance of 100 fF (red lines) and 500 fF (blue lines).

The sensitivity factor for a gain of 60 dB is shown in Figure 3.8 (b). For cases 2 and 4, increasing the K decreases the thermal noise and increases the loading factor, which creates the presence of an optimum value. When K is smaller than the optimum value, the effect of the thermal noise is dominant and when K is larger than the optimum value, the effect of the loading factor becomes dominant. A minimum sensitivity factor is reached when the first amplifier has the gain of 1 and case 1 is applied. This removes the effect of the loading factor and results in the smallest sensitivity factor. It should be emphasized that case 1 is reached by decreasing the transistor lengths, and it should be checked whether it is possible or limited by technology geometry.

The power consumption of the DCA for the different cases can be extracted from Tables 3.2 and 3.3 The DCA has the maximum power consumption when the first amplifier is in case 1 and K is the smallest possible value, or when first amplifier is in case 2 and K is the maximum value. The optimum power consumption is reached for the DCA for the same gain in the first and second stages.

The minimum sensitivity factor of the DCA versus the total gain and for different sensor capacitances is shown in Figure 3.9 (a). These values are obtained by analyzing the sensitivity factors for the different gain modification cases and different values of K. As shown in Figure 3.9 (a), increasing the total gain decreases the minimum sensitivity factor. This can be explained by Figure 3.9 (b), which shows the ratio of the gain of the first amplifier to the total gain for the related minimum sensitivity factor. As shown, the ratio changes based on the total gain and the sensor capacitance, which is justified by the loading factor. Many distributions result in a negligible loading factor, but the minimum sensitivity factor is reached when the first amplifier has a gain of 1 which is attained by case 1 and all amplification is done at the second amplifier via case 2. At this condition, the minimum thermal noise is achieved. As shown in Figure 3.9 (a), increasing the total gain decreases the sensitivity factor because the thermal noise is decreased and the DCA has the ability to keep the loading factor small.
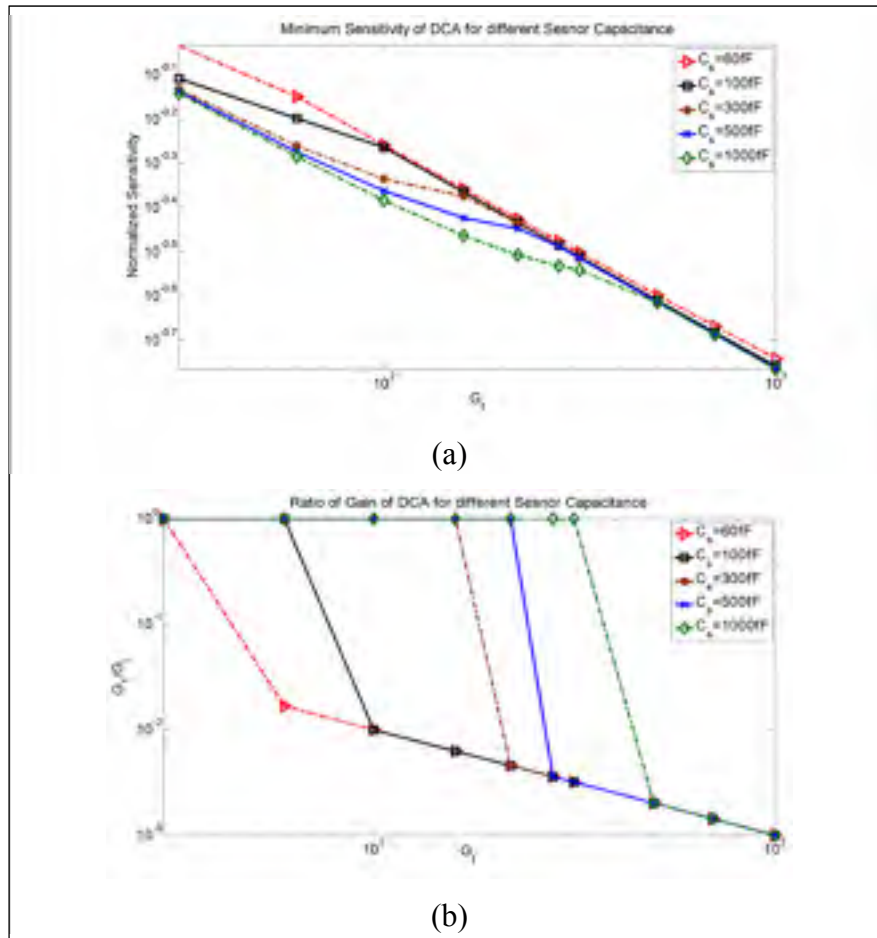
Figure 3.9 (a) Normalized minimum sensitivity factor of the
DCA for different total gains, and (b) ratio of gain of the first
amplifier to the total gain to reach the minimum sensitivity.

To reach the smallest sensitivity factor in the DCA when case 1 is applied, the length of the input transistors should be decreased to have a smaller loading factor. However, the technology can limit the level of scaling that can be achieved. As a result, another option is considered. The sensitivity factor of the DCA is extracted while the length of the input transistors is kept constant and this DCA is named DCA_2.

Figure 3.10 (a) shows the minimum sensitivity factor of DCA_2 and Figure 3.10 (b) shows the ratio of the gain of the first amplifier to the total gain to achieve the minimum sensitivity factor. As shown in Figure 3.10 (a), for a small sensor capacitance, the sensitivity factor is increased by increasing the gain. For this condition, the effect of the loading factor is dominant over the

thermal noise, and because of the assumed technology limitation, the loading factor cannot be reduced. For a larger sensor capacitance, an increasing gain leads to an initial decrease in the sensitivity factor, and then an increase is observed. This is because the effect of the thermal noise is dominant for small gain increases, but for a large increase, the effect of loading factor becomes important. As shown in Figure 10(b), for a small gain, the gain of the first amplifier is equal to the total gain. As the gain is increased, the ratio drops. The value of the total gain for which the ratio starts dropping depends on the sensor capacitance. However, the gain of the first amplifier cannot be as small as 1 because of the limitation in decreasing the transistor length, and this results in a larger sensitivity factor compared to the original DCA for the same condition.

(a)

(b)
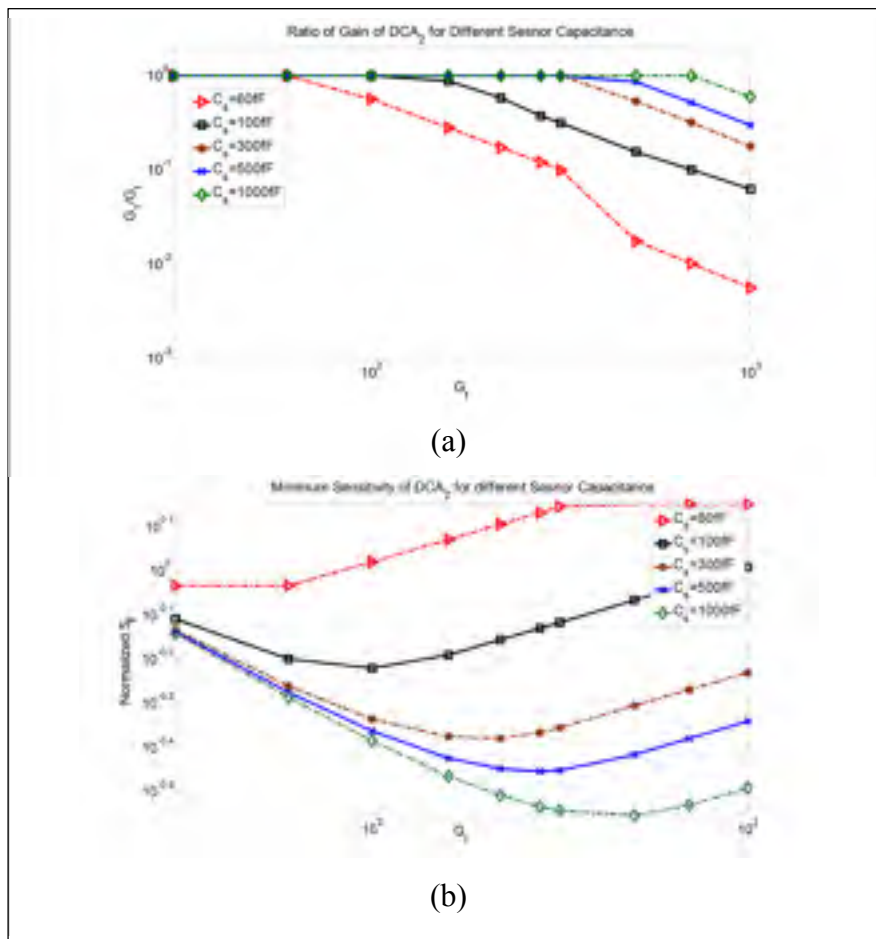
Figure 3.10 (a) Normalized minimum sensitivity factor of DCA$_2$ for different total gain, (b) Ratio of the gain of first amplifier to the total gain to reach the minimum sensitivity.

To illustrate the difference in the minimum sensitivity factor between the DCA and DCA$_2$, the ratio of the sensitivity factor of DCA to DCA$_2$ is shown in Figure 3.11. Based on the sensor capacitance and the total gain, this ratio can be very different. For a small gain, this ratio is 1 because all amplification is done in the first stage. When the gain is increased, this ratio is increased and becomes larger for a smaller sensor capacitance. This is because the DCA can be designed to have an insignificant loading factor, which is important in systems that require a high gain and have a small sensor capacitance.
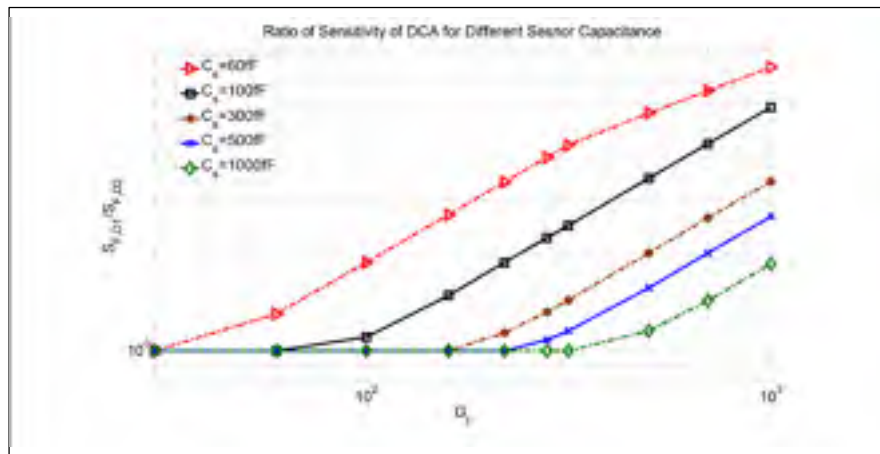
Figure 3.11 Ratio of minimum sensitivity factor in DCA to DCA$_2$

3.5 Comparison of the three chopping techniques

Based on the total gain required and the sensor capacitance, the sensitivity factor of each chopping technique is different. For a given gain and sensor capacitance, one of the chopping techniques has the smallest sensitivity factor. In this section the suitable chopping technique is shown for different required gains and sensor capacitance in order to reach the best possible sensitivity.

The minimum sensitivity factor is extracted for the particular value of K in each technique. Based on the total gain and sensor capacitance, each of these techniques can have the smallest sensitivity factor for a given range of K. To determine the best chopping technique, their sensitivities are compared to each other for different gains and sensor capacitances. For this

purpose, the sensitivity factors are compared, and the chopping technique with the smaller sensitivity factor within a given range of K is determined.

For example, to achieve a better sensitivity factor in DCA2 compared to the SCA, the following should be valid:

$$S_{F,DCA2} < S_{F,SCA} \tag{3.33}$$

Rewriting (3.33) based on the minimum sensitivity of DCA2 and the SCA, the following is obtained:

$$K_c . K - \frac{(1 + G_0 . K_c)\sqrt{G_0}}{\sqrt{1 + G_0{}^2}} \sqrt{K} + 1 < 0 \tag{3.34}$$

Solving for K gives the values of K for which DCA2 has a better sensitivity factor than the SCA. The left side of (3.34) is a quadratic equation with variable $\sqrt{K}$ and (3.34) is valid if the discriminant of shown in (3.35) is larger than 0.

$$\Delta = \left(\frac{(1 + G_0 . K_c)\sqrt{G_0}}{\sqrt{1 + G_0{}^2}} \right)^2 - 4 \times k_c \tag{3.35}$$

If Δ is smaller than 0, equation (3.34) cannot be valid which implies that the SCA has better performance than DCA2. If Δ is larger than 0, DCA2 has better performance for that particular range of K.

In a smaller fashion, by comparing the sensitivity factors of the chopping techniques, the equation related to their sensitivity can be derived and the preferred chopping technique can be determined for a given range of K.

Figure 3.12 shows the chopping technique with the smaller sensitivity factor based on the sensor capacitance and total gain. Sensitivity factors of the SCA, TCA and DCA2 are compared to each other and the chopping technique with the smaller sensitivity factor is shown in Figure 3.12 (a). As shown in this figure, at the smaller gain, the SCA can have the better sensitivity, as shown in the blue region. The yellow region represent the area where both TCA and DCA2 have the best possible sensitivity factor and are better suited than the SCA. At a larger gain and smaller sensor capacitance, DCA2 has a better possible sensitivity factor, shown in the red region. The sensitivity factors of the SCA, TCA and DCA are compared in Figure 3.12 (b). The red region is where the DCA has a better sensitivity factor. The TCA and DCA have the same sensitivity factor over the yellow region and the SCA has the smaller sensitivity factor

(a)

(b)
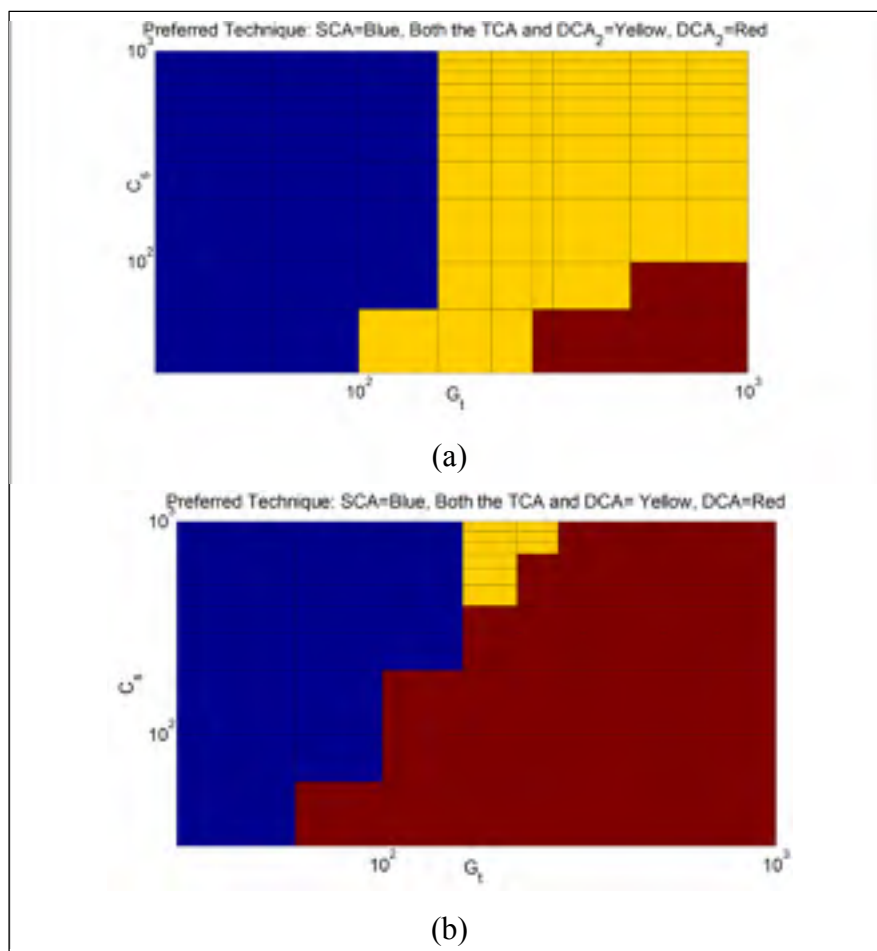
Figure 3.12 (a) Preferred chopping technique between SCA, TCA and DCA2, and (b) preferred chopping technique between SCA, TCA and DCA for different total gain and sensor capacitance.

over the blue region. Accordingly, when the desired gain increases or the sensor capacitance decreases, the DCA achieves better performance. At a small required gain, the SCA is preferred. For an increased gain, both the TCA and DCA can be used to reach a smaller sensitivity factor. However, for a large gain and small sensor capacitance, the DCA is preferred because it can be designed to attain a better sensitivity because of its reduced loading factor. To show the scale at which the sensitivity factor can be improved with the DCA or TCA in comparison to the SCA, different ratios of sensitivity factors are shown in Figure 3.13.

(a)

(b)

(c)
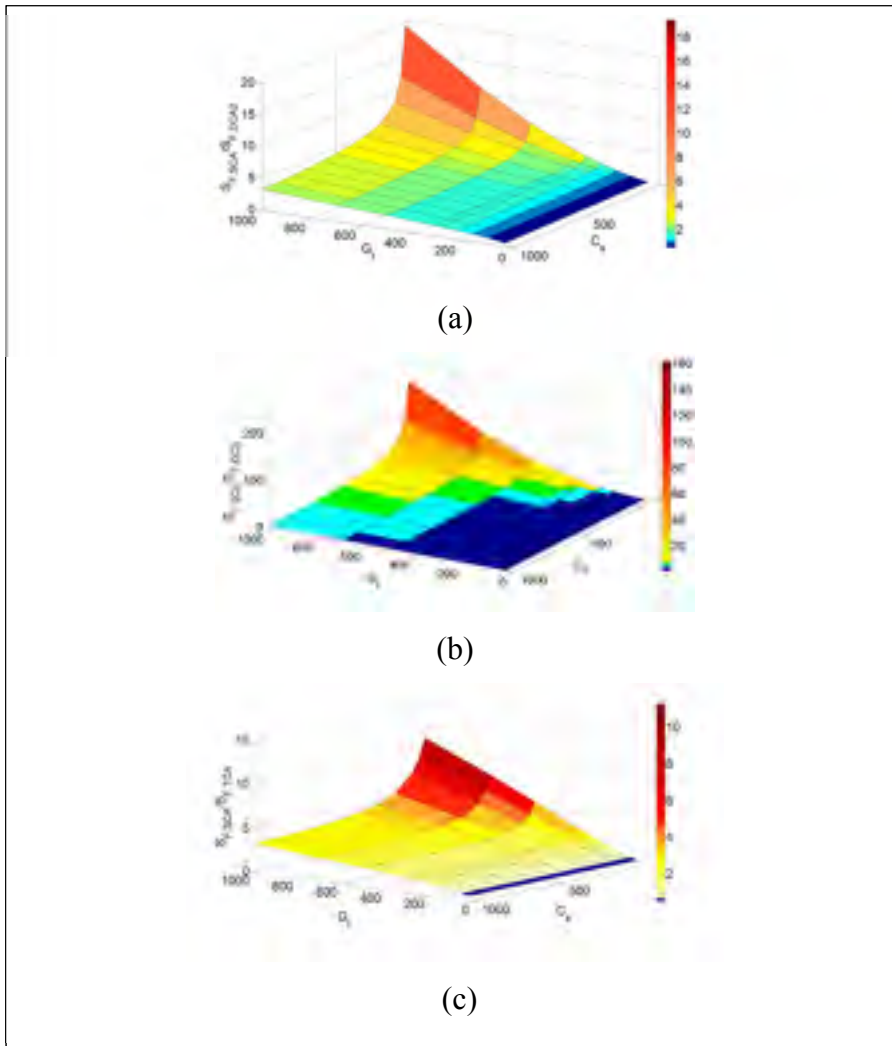
Figure 3.13 Ratio of minimum sensitivity factor between (a)
SCA/DCA2, (b) SCA/DCA, and (c) SCA/TCA

3.6 Design methodology

In this section, a methodology for designing a signal conditioning chopping circuit with the best performance is described. If the sensor capacitance and the desired gain are known specifications, the signal conditioning circuit can be designed with the proper chopping technique to have the minimum sensitivity factor or to have the desired sensitivity with the lowest power consumption.

The design flow graph for this design is shown in Figure 3.14. As shown in this graph, a reference amplifier is considered based on the total required gain and the given sensor capacitance. This reference amplifier should have a valid relationship between the bandwidth and the noise corner frequency as defined in (3.4), and it is used to extract the characteristics of the amplifiers for different gains while also ensuring valid relationships between the bandwidth and noise corner frequency. Moreover, characteristics of the amplifier with the minimum possible length for the input transistors are extracted. In addition, the sensitivity factor of the circuit with the minimum power consumption is determined based on the reference amplifier.

As shown in this flow graph, the preferred chopping technique in order to have the smallest sensitivity factor for a given total gain and sensor capacitance can be extracted based on Figure 3.12. If the preferred chopping technique is the SCA, then the minimum sensitivity factor is calculated from (3.33), and if the preferred chopping technique is the DCA or TCA, the minimum sensitivity factor can be calculated based on (3.35) for the DCA or (3.34) for the TCA. It is noted that in designing the minimum sensitivity factor of the DCA, the input transistor length of the first amplifier must be compatible with the minimum length allowed in the chosen technology.

In the next step, the calculated minimum sensitivity factor is compared with the desired sensitivity factor. It is impossible to have a sensitivity factor smaller than the calculated minimum sensitivity factor; but if the desired sensitivity factor is larger, then circuit can be

designed to optimize power consumption for the desired sensitivity factor. In the case of the TCA, minimum power consumption is reached by setting the same gain for the two stages. If the desired sensitivity factor is larger than the sensitivity factor of the amplifier with optimized power consumption, then the preferred chopping technique with the smallest power consumption is the TCA with the same amplification in each stage. However, if the desired sensitivity factor is smaller than the sensitivity factor of the optimized power consumption amplifier; then the sensitivity factor will be defined based on the preferred chopping region. If the preferred chopping region warrants the use of the SCA, then the value of the sensitivity factor is constant and defined by the relevant equation (i.e., (3.21)). If the preferred chopping region requires the use of the TCA or the DCA, then based on the distribution of gain between the two stages, there is a range for which the sensitivity factor can be equal or smaller than the desired sensitivity factor. In this case, K must be chosen properly to achieve the desired power consumption and sensitivity factor.
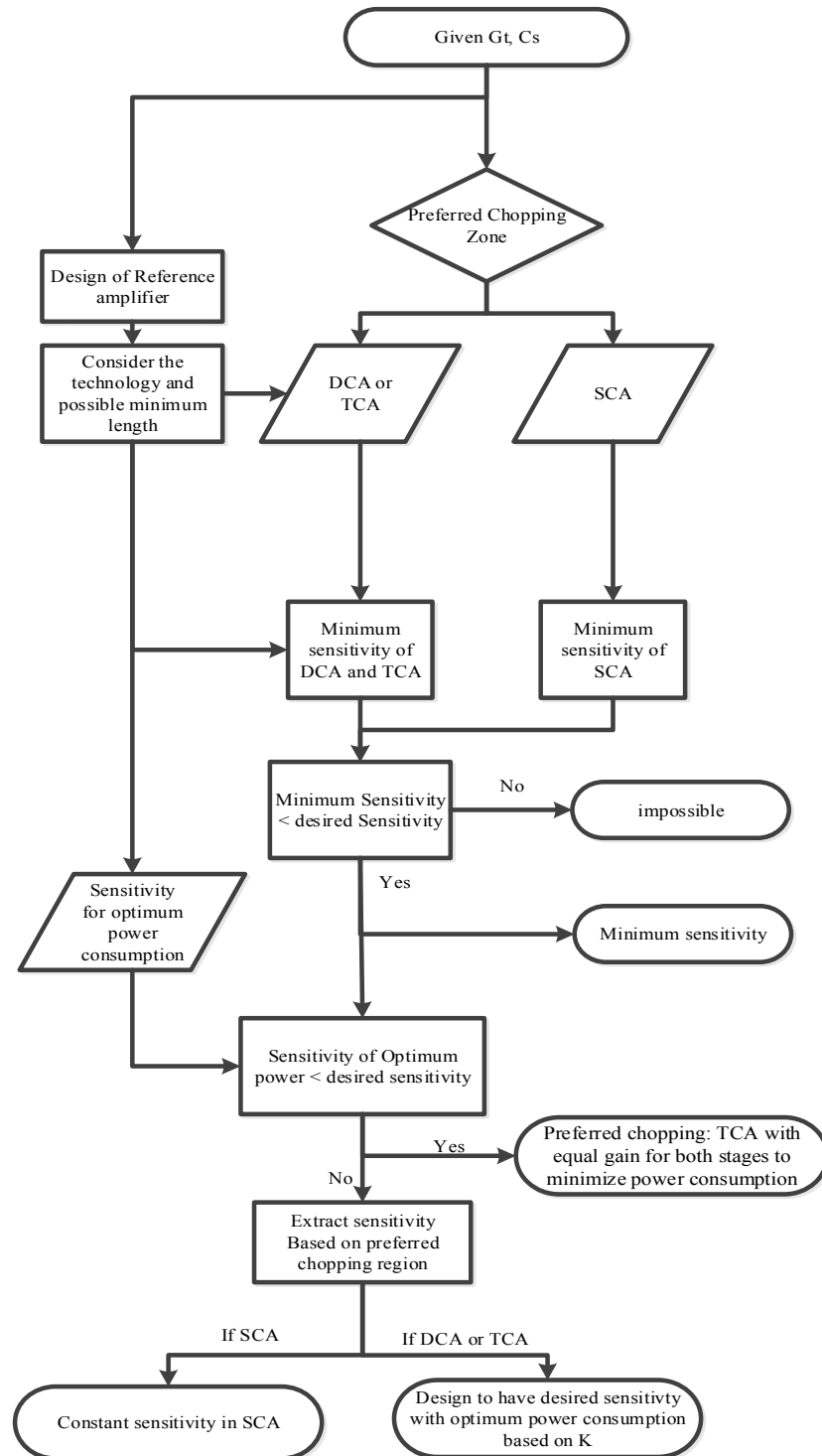
Figure 3.14 Flow graph of the preferred chopping technique
based on total gain and sensor capacitance.

3.7   Conclusion

In this work, it was shown that both the noise and input parasitic capacitance are important factors in determining the sensitivity factor of an interface circuit for a capacitive sensor. A sensitivity factor was defined based on the noise and input parasitic capacitance to be able to compare the sensitivity factor obtained in different conditions. The three chopping techniques of the DCA, SCA and TCA were considered, and their sensitivities for different gains and sensor capacitances were analyzed. Different possible designs were analyzed and the resulting sensitivity factor was extracted. It was shown that the distribution of gain between the two stages in the DCA and TCA has a significant effect on the sensitivity factor and based on this distribution, the sensitivity factor and power consumption vary significantly. For a large gain and small sensor capacitance, the effect of the loading factor is dominant and the DCA has an extra degree of freedom to decrease the input capacitance of the first amplifier and decrease the loading factor; which contributes to a smaller sensitivity factor. For a small gain and large sensor capacitance, the capacitance loading factor is small so the SCA can be suitable. The DCA has the smallest sensitivity factor, and is the most suitable for a small sensor capacitance and large required gains. In this condition, the gain of the first amplifier of the DCA can be set 1 to act as a parasitic capacitance buffer and reduce the capacitive loading effect of the amplifier to minimize the sensitivity factor. For a moderate gain and large sensor capacitance, the TCA is preferred. Moreover, the lowest power consumption is obtained by using the TCA with the same gain for the first and second amplifiers, if that architecture is well suited to the required sensitivity.

Accordingly, this work has presented an analysis of three chopping architectures that can be selected when designing a capacitive interface circuit, and it has outlined the design constraints and guidelines to achieve a well-designed sensing system that ensures that the required gain can be achieved without degrading sensitivity because of capacitive loading. It has also outlined considerations to reduce the power consumption of the designed circuit by preventing the over-design of the amplifier characteristics.

Acknowledgments

Author contributions

K.A. and P.V. and F.N conceived and designed the experiments; P.V. performed the experiments; P.V. and F.N. analyzed the data; P.V. wrote the paper; F.N. and K.A. revised the manuscript critically.

DUAL-PATH AND DUAL-CHOPPER AMPLIFIER SIGNAL CONDITIONING CIRCUIT WITH IMPROVED SNR AND ULTRA LOW POWER CONSUMPTION FOR MEMS

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Abstract

A dual chopper amplifier (DCA) signal conditioning circuit with ultra-low power consumption is presented for microelectromechanical systems (MEMS) transducers. In the first stage, a low voltage high current amplifier is implemented, which improves the power consumption and noise floor. The second stage is composed of two parallel paths that improve SNR and provide two gain settings. To mitigate flicker noise, the amplifiers are chopped at two different frequencies, also providing an additional degree of freedom to the design. The circuit is designed in a 0.13 µm CMOS technology with 0.7 V and 1.2 V supplies. The power consumption is of 2.66 µW at the 0.7 V supply and 3.26 µW at the 1.2 V supply. For a 1.6 mV input, in single path mode, the DCA has a gain of 34 dB, a bandwidth of 4 kHz and achieves an SNR of 89.06 dB in the frequency range of 0.5-4 kHz. In dual path mode, the DCA has a gain of 38 dB, a bandwidth of 3 kHz and achieves an SNR of 92.85 dB in the frequency range of 0.5-4 kHz. The effect of the chopper at the second amplifier in the single path and dual path modes is detailed.

Index Terms: Chopper amplifier, capacitive sensor, high sensitivity, low power, dual chopper, high signal to noise ratio, low power efficiency factor, signal conditioning circuit.

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4.1 Introduction

Today, CMOS-MEMS based sensors are implemented in a wide range of applications such as smart phones, communications, health care, automobiles, navigation systems, chemical reactors, and guidance systems (Blaschke et al., 2006; Mohammed, Moussa, & Lou, 2011; S. Wang et al., 2016; J. Zhao, Jia, Wang, & Li, 2007). This is due in part to their high sensitivity, low power consumption and high reliability (Jiangfeng, Fedder, & Carley, 2004a).

Different sensing techniques have been used to detect the signals stemming from MEMS transducers. These include capacitive sensing (Nizza, Dei, Butti, & Bruschi, 2013; Scotti, Pennisi, Monsurrò, & Trifiletti, 2014; Shiah & Mirabbasi, 2014; Sun et al., 2011; H. Xu, Liu, & Yin, 2015) and piezoresistive sensing (Bazaei, Maroufi, Mohammadi, & Moheimani, 2014; Stassi, Cauda, Canavese, & Pirri, 2014), for instance. Detected signals in MEMS sensors are typically in the microvolt range in voltage mode sensors or in the attofarad range in capacitive mode sensors (Tan et al., 2011). Therefore, signal conditioning circuits are designed to respond to microvolt-level signals at frequencies near DC. This poses stringent requirements on the near-DC performance of these sensors, notably with regard to flicker noise mitigation. For these applications, different methods have been proposed to detect signals at low frequencies and improve the noise performance. Chopper amplifiers are well suited for this purpose, because they mitigate flicker noise and DC offset (Shiah & Mirabbasi, 2014; Witte et al., 2007).

Single chopper amplifiers generally require high power consumption to achieve the necessary gain, and also have a large input parasitic capacitance (P. Vejdani, Allidina, & Nabki, 2016). Alternatively, dual chopper amplifiers (DCAs) reduce the power consumption by using two different chopping frequencies, which provides an additional degree of freedom for the design . (Hongzhi et al., 2011). In DCA architectures, there are many parameters that influence each other and many trade-offs should be considered in order to yield an optimized design for sensing applications. These parameters include the capacitance of the input transistors, the overall gain, the bias currents, the relation of the flicker noise corner frequency to the chopping

frequencies, and the thermal noise floor. The flicker noise corner frequency directly defines the chopping frequency, as it should be much larger than the corner frequency in order to prevent down-folding of flicker noise (Nielsen, 2004). Importantly, the chopped amplifier must provide sufficient bandwidth to support the chopping frequency. Moreover, the ratio of chopping frequencies to each other and to the input frequency should be large enough to prevent intermodulation harmonics. A low pass filter, integrated in the proposed circuit, is needed to remove the harmonics at the output.

In addition, chopper switch non-idealities are important to consider, mostly with respect to charge injection that causes additional noise currents. This poses constraints on the size of the switches and the chopping frequency (J. Xu et al., 2013). A larger chopping frequency results in larger current noise and if a large impedance is connected to the switches, large voltage noise is observed. Nested chopping can be implemented between stages to reduce these non-idealities. Improper design of these parameters can lead to larger power consumption, higher noise or degraded sensitivity.

In (Qu et al., 2008), a DCA is presented, but it is not optimized based on the distribution of the gain between the two stages, and the minimization of the input capacitance is not considered in the circuit design and noise optimization. Moreover, no integrated filter is added at the end of the circuit to remove the harmonics, and the effect of current noise is not considered. In (Hongzhi et al., 2011), a DCA is implemented where it is assumed that the noise of the first amplifier is dominant and the DCA is optimized based on the total power consumption and the noise of the first amplifier only, not considering the second stage. However, the total noise performance of the DCA depends on the gain distribution between its two stages, and it is possible that the noise of the second stage is not mitigated completely by the gain of the first amplifier (Parisa Vejdani, Allidina, & Nabki, 2017). As such, careful design is important in order to achieve optimal performance.

Accordingly, the aim of this paper is to present a DCA circuit architecture to provide high gain along with ultra-low power consumption as well as low thermal noise in order to improve sensitivity. The design is optimized for power consumption and noise performance, while

minimizing its input capacitance to be well suited to capacitive mode MEMS sensors as well. Additionally, by applying dual paths at the second chopping frequency, a higher gain setting and higher SNR can be achieved at the cost of additional power consumption, if required. In (P. Vejdani, Bouchami, & Nabki, 2017), a dual path DCA and its simulation results were presented. This paper expands on that work and presents an expanded analysis and the measurement results of the fabricated circuit.

The paper is structured as follows. First, the proposed circuit architecture is described in section 4.2. This is followed in section 4.3 by a description of the circuitry designed to implement the architecture in a standard 0.13 μm CMOS technology. Finally, measurements are presented in section 4.4, and are followed by a conclusion.

4.2   Architecture of the proposed circuit

Figure 4.1 depicts the block diagram of the proposed signal conditioning circuit, as well as conceptual plots of the signal and noise spectrum at different points throughout the circuit. The circuit is composed of two cascaded parts. The first part consists of a chopped amplifier A_1. This part is followed by a dual-path structure that can have either one or two paths activated. This dual path consists of two identical amplifiers A_2 and A_3, followed by an adder. The output of the adder is filtered with an active low-pass filter to attenuate spurs at the output. To reduce the noise and improve the SNR, both paths can be enabled, which is beneficial on two fronts: firstly, to reduce the noise by a noise correlation effect, and secondly, to improve the SNR. These benefits will be discussed in this section.

4.2.1   Circuit overview

As shown in Figure 4.1, a capacitive mode sensor or voltage mode MEMS sensor is configured to output a signal at a frequency f_H. The sensor is configured in either a capacitive or resistive bridge, not covered in this work.
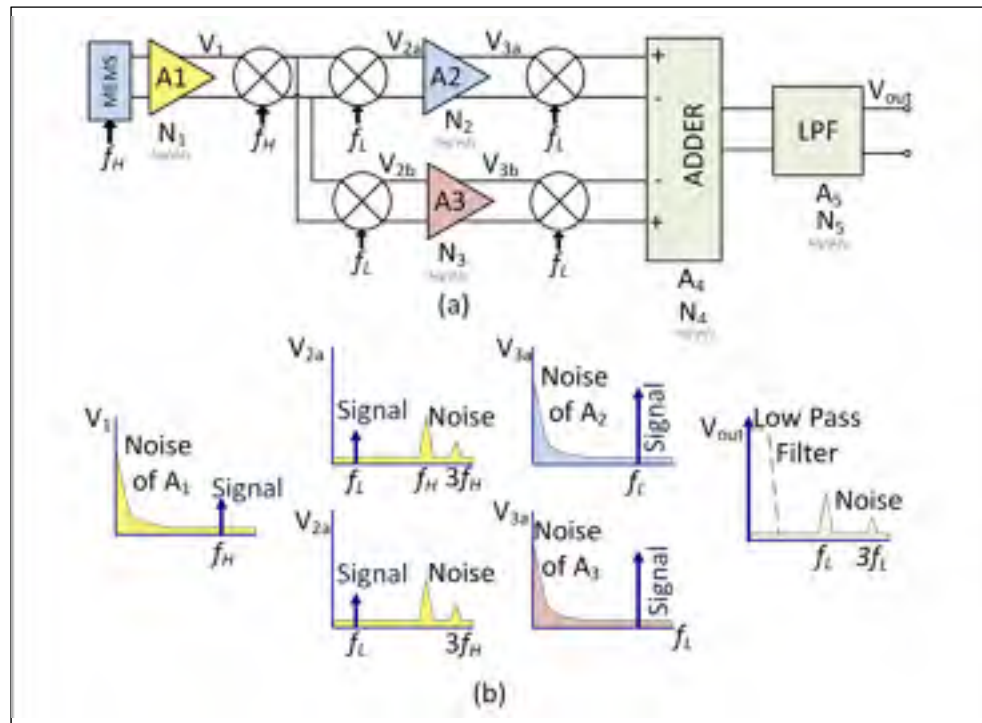
Figure 4.1 Diagram of (a) the modified DCA with an input
capacitive MEMS transducer, and (b) the spectrum of signals and
noise at key nodes of the circuit.

In the first stage, A_1 amplifies the resulting signal, which is centered at f_H. Then the signal is chopped by frequencies f_H and f_L consecutively (note that $f_H > f_L$). This nested technique is used to remove the charge injection of the f_H clock (Wu, Huijsing, & Makinwa, 2013). In the second stage, one or two parallel paths can be active. When the second path is disabled, the signal only passes through the top path in Figure 4.1 (a), and is then centered at f_L, amplified by the second stage, A_2, and chopped by frequency f_L toward baseband. When the second path is enabled, the signal is amplified in both paths, and then down-converted to baseband and added. In this work, f_H is selected to be 1 MHz and f_L is selected to be 100 kHz to ensure sufficient flicker noise mitigation and low enough power consumption in each stage. N_1 represents the input noise of first amplifier, N_2 and N_3 represnets the input noise of second amplifier in first and second paths of dual path respectively. N_4, and N_5, represents the input noise of adder and g_m-C filter, respectively.

The proposed architecture is designed to sense signals in the range of microvolts in voltage mode, while having an ultra-low power consumption. The lowest detectable voltage signal is reduced by the minimizing the input-referred noise. Thus, the gain distribution between the two stages is of significant importance, as it affects the power consumption, input parasitic capacitance as well as the input noise level. Note that minimizing the input parasitic capacitance is especially important in fully-integrated capacitive mode sensors, where interconnect parasitics are minimized, and the input capacitance of the signal conditioning circuit is the dominant parasitic, limiting sensitivity.

Thermal and flicker noise are the dominant noise sources in CMOS circuits. The chopping frequency is chosen to be 10 times larger than each amplifiers' flicker noise corner frequency in order to reduce the flicker noise to 10% of the thermal noise level (Fang, 2006b). The bandwidths of the amplifiers are chosen to be marginally larger than the chopping frequency in order to reduce their power consumption.

The use of a DCA structure allows for the choice of the first and second amplifiers' gains independently. Given that the first amplifier dominates the noise response and is designed to buffer the sensor from parasitic capacitance (for capacitive mode sensors), it is necessary to provide adequate gain to suppress the noise of the following stages, while maintaining thermal noise performance. The resulting small size of the input transistors increases the first amplifier's flicker noise corner frequency. Thus, a relatively high chopping frequency, f_H, is required which is in turn associated with elevated power consumption. Accordingly, in order to reduce the first amplifier's input-referred thermal noise while significantly reducing its power consumption, the input stage of the first amplifier is biased at a high input stage current and low supply voltage (i.e., 3.8 µA, 0.7 V). A low supply voltage can be used, as the input signal is relatively small. As previously stated, the parallel paths of the second stage are controlled such that one or two paths can operate. This enables two different gain settings and improved SNR in the dual-path mode. In each path, the signal is chopped at f_L, and also amplified and demodulated to the baseband. As the second stage input transistors do not contribute to the input capacitance of the circuit, their sizes can be increased, yielding a lower

flicker noise corner frequency. This in turn allows for a lower chopping frequency, f_L, and a reduced power consumption.

4.2.2   Noise overview

In Figure 4.1, amplifiers A_2 and A_3 have the same structure and their output signals are chopped with the passive mixers and then are summed at the adder. The noise of each path includes the thermal noise of the amplifiers and the noise that is produced by switch non-idealities. The latter includes residual offsets, charge injection and clock feedthrough. Charge injection is the dominant noise related to switch non-idealities (J. Xu et al., 2013). It causes current noise that converts to voltage through the impedance that is connected to the switches. The charge injection noise can be reduced by choosing small dimensions for the switch transistors and choosing a low chopping frequency. In (Nielsen, 2004), it was shown that to prevent flicker noise down-folding, the chopping frequency should be at least 10 times larger than the flicker noise corner frequency. However, the flicker noise corner frequency will be decreased by increasing the current and transistor sizes. As such, decreasing the charge injection effect is at the cost of more power consumption of the amplifiers if a single path structure is used. In the dual path structure, the noise of the amplifiers are uncorrelated. However, matched layout of the switches and of the amplifiers results in a similar offset and charge injection in the two paths, correlating much of the switching noise. The noise related to switch non-idealities can then be removed in the adder. Moreover, other sources of common-mode noise which exist in the two paths can be mitigated in the adder (e.g., supply noise).

The noise structure composed of the two paths and the adder is shown in Figure 4.2 (a), and the current noise summation is shown in Figure 4.2 (b).
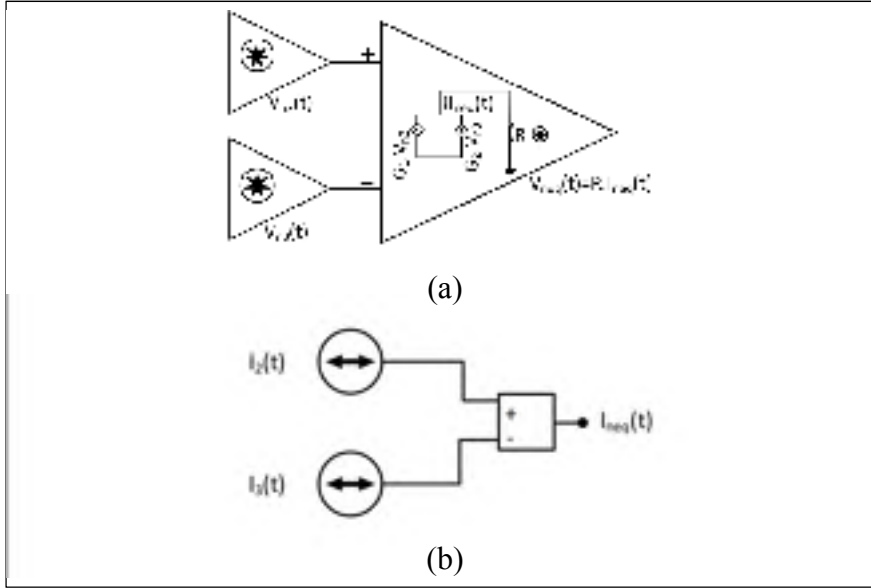
Figure 4.2 Diagram of (a) the noise voltage summation of the amplifiers in the dual path, and (b) the resulting equivalent summation of their noise current.

The noise of both paths are converted to a current in the adder through transconductances. The adder is a g_m-C filter with two differential pairs that yield the transconductances, and each path is connected to one of its input pairs with an opposite polarity. The noise currents are added together and then converted to a voltage by a resistive load and the output of the adder. The related noise formula is given by:

$$V_{n,eq(rms)}^2 = \left(G_1 . V_{n2(rms)} - G_2 . V_{n3(rms)} \right)^2 . R^2 \tag{4.1}$$

where G_1 and G_2 are the transconductances of the input transistors in the adder, and are of the same value, R is the output load of the adder, V_{n2} and V_{n3} are the output noise voltages of the first and second path, respectively. Considering some correlation between the noise sources of these paths, the equivalent noise at the output of adder can be given by:

$$V_{neq(rms)}^2 = \left(V_{n2(rms)}^2 + V_{n3(rms)}^2 - 2\alpha V_{n2(rms)} . V_{n3(rms)} \right) A_4^2 \tag{4.2}$$

where A_4 is the gain of the adder, α is the correlation coefficient, between the paths' noise sources, ranging from 0 to 1. For uncorrelated values, α is 0, and for fully correlated values, α is 1 (Stein, 2001). As was mentioned, in this circuit, a correlation between both parallel paths exists, so α is expected to be larger than 0, but there are some uncorrelated sources between two paths, so α cannot be 1. The exact value of α is dependent on the ratio of the noise of the switches to that of the amplifiers. If the noise of the switches is more important that than of the amplifiers, then α is expected to be larger. The output noise of the dual path DCA is given by:

$$V_{no(rms)}^2 = 2.A_2^2.A_4^2.A_5^2.V_{n1(rms)}^2 + \qquad (4.3)$$
$$V_{neq(rms)}^2 A_5^2 + A_5^2.V_{n4(rms)}^2 + V_{n5(rms)}^2$$

where A_2 is the gain of amplifiers A_2 and A_3, which have identical gains, A_5 is the gain of the low pass filter and V_{n4} and V_{n5} are the output noises of the adder and the low-pass filter, respectively.

4.2.3   SNR improvement

In Figure 4.3, three different structures of cascaded amplifiers are shown for comparison. In this figure, A_1 and N_1 represent the gain and input noise of the first amplifier, respectively. A_2 represents the gain of the second amplifier. N_2 and N_3 represent the input noise of first path and second path in the second stage, respectively. Since the paths are symmetric, N_2 and N_3 have the same value. Finally, N_4 and N_5 represent the input noise of the adder and the low pass filter, respectively.

Figure 4.3 (a) represents a single-path structure, and Figure 4.3 (b) represents a signal-path structure with doubled gain in the second amplifier. In Figure 4.3 (c), the higher gain comes at the cost of increasing the power consumption, while the noise level is reduced by a factor of $\sqrt{2}$. This is an estimation for the noise reduction, and it is assumed that the transconductance of the input transistors and the output resistors are increased by the same ratio, and that the noise of the input transistors is dominant. This is the optimal value of the reduction in noise

and this reduction can be lower in reality. The structure in Figure 4.3(c) yields similar gain, but has a noise benefit as is shown in Table 4.1, where the gain, output noise and SNR related to these three structures are listed. As shown in this table, the structures in Figure 4.3 (b) and Figure 4.3(c) have the same gain, but the output noise of the structure in Figure 4.3 (c) includes a 2X reduction in the first noise term and a correlation effect in the second noise term. When comparing the SNR related to each of these two higher gain structures, the dual-path structure improves the SNR by a factor of about two, without considering any correlation effect (i.e., 3 dB). This SNR improvement can increase if there is correlation between the noise sources of each path.
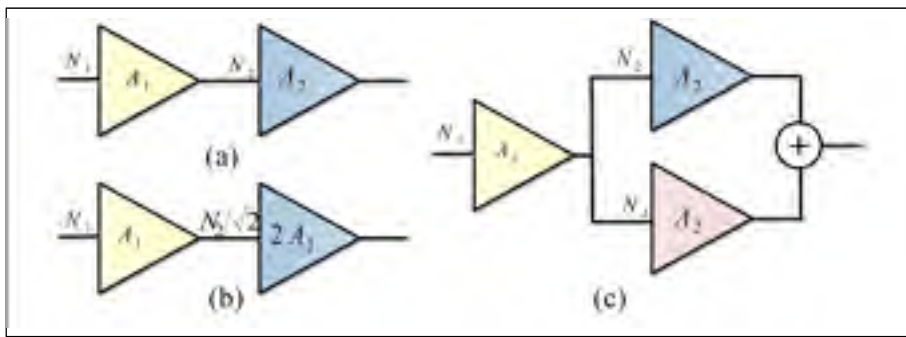
Figure 4.3 Different cascaded amplifier structures: (a)
single-path, (b) single-path with doubled second stage
gain, and (c) dual-path.

Table 4.1 Gain, output noise and SNR of the Structures in Figure 4.3.

Structure	Gain	Output Noise	SNR
Figure 4.3 (a)	$A_1 A_2$	$N_1^2 A_1^2 A_2^2 + N_2^2 A_2^2$	$\dfrac{1}{N_1^2 + N_2^2 \big/ A_1^2}$
Figure 4.3 (b)	$2A_1 A_2$	$4N_1^2 A_1^2 A_2^2 + 2N_2^2 A_2^2$	$\dfrac{1}{N_1^2 + N_2^2 \big/ 2A_1^2}$
Figure 4.3 (c)	$2A_1 A_2$	$2N_1^2 A_1^2 A_2^2 + 2(1-\alpha)N_2^2 A_2^2$	$\dfrac{2}{N_1^2 + N_2^2(1-\alpha) \big/ A_1^2}$

4.3   Proposed circuit description

Figure 4.4 depicts the circuit-level schematic of the proposed signal conditioning circuit. Complementary switches are used as passive mixers to implement the chopping operations. To set the DC bias of the amplifiers, AC-coupling capacitances (C_{ac}) are used in combination with either diode connected transistors or pseudo-resistors (R_{bias}). In addition, the capacitors and bias branches act as high-pass filters to attenuate low frequency spurs caused by the chopping of the amplifiers' DC offset (P. Vejdani et al., 2017). The R_{bias} value implemented is of 200 MΩ. To produce a resistor in this range, two series diode connected PMOS transistors are used. Using such pseudo resistors instead of large resistors reduces the required area and mitigates the large parasitic capacitances associated with large resistor values.

After demodulation to baseband, signals from the two paths are added together using an adder implemented as a two differential input g_m-C low-pass filter. In this fashion, the adder also filters the out-of-band harmonics and the up-converted flicker noise. To enable two paths, a controllable switch mixer is used and described below.
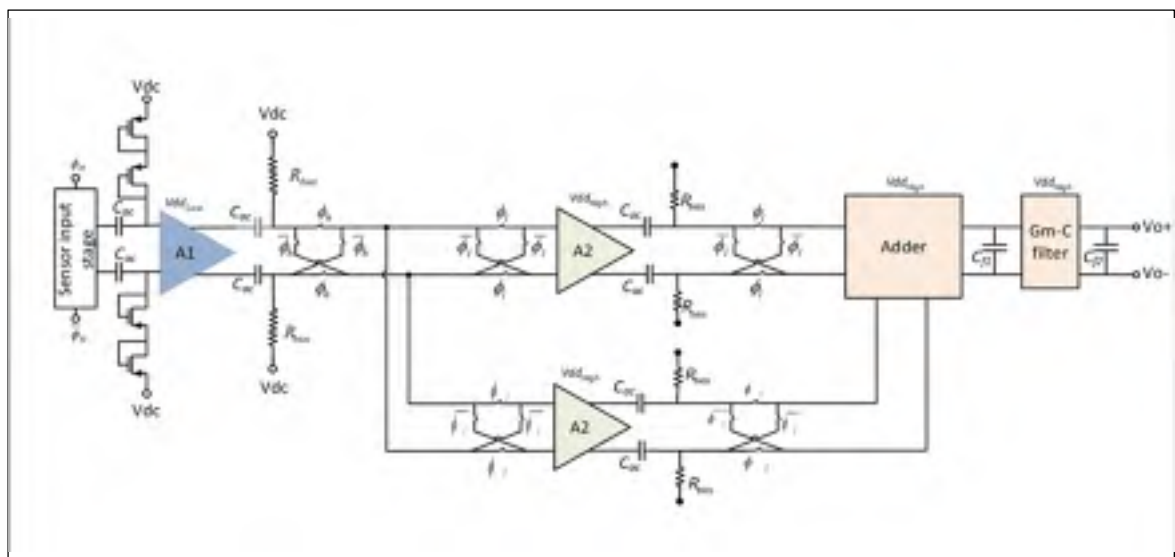
Figure 4.4 Schematic of the proposed circuit. The R_{bias} resistors are implemented as pseudo-resistors to achieve high resistance values.

4.3.1 Controllable complementary-switch mixer

The controllable switch mixer shown in Figure 4.5 (a) is used to enable or disable one of the paths in the DCA. To chop the signal, a passive switch mixer is implemented with two signals $\emptyset_1$ and $\emptyset_2$. These two signals are produced by a control circuit shown in Figure 4.5 (b). The inputs of this circuit are a control signal, *Ctrl*, and a 100 kHz clock running at the same frequency as second chopper frequency, f_L. To disable the second path, the *Ctrl* signal is pulled down to ground so that the outputs go to V_{DD} or ground. These outputs are connected to the gates of the mixer and disconnect the second path. To enable the second path, the *Ctrl* signal is pulled up to V_{DD}, so that the outputs of the control circuit provide the appropriate clocks to drive the mixer and chop the signal. In the chopping technique, clocks non-idealities result in residual offsets. To ensure effective offset cancellation, the two complementary chopping clocks must both exhibit a 50% duty cycle (Wu et al., 2013). In the proposed design, all clocks have near-50% duty cycles and clock skew is less than 0.004% of the different clock periods. Moreover, the coupling capacitors that are added after the amplifiers remove offsets and mitigate clock non-idealities-related offsets.
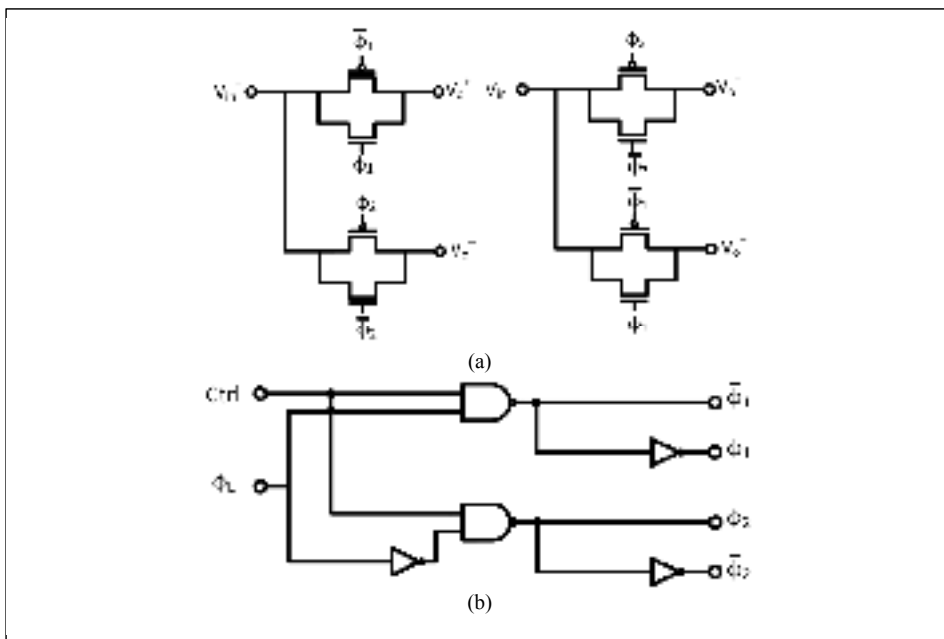
Figure 4.5 Schematic of the (a) controllable complementary-switch mixer, and (b) its control circuit.

4.3.2 First stage amplifier

The first amplifier is designed to have a small input capacitance of 10 fF. As detailed in our previous work in (Parisa Vejdani et al., 2017), the input capacitance of a sensor interface circuit can be important to maintain capacitance sensitivity of the circuit in Figure 4.6. To reduce the thermal noise and increase the transconductance, NMOS input transistors are used. However, NMOS transistors have a larger transconductance and larger flicker noise coefficient in comparison to PMOS transistors. As a result, NMOS transistors require a larger chopping frequency than for PMOS transistors. By choosing a proper chopping frequency, flicker noise can be mitigated in this amplifier. Biasing the transistors in the subthreshold region contributes to maximize the g_m/I_D ratio and also minimize the gate noise voltage (Binkley, 2008; Fonstad, 2009; H. Wang, Mora-Puchalt, Lyden, Maurino, & Birk, 2017). As a result, the input transistors are biased in the subthreshold region to lower their thermal noise, and to mitigate the thermal noise of the load transistors. Their bias current is also increased to make their transconductance larger.
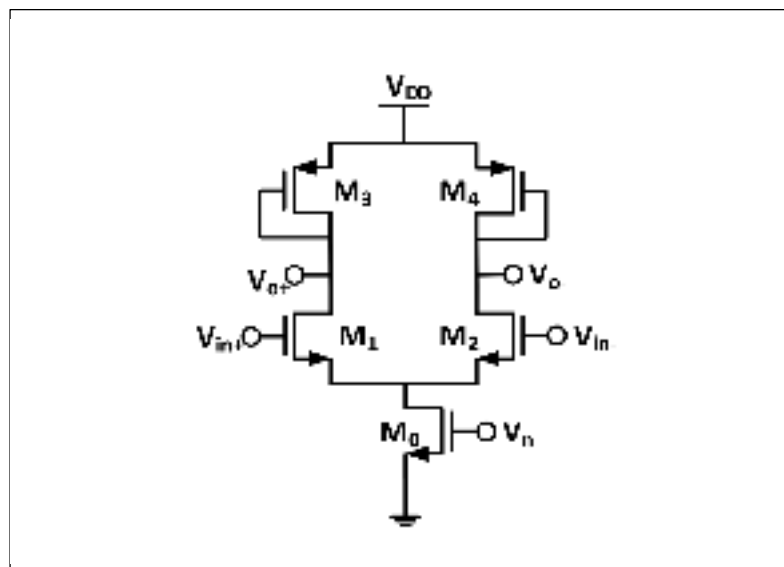
Figure 4.6 Schematic of the first stage amplifier.

The equation of the input-referred thermal noise for this amplifier is given by:

$$V_n^2 = \frac{8KT}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right),$$

(4.4)

where K is the Boltzmann constant, T is temperature, and g_{m1} and g_{m3} are the transconductances of the input transistors and load transistors, respectively. As the noise of the input transistors is dominant, careful design of the first amplifier to minimize the thermal noise of the input transistors is the most effective way to reduce the noise floor of the DCA. The larger bias current allows for a larger bandwidth, which allows for a sufficiently large chopping frequency to mitigate this stage's flicker noise. As previously discussed, this stage has a large flicker noise corner frequency because of the need to minimize capacitive input loading.

The equations of transistor current and transconductance in subthreshold region are given by:

$$I_{DS} = I_S . e^{\frac{(V_{GS} - V_T)}{nV_T}} (1 - e^{\frac{-V_{ds}}{V_T}}),$$

(4.5)

and

$$g_m = \frac{I_{DS}}{n.V_T},$$

(4.6)

where I_S is the sub-threshold saturation current (Fonstad, 2009), respectively, V_T is the thermal voltage, and V_A is the Early voltage. In weak inversion, n is related to the capacitive voltage division between the gate voltage and silicon surface potential resulting from the gate-oxide, depletion, and interface state capacitances. In weak inversion, n is expressed by:

$$n = 1 + \frac{C'_{DEP}}{C'_{OX}} + \frac{C'_{INT}}{C'_{OX}} \approx 1 + \frac{C'_{DEP}}{C'_{OX}}$$

(4.7)

where C'_{OX} is the gate oxide capacitance, and C'_{DEP} and C'_{INT} are the depletion and interface state capacitances per unit area, respectively. In weak inversion, n is approximately 1.4–1.5 for typical bulk CMOS processes.

Note that the tail current of the differential amplifier is set by a current mirror, and that its current is controllable by an off-chip resistor which can be tuned to adjust the gain of the stage and compensate the sensitivity to PVT variations. In order to accommodate a larger bias current, without a large penalty in power consumption, this amplifier is designed to operate from a lower supply voltage of 0.7 V. This also contributes to reduce the thermal noise.

4.3.3 Second stage amplifier

A folded cascode topology, shown in Figure 4.7, is used for the second stage amplifier. The input transistors are increased in size in order to reduce the flicker noise corner frequency. This enables the use of a lower chopping frequency, resulting in a smaller bandwidth requirement and reduced power consumption. The input stage of this amplifier is composed of NMOS transistors which are biased in the subthreshold region to have larger transconductance and reduce the noise impact of the other transistors in order to attain reduced thermal noise. Biasing the input transistors in the saturation region could contribute to better matching at the cost of added power consumption and increased noise. In this design, these transistors are biased in the subthreshold region to decrease the power consumption and noise. This amplifier operates at a supply voltage of 1.2 V as it must provide better linearity. This does not significantly increase this stage's power consumption, as its bias current can be kept low by making the input transistors bigger. *M9* and *M10* are utilized as common mode feedback transistors and are biased in the triode region. Their gates are connected to the output voltage and they control the tail current to set the output bias. This makes the output bias relatively independent of device parameters and lowers the sensitivity to bias V_b (Razavi, 2001).
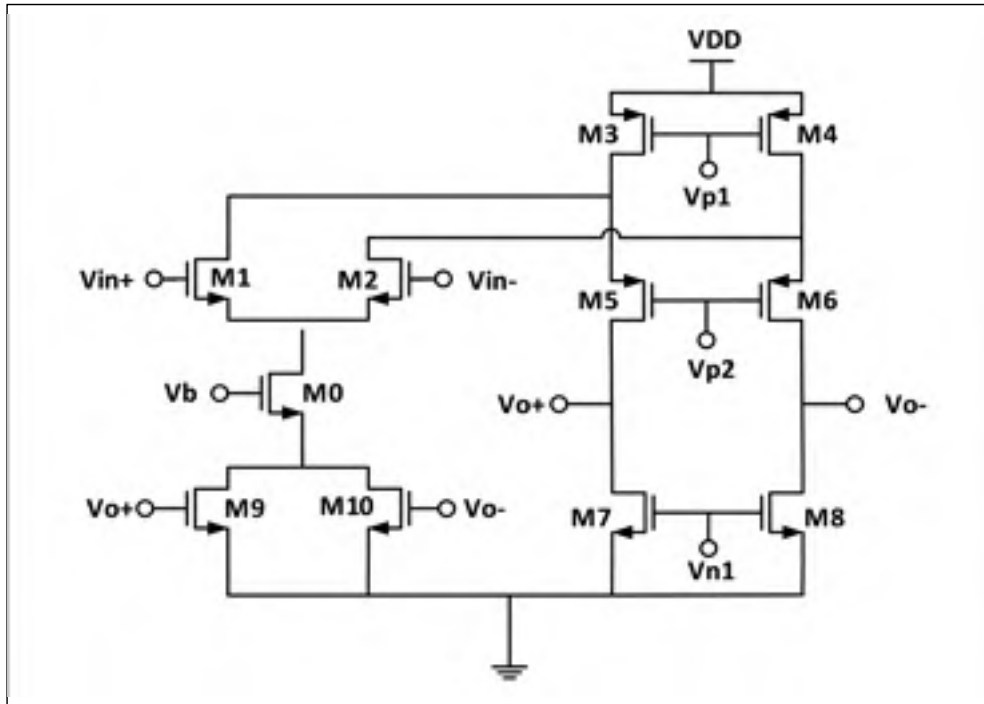
Figure 4.7 Schematic of the second stage amplifier.

4.3.4   Adder and g_m-C low pass filter

The adder circuit is shown in Figure 4.8. This circuit also includes an embedded g_m-C low-pass filter to attenuate spurs caused by the chopping. To add signals from the two paths, two differential-input pairs are used and their output currents are added in the polarity previously outlined. Source degeneration transistors M_5-M_8 are used in order to increase the linearity of the input transistors. The g_m-C low-pass filter is implemented by adding a capacitance between the branches where the currents from both input differential pairs are added. Capacitance C_f is set to 15 pF to provide a sufficiently low bandwidth of 10 kHz. The adder operates from a 1.2 V supply.

Another g_m-C low-pass filter is cascaded to this adder in order to attenuate further out-of-band frequency spurs. This second filter has the same structure as the adder but with only one differential input pair. The simulated power consumption of the adder is of 0.91 μW, and the simulated power consumption of the low pass filter is of 0.48 μW.
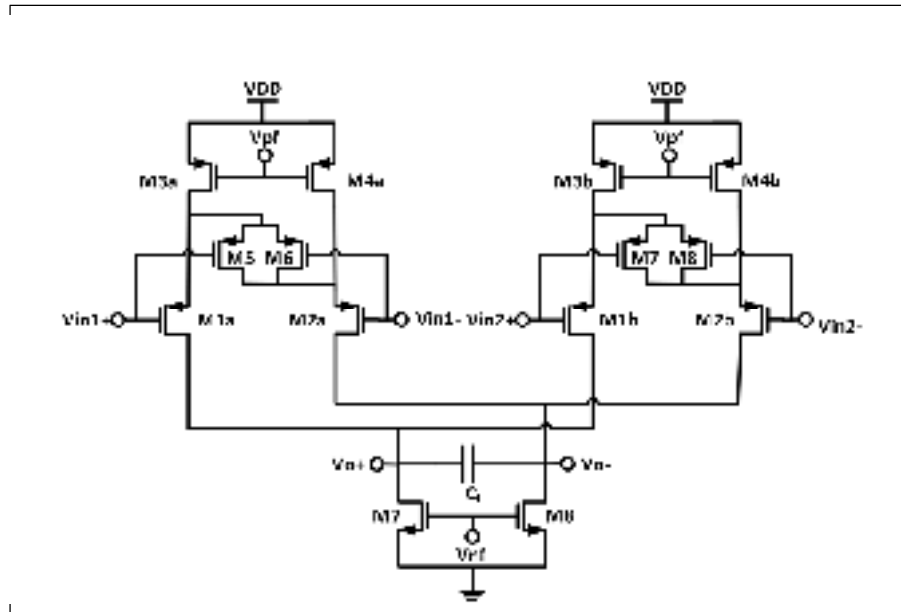
Figure 4.8 Schematic of the adder with embedded g_m-C filter.

4.3.5   Measurement results and comparison

The proposed circuit was designed in Global Foundries 0.13 μm CMOS technology with 0.7 V and 1.2 V supplies. The circuit occupies an active area of 550 × 250 μm, outlined in Figure 4.9. The frequency response of the DCA in single path and dual path modes are shown in Figure 4.10. For this measurement, the input signal is a sine wave that is mixed on-chip with a square wave chopping signal. The spectrums were computed using MATLAB by using time-based measurements that were taken with an oscilloscope. This figure shows gains of 34 dB and 38 dB for the single path mode and dual path mode, respectively. The DCA in dual path mode improves the gain by 4 dB over that of the single path mode. The bandwidth of the dual mode, 3 kHz, is slightly lower than the single path mode, 4 kHz. Parasitic capacitances that are switched into the circuit when the second path is enabled cause the reduction in bandwidth seen in dual path operation. These mismatches also cause the gain of the dual path mode to be 4 dB higher that the single path mode, rather than the 6 dB expected from the ideal analysis presented in Table 4.1.
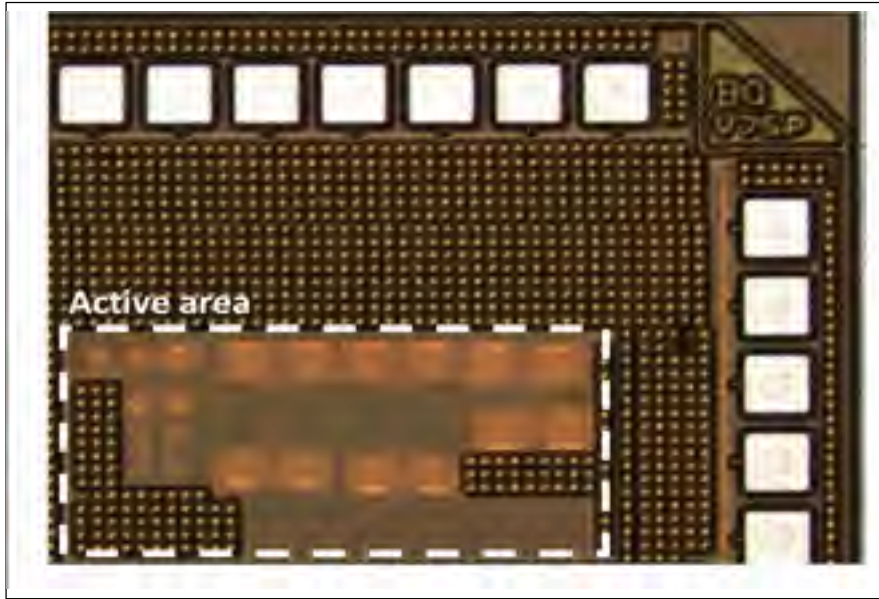
Figure 4.9 Micrograph of die active area of 550 × 250 μm.

The output voltage resulting from a 1 kHz sine input of 1.25 mV in single path mode with and without the second chopper stage activated is shown in Figure 4.10. The second chopper stage results in more high frequency signal noise. Note that part of this high frequency noise is due to 100 kHz clock feedthrough. In the package, the output pin was unfortunately placed too close to this clock pin, causing capacitive feedthrough of this clock to the output signal. This was confirmed by measuring the impact of this feedthrough without bonding a die in the package and observing the output with the clock applied to the clock pin. This capacitive feedthrough represents most of the high frequency noise seen Figure 4.10. When plotting the spectrum of the output, this feedthrough was removed mathematically. To do this, the clock feedthrough is measured without bonding a die within the package to isolate package-related feedthrough. The measured feedthrough is used as the baseline to subtract it from the measurement result with the wire bonded die.
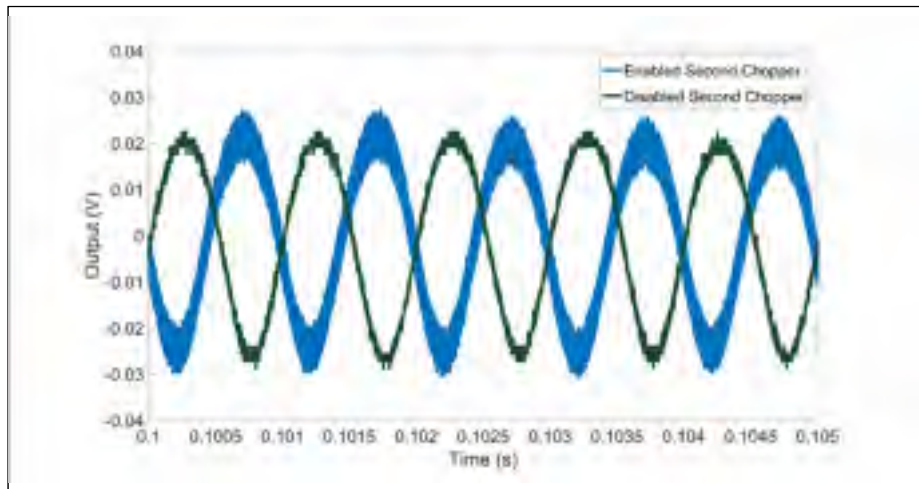
Figure 4.10 Output voltage the DCA in single path mode with
and without the second stage chopper being active.

The input-referred noise voltage over frequency of the DCA in single path and dual path modes is shown in Figure 4.11. The accurate measurement of the noise is not possible at frequencies below 1 kHz. This is because the flicker noise of an off-chip amplifier used to amplify the noise sufficiently to capture it impacts the noise performance recorded at these lower frequencies. The noise floor at 2 kHz is observed to be around 40 nV/$\sqrt{\text{Hz}}$ for the DCA in single path mode and of around 55 nV/$\sqrt{\text{Hz}}$ in dual path mode. Comparing the noise of the single path and dual path mode outlines that the noise of second amplifier has some effect on the total noise. As a result, when the second path is activated, the total noise increases. On the other hand, the dual path mode increases the gain as well, which ultimately results in an improved SNR, as will later be discussed.

The integrated input-referred noise voltage of the DCA in single path and dual path modes for different 500 Hz frequency integration ranges is shown in Figure 4.12 with the second amplifier either chopped or not. As shown in this figure, chopping of the second stage reduces the noise overall. Here as well, the off-chip amplifier used to measure the noise level does not allow an accurate measurement of the noise at low frequencies (i.e., below ~1 kHz).
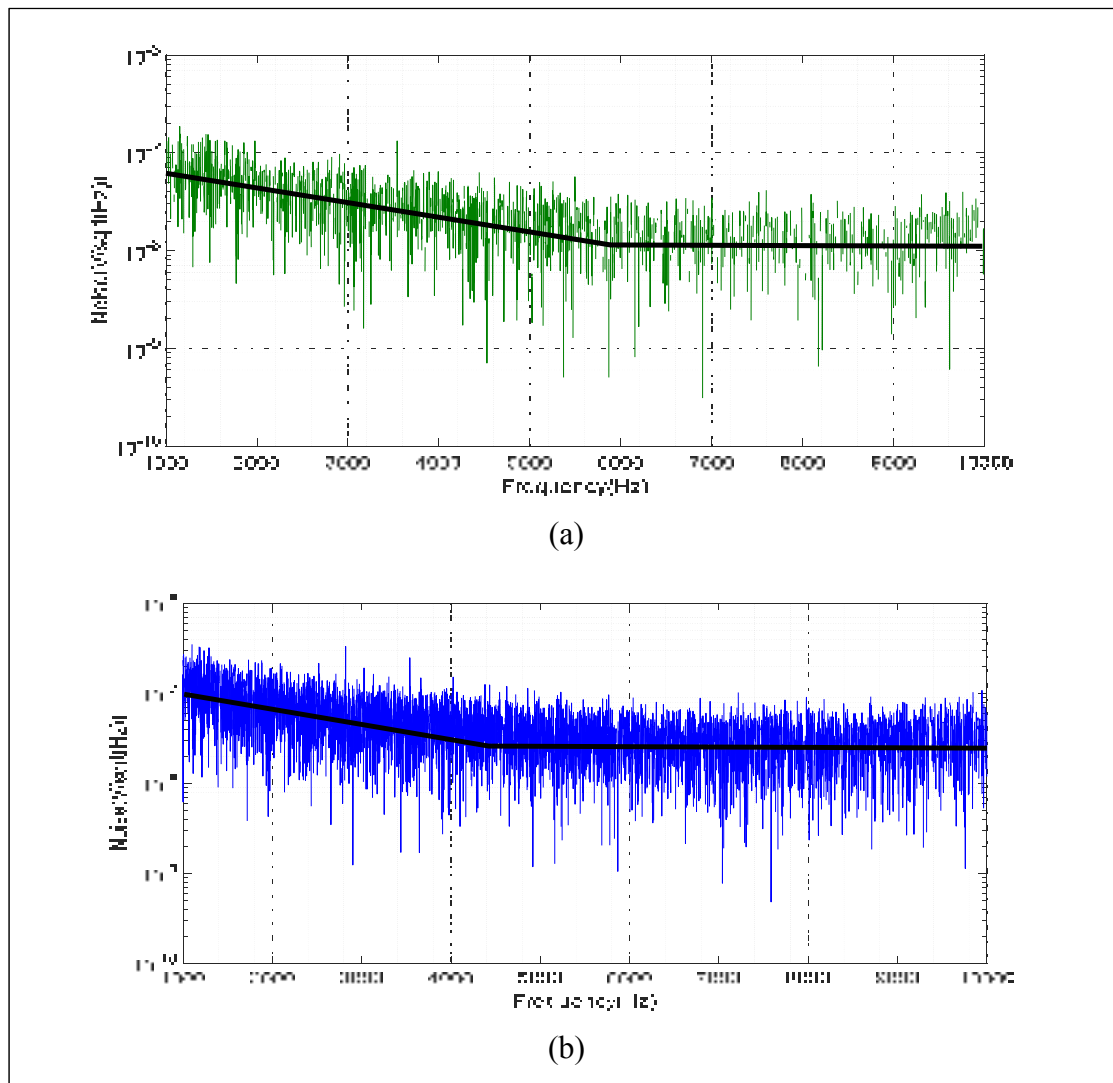
Figure 4.11 Input-referred noise voltage over frequency of the DCA in (a) single
path mode, and (b) in dual path mode.

Table 4.2 shows the integrated input-referred noise voltage of the DCA in single path and dual
path modes with and without chopping of the second stage. Noise values are listed over the
$0.5 - 4$ kHz and $1 - 4$ kHz integration frequency ranges. The related SNR is also listed over
the same frequency ranges for an input signal of 1.6 mV at a frequency of 1 kHz. As shown in
this table, the chopping of the second stage improves the SNR by 2.6 to 3.7 dB, as a result of
the reduced noise level. Also, the SNR in the single path mode is lower than that of the dual
path mode by 3.3 to 4.9 dB. This is because of the fact that, in addition to increasing the gain

in dual path mode, the noise correlation between the paths causes smaller integrated noise. Moreover, the DCA in dual path mode exhibits lower charge injection related spurs due to the addition operation. This also contributes to the enhancement of the SNR.
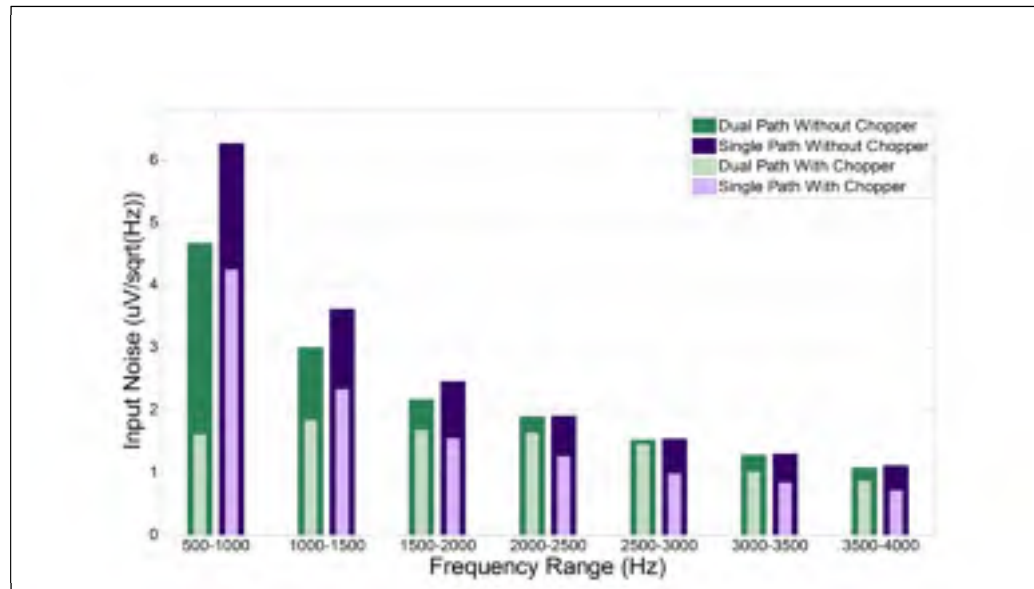
Figure 4.12 Integrated input-referred noise voltage of the DCA in single path mode and in dual path mode within 500 Hz integration ranges.

Table 4.2 Integrated Input-referred Noise Voltage (Int. Noise) and SNR of the DCA

Structure	Int. Noise(μV) 0.5-4 kHz	Int. Noise(μV) 1-4 kHz	SNR(dB) 0.5-4 kHz	SNR(dB) 1-4 kHz
Single path mode with 2nd chopper	4.74	3.16	89.06	93.09
Single path mode without 2nd chopper	6.83	4.41	85.40	90.20
Dual path mode with 2nd chopper	5.15	3.45	92.85	96.33
Dual path mode without 2nd chopper	6.65	4.73	90. 3	93.59

The SNR and THD of the DCA in single path and dual path modes for different 1 kHz inputs signal amplitudes and over a bandwidth ranging from 1 kHz to 4 kHz is shown in Figure 4.13 As shown in this figure, the dual path mode has higher SNR over all the signal amplitudes tested. The THD is similar between both modes except at the highest tested input amplitude where the larger gain of the dual mode starts to exert the non linearity of the later stages. As expected, with an increasing input amplitude, the SNR is increased while THD is degraded. The maximum SNR is reached for a 4.75 mV input signal amplitude. Beyond this point, the SNR decreases because of the compression of the DCA gain (not shown in the figure).

The output spectra of the DCA in single path and dual path modes are shown in Figure 4.13 for a 1 kHz 1.25 mV input. These spectra are shown with and without chopping of the second stage. As shown in this figure, the choppers do not have any significant effect on the amplitude of the amplified signal, and the chopping of the second stage improves performance (e.g., mitigates DC offset of the second stage), albeit adding a spur at 100 kHz. When the second chopper is disabled, the intermodulation between the input signal and the offset yields more spurs at low frequencies. The signal is amplified more in the dual path mode, by a factor of 1.6X. An even harmonic spur at 2 kHz can be seen in all of the spectra plotted. It is due to the mismatches between the differential circuitry. When the second stage chopper is activated, a spur is generated at 100 kHz, the second chopping frequency.

The charge injection of the first chopper is mitigated with the nested chopper technique, and the g_m-C filter attenuates the out of band harmonics and charge injection of the second chopper. Although this charge injection is reduced partially, it cannot be removed completely. To attenuate these spurs further, a higher order filter can be implemented at the cost of higher power consumption.

The DCA performance in single-path and dual-path mode is summarized in Table 4.3, and is compared to others works. As can be seen, the power consumption is decreased significantly in comparison to other works. As shown in the table, the dual path increases the gain and improves SNR. High current and low supply voltage biasing of the first stage contributes to

increasing the achieved gain and lowering the noise. The power efficiency factor (PEF) is used to describe the power/noise trade-off and a lower PEF indicates a more efficient design (Muller, Gambini, & Rabaey, 2012b).
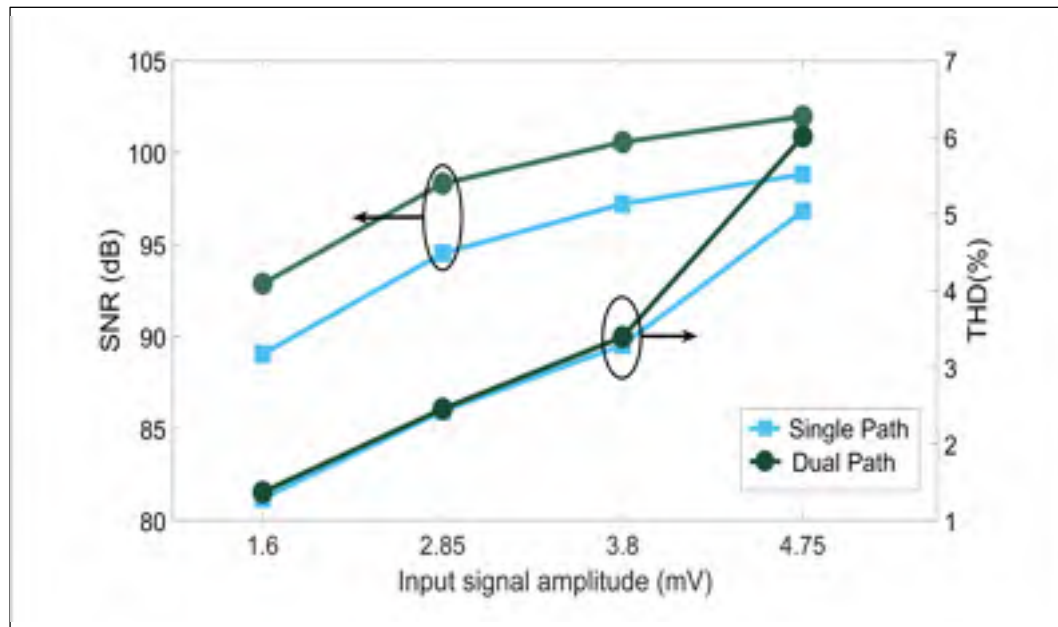
Figure 4.13 SNR (0.5 – 4 kHz) and THD of the DCA in single path mode and dual path modes for different input signal amplitudes.

In the proposed DCA, the PEF is less than that of the other works, indicating that this circuit is optimized for both noise and power consumption. In all of the works which are shown in Table 4.3, a single chopper amplifier is used, which results in more power consumption. In (Maruyama et al., 2016), an optimized chopping frequency and the biasing of the transistors in the subthreshold region results in a low noise floor. However, the input capacitance is not considered in the design, so integrating of this circuit with a capacitance transducer may cause degradation of the sensitive due to capacitive loading. In (H. Wang et al., 2017) a combination of chopping and auto zeroing is proposed. Implementing the auto zeroing results in noise aliasing and an increased noise floor. Moreover, the capacitance feedback degrades the capacitive sensing performance (i.e., reduced sensitivity), as it increases the circuit's input capacitance. The work in (S. Wang et al., 2016) is a capacitive signal conditioning circuit where a single chopping amplifier with an input capacitance parasitic cancellation circuit.

However, this circuit will add extra flicker noise to the input referred noise and the power consumption is relatively high, because of the SCA structure. In (Jiang et al., 2017), an ultra-low noise circuit is designed for resistive sensing. The PEF of 44.1 for this circuit shows that a relatively high power consumption is needed to reach this reduced noise floor.

Overall, the proposed circuit compares favourably to other works and presents well-rounded performance tailored to capacitive sensing and with consideration for noise and power consumption metrics.

Table 4.3 DCA measured performance summary and comparison

	This work		(Maruyama, Taguchi, Yamanoue, & Iizuka, 2016)	(H. Wang et al., 2017)	(S. Wang et al., 2016)	(Jiang, Makinwa, & Nihtianov, 2017)
	1 path	2 paths				
Technology (nm)	130		160	180	350	180
Supply (V)	0.7, 1.2		1.55	2.7-3.6	-	1.8
Power (µW)	2.66 (0.7 V) 3.26 (1.2 V)		2015	270	92	2160
Bandwidth (kHz)	4		3	-	-	0.1 to 10
Gain (dB)	34		38	-	0-42	29.6
Noise Floor (nV/√Hz)	40 @2 kHz	55 @2 kHz	8.2	19	1960	-
SNR (dB) (0.5 – 4 kHz)	89.06[*] 98.82[**]	92.85[*] 101.90[**]	-	-	31.28	-
PEF	11.04	13.8	14.2	-	-	3.7
1-dB comp. (mV)	4.75	3.95	-	-	-	-

Notes: [*]for a 1 kHz sine input of 1.6 mV; [**]for a 1 kHz sine input of 4.75 mV

4.4   Conclusion

A DCA signal conditioning circuit with low noise and ultra-low power consumption for MEMS transducers was proposed. Two supply voltages are used to reduce the power consumption while minimizing the noise floor. The sub 6-µW power consumption is significantly lower than similar works. The first amplifier is chopped with a nested chopper to remove its flicker noise and prevent charge injection. The performance of the DCA was shown with and without the chopping stage of the second amplifier to outline the advantages of the second chopping stage, notably improving SNR by 2.6 to 3.7 dB. The chopping of the second amplifier improves the noise but results in charge injection at the output. Implementing a higher order filter and smaller amplitude for the chopping signal can improve this.

Two parallel paths are implemented in the second stage of the DCA to achieve improved SNR and enable a configurable gain. It was shown that the dual-path mode improved SNR by 3.3 to 4.9 dB and increases gain by 4 dB. In the dual path mode, some noise correlation was observed to enhance the SNR improvement due to the noise current addition performed.

Moreover, the input capacitance of the circuit is minimized to be suitable for high sensitivity fully-integrated capacitive mode sensors. The impact of this input capacitance reduction on the noise performance is minimized by leveraging the added design freedom provided by the DCA structure.

Overall, the proposed circuit enables a high SNR with minimal capacitive loading in order to be amenable to direct integration with MEMS capacitive mode and voltage mode transducers.

CHAPITRE 5

HIGHLY POWER EFFICIENT LOW-NOISE SIGNAL CONDITIONING CIRCUIT WITH SUB-µHz NOISE CORNER FREQUENCY AND TUNABLE BANDWIDTH

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Abstract

This letter introduces a low noise and highly power efficient signal conditioning circuit with configurable bandwidth and sub-µHz flicker noise corner frequency for use in integrated voltage-mode sensors and capacitive-mode sensors that require minimal capacitive loading. Three chopping frequencies are used to remove the flicker noise of three amplifiers stages, and nested chopping in used in the first stage to mitigate switching non-idealities. A resistive feedback amplifier and a capacitive feedback amplifier are used to attain low noise low pass filtering with tunable bandwidth. The simulated circuit is designed in a 0.13 µm CMOS technology with 0.4 V and 1.2 V supplies in order to reduce the power consumption. The total power consumption is of 6.7 µW. A gain of 68 dB and bandwidths of 1, 10, 100 and 1000 Hz are achieved. The input-referred noise floor is of 20.5 nV/√Hz, and the integrated input noise is of 205 nV over a 100 Hz bandwidth. The design attains a low power efficiency factor of 4.0. In capacitive mode, the noise floor is of 3.6 zF for a 100 fF sensor capacitance.

Index Terms: high-resolution sensors, high SNR, low flicker noise corner frequency, low noise, ultra-low power, signal conditioning circuits.

5.1 Introduction

The use of high sensitivity and low power consumption sensors has increased significantly during the past few years in applications such as health care, smart homes, smart phones, automobiles, and environmental sensing (X. Wang et al., 2017; Y. Zhao et al., 2015). These sensors require signal conditioning circuits that must be compatible with multi-type inputs and have high sensitivity to be able to distinguish capacitance variations in the femto farad range or voltage variations in the microvolt range at frequencies near DC. For example, the sensitivity of a gas sensor signal conditioning circuit should be on the order of sub-femto Farads in order to be able to detect extremely small levels of gas concentraitons, or the resolution of a pressure sensor signal conditioning circuit for drone control should be as small as a few micro volts in order to be able to sense height changes in the range of a few centimeters (Maruyama et al., 2016). The overall noise of a sensor is often dominated by the front-end amplifier. To suppress this noise below a certain value, it is necessary to consume more power (Shen, Lu, & Sun, 2018). Therefore, the design of a signal conditioning circuit that can attain a good noise and power tradeoff is crucial in energy-constrained applications (Yazicioglu, Kim, Torfs, Kim, & Hoof, 2011).

The chopping technique is an effective method to remove the offset and flicker noise of an amplifier near DC in order to meet low noise requirements (Fan, Huijsing, & Makinwa, 2012b). In the single chopping amplifier, flicker noise and offset are mitigated, but power consumption is high. In a dual chopper amplifier, noise and power consumption can be optimized with a proper distribution of gain between the two stages (Parisa Vejdani et al., 2017). In addition, the first amplifier can be designed while considering the sensor capacitance in order to maximize the sensitivity (Parisa Vejdani et al., 2017). In (Parisa Vejdani et al., 2017), a g_m-C filter is used to remove up-converted harmonics resulting from the dual chopping, but it adds flicker noise at low frequencies which is not suppressed completely by the gain of the previous stages. Moreover, this filter requires relatively large current and capacitance to filter small enough bandwidths with sufficiently low noise. A drawback of the chopper technique is that the non-idealities of the CMOS switches, such as charge injection

and clock feedthrough, contribute to input current noise (J. Xu et al., 2013). This plays an important role when a chopper amplifier is used with high impedance sensors, and it can cause substantial amounts of input-referred voltage noise. Accordingly, this paper presents a multi chopper circuit with nested chopper and dual supply voltages to remove the flicker noise, suppress switch non-idealities to decrease input current noise, and reduce the thermal noise and power consumption. It also minimizes input capacitance.

5.2   Architecture of the proposed circuit

Figure 5.1 shows the schematic of the proposed circuit. The design is consists of three cascaded blocks. Each block is chopped at a different frequency. The first block consists of a sensor that produces a chopped signal at frequency f_h that can also stem from a capacitive bridge (not shown), and is followed by a chopped amplifier. A fully differential NMOS input stage with diode-connected loads implements the first amplifier block. In order to accommodate highly integrated capacitive-mode sensors, small input transistors are used to minimize input capacitance, yielding a high noise corner frequency. As the noise of the first amplifier is the dominant input-referred noise in the circuit, it is important to mitigate it.
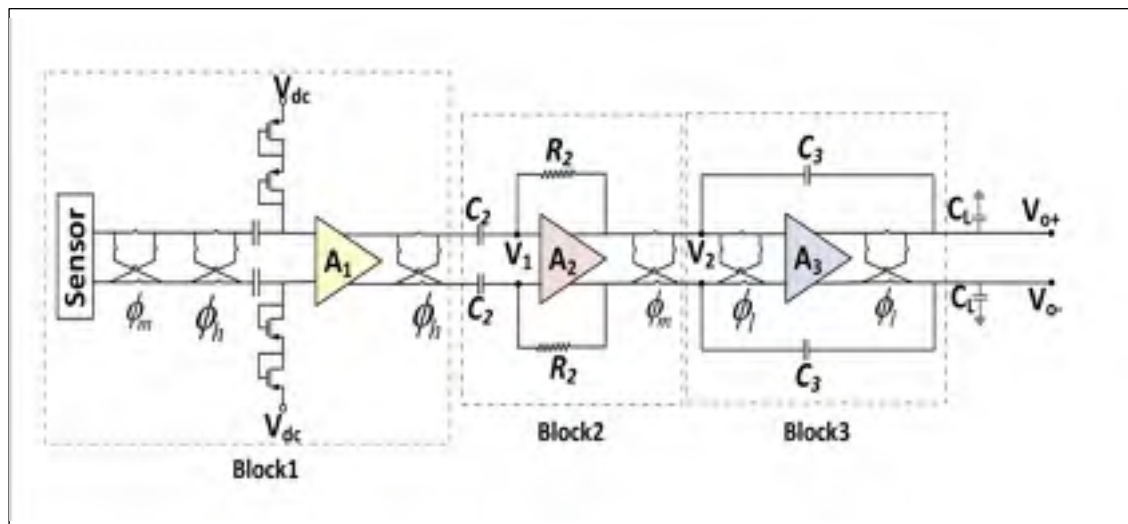
Figure 5.1 Schematic of the proposed circuit

A relatively large bias current of 5.25 μA allows for a lower thermal noise and larger bandwidth. This requires a sufficiently high chopping frequency to mitigate this stage's flicker noise, in this case 1 MHz. To sustain this larger current without significantly increasing the power consumption, the input stage of the first amplifier is biased at a low supply voltage of 0.4 V. Moreover, to reduce the thermal noise of the input transistors, NMOS transistors biased in subthreshold are used to maximize the transconductance to current ratio (H. Wang et al., 2017).

The second block consists of an amplifier with resistive feedback. A folded cascode topology is used, and the input transistors are designed to be bigger and operate in the subthreshold region to decrease the thermal noise floor and increase the transconductance. The chopping frequency at this stage, f_m, is chosen to be of 100 kHz. This block acts as a high pass filter having a low cutoff frequency that is defined by R_2 and C_2. The chopped signal is located at a frequency larger than the cutoff frequency, and is thus amplified. The resulting DC gain of this stage considering the chopping effect is given by:

$$G_2 = C_2 \cdot (2.\pi.f_m) \times R_2 , \tag{5.1}$$

where C_2 is the coupling capacitance, and R_2 is the resistive feedback. The third block consists of a capacitive feedback amplifier. In this block, the amplifier is chopped with a frequency f_l of 20 kHz to mitigate the flicker noise and offset of the third amplifier. The topology of this amplifier is a folded cascode as well. Notably, larger input transistors are used to decrease the flicker corner frequency so that the lower chopping frequency can be used. In addition, an output capacitance C_L of 5 pF mitigates the charge injection of this block. The Miller capacitance, C_{eq}, at node V_2 is given by:

$$C_{eq} = C_3 (1 + A_3) \tag{5.2}$$

where C_3 is the feedback capacitor, and A_3 is the gain of the third amplifier. A capacitor bank implements C_3 in order to allow for a configurable bandwidth. As the bandwidth of the first

amplifier is relatively large, an approximation of the bandwidth of the signal conditioning circuit is given by:

$$BW = \frac{1}{R_2.[C_3(1+A_3)+C_2]} \qquad (5.3)$$

As shown in (5.3), the Miller capacitance allows to reach a smaller bandwidth without the need for implementing a large capacitance that would occupy prohibitively large chip area and have significant parasitic capacitance. Accordingly, the cascade of the second block with the third block results in a low pass filter with a very low cut-off frequency. This cascade avoids the requirement for a g_m-C filter to remove the harmonics. In this fashion, all of the harmonics are filtered with a configurable bandwidth without adding extra flicker noise at low frequencies. Chopping mitigates DC offsets, but it can degrade the performance of the circuit because of the residual ripple that is produced by periodic charge injection and clock feed-through at the chopping frequency that cause transient current with an average value given by (J. Xu et al., 2013):

$$I_{inj,clk} = 2.f_{chop} (WLC_{ox}V_{od} + C_{ol}V_{clk}) \qquad (5.4)$$

where f_{chop} is the chopping frequency, W and L are the width and length of the chopper switches, C_{ox} is the gate oxide capacitance, C_{ol} is the overlap capacitance between the gate and source (drain), V_{od} is the overdrive voltage, and V_{clk} is the clock signal swing amplitude. Among different switch non-idealities, charge injection is the dominant current noise contributor (Yazicioglu et al., 2011). From (5.4), it can be seen that the effect of the charge injection current can be decreased by reducing the size of the switches, and decreasing the chopping frequency. Also, chopping the signal at low impedance nodes results in a smaller charge injection voltage. Therefore, the chopping frequency should be optimized to remove the flicker noise properly and to minimize the charge injection effect. The input transistors of the first amplifier are small to minimize the loading on a capacitive sensor, necessitating a large chopping frequency to compensate for the resulting high flicker noise corner frequency. As a result, a nested chopping

technique is implemented at the input of this amplifier to suppress the charge injection effect, as shown in Fig. 1. Thus, charge injection is reduced by a factor of f_H / f_M, which is set to 10 in this design (J. Xu et al., 2013). The input capacitance of the second stage does not have any effect on the input capacitive loading. As a result, it can be increased to reduce the flicker noise corner frequency, resulting in lower chopping frequency and lower power consumption. The former reduces charge injection. Moreover, because of the Miller capacitance, the impedance at node V_2 is small which results in reduced charge injection due to the chopper switches.

5.3   Simulations results

This circuit was designed in a 0.13 μm CMOS technology from Global Foundries with 1.2 V and 0.4 V supplies. The frequency response of the circuit is shown in Figure 5.2, outlining the gain of 68 dB and four bandwidths settings of 1, 10, 100 and 1000 Hz, determined by the C_3 capacitor bank.
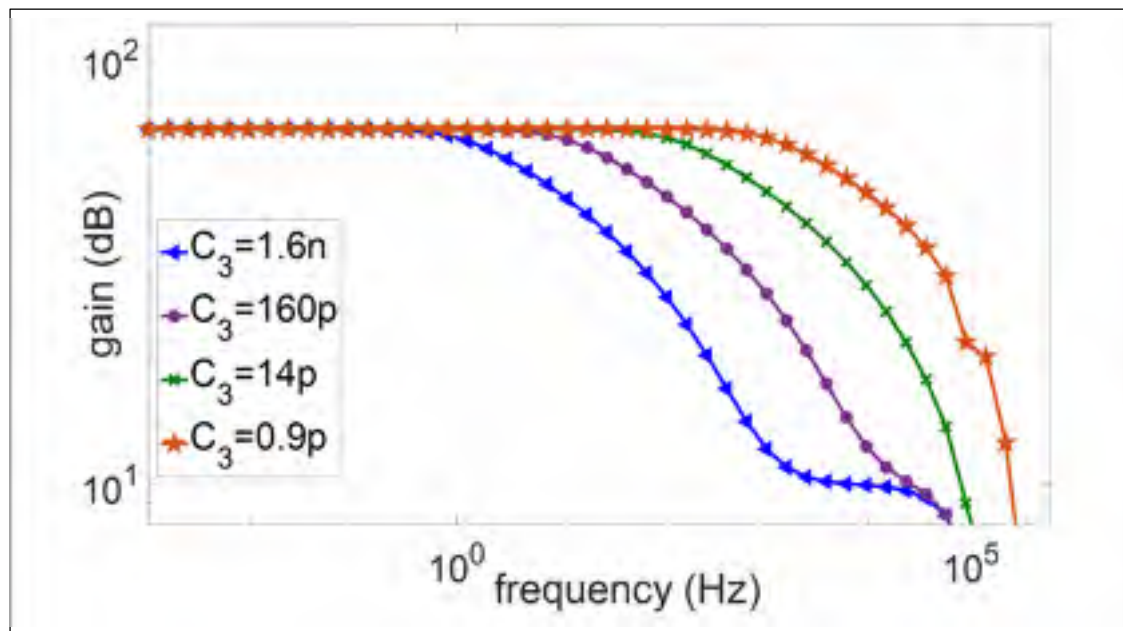
Figure 5.2 Frequency response of the circuit for different capacitor bank (C_3) values.

Figure 5.3 shows the simulation results of the output spectrum for a 150 Hz sine input signal of -81 dBV. The spurious tones are 63 dB below the fundamental output signal. The input-referred noise of the circuit with and without chopping of the third amplifier is shown in Figure 5.4.
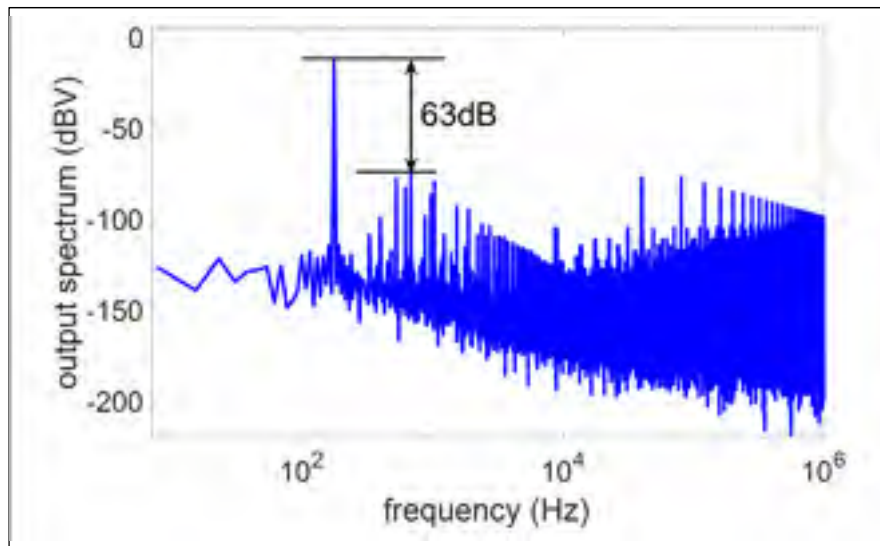
Figure 5.3 Output spectrum for a 150 Hz input signal of -81 dBV
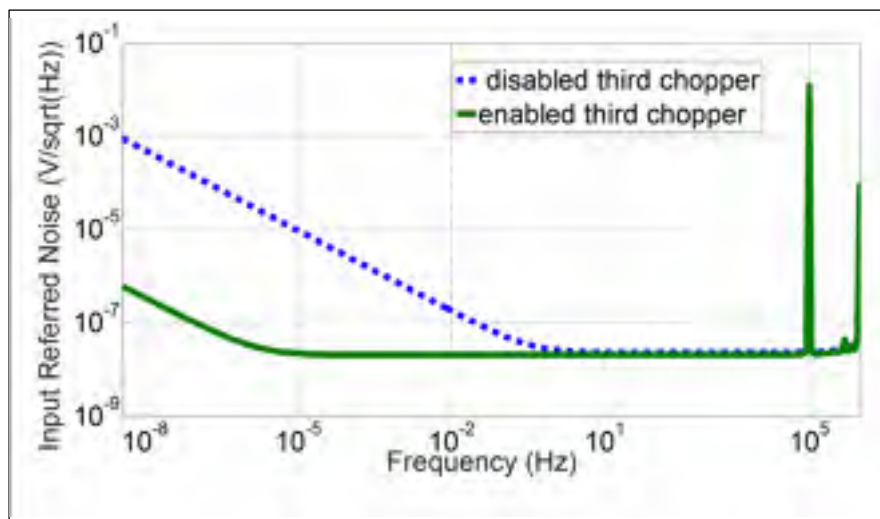
Figure 5.4 Input-referred noise with enabled and disabled third chopper.

The noise floor of this circuit is 20.5 nV/√Hz when the third amplifier is chopped. The contribution of the first stage on the noise floor is 60% and the contribution of the second stage is 40%, while the noise of the third stage is negligible. The corner frequency of circuit without chopping of the third amplifier is of 0.2 Hz, which is much higher than the corner frequency of 0.5 µHz when the third amplifier is chopped. At frequencies lower than 1 Hz, the noise difference with and without the third chopper becomes significant because the flicker noise of the third amplifier is not completely suppressed by the gain of the first and second stages. For instance at 10 mHz, the input-referred noise of the circuit with disabled third chopper is of 2.5 µV/√Hz, and the contribution of the third amplifier flicker noise represents 100% of the noise at this frequency. Accordingly, even by choosing large transistors in the third amplifier to reduce the flicker noise, the flicker noise in the sub-mHz frequency range remains significant, and chopping of the third amplifier is required to mitigate it.

Figure 5.5 shows the flicker noise contribution percentage with respect to the total noise with enabled and disabled third chopper at different frequencies. The dark blue and light blue bars represent the flicker noise contribution percentage of the third amplifier and the other circuit components, respectively, when the third chopper is disabled. The yellow bar presents the flicker noise contribution percentage of the total circuit the when the third chopper is enabled.
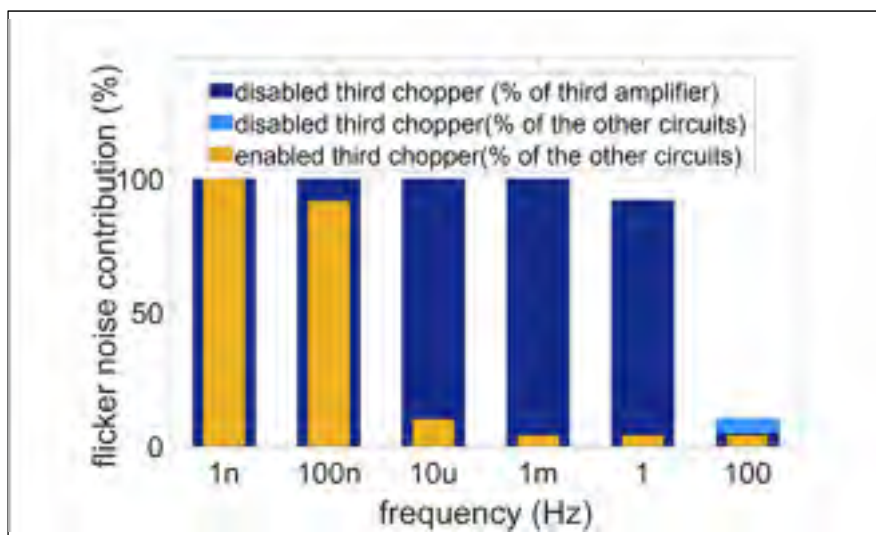
Figure 5.5 Noise contribution of the third amplifier and other
circuits with enabled and disabled third chopper.

The flicker noise of the other circuits dominates when the third chopper is enabled. However, when the third chopper is disabled, the third amplifier flicker noise dominates the total noise at frequencies smaller than 1 Hz.

Table 5.1 shows the integrated input noise, power efficiency factor (PEF) and SNR for the four different bandwidth settings with the enabled and disabled third chopper. The PEF is used to describe the power / noise trade-off and it is given by (Muller et al., 2012b):

$$PEF = V_{rms,in}^2 \cdot \frac{2P_{tot}}{\pi V_T \cdot 4KT \cdot BW} \tag{5.5}$$

where V_T is the thermal voltage, K is Boltzmann's constant, T is the temperature, P_{tot} is the total power drawn by the circuit, BW is its bandwidth, and $V_{rms,in}$ is its input-referred noise. Lower PEF indicates a more efficient design. As shown in this table, the effect of the third amplifier chopping on the integrated input noise, PEF and SNR is significant at low bandwidths.

Table 5.1 Integrated input-referred noise, PEF and SNR for different bandwidths with enabled and disabled third chopper

	Third chopper	Bandwidth (Hz)			
		1	10	100	1000
Integ. input noise (nV)	Enabled	20.5	64.9	205	649
	Disabled	145	162	270	750
PEF	Enabled	4.0	4.0	4.0	4.0
	Disabled	207.3	26.0	7.3	5.3
SNR (dB)	Enabled	135.7	125.7	115.7	105.7
	Disabled	118.8	117.8	113.4	104.5

Table 5.2 lists the circuit performance with enabled and disabled third chopper and compares it with a capacitive sensor in (S. Wang et al., 2016), and a voltage sensor in (Altaf, Zhang, & Yoo, 2015).

Table 5.2 Simulated circuit performance overview and comparison.

	This work[*]	(Muller, Gambini, & Rabaey, 2012a)	(S. Wang et al., 2016)	(Maruyama et al., 2016)	(Altaf et al., 2015)	(H. Wang et al., 2017)
Supply (V)	0.4, 1.2	-	1.8	1.55	1.8	2.7-3.6
Technology (nm)	130	350	180	180	180	180
Gain (dB)	68	29.6	40	-	-	0-42
Power cons. (µW)	2.1 @ 0.4 V 4.6 @ 1.2 V	165	1.62	2015	2160	270
Noise Floor (nV/$\sqrt{Hz}$)	20.5 23	-		8.2	3.7	19
Integ. Input Noise (nV)	205[**] 270[**]	-	900[***]	171[++]	-	-
Noise corner (Hz)	0.5µ 0.2	100	0.5	-	-	-
Cap. noise floor (zF)	3.6[+] 4.7[+]	19.8	-	-	-	-
PEF	4	-	19.5	201.4	44.1	-

[*]First row enabled 3rd chopper, second row disabled 3rd chopper.
[**]Over a 1 nHz-100 Hz bandwidth.
[***]Over a 0.5 Hz-100 Hz bandwidth.
[+]Assuming a 100 fF sensor capacitance.
[++]Over a 0.1 Hz-10 Hz bandwidth.

A low power consumption of 6.7 µW is achieved here, and the noise performance compares favorably. A PEF of 4.0 in this circuit in comparison to the higher PEF of the other references outlines the ability of the architecture to support power efficient operation while attaining low noise performance. In addition, the noise corner frequency of 0.5 µHz is very low, allowing for near-DC high sensitivity operation such that microvolt signals can be detected. For capacitive sensors, the10 fF input capacitance and low noise floor result in a capacitance noise floor of 3.6 zF, in comparison to 19.8 zF in (S. Wang et al., 2016).

5.4   Conclusion

A low noise and low power triple chopper signal conditioning circuit was proposed for capacitive-mode and voltage-mode high efficiency sensors. The input capacitance of the circuit is minimized to be suitable for high sensitivity fully-integrated capacitive sensors. Two supply voltages are used to reduce the power consumption while minimizing the noise floor. A nested chopper technique is used at the input of the circuit to minimize the input current noise due to charge injection. The configurable bandwidth can decrease the integrated input noise and improve SNR for given applications. The third stage chopping enables a very low corner frequency for high sensitivity measurements at DC.

Acknowledgment

CHAPITRE 6

DISCUSSION OF THE RESULTS

The purpose of this work was designing a signal conditioning circuit for MEMS sensors which meets the following criteria:

- Enabling agile functionality: a signal conditioning integrated circuit with variable performance, supporting different input sensor types.
- Minimizing the power consumption for portability.
- Maximizing the sensitivity to be able to detect low-frequency signals in the micro-volt range in resistive sensors and in the atto-Farad range in capacitive sensors.

To reach the mentioned criteria, the following steps were carried-out:

- A design methodology: since the sensing conditions define the required specifications for the signal conditioning circuit, a methodology is necessary to choose the best architecture and design the circuit to have the best possible performance.
- System level analysis of the chosen signal conditioning circuit architecture to improve the performance.
- A circuit level implementation of the signal conditioning circuit: this includes choosing the proper architecture for the amplifiers, while considering the power consumption, and dimension and operation region of the transistors.
- Fabrication and testing the signal conditioning circuit to validate the design, and find and solve the problems that could be faced in practice.

Based on the required specifications, different architectures are compared. Because of the low frequency of the detected signal, the chopping technique was chosen to remove the flicker noise and making it possible to sense the small signals. Chopping can be done with single chopping frequency or more chopping frequencies. Each of these chopping techniques has its advantages and disadvantages.

To reach the optimized performance, three different chopping techniques of SCA, TCA, and DCA are considered, and the sensitivity and power consumption for each of them is extracted. A sensitivity factor is defined and the lower sensitivity factor means the higher sensitivity in the circuit. It is shown that the input noise and the ratio of input capacitance to the sensing capacitance are important in the sensitivity factor. Then, the sensitivity factor and the power consumption of the three chopping techniques are extracted for the different total gains and sensor capacitances. It is shown that the sensitivity factor in the SCA is increased in correspondence with increasing the gain, and it is worst for the smaller sensor capacitance because of the larger ratio of input capacitance to sensor capacitance.

Also, the minimum sensitivity factor of the TCA based on total gains and sensor capacitances is extracted. In this architecture, the distribution of the gain between the two stages is important and it will change the sensitivity and power consumption significantly. It is shown that for the smaller total gain and sensor capacitance, all of the amplification is done at the first stage. As the total gain is increased, the ratio of the gain of first amplifier to the total gain starts to decrease based on the value of the sensor capacitance, and this is justified by the loading factor. It is shown that at the smaller sensor capacitance, most of the amplification is done at the second stage. However, because of the limitation in the design of a TCA, input capacitance could not be decreased enough at the small sensor capacitance and high gain. This limitation contributes to an increased sensitivity factor and a reduced performance.

From the analysis of sensitivity factor in the DCA, it is concluded that there is an extra degree of freedom in the DCA. The gains of the two stages and their chopping frequencies could be chosen in a way that makes a small input capacitance and also a small input noise floor which result in a smaller sensitivity factor. As a result, with increasing the total gain and a small sensing capacitance, most of the amplification can be done at the second stage and the first amplifier can be implemented as a capacitance buffer.

To be able to choose a proper chopping technique, a figure was presented in Figure 3.13 in chapter 3. The preferred chopping technique was based on the total gain, and sensor

capacitance can be chosen from this figure. As shown, for a small gain and a large sensor capacitance, the SCA can be suitable. The DCA is the most suitable for a small sensor capacitance and large required gains. For a moderate gain and large sensor capacitance, the TCA is preferred. Moreover, the lowest power consumption is obtained by using the TCA with the same gain for the first and second amplifiers, if that architecture is well suited to the required sensitivity. Moreover, the flow graph in figure 3.14 was proposed. In this flow graph, the steps to design an optimized chopping techniques were shown. Based on the total gain and sensing capacitances, the chopping technique will be chosen. Then, based on this flow graph, the circuit will be designed to have the minimum sensitivity factor or desired sensitivity factor with the minimum power consumption.

To improve DCA performance and to reach more sensitivity and less power consumption, a novel dual-chopper amplifier was designed and fabricated in the 0.13 μm CMOS technology. The circuit occupies an active area of 550×250 μm. This structure provides two gain settings, and it can be implemented in both capacitive and resistive modes. In this circuit, two supply voltages are utilized. A low supply voltage, high current amplifier is implemented in the first stage, which improves the power consumption and the noise floor. The input transistors of this amplifier have small dimensions, and they are set in the subthreshold region. This helps to minimize the input capacitance and maximize the g_m/I_D ratio, which means the higher gain with utilizing less power consumption. The input capacitance is 10 fF for this circuit. The corner frequency in this amplifier is high and a chopping frequency of 1 MHz is implemented to remove the flicker noise. The second stage of this design is composed of two parallel paths. The folded cascade amplifier is implemented at the second stage, and they are chopped with the frequency of 100 kHz. The second path in the dual-path can be enabled and disabled with a controllable switch mixer that gives us the possibility of two gain settings.
 The dual-path improved SNR in two faces. Firstly, because of the fact that signals are added in voltage and noise is added in power. Secondly, SNR is improved because of the correlation noise at the second path. The current noise in two paths is subtracted in the adder that results in a smaller integrated noise. The charge injection of the first chopper is mitigated with the

nested chopper technique, and the g_m-C filter attenuates the out of band harmonics and the charge injection of the second chopper.

The measurement results show a power consumption of 2.66 µW for the supply voltage of 0.7V and 3.26 µW for the supply voltage of 1.2V. The single-path DCA has the gain of 34dB with bandwidth of 4kHz and an input noise floor of 25 nV/√Hz. The dual-path DCA has the gain of 38dB with bandwidth of 3kHz and an input noise floor of 40 nV/√Hz. Comparing these results with the other similar works shows that the power consumption is reduced significantly, which is yielded because of the proper design of the DCA. Moreover, the input capacitance is considered in the design of the DCA, but it is not included in the design of other works.

At last, to be able to detect the ultra-small variations in a very low frequency range of sensor, a novel signal conditioning circuit is proposed. This design consists of three cascaded blocks and each block is chopped at a different frequency. Utilizing three chopping frequencies to chop three stages helps to remove the flicker noise completely. The implemented chopping frequencies are 1 MHz, 100 kHz and 20 kHz, which are defined by the corner frequencies of amplifiers. The input signal is chopped with a 100 kHz and then 1 MHz to suppress the charge injection effect of the higher chopping frequency at the input. The first amplifier is a NMOS-input fully differential amplifier, which is biased with a higher current and lower supply voltage to reduce the power consumption and input noise floor. The second stage is composed of a resistive feedback amplifier and the third stage is an amplifier with Miller capacitance feedback. A combination of the second and the third stages composes a low-pass filter with configurable bandwidth. The miller effect helps to reach the small bandwidth without increasing the capacitance, which is beneficial in two faces. First, it prevents the extra parasitic capacitance, and second, ultra-small bandwidth is possible that leads to a lower integrated input noise and a higher SNR. A folded cascade amplifier with NMOS input is implemented at the second and the third stages.

The simulated circuit is designed in a 0.13 µm CMOS technology with 0.4 V and 1.2 V supplies to reduce the power consumption. The total power consumption of 6.7 µW and gain

of 68 dB is achieved. Based on the value of miller capacitance, bandwidths of 1, 10, 100 and 1000 Hz are achieved. The noise performance of this circuit was extracted for both a disabled and an enabled third chopper. With enabling the third chopper, the input referred noise floor is 20.5 nV/√Hz. The input referred noise floor with a disabled third chopper is 23nV/√Hz. The simulation results show a significant difference in the corner frequency between an enabled and a disabled third chopper. With a disabled third chopper, the corner frequency is 0.2 Hz while in an enabled chopper it becomes to 0.5 µHz. This small value of corner frequency helps to detect ultra-small signals at DC.

Table 5.1, which was presented in chapter 5, shows the integrated input noise, PEF and SNR of the proposed circuit with an enabled and a disabled third chopper for four bandwidths of 1, 10, 100, and 1000 Hz. Comparing the results reveals that the effect of chopping throughout the amplifier chain has significant impact. For example, for the 1 Hz bandwidth, the integrated input noise of the circuit with an enabled third chopper is 7 times smaller than the one of the circuit with a disabled third chopper. Also, PEF in the chopped circuit is 6 times smaller than the disabled chopper for the 10 Hz bandwidth. As a result, for the small bandwidth circuit, it is very important to chop all stages, and it will contribute to a big difference in the noise results. The design with three chopper frequencies attains a low power efficiency factor of 4.0, which presents the great optimization of noise and power consumption at the same time. In the capacitive mode, the noise floor is of 3.6 zF for a 100 fF capacitance sensor, which makes possible to sense the capacitance variation in the zepto farad range.

CONCLUSION

MEMS-based sensors are experiencing large growth in various applications such as communications, medical, industry and consumer electronics. Because of their applications, developing high-performance signal conditioning circuit is essential to detect the physical stimulus more precisely. Based on the application, the requirement of signal conditioning circuit varies. In portable devices, power consumption is a critical feature and some applications need more sensitivity rather than the others. The goal of this research was to design a high-resolution, low-power signal conditioning circuit for MEMS, which is applicable in both capacitive and resistive sensors. With this goal, this project was started by investigating different circuit architectures to find the most effective way to design a signal conditioning circuit with these features. Among them, a chopping technique was preferred because of the ability to remove the flicker noise and reach low-noise floor in low frequencies. Then, three different chopping techniques were considered and their sensitivity and power consumption were analysed based on the total gain and different sensor capacitances. The characteristics of each chopping technique can be summarized as below:

- SCA: simpler structure, higher power consumption, fixed sensitivity, and the worst sensitivity in the small sensor capacitance, and large gain;
- TCA: flexible sensitivity and power consumption based on the distribution of gain, capability of having the minimum power consumption;
- DCA: capability of having the maximum sensitivity in small sensor capacitance, flexible in power and sensitivity, complexity in the design.

It was shown that the distribution of gain between the two stages in the DCA and TCA has a significant effect on the sensitivity. Based on this distribution, the sensitivity factor and the power consumption vary significantly. For a large gain and a small sensor capacitance, the DCA has a degree of freedom to decrease the input capacitance of the first amplifier and contributing to a smaller sensitivity factor. For a small gain and a large sensor capacitance, the SCA can be suitable. Moreover, it was shown that the lowest power consumption is obtained by using the TCA with the same gain for the first and the second amplifiers if that architecture

is well suited to the required sensitivity. Based on these analyses, an ultra-low power dual-chopper circuit was designed and fabricated in the 0.13 μm CMOS technology.

Moreover, to improve the performance of the dual-chopper amplifier and reduce the power consumption, a novel architecture was proposed and fabricated in the 0.13 μm CMOS technology. The first stage of the dual-chopper amplifier in this design is a low supply voltage, and a high current amplifier to improve the noise floor and power consumption at the same time. Small input transistors were implemented at this amplifier to decrease the parasitic capacitance and improve the sensitivity. At the second stage, two parallel paths were utilized to provide improved SNR and gain configurability, and they were added by a two-differential input g_m-C low-pass filter. The flicker noises of the both stages were removed with the chopping technique, and the up-converted flicker noise was filtered by a g_m-C filter. Although this filter suppresses the up-converted flicker noise of the first and second stages, it added some flicker noise in sub-Hz frequency.

To remove the flicker noise completely and to improve the SNR, the triple-chopping technique was proposed. In this circuit, the first stage is a low supply voltage high current amplifier the same as the previous design which is chopped with a high frequency. However, at the second and third stages, a resistive feedback amplifier and a capacitive feedback amplifier is used respectively to attain a low-noise, low-pass filtering with a tunable bandwidth. All of these stages were chopped to remove the flicker noise completely, which contributes to a sub-μHz corner frequency. The bandwidth of this circuit was configurable and could be as narrow as 1 Hz which contributes to an ultra-small integrated input noise and improved SNR. A nested chopper technique is used at the input of this circuit to minimize the input current noise to charge injection. As a result, an ultra-high sensitivity and an ultra-high power consumption are achievable with this circuit that can detect small signals in the capacitive and resistive sensors in the DC frequency.

To sum up, the first step to design a signal conditioning circuit is to identify the required specifications, such as the values of the capacitive or resistive sensors, desirable resolution,

required total gain, and frequency range of the input signal. After that, the type of chopping could be defined. The SCA is utilized when a lower resolution is needed. The TCA can be implemented to decrease the power consumption, while the highest sensitivity can be achievable with the DCA. Distribution of the gain between the two stages in the TCA and DCA contributes to different power consumptions and sensitivities. In addition, a triple-chopping technique could be implemented to remove the flicker noise at sub-Hz frequency. The desig of the amplifier is important in the chopping technique. To reach the ultra-low-noise amplifier with low-power consumption, a high-current low-supply voltage amplifier could be implemented at the first stage. This has the most contribution at the input noise floor. To improve performance of the chopping amplifier, this technique can be combined with the other techniques. For example, a multi-path can be applied to reach a configurable gain and improvement in SNR. A configurable and narrow bandwidth can be reached with implementation of the resistive and capacitive feedback amplifiers. For the applications near the DC frequency range, the flicker noise should be suppressed completely. Accordingly, all stages should be chopped properly to remove the flicker noise maximally.

The main contributions of this thesis are:

1) A methodology was proposed to design an optimized signal conditioning circuit with chopping technique based on the sensor capacitance and the required total gain. This structure is beneficial because the circuit could be designed to reach the maximum possible sensitivity, or reach the desired sensitivity with minimum power consumption.

2) A dual-path dual-chopper amplifier was designed and fabricated. In this circuit, low-noise and ultra-low-power circuit was achieved. Power efficiency factor (PEF) of this circuit is 11 for a single-path circuit and 13 for a dual-path circuit, which indicates a good trade-off of noise and power consumption. The power consumption of this circuit is 2.66 μW from the 0.7 V supply voltage and 3.26 μW from the 1.2 V supply voltage that make this signal conditioning circuit a proper choice for portable devices.

3) A low-power low-noise signal conditioning circuit with sub-μHz noise corner frequency and tunable bandwidth was designed. Simulation results show that with this circuit, a corner frequency of 0.5 μHz and noise floor of 20.5 nV/$\sqrt{}$Hz are achievable. This structure

helps to measure near DC signals. In addition, the bandwidth is tunable, and it can be set based on the application. A bandwidth as small as 1 Hz is achievable in this circuit, which helps to reduce the integrated input noise and to improve the SNR. A power efficiency factor of 4 and SNR of 115.7 dB for the bandwidth of 100 Hz is achievable with this circuit.

List of published journal and conference papers:

- P. Vejdani and F. Nabki, "Dual-Path and Dual-Chopper Amplifier Signal Conditioning Circuit With Improved SNR and Ultra-Low Power Consumption for MEMS," *IEEE Transactions on Circuits and Systems I: Regular Papers,* pp. 1-10, 2019.

This paper presents the measurement result of a novel DCA that has two supply voltages in addition to using dual-path at the second stage. This architecture helps to decrease the noise and input capacitance that results in higher sensitivity in capacitive sensing. Moreover, the power consumption is low, which makes it proper for portable applications.

- P. Vejdani, K. Allidina, and F. Nabki, "Analysis of Sensitivity and Power Consumption of Chopping Techniques for Integrated Capacitive Sensor Interface Circuits," *Journal of Low Power Electronics and Applications,* vol. 7, 2017.

A complete analysis of power consumption and sensitivity is shown in this paper for different chopping techniques. With the proposed methodology, the suitable chopping amplifier could be designed to optimize both the sensitivity and the power consumption in the capacitive sensing.

- P. Vejdani, A. Bouchami, and F. Nabki, "Signal Conditioning Circuit with Ultra-high Sensitivity and Ultra-low Power Consumption for MEMS," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017, pp. 930-933.

This paper presents the simulation result of a dual-path dual-chopper signal conditioning circuit.

- P. Vejdani and F. Nabki, "A Low-noise, Low-power Signal Conditioning Circuit with Narrow Bandwidth," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017, pp. 1461-1464.

The circuit presented in this paper has three cascaded stages. A high-current and low-supply voltage amplifier as the first stage, and a differentiator and an integrator at the second and third

stages are used to reach the amplification with a narrow bandwidth. Moreover, the first and the second stages are chopped with two different frequencies to remove their flicker noise. A high sensitivity with high SNR circuit is achievable with this design.

- P. Vejdani, K. Allidina, and F. Nabki, "Ultra-high Sensitivity, Low-power Dual Chopper Signal Conditioning Circuit for Integrated Sensors," in *2016 14th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2016, pp. 1-4.

A low power high sensitivity DCA is presented in this paper. This DCA is optimized based on the distribution of gain between the two stages to minimize the input noise and input capacitance that results in high sensitivity circuit. This circuit can be used in both capacitive and resistive sensors.

- P. Vejdani, A. Bouchami, and F. Nabki, "Design Constraints of High Performance Chopping Signal Conditioning Circuits for Integrated Sensors," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2014, pp. 690-693.

This paper presents the design constrains for the chopping techniques of SCA, TCA, and DCA. Also the optimization based on noise, power consumption, and noise-power factor is presented. This analysis could be implemented to design a signal conditioning circuit in resistive sensing.

List of submitted manuscripts:

- P. Vejdani and F. Nabki, "Highly Power Efficient Low-Noise signal Conditioning Circuit with Sub-µHz Noise Corner Frequency and Tunable Bandwidth", submitted in Sensor Letters (Feb. 2019)

The proposed circuit in this paper composed of three stages, and all of them are chopped. This helps to have a very low corner frequency. Moreover, resistive and capacitive feedback amplifiers are used in the second and third stages, respectively. A capacitive bank in a capacitive amplifier helps to have a configurable bandwidth.

RECOMMANDATIONS

MEMS designers and researchers are increasingly encouraged to focus on improving the performance of the MEMS sensors to make the most information out of a physical signal. As a result, the design of the signal conditioning circuit, transducer, and their proper integration is important to achieve a high performance sensor.

In this design, a high performance signal conditioning circuit is designed. However, it is important to consider the performance of this circuit in the integration with a capacitive or resistive sensor. In the design, a capacitive emulator could be considered and added to the input of the circuit to see the sensitivity result. Moreover, this circuit could be fabricated with a MEMS sensor in a package. The integration could be done with a pressure sensor that is a resistive sensor or accelerometer, which is a capacitive sensor. For example, integration of this circuit with pressure sensor in (Arunachalam, Gupta, Izquierdo, & Nabki, 2018) could be carried out. The input capacitance of the signal conditioning circuit is not important in the integration with resistive sensors. Moreover, because of the small value of the impedance in this pressure sensor, the noise that is produced in chopping modulation and converted to voltage noise in the sensor, does not have an important effect on the performance. However, for the large sensing impedances, this could be important.

The integration of this circuit with capacitive sensor, such as (Alfaifi, Alhomoudi, Nabki, & El-Gamal, 2019), could be challenging. To integrate with this sensor which has the nominal capacitance of 500 fF, the input capacitance of the signal condition circuit should be smaller than 10 fF to prevent more than 5% degradation in the performance.

In addition to integration with sensors, there are some points that could be considered in the design of a signal conditioning circuit, which are explained in the following:

1) improvement in the system level:

In this work, a complete methodology design of a low-noise low-power circuit with different chopping techniques has been discussed. The sensitivities and power consumptions of the

SCA, TCA, and DCA for different total gain and sensor capacitances were analysed. In future works, the effect of switch non-idealities such as charge injection, clock feedthrough, and residual offset can be considered in the SCA, TCA, and DCA. Their effects on the performance of the circuit in different gains and different sensors can be extracted and the circuit with the minimum non-idealities can be extracted based on the distribution of gain between the two stages in the DCA and TCA. Then based on these results, the circuit can be optimized for noise, power consumption, and non-idealities of the switches at the same time.

In our design, chopping is implemented to remove the flicker noise. However, chopping could contribute to the input current noise and the value of the current noise is dependent on the chopping frequency and switch dimensions. As a result, if a highly-resistive sensor is implemented, the input current noise can degrade the sensing performance. In future works, the effect of input current noise of the circuit can be considered in the design, and the circuit can be optimized based on both the input voltage noise and the input current noise.

2) improvement in the circuit level:

In our design of the DCA, a g_m-C filter is utilised to mitigate the upconverted harmonics. However, this filter mitigated the harmonics partly. A higher order low-pass filter can be implemented instead of this filter to suppress the out of band harmonics completely which results in a better performance. In addition, in the case that switch non-idealities are destructive, extra circuits can be added to the signal conditioning circuit to mitigate the effect of the residual offset. Besides, a structure could be implemented to minimize the PVT variations.

3) improvement at the layout level:

Improving the layout of the signal conditioning circuit can be considered in future works to reach more matching and decreasing the non-idealities. For example, mismatches in the transistors of the amplifiers result in nonlinearity and offset, and mismatches in the transistors of the switches results in charge injection and clock feedthrough. As a result, a better layout results in a better performance and a higher sensitivity to make the circuit more reliable.

The design of a signal conditioning circuit becomes more challenging in modern CMOS technology nodes. In the smaller CMOS technology, flicker noise becomes larger. As a result, with utilizing the smaller technology, the effect of flicker noise becomes more challenging. As shown, a chopping technique is the best way to remove the flicker noise, and this structure is recommended to remove the flicker noise. However, in the smaller technology, the corner frequency become larger, which necessitates a larger chopping frequency or a larger dimension for the transistors. On the other hand, decreasing the size of the sensors, leads to a nominal sensor capacitance that is smaller. So, the need to have a smaller input capacitance becomes more essential. This means to remove the flicker noise completely, a large chopping frequency should be implemented. Since the charge injection of the switches has a direct relationship with chopping frequency, the charge injection will be increased that causes a higher current noise. As a result, in the next generation, the values of input capacitance, flicker noise, current noise, and power are the most important factors that should be considered. In our work, we showed the techniques to remove the flicker noise, decrease the input capacitance, and minimize the power consumption.

To reduce the current noise, it is important that the performance of the switches be improved. The following actions could be considered to reduce the current noise:

1) Studying the clocks: considering their shape, duration, and overlaps and proposing the best clock structure to reduce the charge injection as much as possible;

2) Improvement in the switch design and proposing a novel switch structure to minimize the charge injection;

3) Studying a structure at the system level of the signal conditioning circuit to remove the produced charge injection effect.

Moreover, to have a reliable circuit, it is important that a circuit is designed that has stability in PVT variation.

The following topology is proposed for the next generation of the signal conditioning circuits. As shown, it is composed of two main stages, and each stage is chopped separately.
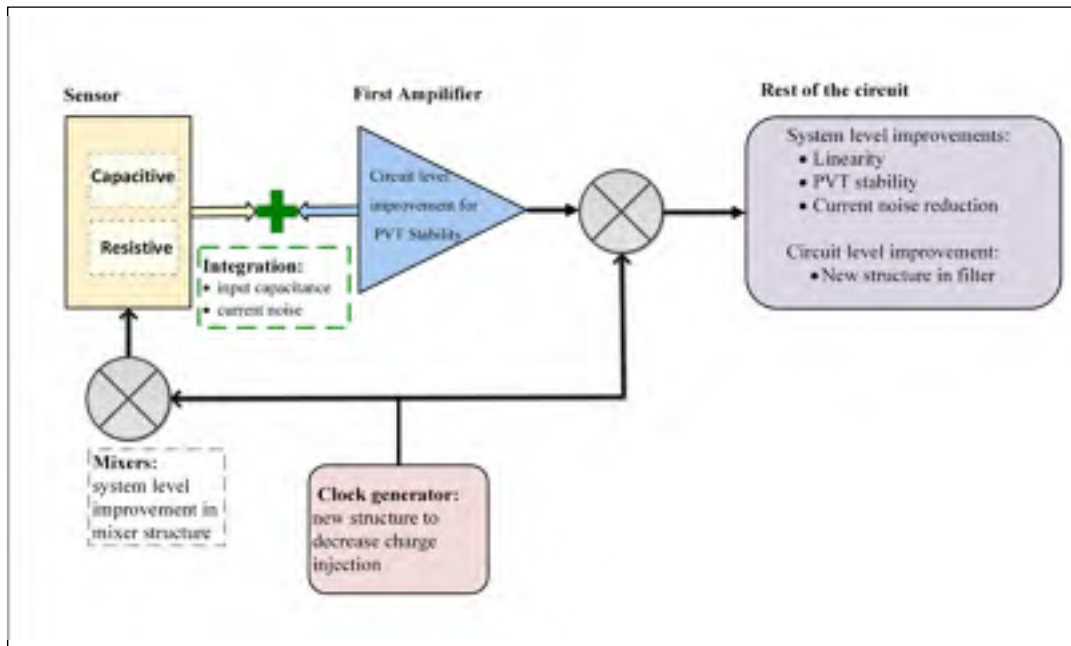
Figure 8.1 Proposed topology for the next generation of signal conditioning circuit

It is suggested that:

1) The first amplifier is improved and optimized in the circuit level to be stable in the PVT variation;

2) A new architecture is proposed in the system level of the second stage to minimize the PVT variation and reduce the current noise;

3) A new methodology is implemented in the mixers to reduce the charge injection effect.

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