Controlled fabrication and electrical properties of long quasi-one-dimensional superconducting nanowire arrays

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Supporting Information

Description of the fabrication processes:

Si substrates with a 300 nm thick SiO_2 or Si_3N_4 top layer are cleaned in piranha solution (H_2SO_4/H_2O_2) and rinsed thoroughly with deionized water. SiO_2, Si_3N_4 and Si substrates are all found to be compatible with the fabrication procedure, and consistent results are observed on SiO_2 and Si_3N_4 substrates (Si substrates are not tested due to the large current through the Si channel). Fully functional thin Pt/Ti (5 nm/2 nm) contact electrodes with thick Au/Ti (50 nm/10 nm) wire-bonding pads are fabricated on some of the substrates by electron-beam lithography (EBL).

The superconducting Nb films are prepared in a Denton Vacuum Discovery 550 multi-cathode DC/RF magnetron sputter deposition system. Substrates are loaded onto a rotating stage and the chamber is pumped down overnight to achieve a base pressure of 10^{-7} Torr (1 Torr ~ 133 Pa). Pure argon (99.999%+) is introduced into the system as the sputtering gas at 15 sccm (standard cubic centimeters per minute) and kept at 2.5 mTorr. Nb films are deposited at ~0.8 nm/s by DC sputtering

from a 3-inch Nb target (99.96%, Plasmaterials, Livermore, CA), after an extensive (>30 minutes) pre-sputtering with a shield between the substrates and the target to clean the surface of the target thoroughly and getter-absorb the residual background gases in the chamber. Without breaking the vacuum, 4 nm SiO_2 is immediately RF sputtered from a 3-inch silicon dioxide target (99.995%, Kurt J. Lesker, Livermore, CA) to cover the films.

Pt SNAP NW arrays are fabricated on top of the SiO_2-covered Nb films (Fig. S1A), with the width and periodicity of the NWs precisely controlled through the MBE growth of the starting GaAs/$Al_xGa_{1-x}As$ superlattice wafers (IQE, Cardiff, UK).(Melosh *et al.* 2003) For substrates with pre-defined contact electrodes, Pt NW arrays are aligned perpendicular to and across the underlying electrodes with ~1 μm registration.(Green *et al.* 2007) For substrates without pre-defined contact electrodes, Pt NW arrays are put down in the center of the substrate, and EBL is used to pattern a 40 nm thick Al_2O_3 mask for the contact electrodes (Fig. S1B). The Pt NW array and Al_2O_3 electrode masks are translated into the underlying Nb film by highly directional reactive-ion etching (RIE) in a 40 MHz Unaxis SLR parallel-plate RIE system with CF_4/He (20/30 sccm, 5 mTorr, 40 W). Devices are ready for measurement after the pattern translation: for substrates with predefined electrodes, the Nb NWs are contacted by the Pt electrodes beneath, while for substrates without predefined electrodes, the Nb NWs are seamlessly connected to the contacts made out of the *same* superconducting film, forming monolithic Nb NW array circuits defined by the Pt NW and Al_2O_3 contact electrode masks (Fig. S1C and S1D). With this careful design, the obtained Nb NWs are well insulated from the Pt NW masks above by the SiO_2 and epoxy layers (Fig. S1C), and the whole structure is covered and protected by the SiO_2 layer on the top and the very thin fluorocarbon polymer films coated on the sidewalls during the dry etching step.(Kay *et al.* 1980) Measurements are done in a pumped ^{4}He system (Quantum Design MPMS-XL; base temperature ~1.7 K) with standard DC or AC lock-in techniques at low frequency.

Supplementary Figures S1-S4:

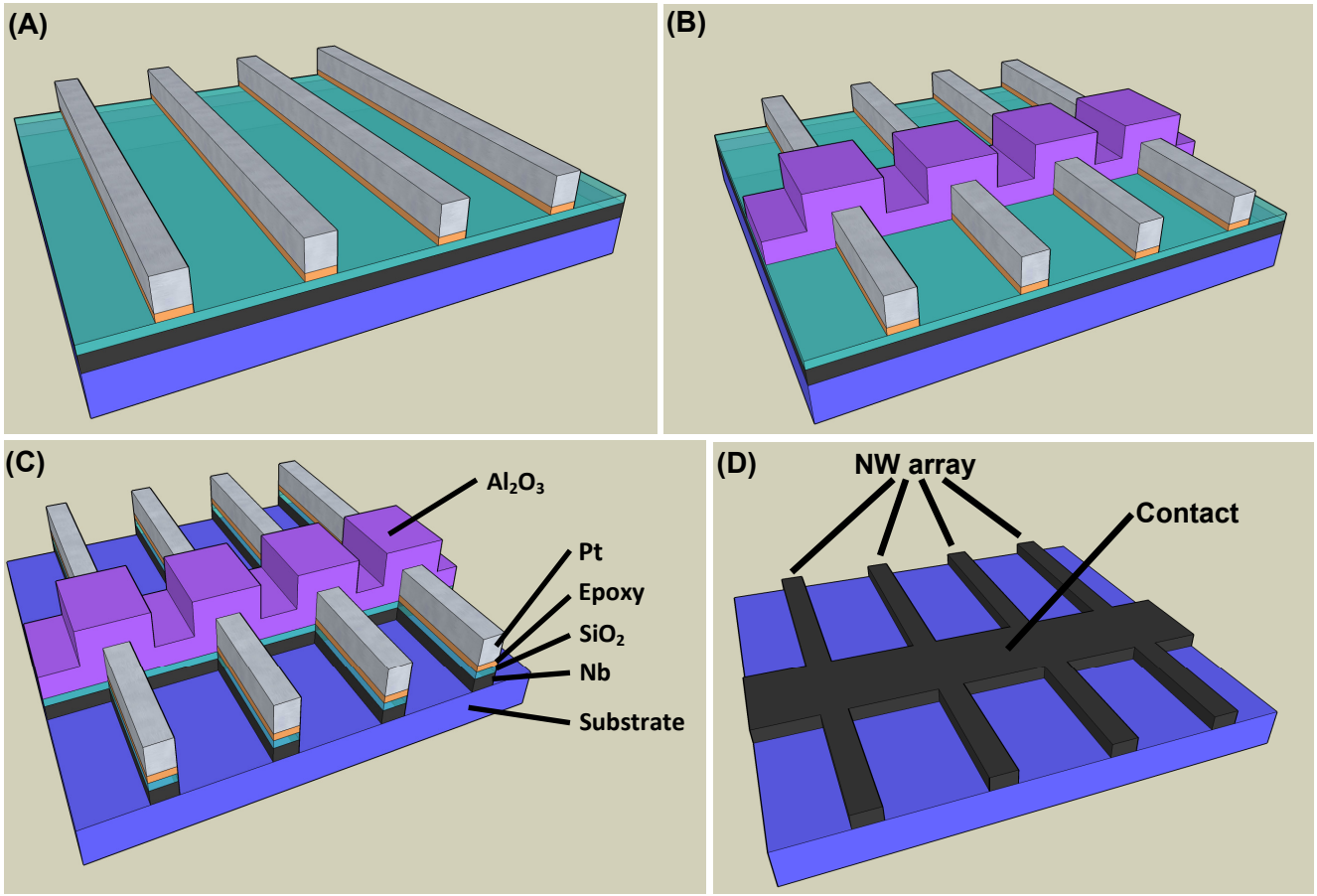

Figure S1. Process flow for the fabrication of superconducting NW array circuits. (A) An array of Pt SNAP NWs is placed onto a SiO_2-covered superconducting Nb film. (B) Al_2O_3 is deposited as a pattern for the contact electrodes. (C) A monolithic (all Nb) NW array circuit is obtained after the pattern is translated with a directional dry etch. (D) The resultant NW array circuit is drawn here. In practice, it is protected by the SiO_2 cover layer.

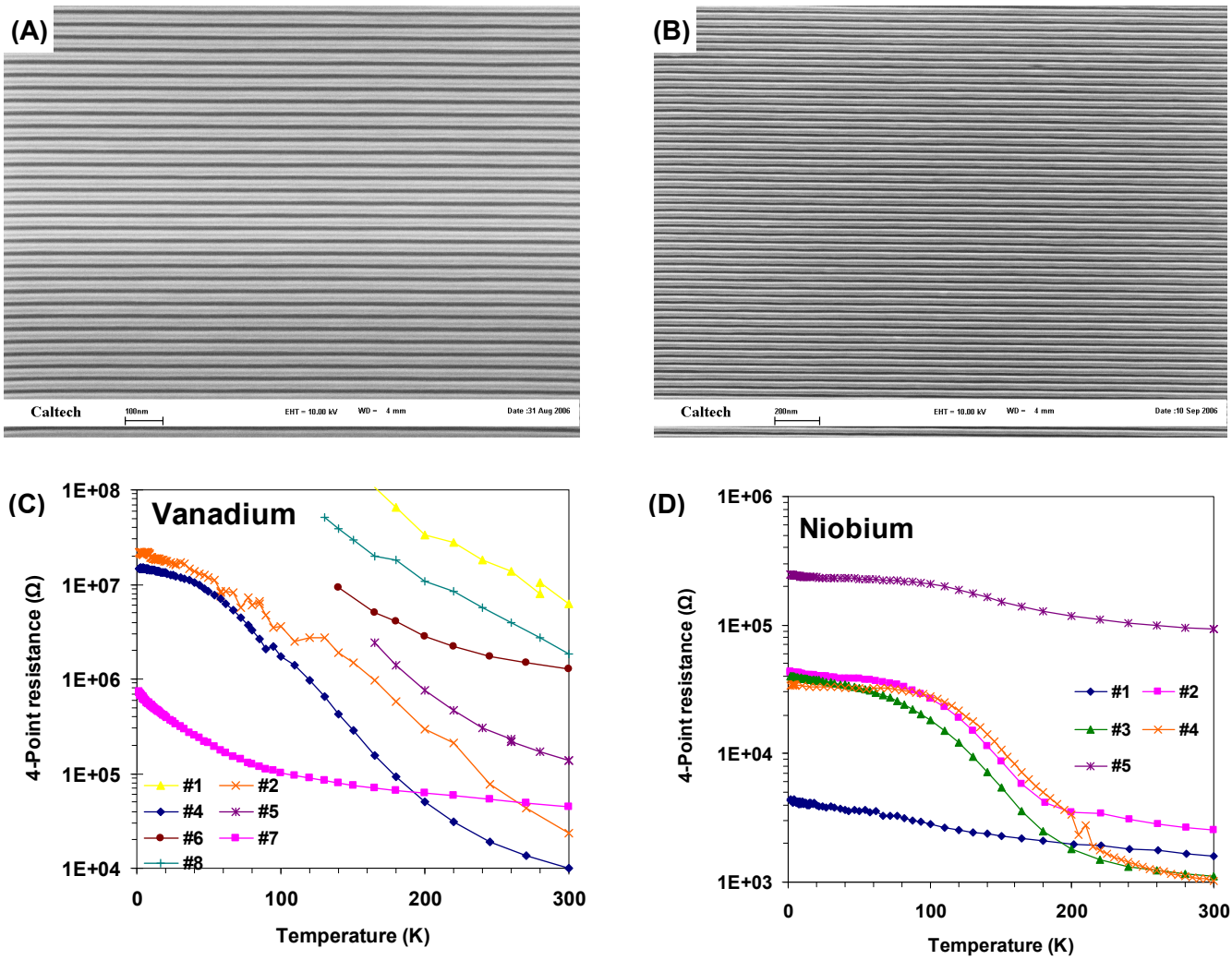

Figure S2. Results on vanadium and niobium NW arrays fabricated by direct application of the SNAP process, using the corresponding metals to replace Pt for the directional e-beam evaporation step. (A) Scanning electron microscope (SEM) image of an array of 20 nm wide vanadium NWs. Scale bar: 100 nm. (B) SEM image of an array of 20 nm wide niobium NWs. Scale bar: 200 nm. (C) Four-point resistance measured on different vanadium NW arrays similar to those shown in (A): all arrays have higher resistance at lower temperature, and no superconductivity is observed. (D) Four-point resistance measured on different niobium NW arrays similar to those shown in (B): all arrays have higher resistance at lower temperature, and no superconductivity is observed.

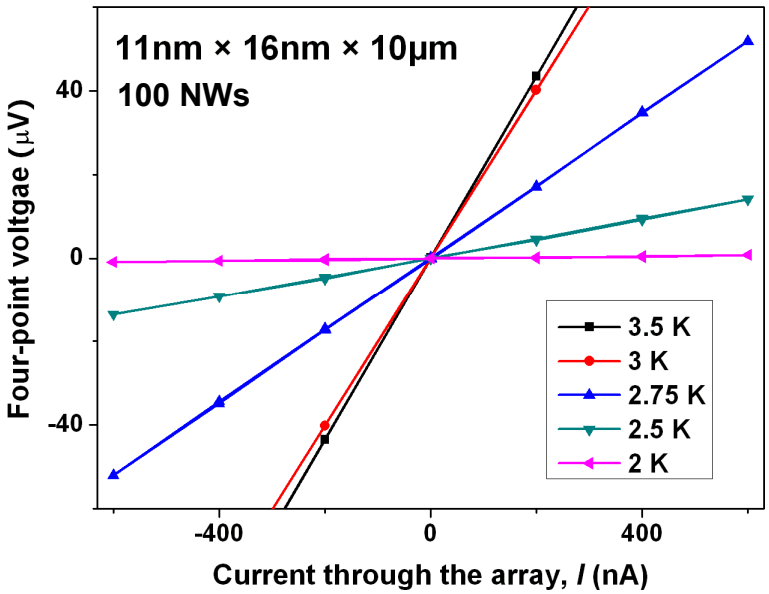

Figure S3. Representative four-point *V-I* curves in the low-current limit for an array of 100 Nb NWs of cross section 11nm × 16nm and *L* = 10 μm. Because there are typically ~100 parallel NWs in each array, the *total* current level of ~100 nA used in our resistance measurements corresponds to ~1 nA per individual NW. This is well below the current limit beyond which the *V-I* relationship is expected to become nonlinear in a NW, $I_0 = 4ekT/h = 13\ \text{nA}\cdot(T/\text{K})$,(Tinkham 1996) which is ~20 nA for the base temperature of our system. As a result, Ohmic (linear) *V-I* curves are obtained at all temperatures, and the resistance calculated from linear fits to such *V-I* curves can be directly compared with theories.

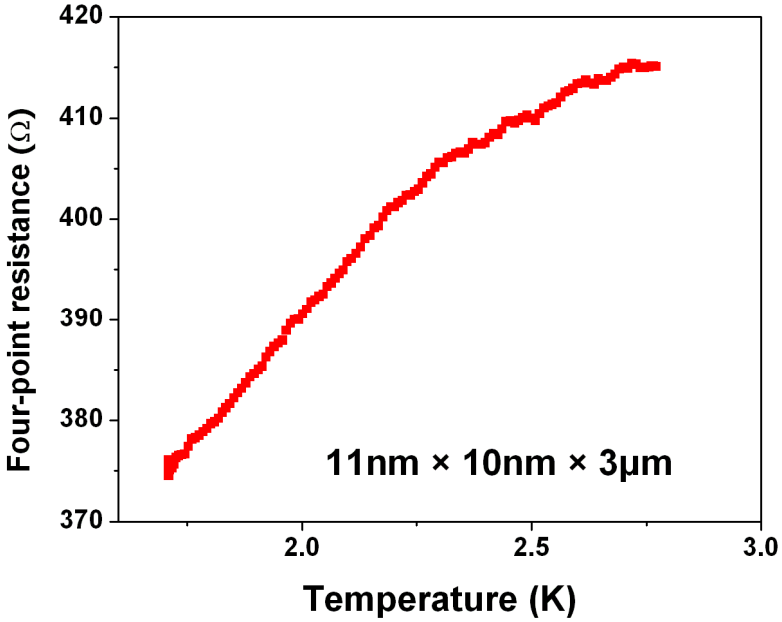

Figure S4. A close-up of the temperature dependence for the four-point resistance of an array of 12 NWs of cross section 11nm × 10nm and *L* = 3 μm. Onset of superconductivity is found ~2.5 K, and the resistance continues to drop toward zero when the temperature is lowered. 10% of total resistance vanishes at the base temperature 1.7 K.

References for the Supporting Information

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