# DESIGN OF SOFT-ERROR-AWARE SEQUENTIAL CIRCUITS WITH POWER AND SPEED OPTIMIZATION


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To my husband, Zach, with whom all things are possible and without whom none of this would have been possible

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# CHAPTER I

# INTRODUCTION

The increasing demand of mobile, battery-powered electronic systems (e.g., lap-top computers, cellular phones, etc.) has been a major driving force for the design of microelectronic circuits with low power dissipation. More generally, as density, speed, and complexity of the digital chips continue to increase, the cost associated with cooling and heat removal such chips are becoming prohibitive. In addition to cost, there is the issue of reliability that points to the need for low power design [1]. Apparently, there is a high need for designing of high-throughput, low-power digital systems. For the low-power design techniques, it ultimately come down to a fundamental set of concepts: power is reduced by lowering either *the supply voltage*, *the voltage swing*, *the physical capacitance*, *the switching activity* or a combination of the above [2]. A single-event effect (SEE) of circuits is however strongly dependent on the supply voltage and the physical capacitance. Reduction in supply voltage as well as technology scaling trends (smaller nodal capacitances) may result in dramatically increased sensitivity of the circuits to radiation. For this reason, SEE induced errors of the low power design has very high demanding to be taken into account especially when designing circuits for applications require high reliability.

A SEE occurs when an ionizing particle that travels through silicon producing electron-hole pairs in an integrated circuit (IC). If the SE ion strike deposits charge near a transistor, the deposited charge may potentially lead to a voltage change of the circuit node associated with that transistor. The voltage change of the circuit node may result in a single-event upset (SEU) in memory storage elements or a single-event transient (SET) in

combinational logic that may be latched into memory [3]. A SEU occurs when the deposited charge ($Q_{coll}$) is greater than the critical charge ($Q_{crit}$). The $Q_{crit}$ are based upon both the node capacitance and the restoring current (i.e., drive strength) of the logic cell. As the operating voltages and the dimensions of ICs are reduced to satisfy the ever-increasing demand for low power and higher density, the $Q_{crit}$ has decreased dramatically. $Q_{coll}$ was not shrinking as fast as $Q_{crit}$ have made deep submicron low power ICs increasingly susceptible to radiation induced errors [4]. A SET in combinational logic result in an error is a strong function of three masking factors: electrical masking (SET pulse have insufficient amplitude to propagate through logic gates), logic masking (SET pulse is blocked from propagating through the circuit), and latch-window masking (SET pulse can not get latched in to a latch).

In this proposed research, a methodology for evaluating SEE performance of sequential logic circuits have been developed. A study of the relationship between circuit SEE tolerance and power consumption is performed using this methodology. The purpose is to provide a figure-of-merit (FOM) for designers to make informed decisions on meeting power, speed, and SE specifications. To comprehensively comment on the design parameters of different sequential logic circuits, a FOM is defined as the inverse of the product of power and SE cross-section ($PCSP^{-1}$). Since minimization of power and SE cross-section is desirable, a lower PCSP value and thus a higher FOM value can be considered to be an indicator of an optimized design. This work focuses on the study of both power consumption and SEE tolerance at device and circuit-level. Sequential circuits are used as circuit examples in this proposed research. The ultimate goal of the work is to provide designers with capabilities and FOM to choose the suitable low power and SEE tolerance design for different targeted design specifications and operating environment.

## 1.1 Contribution

Upon completion of this work, some of the novel contributions of this dissertation include:

1. **An empirical model for evaluating SEE performance of logic circuits have been developed.** Computing power can be reduced compare to previous simulation-based approaches. In additional, the proposed approach is easy to obtain and characterize compare to previous experimental-based approaches.

2. **SE characterization of different FFs fabricated in a 16-nm bulk FinFET CMOS technology have been performed for designing soft-error-aware circuits with power and speed optimization.** First time differential FF have been detailed analyzed for SE performance at 16-nm bulk FinFET technology node.

3. **A framework of designing soft-error-aware sequential circuits with power and speed optimization have been developed. This framework allows designers to expand sequential circuit designs of choice in terms of the low power designs for meeting target SER and speed specifications.** Usually there is a target SER value (protection level) that needs to be met by designers. Therefore, instead of traditional analysis (SER as a function of supply voltage, frequency, temperature, etc.) comparative analysis (FF/logic designs, supply voltage, and frequency yielding identical SER values) is carried out to identify the best performing (lowest power) designs for meeting SER specifications. By analyzing the test results based on such an approach, designers will have access to data that will allow them to optimize a circuit design along multiple dimensions (such as SER, power, and operating frequency). Such an analysis may also

yield significant power savings while meeting SER and speed specifications.

## 1.2 Summary of Document

The dissertation is composed of six additional chapters. **Chapter 2**, Background, provides a background on radiation effects in digital integrated circuits (ICs) and sequential circuits in particular. In this chapter, the fundamentals of power consumption in CMOS circuits, as well as literature review materials to understand the various power minimization techniques are presented.

Logic SER, similar to FF SER are a strong function of particles LET values, supply voltage and operating frequency. If designers focus on hardening FF cells only, unmitigated logic errors may not reduce overall SER to required specifications (especially if operating frequencies are in GHz range). Hence, characterization and mitigation of logic SER is necessary to determine the optimized approach for meeting SER specifications for sequential circuits. **Chapter 3**, Characterization of Logic SEEs for Advanced Technology, presents experimental results that characterize logic SEEs as a function of LET and supply voltage for 16-nm bulk FinFET technology node. Although the SER performance of logic circuits at low-LET particles is well studied for planar bulk CMOS nodes, characterization for FinFET nodes has been done only for frequency and not for particle LET's or supply voltages. In this work, the impact of supply voltage, operating frequency, and particle LET's on the logic SER for the 16-nm bulk FinFET node is experimentally characterized. It was observed that only mitigate the SET pulse-width may not necessarily be effective to reduce the strong impact of the supply voltage on the logic SER for the high-LET particles. In addition, results indicate that particle LET strongly affects logic SEU cross-section and reducing the operating voltages, used for reducing power consumption, will significantly increase SEU

cross-section for high-LET particles. Therefore, accurate and efficient estimation of combinational logic SEU cross-section at different circuit parameters and control variables (different LET particles, operating frequency, temperature, and supply voltage) is necessary for designers to identify best hardening design approaches. **Chapter 4**, An Empirical Model for Predicting SE Cross-Section for Combinational Logic Circuits in Advanced Technologies, develops a novel approach for evaluating SEE performance of logic circuits at different circuit parameters and control variables. An empirical method that uses experimental data from simple test structures for estimating SE vulnerability of any combinational logic circuit is presented. The estimated logic SE cross-section results obtained with the proposed method are within 2X average error when compared to the experimentally measured logic SE cross-section.

The primary goal of this work is to build a framework of designing soft-error-aware sequential circuits with power and speed optimization. A model for predicting SEU cross-section for any arbitrary logic circuit developed in Chapter 4 has been used to explore design space for logic circuits. In order to create a model for FF cells that will allow designers to identify the best performing (lowest power) designs for meeting SER specifications, comprehensive study on the SEU of different FF designs have been carried out in this work. **Chapter 5**, Characterization of FFs SEEs for Advanced Technology, details the process to characterize SEU of different FFs. Effects of operating frequency, supply voltage, particle LET, and temperature on SEU cross-section for different FFs are evaluated and actual experimental data are reported. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints.

Designers have access to a library containing a wide variety of FF cells and logic circuits with varying levels of performance penalty and radiation hardness. Traditional SE analysis for these FF designs and logic circuits usually compares SE performance for a given set of conditions (supply voltage, speed, temperature, particle LET, etc.). Designers need to identify the best performing (the lowest power requirement) FF designs and logic circuits for meeting SER specifications. Since design library dose not contain such comparative analysis (SER as a function of power), designers have to carry out additional analysis and test. **Chapter 6**, An Empirical Model Based Approach to Explore Design Space for Sequential Circuits, explains a design methodology employing empirical models for identifying the optimum combination of topology, supply voltage, and frequency for a given SEU cross-section specification. By analyzing the sequential circuits based on such an approach, designers will have access to data that will allow them to optimize a circuit design along multiple dimensions (such as SER, power, and operating frequency). Such an analysis may also yield significant power savings while meeting SER and speed specifications.

**Chapter 7**, Conclusions, summarizes the major contributions of the research.

Fig I.1 is used to summarize the research objectives of this work discussed above. This work main objective is to develop a framework of designing soft-error-aware sequential circuits with power and speed optimization for designers to identify the lowest power designs for meeting SEU and frequency specifications. SEU analysis of sequential circuits in this work has been divided into SEU analysis of FFs and logic circuits. In order to explore designs space of power, SEU, and operating frequency for FFs and logic circuits, SEU analysis of FFs and logic circuits as a function of supply voltage and frequency are carried out in this work. For SEU analysis of FFs, simulation-based method and experimental results are

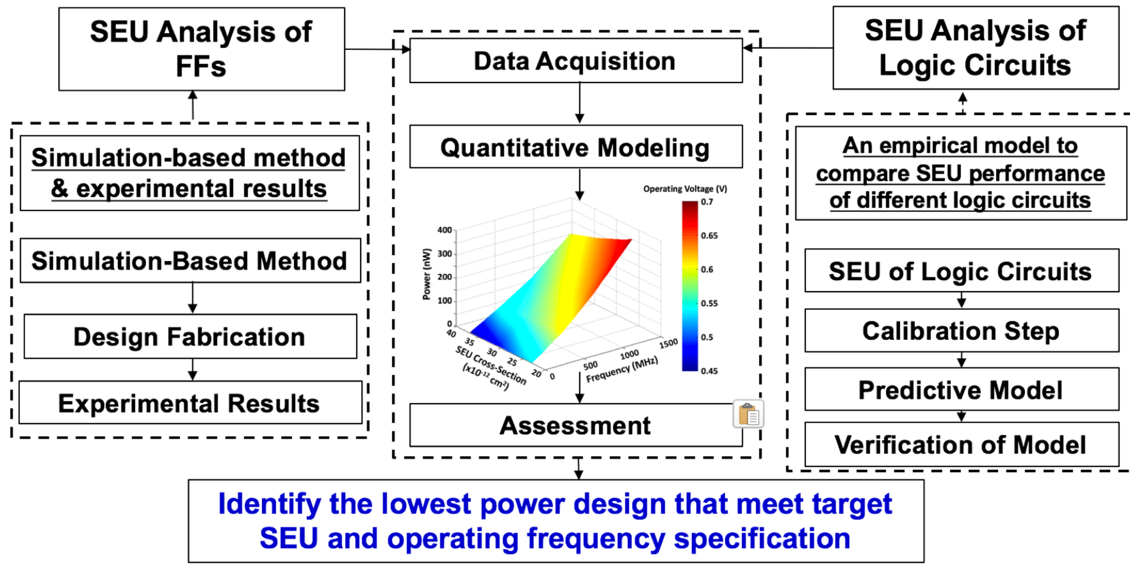



Figure I.1: Summary of the main research objectives of this work.

discussed in this work (Chapter 5). Experimental results have been used in this work for improving accuracy of the framework. A method to compare SEU performance of different logic circuits for early design phase is presented (Chapter 4). The method is used to created the design space of logic circuits that will allow designers to identify the lowest power designs for meeting SEU and operating frequency specifications. After analyzing the SEU of FFs and logic circuits, the data are imported to the Data Acquisition step. Results from Data Acquisition step are used to calculate the fitting parameters that will allow designers estimate the necessary parameters (e.g., power, frequency, and SEU) quickly and easily during Assessment step. During Assessment step, different logic designs and FFs are evaluated as a function of supply voltage, frequency, power, and SEU with the fitting parameters developed in Quantitative Modeling step. A multi-dimensional chart for all designs is then generated to allow designer to identify the lowest power designs for meeting SEU and operating frequency specifications.

Each chapter corresponds to a published paper, and contains expanded detail not included in the paper publication.

# CHAPTER II

# BACKGROUND

The overview of radiation effects in digital ICs and radiation environment are summarized in this chapter. In addition, previous methods to predict the SEU at the sequential circuits level are discussed. The fundamentals of power consumption in CMOS circuits, as well as literature review materials to understand the various power minimization techniques are also presented.

## 2.1 Overview of Single-Event Effects in ICs

Electron-hole pairs are created when an energetic particle pass through a semiconductor material. The electron-hole pairs are generated mainly via three mechanisms: coulomb scattering [5], ion-nuclei [6-8], and spallation [9]. When the electron-hole pairs generated in or in the neighborhood of a p-n junction, the charge is collected in the depletion region of the p-n junction, producing a measurable transient photocurrent [10]. The charge collection in IC junctions takes place via drift collection [10], funneling [10-12], and diffuse [5]. In summary, a typical time-dependent current at a struck p-n junction as shown in Fig. II.1. The charge collected ($Q_{coll}$) in the junction is the integral of the illustrated pulse. The figure illustrates that the rise times are controlled by the drift and the funnel mechanisms, which lasts up to a few hundred picoseconds. The slow component or the tail of the transient is a result of the carriers collected from outside the depletion region of the p-n unction (via diffusion). When electrons or holes released by a particle strike are confined to a well or body region in which a transistor is located, a somewhat similar but distinct mechanism exists. A potential raise in the channel (body) region, for instance for the NMOS transistor, can lower the source/well potential barrier leading to the source injects electrons into the

channel [13-15]. The drain collects these electrons, thus increasing the total amount of charge

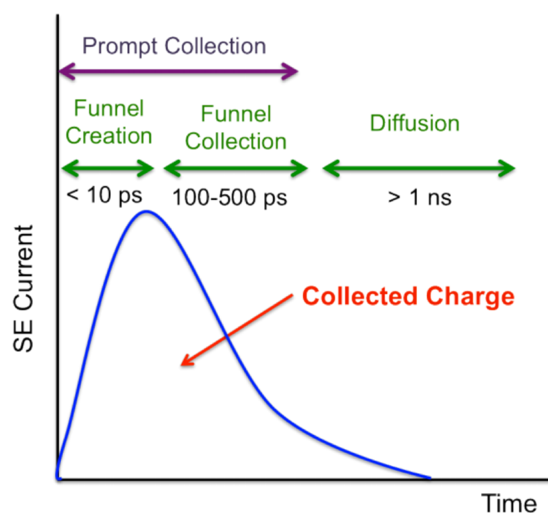



Figure II.1: Shape of a representative single event pulse measured at a struck p-n junction [5].

collected by the drain region during the radiation event. At circuit-level, this charge will be represented as a transient current and causing a transient voltage glitch. The deposition of the charge in a circuit relate to the particle LET and location of the strike. If the glitch occurs in a combinational node, one or more downstream state elements can be latched due to the glitch. If the glitch occurs in a state holding element, the stored bit can be flipped in the element feedback structure.

2.1.1 SEUs in Logic

Three masking factors can prevent the glitch from causing an upset in state, depending upon the input vector applied to the circuit when the strike occurs [25]: 1) Electrical Masking occurs if a SET pulse is not of sufficient magnitude to propagate through logic gates, 2) Logic Masking occurs if a SET pulse dose not have a logically sensitized path through the circuit, 3) Temporal Masking occurs if erroneous SET pulse is not get stored in to a downstream state element.

2.1.2 SEUs in FFs

Data loss of FF occurs when the $Q_{coll}$ exceeds the critical charge ($Q_{crit}$) that is stored in the sensitive node [3]. $Q_{crit}$ is the minimum amount of charge required to flip the nodal value of a feedback structure. It depends on the output capacitance of the struck node, supply voltage, restoring drive, and the feedback delay.

2.1.3 Radiation Environments Overview

Different regions of the magnetosphere including the bow shock, magnetopause, and radiation belts are shown in Fig. II.2 [16]. In space, the main sources of energetic particles

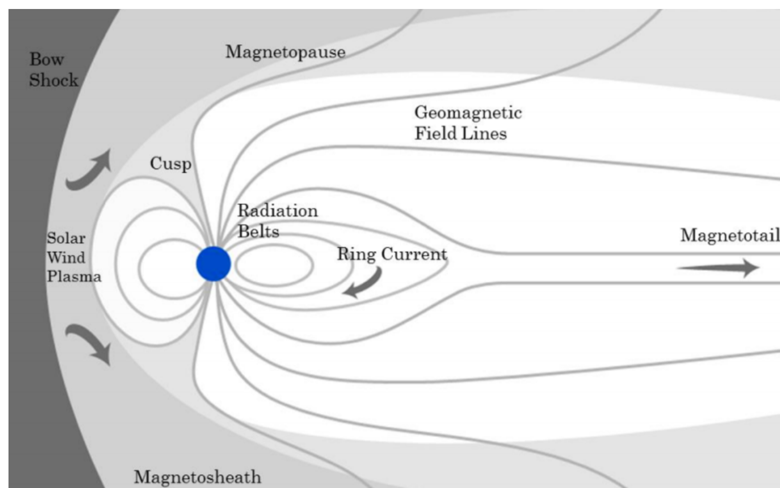



Figure II.2: The Earth's magnetosphere including the solar wind (pictured to the left), bow shock, magnetosheath and magnetopause [16].

(space radiation) are 1) protons and electrons trapped in the Van Allen radiation belts, 2) cosmic or galactic ray protons and heavy ions (from outside the solar system), 3) protons and heavy ions from solar flares, 4) heavy ions trapped in the magnetosphere. Energy to generate the ionization required to cause SEEs are not sufficient for the trapped heavy ions. Also, low-energy electrons are not known to cause SEEs. Therefore, the energetic particles causing

SEU include trapped protons in the radiation belts, cosmic solar particles (heavily influenced by solar flares), and galactic cosmic rays. Some protons undergo nuclear spallation reaction with nuclei (mainly oxygen and nitrogen nuclei) in the atmosphere to produce a number of light particles including neutron, photons, electrons, muons, pions, protons and neutrons, when the energetic protons enter the atmosphere (troposphere and stratosphere) of the Earth.

#### 2.1.3.1 The Van Allen Belts

The Inner Van Allen Belt traps high energy protons (energies < 1 GeV) and energetic electrons (less than 0.8 MeV) [17]. High-energy protons can damage spacecraft microelectronics [18]. For example, total dose problems, SEUs, and solar panel degradation can be caused by energetic proton events. Low-energy electrons do not possess enough energy to penetrate shielding materials [19]. At the South Atlantic Anomaly (SAA) the Inner Van Allen Belt dips closest to the Earth's surface and causes an increase in particle flux [20]. Hundreds of satellites operating in low earth orbit (LEO) at the Inner Van Allen Belt. The outer radiation belt in calm solar wind activity traps energetic electrons with energies up to ~10 MeV [21]. High-energy electrons are capable of penetrating spacecraft shielding and contribution to internal charging. Geostationary orbit moves in and out of the outer radiation belt. A region dominated by high-energy electrons and bombarded with energetic protons from solar events [18].

#### 2.1.3.2 Galactic Cosmic Rays (GCRs)

GCRs consist mostly of proton (84% hydrogen), alpha particles (15% helium), and less than 1% of heavier nuclei (e.g. C, N, O, Fe) [22]. Major SEUs in electronics are caused by GCRs ($> 10^{14}$ MeV), which in combination with the heavy ions (ions of any element heavier than helium). GCRs are capable of reaching the Earth's magnetosphere at solar

minimum, when the solar wind is low. However, at solar maximum when the high-speed solar wind speeds towards the earth act as a shield, GCRs are prohibited from entering a trajectory towards the magnetosphere. Therefore, the radiation from GCRs peaks at solar minimum and reaches a minimum at solar maximum.

#### 2.1.3.3 Terrestrial Environment

The most important product of the cosmic ray showers is the neutrons in terms of SEEs in the atmosphere [23]. An other important contribution of SEEs comes from alpha particles (helium nucleus built with two neutrons and two protons) [24]. Three natural decay chains called Thorium, Radium, and Actinium decay chains cause alpha emitters. Alpha particles lose energy as they penetrate through the package and device. Fig. II.3 shows the LET measured in charge per unit distance (fC/um) in silicon as a function of alpha energy.

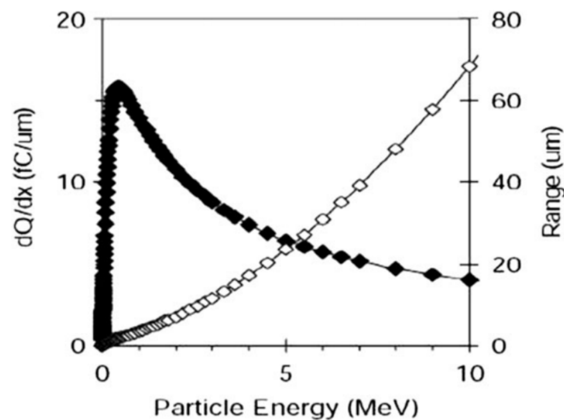



Figure II.3: Charge transfer (*solid boxes*) and range (*open boxes*) of alpha particles in silicon [24].

### 2.2 Previous Approaches to Sequential Logic SEU Analysis

This section reviews several of the SEU model methods that incorporate various masking factors (i.e. electrical, logic, and temporal) that affect whether a fault ultimately appears as an upset in the sequential logic circuits or not.

Analytical model using binary decision diagrams (BDD) and algebraic decision diagrams (ADD) for a unified symbolic analysis for circuit SEU performance is discussed in [26]. SEU_Tool uses parameterized closed-form circuit models for transient pulse generation, a structural VHDL logic-level simulation for pulse attenuation and propagation, a probabilistic model for transient capture, and a second high-level VHDL logic simulation for bit-error observability [27]. Serfert et al. uses SPICE-level simulation to investigate temporal masking of sequential circuits [28]. Mukherjee et al. have developed a performance model that is accepted for calculating architectural vulnerability factor (AVF) [29]. In [29], AVF is the probability that a fault in a processor structure will result in a visible error in the final output of a program. Other simulation-based approaches that are used to calculate impact of SEU in sequential circuits are [30-33].

## 2.3 Sources of Power Consumption

Following equation are summarized three sources of power dissipation in digital CMOS circuits:

$$\boldsymbol{P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage}} \qquad \text{(II.1)}$$

$P_{switching}$ represents the switching power of the circuits. $P_{short\text{-}circuit}$ is due to the direct-path short circuit current, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, $P_{leakage}$ is due to the leakage current, which can arise from reverse bias diode currents, sub-threshold effects, gate-oxide tunneling, punchthrough leakage current, and gate induced drain leakage. Each of these components are described in detail below.

### 2.3.1 Switching Power of the Circuits

Switching power dissipation occurs when the output of a gate changes states. Fig.

II.4 shows a circuit model for computing the dynamic power. The switching power dissipation is relatively independent of the rise or fall times for the input signals of the CMOS gate and the function being performed (i.e. the interconnection network of the NMOS and PMOS transistors). Referring to the figure, $V$ is an ideal constant voltage source. According to the laws of physics, the voltage $v_c(t)$ and the current $i_c(t)$ of a capacitance $C_L$ at time $t$ are given by [34]

$$\boldsymbol{i_c(t) = C_L \frac{dv_c(t)}{dt}} \tag{II.2}$$

During the charging cycle from time $t_0$ to $t_1$, the energy $E_s$ drawn from the voltage source is [34]

$$\boldsymbol{E_s = \int_{t_0}^{t_1} V i_c(t) dt} \tag{II.3}$$

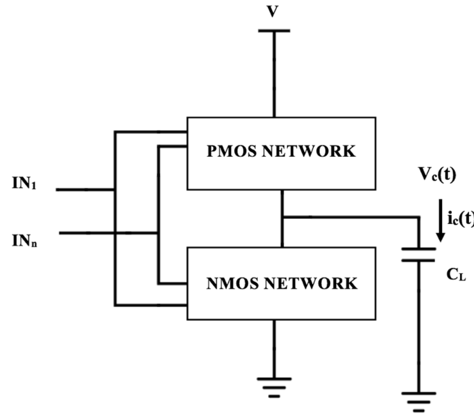



Figure II.4: Circuit model for computing the dynamic power of a CMOS gate.

Initially the voltage across the capacitor contains no charge, i.e. $v_c(t_0) = 0$. Assume that at the end of the charging cycle, the capacitor is fully charged, we have $v_c(t_1) = V$. Substituting Equation (II.2) into (II.3), we have [34]

$$E_s = C_L V \int_{t_2}^{t_1} \frac{dv_c(t)}{dt} dt = C_L V \int_0^V dv_c = C_L V^2 \quad \text{(II.4)}$$

Half of this is dissipated immediately in the PMOS network, while the other half is stored on the load capacitance. Then, when the capacitance is discharged, its energy being dissipated in the NMOS network. In summary, an energy of $C_L V^2$ is consumed when every time a capacitive node switches from ground to $V$ (and back to ground).

This leads to the conclusion that the switching activity of the signals is related to the CMOS power consumption. In this context, the node transition-cycle activity ($\alpha$) is the number of up transitions a circuit node traverses in one period of the clock. If we charge and discharge the capacitance at the frequency of $f$ cycles per seconds, for average CMOS power consumption [34,35]:

$$P_{switching} = \alpha C_L V^2 f \quad \text{(II.5)}$$

This classical result illustrates that the switching power is proportional to switching activity, capacitive loading, and the square of the supply voltage.

2.3.2 Short-Circuit Component of Power

A direct current path between power supply and ground are turned on for a short period of time during switching when the input waveforms are finite rise and fall times. This causes a short-circuit current from power source to ground and dissipates power. The shape of the short-circuit current curves is mainly dependent on three factors: the duration and slope of the input signal, the I-V curves of the P and N transistors (depend on their sizes, process technology, temperature, etc.), and the output loading capacitance of the inverter [34]. Short-circuit current can be computed quite accurately using circuit simulators such as SPICE. In

the case with no capacitive load, the short-circuit power can be given by [34,35]:

$$P_{short-circuit} = I_{sc} \cdot V = \frac{\beta}{12}(V - 2V_t)^3 \frac{\tau}{T_{clk}} \tag{II.6}$$

where $I_{sc}$ arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. $V$ is the supply voltage value. Let $\beta$ is the size of the transistors and $\boldsymbol{\tau}$ is the duration of the input signal. Let $V_t$ be the threshold voltage of both PMOS and NMOS transistors. $T_{clk}$ is the operating frequency of the system. The duration of short-circuit current depends on the transition period of the input signal and the output loading capacitance [36].

2.3.3 Leakage Component of Power

Two mainly sources of leakage current are described in detail below: reverse-bias diode leakage at the transistor drains, and sub-threshold conduction current. M. Haataja et al. described gate-oxide tunneling, punchthrough leakage, and gate induced drain leakage in detail [47].

2.3.3.1 Diode Leakage

When a transistor is turned off and other active transistor charges up/down the drain with respect to the off transistor's bulk potential, there is a diode leakage. The leakage current for the diode is given by [34,35]

$$I_{reverse} = I_s(e^{\frac{V}{V_{th}}} - 1) \tag{II.7}$$

where $I_s$ is the reverse saturation current, $V$ is the diode voltage, $V_{th} = KT/q$ is the thermal voltage ($V_{th}$ = 25.9 mV at room temperature). Due to the exponential dependence, the leakage current will be relatively independent of the diode voltage and will equal to the

reverse saturation current. Diode leakage could be significant for a system application which spends much of the time in standby operation.

#### 2.3.3.2 Sub-Threshold Leakage

There is a non-zero leakage current through the channel at the microscopic level, even though a transistor is logically turned off. Sub-threshold conduction current is given by [34,35]

$$\boldsymbol{I_{sub} = I_0 e^{(V_{gs} - V_t)/(\eta V_{th})}} \tag{II.8}$$

where $V_t$ is the device threshold voltage; $V_{th} = KT/q$ is the thermal voltage as defined in Equation II.7; and $I_0$ is the current when $V_{gs} = V_t$. The parameter $\eta$ is a constant depending on the device fabrication process. $I_{sub}$ drops exponentially as $V_{gs}$ decreases, since the exponent factor ($V_{gs}$ - $V_t$) has a negative value. At room temperature, the typical values for the sub-threshold slope (the amount of voltage required to drop the sub-threshold current by one decade) lie between 60 to 90 mV/(decade current), with 60 mV/dec being the lower limit.

## 2.4 Low-Power Design Methodologies

In this section, various low-power design techniques will be reviewed which span from the device-level to the circuit-level.

### 2.4.1 Device-driven voltage scaling

One approach to the selection of an optimal power supply voltage for deep-submicron technologies has been proposed based on considering the effects of device level properties involving velocity saturation. As feature sizes shrink below 1 um, carrier velocity saturation under high electric fields needs to be considered for the delay characteristics as a function of lowering the supply voltage. The current drive is significantly reduced due to the carrier

velocity saturation and is approximately given by

$$I = WC_{ox}(V_{dd} - V_t)v_{max} \tag{II.9}$$

where $v_{max}$ is the maximum velocity. Delay for submicron circuits is relatively independent of supply voltage at high electric fields when consider the equation for delay as $C_L V/I$.

The power supply voltage based on maintaining the speed performance for a given submicron technology is a "technology" based approach [37]. Kakumu et al. yielding the concept of a "critical voltage" which provides a lower limit on the supply voltage [37]. Very little penalty in speed performance when the voltage dropped to some extent for a velocity-saturated device. X. Wu et al. investigated the delays for FinFET and planar CMOS circuits at different voltages in Fig. II.5 [38]. One can observe that for FinFET/planar technology, the lower limit on supply voltage (critical voltage) was found to be about 0.355 V/0.85 V.

### 2.4.2 Energy-delay minimum based voltage scaling

Another approach for voltage reduction involves minimizing the energy-delay product [39]. Due to a lower supply voltage, there is reduced energy per computation and increased circuit delays for the ICs. The power-delay product (PDP) is used to measure the

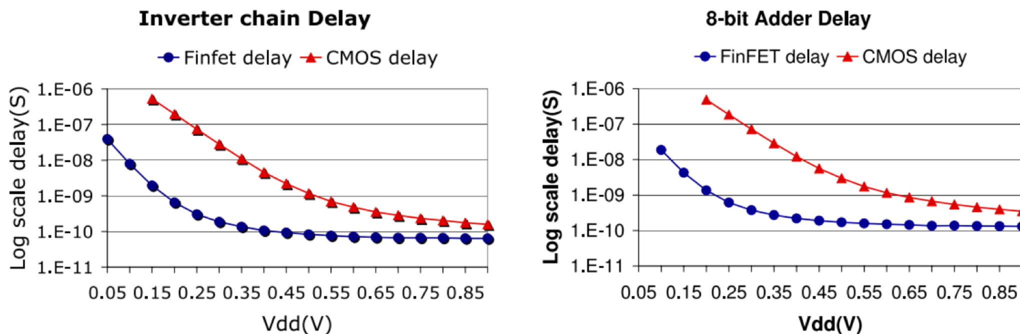



Figure II.5: Delay comparison at different $V_{dd}$ for FinFET and planar circuits. After [38].

average energy consumed per switching event. The energy-delay product (EDP) unifies a measure of performance and energy. The equation of EDP is given by:

$$\boldsymbol{EDP\ (Js) = PDP\ (J) \times Propagation\ Delay}$$
$$\boldsymbol{= Propagation\ Delay \times Average\ Power\ Dissipation \times Propagation\ Delay} \quad \text{(II.9)}$$

Q. Xie et al. studied the EDP results of a 20-stage inverter chain synthesized by using 7-nm FinFET devices as shown in Fig. II.6 [40]. One can see that the minimal EDP point (MEDP) is in the near-threshold voltage regime ($V_{MEDP} \approx 0.3$ V).

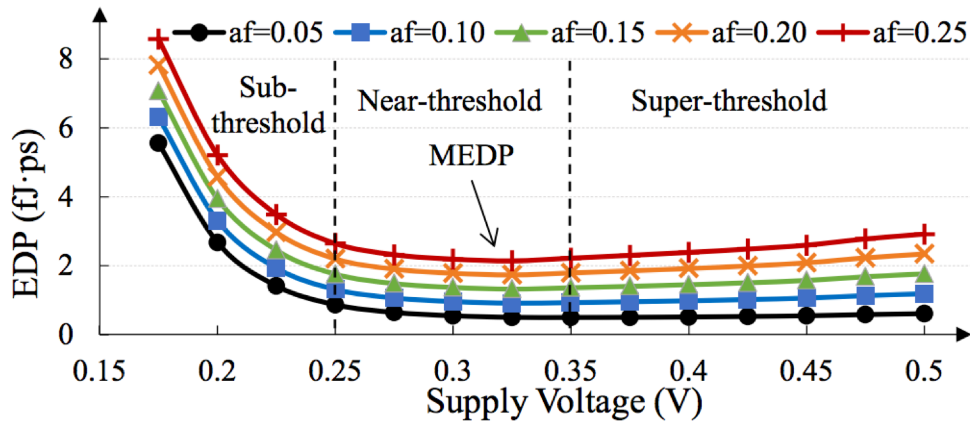


Figure II.6: Energy-delay product of a 20-stage inverter chain versus supply voltage at different activities factors (af) for FinFET 7-nm. After [40].

### 2.4.3 Voltage Scaling Through Optimal Transistor Sizing

Transistor sizing has been shown to be one of the most effective methods for reducing power consumption in CMOS digital circuits, independent of the choice of circuit topology. There are two issues of to what extent the (W/L) ratios should be used: logic-path gate sizing and gate-transistor sizing [41]. Logic-path gate sizing determines the sizes of the individual gates in relation to each other. On the contrary, gate-transistor sizing decides the best actual transistor sizes of each gate to attain the required performance. S. Turgis et al. investigated

the lowest power consumption of a chain of inverters (logic-path gate sizing) is when the tapering ratio equal to 4.25 [42]. However, when we are not allowed to restructure the transistor network, the gate-transistor sizing to attain the required performance needs to be estimated. For a path with general gates, H. Q. Dao et al. studied the minimal energy solution can be obtained by numerically solving a set of equation which was resulted from LaGrang method (different gate efforts) [43]. Inversely, A. Kabbani proposed the equal gate efforts to minimize the switching power dissipation [44]. Equal delay effort with scaled supply voltage technique provides a better power-delay product saving than only equal effort delay technique [45].

### 2.4.4 Voltage Scaling Using Threshold Reduction

In modern power optimization schemes, the gates on the critical path operate at lower threshold voltage to meet the performance requirements, and the gates on the noncritical paths operate at the higher threshold voltage to reduce the overall power consumption without performance degradation. Also, supply voltage can be scaled down (therefore lower switching power) without loss in speed by reducing the threshold voltage of the device. However, there are two main reasons that threshold voltage cannot be decreased unlimited [46]. The first reason is that the sub-threshold leakage current of the device increases exponentially as the threshold voltage decreases. The second reason is that the process variation the threshold voltage dose not scale accordingly. Moreover, the optimum threshold voltage must compromise between the control of the sub-threshold leakage and improvement of current drive at low supply voltage operation. For example, Fig. II.7 shows energy vs.

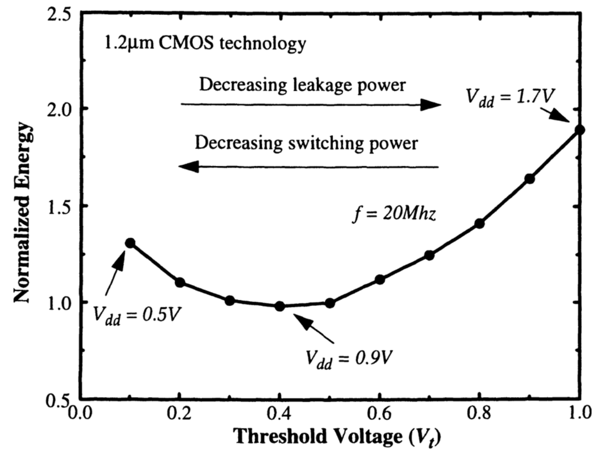



Figure II.7: Compromise between dynamic and leakage power dissipation through $V_t$ variation. After [34].

threshold voltage for a fixed through-put for a 16-bit data path ripple carry adder [34]. The optimum threshold voltage of the 16-bit data path ripple carry adder is around 0.4 V.

### 2.4.5 Leakage Power Reduction Approaches

Various leakage power reduction techniques at circuit level have been investigated [48-52]. These techniques include sleep, stack and sleepy stack, and power gating or MTCMOS for leakage power reduction. P. Oldiges et al. investigated the SEE performance of stacked devices on SOI. The paper shows that stacked devices have the potential to provide SEU immune design [53]. Moreover, it is obvious that most of the leakage power reduction techniques will not significant increase the SEE performance of the ICs. Therefore, in this paper, the SEE performance of leakage power reduction techniques will not be discussed.

## 2.5 Summary

The fundamentals of power consumption in CMOS circuits has been presented. Equations (II.5), (II.6), (II.7), and (II.8) express the fundamental modes of power dissipation

in CMOS ICs. Several basic principles of low power design techniques have been discovered by examining the equations. Since power is proportional to the square of the supply voltage, lowering the power supply voltage is the key to power reduction. However, lowering supply voltage comes at the cost of increased the sensitivity of the circuits to radiation. Since ICs dissipate most of the power when they are switching, an other major focus of low power design is to reduce the power switching activity and the effective switched capacitance. Decreasing capacitance comes at the cost of increased the sensitivity of the circuits to radiation as well. Therefore, design suggestions to the assurance that both the power consumption and SEE performance specifications are not violated are demanding.

In addition, being able to estimate any sequential logic circuits SEUs at different circuit parameters and control variables is necessary for designers to identify best hardening design approaches and confirm to the SEE performance specifications. Most previous approaches for modeling and/or predicting sequential logics SEUs are simulation-based approaches. An approach to couple experimental results and predictive models for SEE performance of logic circuits have been developed in this dissertation. The advantages and disadvantages of the proposed empirical method are compared to the previous approaches.

# CHAPTER III

# CHARACTERIZATION OF LOGIC SEES FOR ADVANCED TECHNOLOGY

The following content is an expanded version of a paper that is © 2018 IEEE. Reprinted, with permission, from:

H. Jiang, H. Zhang, R. C. Harrington, J. A. Maharrey, J. S. Kauppila, L. W. Massengill, and B. L. Bhuva, "Impact of supply voltage and particle LET on the soft error rate of logic circuits," *IEEE IRPS*, March 2018.

Logic SER, similar to FF SER are a strong function of particles LET values, supply voltage and operating frequency. If designers focus on hardening FF cells only, unmitigated logic errors may not reduce overall SER to required specifications (especially if operating frequencies are in GHz range). Hence, characterization and mitigation of logic SER is necessary to determine the optimized approach for meeting SER specifications for sequential circuits. This chapter presents experimental results that characterize logic SEEs as a function of LET and supply voltage for 16-nm bulk FinFET technology node. It was observed that only mitigate the SET pulse-width may not necessarily be effective to reduce the strong impact of the supply voltage on the logic SER for the high-LET particles. In addition, the chapter results indicate that particle LET strongly affects logic SEU cross-section and reducing the operating voltages, used for reducing power consumption, will significantly increase SEU cross-section for high-LET particles.

## 3.1 Introduction

Even though soft errors are a major threat to reliability, designers still need to focus

on power consumption first and foremost. Therefore, minimizing power consumption is the primary objective for all designers [54-56]. Reduced supply voltages are used to save power at the expense of increased soft-error rate (SER) [57]. Increased SER is mitigated through the use of hardened flip-flop (FF) cells. Experimental SER data for such FF cells as a function of supply voltage are used to ensure compliance with SER requirements. Such an approach worked very well for old technologies where FF SER dominated the overall SER and logic SER was minimal.

At GHz range of operating frequencies, contribution of logic SER to overall SER is significant [57]. Logic SER, similar to FF SER, are a strong function of particle LET values, supply voltage and operating frequency. If designers focus on hardening flip-flop cells only, unmitigated logic errors may not reduce overall SER to required specifications (especially if operating frequencies are in the GHz range). Hence characterization and mitigation of logic SER is necessary to determine the optimized approach for meeting SER specifications for sequential circuits [58].

Although the SER performance of logic circuits at low-LET particles is well studied for planar bulk CMOS nodes [58], [59-61], characterization for FinFET nodes has been done only for frequency and not for particle LET's or supply voltages [62-63]. In this work, the impact of supply voltage, operating frequency, and particle LET's on the logic SER for the 14/16-nm bulk FinFET node is experimentally characterized. Conventional SER models for logic errors along with experimental SET data are used to explain combined effects of particle LET, supply voltage, and frequency on logic SER.

## 3.2 Test Circuit Description & Experiments

### 3.2.1 Circuit Description

Multiple test ICs containing FF designs and three different logic circuits (*LC-1/2/3*) were fabricated in a 14/16-nm bulk FinFET CMOS technology node from a commercial foundry for SER characterization. The test circuits for DFF and DICE-like FF designs were implemented in CREST [64] configuration with an 8K-stage shift registers. Fig. III.1 shows the block diagram of the CREST circuit. Logic circuit designs were implemented using C-CREST approach [65]. C-CREST design consisted of a shift register design with logic circuits interspersed with DICE-based FF as shown in Fig. III.2. One DICE-based FF along

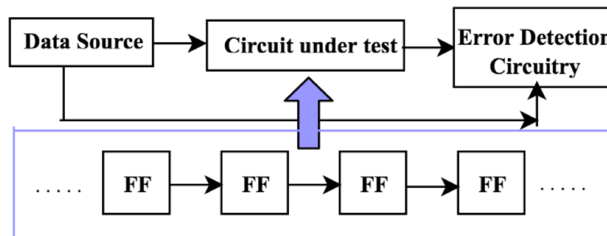



Figure III.1: CREST block diagram for the test circuit to evaluate SEU effects on flip-flops, after [64].

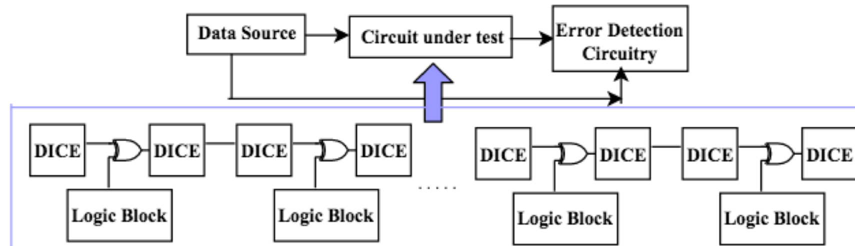



Figure III.2: C-CREST block diagram for the test circuit to evaluate SEU effects on flip-flops and logic circuits, after [65].

with the associated logic circuit comprises a single stage. The fabricated design consists of 2K of such stages to improve the error statistics. NMOS and PMOS transistors in each logic

gate were sized to yield equal sinking/sourcing currents. A separate test IC for autonomously capturing SETs at reduced supply voltages was also designed in a 14/16nm bulk FinFET technology generation. Similar to previous SET test chips, it consists of target logic, a propagation network and an SET capture circuit. Inverter design is utilized (3 fin and low $V_t$ design). The target logic is constructed by utilizing short logic chains combined in parallel by a balanced OR tree. This test IC used vernier method for measuring SET pulses for different logic gates [66].

### 3.2.2 Test Details

Heavy-ion tests were carried out at LBNL with 10 MeV/nucleon cocktail in vacuum for a variety of particles, at normal incidence, and at room temperature. Tests were carried out over a range of frequency varying from 2.5 MHz to 1.3 GHz at 600 mV, 700 mV, and 800 mV (nominal) of supply voltage for CREST and C-CREST circuits. All logic inputs for all logic circuits were kept constant during testing. Results presented below are for inputs $A_3A_2A_1A_0$ = 1000 and $B_3B_2B_1B_0$ = 0110 for logic circuits. The results presented below for logic circuits are for particle LET values of 6.09 (Si), 21.17 (Cu), and 58.78 (Xe) MeV-cm$^2$/mg. Data collected for the SET measurement circuits are for supply voltages ranging from 0.45 V to 0.8 V and particle LET values ranging from 0.89 (B) to 58.78 (Xe) MeV-cm$^2$/mg.

### 3.2.3 Experimentally Measuring Logic Cross-Section

To determine the FF cross-section alone, shift register chains with FF only (without logic circuits) were used (CREST circuit). To yield the logic cross-section, the value of the DICE-based FF cross-section was subtracted from the total cross-section for C-CREST circuit [65]. SET cross-section can be obtained from SET measurement circuits. The

expressions used to calculate the FF, logic, and SET cross-section are as follows:

$$\boldsymbol{Flip\ Flop\ Cross\ Section} = \frac{n_{FF-SEU}}{N_{FF} \times Fluence} \tag{III.1}$$

$$\boldsymbol{Logic\ Cross\ Section\ per\ Stage} = \frac{n_{C-CREST} - n_{FF-SEU}}{N_{logic} \times Fluence} \tag{III.2}$$

$$\boldsymbol{SET\ Cross\ Section} = \frac{n_{SET}}{N_{gates} \times Fluence} \tag{III.3}$$

where $\boldsymbol{n_{FF-SEU}}$ is the number of measured single-event upsets for FF, $\boldsymbol{N_{FF}}$ is the number of FFs in the CREST block shift register, $\boldsymbol{n_{C-CREST}}$ is the total number of errors measured from C-CREST circuit, $\boldsymbol{N_{logic}}$ is the number of logic circuits in the C-CREST block shift register, $\boldsymbol{n_{SET}}$ is the total number of SETs captured from the SET measurement circuit, and $\boldsymbol{N_{gates}}$ is the number of gates in the target logic blocks.

The FF, logic, and SET cross-section error bars were calculated as the standard error of the measurements (StdErr) [67]. The expressions used to calculate the error bars of the FF and logic circuits are as follows:

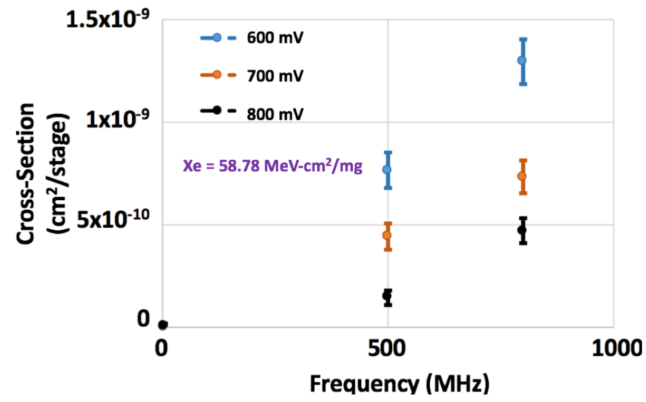
$$\boldsymbol{Flip\ Flop\ StdErr} = \frac{\sqrt{n_{FF-SEU}}}{N_{FF} \times Fluence} \tag{III.4}$$

$$\boldsymbol{Logic\ StdErr} = \frac{\sqrt{n_{C-CREST} - n_{FF-SEU}}}{N_{logic} \times Fluence} \tag{III.5}$$

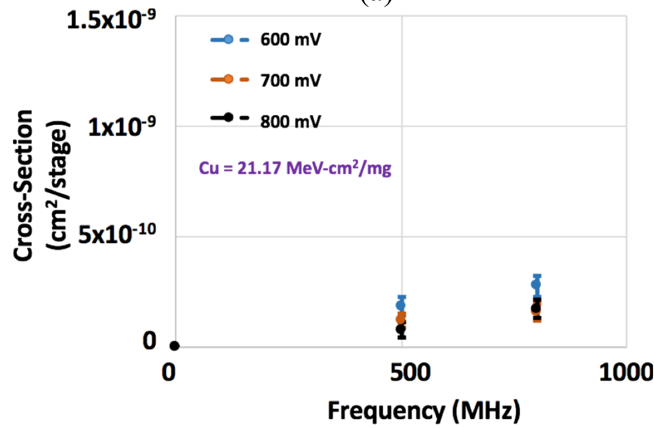
$$\boldsymbol{SET\ StdErr} = \frac{\sqrt{n_{SET}}}{N_{gates} \times Fluence} \tag{III.6}$$

### 3.3 Experimental Results

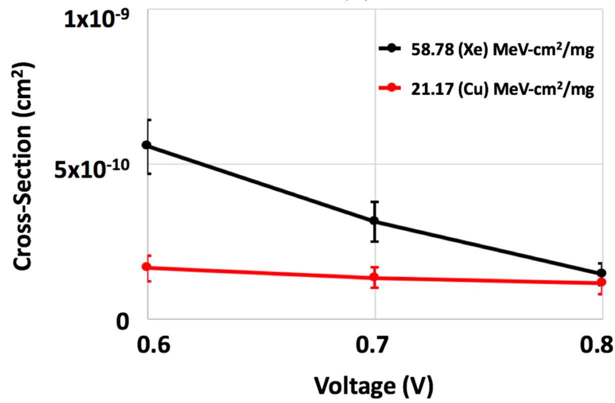
The impact of supply voltage and frequency on the logic cross-section (*LC-1*) at different values of particle LET is plotted in Fig. III.3. Fig. III.3(a) and III.3(b) show the cross-section for the logic circuit as a function of frequency (2.5 MHz, 500 MHz, and 1300 MHz) and supply voltage for low and high LET values. Solid lines in Fig. III.3(a) and III.3(b) are the trend lines for logic cross-section as a function of frequency, since SE cross-section




(a)




(b)




(c)

Figure III.3: Expreimental cross-section for LC-1 with inputs A = ’1000’ and B = ‘0110’ and 600/700/800 mV at (a) 58.78 (Xe) MeV-cm$^2$/mg and (b) 21.17 (Cu) MeV-cm$^2$/mg as a fucntion of frequency; (c) Cross-section of LC-1 for two different LET particles as a function of supply voltage at 500 MHz. For the other operating frequency, the trends are similar.

will increase linearly with operating frequency [68-71]. For low-LET particles, the slope of the logic cross section as a function of frequency is not affected significantly by a change in supply voltage. However, there is a strong supply voltage dependence for logic cross-section for high-LET particles. Fig. III.3(c) shows cross-section as a function of supply voltage for 500 MHz frequency. These results show that particle LET strongly affects the logic SER along with supply voltage and operating frequency and provides necessary data for modeling these effects for predictive capability. The impact of supply voltage and frequency on the other logic circuits (*LC-2* and *LC-3*) cross-section at different values of particle LET showed a similar trend as *LC-1* (as shown in Fig. III.3).

### 3.4 Discussion

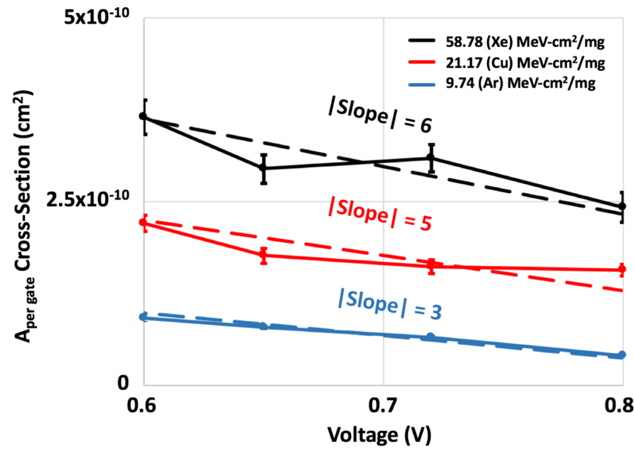
A simplified expression for logic cross-section as a function of masking factors is given as [72]

$$\boldsymbol{\sigma_{circuit}} \approx \sum_{\boldsymbol{logic\ gates}} \boldsymbol{A_{per\ gate}} \cdot \boldsymbol{LM} \cdot \boldsymbol{EM} \cdot \boldsymbol{TM} \qquad \textbf{(III.7)}$$

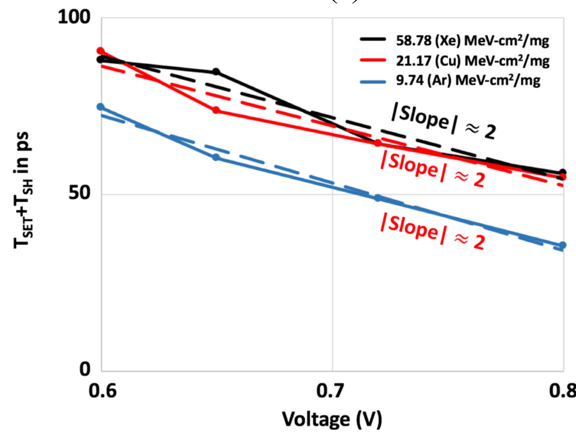
where $A_{per\ gate}$ is the sensitive area of a gate. *LM*, *EM*, and TM are the logical, electrical, and temporal masking factors at a given frequency. Sensitive area of a gate, electrical masking, and temporal masking are directly influenced by a change in the supply voltage and particle LET values). The temporal masking factor or latching probability of transients can be expressed as [73]

$$\boldsymbol{TM} = \sum_{\boldsymbol{T_{SET}}} \frac{\boldsymbol{T_{SET}} + \boldsymbol{T_{SH}}}{\boldsymbol{T_{cycle}}} \qquad \textbf{(III.8)}$$

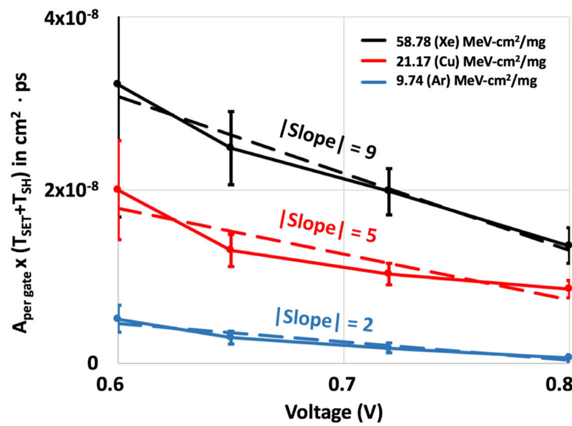
Here $T_{cycle}$ is the clock period and is the inverse of the frequency at which logic SEU cross-section is being estimated. $T_{SET}$ and $T_{SH}$ are the SET pulse widths and setup-and-hold time of the latch. Sensitive area of an inverter, average SET pulse widths, and setup-and-hold time




(a)




(b)




(c)

Figure III.4. Sensitive area of an inverter, average SET pulse widths, and setup-and-hold time as a function of supply voltage for different LET values (a) Sensitive area of an inverter; (b) Sum of average SET pulse widths and setup-and-hold time; (c) Sensitive area of an inverter times the sum of average SET pulse widths and setup-and-hold time.

as a function of supply voltage for different LET values are shown in Fig. III.4. Circuit-level simulator (SPICE) are used to obtain $t_{SH}$ as a function of supply voltage [74]. The slope of the curves (as shown in Fig. III.4) indicates the rate of change of $A_{per\ gate}$, $T_{SET} + T_{SH}$, and $A_{per\ gate} * (T_{SET} + T_{SH})$ with supply voltage. Higher value of the slope suggests steeper increase with frequency. Error bars in Fig. III.4(a) are obtained from (III.6). Average SET pulse width ($T_{SET}$) is used in Fig. III.4(b) [75, 76]. The slope of the curve increases as the charge deposited increases for $A_{per\ gate}$ (as shown in Fig. III.4(a)), since the sensitive area of a gate at low-LET particle is about several orders of magnitude smaller than at high-LET particle. Unlike the sensitive area of a gate, the value of $T_{SET}$ at low-LET and high-LET are of the same order of magnitude. Thus the slope of the curve is similar as the charge deposited increases for $T_{SET} + T_{SH}$ (as shown in Fig. III.4(b)). As a result, the slope of the curve increases as the charge deposited increases for $A_{per\ gate} * (T_{SET} + T_{SH})$ (as shown in Fig. III.4(c)). Based on (III.7) and (III.8), the supply voltage has a strong impact on the high-LET particles SER of combinational logic circuits and the low-LET particles of the combinational logic SER is relatively unaffected by supply voltage variation can be explained (as shown in Fig. III.3(c) and Fig. III.4(c)). Based on data from Fig. III.4, it is clear that reduced supply voltage will yield increased sensitivity to SER for high-LET particles. SET mitigation techniques, that only mitigate the SET pulse-width [77, 78], alone will not be sufficient to overcome strong impact of the reduced supply voltage on the logic SER for high-LET particles.

## 3.5 Conclusions

Logic SER shows much steeper increase as a function of frequency for high-LET particles compared to that for low-LET particles. Single-event transient (SET) experimental data are used to explain the results. Results suggest that reducing the operating voltages, used

for reducing power consumption, will significantly increase SER for high-LET particles. SER susceptibility for low-LET particles does not increase significantly as supply voltage is reduced compare to high-LET particles. It was observed that SET mitigation techniques that only mitigate the SET pulse-width may not necessarily be effective to reduce the strong impact of the supply voltage on the logic SER for the high-LET particles.

CHAPTER IV

# AN EMPIRICAL MODEL FOR PREDICTING SE CROSS-SECTION FOR COMBINATIONAL LOGIC CIRCUITS IN ADVANCED TECHNOLOGIES

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H. Jiang, H. Zhang, J. S. Kauppila, L. W. Massengill, and B. L. Bhuva, "An empirical model for predicting SE cross-section for combinational logic circuits in advanced technologies," *IEEE Trans. on Nucl. Sci.*, vol. 65, no. 1, pp. 304 – 310, Jan. 2018.

Previous chapter results indicate that particle LET strongly affects logic SEU cross-section and reducing the operating voltages used for reducing power consumption, will significantly increase SEU cross-section for high-LET particles. Therefore, accurate and efficient estimation of combinational logic SEU cross-section at different circuit parameters and control variables (different LET particles, operating frequency, temperature, and supply voltage) is necessary for designers to identify best hardening design approaches. This chapter develops a novel methodology for evaluating frequency dependence of combinational logic SEU cross-section at different circuit parameters and control variables. An empirical method that uses experimental data from simple test structures for estimating SE vulnerability of any combinational logic circuit is presented. The estimated logic SE cross-section results obtained with the proposed method are within 2X average error when compared to the experimentally measured logic SE cross-section. Computing power can be reduced compare to previous simulation-based approaches. Moreover, the proposed approach is easy to obtain

and characterize compare to previous experimental-based approaches. The approach presented in this chapter can be used to explore design space for logic circuits in Chapter 6.

## 4.1 Introduction

Due to the scaling down of CMOS technology, both the number of transistors on an IC and the frequency of operation are increasing. With the ever increasing number of systems operating at GHz range of frequencies, contribution of combinational logic upsets has increased significantly to the overall SER of sequential circuits [58], [68], [79]. However, accurate and efficient estimation of logic SEU cross-section has been very difficult, mainly because of the large number of variables involved in characterization of logic SER.

Most approaches for modeling and/or predicting logic SER fall into two categories: pure simulation-based approaches and pure experiment-based approaches. Simulation-based approaches simulate logic SE effects by injecting charges at circuit nodes (for circuit-level simulations) and allowing the resultant single-event transient (SET) pulse to propagate through the circuit. These approaches usually need a lot of computing power and uneasy to change the circuit control variables [30-33]. Experiment-based approaches usually require fabrication of actual circuits to implement the application functions, followed by irradiation experiments while exercising the circuit with appropriate software/input conditions. Both of these approaches represent high cost in terms of manpower and time commitments. Other researchers have tried using empirical data (for SET pulse-widths) to estimate logic SER [74]. Their approach requires SET pulse-width measurements which require a specialized test circuit and are difficult to obtain and characterize. Novel methods that can take existing test methods and test structures into consideration to make accurate SEU performance comparison for different logic SER will reduce overhead for incorporating SE analysis into

the design flow.

In this chapter, an empirical method to estimate the combinational logic SEU cross-section is presented. Proposed method uses experimentally measured cross-section of a conventional D Flip-Flop (DFF) and any arbitrary logic circuit cross-section to obtain necessary parameters. Once a given fabrication process is characterized this way, SEU cross-section for any logic circuit designed/fabricated in that process can be predicted. The estimated logic SE cross-section results obtained with the proposed method are within 2X average error when compared to the experimentally measured logic SE cross-section. Availability of such a model will allow designers to evaluate logic SEU cross-section and identify most sensitive sub-circuits for mitigation to meet IC-level SER specifications during the design phase.

The rest of the chapter is organized as follows. In Section 4.2, different simulation-based and experiment-based approaches to predict combinational logic SEU cross-section are classified and summarized. Section 4.3 describes the proposed methodology used to estimate the SEU performance of combinational logic circuits. Section 4.4 describes the test circuits and heavy-ion experimental details. Experimental results for estimating SE vulnerability of any combinational logic circuits are also discussed. In Section 4.5, estimated combinational logic SE cross-section and experimental results are analyzed and compared along with implications of the proposed methodology. Section 4.6 concludes the chapter.

## 4.2 Background

After an ion is incident on a semiconductor region, in order for a soft error caused by combinational logic cells, the ion strike must generate an SET pulse that can propagate through the circuit; the circuit-level inputs must allow an active path from the hit node to an

output of the logic circuit; and the SET pulse at the logic circuit output must get stored in a latch. The probability that an ion incident on a logic circuit will result in an error is a strong function of three masking factors: electrical masking (SET pulse must have insufficient amplitude to propagate through logic gates), logical masking (SET pulse must not be blocked from propagating through the circuit), and temporal masking (erroneous SET pulse must get stored in to a latch).

A number of simulation-based approaches have been proposed to evaluate the susceptibility of combinational logic circuits to soft errors by modeling these masking effects. Fault simulation methods [80], BDD-based techniques [81], or probability-based approaches [82] can be used to estimate the logical masking effect. Unlike logical masking estimation which only requires static analysis, estimation of electrical masking and temporal masking need dynamic analysis of SET pulse propagation (e.g. fault injected at a random time within the clock period) and are strong functions of SET pulse characteristics. As a result, electrical masking and temporal masking calculations are orders of magnitude more tedious and less accurate than logical masking calculations. Various techniques have been proposed to capture the electrical and temporal masking effects in SEU simulations [31], [83-87]. However, these simulation-based approaches are either not sufficiently accurate or efficient to estimate the parameters for electrical and temporal masking effects for use by designers during the design phase. Other approaches have tried using experimental data (for SET pulse widths) to estimate logic SER [69], [74]. Their approach requires SET pulse-width measurements which are difficult to obtain and characterize.

To make assessment of SE effects during the design phase, a method to estimate the combinational logic SEU cross-section based on an empirical model is proposed here. The

accuracy of the model is traded off against the simplicity to quickly estimate SE cross-section values for different logic circuits to guide designers. Simple test circuits were fabricated at the 16-nm bulk FinFET node to obtain necessary parameters for the proposed model. Multiple combinational logic circuits were also fabricated in the same 16-nm bulk FinFET process and exposed to heavy-ion irradiations.

### 4.3 Proposed Empirical Approach

Estimating the logic SE cross-section involves calculating the sensitive area of a transistor in the circuit for a given SET pulse width and the associated masking factors for logical masking, electrical masking and timing masking (as mentioned in Section 2.2). A simplified expression for logic SEU cross-section as a function of masking factors is given as [88]

$$\boldsymbol{\sigma_{circuit}} \approx \sum_{\boldsymbol{logic\ gates}} \boldsymbol{A_{per\ transistor}} \cdot \boldsymbol{LM} \cdot \boldsymbol{EM} \cdot \boldsymbol{TM} \qquad \textbf{(IV.1)}$$

where $A_{per\ transistor}$ is the sensitive area of a transistor. *LM*, *EM*, and TM are the logical, electrical, and temporal masking factors at a given frequency. For advanced technologies, accurate temporal masking (the probability of storing an SET in a latch) has been derived from fundamental principles in [69], and is a function of the SET pulse width, flip-flop setup-and-hold time, and clock period. The temporal masking factor is given by the probability that a SET pulse ($t_{pw}$) perturbs the input voltage during the setup-and-hold time ($t_{SH}$), violating the setup-and-hold time rule. Based on their model in [69], Equation (IV.1) can be rewritten as

$$\boldsymbol{\sigma_{circuit}} \approx \sum_{\boldsymbol{logic\ gates}} \sum_{\boldsymbol{t_{pw}}} \boldsymbol{A_{per\ transistor}} \cdot \boldsymbol{LM} \cdot \boldsymbol{EM} \cdot \frac{\boldsymbol{t_{pw}} + \boldsymbol{t_{SH}}}{\boldsymbol{T_{cycle}} + \boldsymbol{t_{pw}}} \qquad \textbf{(IV.2)}$$

Here $T_{cycle}$ is the clock period and is the inverse of the frequency at which logic SEU cross-section is being estimated. $t_{pw}$ and $t_{SH}$ are the SET pulse widths and setup-and-hold time of the latch. Measurements for SET pulse widths have shown a wide variety of distributions, necessitating the second summation in (IV.2) over all SET pulse widths.

The logical masking prevents transients from propagating through the circuit due to input conditions on certain gates blocking the passage of the erroneous signal. The erroneous signal can only pass through logic gates that have favorable input conditions. For example, if the first input of a NAND gate were to receive an SET pulse with the second input at logic 0, the SET pulse will not affect the NAND gate output (effectively blocking the SET pulse from propagating through the NAND gate). For a given circuit with an SET pulse generation at a given node within the circuit, there may be only a few logic gates through which the SET pulse can propagate and reach an output node. These logic gates are termed as sensitive gates. Under these conditions, (IV.2) needs to be evaluated for only the sensitive transistors in the sensitive gates, and not all the transistors in the circuit (because contribution to the overall SER for non-sensitive transistors will be 0). Thus (IV.2) can be further simplified to

$$\sigma_{circuit} \approx \sum_{t_{pw}} A_{per\ transistor} \cdot N_{transistor} \cdot EM \cdot \frac{t_{pw} + t_{SH}}{T_{cycle} + t_{pw}} \qquad \text{(IV.3)}$$

Here $N_{transistor}$ is the number of the sensitive transistors for the logic block for an SET pulse under given input conditions.

Any circuit-level simulator (e.g. SPICE or HSPICE) can be used to obtain $t_{SH}$ from the worst case to the best case due to process variations [89]. Due to $t_{SH}$ variations, a range for the SEU cross-section of a combinational logic circuit will result. In this work, nominal value of the $t_{SH}$ is simulated in the SPICE simulator and used for the following analysis. For

better results, designers may wish to use corner parameter values for $t_{SH}$ estimation instead of nominal values.

The most challenging part for solving (IV.3) is calculation of sensitive area per transistor for a given SET pulse width. Both of these variables represent a range of values, making the overall estimation of logic SE cross-section very difficult. Researchers usually use many 3D TCAD simulations to obtain the sensitive area for a given logic (or for individual transistors within a logic gate). This is a very tedious process requiring significant investment in time and computing resources [90].

One way researchers have tried to reduce this complexity is by using an "equivalent" value of SET pulse widths [74]. This approach uses "equivalent" SET pulse width based on experimentally measured data. This empirical approach assumes a single-valued SET pulse width for the whole distribution and uses it for calculating SE cross-section. Their results show a very good predictive capability for logic SE cross-sections. Their approach still requires measurement of individual SET pulse widths through a dedicated test circuit.

Empirical approach proposed here uses a similar technique to estimate the representative values of sensitive area and SET pulse width. The proposed method uses SEU cross-section of a DFF and SEU cross-section of any combinational logic circuit as a function of frequency to estimate needed parameters. This characterization only needs to be done once for each technology node. Since these two test circuits are usually available in any circuit, fabrication of custom-designed test ICs may not be necessary for the proposed approach. Most commercial ICs will have scan chains available for evaluating the saturated DFF cross-section. Scan-DFF may have a slightly higher cross-section than a conventional DFF. Experimental data needs to be analyzed accordingly to account for additional gates.

The representative value of the sensitive area is estimated based on the cross-section of a conventional DFF design. Based on the SE cross-section of a conventional DFF and the number of the sensitive transistors in the DFF, equivalent sensitive area of a transistor ($A_{per\ transistor}$) can easily be estimated. This is used as a representative value for sensitive area for a transistor in (IV.3). This "equivalent" sensitive area per transistor represents all variations of logic gates on an IC (including those due to fabrication process parameters [91], [92]). Such an "equivalent" value of sensitive area loses accuracy, but makes the model simplistic for quick assessment of SE effects. As will be shown later in the Section 4.5, the use of "equivalent" sensitive area does yield reasonably accurate estimations for SEU cross-sections.

The remaining unknown factors in (IV.3) are $t_{pw}$ and $EM$. Since the measured combinational logic circuit's SEU cross-section already includes the electrical masking factor, if the SE cross-section for a logic circuit is available ($\sigma_{circuit}$ in (IV.3)), the

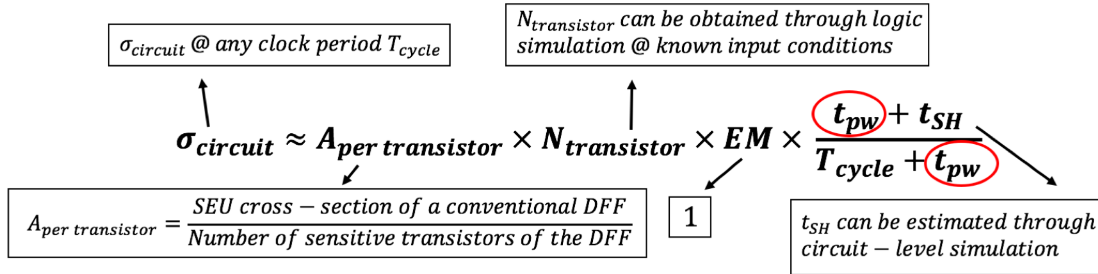



Figure IV.1: The process for obtaining the necessary parameters for Eqn. (IV.3) to solve $t_{pw}$.

"equivalent" value of $t_{pw}$ can be estimated for a given technology node with $EM$ equal to 1. Therefore, broadening or attenuation of the propagated transient pulse width doesn't require detailed analysis as carried out in [93]. Once $A_{per\ transistor}$ and $t_{pw}$ for a given fabrication process are known, they can be used to estimate logic SEU for any arbitrary logic circuit

design for that process. Fig. IV.1 pictorially shows the process for obtaining the necessary parameters for (IV.3) to solve $t_{pw}$.

## 4.4 Test IC Designs and Experimental Details

### 4.4.1 Circuit Description

Multiple test ICs containing DFF design and different logic circuits were fabricated in a 16-nm bulk FinFET CMOS technology from a commercial foundry to characterize their SER performance. The test circuits for DFF design were implemented in CREST [64] configuration with an 8K-stage shift registers. Fig. IV.2 shows the block diagram of the

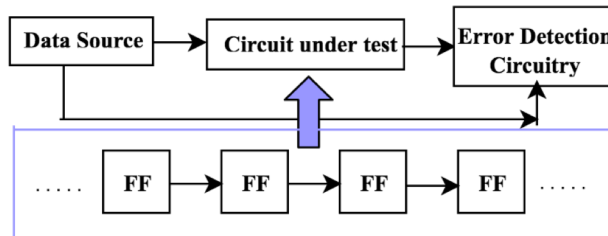



Figure IV.2: CREST block diagram for the test circuit to evaluate SEU effects on flip-flops, after [64].

CREST circuit. Conventional DFF and DICE-based FF designs with high (SVT) and low (LVT) threshold voltage options ($V_T$: SVT>LVT) were used in CREST configuration.

Logic circuit designs were implemented using C-CREST approach [65]. The Circuit-

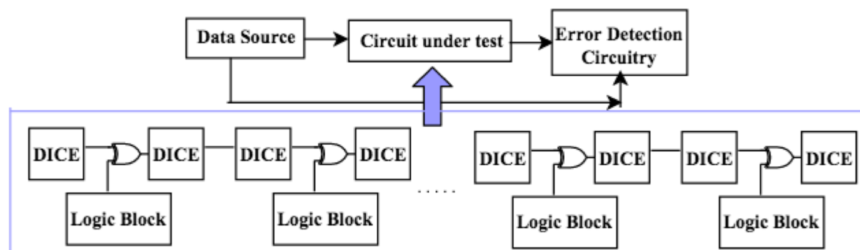



Figure IV.3: C-CREST block diagram for the test circuit to evaluate SEU effects on flip-flops and logic circuits, after [65].

Under-Test (CUT) consisted of a shift register design with logic circuits interspersed with DICE-based FF as shown in Fig. IV.3. One DICE-based FF along with the associated logic circuit comprises a single stage. The fabricated design consists of 2K of such stages to improve the error statistics. Six different C-CREST blocks each using a different logic circuit design and identical DICE-based FF were fabricated. NMOS and PMOS transistors in each logic gate were sized to yield equal sinking/sourcing currents. Table IV.I provides details about the gate count and transistor count for each individual logic circuits. Two versions of logic circuit LC-3 and LC-4 were designed using LVT and SVT options to evaluate the effectiveness of the proposed approach. LC-1 and LC-2 were designed using LVT option.

Table IV.I
Number of gates, gates type, and transistor count for logic circuits

| Circuit type | *LC-1*<br>Inverter | *LC-2*<br>Hardened Comparator | *LC-3*<br>Adder (Four-Bit) | *LC-4*<br>Comparator |
|---|---|---|---|---|
| Total # of gates | 104 | 24 | 56 | 48 |
| Type of gates | 91 NOT<br>11 NOR<br>2 XOR | 11 NOT<br>10 NAND<br>3 XOR | 40 NOT<br>24 NAND<br>16 XOR<br>16 NOR | 26 NOT<br>12 NAND<br>2 NAND<br>6 NOR<br>2 XOR |
| Total # of transistors | 238 | 88 | 200 | 148 |

All sub-circuits (on-chip error detection, error counter, etc.) other than the shift register used triple-modular redundancy (TMR) to eliminate error generation in support circuits. The design allows for GHz range testing of all test circuits on each IC. On-chip error detection and a serial output interface were utilized to export the data (error counts) for each shift register. FPGA was utilized to generate control signals and storage errors counts. An

on-chip PLL (capable of running up to 3 GHz) was used to clock shift registers.

### 4.4.2 Test Details

Heavy ion tests were carried out at LBNL with 10 MeV/nucleon cocktail in vacuum for a variety of particles, at normal incidence, and at room temperature. Tests were carried out over a range of frequency varying from 2.5 MHz to 1.3 GHz at 800 mV (nominal) of supply voltage. All logic inputs for all logic circuits were kept constant during testing. Different sets of input conditions were used during testing. Results presented below are for logic inputs $A_3A_2A_1A_0$ = 1000 and $B_3B_2B_1B_0$ = 0110. Input voltage conditions were chosen randomly. Since the test results are used only for estimating the temporal masking factor, test results from one set of input conditions is sufficient. The results presented below for logic circuits are for Xe with LET = 49.29 MeV-cm$^2$/mg.

### 4.4.3 Experimentally Measuring Logic Cross-Section

The logic and FF SE cross-section error boars were calculated as the standard error of the measurements. To determine the FF cross-section alone, shift register chains with FF only (without logic circuits) were used. To yield the logic cross-section, the value of the DICE-based FF cross-section was subtracted from the total cross-section for C-CREST circuit [64]. The expressions used to calculate the FF and logic cross-section are as follows:

$$Total\ Cross\ Section = \frac{Total\ Number\ of\ Errors}{Total\ Number\ of\ Stages \times Fluence} \qquad (IV.4)$$

$$Logic\ Cross\ Section\ per\ Stage\ = (Total\ Cross\ Section) - (Flip\ Flop\ Cross\ Section) \qquad (IV.5)$$

## 4.5 Experimental Results Vs. Estimated Results

In order to estimate the SE cross-section of any combinational logic circuits, $A_{per\ transistor}$ and $t_{pw}$ has to be solved first as mentioned in Section 4.3 (Fig. IV.1). Based on the

SEU cross-section for DFF and SEU cross-section for a logic circuit, values of these parameters were calculated. Table IV.II summarizes all necessary parameters values ($\sigma_{circuit}$, $A_{per\ transistor}$, $N_{transistor}$, $t_{SH}$, and $T_{cycle}$) for a logic circuit used for calculating parameters for the empirical model. The value of $t_{pw}$ was found to be 36.9 ps. The "equivalent" value of $t_{pw}$ (along with extrapolated values) is used for estimation of logic cross-sections for the other circuits listed in Table IV.IV and Table IV.V. All parameters, except $N_{transistor}$, in Table IV.II will remain the same for any circuit fabricated at the same 16-nm bulk FinFET technology node. In this work, $N_{transistor}$ for each circuit design was calculated by injecting faults at each node in the circuit and recording the number of faults

Table IV.II
Parameters Value As Needed To Solving $t_{pw}$ Based on (IV.3) And the Logic Circuit Used for the Empirical Model.

| Name | **LVT Circuit** |
|---|---|
| $\sigma_{T_{cycle}}$ | $3.34\text{x}10^{-9}$ cm$^2$ (*LC-1*) |
| $A_{per\ gate}$ | $4.26\text{x}10^{-10}$ cm$^2$ |
| $N_{gate}$ | 115 |
| $t_{SH}$ | 18 ps |
| $T_{cycle}$ | 769 ps (1300 MHz) |

that propagate to the output for a given input conditions. However, any one of the previously published approaches [80-82] may be used for estimating $N_{transistor}$. In this work, circuit-level simulations for injecting faults were carried out with the 16-nm bulk FinFET transistor models from the Arizona State University Predictive Technology Model (ASU PTM) set and Bias-Dependent model for injected charge using Cadence tool suite [73], [94], [95]. LET value of 49.29 MeV-cm$^2$/mg is used for the bias-dependent model based on the experimental

condition. However, any LET value that can generate a SET pulse width that does not get attenuated through the logic circuits can be used. SET pulse width will affect $N_{transistor}$ if *EM* is taken into consideration (shorter pulses may get attenuated and result in lower number for $N_{transistor}$). For the proposed model, *EM* is taken into consideration through SEU cross-section measurements, resulting in $N_{transistor}$ independent of SET pulse width.

Table IV.III lists $N_{transistor}$ for three different logic circuits fabricated on test ICs. It must be kept in mind that $N_{transistor}$ will be input conditions dependent. The results presented in the Table IV.III and the rest of the paper are for input conditions A = 1000 and B = 0110.

Fig. IV.4 and Fig. IV.5 compare the SEU cross-section of all logic circuits with LVT

Table IV.III
The Number of the Sensitive Gates for Different Logic Circuits Designs at Input Conditions $A_3A_2A_1A_0$ = 1000 and $B_3B_2B_1B_0$ =0110.

| Sorting order of logic circuits | Number of the sensitive gates |
|---|---|
| *LC-2* | 14 |
| *LC-3* | 13 |
| *LC-4* | 34 |

Table IV.IV
The SEU Cross-Section Ratio Between the Measured Logic Cross-Section and Estimated Cross-Section for LVT Designs.

| LVT | | | |
|---|---|---|---|
| Sorting order of logic circuits | Cross-section ratio | | |
| | 400 MHz | 800 MHz | 1300 MHz |
| *LC-2* | 1.3 | 0.78 | 1.1 |
| *LC-3* | 0.5 | 1.2 | 0.99 |
| *LC-4* | 0.65 | 1.2 | 0.84 |

Table IV.V
The SEU Cross-Section Ratio Between the Measured Logic Cross-Section and Estimated Cross-Section for SVT Designs.

| SVT | | | |
|---|---|---|---|
| Sorting order of logic circuits | Cross-section ratio | | |
| | 400 MHz | 800 MHz | 1300 MHz |
| *LC-3* | 1.9 | 2 | 2.2 |
| *LC-4* | 1.3 | 1.8 | 1.4 |

and SVT designs measured using C-CREST configuration experimentally and using the proposed model. Table IV.IV lists the SEU cross-section ratio between the measured data and estimated results at 400 MHz, 800 MHz, and 1300 MHz. Table IV.V lists the SEU cross-section ratio between the measured data and estimated results at 400 MHz, 800 MHz, and 1300 MHz for SVT designs. The ratio of predicted SEU cross-section to experimentally-measured SE cross-section for these logic circuits is less than 2X for all logic circuits at all frequency values. These results clearly show that the proposed technique can be used to estimate logic SEU cross-section of any arbitrary circuit. According to (IV.3) and the number of the sensitive gates for different logic circuits as listed in Table IV.III, SEU cross-section data for *LC-4* (shown in Fig. IV.4 (c)) will have the highest value and the highest slope (slope = 4) for SEU cross-section vs. frequency curve among all circuits tested in this work. SEU cross-section for *LC-3* (shown in Fig. IV.4 (b)) will have the lowest slope (slope = 1.7) for SEU cross-section vs. frequency curves. As shown in Fig. IV.4, both estimated logic SEU cross-sections and measured logic SEU cross-section are consistent with this analysis (based on (IV.3) and number of sensitive gates as listed in Table IV.III). The "equivalent" value of $t_{pw}$ (along with extrapolated values) from the logic circuit with LVT option are used for

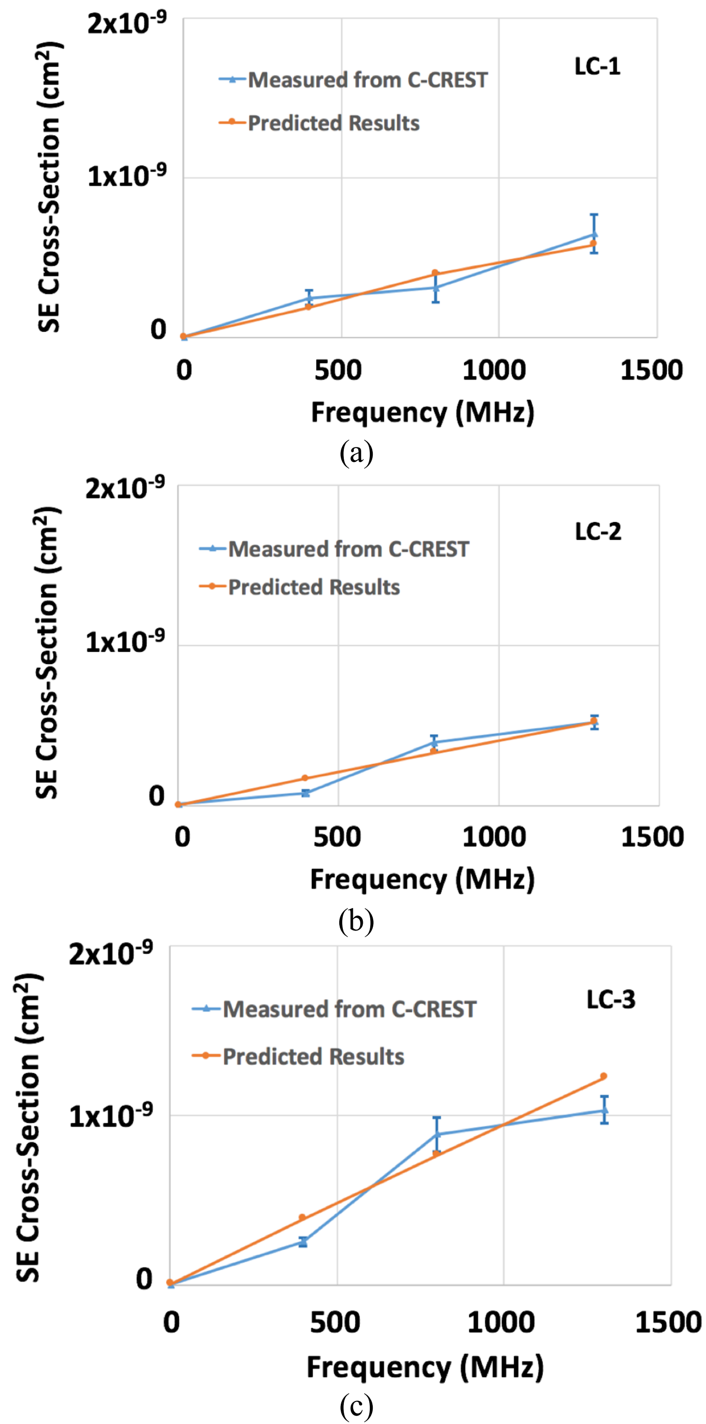
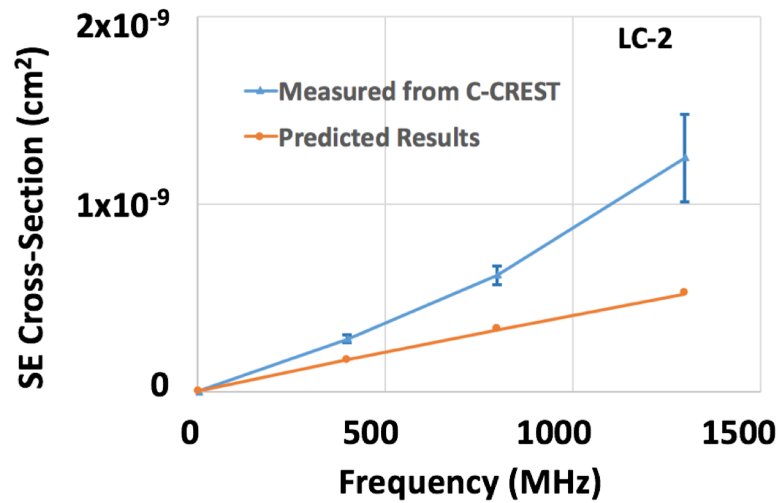
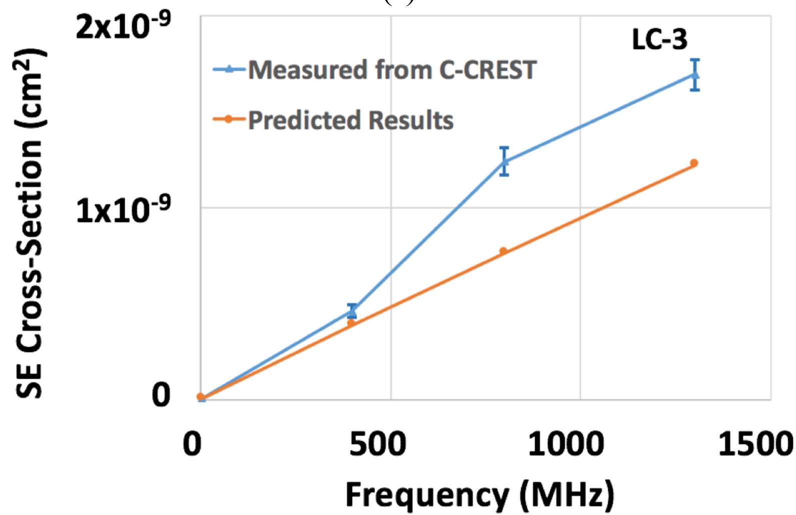



Figure IV.4: Comparison of estimated and experimental value of four different logic circuit. Comparison of estimated and experimental value for (a) LC-2, (b) LC-3, and (c) LC-4 circuits. The same scale on Y-axis is used to show the relative hardness for these circuits.




(a)




(b)

Fig. IV.5. Comparison of estimated and experimental value of two different logic circuit with SVT designs. Comparison of estimated and experimental value for (a) LC-3 and (b) LC-4 circuits. The same scale on Y-axis is used to show the relative hardness for these circuits.

estimation of logic cross-section for the circuits with LVT option. The ratio of predicted SEU cross-section to experimentally-measured SEU cross-section for these logic circuits is less than 1.2X average error for all logic circuit (as listed Table IV.IV). The "equivalent" value

of $t_{pw}$ (along with extrapolated values) from the logic circuit with LVT option are also used for estimation of logic cross-section for the circuits with SVT option. The ratio of predicted SEU cross-section to experimentally-measured SEU cross-section for these logic circuits is still less than 2X average error for all logic circuit. Average error differences in the predicted SEU cross-section for the SVT and LVT options can be ascribed to a significant difference in $A_{per\ transistor}$ of SVT and LVT options (68%).

The proposed model will also help designers determine the relative SE cross-section contribution of logic and FF designs (assuming FF SE cross-section data is available). Assume cross-over frequency is the one at which logic SE cross-section exceeds FF SE cross-section. If the operating frequency of a sequential circuit is higher than the cross-over frequency, it is better to harden logic circuits than to do so for FF cells [96]. Fig. IV.6 shows

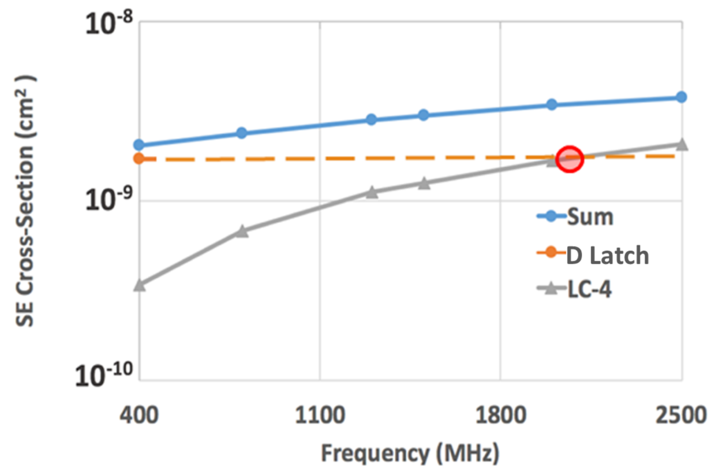



Figure IV.6: SE cross-section as a function of frequency for measured D latch SEUs and estimated LC-4 logic errors as well as their sum for Xe (LET~49.29 MeV-cm$^2$/mg) with supply voltage of 800 mV (nominal).

the SE cross-section values of D latch SEUs and LC-4 circuit logic errors as a function of

frequency. The cross-over frequency for these two circuits is ~2 GHz. The D latch curve shows experimentally measured results while the LC-4 curve shows predicted results using the proposed model. If the operating frequency of the resultant sequential circuit is higher than 2 GHz, designer should focus on hardening logic circuits to get the most improvement in SE cross-section for minimizing performance penalty. For this circuit, hardening D latch (for example, by replacing it with a DICE-based latch) will not improve the overall SE cross-section for the sequential circuit significantly. Proposed model will help designers to identify correct approach for such a scenario.

The proposed model is technology agnostic because it does not depend on the underlying technology node. For each technology node, it is necessary to carry out initial set of experiments to obtain the empirical values of "equivalent" sensitive area and "equivalent" SET pulse width. But once these are known, no further experiments are necessary for obtaining a reasonably accurate compare SEU performance of different logic circuits. These results show that the proposed empirical model will help designers and test engineers to make quick estimates of SE cross-sections based on just two experimental measurements.

### 4.6 Uncertainty and Error

The uncertainty in the proposed model is mainly come from $A_{per\ transistor}$, $N_{transistor}$ and $t_{pw}$. Fig. IV. 7 show the sensitivity of $A_{per\ transistor}$ and $t_{pw}$ on predicting SE cross-section of logic circuit *LC-1*. Results show that the sensitivity of $A_{per\ transistor}$ and $t_{pw}$ on predicting SE cross-section of logic circuits is insignificant. The sensitivity of $A_{per\ transistor}$ and $t_{pw}$ on predicting the other logic circuits (*LC-2* and *LC-3*) cross-section showed similar results as *LC-1* (as shown in Fig. IV.6). As shown in Fig. IV.4 and Table IV.III, slope difference in the SE cross-section for all the logic circuits (*LC-1*, *LC-2*, and *LC-3*) can be ascribed to $N_{transistor}$.

Therefore, highly accurate analysis of $N_{transistor}$ can improve the accuracy of the proposed

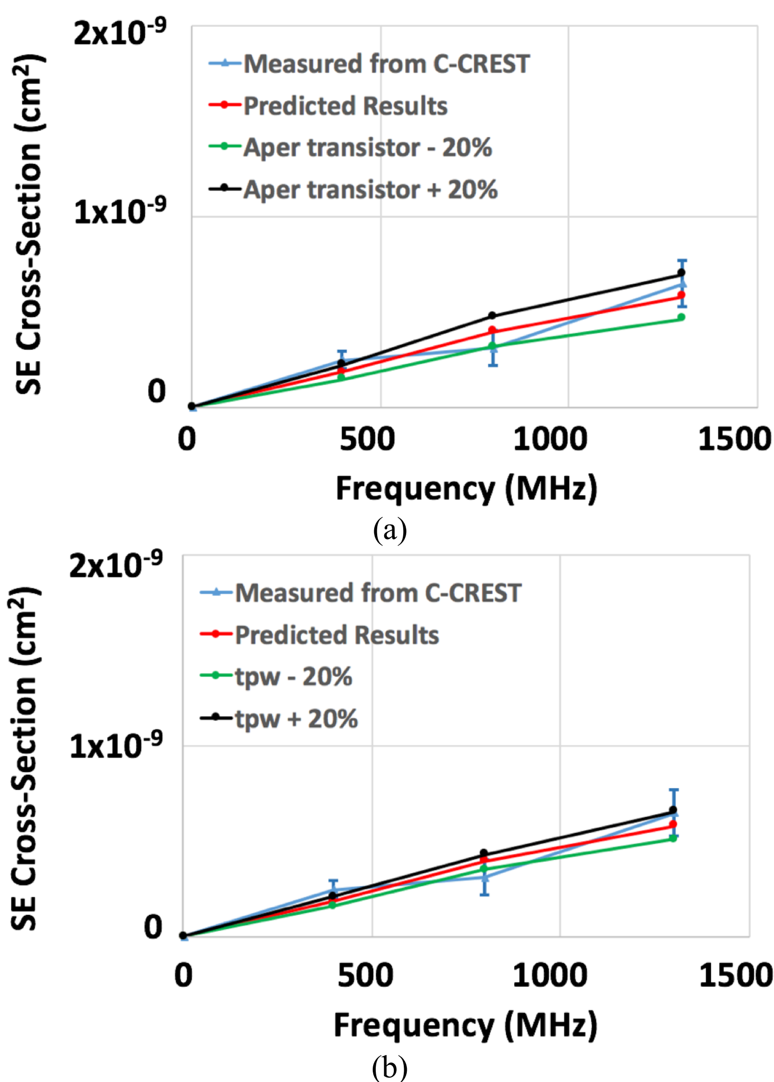



Fig. IV.7. sensitivity of $A_{per\ transistor}$ and $t_{pw}$ on predicting SE cross-section of logic circuit *LC-1*.

model. Fault simulation methods [80], BDD-based techniques [81], or probability-based approaches [82] have been developed to estimate $N_{transistor}$, since $N_{transistor}$ is strongly dependent on the circuit applications (input conditions).

## 4.6 Conclusions

An empirical model for predicting SE cross-section of logic circuits is developed. SE

cross-section values estimated using the proposed method were compared with the experimentally measured SE cross-section for a variety of logic circuits. Estimated SE cross-section matches well with the experimentally measured SE cross-section for all of these logic circuits. The “equivalent” value of $t_{pw}$ (along with extrapolated values) from the logic circuit with LVT option are used for estimation of logic cross-section for the circuits with LVT and SVT options. The ratio of predicted SEU cross-section to experimentally-measured SEU cross-section for LVT logic circuits is less than 1.2X average error. The ratio of predicted SEU cross-section to experimentally-measured SEU cross-section for SVT logic circuits is still less than 2X average error. The estimated logic SE cross-section results obtained with the proposed method are within 2X average error when compared to the experimentally measured logic SE cross-section. The proposed method can easily be included in the design flow to optimize and improve the SE performance of sequential circuits.

# CHAPTER V

# CHARACTERIZATION OF FFS SEES FOR ADVANCED TECHNOLOGY

The following content is an expanded version of three papers that are © 2016, 2017, and 2018 IEEE. Reprinted, with permission, from:

H. Jiang, H. Zhang, D. R. Ball, L. W. Massengill, and B. L. Bhuva, “SE performance of a Schmitt-trigger-based D-flip-flop design in a 16-nm bulk FinFET CMOS process,” *IEEE IRPS*, pp. 3B-2-1 - 3B-2-6, 2016.

H. Jiang, H. Zhang, T. R. Assis, B. Narasimham, B. L. Bhuva, W. T. Holman, and L. W. Massengill, “Single-event performance of sense-amplifier based flip-flop design in 16-nm bulk FinFET CMOS process,” *IEEE Trans. on Nucl. Sci.*, vol. 64, no. 1, pp. 477 – 482, Jan. 2017.

H. Jiang, H. Zhang, I. Chatterjee, J. S. Kauppila, B. L. Bhuva, and L. W. Massengill, “Power-aware SE analysis of different FF designs at the 14/16-nm bulk FinFET CMOS Technology Node,” *IEEE RADECS*, Oct. 2017.

The primary goal of this work is to build a framework of designing soft-error-aware sequential circuits with power and speed optimization. A model for predicting SEU cross-section for any arbitrary logic circuit developed in Chapter 4 has been used to explore design space for logic circuits. In order to create a model for FF cells that will allow designers to identify the best performing (lowest power) designs for meeting SER specifications, comprehensive study on the SEU of different FF designs have been carried out in this work. This chapter details the process to characterize SEU of different FFs. Effects of operating

frequency, supply voltage, particle LET, and temperature on SEU cross-section for different FFs are evaluated and actual experimental data are reported. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints in chapter 6.

## 5.1 Introduction

For the terrestrial environment, soft errors have become a serious reliability concern for advanced technology nodes [97]. For SRAM circuits, ECCs (Error Correcting Codes) and interleaving effectively reduce SE rates to a manageable level. SE mitigation for FF cells is still a major area of research, with many techniques for hardening FF cells proposed. However, the performance penalty for these techniques in terms of area, speed, and power can be significant. Compared to the spatial redundancy techniques (such as DICE FF [98], for example), techniques that provide a range of compromises on performance and SE rates reduction are highly desired by the semiconductor industry. In addition, with the ever increasing need for high-speed computation and communication systems comes the need for circuit designs that are power efficient and can operate at 10's of GHz. Conventional FF cells are power and area efficient for nominal operation of less than 1 GHz, but lose power efficiency when operated at 10's of GHz range. As a result, differential FF designs are fast becoming the design of choice for all communication networks. Therefore, investigation of SEU characterization and hardening techniques for differential FF designs are much needed by the semiconductor design community.

In this chapter, a conventional DFF, three representative radiation-hardening-by-design (RHBD), four available threshold voltage ($V_T$) implants of DFF, and a differential FF design (sense-amplifier based FF designs) fabricated at a 16-nm bulk FinFET CMOS

technology node is investigated for SEU performance. Effects of temperature, operating frequency, and particle LET on SEU cross-section for these different FFs are evaluated. Process to characterize SEU of different FFs are also included.

## 5.2 SE Analysis of Conventional DFF and three RHBD FF Designs

### 5.2.1 Schematic of FF Designs

Along with a conventional DFF design, shown in Fig. V.1, three representative RHBD are investigated. These RHBD designs are Schmitt-trigger-based DFF (STDFF), guard-gate-based DFF (GGDFF), and DICE-based DFF (DICE) [98-100]. The conventional DFF serves as a benchmark FF for comparing the performance of RHBD FFs. Fig. V.1 shows

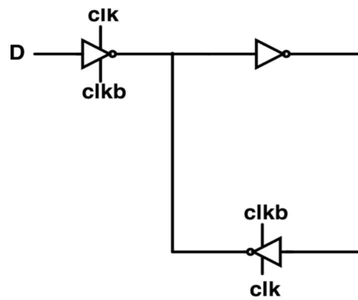


Figure V.1: A conventional D-latch design.

a conventional D-latch design. *D* node is the input of the circuit. When the *clk=0* (and *clkb=1*), the latch is operating in a transparent mode. Conversely, when *clk=1* (and *clkb=0*),

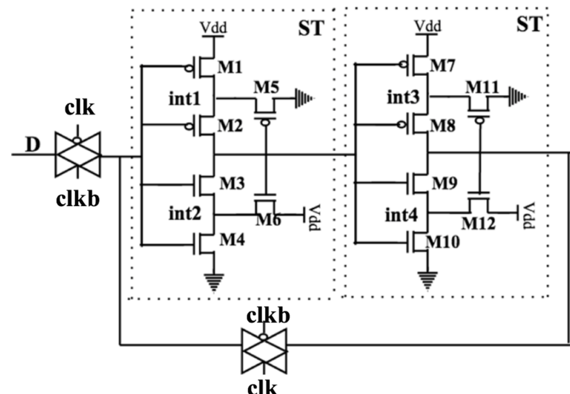


Figure V.2: Schmitt-trigger-based latch design.

the latch is operating in a storage mode. Fig. V.2 shows the schematic design of the Schmitt-trigger-based (ST) latch design (hysteresis-based structure) [99]. The presence of transistor M5 and M6 in the first ST inverter (M11 and M12 in the second ST inverter) introduce

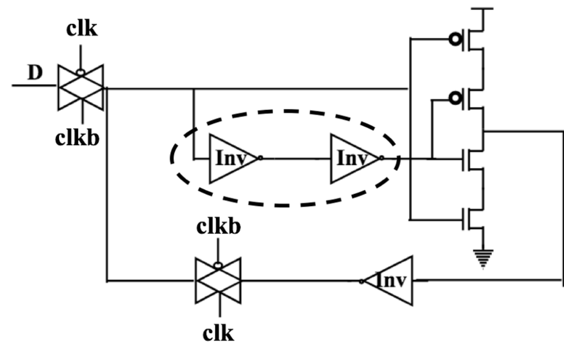



Figure V.3: Guard-gate-based latch design.

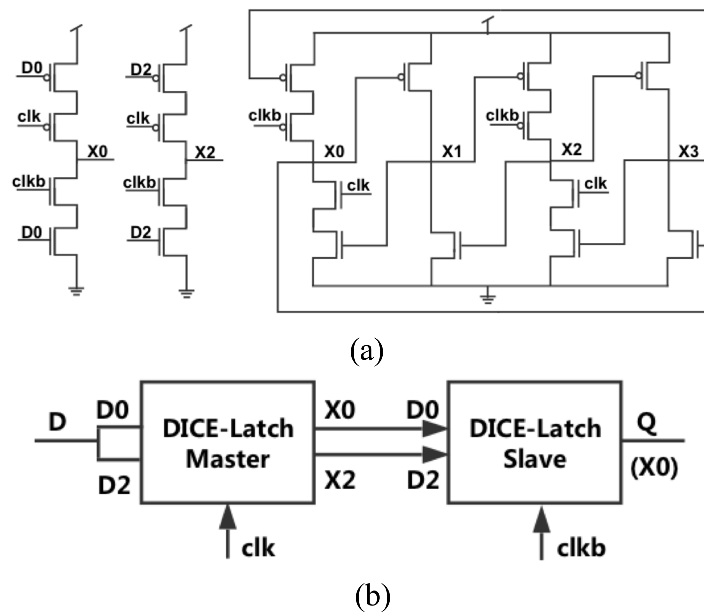



Figure V.4: (a) Schematic design of the DICE-latch containing four storage nodes. (b) The master-slave connections for the DICE flip-flop.

hysteresis by changing the charging and discharging currents at the inverter output node. Fig. V.3 shows the schematic design of a guard-gate-based (temporal filter or C-element

structure) latch design. The temporal structure is capable of rejecting SET pulses narrower than the two inverter delay element (circled in Fig. V.3) [100]. Fig. V.4 shows the schematic design of the DICE-based FF with the master and slave latches [98]. The DICE-based FF designs are known for their excellent SE performance. For all the FF designs, transistors with two fins are used as the smallest size transistors. Previous results have shown the effectiveness of these designs over DFF design in improving SE performance [98-100].

5.2.2 Simulation Results

The power, clk-to-q delay, total number of transistors, and IC area of the hardened FFs and the unhardened FF are tabulated in Table V.I. The power and delay simulation for the FFs in Table V.I were performed at 0.8 V, nominal supply voltage, and 0.55 V with 0%

Table V.I Power (at 0% and 100% data activity), clk-to-q delay, total number of transistors, and IC area of the three representative RHBD FFs and the conventioanl DFF (@16-nm bulk FinFET & *Vdd*=0.8 V and 0.55 V)

| Flip-Flops | Power @ 0% | | Power @ 100% | | Clk-to-q delay | | Total # of transistors | IC area |
|---|---|---|---|---|---|---|---|---|
| | At supply voltage (V) | | | | | | | |
| | 0.55 | 0.8 | 0.55 | 0.8 | 0.55 | 0.8 | | |
| Conventional DFF | 1 | 2.7 | 1.1 | 3.1 | 1 | 0.8 | 20 | 1 |
| Schmitt-trigger DFF | 1.5 | 4.1 | 1.9 | 5.1 | 2.4 | 1.7 | 32 | 2 |
| Guard-gate DFF | 1.4 | 3.7 | 1.93 | 5.2 | 1.7 | 1.2 | 28 | 1.7 |
| DICE | 2 | 5.3 | 2.3 | 6.1 | 1.2 | 0.8 | 40 | 3.8 |

and 100% data activity. Simulation results at other supply voltages are not shown for clarity. Data activity rate presents the average number of output transitions per clock cycle [101].

All the simulation results in this chapter were generated using the 16-nm models from the Arizona State University Predictive Technology Model (PTM) set and were carried out using the Cadence tool suite [73], [94]. All the power simulation results in this paper are average power over four clock cycles. The power results are normalized to the conventional DFF operating at 0.55 V with 0% data activity. The clk-to-q delay results are also normalized to the conventional DFF operating at 0.55 V. The IC area results are normalized to the conventional DFF. Power penalty of the DICE-based FF has the highest value among all of the other RHBD when the circuits are operating at the same supply voltage. STDFF has higher power penalty than GGDFF at 0% data activity. However, at 100% data activity, STDFF has lower power penalty than GGDFF. DICE-based FF has better clk-to-q delay than all the other DFF designs due to the master-slave connections as shown in Fig. V.4. The output of the master stage only has the delay of a clocked inverter to the output of the slave stage.

5.2.3 Test Details

A test chip was designed in a 16-nm bulk FinFET CMOS technology generation with 8K-stage shift-register chains of conventional DFF and the three representative RHBD FF designs implemented as CREST-circuit [64]. In addition, all four available threshold ($V_T$) implants (SVT, LVT, iLVT, and uLVT) of conventional DFF were used for identical circuit schematic and layout ($V_T$: SVT>LVT>iLVT>uLVT). Three representative RHBD FF designs are LVT implants. Error detection was carried out using on-chip circuits. Each FF shift register was clocked by an on-chip PLL that could operate at multi-GHz frequencies. The error detection and counter circuitry have the same voltage domain as the shift register chain. All support circuits used Triple-Modular Redundancy (TMR) to eliminate all SE

related errors at all test conditions.

Isotropic alpha particle tests were conducted using a 10 μCi Americium-241 button source at Vanderbilt University. The alpha source is 1cm$^2$ in size, and die size is 2mm x 2mm. The alpha source was placed approximately 1mm away from, and centered over, the die. The alpha emissivity at this distance has been determined to be approximately 1000 alpha/mm$^2$/s with a mean energy of approximately 5.4 MeV. Total fluence is approximately about 2.6x10$^8$ alpha/mm$^2$ for each experiment. Tests were performed for supply voltage values of 1.1 V, 0.95 V, 0.85 V, 0.8 V, 0.7 V, 0.6 V, and 0.55 V at room temperature. During this test, shift registers were clocked at 2.5 MHz frequency. In addition, SE response of test circuits was evaluated as a function of operating frequency up to 1300 MHz at room temperature, at 0.8 V, 0.7 V, and 0.6 V. All-0 test patterns were used for all the tests to eliminate errors due to ion hits on clock-tree.

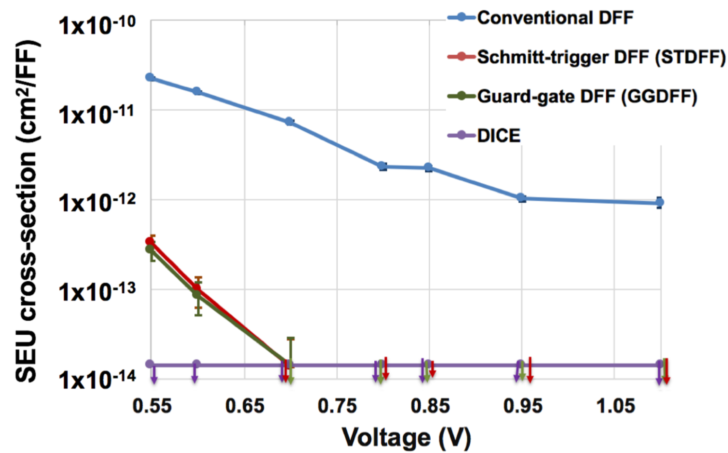



Figure V.5: Irradiation data plot of the SEU cross-section as a function of the supply voltage for conventional DFF, STDFF, GGDFF, and DICE FF at 2.5 MHz.

5.2.4 Irradiation Test Results

Fig. V.5 shows the irradiation results for all four FF designs as a function of supply voltage. The FinFET process shows a strong exponential increase in SEU cross-section with reduction in bias [63]. The data fit can be described by an exponential trend (as shown in Fig. V.5). The error bars for all experimental results are calculated (and included) as the standard error of measurement. Results indicate that the STFF and GGFF offers ~162X SEU cross-section improvement compared to conventional DFF at nominal voltage (0.8 V). As supply voltage is reduced, the differences between conventional DFF and STFF/GGFF also reduces to ~67X at 0.55 V. Fig. V.6 and Fig. V.7 show the irradiation results up to the operating frequency of 800 MHz at 0.6 V, 0.7 V, 0.8 V. SEU cross-section for all FF,

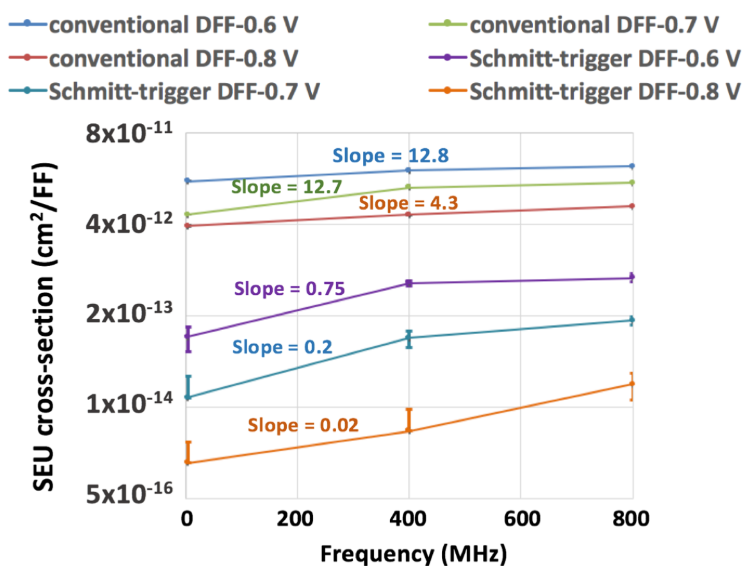



Figure V.6: Irradiation data plot of SEU the cross-section as a function of frequency for conventional DFF and STDFF at 0.6 V, 0.7 V, and 0.8 V. Please note the logarithmic scale for the Y-axis.

showing positive slope, indicate linearly increasing SEU cross-section with frequency.

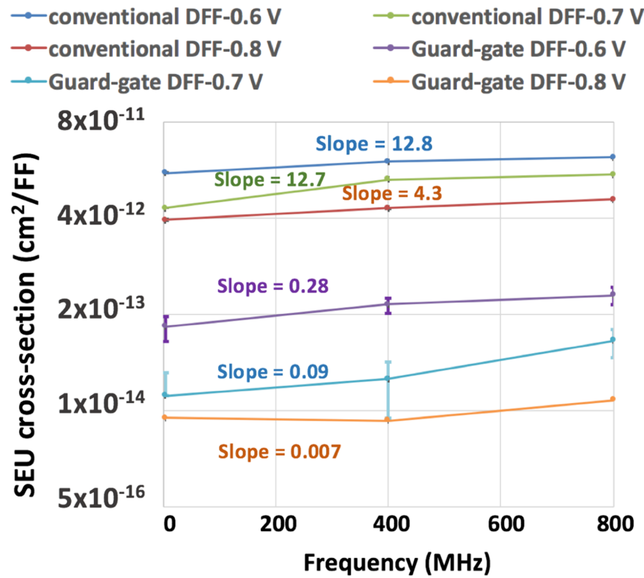



Figure V.7: Irradiation data plot of the cross-section as a function of frequency for conventional DFF and GGDFF at 0.6 V, 0.7 V, and 0.8 V. Please note the logarithmic scale for the Y-axis.

Transparent stage of the FF acts like a logic circuit at high frequency operations, resulting in an increase in SEU cross-section for FF designs [68]. Higher value of the slope suggests higher number of transistors capable of generating SET pulses. The small slope for Schmitt-trigger DFF is mainly due to the longer SET pulse-width requirement to cause an upset compared to those for DFF design. Because DICE-based FF designs have excellent SE performance, only a few errors (none or one error) were detected for alpha experiments.

Fig. V.8 shows the irradiation results for all four FF designs with different threshold votlage implants as a function of supply voltage at 2.5 MHz. The SER trends at different frequency for all four FF designs with different threshold votlage implants as a function of supply voltage are similar to Fig. V.8. Fig. V.9 shows the SER results for SVT FF designs as a function of frequency at 0.6 V, 0.7 V, 0.8 V, and 0.9 V. The SER trends at different

supply votlage for the other FF designs (LVT, iLVT, and uLVT) as a function of frequency

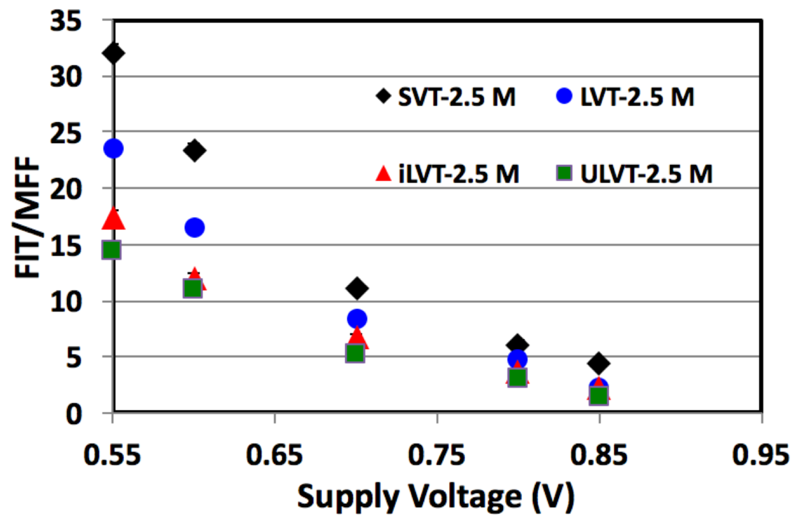



Figure V.8: Irradiation data plot of SER as a function of supply voltage for all four DFF designs at 2.5 MHz.

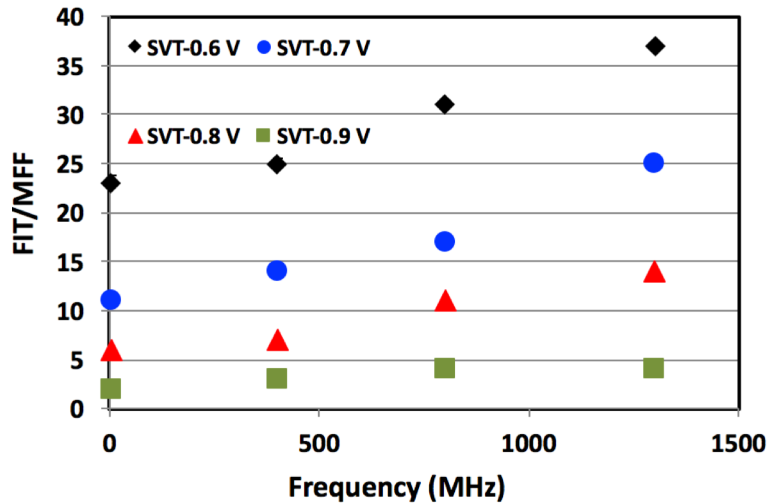



Figure V.9: Irradiation data plot of SER as a function of frequency for SVT DFF designs at 0.6 V, 0.7 V, 0.8 V, and 0.9 V.

are similar to Fig. V.9.

Even though most experiments for evaluating SEUs are carried out at room temperature, circuits operating in the field experience significantly different temperature. For the FinFET node, as reported earlier [102], the change in SE performance over a temperature

range of 27 °C to 125 °C is insignificant. FF designs fabricated at the 16-nm FinFET node may show only a small change in SE cross-section over the temperature range of intererst.

## 5.3 SE Analysis of Sense-Amplifier Based FF Design

### 5.3.1 Introduction

In recent years, the low-power, high-speed flip-flops based on differential inputs have been reported [103-105]. Differential FF cells enable 10's of GHz range of operation for current generation of technologies (28-nm bulk planar technology node supports 50 GHz range of operations). Unlike conventional FF designs that require a full logic swing on the input, differential FF designs minimally require a partial swing around the mid-point on the inputs, resulting in excellent power and speed characteristics [106]. These differential FF designs are fast becoming the design of choice for all communication networks. While SEU characterization and hardening techniques for conventional FF cells have been studied and published extensively, same is lacking for differential input FF cells. Because of the small voltage swings needed for differential operation, noise margins for these circuits are typically smaller than that for the conventional digital circuits. This makes them highly vulnerable to voltage perturbations caused by SEs. Therefore, investigation of SEU characterization and hardening techniques for differential FF designs are much needed by the semiconductor design community.

The sense-amplifier based flip-flop (SAFF), initially proposed in [105], [107], is one of the most effective differential FF available. High-speed operation can be achieved by the SAFF [105]. It can easily be integrated with conventional logic circuits and allows reduced voltage swings for input voltages and clock pulses [108]. Moreover, SAFF is characterized by a near-zero setup time, a reduced hold time, a low clock load, and true single-phase

operation. All of these characteristics have attracted most designers to using SAFF in their high speed designs. In this section, the differential FF designs of sense-amplifier based flip-flop (SAFF) fabricated at the 16-nm bulk FinFET CMOS technology node is investigated for SEU performance. Effects of temperature, operating frequency, and particle LET on SEU cross-section for the SAFF are evaluated for the first time. Results presented in this section will guide designers to optimize their differential FF designs to achieve desired SEU performance. The results can also use to create a model in chapter 6.

The rest of the section is organized as follows. In Section 5.3.2, three separate phases of operation during a clock cycle of the SAFF are classified and summarized. Details on the SE response of each of the phases are discussed and simulation results are presented, followed by the SE response of SAFF design as a function of temperature. Section 5.3.3 describes the test circuit. Experimental details including the experimental setups and test conditions are also presented. In Section 5.3.4, the experimental results of temperature, operating frequency, and particle LET on SEU cross-section for the SAFF are provided and analyzed.

#### 5.3.3 SE Vulnerability of SAFF Design

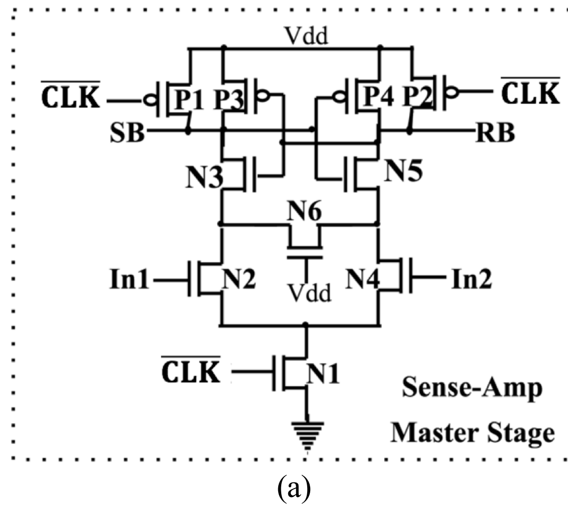
Conventional FF cells usually have a single-ended input with almost a full rail-to-rail swing required for proper operation. Some FF cells, such as conventional SR FF, do have two inputs, but both the inputs are still expected to provide rail-to-rail swing for all input signals. The rail-to-rail charging and discharging of nodal capacitances increases power dissipation and decreases operating speeds. Differential FF designs, on the other hand, only require a small differential signal between two inputs to sample data. The small differential signal requirement means the charging and discharging of input nodes (and the time required

to do so) is small, resulting in improved power and speed performance. Most differential FF designs employ a differential amplifier configuration in the master stage to amplify the differential signal and suppress common-mode signal between the two inputs, improving the noise performance. The conventional slave stage accepts the output from the amplification phase and maintains full-rail signals on the FF outputs. There are quite a few differential FF designs published in the literature, for example a dual rail pulse edge-triggered latch flip flop [1], a static differential flip flop (SDFF) [2], and a sense-amplifier based flip flop [3]. Out of all these designs, the sense-amplifier based flip-flop (SAFF) design shows the best performance for power, speed and area.

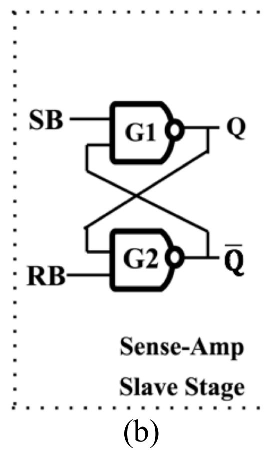
SAFF design consists of a fast differential sense-amplifier stage, followed by a slave latch, as shown in Fig. V.10. The sense-amplifier stage is very similar to the sense amplifiers used in memory ICs (hence the name). The SAFF design can achieve higher operating speed than other differential input FF designs, it is easier to integrate with conventional logic circuits, and allows reduced voltage swings on clock lines [105], [108]. Moreover, SAFF is characterized by a near-zero setup time, a very small hold time, a low clock load, and true single-phase operation as mentioned earlier. Since SAFF is designed to operate at reduced input voltage swings, the stage preceding SAFF operates at significantly reduced power compared to static CMOS design. Also, the SAFF is a true single-phase master latch, allowing a reduced swing on clock signal. This clock signal also drives a reduced number of transistors (3 transistors) compared to that for a conventional clocked-inverter DFF (8 transistors). These factors result in significantly reduced operating power requirements at high frequencies for SAFF design compared to conventional FF designs. The improvement in speed of the SAFF comes from the input side where the circuit generating the differential

signals does not have to swing rail-to-rail. Properly designed SAFF will yield a factor of more than two improvements in delay [108]. Because of the power and speed performance of SAFF design, most designers have migrated to using SAFF in their high speed designs.

The SAFF design is a mixed-signal circuit composed of a sense amplifier master stage followed by a NAND-based S-R slave latch. There are other design variations, but the main basis of the design remains the same. Fig. V.1 shows a conventional D-latch design (total 11 transistors). Fig. V.10 shows the SAFF design (total 18 transistors), the first stage is the sense amplifier [109], [110], the S-R latch operates as follows. Sample the data during clock LOW phase and hold the data in the slave stage during clock HIGH phase. For SAFF design, during clock LOW state, input data is amplified and stored in the SRAM-like circuit within the master stage. The operation of the SAFF can be divided into three separate phases of operation during a clock cycle. The first phase is data sampling. During the data sampling period, transistor N1 turns on (clock goes LOW) and the amplifier stage consisting of differential pair N2, N4 amplifies the differential input voltage between *In1* and *In2* to provide stable data on SB and RB nodes. During the second phases, stable data on SB and RB nodes are latched into the SRAM-like circuit formed by P3-N3 and P4-N5 transistors. This SRAM-like cell holds the data for the rest of the LOW clock cycle and resists further changes in the stored data (resulting in increased critical charge). SB and RB output from the master stage also transfer the stored data to slave stage during this second phase. When clock goes HIGH (third phase of operation), SB and RB node voltages are pulled HIGH by transistors P1 and P2 to provide HIGH input to the slave stage to hold the data until the next clock LOW transition [108]. In this section, the SE response of the SAFF are evaluated for all three phases of operation.




(a)




(b)

Figure V.10: Schematic of a SAFF with NAND SR slave latch. (a) Master stage of a SAFF. (b) Slave stage of a SAFF.

5.3.3.1 First Phase: Data Sampling Phase

During the first phase, only the differential amplifier is vulnerable to an incident ion. The incident ion may generate an SET pulse on the differential outputs of the amplifier (in SAFF case, they will be SB and RB in Fig. V.10). If an ion hit results in charge collection at the drain node of any the NMOS transistors (N2, N4, N3 or N5 in Fig. V.10), it will increase the current flowing through that transistor and may alter data on respective SB and

RB nodes. Depending on the SET pulse width, this will cause wrong data to be latched into the SRAM-like circuit. During this phase, the SAFF design is most vulnerable because a small change in any of the node voltages is amplified. Fig. V.11 shows the lowest critical

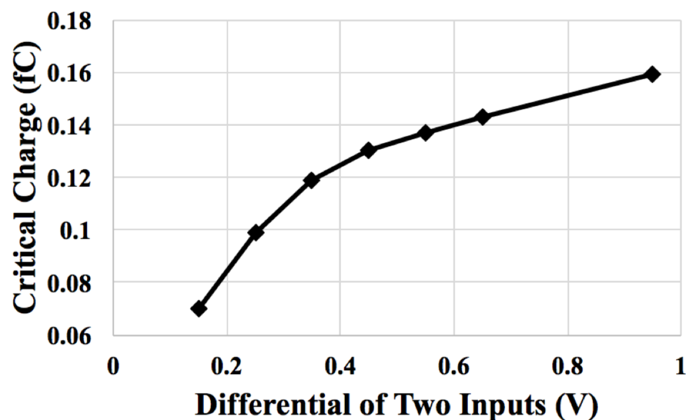



Figure V.11: Critical charge of the data sampling phase of SAFF as a function of differential input voltage.

charge requirement during this phase as a function of differential input voltage at 27 ˚C. Circuit simulations were used to extract the critical charge to upset the cell. All the simulation results were generated using the 16-nm models from the Arizona State University Predictive Technology Model (PTM) set and were carried out using the Cadence tool suite [73], [94]. Bias-dependent model was used to inject charge at every storage node [111]. Simulation results show that the time spent in this phase is inversely proportional to the differential input voltage, yielding better SEU performance for higher differential input voltage. However, higher differential input voltage significantly affects the performance (power and speed) of the preceding stage, necessitating a compromise between performance and SEU hardness.

#### 5.3.3.2 Second Phase: SRAM-Cell Like Phase & Third Phase: SR Latch Hold Data Phase

During the second phase (when SB and RB nodes have stable voltages and SRAM-like cell has latched the data), the latch functions similar to an SRAM cell. The transistors

that are most vulnerable to cause an upset is limited to those in OFF state of the SRAM structure (N3, P2 and P4 OR N5, P1 and P3 in Fig. V.10). Just like an SRAM cell, an ion hit on any of these transistors will cause the master stage to latch wrong data and pass it on to the slave stage. During the third phase (when clock is HIGH), the data is stored in the slave latch consisting of NAND gates with higher critical charge than SRAM-cell like circuit. During this phase, the PMOS transistors P1 and P2 pull SB and RB nodes high along with turning on N3 and N5 transistors in SRAM-like circuit. In the third phase, the SEU response of this phase is the same as the SEU response of NAND gate latch.

#### 5.3.3.3 Three Separate Phases of SAFF Comparison

Table V.II summaries the critical charge, $Q_{critical}$, as a function of differential input

Table V.II
Critical Charge for All Three Stages of Operation for The SAFF as A Function of Differential Input Voltage at Node *In1* and *In2*

| **Differential of two inputs (V)** | **0.35** | **0.45** | **0.55** | **0.65** | **0.95** | **1.1** |
|---|---|---|---|---|---|---|
| First phase $Q_{critical}$ (fC) | 0.12 | 0.13 | 0.14 | 0.14 | 0.16 | 0.17 |
| Second phase $Q_{critical}$ (fC) | 1.22 | 1.22 | 1.22 | 1.22 | 1.22 | 1.22 |
| Third phase $Q_{critical}$ (fC) | 2.59 | 2.59 | 2.59 | 2.59 | 2.59 | 2.59 |

voltage at all three phases of operation and 27 ˚C. The $Q_{critical}$ results shown in Table V.II are for the lowest values among all circuit nodes in the SAFF at each operation phase. The critical charge for slave stage (during the third phase) is independent of the differential input voltage. These results indicate that SAFF is most vulnerable during the first phase (data

sampling phase). $Q_{critical}$ of conventional DFF is usually the same whether data is currently being held in the master or slave stage. $Q_{critical}$ of conventional DFF is 0.807 fC at 0.95V. It is higher than the $Q_{critical}$ of SAFF first operation phase, but lower than both second phase and third phase of SAFF. Depending on the duration of the first phase for SAFF operation, SAFF may show higher (or lower) SEU cross-section than conventional DFF design. Since the SAFF is most vulnerable during first phase, reducing the time spent in first phase will reduce the overall SEU vulnerability of the latch. Previously published literature has detailed analysis about the electrical characterization (speed, delay, power, etc.) between DFF and SAFF for other technologies [105], [108]. Similar results were observed for the design analyzed in this paper.

#### 5.3.3.4 SEU Response of the SAFF as A Function of Temperature

Since SAFF designs will be used mostly for high frequency operations (and these operations usually dissipate a lot of power, resulting in higher operating temperatures), it is important to evaluate this design at high-frequency and high-temperature. Table V.III

Table V.III
Critical Charge for The SAFF as A Function of Temperature With *In1* = 0.95 V and *In2* = 0 V

| **Temperature (˚C)** | **27** | **75** | **110** |
|---|---|---|---|
| First phase $Q_{critical}$ (fC) | 0.16 | 0.17 | 0.17 |
| Second phase $Q_{critical}$ (fC) | 1.22 | 1.20 | 1.17 |
| Third phase $Q_{critical}$ (fC) | 2.59 | 2.6 | 2.58 |

summarizes the critical charge $Q_{critical}$ values as a function of temperature for the SAFF designs for the three operational phases discussed above. Since this is a differential design with very good common-mode rejection ratio (CMRR) properties, charge-sharing will actually enhance the SEU performance for the master stage for optimized layout. The $Q_{critical}$ results shown in Table V.III are for the lowest values among all circuit nodes in the FF during three phases. For the FinFET technology, as reported earlier [102], the change in SEU error rates (or cross-sections) over a temperature range of 27 ˚C to 110 ˚C is insignificant. This is mainly due to both SET pulse-width and feedback-loop delay show comparable changes with temperature over the range of interest. Since both these parameters affect SEU cross-sections in opposite manner (increasing SET pulse width increases SEU cross-section, increasing feedback-loop delay decreases SEU cross-section), similar changes in both parameters negates their effects on SEU cross-sections, resulting in minimal changes in SEU cross-section over temperature. Simulations results in Table V.III also indicate that 16-nm FinFET SAFF design may show only a small change in SEU error rates over the temperature range of interest.

### 5.3.4 Test IC Design and Experimental Details

The test IC to characterize SER performance for conventional DFF and SAFF designs were fabricated in a 16-nm bulk FinFET CMOS technology from a commercial foundry. The test circuits were implemented in CREST [64] configuration with an 8K-stage shift registers. All sub-circuits other than the shift register used triple-modular redundancy (TMR) to eliminate errors. The design allows for simultaneous at-speed testing of a variety of flip-flop types. On-chip error detection and an output serial interface were utilized to export the data (error counts) for each shift register. FPGA was utilized to generate control signals and

storage errors counts. An on-chip PLL (capable of running up to 3 GHz) was used to clock the shift register.

Alpha particle tests were conducted using a 10 μCi Americium-241 5.4 MeV alpha source (flux = 1000 particles/$mm^2$/sec) in air. The IC was subjected to a range of three temperatures tests at 0.95 V; 27 °C, 75 °C, and 110 °C at the die as measured using a hand-held laser-based temperature sensor. During all these tests, the differential input signal applied was at power rails and shift registers were clocked at 2.5 MHz frequency. In addition,

TABLE V.IV
16 MEV/ NUCLEON COCKTAIL COMPONENTS

| Ion | Energy (MeV) | LET (MeV-$cm^2$/mg) | $Range_{max}$ (μm) |
|---|---|---|---|
| $^{14}Ne^{+5}$ | 233.75 | 1.16 | 505.9 |
| $^{20}Ne^{+7}$ | 321.00 | 2.39 | 347.9 |
| $^{40}Ar^{+14}$ | 642.36 | 7.27 | 255.6 |
| $^{63}Cu^{+22}$ | 1007.34 | 16.53 | 190.3 |
| $^{78}Kr^{+27}$ | 1225.54 | 24.98 | 165.4 |
| $^{124}Xe^{+43}$ | 1954.71 | 49.29 | 147.9 |

SEU response of test circuits was evaluated as a function of operating frequency between 2.5 MHz and 1 GHz at 1.1 V and 27 °C. The supply voltage was increased to 1.1 V to ensure proper operation of all circuits (some of the circuits failed to operate at 0.95 V. The elevated supply voltage should not affect the trend in SEU frequency response of the SAFF). The input to the shift register was fixed at logic LOW level.

Heavy-ion experiments were conducted with ions with different LET values at Lawrence Berkeley National Laboratory (LBNL). The 16 MeV/nucleon cocktail was used for testing the ICs. The LET values of heavy-ions were between 0~60 MeV-cm$^2$/mg, as listed in Table V.IV. All heavy-ion tests were conducted in vacuum, at normal incidence, at room temperature, and at 0.95 V with total fluence running up to $5\times10^{7}$ /cm$^2$.

5.3.5 Experimental Results & Analyses

Test with alpha particles and heavy-ions have showed very little differences between input at logic level 0 and 1. Therefore, in this section only input at logic level 0 experimental results are presented. Also, due to the symmetric design of the SAFF, input at logic level 1 and 0 will have similar SEU cross-section.

5.3.5.1 Heavy-Ion Experimental Results

Fig. V.12 shows the heavy-ion results for conventional DFF and SAFF as a function of particle LET. For low LET particles (<20 MeV-cm$^2$/mg), the SAFF shows about better performance compared to conventional DFF design. The decrease in SAFF cross-section is approximately $1.22\times10^{-12}$ cm$^2$/FF. The differences in SEU cross-sections between SAFF and DFF for low-LET particles are similar to what was observed for alpha particle exposures. For high LET particles (>20 MeV-cm$^2$/mg), SAFF and DFF cross-sections are comparable. The decrease in SAFF SEU cross-section is approximately $4\times10^{-10}$ cm$^2$/FF. It must be kept in mind that percent difference between SAFF and DFF SEU cross-sections are higher for low-LET particles compared to high-LET particles. The observed experimental results can be explained by the critical charge of conventional DFF and SAFF as mentioned in Section 5.3.3. $Q_{critical}$ of conventional DFF is 0.807 fC at 0.95V. It is lower than both second phase (1.227 fC) and third phase of SAFF (2.591 fC), but higher than the $Q_{critical}$ of SAFF first

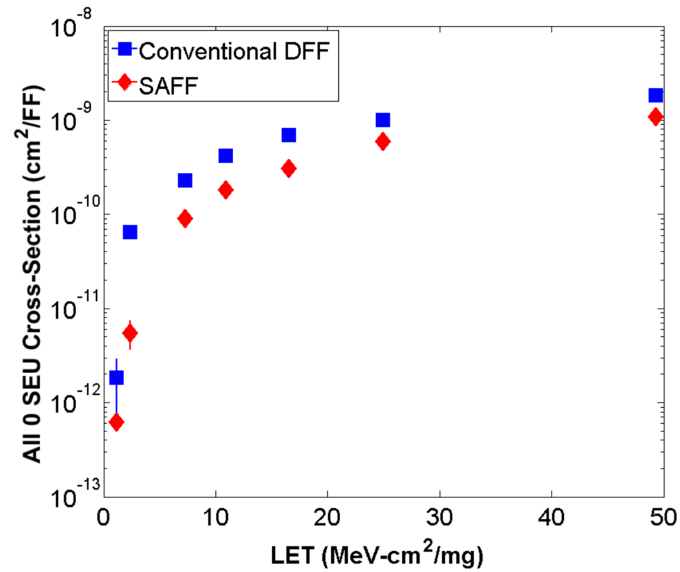



Figure V.12: SEU cross-section for heavy-ions as a function of particle LET for conventional DFF and SAFF at 0.95 V.

operation phase (0.159 fC). Even though the $Q_{critical}$ of conventional DFF is higher than that of the first operation phase of SAFF, DFF design will be vulnerable to LET particles throughout the clock period of 400 ns compare to the first operation phase of SAFF will be vulnerable only for a few 10's of pico-seconds when circuit operating at 2.5 MHz clock. Therefore, conventional DFF has higher SEU cross-section than SAFF design. From the heavy-ion experimental results, both circuits design has similar low threshold LETs. Even though, SAFF design second and third phase has higher critical charge than DFF design, SAFF design still has first phase critical charge less than conventional DFF.

5.3.5.2 Alpha Particle Experimental Results

For low LET particles, the SAFF design showed cross-section values that are much smaller than those for the conventional DFF design. Even though SAFF design has higher number of transistors than DFF design, it is vulnerable to low LET particles (such as alpha particles) only during a very short time duration (during the data sampling phase only). As

a result, the upset cross-section for SAFF ($1.57\times10^{-14}$ $cm^2$/FF) is orders of magnitude lower than that for conventional DFF ($1.42\times10^{-12}$ $cm^2$/FF) design when operating at 2.5 MHz clock. Previously published results have shown that the charge collected at the output node of a 16-nm bulk FinFET inverter for 1 MeV-$cm^2$/mg (particle LET) is 0.7 fC at 0.9 V [112]. Based on the 3D TCAD simulation results, it would imply that the alpha particles don't produce enough charge collection to exceed the critical charge during second and third operation phase (1.227 fC and 2.591 fC) in the SAFF, but yet may have just enough charge collection to exceed the critical charge in the conventional DFF (0.8 fC). Therefore, DFF design will be vulnerable to alpha particles throughout the clock period of 400 ns, but SAFF will be vulnerable only for a few 10's of pico-seconds. Fig. V.13 shows the cross-section for both the designs over the temperature range tested for alpha particle exposures. The error bars for all experimental results are calculated as the standard error of measurement. Some error bars are smaller than symbol. As expected, both the FF designs showed very little change in cross-section over this temperature range.

With the SAFF expected to operate at very high frequencies, it is important to evaluate their performance over frequency. Previously, it has been shown that the transparent stage of a FF acts like a logic circuit and ion hits on this stage will increase the overall SEU error rate as a function of frequency [68]. Fig. V.14 shows the SEU performance of conventional DFF and SAFF designs up to the operating frequency of 1 GHz for alpha particle exposures. Results show the SEU cross-section percentage ((1 GHz SEU cross-section – 2.5 MHz SEU cross-section) / 1 GHz SEU cross-section) increase of the SAFF is ~97% (up to 1 GHz) and that for the DFF is ~45% (up to 1 GHz) over static operation. The primary reason for this is that with increasing clock frequency, the operation time for the

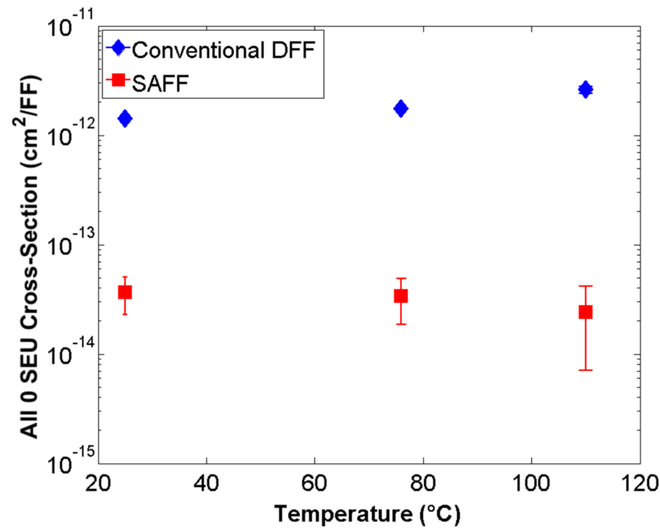



Figure V.13: SE cross-section for alpha particle exposures as a function of temperature for conventional DFF and SAFF at 0.95 V.

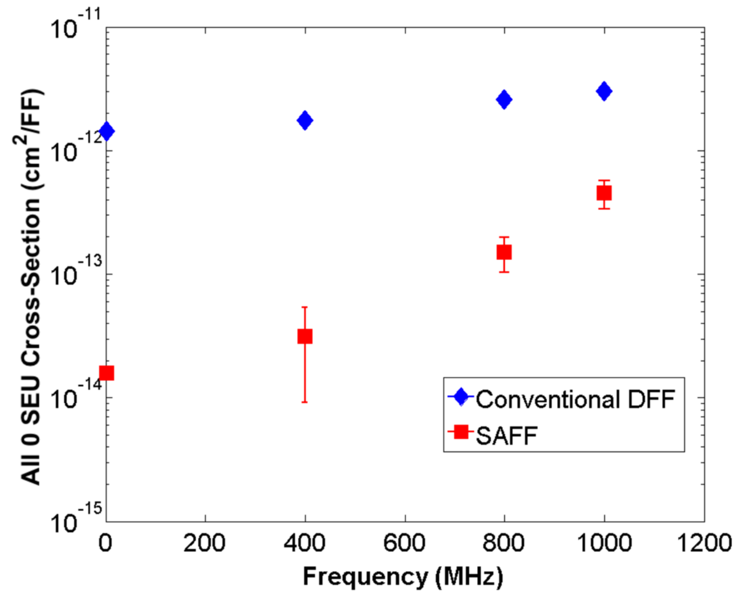



Figure V.14: SE cross-section for alpha particle exposures as a function of frequency for conventional DFF and SAFF at 1.1 V.

first phase (data sampling) of SAFF is a larger percentage of time per clock cycle. The period of the first phase depend on the size of transistors N2 and N4 (as shown in Fig. V.10). It does

not change with clock frequency. Therefore, with increasing clock frequency, the operation time for the first phase will become larger percentage of time per clock cycle. Additionally, with higher number of sensitive transistors in the SAFF design compared to that for DFF design results in increased vulnerability as operating frequency is increased. If the trend in operating frequency were to continue, the SAFF design will show higher SEU cross-section than DFF designs at 1.6 GHz and beyond. At such high operating frequencies, designers will have to carefully evaluate power and SEU trade offs to determine the best FF design for a given application. The trend in SEU cross-section shown in Fig. V.13 is for alpha particles.

### 5.3.6 Conclusions

In modern high-speed communication networks application, the state-of-the-art flip-flop designs have migrated to sense-amplifier based design. The experimental results presented in this work show SAFF SEU cross-sections as a function of temperature, operating frequency, and particle LET. Results indicate that even at high temperature condition, the SER for the 16-nm FinFET changes minimally. However, SAFF cross-section increases by ~97% when operating frequency is raised to 1 GHz. This is the first time differential FF have been analyzed for single-event performance at the 16-nm bulk FinFET technology node. Results presented in this work will help designers understand the SEU vulnerability of the SAFF and allow them to optimize their designs. Similar process can be carried out to characterize SEU of other differential FFs.

## 5.4 Summary

Different FF designs fabricated in a 16-nm bulk FinFET CMOS process are analyzed for SEU performance at different circuit parameters and control variables (different LET particles, operating frequency, temperature, and supply voltage). First time differential FF

have been detailed analyzed for SE performance at 16-nm bulk FinFET technology node. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints.

# CHAPTER VI

# AN EMPIRICAL MODEL BASED APPROACH TO EXPLORE DESIGN SPACE FOR SEQUENTIAL CIRCUITS

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H. Jiang, H. Zhang, B. Narasimham, L. W. Massengill, and B. L. Bhuva, "Designing soft-error-aware circuits with power and speed optimization," *IEEE IRPS*, March 2018.

Traditional SE analysis for sequential circuits usually compares SE performance for a given set of conditions (supply voltage, speed, temperature, particle LET, etc.). Designers need to identify the best performing (the lowest power requirement) FF designs and logic circuits for meeting SER specifications. Since design library dose not contain such comparative analysis (SER as a function of power), designers have to carry out additional analysis and test. This chapter explains a design methodology employing empirical models for identifying the optimum combinatoin of topology, supply voltage, and frequency for a given SEU cross-section specification. By analyzing the sequential circuits based on such an approach, desingers will have access to data that will allow them to optimize a circuit design along multiple dimensions (such as SER, power, and operating frequency). Such an analysis may also yield significant power savings while meeting SER and speed specifications.

## 6.1 Introduction

Integrated Circuit designers have a wide variety of flip-flop (FF) cells available in standard-cell libraries to achieve desired parameters. The choice depends on the desired timing properties, drive strength, area, power dissipation, functionality (e.g., clear- or preset-

FF; scannable or non-scannable), etc. Designers usually select a FF design based on power constraints then make changes in the design (transistor sizing) or operating parameters (supply voltage) to meet design specifications [113], [114]. Many design techniques have been introduced to optimize power consumption in production designs, such as creating multi-supply-voltage (MSV) designs [115], gate sizing [116], use of different threshold voltages [117], etc. Among these methodologies, use of different threshold voltages is one of the most effective methodologies in saving power consumption at a speed penalty. Usually, this process becomes an *ad-hoc* design process without any possibility of optimization or formalization.

Such changes to a design are usually accompanied by a performance degradation in one or more parameters. For example, reduction in power is usually accompanied by a decrease in speed and an increase in soft-error rates (SER). For advanced technologies, SER has been added as an additional parameter for such library cells (in addition to speed, power, and area), making the selection of FF and operating parameters very complex. In addition, aggressive technology trends (smaller feature sizes, lower supply voltage levels, higher operating frequencies, reduced logic depth) are projected to cause significant increase in the single-event (SE) error rate of combinational logic circuits. This means, unlike old technologies where FF SE upsets (SEU) dominated, logic SE upsets will contribute significantly to the overall single-event error rate (SER) of electronic systems [118-120]. In addition to meeting power and performance requirements, designers now have to spend a significant effort ensuring that logic circuit designs also meet target SER level. Similar to make the selection of FFs, designers usually select the logic design topology with the best power performance and then tweak the design to meet design specifications. Such an

approach does not allow for optimization or formalization of the design process. Since estimation of logic SER is a complex process involving multitude of variables (specially power and speed), it is important to develop a simple method for comparing different options that meet power, speed, area, and SE specifications as well.

Designers need to meet IC-level SER budget (along with power, speed, and area) for applications that require high reliability [121]. Therefore, designers usually have a target SER value (protection level) that needs to be met [122]. Although previous works have extensively studied the SER of latches, FFs, and logic circuits at different operating frequencies and supply voltages [123-125], the results are usually presented in a SER vs. Supply Voltage (or SER vs. Particle LET). Such data do allow designers to see if a design meets the specifications after the design process is completed. If designers were to follow an analytical process to evaluate different FF cells and logic circuits for suitability to given set of specifications at the onset of design process, optimum design parameters may be achieved. In this paper, different DFF designs and logic circuits are evaluated for a given SER specifications to identify optimum supply voltage and speed parameters. The main goal of the project is to allow designers to identify a multitude of FF designs (or logic circuits) and supply voltages that meet desired specifications at the start of the design process. Logic circuits fabricated at the 16-nm bulk FinFET CMOS technology node are used to evaluate the effectiveness of the proposed method. The proposed methodology is circuit and technology agnostic.

The remainder of this section is organized as follows: Section 6.2 introduces the proposed analytical method for designing power optimization FFs and logic circuits while considering area, speed, and SER specifications. In Section 6.3, the experimental details and

results are presented for evaluating the proposed analytical method. Section 6.4 discusses the evaluation results of the method. Finally, conclusions are drawn in Section 6.5.

## 6.2 Design Methodology and Empirical Models

The proposed model can be broken down into three major steps: Data Acquisition, Quantitative Modeling, and Assessment. For Data Acquisition step, basic parameters (area, delay, power, SE cross-section) of FFs and logic gates are obtained through experimentation or simulation for a given technology. In the Quantitative Modeling step, results from this step are used to extrapolate these parameters to all operational parameters. For the Assessment step, circuit designs chosen by a designer are evaluated to identify the optimum combination of design and operating conditions to meet specifications. Fig. VI.1 shows flowchart of the proposed model with the three major steps. The design optimization steps are discussed next.

For Data Acquisition step, operating parameters (area, speed, power as functions of supply voltage and temperature) can be obtained through simulations and may be available from the manufacturer. Obtaining SE related parameters (cross-section for transistors and/or basic gates) requires either TCAD simulations or a test IC [30-34]. During the Quantitative Modeling step, continuous functions for power and SER as a function of frequency and supply voltage are developed. For example, SER will increase linearly with operating frequency [68-71]. Therefore, the SER function can be modelled as

$$f_{@V} = \alpha_{@V} \cdot SER_{@V} + \beta_{@V} \quad \text{(VI.1)}$$

where $f_{@V}$ is the maximum operating frequency of the circuits at a certain supply voltage, $SER_{@V}$ is the FF SERs at that supply voltage, and $\alpha_{@V}$ and $\beta_{@V}$ are the fitting parameters based on the Data Acquisition step. Similarly, with reduction in bias, FFs show

an exponential increase in SER [128]. This can be modelled as

$$SER_{@f} = \delta_{@f} \cdot e^{\gamma_{@f} \cdot V_{@f}} \tag{VI.2}$$

where $SER_{@f}$ is SER at a certain frequency, $V_{@f}$ is the supply voltage to ensure operational frequency, $\gamma_{@f}$ and $\delta_{@f}$ are the fitting parameters based on the Data Acquisition

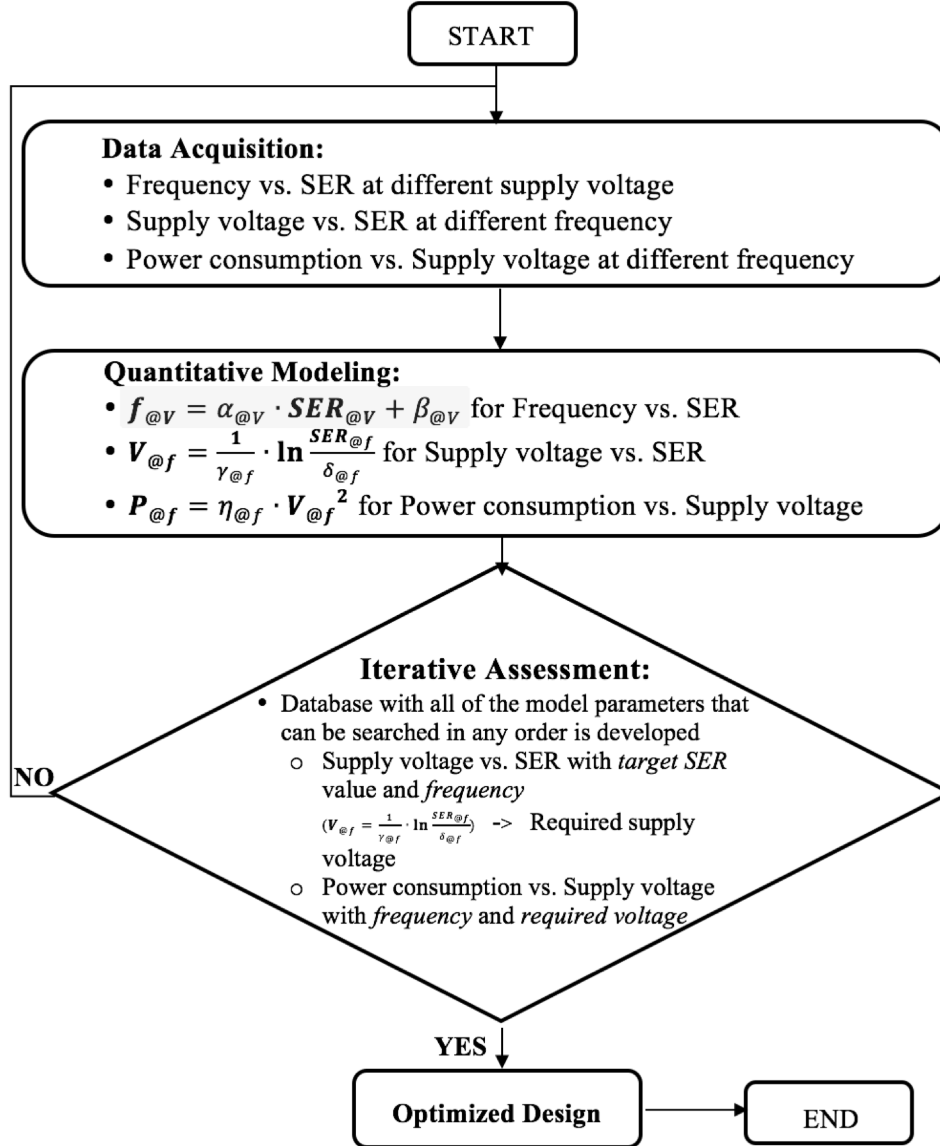



Figure VI.1: Flowchart of the proposed analytical method.

step. Eqn. VI.2 may be rewritten as

$$V_{@f} = \frac{1}{\gamma_{@f}} \cdot \ln \frac{SER_{@f}}{\delta_{@f}} \quad \text{(VI.3)}$$

Similarly, the power consumption of a circuit can be defined as [130]

$$P_{@f} = \eta_{@f} \cdot {V_{@f}}^2 \quad \text{(VI.4)}$$

where $P_{@f}$ is the power consumption of the circuits at a given frequency, $\eta_{@f}$ is the fitting parameters based on the Data Acquisition step. Results from Data Acquisition step are used to calculate all fitting parameters in (VI.1) – (VI.4). Such simple models for each library cell will allow estimation of necessary parameters (power, speed, and SER) quickly and easily during Assessment step. The accuracy of these empirical models depends on the precision of the measured data. Increasing the precision/resolution in Data Acquisition step may improve the accuracy of the fitting parameters in the Qualitative Modeling step.

During the Assessment step, different logic designs and FFs (chosen by a designer) are evaluated as a function of supply voltage (power), frequency, area, and SER with models developed in Quantitative Modeling step. Designers may specify a range of values for any parameter for optimization. For example, designers may decide to allow supply voltage to vary between (Nominal $V_{DD}$ ± 250 mV) and/or vary operating frequency between (nominal value ± 500 MHz). A multi-dimensional chart for all designs is then generated to allow designer to identify the best combination of design and operational parameters for a given set of specifications.

## 6.3 Experimental Details and Results

In this section, the experimental details and results are presented for evaluating the proposal model.

### 6.3.1 Circuit Description and Test Results

A test chip was designed in a 16-nm bulk FinFET CMOS technology generation with

8K-stage shift-register chains of conventional DFF and the three representative RHBD FF designs implemented as CREST-circuit [64]. In addition, all four available threshold ($V_T$) implants (SVT, LVT, iLVT, and uLVT) of conventional DFF were used for identical circuit schematic and layout ($V_T$: SVT>LVT>iLVT>uLVT). Error detection was carried out using on-chip circuits. Each FF shift register was clocked by an on-chip PLL that could operate at multi-GHz frequencies. The error detection and counter circuitry have the same voltage domain as the shift register chain. All support circuits used Triple-Modular Redundancy (TMR) to eliminate all SE related errors at all test conditions.

In addition, for the proposed model, one needs experimental data for SER of logic gates as a function of supply voltage and frequency to obtain fitting parameters in Eqn. VI.1-VI.3. To obtain these test results, a test circuit was designed based on the Combinational Circuit for Radiation Effects Self Test (C-CREST) [65]. Three C-CREST blocks were also designed using identical function but different topology. These logic functions are designated as Circuit-A, Circuit-B, and Circuit-C implementing a 4-bit comparator function. Test results from these blocks were used for evaluating the applicability and accuracy of the proposed methodology.

For different FF designs, alpha particle tests were conducted using a 10 μCi Americium-241 5.4 MeV alpha source (flux = 1000 particles/$mm^2$/s) in air. The gap between the alpha source and the die was less than 1 mm. Tests were performed for supply voltage values of 0.8 V, 0.7 V, and 0.6 V at room temperature. SER response of test circuits was evaluated as a function of operating frequency up to 1300 MHz at room temperature. All-0 test patterns were used for all the tests to eliminate errors due to ion hits on clock-tree. For combinational logic circuits, Heavy ion tests were carried out at LBNL with 10 MeV/nucleon

cocktail in vacuum, at normal incidence, and at room temperature. Tests were carried out over a frequency range from 2.5 MHz to 800 MHz at 0.6 V, 0.7 V, and 0.8 V of supply voltage. The results presented below are only for Xe with LET = 58.78 MeV-cm$^2$/mg. Error bars for all experimental results were calculated (and included) as the standard error of measurement.

Test results of FF designs are presented in Chapter 5. Power for these FF cells were simulated using Cadence tool suite under nominal corner [73], [101]. In this work, clk-to-q delay for all FF designs are assumed to meet the operating frequency in the early design phase. Since the delay are evaluated in the logic synthesis step (static timing analysis) for EDA tools [131]. The power simulation for the FFs were performed at 0.8 V, 0.7 V, and 0.6 V with 0% data activity. Data activity rate represents the average number of the output transitions per clock cycle [101]. All the power simulation results for FFs in this paper are average power over five clock cycles. Simulation methods as mentioned above can be used for different output load and slew conditions. Only one situation is presented in this chapter for demonstrating the proposed model. A model for predicting SE cross-section for any arbitrary circuit developed in chapter 4 has been used to estimate the three logic circuits (Circuit A, B, and C) in this chapter. Power requirements for these logic circuits were estimated based on probability model [132].

### 6.3.2 Proposed Model for FF Designs

#### 6.3.2.1 Quantitative Modeling Results

Fitting parameters ($\alpha_{@V}$, $\beta_{@V}$, $\gamma_{@f}$ , $\delta_{@f}$, and $\eta_{@f}$) for all four different $V_T$ implants of conventional DFF and three RHBD FF designs (as mentioned in chapter 5) were obtained from the experimental results based on the flowchart as shown in Fig. VI.1. Table VI.I and

Table VI.I Fitting parameters ($\alpha_{@V}$, $\beta_{@V}$, $\gamma_{@f}$ , $\delta_{@f}$, and $\eta_{@f}$) for DFF design with SVT, LVT, iLVT, and uLVT implants

| Parameters | | 0.8 V | 0.7 V | 0.6 V |
|---|---|---|---|---|
| $\alpha$ | SVT | 147.4 | 90.2 | 86.5 |
| | LVT | 138.9 | 87 | 68.9 |
| | iLVT | 136.7 | 87.4 | 59.7 |
| | uLVT | 161.2 | 94.5 | 61.2 |
| $\beta$ | SVT | -774.2 | -885.4 | -1884.1 |
| | LVT | -589.7 | -694.2 | -1148 |
| | iLVT | -502.2 | -620.2 | -807.2 |
| | uLVT | -422 | -484.6 | -751 |

| Parameters | | 2.5 M | 400 M | 800 M | 1300 M |
|---|---|---|---|---|---|
| $\delta$ | SVT | 1267.5 | 1160.6 | 675 | 704.7 |
| | LVT | 505.2 | 1340.1 | 583.4 | 626.8 |
| | iLVT | 325.12 | 1304.8 | 692.7 | 489.5 |
| | uLVT | 517.74 | 1543.2 | 1748.3 | 617.7 |
| $\gamma$ | SVT | -6.7 | -6.4 | -5.2 | -4.9 |
| | LVT | -5.8 | -6.7 | -5 | -4.8 |
| | iLVT | -5.5 | -6.7 | -5.3 | -4.5 |
| | uLVT | -6.5 | -7.2 | -6.9 | -5 |
| $\eta$ | SVT | 1.6 | 250.6 | 501.2 | 814.5 |
| | LVT | 1.6 | 260.2 | 520.4 | 845.7 |
| | iLVT | 1.7 | 267.6 | 535.3 | 869.8 |
| | uLVT | 1.8 | 283.5 | 566.9 | 921.3 |

Table VI.II list these parameters for different supply voltages and operating frequencies for all four DFF designs with different threshold voltage implants and three RHBD FF designs. Voltage and frequency test/simulation ranges can be derived from the circuit design

Table VI.II Fitting parameters ($\alpha_{@V}$, $\beta_{@V}$, $\gamma_{@f}$ , $\delta_{@f}$, and $\eta_{@f}$) for conventional DFF design and three RHBD FF Designs with LVT implant

| Parameters | | 0.8 V | 0.7 V | 0.6 V |
|---|---|---|---|---|
| $\alpha$ | DFF | $2.34\text{x}10^{14}$ | $7.87\text{x}10^{13}$ | $7.81\text{x}10^{13}$ |
| | STDFF | $4\text{x}10^{16}$ | $5.1\text{x}10^{15}$ | $1.34\text{x}10^{15}$ |
| | GGDFF | $1.35\text{x}10^{17}$ | $1.1\text{x}10^{16}$ | $3.5\text{x}10^{15}$ |
| | DICE | $1.35\text{x}10^{17}$ | $1.28\text{x}10^{17}$ | $1.24\text{x}10^{17}$ |
| $\beta$ | DFF | -885.2 | -503.1 | -1320.3 |
| | STDFF | 29.7 | -75 | -215.8 |
| | GGDFF | -909.6 | -82.1 | -505.3 |
| | DICE | -909.6 | -1964.3 | -2111.8 |

| Parameters | | 2.5 M | 400 M | 800 M |
|---|---|---|---|---|
| $\delta$ | DFF | $6\text{x}10^{-10}$ | $1.87\text{x}10^{-9}$ | $1.4\text{x}10^{-9}$ |
| | STDFF | $3.12\text{x}10^{-8}$ | $1.18\text{x}10^{-7}$ | $2.53\text{x}10^{-7}$ |
| | GGDFF | $1\text{x}10^{-8}$ | $1.18\text{x}10^{-8}$ | $7.15\text{x}10^{-9}$ |
| | DICE | $3.22\text{x}10^{-13}$ | $1.44\text{x}10^{-13}$ | $1.59\text{x}10^{-13}$ |
| $\gamma$ | DFF | -6.3 | -7.2 | -6.5 |
| | STDFF | -21 | -23.6 | -24.5 |
| | GGDFF | -19.36 | -18.1 | -16.4 |
| | DICE | -3.63 | -4.52 | -3.16 |
| $\eta$ | DFF | 101.32 | 538.5 | 963.39 |
| | STDFF | 159.57 | 632.06 | 1080.6 |
| | GGDFF | 140.52 | 822.96 | 1481.4 |
| | DICE | 200.03 | 1087.4 | 1950.8 |

specifications for improving accuracy. In this chapter, the voltages (0.8 V, 0.7 V, and 0.6 V) and the frequencies (2.5 MHz, 400 MHz, 800 MHz, and 1300 MHz) are used only for demonstrating the proposed model.

6.3.2.2 Discussion

The main objective of this project is to identify performance of each FF design for a given set of specifications. Table V.III and Table V.IV derived from the proposed model (as

Table VI.III Four different design specifications with the minimized power consumption design after applying the proposed analytical method

| Design Specifications | Case 1 | Case 2 | Case 3 | Case 4 |
|---|---|---|---|---|
| Given SER | 10 FIT/MFF | 10 FIT/MFF | 50 FIT/MFF | 50 FIT/MFF |
| Frequency | 2.5 M | 800 M | 1300 M | 5000 M |
| Best Case | uLVT @ 0.6 V | uLVT @ 0.75 V | iLVT @ 0.5 V | uLVT @ 0.69 V |
| Worst Case | SVT @ 0.72 V | LVT @ 0.8 V | SVT @ 0.54 V | iLVT @ 0.75 V |
| Power Difference | 20% | 8% | 6% | 11% |

Table VI.IV Four different design specifications with the minimized power consumption design after applying the proposed analytical method

| Design Specifications | Case 1 | Case 2 | Case 3 |
|---|---|---|---|
| Given SER | $9.1 \times 10^{-13}$ $cm^2$/FF | $3 \times 10^{-11}$ $cm^2$/FF | $9 \times 10^{-11}$ $cm^2$/FF |
| Frequency | 400 M | 800 M | 800 M |
| Best Case | DICE @ 0.3 V | STDFF @ 0.35 V | GGDFF @ 0.3 V |
| Worst Case | DFF @ 1 V | DFF @ 0.6 V | DFF @ 0.4 V |
| Power Difference | 84% | 56% | 38% |

shown in Fig. VI.1) shows results when the designer chooses to select SER and operating

frequency as the primary parameters. For a given SER value and operating frequency, the model identifies all possible FF designs and associated supply voltages to meet these specifications. Associate supply voltage can be used for the whole chip with the best FF design type to achieve low power consumption. By replacing a small fraction of the FFs with the best FF design to obtain better power performance might work as well. However, the power penalty due to increases different power domains need to be considered.

For example, for SER of 10 FIT/MFF and operating frequency of 800 MHz, the best choice for the designer is to use uLVT DFF at 0.75 V. This option yields 8% power savings over SVT DFF design operating at 0.8 V. Fig. VI.2 and Fig. VI.3 shows the model for SVT, LVT, iLVT, and ULVT DFF designs for a 3-D plot of power, SER, and frequency. Having access to such a model, and the resultant database, will allow designers to meet the specifications from the onset of the design process. A FOM can be used to help designers to make informed decisions on meeting power, speed, and SE specifications. A FOM is defined as the inverse of the product of power and SE cross-section (PCSP-1). Since minimization of power and SE cross-section is desirable, a lower PCSP value and thus a higher FOM value can be considered to be an indicator of an optimized design. By applying the proposed model before tradiational logic synthesis step, a rank of FF designs for the optimized design specifications can be obtained. During logic synthesis, the FF designs can be evaluated sequencely based on the rank to get the optimized design with respect to all target specifications (power, speed, SER, and area).

Desginers usually employ selective hardening to a design's most error-sensitive sub-circuits to meet SER specifications [133],[134]. For selective hardening techniques, a circuit is designed to meet a given set of performance specifications (power, speed, and area)

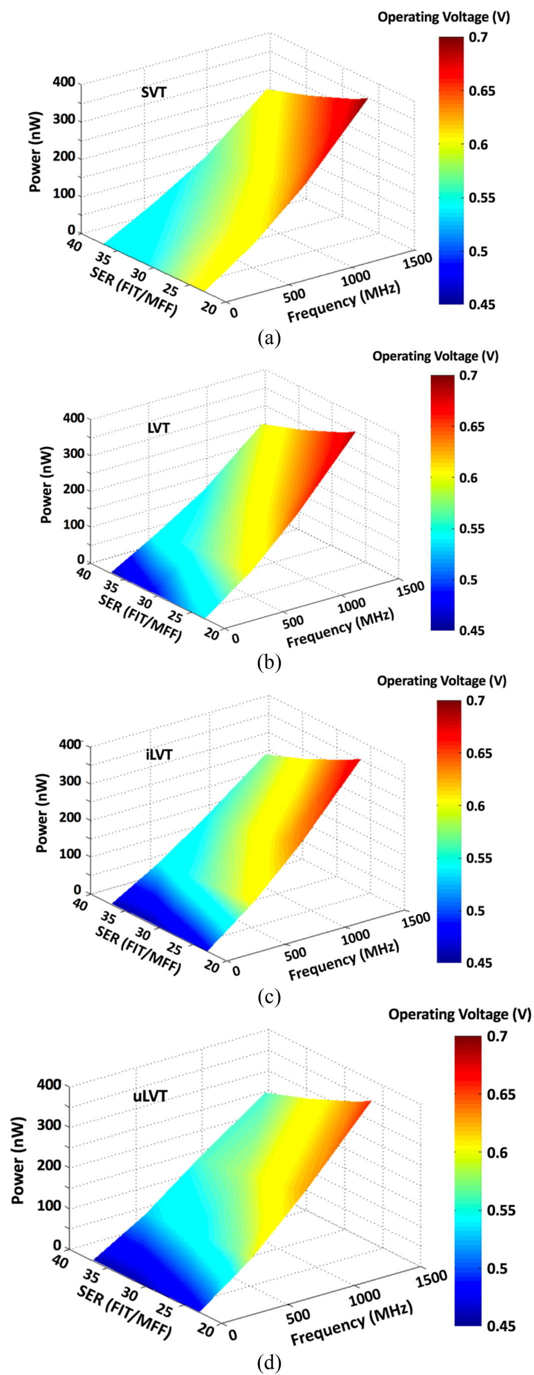
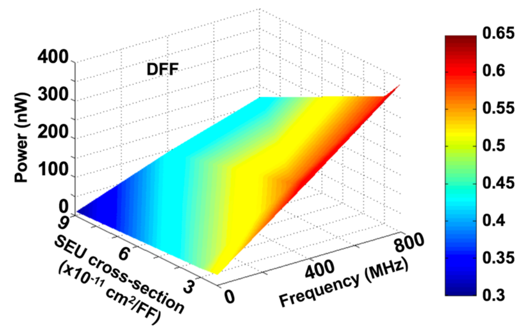
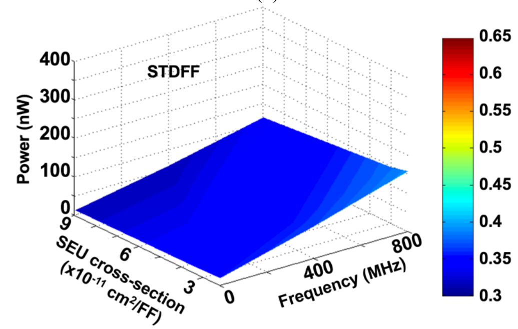


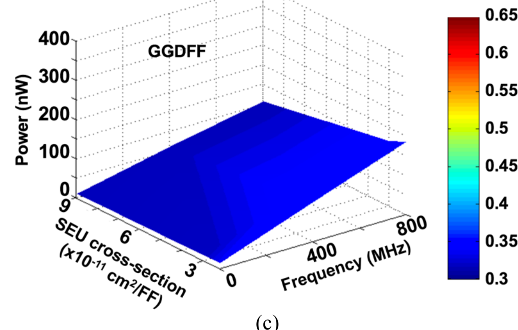

Figure VI.2: Data set with four numerical dimensions for the DFF (SER, frequency, power, and voltage) are generated by using the proposed analytical method (a) DFF design with SVT options; (b) DFF design with LVT options; (c) DFF design with LVT options; (d) DFF design with LVT options.



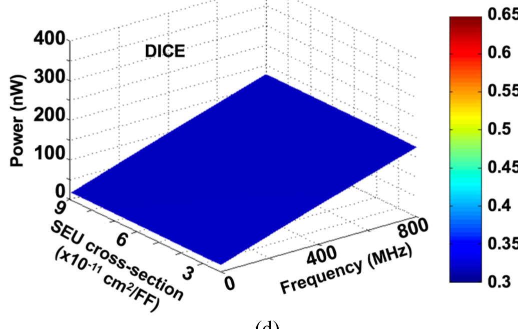

(a)




(b)




(c)




(d)

Figure VI.3: Data set with four numerical dimensions for the DFF and three RHBD FF designs (SER, frequency, power, and voltage) are generated by using the proposed analytical method (a) DFF; (b) STDFF; (c) GGDFF; (d) DICE.

without considering SER. Then, critical FFs are selectively hardened to reduce SER to a given specification. However, for the proposed model, SER is considered in the early design process along with other design parameters (power, speed, and area). Such an approach, in theory, will result in optimum operating conditions while meeting all specifications. It is possible that the voltage domain of sub-circuits may be different between the proposed model and the selective hardening technique, resulting in different power and speed requirements. FFs used in the circuits for both the methods may also be different. Depending on the circuit design technique used, proposed model can help designers meet SER requirements while having lower power consumption than the selective hardening techniques.

### 6.3.3 Proposed Model for Logic Circuits

#### 6.3.3.1 Quantitative Modeling and Assessment Step

Based on experimental results, fitting parameters ($\alpha_{@V}$, $\beta_{@V}$, $\gamma_{@f}$ , $\delta_{@f}$, and $\eta_{@f}$) for Eqn. VI.1-VI.3 were obtained for Circuit-A, Circuit-B, and Circuit-C. These parameters as a function of supply voltage (0.8 V, 0.7 V, and 0.6 V) and frequency (500 MHz, 800 MHz, and 1300 MHz) are listed in Table VI.V and Table VI.VI.

Table VI.V Fitting parameters ($\alpha_{@V}$ and $\beta_{@V}$) for three logic circuits

| **Parameters** | 0.8 V | | 0.7 V | | 0.6 V | |
|---|---|---|---|---|---|---|
| | $\boldsymbol{\alpha}$ | $\boldsymbol{\beta}$ | $\boldsymbol{\alpha}$ | $\boldsymbol{\beta}$ | $\boldsymbol{\alpha}$ | $\boldsymbol{\beta}$ |
| **LC-1** | $2 \times 10^{12}$ | 60 | $1.1 \times 10^{12}$ | -15.8 | $6.2 \times 10^{11}$ | 8.83 |
| **LC-2** | $2.5 \times 10^{12}$ | -25 | $1.1 \times 10^{12}$ | 31.3 | $6.9 \times 10^{11}$ | 14.6 |
| **LC-3** | $1.2 \times 10^{12}$ | 4.4 | $8.3 \times 10^{11}$ | 5 | $3 \times 10^{11}$ | -2 |

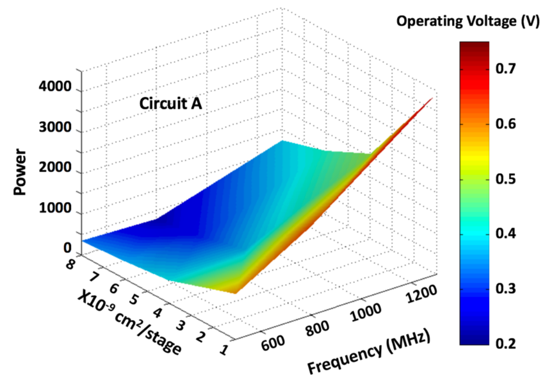
Once the fitting parameters were available, Assessment step was performed for Circuit-A, Circuit-B, and Circuit-C. Table VI.VII lists a few examples of design and

Table VI.VI Fitting parameters ($\gamma_{@f}$ , $\delta_{@f}$, and $\eta_{@f}$) for three logic circuits

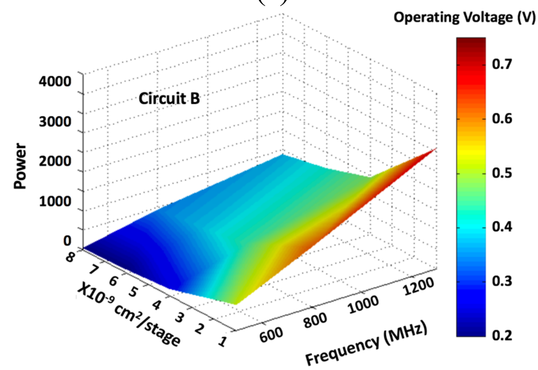
| Parameters | | 500 M | 800 M | 1300 M |
|---|---|---|---|---|
| $\delta$ | LC-1 | $1.21x10^{-7}$ | $2.64x10^{-8}$ | $8.13x10^{-8}$ |
| | LC-2 | $1.64x10^{-8}$ | $9.56x10^{-8}$ | $8.47x10^{-8}$ |
| | LC-3 | $8.53x10^{-8}$ | $1.32x10^{-7}$ | $2.05x10^{-7}$ |
| $\gamma$ | LC-1 | -8.3 | -5.1 | -6.1 |
| | LC-2 | -5.4 | -7.2 | -6.3 |
| | LC-3 | -6.8 | -6.7 | -6.7 |
| $\eta$ | LC-1 | 3281 | 5250 | 8531.3 |
| | LC-2 | 2387.7 | 3820 | 6208 |
| | LC-3 | 1968.8 | 3150 | 5118.8 |

operating conditions for a given SE cross-section target. Column for Case 1 shows that it is possible to achieve 55% savings in power if SE cross-section target is $2x10^{9}$ $cm^{-2}$ and operating frequency is 500 MHz.

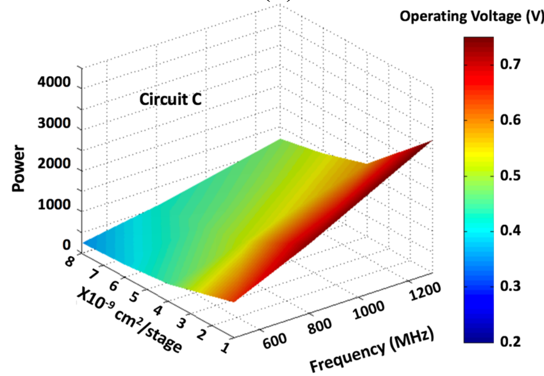
Using the proposed analytical method, the full data set of the four numerical dimensions (SER/frequency/power/voltage) for Circuit A, B, and C are shown in Fig. VI.4. Such a database can be used to easily identify the range of parameters that can satisfy the given design specifications. Similar to evaluate the FF designs, the FOM can be also used to help designers to make informed decisions on meeting power, speed, and SE specifications for logic circuits. Higher FOM value can be considered to be an indicator of an optimized design. This will allow designer to identify optimum design for a given set of specifications. Both power and SE cross-section are strongly dependent on supply voltage, frequency, nodal capacitance, etc. Therefore, the relationship between power and SE cross-section for different circuit designs as a function of different control/design variables can not be easily




(a)

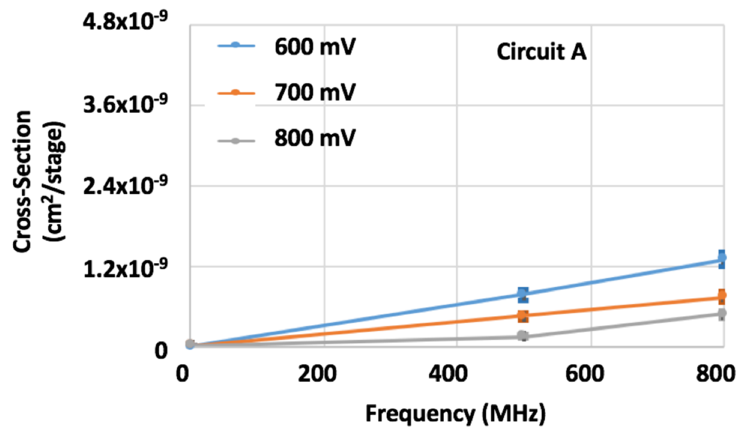



(b)

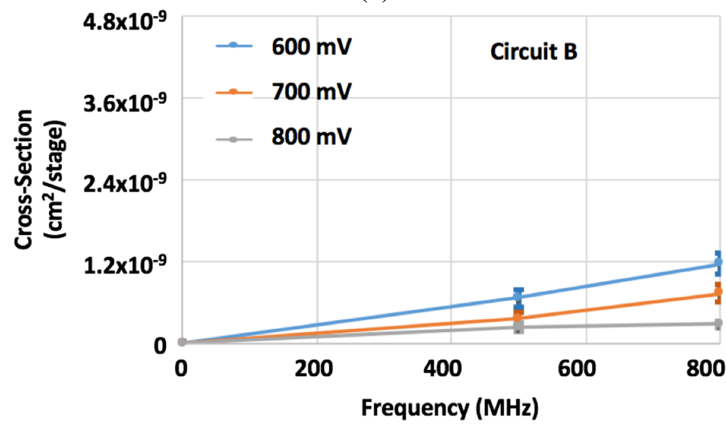



(c)

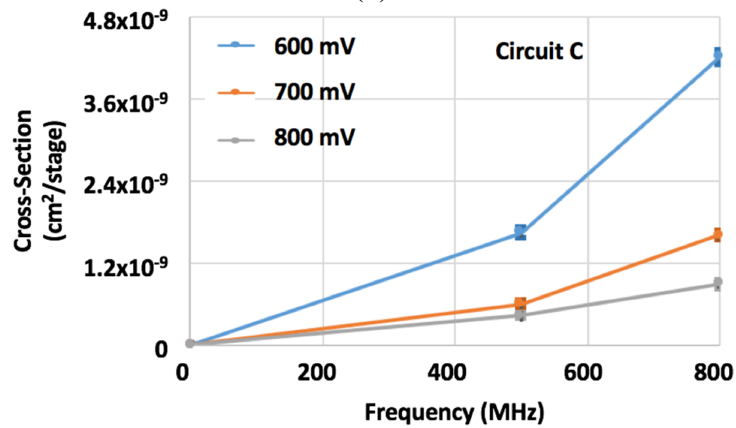
Figure VI.4: Data set with four numerical dimensions for the logic circuit (SE cross-section, frequency, power, and voltage) are generated by using the proposed model (a) Circuit A; (b) Circuit B; (c) Circuit C.




(a)

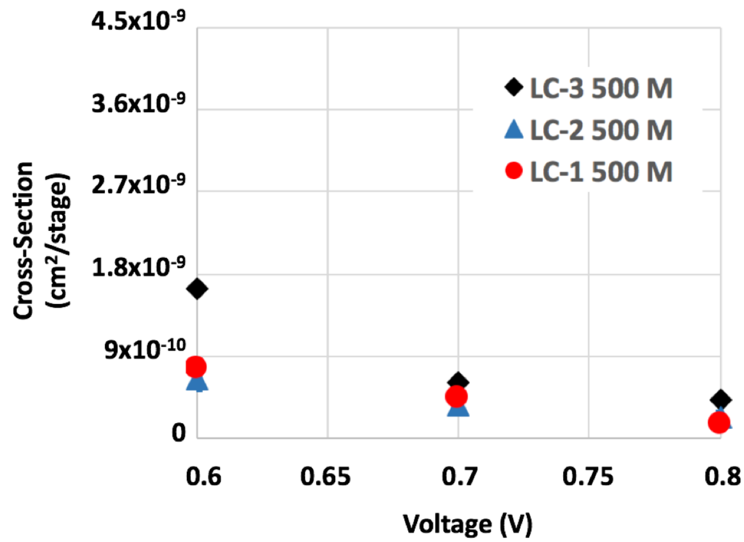



(b)

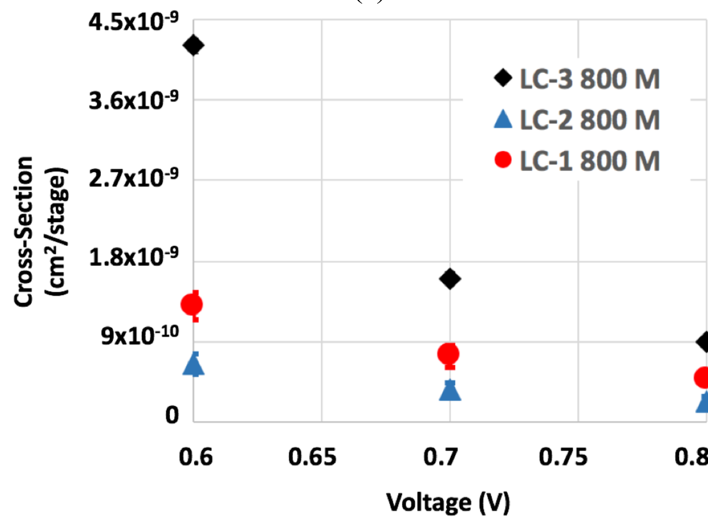



(c)

Figure VI.5: Irradiation data plot of SE cross-section as a function of frequency for (a) Circuit A; (b) Circuit B; (c) Circuit C logic circuits at 600 mV, 700 mV, and 800 mV.




(a)




(b)

Figure VI.6: Irradiation data plot of SE cross-section as a function of supply voltage for (a) Circuit A; (b) Circuit B; (c) Circuit C logic circuits at 500 MHz and 800 MHz.

represented by a simple equation. In order to use a simple equation to make informed decisions on satisfy the given design specifications, in this work $PCSP^{-1}$ (FOM) is used after the proposed framework (three major steps: Data Acquisition, Quantitative Modeling, and Assessment). Since the proposed framework includes the relationship between power and

SE cross-section as a function of different control/design variables, use $PCSP^{-1}$ (FOM) after the framework can help designers to make informed decisions on meeting power, speed, and SE specifications for different circuit designs.

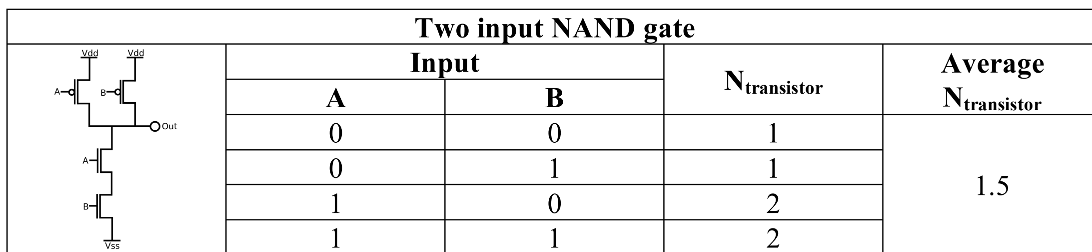
Fig. VI.5 shows the experimental SE cross-section results for Circuit A, Circuit B, and Circuit C logic designs as a function of frequency at 0.6 V, 0.7 V, and 0.8 V. Fig. VI.6 shows the irradiation results for Circuit A, Circuit B, and Circuit C circuits as a function of supply voltage at 500 MHz and 800 MHz. These experimental results are within 1.2X average error when compared to the predicted results in Fig. VI.4.

Proposed method can be used at the sub-circuit granularity level (though nothing prevents designers to use it at the IC level). Granularity finer than sub-circuit module may increase the power routing complexity. Designers should have the freedom to define the level of sub-circuit (availability of different supply voltages may dictate the sub-circuit size). Depending on the design, each sub-circuit module may have different supply voltages. If all the FF on the sub-circuit are replaced by the best combination of FF design and associated supply voltage, optimum power and SER conditions are achieved (but not necessarily the operating frequency). Usually, designers may prefer to use different combinations of FF design and supply voltages for different sub-circuits to meet target specifications (power, speed, area, and SER).

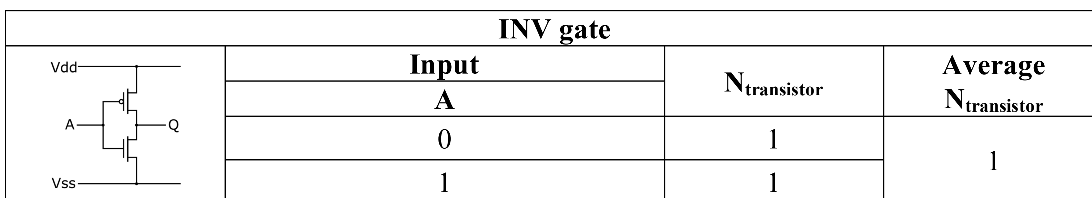
#### 6.3.3.2 Discussion

Analysis and modeling the effect of transient faults in logic circuits has been done intensively [5-12]. In order to find whether the fault propagates ($N_{transistor}$), inject the fault into the given node of the circuit and simulate the circuit for different input vectors is one obvious approach [11], [12]. However, for larger circuits and larger number of inputs, this

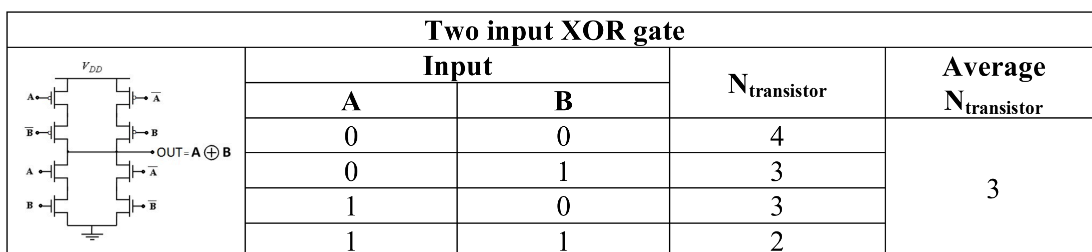
Table VI.VII Average number of $N_{transistor}$ for different logic gates



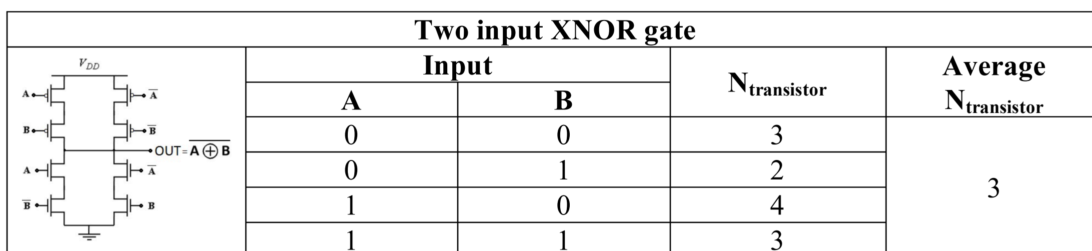

| Two input NAND gate | | | |
|---|---|---|---|
| Input | | $N_{transistor}$ | Average $N_{transistor}$ |
| A | B | | |
| 0 | 0 | 1 | 1.5 |
| 0 | 1 | 1 | |
| 1 | 0 | 2 | |
| 1 | 1 | 2 | |



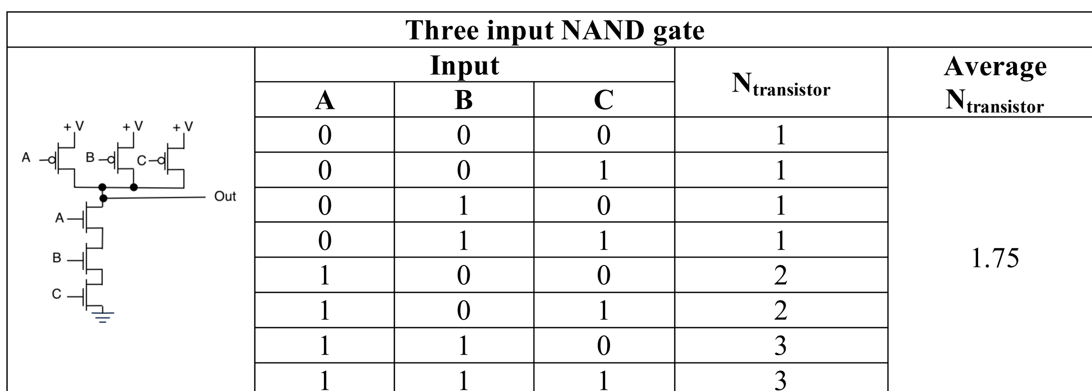

| INV gate | | |
|---|---|---|
| Input | $N_{transistor}$ | Average $N_{transistor}$ |
| A | | |
| 0 | 1 | 1 |
| 1 | 1 | |




| Two input XOR gate | | | |
|---|---|---|---|
| Input | | $N_{transistor}$ | Average $N_{transistor}$ |
| A | B | | |
| 0 | 0 | 4 | 3 |
| 0 | 1 | 3 | |
| 1 | 0 | 3 | |
| 1 | 1 | 2 | |

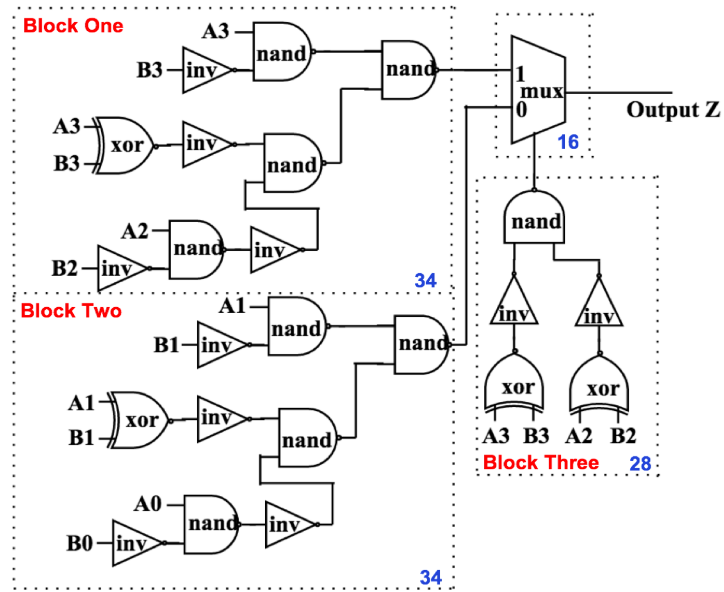



| Two input XNOR gate | | | |
|---|---|---|---|
| Input | | $N_{transistor}$ | Average $N_{transistor}$ |
| A | B | | |
| 0 | 0 | 3 | 3 |
| 0 | 1 | 2 | |
| 1 | 0 | 4 | |
| 1 | 1 | 3 | |

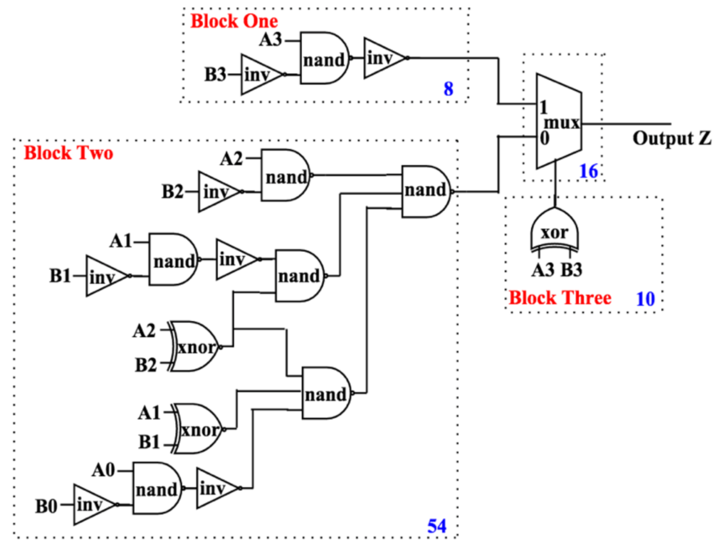



| Three input NAND gate | | | | |
|---|---|---|---|---|
| Input | | | $N_{transistor}$ | Average $N_{transistor}$ |
| A | B | C | | |
| 0 | 0 | 0 | 1 | 1.75 |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 2 | |
| 1 | 0 | 1 | 2 | |
| 1 | 1 | 0 | 3 | |
| 1 | 1 | 1 | 3 | |

approach becomes intractable. Symbolic, mathematical, and probabilities models have been




(a)




(b)

Fig. 7. Circuit design of second hardened four-bit comparator. (a) CMP1, It consists a total of 112 transistors. The number at right bottom corner of each block is the total number of transistors in each block. (b) CMP2, It consists a total of 88 transistors. The number at right bottom corner of each block is the total number of transistors in each block.

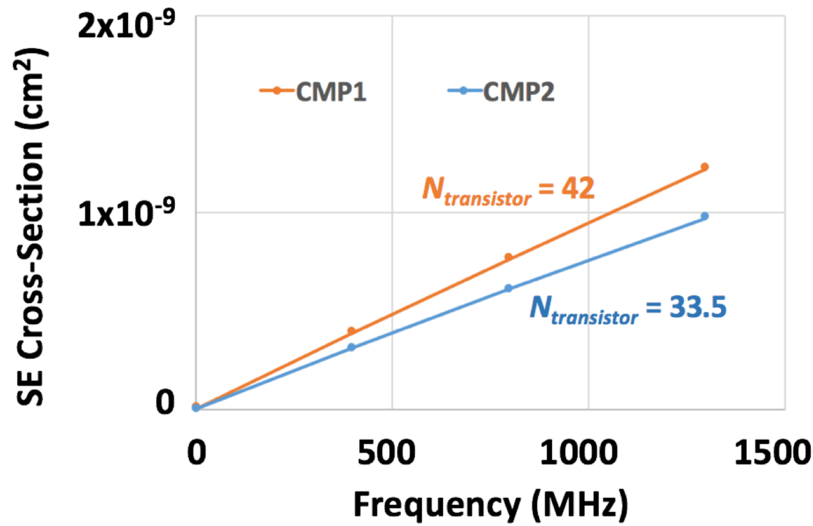



Fig. VI.8. Estimated SE cross-section of CMP1 and CMP2 by using the average number of $N_{transistor}$ with the empirical model that developed in chapter 4.

developed to speed up the evaluation of $N_{transistor}$ of logic circuits [8], [9], [13]. In this work, average number of the $N_{transistor}$ for different input conditions of logic circuits have been used to estimate the SE cross-section of logic circuits. Table VI.VII shows the average number of $N_{transistor}$ for different logic gates (e.g. inverter, NAND, XOR, etc.) with different input conditions. The average number of $N_{transistor}$ can be used to estimate different logic circuits with the empirical model that developed in chapter 4. Fig. VI.8 shows the estimated SE cross-section of two four-bit comparators (as shown in Fig. VI.7) by using the average number of $N_{transistor}$ with the empirical model that developed in chapter 4.

## 6.4 Conclusions

Designers are asked to meet specifications for power, speed, and SER for any given design. Designers have access to a library containing a wide variety of FF cells (or logic circuits) with varying levels of performance penalty and radiation hardness. Traditional SE

analysis for these FF designs and logic circuits usually compares SE performance for a given set of conditions (supply voltage, speed, temperature, particle LET, etc.). Designers need to identify the best performing (usually the lowest power requirement) FF designs and logic circuits for meeting SER specifications. Since design library does not contain such comparative analysis (SER as a function of power), designers have to carry out additional analysis and test. In this chapter, instead of traditional analysis (SER as a function of supply voltage, frequency, temperature, etc.) comparative analysis (FF design/logic cicuits, supply voltage, and frequency yielding identical SER values) is carried out to support design efforts. By analyzing the test results (or simulation results) based on such an approach, designers will have access to data that will allow them to optimize a circuit design along multiple dimensions (such as SER, power, and operating frequency). Such an analysis may also yield significant power savings while meeting SER and speed specifications.

A methodology based on empirical models for estimating power, speed, and SE cross-section for sequential circuits is presented. Test circuits fabricated at the 16-nm bulk FinFET CMOS technology node are used to evaluate the proposed models and methodology. Results clearly show the effectiveness of the proposed methodology in finding optimum design and operating condition combination to meet design specifications.

# CHAPTER VII

# CONCLUSIONS

A SEE of ICs is strongly dependent on the supply voltage and the physical capacitance. Reduction in supply voltage as well as technology scaling trends (smaller nodal capacitances) may result in dramatically increased sensitivity of the circuits to radiation. For this reason, SEE induced errors of the low power design has very high demanding to be taken into account especially when designing circuits for applications require high reliability. In addition to meeting power and performance requirements, designers now have to spend a significant effort ensuring that FF cells and logic circuit designs also meet target SER level. Designers usually select the FFs and logic circuits with the best power performance and then tweak the design to meet design specifications. Such an approach dose not allow for optimization or formalization of the design process. Since estimation of sequential logic circuits SER is a complex process involving multitude of (especially power and speed), it is important to develop a simple method for comparing different options that meet power, speed, and SE specifications as well. The primary goal of this work is to build a framework of designing soft-error-aware sequential circuits with power and speed optimization. This framework allows designers to expand sequential circuit designs of choice in terms of the low power designs for meeting target SER and speed specifications.

The key results of this research are 1) A novel approach for evaluating SEE performance of logic circuits have been developed. Computing power can be reduced compare to previous simulation-based approaches. Moreover, the proposed approach is easy to obtain and characterize compare to previous experimental-based approaches. 2) SE

characterization of different FFs fabricated in a 16-nm bulk FinFET CMOS technology have been performed for designing soft-error-aware circuits with power and speed optimization. First time differential FF have been detailed analyzed for SE performance at 16-nm bulk FinFET technology node. 3) A framework of designing soft-error-aware sequential circuits with power and speed optimization have been developed. This framework allows designers to expand sequential circuit designs of choice in terms of the low power designs for meeting target SER and speed specifications. Instead of traditional analysis (SER as a function of supply voltage, frequency, temperature, etc.) comparative analysis (FF/logic designs, supply voltage, and frequency yielding identical SER values) is carried out to identify the best performing (lowest power) designs for meeting SER specifications. Such an analysis may yield significant power savings while meeting SER and speed specifications.

Logic SER, similar to FF SER are a strong function of particles LET values, supply voltage and operating frequency. Hence, characterization of logic SER is necessary to determine the optimized approach for meeting SER specifications for logic circuits. This work first, presents experimental results that characterize logic SEEs as a function of LET and supply voltage for 16-nm bulk FinFET technology node. It was observed that only mitigate the SET pulse-width may not necessarily be effective to reduce the strong impact of the supply voltage on the logic SER for the high-LET particles. In addition, results indicate that particle LET strongly affects logic SEU cross-section and reducing the operating voltages, used for reducing power consumption, will significantly increase SEU cross-section for high-LET particles. Therefore, accurate and efficient estimation of combinational logic SEU cross-section at different circuit parameters and control variables (different LET particles, operating frequency, temperature, and supply voltage) is necessary for designers

to identify best hardening design approaches.

A methodology for evaluating frequency dependence of combinational logic SEU cross-section at different circuit parameters and control variables have been developed. By using experimentally measured cross-section of a conventional DFF and any arbitrary logic circuit cross-section to obtain necessary parameters. SE cross-section values estimated using the proposed method were compared with the experimentally measured SE cross-section for a variety of logic circuits. The estimated logic SE cross-section results obtained with the proposed method are within 2X average error when compared to the experimentally measured logic SE cross-section. The proposed method can be included in the design flow to optimize and improve the SE performance of sequential circuits. The proposed method is used to explore design space for logic circuits.

The primary goal of this work is to build a framework of designing soft-error-aware sequential circuits with power and speed optimization. In order to create a model for FF cells that will allow designers to identify the best performing (lowest power) designs for meeting SER specifications, comprehensive study on the SEU of different FF designs have been carried out. Effects of operating frequency, supply voltage, particle LET, and temperature on SEU cross-section for different FFs are evaluated and actual experimental data are reported. It was found out that even at high temperature condition, the SEUs for the 16-nm bulk FinFET changes minimally. Also, first time differential FF have been analyzed for SE performance at the 16-nm bulk FinFET technology node in this work. Similar process can be carried out to characterize SEU of other differential FFs. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints.

Traditional SE analysis for sequential circuits usually compares SE performance for a given set of conditions (supply voltage, speed, temperature, particle LET, etc.). Designers need to identify the best performing (the lowest power requirement) FF designs and logic circuits for meeting SER specifications. Since design library dose not contain such comparative analysis (SER as a function of power), designers have to carry out additional analysis and test. A design methodology employing empirical models for identifying the optimum combination of topology, supply voltage, and frequency for a target SEU budget specification was proposed. The proposed method was able to create a multitude database (supply voltage, operating frequency, power, and SEUs) for FFs and logic circuits. This will allow designers to identify optimum design for a given set of specifications. Specific examples clearly show the effectiveness of the proposed methodology yield significant power savings while meeting SER and speed specifications.

Future work includes to apply these developed methods to a real world full scale system. Optimum design for a given set of specifications could yield, even though this would be a significant investment.

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