SINGLE-EVENT CHARACTERIZATION OF A 90-nm

BULK CMOS DIGITAL CELL LIBRARY

by

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CHAPTER I

INTRODUCTION

1.1 Overview

A single event occurs when an ionizing particle strikes a microelectronic circuit and deposits charge in the semiconductor material. The charge deposited by the particle is often collected by the circuit, resulting in a current transient that can lead to soft errors, depending on the circuit response. In this thesis, single-event (SE) mechanisms in combinational logic are discussed in the context of a 90-nm digital cell library in bulk CMOS. Technology Computer Aided Design (TCAD) simulations are used to investigate various parameters across different cell designs. Knowledge of the effects of layout- and circuit-level parameters on SE response is used to perform a TCAD characterization of a 90-nm digital cell library. The results give insight into relative SE vulnerability of different types of logic cells and structures.

1.2 Overview of previous work

The findings of previous work provide strong motivation for the study of single-event transients (SETs) performed for this thesis. As transistors continue to scale down in size, soft errors due to SETs become a great concern in the radiation response of electronics. In particular, the soft error rate due to SETs in combinational logic increases linearly with clock frequency, due to increased probability of latching an erroneous pulse [1]-[3]. The critical transient width for a pulse to propagate through circuitry to a latch

has decreased with technology scaling because circuits have become fast enough to propagate short pulses on the order of hundreds of picoseconds [4]-[6]. Coupling the decreasing critical transient width with the decreasing critical Linear Energy Transfer (LET) for production of SETs in combinational logic [5] in highly scaled technologies, it is clear that SETs must be well understood in order to ensure the reliability of current and future technology nodes.

In addition to changing the circuit- and system-level sensitivity to SETs, scaling has drastically changed the single-event (SE) response at the device level. The mobile charge cloud deposited by an ion strike can entirely encompass one or more transistors and well contacts. Due to the potential push-out caused by the charge cloud, the SET current pulse shows a plateau which corresponds to the restoring current of the complementary device [7]. As a result, restoring current is very important parameter that governs the SE response of a circuit.

Not only does scaling change the shape of the SET, but it allows for SE charge sharing, i.e. multiple devices collecting charge from a single strike [7]-[8]. While charge sharing can be detrimental to digital cells such as SRAMs [9] and latches [10], it can also be beneficial in certain combinational logic configurations in which SET pulse quenching can occur [11]. In this thesis, both the negative and positive impacts of charge sharing are investigated in combinational logic cells.

Moving up above the device-level in the desing hierarchy, the circuit and logic aspects of single-event effects are crucial to the performance of cell libraries in a radiation environment. In [12] a testing approach for assessing hardness of ASIC libraries was presented. By fabricating and testing worst-case structures from library

cells, the library characterization process was optimized, and the results be used to design SE-tolerant ASICs. The SE experiments were able to compare pulse widths and cross sections of different logic cells. Although the methodology used in this thesis is similar to that in [12], this thesis focuses on library characterization via simulation. Another testing method for SET characterization of logic libraries was presented in [13]. A study of multiple-event transients from nuclear reactions focused on charge collection voumes several logic cells in a similar way that the worst-case SET parameters are investigated in Chapter 6 of this thesis [14]. Finally, a design method that mitigates SET propagation by selecting library cells to increase logical masking is presented in [15]. All of these previous works focus on either circuit-level simulation or testing to characterize SETs in cell libraries, whereas this work focuses on the mechanisms that govern the SE response of digital library cells.

1.3 Statement of research problem and overview of thesis

The goal of this work is to perform a single-event characterization of a 90-nm digital cell library using TCAD simulation. This is a challenging problem due to the number of cells, device sizes, and possible circuit conditions (e.g., input states). The library considered in this work contains over 500 cells, from a minimum-size inverter to complex latches and multiplexers. The cells in the library include about 60 NMOS and 100 PMOS channel widths. Standard TCAD single-event simulation on all device and circuit variants for all the cells is difficult to complete in a reasonable time. By identifying the critical factors and trends in SE simulation of digital library cells, the single-event library characterization can be simplified and the simulation time reduced. In

the process of the library characterization, many critical aspects of charge collection by devices in 90 nm bulk CMOS were investigated. In this thesis, device, circuit and layout parameters of logic cells are investigated to understand their contribution to a cell's SE response.

Chapter 2 is a discussion of the 3-D TCAD and compact models of the 90 nm CMOS transistors used for mixed-mode simulations throughout this work.

In Chapter 3, the basic mechanisms of SEs in 90-nm bulk CMOS are discussed by looking closely at three basic simulations. Ion strikes are simulated in a diode, an unloaded pMOSFET, and a pMOSFET in a mixed-mode inverter in order to demonstrate how the deposited charge is transported within the silicon.

In Chapter 4 the effects of device folding on SE response are investigated. Variations on pFET and nFET folding schemes are simulated and compared. This study reveals important differences in pFET and nFET charge collection in folded transistors. Specifically, increasing a CMOS inverter's size by folding the devices is much more effective in mitigating SETs originating in nFETs than those originating in pFETs.

Chapter 5 presents a study of three critical factors of digital cell SE response: 1) device drain area, 2) restoring current, and 3) n-well contact scheme. Drain area and restoring current (drive strength) are two parameters that vary widely in a cell library. Simulations show positive correlation between drain area and pule width and negative correlation between restoring current and pulse width. The distance from pFET to n-well contact and the area of the well contact directly affect the bipolar amplification of SE charge, however these parameters are relatively fixed for all cells in the library. Therefore, n-well contact parameters govern the overall response of all library cells. On

the other hand, drain area and restoring current produce cell-to-cell variations in the SE response.

In Chapter 6, the worst-case SE characterization of a digital cell library is discussed. The SE response of inverter, NAND, NOR, and complex logic cell types are compared as functions of single-event LET and transistor drive strength. As LET increases, the bipolar amplification of SE charge becomes more pronounced, and SET pulse widths of different cells become less varied. This is because the n-well contact scheme is similar for all cells, meaning the SET duration is determined predominantly by the n-well response to high LET ions.

Chapter 7 is an in-depth look at SETs in a single logic cell, the AND gate. Strike location is varied across the layout of both the pFET and nFET portions of an AND gate. In the pFET simulations, a charge sharing effect known as pulse quenching [11] reduces the pulse widths and sensitive areas of ion strikes. The effect is more pronounced for high LET and high angle of incidence when charge sharing is promoted. The effectiveness of charge sharing in reducing SET pulse widths suggests a cheap and simple way to decrease SE vulnerability of digital cells, which is discussed in some detail.

CHAPTER II

DEVICE MODELS

In this work, Technology Computer Aided Design (TCAD) simulation is used to investigate single-event effects in the IBM 9SF 90 nm bulk CMOS process. In order for these simulation results to be meaningful, accurate device models are necessary. This chapter focuses on the TCAD models used throughout this work.

2.1 3-D TCAD models

The creation and initial calibration of the device models used in this work is well documented in [16]. The TCAD models were developed in Synopsys Structure Editor and simulated in SDevice [17]. All simulations in this work were performed on the ACCRE cluster at Vanderbilt University [18]. However, since the original model calibrations were for specific gate widths (200 nm for n-channel and 480 nm for p-channel), it was necessary to verify the calibration using larger gate widths, in order to characterize all the device sizes used across a cell library.

The 1x inverter in the library was used to select the channel widths of the TCAD devices to be calibrated. It should be noted that the 1x inverter in this case does not use the minimum device dimensions of the technology; it is simply the smallest inverter in the library. The pMOS device model with channel width of 840 nm required further tweaking while the nMOS device model with width 280 nm did not. A reasonable match was obtained through slight adjustments to the V_t implant, the lightly doped drains

(LDD), and the halo implants. The calibration of the TCAD models can be verified against (matching within 10%) the IBM CMOS9SF Spice models available from the MOSIS Service [19]. Figures 1(a) and (b) show the I_D-V_{DS} and I_D-V_{GS} curves for the TCAD nFET model, and Figures 1(c) and (d) show the same curves for the pFET model.

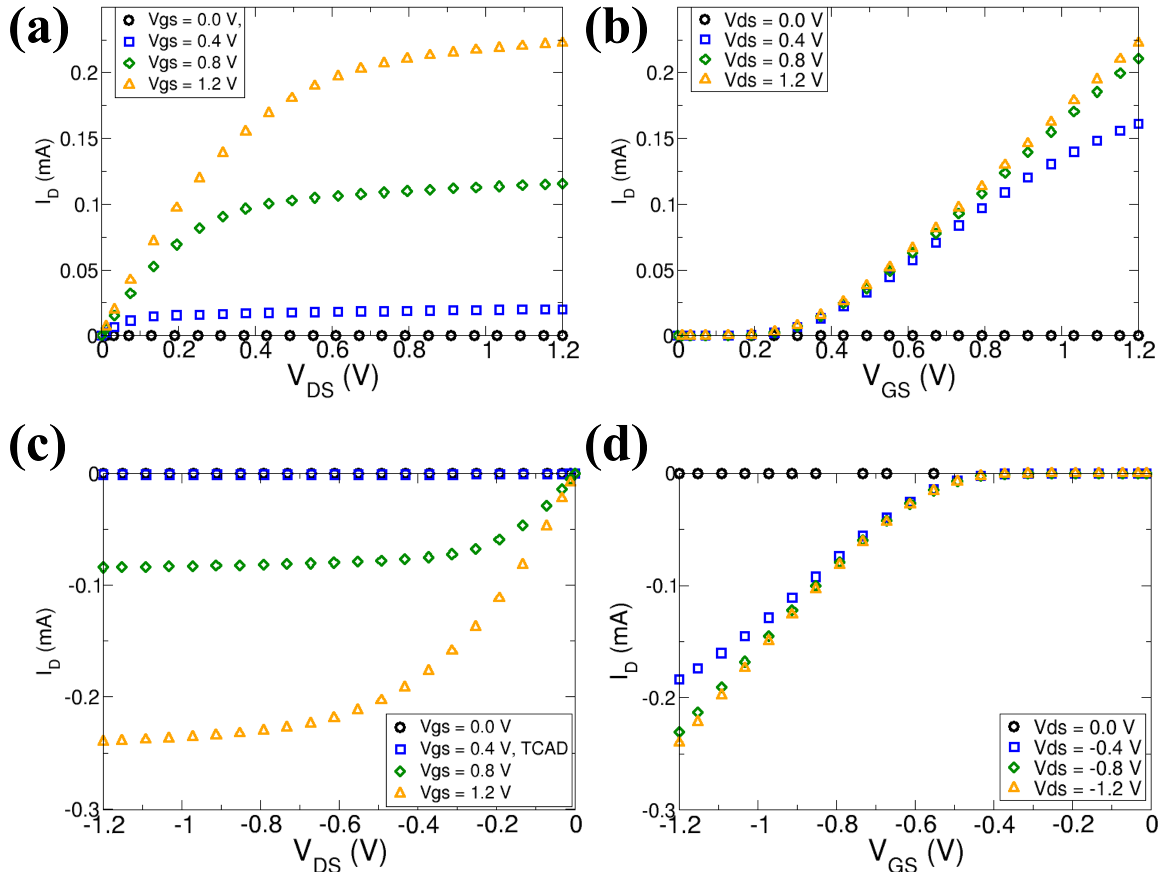

Fig. 1: (a) I_D-V_{DS} curves for the TCAD nFET model with W = 280 nm, (b) I_D-V_{GS} curves for the TCAD nFET model with W = 280 nm, (c) I_D-V_{DS} curves for the TCAD pFET model with W = 840 nm, (d) I_D-V_{GS} curves for the TCAD pFET model with W = 840 nm

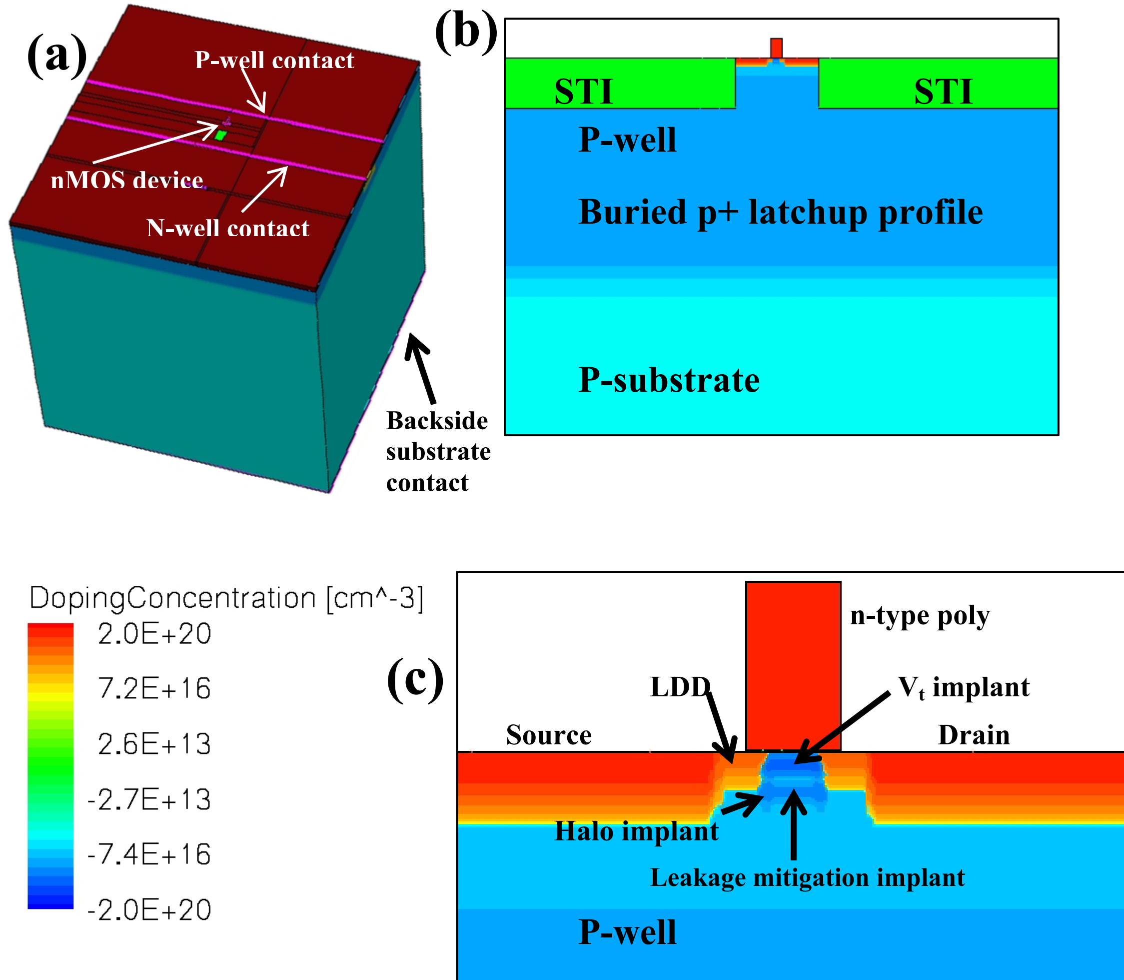

Fig. 2: (a) NMOS device TCAD model on 20x20x20 μm^3 substrate, (b) cross section of nMOS device model and well/substrate structure, (c) zoomed-in cross section of nMOS device model showing all doping profiles

Figures 2(a)-(c) show the nFET TCAD model used throughout this work. In Fig. 2(a) the entire 3-D structure is shown. The large substrate volume of 20x20x20 μm^3 was chosen to reduce the possible carrier reflections at the silicon volume boundaries that a smaller volume exhibits. Both the p-well and n-well are included in all simulations to capture all possible well and substrate effects. The relative size of each well and its contact is kept the same for both pFET and nFET simulations. Figures 3(a)-(c) show the pFET TCAD model. The same substrate and well structures are used for both n- and p-

channel transistor models. A backside substrate contact is used with a resistance of 1 kΩ to model the contact of the p-type substrate to ground. Details on the doping profiles for both models are available in detail in Appendix A.

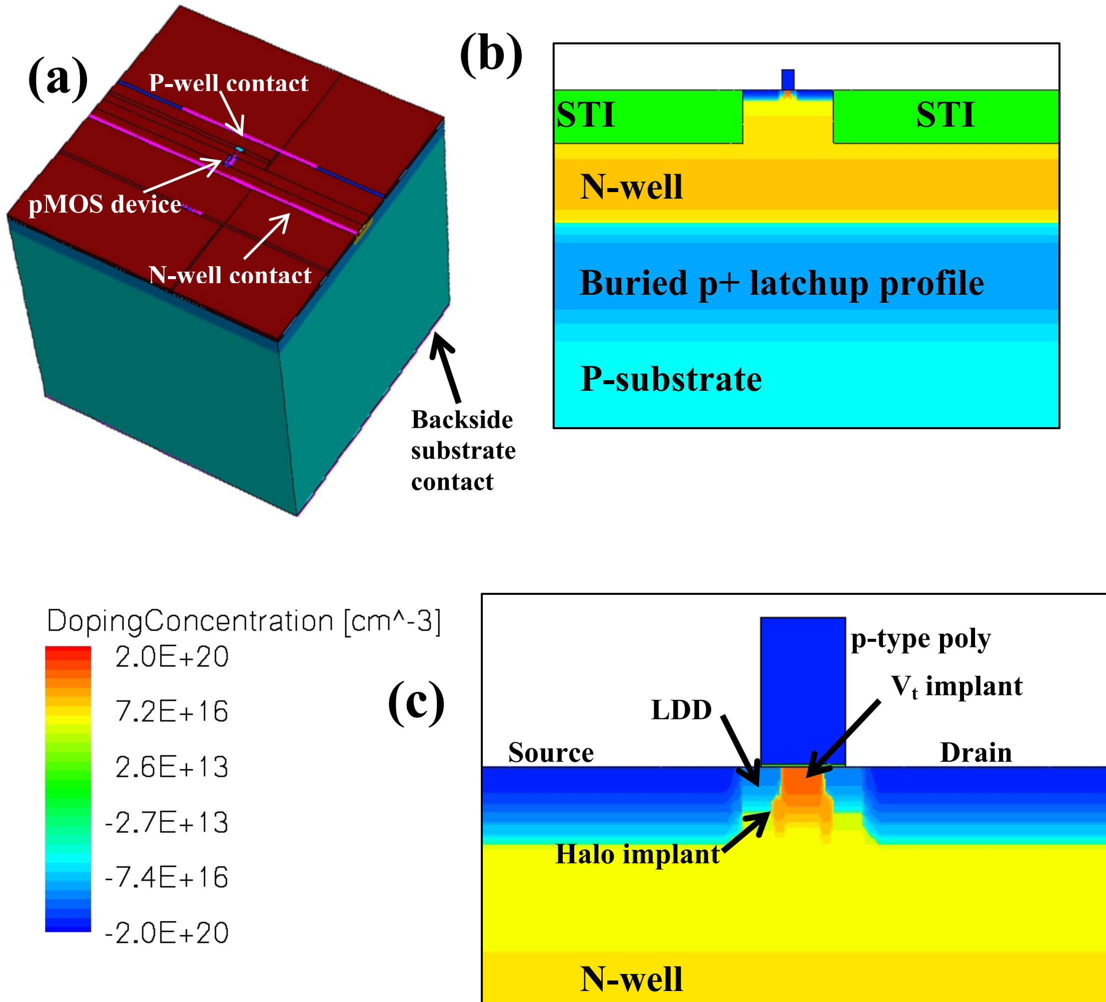

Fig. 3: (a) NMOS device TCAD model on 20x20x20 μm^3 substrate, (b) cross section of nMOS device model and well/substrate structure, (c) zoomed-in cross section of nMOS device model showing all doping profiles

2.2 Compact modeling

When circuits with too many devices for pure TCAD simulation are required in a single-event simulation, it is necessary to use mixed-mode simulation, which models some transistors in Spice and some transistors in TCAD. The SDevice simulator uses BSIM3v3 MOSFET models, which can be extracted from any representative set of 9SF compact models.

The Structure Editor SDE scripts and a sample SDevice simulation script are included in the Appendix A. Details on carrier-carrier scattering models and variations in doping profiles are contained in Appendices B and C.

CHAPTER III

BASIC SINGLE-EVENT SIMULATION

In order to discuss SEEs in different device geometries, it is first necessary to discuss the fundamental mechanisms of SEEs. An ion strike begins the charge collection process by first depositing charge in the semiconductor region. The amount of charge depends on the linear energy transfer (LET) of the ion, the strike's path length through the sensitive volume, and the struck material which is assumed to be silicon for the remainder of this discussion. Deposited charge can be estimated by the product of LET [pC/μm] and path length [μm]. If this SE charge is deposited in a simple block of silicon, it will eventually recombine and equilibrium will be restored. However, if the charge is deposited at or near a p-n junction, then separation of charge carrier types, collection of this charge in different semiconductor regions, and propagation to the device terminals occur and a single-event effect is observed.

One primary mechanism by which SE charge is collected is drift across reverse-biased junctions. In this way, minority carriers are collected by either device drains or well-substrate junctions. Additionally, carriers diffuse away from the high-density ion track, so the drift collection process is assisted by diffusion.

A particularly interesting collection mechanism that is repeatedly observed in this work is bipolar amplification of SE charge in pFETs. In a dual-well CMOS process, the n-well is relatively small and isolated from the substrate, with electrons only able to exit via the n-well contact. On the contrary, holes in the p-well can easily transport down into

the large p-type substrate. Because of this isolation, an ion strike in the n-well can cause the n-well potential to drop significantly below V_{DD}, termed well collapse. The magnitude and extent of the n-well collapse depend on the charge deposited (strike LET and path length). Electrons deposited in the n-well must exit through the n-well contact to stabilize the potential. Since the p+ source of the pFET is biased at V_{DD}, the source/n-well junction becomes forward-biased when the n-well potential drops sufficiently. Therefore, the source injects holes into the n-well resulting in additional charge that can be collected by reverse-biased junctions, i.e. the deposited charge is amplified. However, a secondary effect of the well-collapse is electron back-injection, or departure from the n-well, through the forward-biased source/n-well junction. Electrons deposited in the n-well by an ion can exit through the source as well as the n-well contact. Although the back-injected electron current is lower than the n-well current, it still rather important because it helps to stabilize the n-well potential. These various effects will be described by looking at three basic simulations.

3.1. Ion strike on p+ diode

Perhaps the most basic SEE simulation is an ion strike on a diode, in this case a p+/n-well diode identical to the drain of a pFET. Figure 4 shows a cross section of the diode with every electrode of the device labeled. In this TCAD model, Kirchoff's current law must be satisfied, i.e. the charge deposited by the strike must exit through the electrodes shown in Fig. 4 so that the electrical terminal currents sum to zero. Consequently the sum of the negative charge and positive charge leaving the terminals must also sum to zero. The electron and hole currents **into** each of these electrodes are

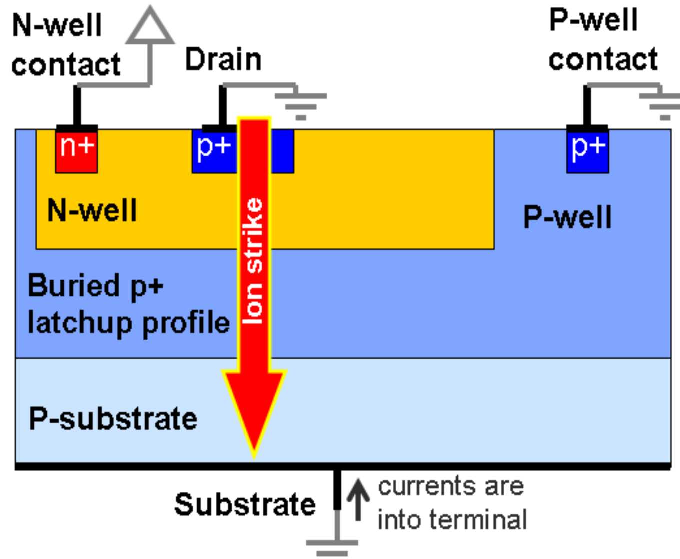

Fig. 4: Cross section of p-drain/n-well diode model with all device terminals labeled. Ion strike location and direction are displayed.

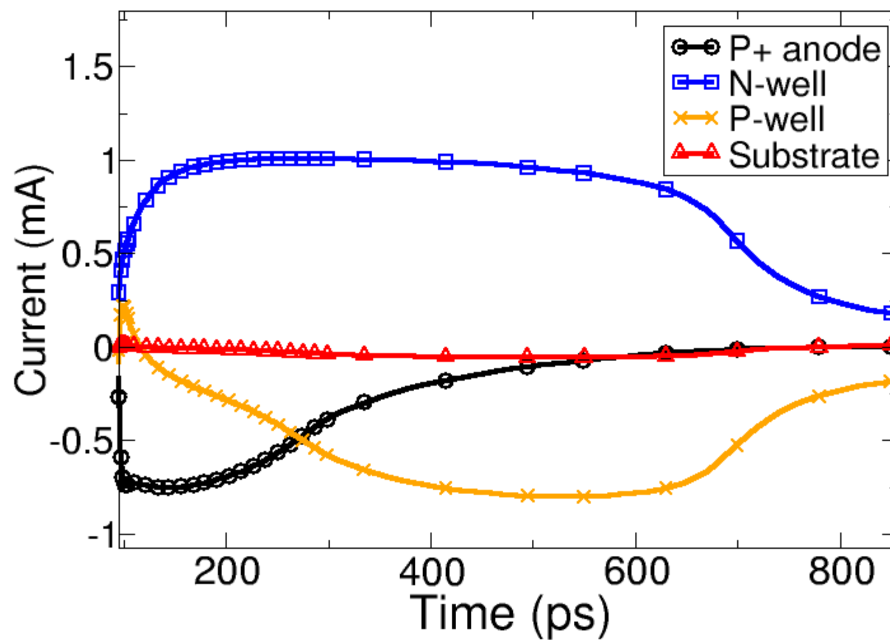

Fig. 5: Single-event currents of all terminals of diode resulting from a 40-MeV-cm^2/mg strike.

plotted in Fig. 5. The only positive current resulting from the strike is the n-well current. The electrons exiting through the n-well contact produce a net positive current into the terminal. In order to quantitatively compare the charge collected by each electrode, each current transient in Fig. 5 is integrated and tabulated as electron (e) and hole (h) charge in

Table 1. For example, a negative hole current indicates holes exiting a terminal, while a positive electron current indicates electrons exiting a terminal. This gives insight into where the deposited charge is going.

Table 1: Charge collected by the device terminals in Fig. 4 from a 40-MeV-cm^2/mg normal strike ('e' indicates integrated electron current and 'h' indicates integrated hole current)

	Net charge (fC)
P+ anode	-180 (h)
N-well	710 (e)
P-well	-520 (h)
Substrate	-10 (h)
Sum	710 - 710 = 0

Since the p+/n-well diode is reverse-biased, the p+ anode collects only minority carriers in the n-well, holes. The n-well and p-well each collect majority carriers only. Finally, the backside substrate contact collects large amounts of both holes and electrons, since there are no electric fields to separate the carriers in the bulk. These carriers simply diffuse together and exit the substrate. The resulting net substrate current is very small compared to the other terminals.

Holes exit via the p+ diode, p-well, and substrate, resulting in net negative charge (negative current in Fig. 5) through these terminals. Electrons exit via the n-well, resulting in net positive chare. As expected, the sum of these charges is zero, with the magnitude of either the positive or negative charge being equal to the charge deposited by the ion, since electrons and holes are liberated in pairs. Because the strike's LET was 40 MeV-cm^2/mg, which is 0.4 pC/μm in Si, the path length through the sensitive region was approximately 0.71 pC / (0.4 pC/μm) = 1.8 μm. Since the strike was at normal incidence, this length corresponds to the depth of the sensitive region, which is physically the bottom of the buried p+ latchup profile. The interaction of the ion with the silicon

beyond a depth of 1.8 μm simply liberates pairs that do not separate. Performing this calculation at different LETs results in variations, e.g. the same strike with LET of 80 MeV-cm^2/mg yields a collection depth of 1.4 μm. This is due to the STI reducing the amount of charge deposited for these very high LET ions. Therefore, the collection depth is very approximately ~1.6 μm.

3.2 Ion strike on unloaded pMOSFET

The next simulation is of a pFET, achieved by adding the gate and source to the previously modeled p+ drain. In this simulation the pFET is unloaded, tying the drain

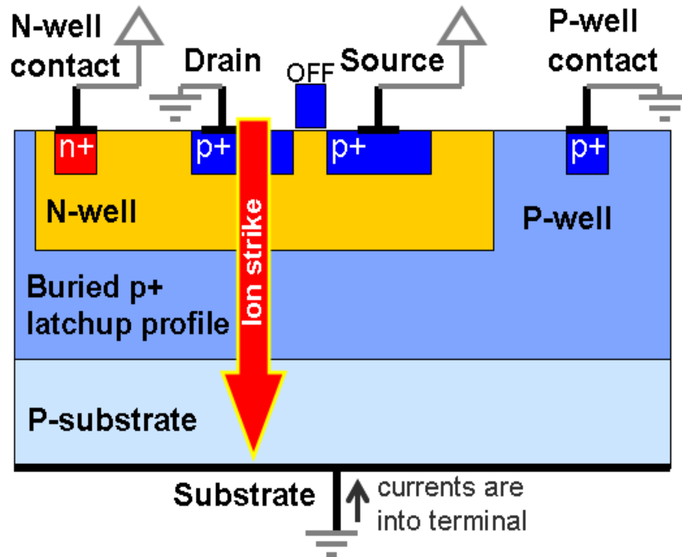

Fig. 6: Cross section of p-drain/n-well diode model with all device terminals labeled. Ion strike location and direction are displayed.

directly to ground. The cross-section of the device, with all electrodes labeled, is shown in Fig. 6. In changing the device from a diode to a transistor, the only new terminal that draws appreciable current is the source, which changes the SE response significantly. As

with the diode, a 40-MeV-cm^2/mg, normal strike was simulated through the drain and the current transients of the device electrodes are plotted in Fig. 7. The large, positive source current indicates the injection of holes and back-injection of electrons, which significantly affects the other terminal currents compared to the currents of the diode in Fig. 5. Table 2 shows the integrated currents (collected charge) of each electrode.

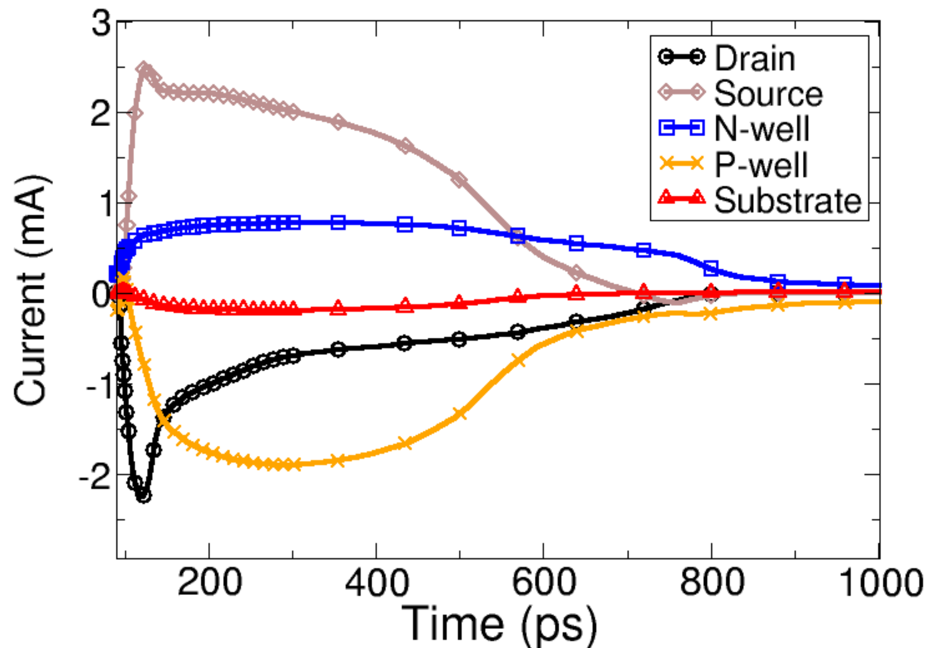

Fig. 7: Single-event currents of all terminals of unloaded pFET resulting from a 40-MeV-cm^2/mg strike.

Table 2: Charge collected by the device terminals in Fig. 6 from a 40-MeV-cm^2/mg normal strike ('e' indicates integrated electron current and 'h' indicates integrated hole current)

	Net charge (fC)
Drain	-430 (h)
Source	840 = 270(e) + 570(h)
N-well	540 (e)
P-well	-920 (h)
Substrate	-30
Sum	1380 - 1380 = 0

As in the diode simulation, the drain, p-well, and substrate all exhibit negative charge (holes exiting), while the n-well exhibited positive charge (electrons exiting). The source exhibits positive charge due to electrons exiting and holes entering, with the electron and hole components are shown in Table 2. As with the diode, the sum of all these charges is zero, but the magnitude of both the positive and negative charge (1380 fC) is much greater than the value obtained from the diode simulation (710 fC) with the same ion strike and deposited charge. The difference in charge collected by diode and pFET demonstrates the bipolar amplification phenomenon.

The difference between total pFET charge (Table 2) and total diode charge (Table 1) is 1380 – 710 = 670 fC, which is reasonably close to the amount of charge injected by the source, 570 fC. The presence of the source also affects the other terminals when compared to the diode simulation. Since the drain is the terminal connected to a circuit element and not power or ground, the increased collection of charge on the drain is a significant effect. Because the source, acting as a pnp emitter, injects holes into the n-well (base), there are more holes to diffuse to and be swept in by the drain (collector). An in-depth analysis of the well-collapse source-injection mechanism is given in [19]. This is why the drain-collected charge is much higher than the diode-collected charge. However, the p-well can also act as a collector in this bipolar process, thus, the presence of the source also results in more charge collected by the p-well. However, the n-well collects less charge when the source is present because a significant number of electrons are back-injected through the source instead of exiting through the n-well contact.

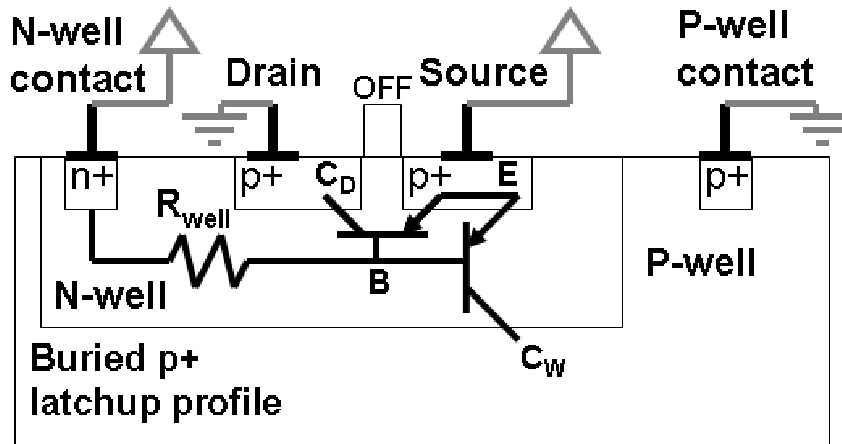

Fig. 8: Cross section of pFET with bipolar transistors drawn schematically.

Figure 8 shows the schematic of the parasitic bipolar transistors super-imposed on the pFET cross section. The two pnp transistors seen in this simulation are formed by the source/n-well/drain and source/n-well/p-well. These transistors turn ON when the ion strike causes the voltage in the n-well (the base) to drop (i.e., n-well potential collapse). The voltage drop creates a potential gradient between the strike location and the n-well contact (held firmly at V_{DD}). The result of this gradient is current flow in the n-well, along the resistance R_{well} which is discussed in detail in Chapter 5. Thus R_{well} has a significant effect on the emitter-base voltage V_{EB} seen between n-well and source. The positive V_{EB} voltage results in positive current flow from emitter to base. The two acting collectors in the pFET structure are the p-drain (C_D) and the buried p-well/latchup profile (C_W). Since the drain/n-well diode without the source collected 180 fC of hole charge, the number of **source-injected** holes collected by the drain is approximately 430 – 180 = 250 fC. This means the p-well collects the remainder of the source-injected holes, 320 fC. The charge collected by these terminals would be different if the drain voltage were not fixed at 0 V. In a real circuit the drain would not be tied to ground but would be

connected to a complementary device, allowing the drain voltage to change. The effect of loading the struck pFET will be investigated in the next section.

3.3 Ion strike on pMOSFET in mixed-mode inverter

Finally, the same pMOSFET was simulated with a current-matched nMOSFET connected in an inverter configuration. The nFET is implemented as a compact model in Spice, making this a mixed-mode simulation. The reasons for adding the complementary device are: 1) this is a much more realistic situation and 2) the nFET limits the drain current, which alters the SE response of the other terminals. A cross-section of the model is shown in Fig. 9 with the complementary device added. The same normal, 40-MeV-cm^2/mg strike was simulated, and the resulting current transients are plotted in Fig. 10. The pull-down nFET clearly limits the drain current compared to the transient in Fig. 7. The integrated currents into each electrode are tabulated in Table 3.

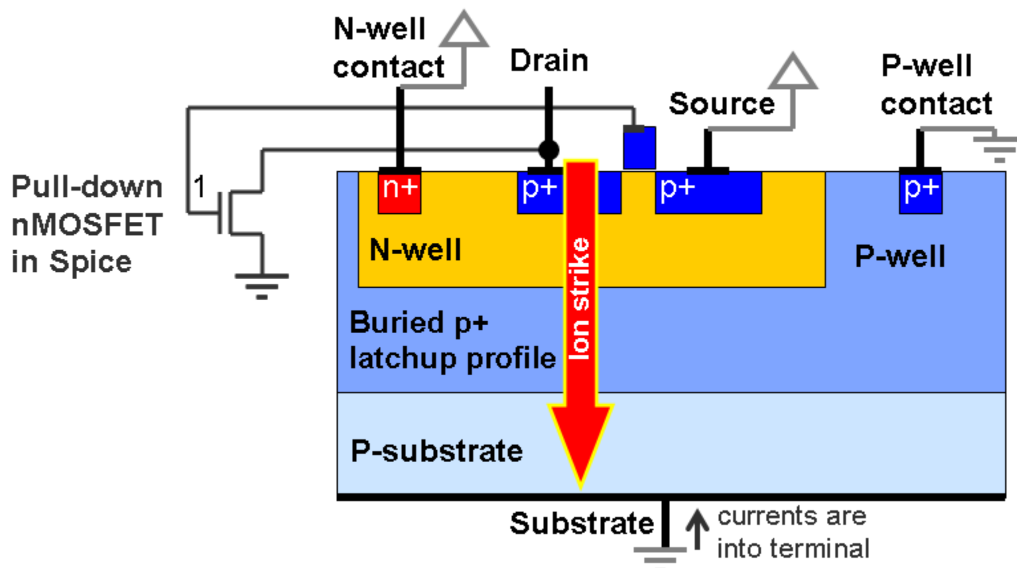

Fig. 9: Cross section of p-drain/n-well diode model with all device terminals labeled. Ion strike location and direction are displayed.

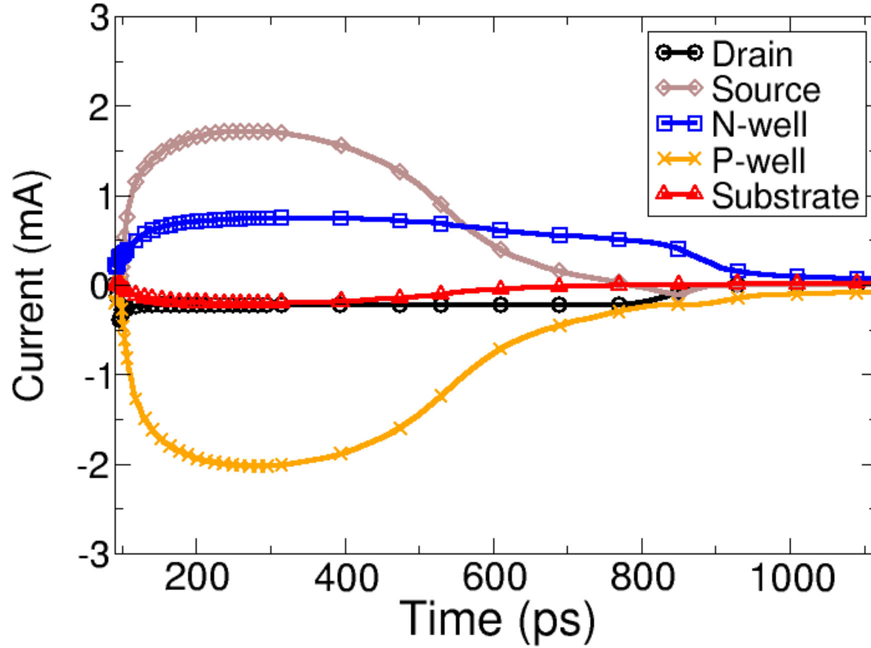

Fig. 10: Single-event currents of all terminals of pFET in current-matched inverter resulting from a 40-MeV-cm^2/mg strike.

Table 3: Charge collected by the device terminals in Fig. 9 from a 40-MeV-cm^2/mg normal strike ('e' indicates integrated electron current and 'h' indicates integrated hole current)

	Net charge (fC)
Drain	-170 = 40(e) – 210(h)
Source	690 = 230(e) + 460(h)
N-well	570 (e)
P-well	-1040 (h)
Substrate	-50 (h)
Sum	1260 - 1260 = 0

In comparing the loaded pFET to the unloaded pFET, the charge polarities are the same, but the magnitudes are different. The largest difference is in the drain-collected charge. Because the nFET limits the drain current to 230 μA, the collected charge is limited and, thus, much smaller than in the unloaded pFET. Since the SE current exits the drain through the nFET channel resistance, a voltage transient (shown in Fig. 11) is generated. The voltage rises from 0 V to almost V_{DD} (1.2 V) for a certain amount of

time. The current and voltage plateau effects are described extensively in [16]. When the drain voltage is high, the drain/n-well barrier is lowered, so some electrons do actually exit via the drain. This electron component of drain-collected charge is shown in Table 3. If the total charge collected by the drain is divided by the nFET drive current, the time value 170 fC / 230 μA = 740 ps is obtained. This value is within 4% of the full-width half-rail (FWHR) voltage SET pulse width (710 ps), since it is a measure of the time for the collected charge to be sunk by the nFET.

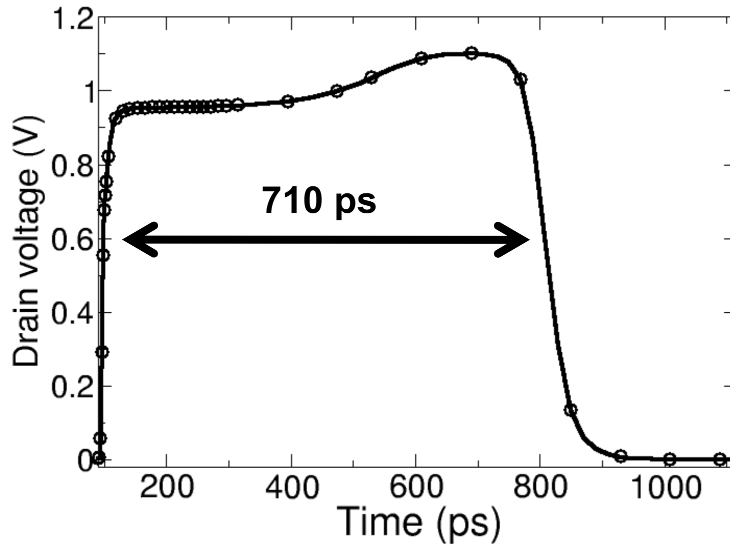

Fig. 11: Drain voltage transient resulting from a 40-MeV-cm^2/mg strike on the pFET of a current-matched inverter. The full-width half-rail pulse width of the transient is shown.

The current-limiting nFET also affects the other device electrodes. The p-well collects more charge when the drain is loaded, because the holes not collected by the drain are collected by the p-well (according to the bipolar structure in Fig. 8). The electrons back-injected through the source are reduced when the drain is loaded, because some electrons are also back-injected through the drain. Because the drain ejects

electrons, the potential of the n-well near the source is slightly higher than in the unloaded pFET. As a result, the forward-bias of the source/n-well junction is slightly less, and, being an exponential relationship, this smaller voltage drop results in significantly fewer holes injected by the source. The n-well and substrate terminals show only small changes (tens of fC) in collected charge.

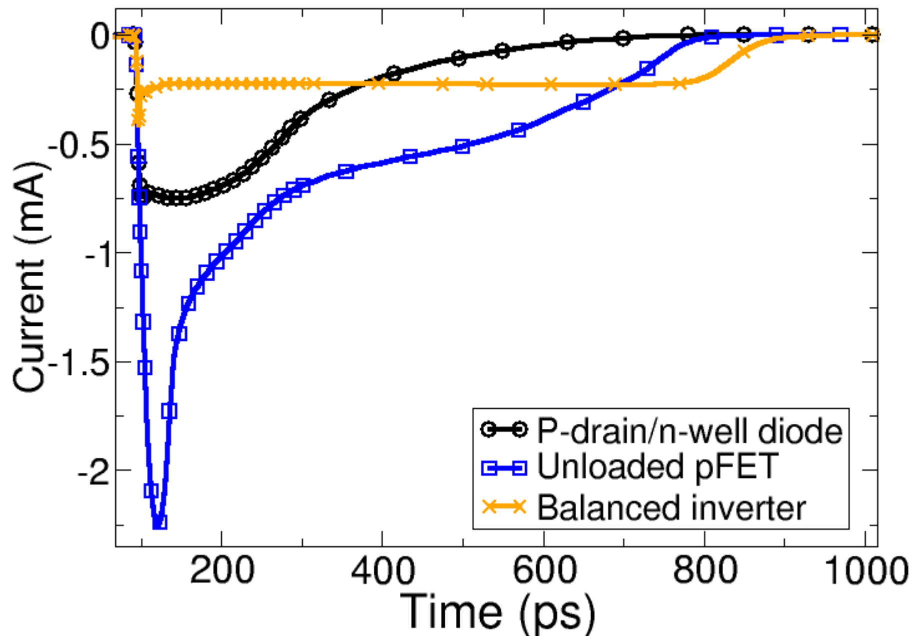

Fig. 12: Current transients of p-drain/n-well diode, unloaded pFET, and pFET in balanced inverter resulting from normal 40-MeV-cm^2/mg through center of drain.

Finally, by plotting the drain currents of each of the three simulations, the qualitative differences can be discussed. In Fig. 12, the difference between the diode current and the unloaded pFET current illustrates the bipolar enhancement of the SE current. Both the magnitude and duration of the unloaded pFET current transient are greater than that of the diode current transient due to the pnp device formed by source (emitter), n-well (base), and drain (collector). The difference between the unloaded

pFET and the balanced inverter transients illustrates the effect of current limiting. The balanced inverter transient exhibits a pronounced current plateau, which corresponds to the saturation current of the complementary device. Although integrating both the pFET currents yields markedly different collected charge values, the duration of the transients is nearly the same. The duration of the n-well collapse is similar for both cases, and the n-well collapse directly controls the parasitic bipolar device. Thus, the duration of drain current transients is similar.

3.4 Conclusion

The basic function of each terminal in the p-MOSFET SE response has been discussed. The low-biased p+ drain collects excess holes from the n-well. The excess holes in the n-well not collected by the drain are collected by the p-well, so holes exiting through the p-well contact consist of holes drifting out of the n-well and holes deposited directly in the p-well. Electrons are either deposited in the n-well or drift into the n-well from the p-well. These electrons exit via the n-well contact and source (if forward-biased). The high-biased p+ source acts as a bipolar emitter, injecting holes and ejecting electrons, because the well collapse forward-biases the source/n-well junction. The injected holes are collected by the drain and p-well, and the ejection of electrons helps to stabilize the n-well potential. Thus the pnp device formed by source/n-well/drain amplifies the charge collected by a circuit.

CHAPTER IV

SINGLE-EVENT RESPONSE OF MULTIPLE-FINGER TRANSISTORS

Multiple-finger (or folded) transistors are commonly used in digital and analog circuits, and are widely used in logic gate libraries. For example, if a wide pFET is required for a design, it may be constrained by the width of the n-well. Figure 13 illustrates a case in which a device must be folded three times to fit in the well. In normal circuit operation folding a device decreases the diffusion-to-well capacitance because of reduced source and drain area, along with a slight increase in gate capacitance due to the extra polysilicon connecting the fingers. In this chapter, nFETs and pFETs with different folding schemes were simulated and compared using SET pulse width and collected charge as the primary metrics. It was seen that the effects of folding are different for n-channel and p-channel transistors due to the different charge sharing mechanisms.

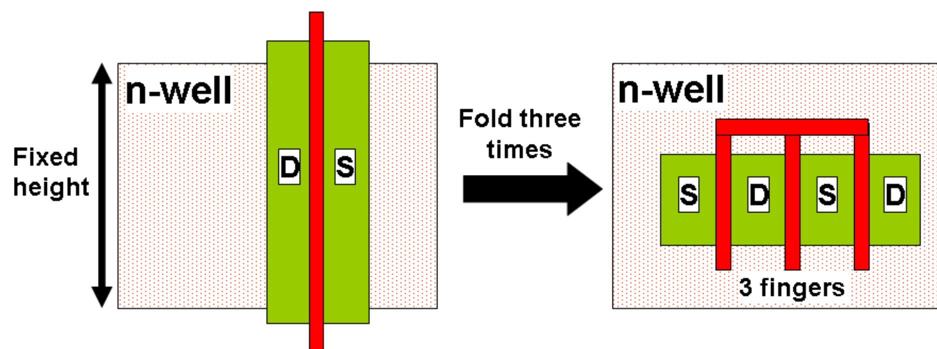

Fig. 13: Illustration of necessity of multiple-finger device to fit wide in well.

4.1 Simulation setup

The calibrated 9SF TCAD models were used for all simulations. For both nFET and pFET simulations, the same well structure was used, as shown in Figs. 14(a) and (b). Both the p-well and the n-well were contacted with strip contacts along the entire length of the well surface. All simulations were performed in a mixed-mode, current-matched inverter configuration. In order to simulate nFET strikes (n-hits), the nFET was modeled in 3-D TCAD, while the current-matched pFET was modeled in Spice using a calibrated compact model. For p-hits, the pFET was modeled in TCAD and the nFET was modeled in Spice. In TCAD the heavy ion with LET 40 MeV-cm^2/mg was modeled as a column with characteristic radius 50 nm.

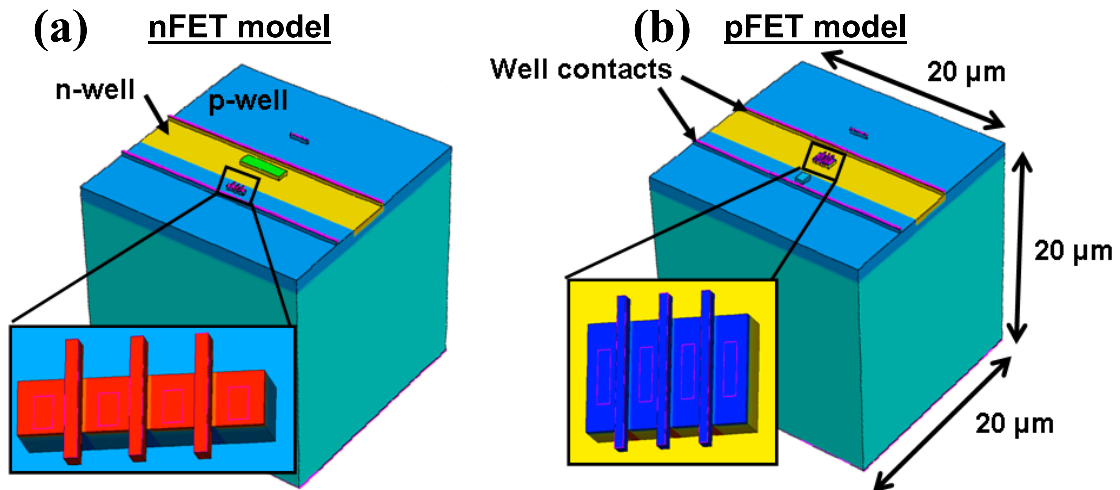

Fig. 14: (a) 3-D TCAD model of 3-finger nFET. STI is not shown to make the well structure visible. (b) 3-D TCAD model of 3-finger pFET. STI is not shown to make the well structure visible.

4.2 Constant drive strength

The first set of simulations kept the total device width (product of finger width and number of fingers) constant while varying the number of fingers. The constant p-

channel width was 3 μm, and the constant n-channel width was 1 μm. The different folding schemes are shown in Fig. 15. As number of fingers increases, finger width decreases and relative source and drain areas change. With the total width constant, the same complementary device is used for all simulations, since drive strength does not change. By varying number of fingers, the effect of folding on SE response can be investigated.

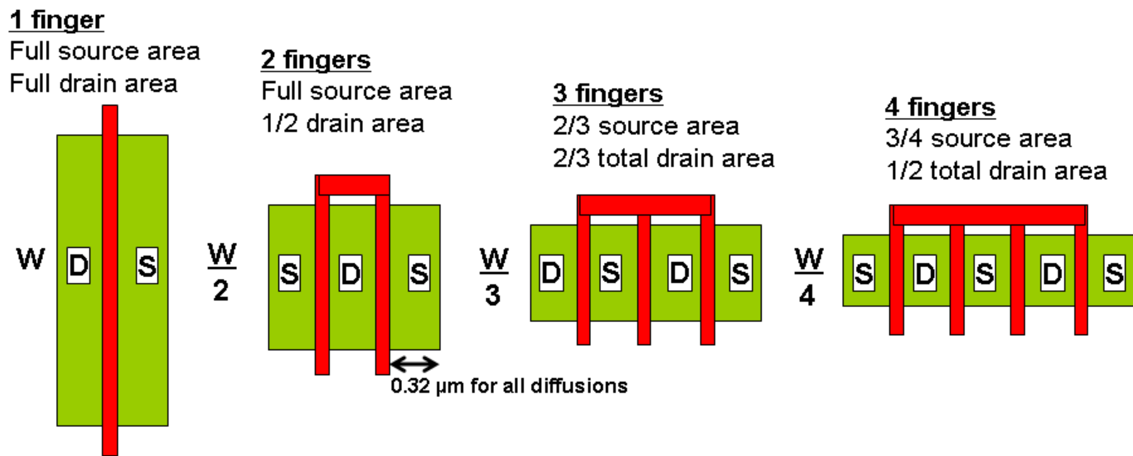

Fig. 15: Folding schemes with constant total device width W = (finger width) x (number of fingers). Source and drain areas are compared to 1-finger device.

Strikes at both normal incidence and 60° to normal incidence were simulated on these structures. The normal strikes passed through the center of the device drain. Since the 3-finger devices were asymmetric, both drains were hit and the worse response was used (the drain with sources on each side). The 60° strikes were angled along the length of the n-well, so the strikes would pass under multiple diffusions. The same approach of finding the worst response was used for the 60° strikes; a typical set of strike locations is shown in Fig. 16.

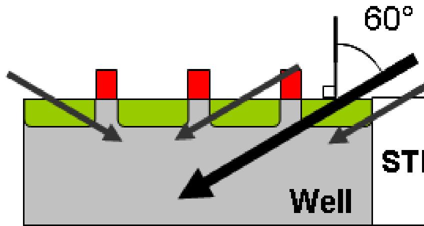

Fig. 16: Cross section of multiple-finger transistor with multiple 60° strike paths shown. The large black arrow indicates the worst-case strike of the strikes shown.

Strikes with LET of 40 MeV-cm^2/mg were simulated on both nFETs and pFETs using these four different folding schemes. First, the charge collected by the device drains is compared. Since the 3- and 4-finger devices had two drains, the current transients of each drain were added together before integrating to compute collected charge. The percent change in collected charge is plotted as a function of the number of fingers for nFETs in Fig. 17(a) and pFETs in Fig. 17(b). For both plots, the percent change is relative to the single finger device. Percent change was used so that nFET and pFET responses could be compared, since the pFETs collected more charge than the nFETs (due to larger size and bipolar amplification).

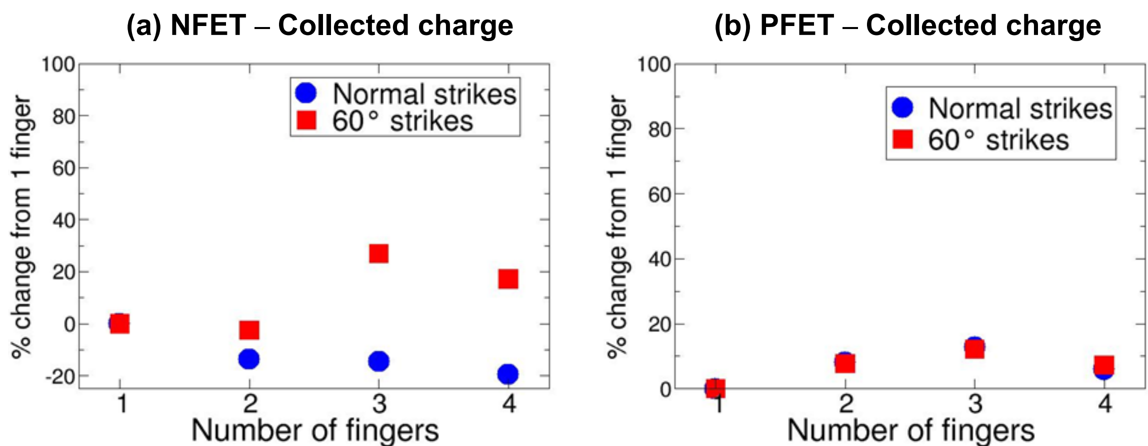

Fig. 17: Change in SE collected charge due to folding in (a) nFETs and (b) pFETs for normal and 60° strikes with LET = 40 MeV-cm^2/mg. The 1-finger device is the reference for % change.

For the nFETs, normal strikes show a decrease (down to -20%) in collected charge as number of fingers increases and 60° strikes show the opposite, increasing as much as 30%. The change in charge collected by multiple-finger pFETs shows no angle dependence. In fact, collected charge changes by a maximum of 14%, showing a fairly weak dependence on number of fingers. Since the pulse width of voltage SETs is often more useful in characterizing SE response of a circuit, the percent change in pulse width for both device types is plotted in Figs. 18(a) and (b).

Single-event transient pulse width shows virtually the same trends as collected charge. The n-hits show between 20% and -20% change in pulse width depending on angle of incidence, and the p-hits show up to 20% increase in pulse width for both angles. The collected charge and pulse width plots indicate a fundamental difference in charge collection of multiple-finger nFETs and pFETs. This difference arises due to charge sharing between drains.

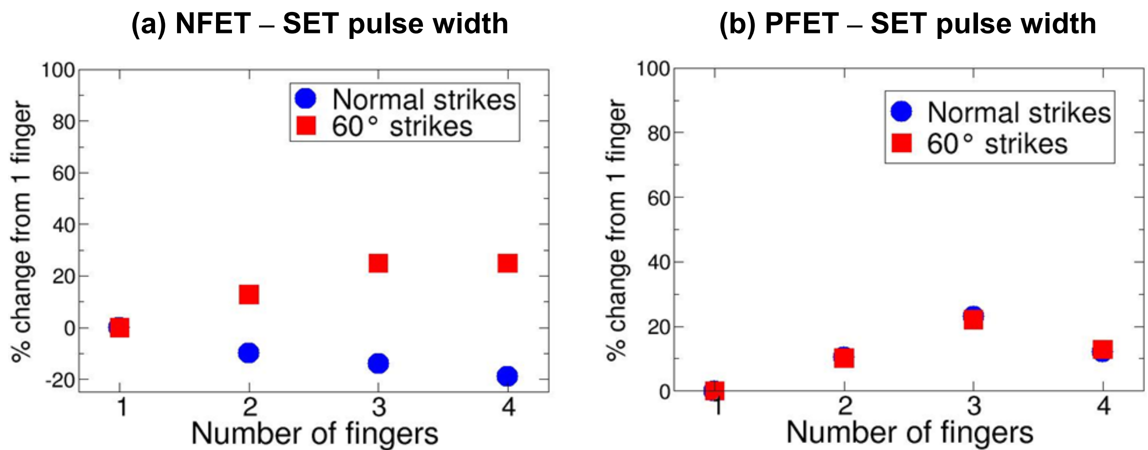

Fig. 18: Change in SET pulse width due to folding in (a) nFETs and (b) pFETs for normal and 60° strikes with LET = 40 MeV-cm^2/mg. The 1-finger device is the reference for % change.

The 3- and 4-finger transistors had two drains in all these simulations, but only one was struck. The drain that is not directly struck can potentially collect charge that diffuses away from the strike path, as shown in Fig. 19. In this figure, Drain 2 is not struck but still collects charge from the strike. By comparing the charge collection of Drain 2 of the nFETs to that of the pFETs, the reason for the different responses can be determined.

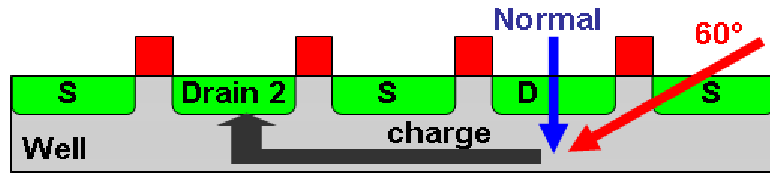

Fig. 19: Cross section of 4-finger device illustrating charge sharing between drains.

In Figs. 20(a) and (b), the charge collected by the struck drain and Drain 2 for the n-hit and p-hit simulations is plotted versus number of fingers. The dashed lines show the total collected charge that was previously plotted as percent change in Fig. 17. For normal n-hits the charge collected by Drain 2 is nearly 0 fC. On the contrary, Drain 2 collects more than 25% of the total charge in the 3-finger and 4-finger pFET normal strike simulations. It was only from an angled strike that Drain 2 collected significant charge in the nFETs, contributing up to 27% of the total collected charge. Similarly, the pFET Drain 2 also collects more charge from the angled strike.

Figure 20(a) explains the angle dependence of nFET collected charge. The struck drain essentially collects the same charge from both normal and 60° strikes, and this charge decreases as number of fingers increases. This is simply due to the decreasing area of this single drain diffusion. Since Drain 2 collects nearly no charge from normal

strikes, the total collected charge decreases as number of fingers increases. Conversely, Drain 2 does collect charge from 60° strikes, so collected charge increases with number of fingers.

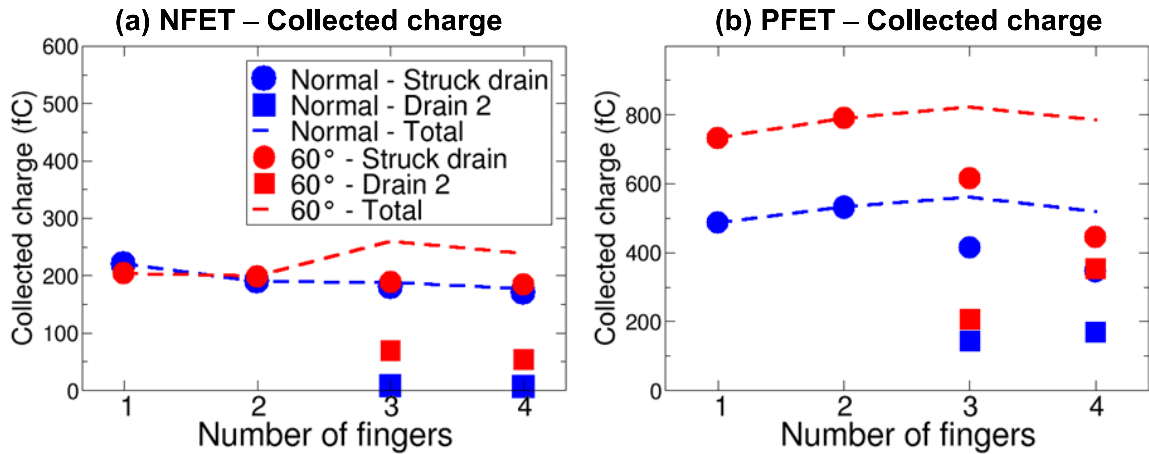

Fig. 20: Charge collected by struck drain and Drain 2 of multiple-finger (a) nFETs and (b) pFETs. There are no Drain 2 values for 1 and 2 fingers because there is only a single drain.

Because of the parasitic bipolar transistors present in the pFET structure, charge collection on multiple nodes, termed charge sharing, is much more prominent compared to nFETs [8]. When the strike causes the n-well potential to collapse, each source diffusion within that collapse area injects holes into the n-well, as discussed in Chapter 3. These holes can be collected by one or more drain diffusions. Due to these complex bipolar processes, the trends in pFET charge collection are not monotonic with number of fingers. The structure of the pnp transistors changes when the folding geometry changes.

To illustrate the changing pnp structures, 1- and 3-finger devices are shown in Fig. 21 with simplified bipolar transistors drawn schematically on the structure. In the 1-finger case, there are two pnp structures that govern charge collected by the drain and p-

well. The 3-finger pFET has five pnp devices that can potentially affect the SE response of the device. The voltages of the bases B_1 and B_2 depend on the strike location so the carrier injection of the each of the sources will be different. Due to the complexity of the bipolar structures, it is unclear from inspection how the SE response changes due to transistor folding, and simulations show that the change in SE response does not follow a monotonic trend with number of fingers.

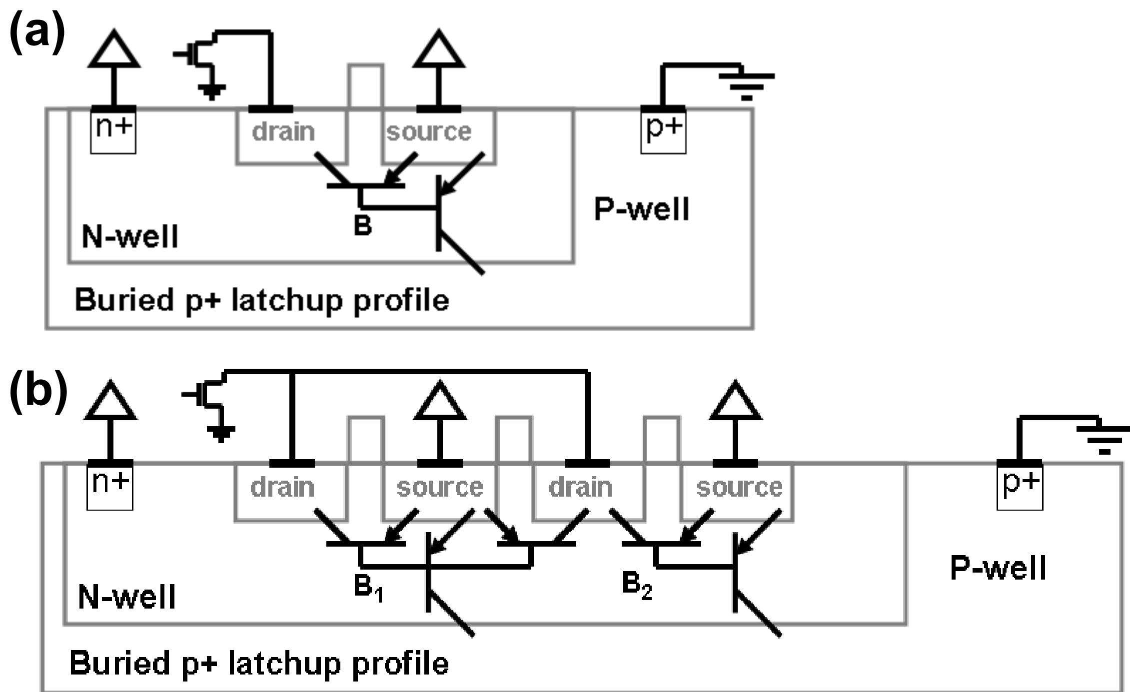

Fig. 21: Cross sections of (a) 1-finger and (b) 3-finger pFETs illustrating pnp structures that affect charge collection.

Charge sharing between drains in nFETs is not as dramatic as in pFETs because the well structures are quite different. While excess majority carriers in the p-well are free to diffuse down into the p-substrate, majority carriers in the n-well are confined. This difference manifests itself in the potential collapse of each of these wells. As shown

in Fig. 22, the n-well voltage drop is significant in both magnitude and area, while the p-well voltage rise is small and very localized. The n-well collapse easily encompasses an entire 4-finger device, while hardly more than a single diffusion is encompassed by the p-well collapse. For these reasons, the primary mechanism for charge sharing in pFETs is bipolar amplification while charge sharing in nFETs happens through simple drift and diffusion [8].

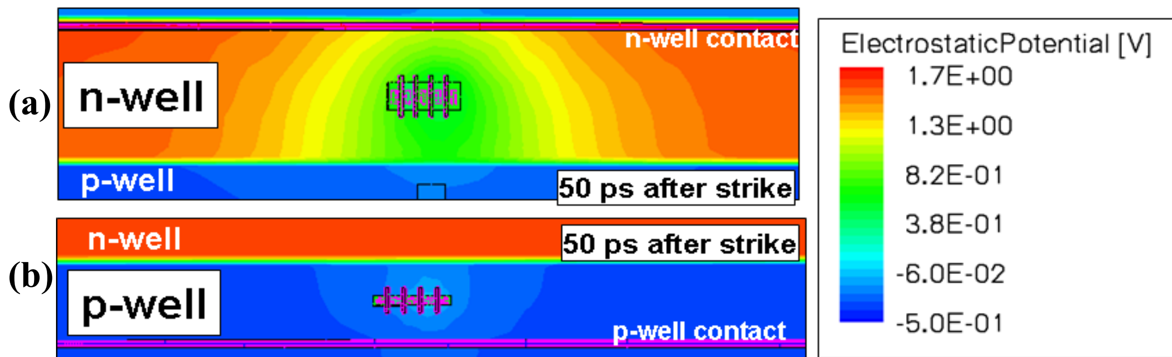

Fig. 22: (a) The potential in a 4-finger pFET and n-well 50 ps after a 40-MeV-cm^2/mg strike, (b) the potential in a 4-finger nFET and p-well 50 ps after a 40-MeV-cm^2/mg strike.

4.3 Varied drive strength with constant finger width

This section focuses on a typical method for increasing transistor width in which the finger width is kept constant while fingers are added. Using this method, illustrated in Fig. 23, a 1-finger device has 1x drive current, a 2-finger device has 2x drive, etc. The nFET finger width was 0.5 μm and the pFET finger width was 1.5 μm. Hence, in this section the 1x drive inverter refers to an inverter with a 0.5 μm wide nFET and a 1.5 μm wide pFET. Since each device had a different current drive, the complementary device compact model was appropriately scaled to keep the current matched. This is essentially a study of inverter size, with the increase in size achieved by folding.

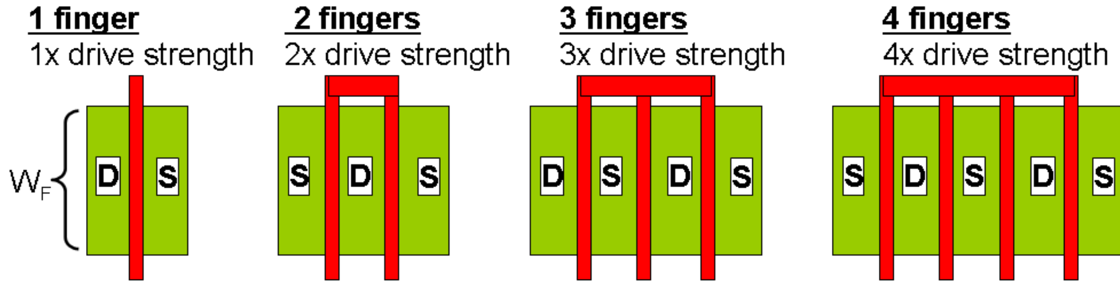

Fig. 23: Devices with 1 to 4 fingers with constant finger width. The total width of each device is simply $W = W_F$ x (Number of fingers).

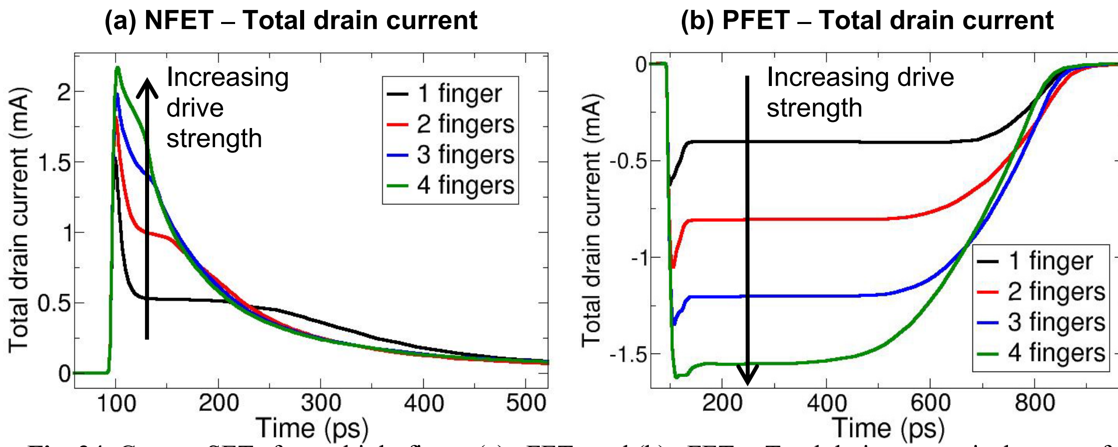

Fig. 24: Current SETs for multiple-finger (a) nFETs and (b) pFETs. Total drain current is the sum of the two drain currents in 3- and 4-finger devices. The number of fingers is proportional to inverter drive strength. LET = 40 MeV-cm^2/mg

Single events were simulated on both nFETs and pFETs to compare the responses. A normal, 40-MeV-cm^2/mg strike through the drain was simulated in each TCAD model in a mixed-mode inverter configuration. Figure 24 shows the nFET and pFET current transients of the device drains (the sum of two drain currents was used for 3- and 4-finger devices). The current transients show the effect of the increased drive strength. In Fig. 24(a) the nFET drain current shows less of a plateau as the drive increases, approaching a shape similar to a double exponential as the current becomes less limited by the complementary device. However, the pFET drain current in Fig. 24(b) shows a definite plateau that increases in magnitude as drive strength increases. The

width of the plateau decreases as drive strength increases. The difference between nFET and pFET is already apparent in the drain currents, i.e. the pFET current does not change shape while the nFET current does. For further comparison, the drain currents were integrated to compute collected charge, plotted in Fig. 25.

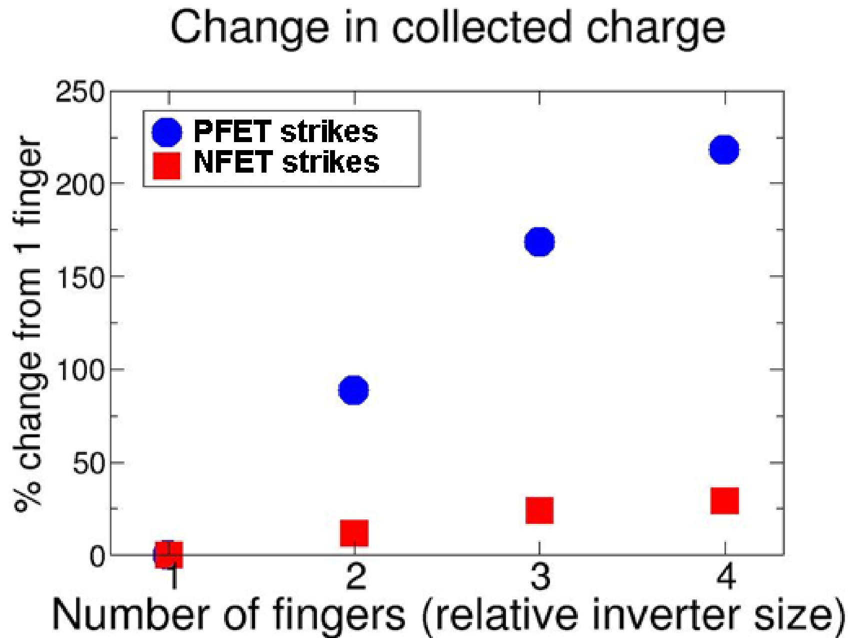

Fig. 25: Effect of increasing number of fingers on SE charge collection of nFETs and pFETs. The width of each finger is constant, so the number of fingers is proportional to inverter drive strength.

The collected charge of the pFETs increases dramatically (up to 220%) with inverter size, while the nFETs show a modest increase (up to 30%). As the struck device size increases, the complementary device also increases in size to maintain current matching in the inverter. As a result, the SE current is less limited by the restoring device, seen by the increase in plateau in Fig. 24. The higher current flow results in more collected charge in both nFET and pFET simulations. This is the sole reason for the increase in nFET collected charge with inverter size. Due to charge sharing and changing

pnp structures, increasing inverter size greatly increases pFET collected charge. Not only is the maximum current increased, but the larger pFET geometry allows for more charge collection.

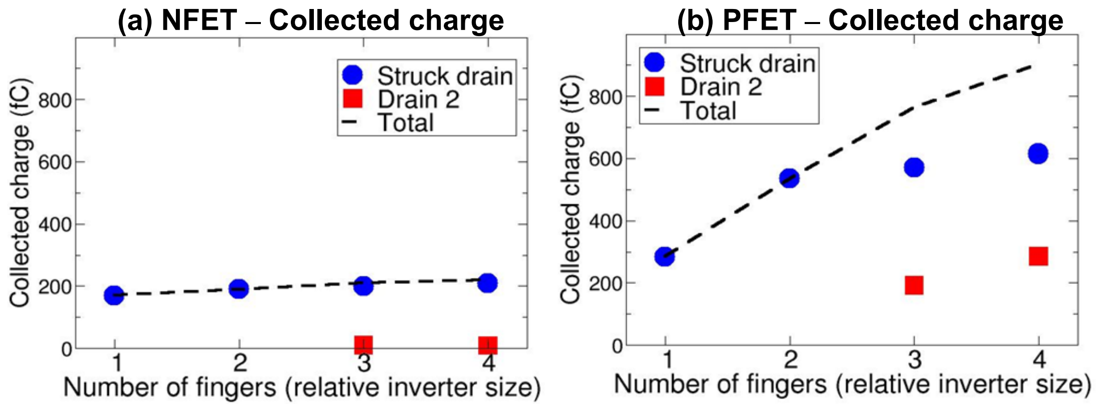

Fig. 26: Charge collected by struck drain and Drain 2 of multiple-finger (a) nFETs and (b) pFETs with constant finger width. There are no Drain 2 values for 1 and 2 fingers because there is only a single drain.

As in Section 4.2, charge sharing between device drains is an important factor in these simulations. As shown in Fig. 19, both the struck drain and the drain not in the ion's path (called Drain 2) can collect charge in these 3- and 4-finger devices. Figure 26 plots the charge collected by each drain along with the total collected charge for the n-hit and p-hit simulations. Drain 2 collects negligible charge in the nFET simulations, but it collects more than 25% of the total charge in the pFET simulations. This difference in charge sharing between drains was previously discussed in Section 4.2. The charge collection of Drain 2 helps explain why pFET-collected charge increases drastically with inverter size.

It is interesting to look at the voltage SET pulse width in these simulations not only because pulse width is a key concern in circuits but because it reveals a complex

interplay between collected charge and charge dissipation. Collected charge showed an increase with drive strength, but Fig. 27 shows that SET pulse width does in fact decrease with increasing drive strength. This, of course, is the expected result, since higher drive strength means a higher restoring current that can source or sink the SE charge more quickly. The decrease in pulse width indicates that the effect of faster charge dissipation dominates over the effect of increased charge collection; otherwise, pulse width would increase with drive strength.

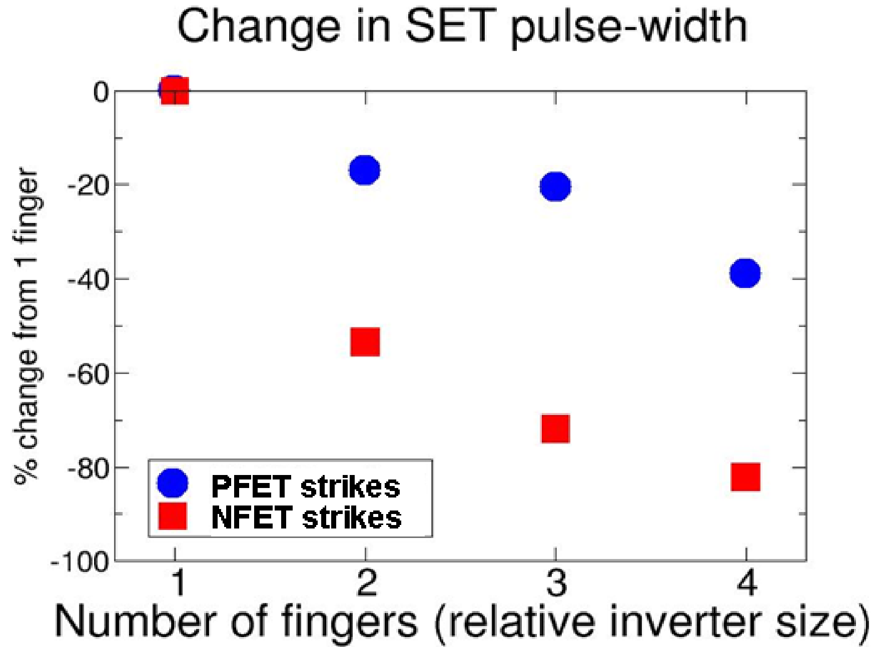

Fig. 27: Effect of increasing number of fingers on SET pulse width of nFETs and pFETs. The width of each finger is constant, so the number of fingers is proportional to inverter drive strength.

The different charge collection trends with inverter size of p-hits and n-hits result in different trends in pulse width. In Fig. 27 the n-hit pulse width decreased by nearly 80% when the inverter size increased by 4x. This dramatic reduction occurred because the collected charge only increased by 30%, while the restoring current increased by

300% (from 1x to 4x). The positive impact of the increase in restoring current is much greater than the negative impact of increased collected charge, so the pulse width decreases dramatically. Figure 27 shows that the p-hit pulse width decreased by only 40% for the same increase in inverter size. The 300% increase in drive current did dominate over the 220% increase in collected charge, but by a much smaller margin than seen with the n-hits. These results indicate that increasing device size by folding is much more effective for mitigating SETs in nFETs than in pFETs.

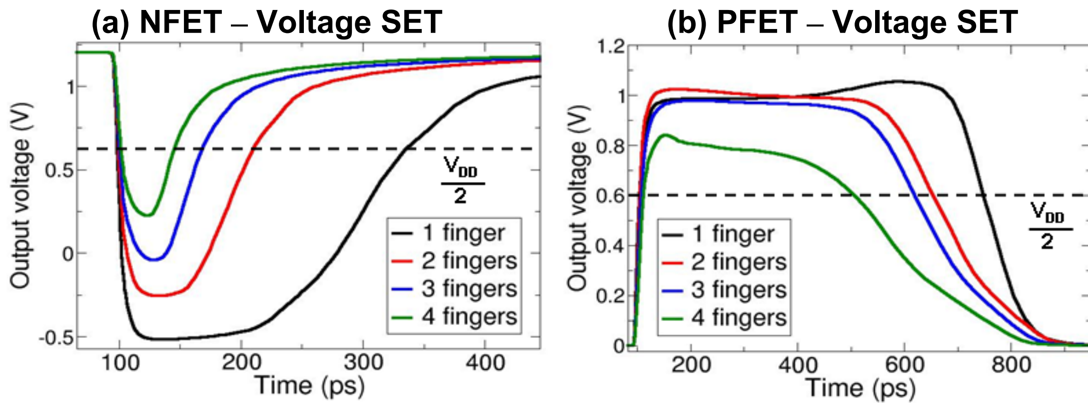

Fig. 28: Voltage SETs for (a) n-hits and (b) p-hits in current-matched inverters. The half-V_{DD} threshold of 0.6 V (used for FWHR pulse width) is shown as a horizontal dashed line.
(LET = 40 MeV-cm^2/mg)

Finally, the voltage transients in Fig. 28 allow for extrapolation to larger inverter sizes. The pulse widths were calculated using full-width half-rail (FWHR). In Fig. 28(a), the troughs of the n-hit pulses approach half-V_{DD} as the inverter size is increased. Similarly the peaks of the p-hit pulses in Fig. 28(b) approach half-V_{DD} as size is increased. Thus, it is reasonable to assume that at some inverter size both n- and p-hit pulses will not be of sufficient magnitude to change the logic state of the next stage. The 4-finger pFET has a total device width of 6 µm, which means a (W/L) of 75, and the W/L

of the 4-finger nFET is 25. It would require sizes even larger than these to fully mitigate these SETs.

4.4 Conclusion

In this chapter, the SE response of multiple-finger transistors was investigated. It was found that, when drive strength is kept constant, folding can increase p-hit pulse width by up to 20%, whereas n-hit pulse width can change by ±20% depending on the strike angle. The disparity between pFET and nFET results is due to the different well structures. Being relatively confined, the n-well voltage drops significantly after an ion strike and acts as a base in a parasitic pnp transistor. As a pFET is folded, the pnp structure changes and it exacerbates multiple-drain charge collection for normal and angled strikes. On the other hand, nFETs primarily collect charge through drift and diffusion, so multiple drains only collect charge from angled strikes.

The effect of increasing device size by folding was also investigated in both nFETs and pFETs. It was found that increasing inverter size by 4x reduced n-hit pulse widths by 80% while only reducing p-hit pulse widths by 40%. As before, this difference is due to the bipolar amplification of charge in the pFET, which causes collected charge to increase dramatically with inverter size. Since the nFET-collected charge shows only a modest increase with inverter size, the pulse widths are greatly reduced as inverter size increases.

The trends described in this chapter are strongly process-dependent. The disparate nFET and pFET trends are consequences of the dual-well structure used in this library. The isolation of the n-well causes the n-well to collapse and trigger the parasitic

bipolar device, which is one of the most significant effects in the single-event response of pFETs. For example, in a triple-well process the p-well is isolated in a manner similar to the n-well. The confinement of majority carriers in their respective wells causes both the n-well and p-well to experience significant voltage perturbation during a single event. The perturbation of well voltage causes significant bipolar amplification of SE charge in both nFETs and pFETs in a triple-well process. In the dual-well process, only the pFETs experience significant bipolar amplification of charge. Thus, in a triple-well process, the SE response trends in multiple-finger nFETs and pFETs would be similar.

CHAPTER V

CRITICAL FACTORS IN SINGLE-EVENT RESPONSE OF DIGITAL CELLS

To perform a single-event characterization of a digital cell library, it is first necessary to understand the factors that determine a cell's SE response. In this chapter, TCAD simulation is used to investigate three different factors: drain area, restoring current, and n-well contact scheme. The drain area of a MOSFET affects the amount of charge collected during a single event because the drain area is essentially the area of the sensitive reverse-biased junction that collects charge. The restoring current during a single event is the current provided by the circuit to source or sink the SE charge that is collected. For example if the pFET is struck in an inverter, the nFET provides the restoring current to sink the SE charge. The restoring current controls the rate of charge removal and, thus, dramatically impacts the SE response of a logic cell. Finally, the parasitic pnp device in a pFET is turned ON by the n-well voltage collapse following an ion strike, and the n-well contacting scheme governs the duration of the n-well collapse. Consequently, the n-well contact area and the distance between well contact and pFET are important parameters concerning the duration of SETs generated in pFETs. The critical factors identified in this chapter will be used to perform the SE characterization discussed in Chapter 6.

5.1 Diode area

Before investigating SE charge collection in a MOSFET, it is beneficial to investigate a simpler case, a diode. In this section, heavy ion simulations were performed on a p+/n-well diode to understand the effect of diffusion area on charge collection. The p+ diode was simply a pFET drain with the source and gate regions removed, to enable later comparisons to pFETs. The diode is surrounded by STI to more closely match the structure of an actual device. Fig. 29(a) shows a layout view of the diode. The y dimension of the p+ region was fixed at 0.84 μm, to match the pFET width in the 1x inverter used throughout this study. The x dimension (labeled "L_d") was varied from 0.27 μm to 1.62 μm in order to see how diode area effects the SE charge collected. The diode area is simply the product of L_d and 0.84 μm.

Figure 29(b) shows the cross-section of the diode model, taken from the cut line in Fig. 29(a). The anode of the diode is connected to a pull-down nFET with W = 280 nm and L = 80 nm. The nFET is a compact model simulated in Spice while the diode is modeled in TCAD, so the heavy ion simulations are mixed-mode. The nFET is ON, so the anode is biased low and the n-well contact is biased high, creating a reverse-biased junction. The simulation is basically a 1x inverter with HIGH input, with a reverse-biased diode instead of an OFF pFET. This eliminates any bipolar effects due to the p-source, while keeping the current-limiting effects of a complementary transistor.

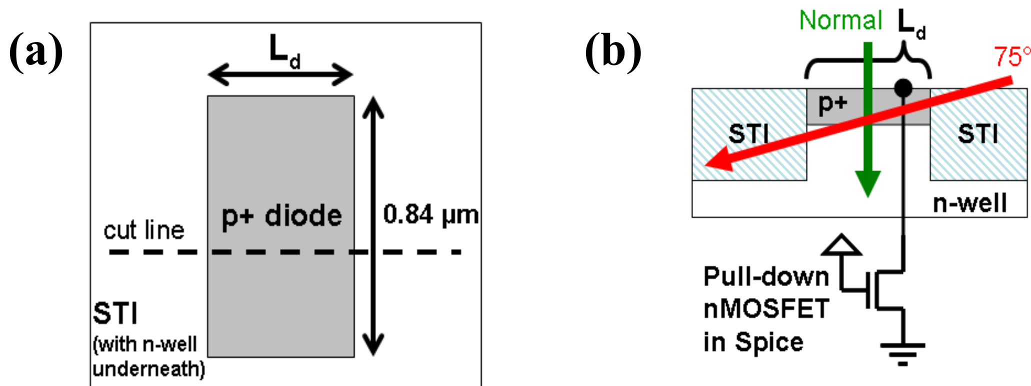

Fig. 29: (a) Layout view of p+/n-well diode with fixed width and variable length L_d (b) Cross section of p+ diode showing two different strikes of mixed-mode TCAD simulation. A compact model nFET is shown connected to the anode, which is biased low.

The two simulated strike paths are illustrated in Fig. 29(b). The green arrow shows the path of the normal strike with entry point 140 nm from the right edge of the p+ diffusion. The blue arrow shows the strike angled at 75° to normal, with entry point always 200 nm from the diffusion edge. The strikes were first simulated with LET of 5 MeV-cm^2/mg, and the resulting collected charge is plotted against diode area in Fig. 30.

The results indicate a positive correlation between charge collection and diode area. With larger area, more carriers can be swept into the p+ region, resulting in more collected charge. There is a notable difference between the two strikes, other than the magnitudes. The normal strikes show very little variation in collected charge with respect to diode area; however, the 75° strikes show variation from 12 to 50 fC, a 317% increase. The effect of area on collected charge is largely absent for normal strikes because the path of the strike through the diode is identical in all cases.

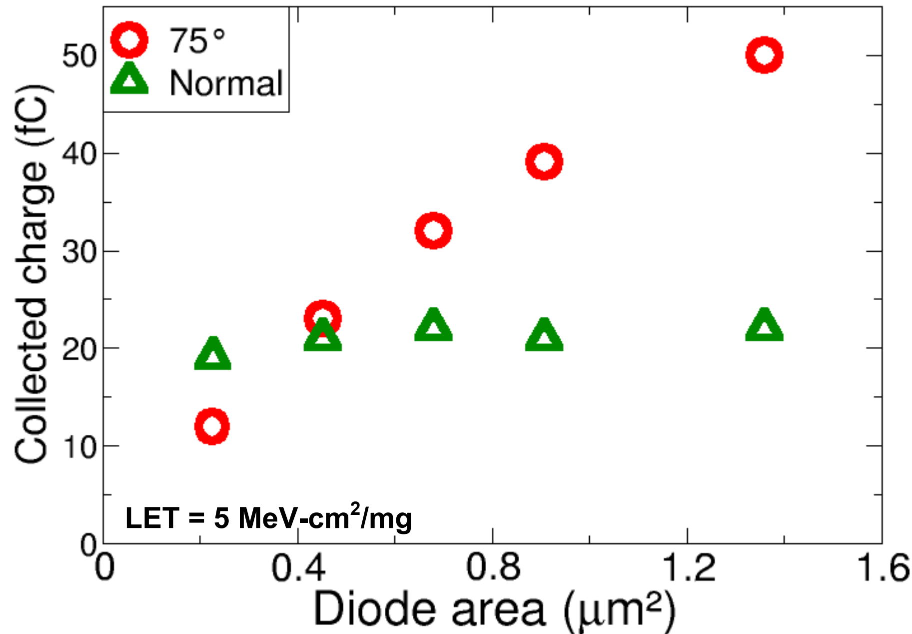

Fig. 30: SE collected charge vs. diode area for normal and 75° strikes with LET = 5 MeV-cm^2/mg

Diode area significantly changes the charge collected from a 75° strike for two reasons. The first is the increased collection area of the reverse-biased junction. Since the grazing-angle strike deposits charge along the plane of the junction, more charge is collected when the junction area is larger, unlike the normal strike. The second reason for the trend is the change in the strike's path length through silicon. Because the p+ diffusion is surrounded by STI, the high angle strike's path length is limited by the distance between STI regions. As the diode is stretched in the horizontal dimension, the strike is able to transfer energy to more silicon, thus depositing more charge. Therefore, as diode area increases both charge deposition and collection increase.

In Section 3.1, it was determined that charge collected at the n-well contact is indicative of the charge deposited, since all deposited and separated electrons are collected by the n-well. In Fig. 31 the charge collected by the n-well contact is plotted

against diode area for both normal and 75° strikes. For normal strikes the n-well-collected charge is nearly constant, within 2 fC of 81 fC. However, the lower four values of the 75° set increase linearly from 239 fC to 279 fC. This linear trend is because the path length increases with L_d by a factor of $1/\sin(75°) \approx 1.04$, and the x-axis area is simply L_d x 0.84 μm. The highest charge value of 286 fC shows a break in the linear trend because the distance between STI regions is such that the strike does not pass through the left STI region, but under it. Since charge collected by the n-well contact indicates deposited charge, this plot demonstrates the increase in deposited charge with increasing diode area.

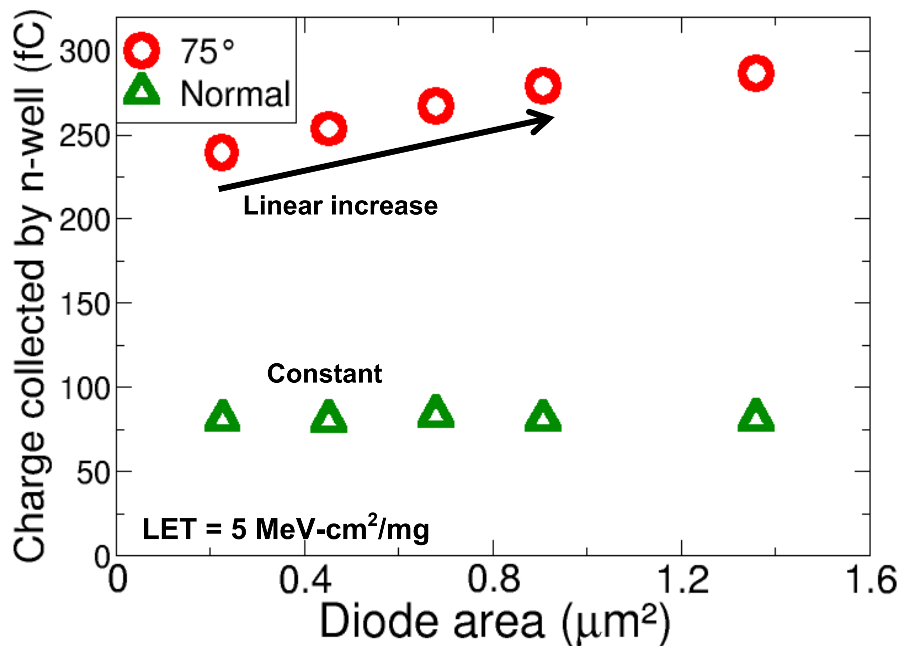

Fig. 31: SE charge collected by n-well vs. diode area for normal and 75° strikes with LET = 5 MeV-cm^2/mg

In order to further understand these trends, the same diode structure was simulated without the STI immediately around the p+ region. This structure, shown in

Fig. 32, eliminates the dependence of deposited charge on diode area, i.e. the same amount of charge is deposited for all diode areas; only the amount of charge collected by the diode changes. The same 75° strikes were simulated as before, but, unlike before, the n-well-collected charge (which indicates the deposited charge) was 294 fC for all simulations. Fig. 33 shows the plot of charge collected by the p+ diode vs. diode area for simulations both with and without STI.

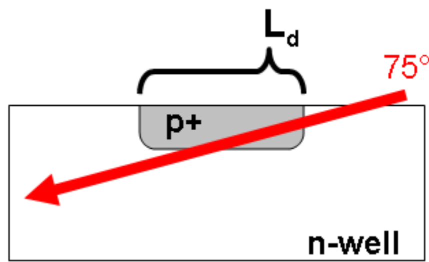

Fig. 32: Cross section of p+/n-well diode structure without STI immediately on each side. The 75° is not limited by the STI in this case.

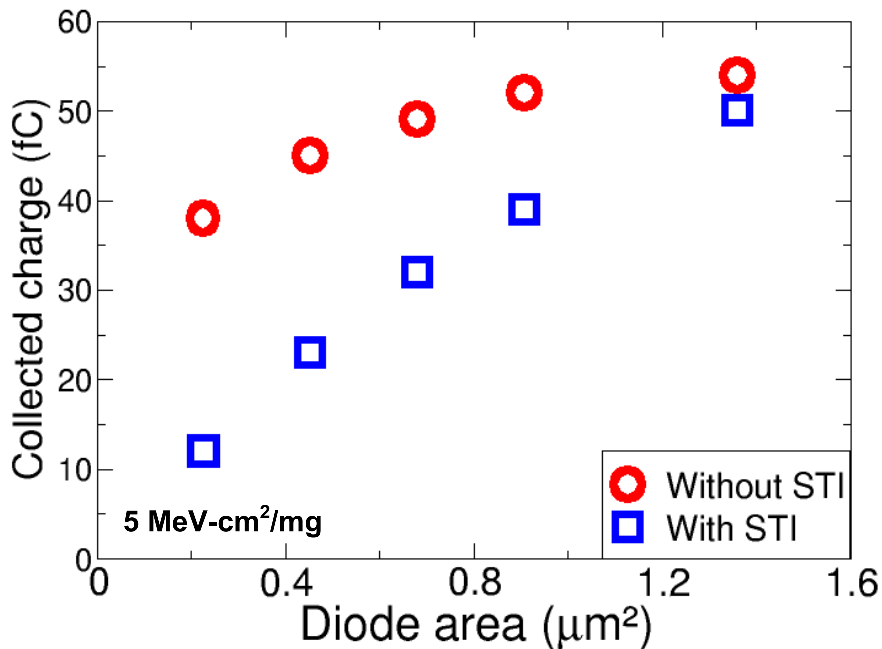

Fig. 33: SE collected charge vs. diode area for 75°, 5-MeV-cm^2/mg strikes on a p+/n-well diode with and without STI surrounding it. The "With STI" set is identical to the 75° set in Fig. 30.

The red circles in Fig. 33 show the new simulations in which deposited charge is the same for all diode areas, and the blue squares show the simulations from Fig. 30. First, it is important to note that without the STI the strike was able to deposit more charge, so the collected charge was higher without STI than with STI. Beyond the magnitude difference, the trends of the two plots are quite different. With STI, the collected charge shows over 300% increase from the smallest to the largest diode. Without STI, the same change in diode area causes only a 42% increase in collected charge. This shows that increasing diode area does result in greater charge collection purely due to the larger junction area (sensitive area) that can collect charge. However, in the usual case where STI is present, the charge deposition is limited by the volume of silicon between STI regions. In this case, the variations in strike path length dominate the correlation between diode area and collected charge. The charge deposition in each of the two cases is illustrated in Fig. 34. In Fig. 34(a), the number of carriers liberated (or charge deposited) by the ion is proportional to L_d, while the number of liberated carriers is independent of L_d in Fig. 34(b).

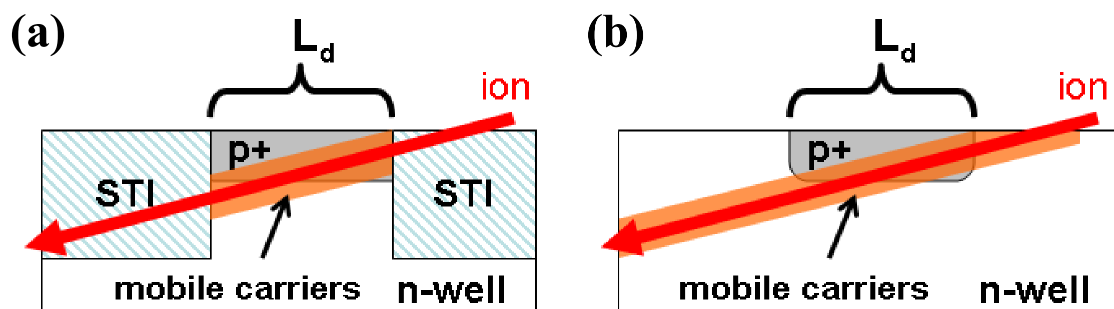

Fig. 34: (a) Cross section of diode surrounded by STI showing mobile carriers liberated by 75° ion strike. The charge deposition is truncated by the STI so increased L_d in (a) results in greater charge deposition. (b) Cross section of diode without STI showing mobile carriers liberated by 75° ion strike. The total charge deposition is unaltered by changes in L_d, so changes in L_d in (b) exclusively change the amount of charge collected by the diode.

5.2. Drain area

In this section the study of diode area is extended to pFETs by investigating the effect of drain area on SE response. In normal circuit operation the primary effect of drain area is on the transistor's parasitic capacitance, i.e. switching speed. However, in the case of a heavy ion strike, these parameters could potentially affect the charge collected by a device. Previous diode simulations indicate that drain area would likely affect the charge collected from angled strikes but not from normal strikes. To investigate this, ion strikes were simulated on the pMOS device model with varied drain area.

Figure 35(a) shows the cross section of the device, with the source and drain lengths labeled 0.32 μm and L_d, where 0.32 μm is the length of the source and L_d is the length of the drain diffusion, respectively. The device width is held constant at 840 nm, so the drain diffusion area is simply the product of L_d and 840 nm. Figure 35(b) shows the same cross section, but with the three different strike paths shown. The red arrow labeled "Towards source" enters the STI at a point 200 nm from the drain edge; this entry point moves as the drain size changes. The blue arrow labeled "Away from source" passes through the drain from the source side of the device; this entry point is identical for all device geometries. Both of these strikes are angled 75° to normal incidence. The green arrow shows the normal strike, which always passes through the drain at a point 160 nm from the gate. The "Away from source" and "Normal" strikes are identical to those simulated in the previous section. The pFET in TCAD is connected to a compact model nMOS with width 280 nm in Spice to simulate a current-matched inverter in mixed-mode.

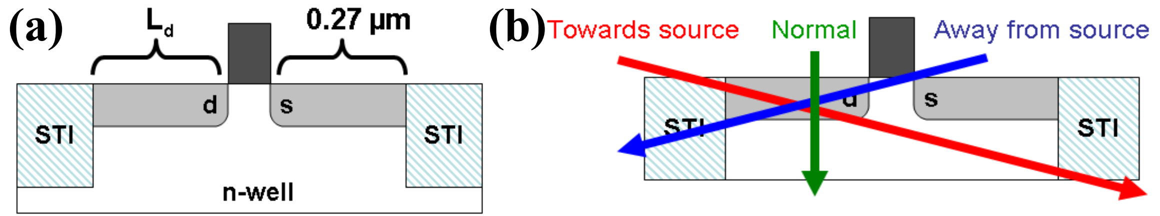

Fig. 35: (a) Cross section of pMOS device showing variable L_d (b) Cross section of pMOS device showing three different strikes. Both strikes towards and away from source are at 75°. The "Towards source" strike entry point moves to the left as L_d increases; the "Normal" and "Away from source" strikes are identical for all drain areas.

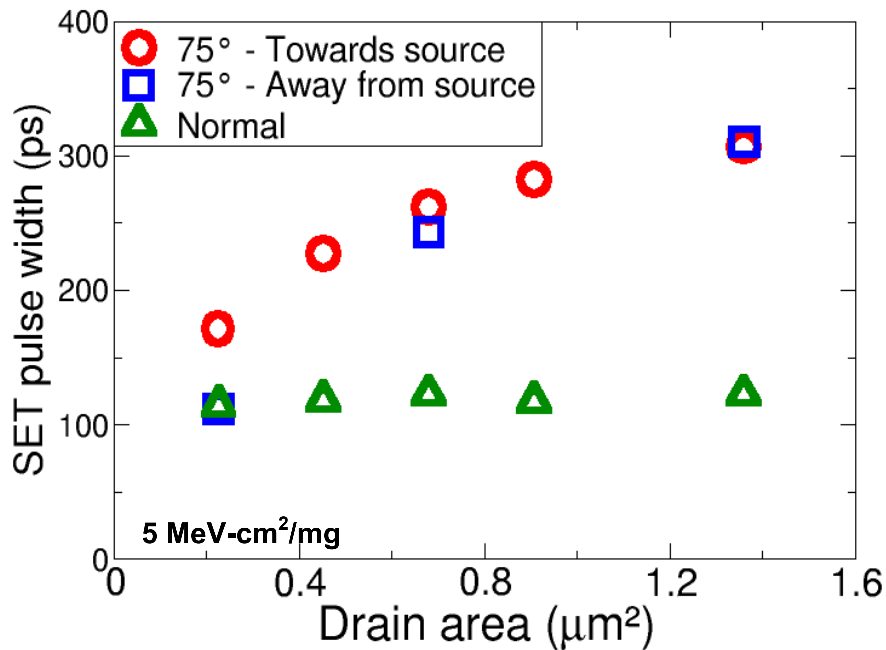

Fig. 36: SET pulse width of pFET with varied drain area. Strikes were with LET of 5 MeV-cm^2/mg.

Simulations are performed that vary the drain area while keeping the source area constant at 0.27 µm x 0.84 µm ≈ 0.23 µm^2. Figure 36 shows the SET pulse widths from the three different strikes at LET of 5 MeV-cm^2/mg as a function of drain area. Both of the 75° strikes show an increase in pulse width with drain area (as before, the 75° stike enters 200 nm from the edge of the diffusion for each size of drain area). The "Towards source" plot shows an 80% increase in pulse width when drain area increases from 0.23

μm^2 to 1.4 μm^2, and the "Away from source" plot shows a 180% increase for the same change in drain area. Conversely, the "Normal" pulse widths show no appreciable change across drain area. This is similar to the trend between collected charge and diode area in Section 5.2. The charge deposited by the angled strikes increases with drain area because the strike path length increases, and the charge collected by the drain increases because the charge is deposited along the plane of the junction.

Note on source area:

The effect of source area on SET pulse width is not as dramatic as that of drain area. During a pFET strike, the source functions as the emitter of the parasitic bipolar transistor, as described in Chapter 3 and as shown in Fig. 8. With the drain functioning as collector, the lateral pnp structure causes amplification in the drain-collected charge which largely determines the pulse width. The geometry of this lateral BJT does not change as the source area is increased; the only designer-controlled parameters to alter the lateral pnp structure are the channel width and length. However, the vertical pnp structure (with the buried p-well as collector, Fig. 8) does depend on the source area. Thus, increasing the source area would increase the holes collected by the p-well. In summary, since the lateral BJT primarily controls the drain-collected charge and does not depend on source area, the effect of source area on SET pulse width is minimal.

5.3 Restoring current

Single-event response is not only determined by parameters of the the struck device, but by the rest of the circuit as well. The restoring current during a single event is

the current provided by the circuit to source or sink the SE charge that is collected. In this section, the effect of restoring current on SE response is examined. Mixed-mode inverter simulations were performed which model the struck pFET in 3-D TCAD and the pull-down nFET in Spice. The pFET TCAD model is unchanged while the n-channel width is varied to change the restoring current to the pFET. The results show that restoring current is an extremely critical factor in a cell's SE response.

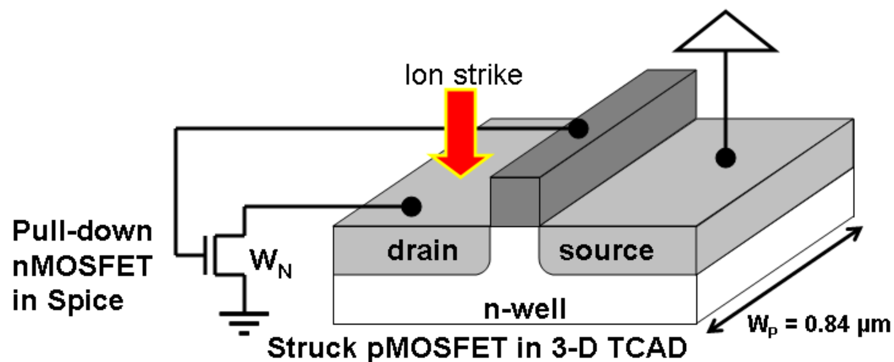

Fig. 37: Simulation setup of mixed-mode inverter with variable nFET width W_N

Figure 37 shows the simulation setup used for p-hits in a mixed-mode inverter. The compact model nFET has a variable width that is proportional to the restoring current to the struck device. The pFET width is 840 nm, and the strike is at normal incidence through the center of the drain, with an LET of 40 MeV-cm^2/mg. The resulting drain current SETs are shown in Fig. 38. As W_N increases from 0.2 µm to 1.12 µm, the current plateau changes magnitude and duration. The plateau magnitude is simply the drive current of the pull-down nFET, and the plateau duration changes because the current determines the rate of SE charge removal [21]. For nFET widths of 1.12 µm and 2.24 µm, the current shape is similar to the double-exponential seen in the "Unloaded" curve,

obtained by tying the pFET drain directly to ground. The plateau effect is not seen at very high drive currents because the the SE current is smaller than (and, thus, not limited by) the nFET saturation current.

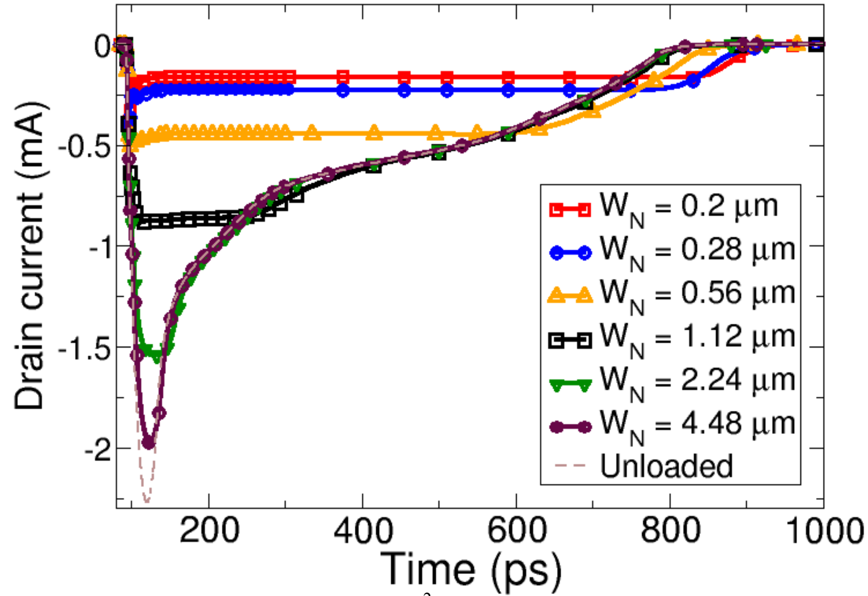

Fig. 38: Current SETs resulting from 40-MeV-cm^2/mg p-hits in mixed-mode inverter with variable pull-down nFET width W_N. "Unloaded" indicates that the pFET drain was tied directly to ground.

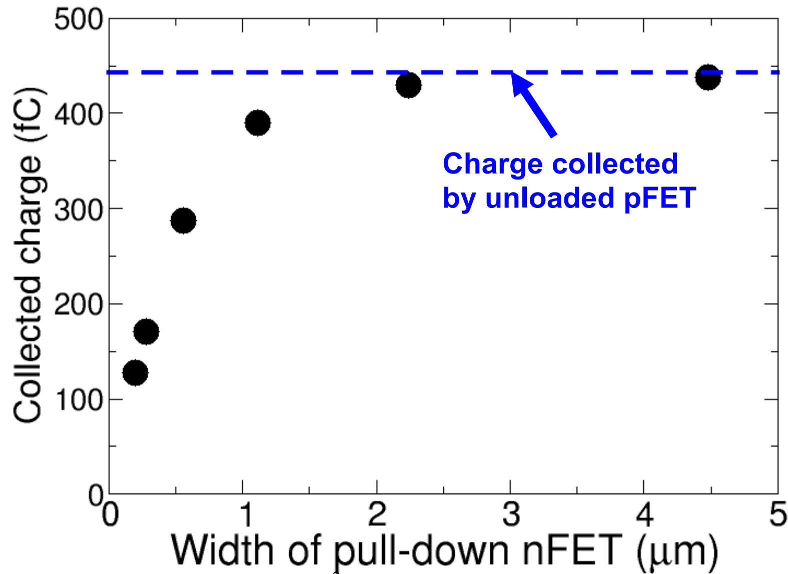

Fig. 39: Charge collected from 40-MeV-cm^2/mg p-hits in mixed-mode inverter with variable pull-down nFET width W_N. Charge collected by unloaded pFET with drain tied to ground shown in blue.

Next, each of the current transients in Fig. 38 was integrated to compute collected charge. The collected charge is plotted as a function of nFET width, which is proportional to restoring current, in Fig. 39. Although the struck device is identical in all simulations, the collected charge shows large variations when the pull-down nFET width is changed. However, this result makes intuitive sense when the transients in Fig. 38 are examined. When the restoring current is increased, more charge is collected from the struck device at a given time, shown by the increasing magnitude of current in Fig. 38. Thus, the total charge to exit the pFET drain increases when the restoring current increases. In fact as the nFET width increases, the collected charge in Fig. 39 appears to asymptotically approach the charge collected by the unloaded pFET. If collected charge were the primary metric in comparing the SE response of these different configurations,

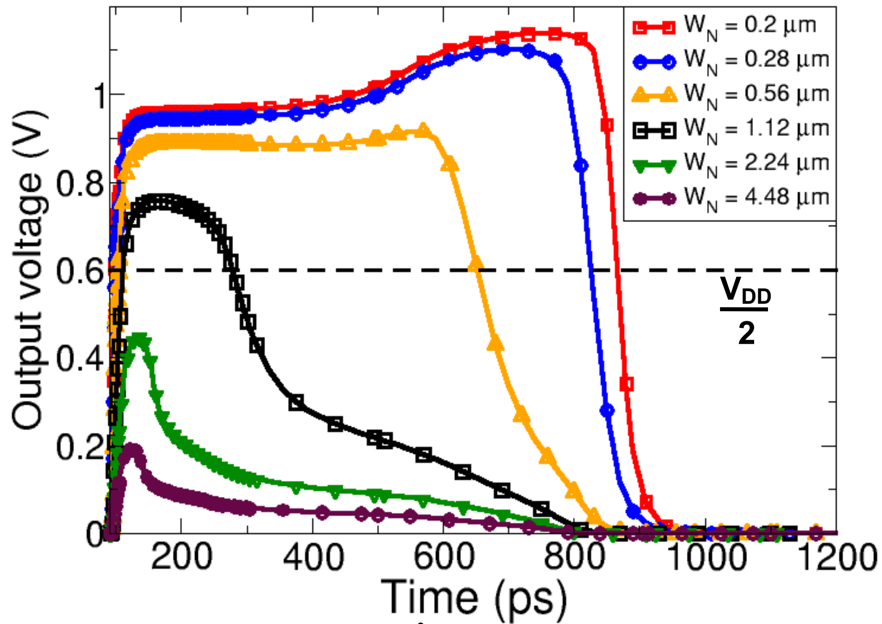

Fig. 40: Voltage SETs resulting from 40-MeV-cm^2/mg p-hits in mixed-mode inverter with variable pull-down nFET width W_N.

then the response would appear to worsen by increasing restoring current. However, the voltage SETs in Fig. 40 clearly show how the response is improved by increasing restoring current.

In Fig. 40, the voltage pulses decrease in both magnitude and duration as the restoring current increases. For example, doubling the nFET width from 0.28 μm to 0.56 μm reduces the FWHM pulse width by 25%, and doubling the nFET width again reduces the pulse width by 70%. At W_N values of 2.24 μm and above the voltage transients do not reach the half-V_{DD} line shown, making it highly unlikely that these transients will propagate through any logic gates. Figure 41 shows the decreasing trend of the FWHM pulse width with increasing n-channel width. The mixed-mode inverter is current-matched when W_N = 0.28 μm, so significant SET mitigation is achieved when the

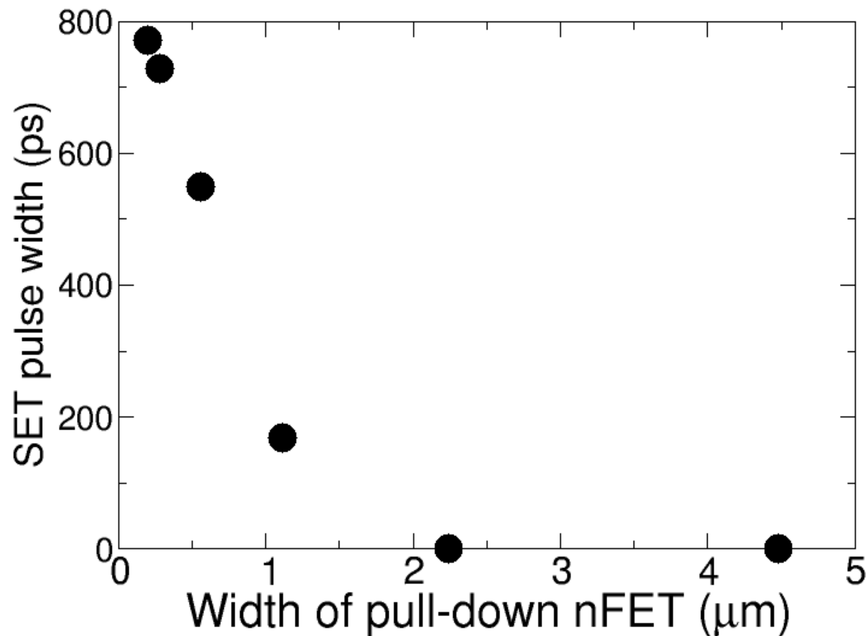

Fig. 41: FWHM pulse widths of voltage SETs resulting from 40-MeV-cm^2/mg p-hits in mixed-mode inverter with variable pull-down nFET width W_N. A pulse width of 0 ps indicates the voltage transient did not reach the half-V_{DD} threshold.

inverter is made to be rather n-heavy, because the larger nFET increases the rate of removal of SE charge. An n-heavy inverter mitigates the duration of p-hit SETs, which are typically much longer than n-hit SETs [21].

5.4 N-well contact area and location

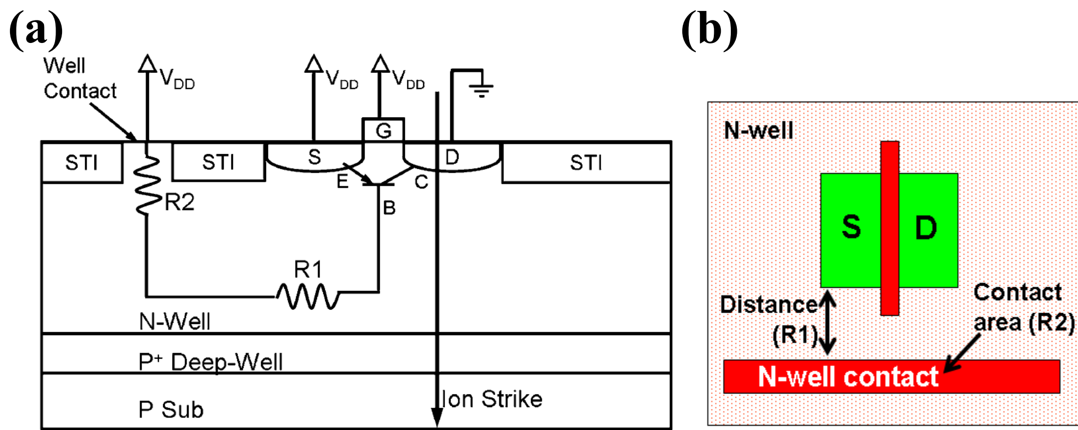

Fig. 42: (a) Cross section of pMOS device showing schematic representation of parasitic bipolar device and base resistances; after [22]. (b) Layout of pFET and n-well contact showing components of n-well base resistance

Past studies have indicated that the n-well contacting scheme can greatly affect the SE response of a pFET [21]-[22]. As described in Chapter 3, the n-well acts as the base of the parasitic bipolar device shown in Fig. 42(a). The two resistances R1 and R2 indicate how effectively the n-well is contacted. R1 is the horizontal resistance between the base region near the pFET and the well-contact to V_{DD}. This is controlled by the distance from the well contact to the pFET, shorter distance yielding lower resistance. R2 is the vertical resistance from the bulk of the n-well to the top of the n-well contact. This is controlled by the n-well contact area, larger contact area yielding lower resistance,

as well as the doping profile of the n-plus contact diffusion. A simple layout showing the parameters controlling these resistances is depicted in Fig. 42(b). Lowering either of these well resistances mitigates the collapse of the well potential by giving excess carriers a less resistive exit path to V_{DD}. [21]-[22]

Figures 43(a) and (b) from [21] show how SET pulse width varies with n-well contact area and distance, respectively. As expected, pulse width decreases as contact area increases, due to the decrease in R2. Similarly, pulse width decreases as contact distance decrease, due to the decrease in R1. When considering the variations in a cell library, the n-well contact area is typically the same for all cells. In the cell library that is characterized in this work, the well contact area, and hence R2, is identical for all cells. However, the distance between pFET and n-well contact does vary from cell to cell, so R1 is variable. The n-well is only 2 μm wide (vertical dimension of Fig. 42b), so the contact distance varies between approximately 0.3 μm and 0.9 μm. Based on the results

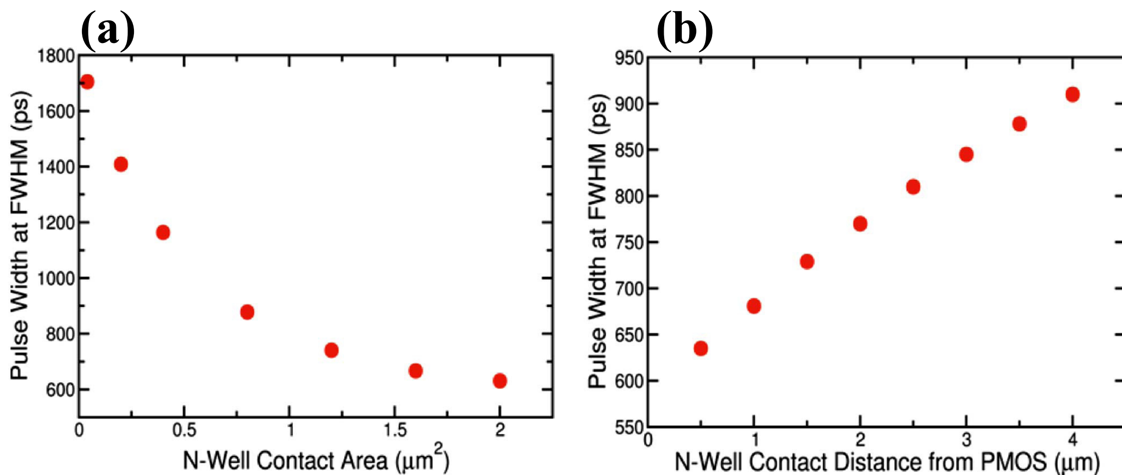

Fig. 43: (a) Effect of n-well contact area on SET pulse width. This shows how R2 influences the pFET SE response; after [21]. (b) Effect of n-well contact distance on SET pulse width. This shows how R1 influences the pFET SE response; after [21].

in Fig. 43, a 0.6 μm change in well contact distance yields a ~7% change in pulse width. In general, well contact area and distance have a strong effect on pFET SE response, but in the scope of a digital cell library, there is little or no variation in these parameters.

5.5 Conclusion

Drain area, restoring current, and n-well contacting scheme have been identified as critical factors of SE response of digital cells. The two processes affected by drain area are charge deposition and charge collection. Charge deposition of a grazing-angle strike can be altered by drain area if the STI boundaries truncate the ion's path length. The amount of charge collected by a sensitive drain is partially determined by the area of the reverse-biased drain/n-well junction. For normal-incident strikes, these effects are not observed, and collected charge and pulse width are insensitive to drain area. A struck device's restoring current is set by the complementary device, and this current is the rate at which SE charge can be removed from the node. Therefore, there is negative correlation between restoring current and SET pulse width. Both drain area and restoring current vary widely within a cell library, but the n-well contacting scheme, which directly affects bipolar amplification of SE charge in p-hits, shows little or no variation. The n-well contact area is identical for all cells and the distance from pFET to n-well contact varies by 0.6 μm at most. This variation can cause a ~7% change in pulse width, so it is not a determining factor when comparing the SE responses of different cells. In the next chapter, these critical factors are used to perform a worst-case characterization of the SE response of the digital cell library.

CHAPTER VI

SINGLE-EVENT CHARACTERIZATION OF A 90-NM BULK CMOS DIGITAL CELL LIBRARY

This chapter describes the basic methodology and results of the characterization of single-event transients in a 90-nm bulk CMOS RHBD digital cell library containing approximately 500 cells. Worst-case single-event transients are identified and parameterized in the logic cells using TCAD. The results give insight into single-event sensitivities of complex logic cell design.

For advanced integrated circuit technologies, complex mechanisms related to charge collection after a single-event hit necessitate the use of 3-D finite element (or TCAD) simulations for accurate prediction of single-event performance. Such 3D simulations are very time- and computing-resource intensive, often requiring tens of hours for one single-event simulation. The task is even more challenging when evaluating a digital cell library, rather than a single device or digital cell, due to the large number of cells, device sizes, and possible circuit conditions (e.g., input states) that need to be simulated for complete vulnerability coverage.

The 90-nm radiation–hardened-by-design (RHBD) cell library considered in this work was characterized under support provided by DARPA and DTRA. The library is implemented in the IBM 9SF bulk CMOS process and contains over 500 cells, from a minimum-size inverter to complex latches and adders. Standard TCAD single-event (SE) simulation on all device and circuit variants for all the cells is difficult or impossible to

complete within a reasonable time because of the number of cells and possible single-event test cases. By focusing on worst-case single-event transients (SETs), based on known critical factors and parameterized trends in SET characteristics for the baseline technology, the single-event library characterization is simplified and the total single-event simulation time reduced to a manageable level. This method is presented along with simulation results showing worst-case SE sensitivity comparison of all logic cells.

6.1 Worst-case SET simulation setup

The evaluation of what contributes to a "worst-case" single event pulse of long duration involves several characteristics of both the strike and the device. As described in Chapter 4, ion strikes on pFETs produce longer SETs than strikes on nFETs due to parasitic bipolar amplification in the pFET structure. This is also seen in initial simulations of basic library cells in this library, such as inverters and NAND gates. Next, simulations were performed that vary the angle and location of a p-hit on a balanced inverter where n- and p-channel transistor drive currents are equal. The longest voltage pulse widths on cell outputs are observed with strike angle of 75° to normal incidence, and with strike direction longitudinal to the n-well long axis (higher angles produced little change). We found that the SETs produced at this angle are longest when the strike enters from outside the sensitive drain (the output node) and passes through the drain region such that the strike path length through active silicon is as long as possible (Fig. 44a).

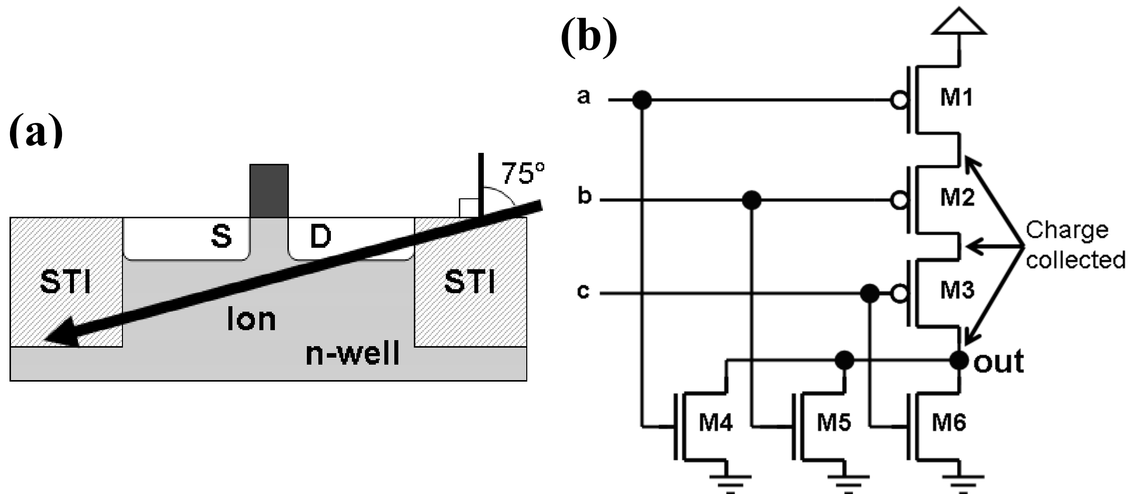

Fig. 44: (a) Worst-case pFET strike at 75° along n-well, (b) Schematic of 3-input NOR gate, showing nodes that collect charge in worst-case input state

Having identified the worst-case strike parameters for an individual transistor, the next step is to determine the worst-case circuit input state for the cell, i.e. the logic state of a circuit that results in the longest SET. Simulations on NAND and NOR gates revealed that the longest SETs are produced for p-hits when the input state minimizes nMOS pull-down current. The pull-down current is responsible for restoring the hit-node voltage to the original logic state, as described in the previous chapter. Additionally, the number of p-channel transistor drains connected to the hit node determines the number of sensitive drains that can collect charge from an ion strike.

To illustrate these concepts, a 3-input NOR gate is shown schematically in Fig. 44(b). The worst-case input for this circuit is a = ‘1’, b = ‘0’, and c = ‘0’. The only nFET that draws current is M4, so the restoring current is minimized. With pFETs M2 and M3 ON, they electrically connect three pMOS drain nodes together, maximizing the composite drain area that can collect charge from the strike. Using these two concepts,

worst-case input states are determined a priori for all the cells. All simulation results presented below for this library characterization use these worst-case parameters.

6.2 Simulation results and discussion

The simulation methodology was used to generate a table of worst-case SET pulse widths as a function of LET for different library cells. Such results are useful for circuit designers as it allows a direct comparison of SE sensitivity of different logic structures. For more complex circuit structures (in this case, a particular ALU design of interest to the sponsor), cells were selected for characterization based on frequency of usage in the particular design architecture. All the simulated library cells were divided into four categories: inverters, NAND cells, NOR cells, and combinational logic cells (Boolean functions). Multiple versions of each cell exist in the library with different size scale (driving factor) or number of inputs. For example, inverter cells with 1X, 2X, 3X, 4X, 6X, and 8X drive strengths are in the library, and there are 1X drive NAND gates with 2, 3, and 4 inputs. Using post processing of simulation data from each cell type, the mean worst-case pulse width of each cell group is plotted as a function of LET in Fig. 45. Since the pulse widths are interesting from a cell comparison standpoint, they are normalized by the maximum value on the plot.

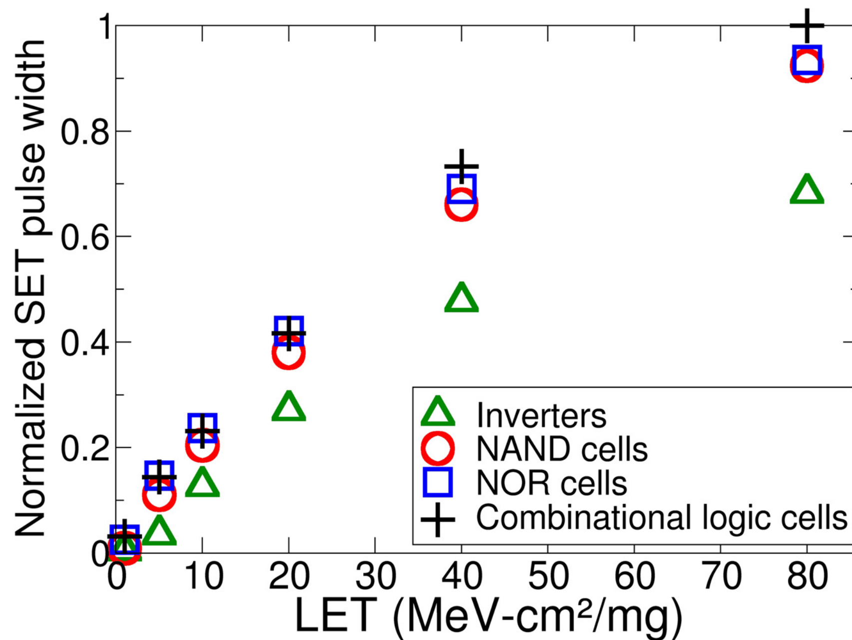

Fig. 45: Mean worst-case pulse widths of each cell group normalized to the maximum value on the plot (Note: a pulse width of 0 indicates the voltage transient did not rise up to V_{DD} / 2 = 0.6 V)

Comparison of different cell types

The most striking difference in pulse widths of the cell types shown in Fig. 45 is between the inverters and the rest of the cells. This is largely due to the relative differences in sensitive area and current drive, the critical factors discussed in Chapter 5. Sensitive area, in this case, refers to the total area of the reverse-biased p-drain/n-well junctions that collect charge from an ion strike. Current drive is the rate at which the pull-down nFETs can dissipate the charge collected by the pFETs, since p-hits are considered. The pull-down current of inverters scales directly with size, since there is a single nFET. However, the pull-down current of a NAND gate scales more weakly with size since there are two or more stacked nFETs, reducing the current that passes through them. The sensitive area of a NOR gate is larger than that of a NAND gate or inverter because of the series-connected p-channel transistors. As Fig. 44(b) illustrates, an ON p-

channel can electrically connect the drains of series-connected devices, increasing the area that can collect charge from an ion strike. The sensitive area in this case is the sum of these drain areas that can collect charge. Finally, the combinational logic cells have both NAND and NOR structures in the pull-up and pull-down networks, so they exhibit both the low current drive of a NAND gate and the large sensitive area of a NOR gate. In fact, the worst-case input state was chosen to make these cell-level differences more pronounced.

This analysis indicates that the inverter has the optimal combination of current drive and sensitive area to obtain a short single event pulse, since only a single complementary pair is involved. Thus, the inverters consistently show the shortest SETs in these simulations. Due to the complex interplay of sensitive area and current drive in the other cell types, their relative SE sensitivities fluctuate, although the combinational logic cells and NOR cells appear to have the worst responses.

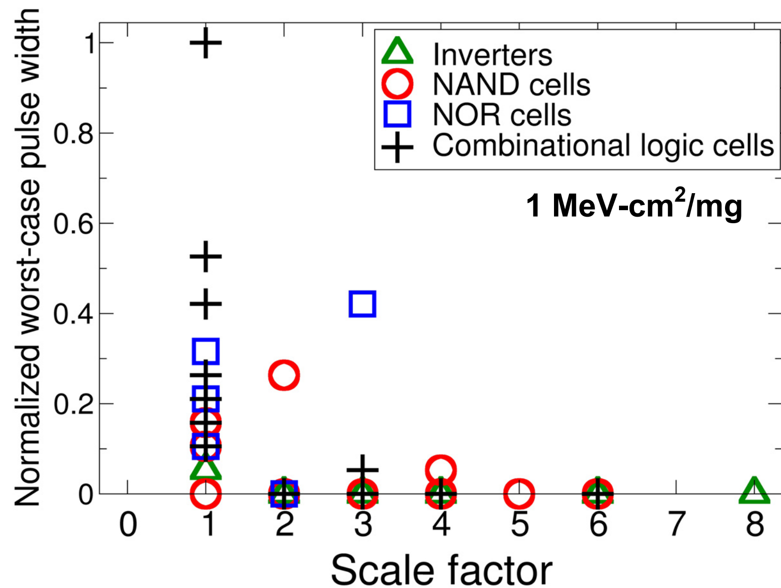

Fig. 46: Normalized worst-case SET pulse width as a function of scale factor, LET = 1 MeV-cm^2/mg

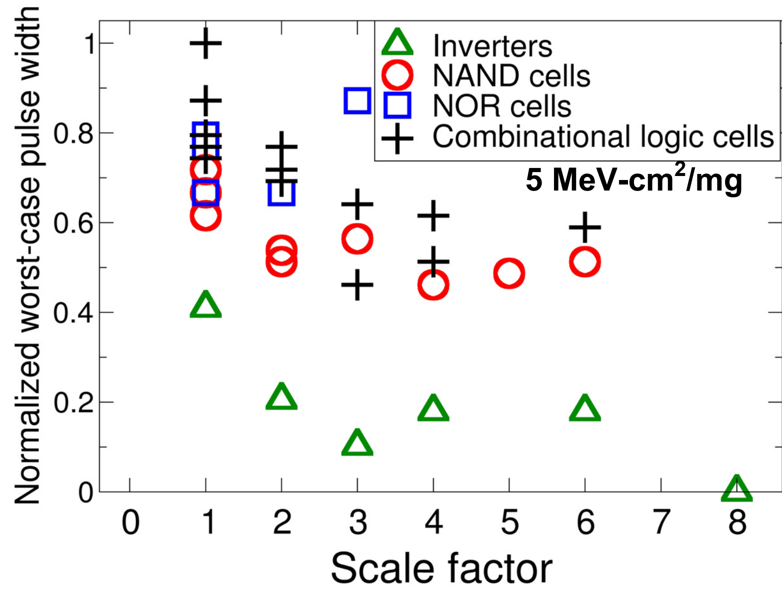

Fig. 47: Normalized worst-case SET pulse width as a function of scale factor, LET = 5 MeV-cm^2/mg

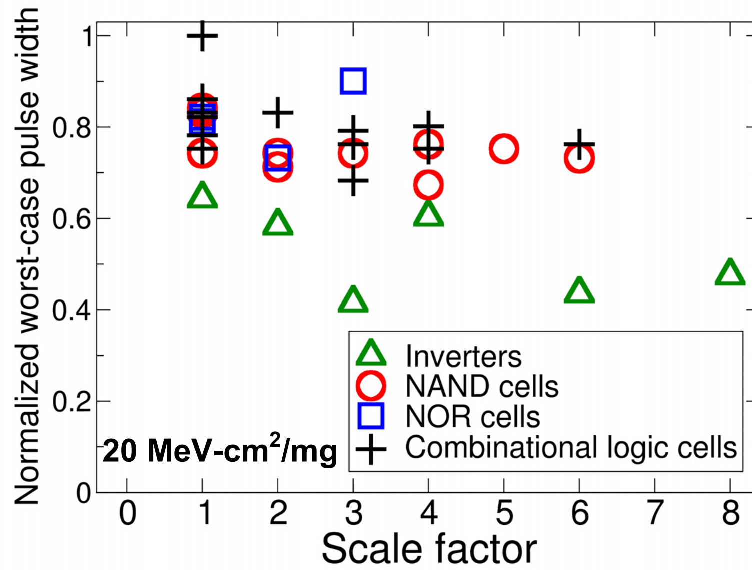

Fig. 48: Normalized worst-case SET pulse width as a function of scale factor, LET = 20 MeV-cm^2/mg

<u>Effect of LET on cell responses:</u>

Figures 46 through 49 show normalized worst-case pulse widths for the four groups of cells at LETs of 1, 5, 20 and 80 MeV-cm^2/mg, respectively, as a function of the size scale (driving factor). Each point on these plots represents an individual cell.

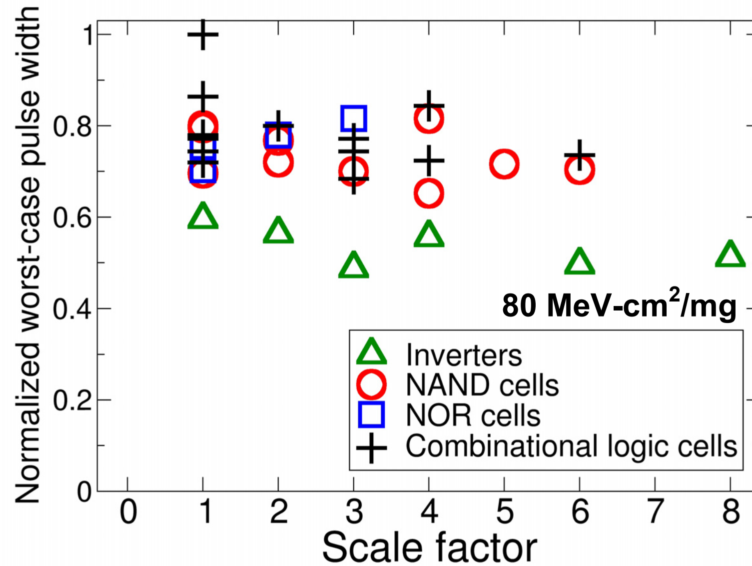

Fig. 49: Normalized worst-case SET pulse width as a function of scale factor, LET = 80 MeV-cm^2/mg

Multiple NAND, NOR and combinational logic cell results for a given scale factor indicate different cell versions with different numbers of inputs or logic functions, e.g. "NAND2_1X" or "NAND3_1X" and so on. The low LET strikes in Figs. 46 and 47 show wide variations in pulse width across cell type and scale factor. In fact, Fig. 47 indicates the relative SE tolerance of each group of cells. The inverters show the shortest SETs and the most pronounced decrease in pulse width with increasing drive strength, for reasons discussed above. The NAND cells show the next shortest SETs and a loosely correlated decrease in pulse width with higher drive. Finally, the NOR and combinational logic cells have similarly long SETs, and the combinational logic cells show a decrease in pulse width with increasing drive strength. The variations in pulse width are less pronounced with higher LET strikes. The largest variation from the maximum pulse width is approximately 60% in Fig. 48 and 50% in Fig. 49. Compared to the low LET results in Figs. 46 and 47, which showed up to 100% variation, this change

is significant. At LETs of 20 and 80 MeV-cm^2/mg the NAND, NOR, and combinational logic cells are more closely grouped than at 5 MeV-cm^2/mg. In addition, the difference between SETs in the inverters and non-inverter cells decreases. Not only do cell-to-cell variations decrease, but the correlation between pulse width and scale factor weakens. In summary, for low LET strikes, there is a variation of about ten-to-one in pulse width across the cell library, but for high LET strikes, the pulse variation across the cells is only about two-to-one.

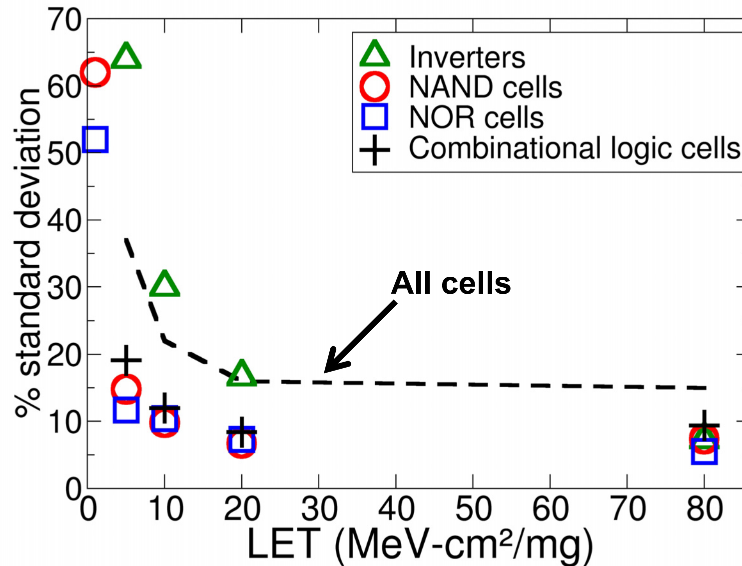

Fig. 50: Percent standard deviation of pulse widths as a function of LET

To illustrate the decrease in pulse width variation with increasing LET more exactly, the standard deviation of the pulse widths for each cell group at each LET was calculated and related to the mean pulse width (from Fig. 45) to determine percent standard deviation. Figure 50 shows the results of this calculation for each cell group as well as for all cells. For instance, the inverter data point at LET = 5 MeV-cm^2/mg in

Fig. 50 is the relative standard deviation for all the inverter pulse widths plotted in Fig. 47, approximately 65%. Since many of the inverters and combinational logic cells did not generate SETs at LET = 1 MeV-cm^2/mg, a standard deviation value for LET = 1 MeV-cm^2/mg is not plotted.

For each cell group (such as NAND gates of various output strengths and input number), the SE response varies across parameters such as drive strength and number of inputs, while the dashed line in Fig. 50 shows variation across all different cell types, sizes, and structures. For any group of cells, or all cells together, the standard deviation decreases sharply between 5 and 20 MeV-cm^2/mg. Although the pulse widths of all these cells increase with LET, the distribution of these pulse widths becomes more closely grouped. The factors that clearly differentiated each cell's SE response at lower LETs, such as drive strength and drain area, become dominated by a high-LET effect that is similar for all cells, as will be discussed in the next section. Since the only structure kept constant for all cell simulations is the well structure, this trend suggests that as LET increases, the SE response of pMOS devices is dominated by the n-well response.

<u>N-well response at high LETs:</u>

The parasitic bipolar device in 90-nm pFETs can significantly enhance SE charge collection. The amount of enhancement depends on the de-biasing of the n-well, which depends on the well contact scheme, i.e. contact area and distance from struck device [3]. In library studied in this work, the n-well size and contact area is the same for all cells, so the only variation between cells is the distance from device to well contact. Since the n-well height is fixed, the distance from the pFETs to the n-well contact is approximately

0.6 ± 0.3 μm throughout the library. Combining this spacing with the large strip contact used to contact the n-well, a past study [22] indicates that collected charge from a 40 MeV-cm^2/mg strike is enhanced by a factor of approximately four. This enhancement increases with LET, since depositing more charge exacerbates the well collapse, which triggers the bipolar effect. With charge enhancement on the order of 4X, direct charge collection constitutes only 25% of charge collection during the single-event. Because bipolar amplification strongly depends on the well response, the SET pulse width is largely determined by the well response for these high LET strikes.

6.3 Comparison to experimental data

Heavy ion and proton experiments were performed on inverter, NAND, and NOR cells in the digital library in [23]. While the TCAD characterization compared SET pulse widths of digital cells, the experiment compared SET pulse widths and cross sections. Many of the observations made in the simulations of this work were also made in the experimental results. Particularly, the competition between sensitive drain area and drive strength is discussed when comparing the SE response of different cells. Due to this competition, the 2X NAND gate exhibits longer SETs and higher sensitive area than the 1X NAND gate. [23]

One of the primary conclusions of both the TCAD and experimental characterizations was that inverters exhibit the shortest transient. At a given scale factor, the inverter drive current is larger than in any other cell, and the inverter sensitive drain area is smaller than in any other cell. Stacked pFETs result in larger sensitive drain areas in NOR gates, and stacked nFETs result in lower pull-down currents in NAND gates,

when compared to an inverter. These results validate the critical factors identified in Chapter 5. [23]

6.4 Conclusion

Worst-case SET simulations on a variety of cells from a digital library indicate that the longest SETs are most likely to be seen in the NOR gates and combinational logic cells of the library. This result is primarily due to the number of series-connected pFETs with merged source/drain diffusions which can result in large sensitive drain areas in these cells. Comparing the worst-case SE responses of cells is useful in designing circuits for a radiation environment because it aids in the selection of cells that exhibit the shortest SET pulses. In addition, this characterization identifies some instances where increasing cell drive strength is not beneficial to the SE response, e.g. the 2x NAND gate actually has longer pulse widths and a larger sensitive area (due to larger transistors) than the 1x NAND gate. It should be noted that, as shown in Chapters 4 and 5, increasing drive strength to values sufficiently above those examined in this chapter does result in shorter SETs. The simulation results also indicate that the n-well recovery dominates the SE response to high LET ion strikes because of parasitic bipolar action. Therefore, the comparison of cell pulse widths from low LET strikes would be more informative when designing for single-event tolerance.

CHAPTER VII

EFFECTS OF SINGLE-EVENT STRIKE LOCATION AND CHARGE SHARING ON 90-NM COMBINATIONAL LOGIC

While the previous chapter focused on many different cells in a library, this chapter focuses on a single cell by investigating single-event transient pulse widths and sensitive areas in an AND gate across different ion strike parameters. TCAD simulation shows charge sharing between PMOS devices reduces both pulse width and sensitive area through pulse quenching.

7.1 Simulation setup

The AND gate described in this chapter is implemented in the IBM 9SF 90 nm bulk CMOS technology. For all simulations, 3D TCAD device models developed with Synopsys Structure Editor and SDevice tools are used. Calibrated compact models were used for the devices not in TCAD. Heavy ion strikes were modeled with Guassian of radius 50 nm, striking through the device on a 20x20x20 μm^3 substrate, and a Guassian time of 2 ps. A backside substrate contact was used along the bottom surface of the substrate in series with a 1-kΩ resistor.

7.2 Simulation results: pFETs

The first set of simulations was performed for p-hits on the AND gate, which is shown schematically in Fig. 51(a). The two nodes X and Y can be used to

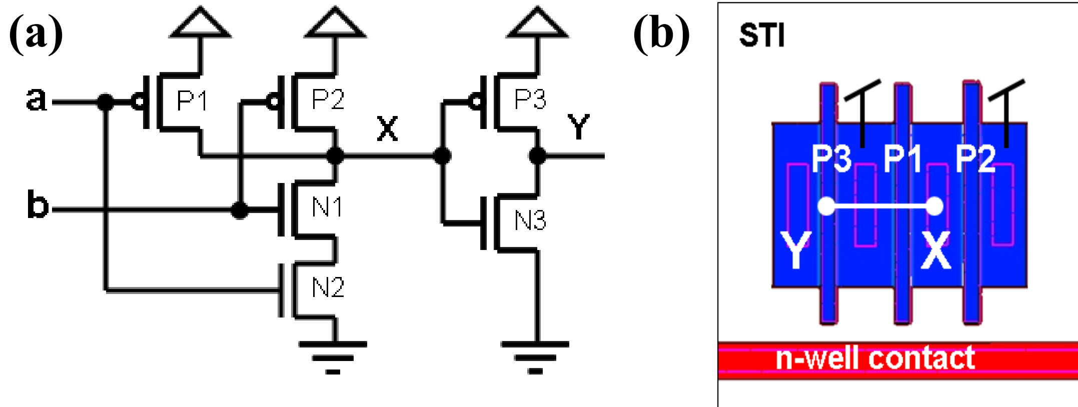

Fig. 51: (a) Schematic of AND gate with nodes X and Y labeled. (b) TCAD model of pFETs in AND gate. Transistor labels in (b) correspond to those in (a).

compare the SE response of a NAND gate to that of an AND gate. The first logic state chosen for the gate sets the X node low and the Y node high. Node X is vulnerable to p-hits, since charge collection in pFETS causes a low-high voltage transient. This input state was chosen to illustrate the pulse-quenching phenomenon discussed later. Fig. 51(b) shows a zoomed-in layout view of the 3-D TCAD model of the AND gate pFETs. P1 and P2 comprise the NAND structure, and P3 is the pull-up device of the output inverter, whose drain is the X node. The devices are surrounded by shallow trench isolation (STI). The n-well and the n-well contact expand beyond the figure to both the left and right, for the full length of 20 μm across the entire silicon volume in TCAD. The width of the n-well (2 μm) corresponds to the vertical dimension of the area shown in Fig. 51(b).

Multiple mixed-mode simulations were conducted with the location of a normal incidence, 10-MeV-cm^2/mg strike varied in a grid-like pattern over the pFET structure shown in Fig. 51(b). The resulting full-width half-rail (FWHR) pulse widths from the voltage waveforms at the X node are super-imposed on the TCAD model in Fig. 52 at the strike entry points. A pulse width of 0 ps simply indicates that the voltage transient did

not rise above the $V_{DD}/2$ threshold used to calculate the full-width half-rail (FWHR) pulse width. The diffusion labeled X is the sensitive, reverse-biased junction in this simulation, so strikes directly through it produce the longest pulses. Strikes in the source areas adjacent to the X drain produce SETs that are 20% to 50% shorter. Strikes outside of these three diffusion areas essentially produce no SETs. The sensitive area for this type of strike, i.e. the area in which a normal 10-MeV-cm^2/mg strike produced a low-high-low transient, of the X node is approximately 1.4 μm^2 with an average pulse width of 160 ps within the area.

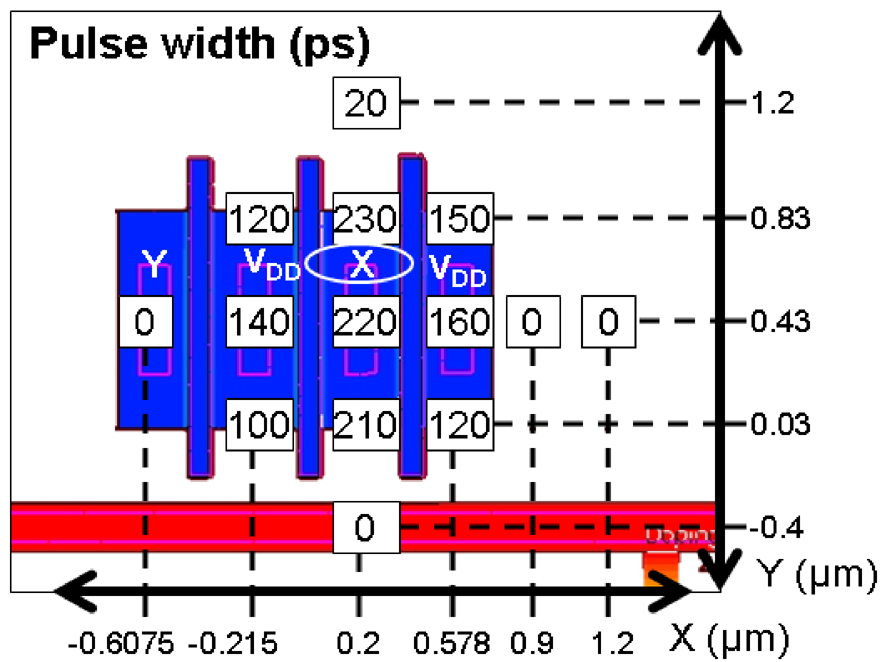

Fig. 52: SET pulse widths at node X for various strike locations (LET = 10 MeV·cm^2/mg)

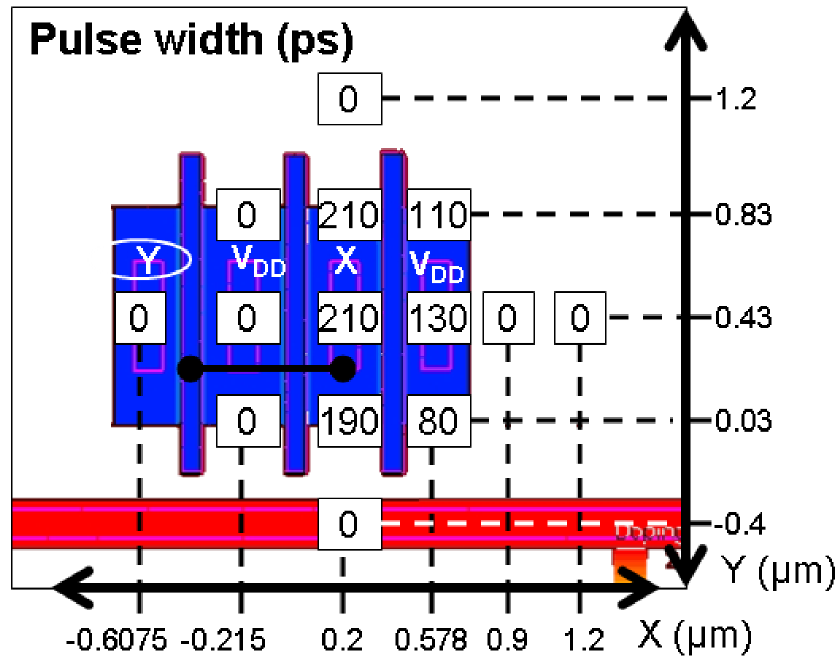

Fig. 53: SET pulse widths at node Y for various strike locations (LET = 10 MeV·cm^2/mg)

In Fig. 53 the FWHR SET pulse widths at the Y output node for the same strike simulations are shown. Interestingly, the pulse widths are shorter and the sensitive area seems to be smaller when the second stage of the logic gate is considered, as shown by comparing the pulse widths at the same strike location in Figs. 52 and 53. Some pulse widths are simply shorter from electrically propagating through the inverter. However, the SETs due to strikes at x = -0.215 µm have been completely eliminated, or quenched, by charge collected on the output inverter.

Figures 54 and 55 illustrate the pulse quenching effect by showing the current and voltage transients of the strike at the location x = -0.215 µm, y = 0.43 µm. The current transient in Fig. 54 shows 50 fC of charge collected by node X, which is

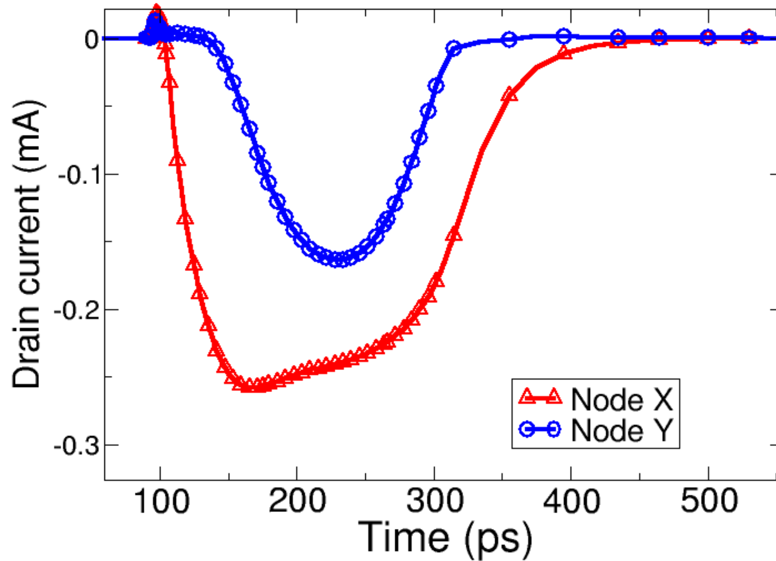

Fig. 54: Current transients of 10 -MeV-cm^2/mg strike between NAND and AND node

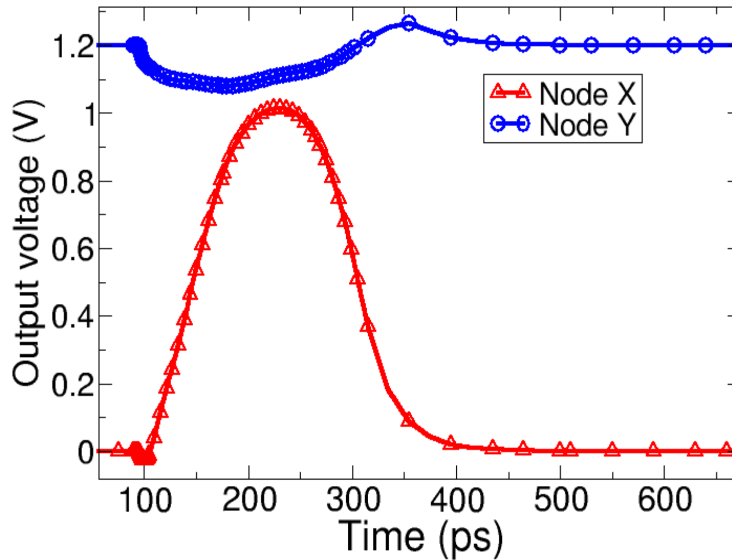

Fig. 7.5: Voltage transients of 10 MeV-cm^2/mg strike between NAND and AND node

the sensitive, reverse-biased junction. Next, Fig. 55 shows how that collected charge toggles the X node voltage from LOW to HIGH to begin a pulse. This pulse electrically propagates to the output inverter, and the Y node begins to switch from HIGH to LOW, seen around 100 ps in Fig. 55. Due to the proximity of the strike to the output inverter, the charge cloud is present underneath the output inverter (the Y node). When the Y

node voltage drops, the node collects approximately 20 fC of charge, as shown in Fig. 54. This Y node charge collection pushes the Y node voltage up from LOW to HIGH, which was the level before the ion strike. Thus, the Y node voltage in Fig. 55 does not actually show a pulse, but stays high with a small transient dip in the voltage level. This is the pulse quenching mechanism described in [11]. SET pulse quenching occurs for all the strikes on the source area between the X and Y nodes, reducing the sensitive area to 0.90 μm^2 but leaving the average pulse width of 160 ps unchanged. This phenomenon depends strongly on strike location because enough charge must be shared between the two nodes by charge deposition or charge carrier movement for the pulse to be quenched.

In order to examine longer SET pulses as well as increased charge sharing, ion strikes with LET of 40 MeV-cm^2/mg at normal incidence and ion strikes with LET of 10 MeV-cm^2/mg at 75° to normal along the n-well (right to left in Fig. 51b) were simulated in a similar fashion. Table 4 shows the sensitive areas and average pulse widths of the three different strike types for each of the circuit nodes.

Table 4: Sensitive areas and average set pulse widths of p-hits in AND gate

	NAND stage: node X		**Inverter stage: nodeY**	
Strike (LET in MeV-cm^2/mg)	Sensitive Area (μm^2)	Avg. Pulse Width (ps)	Sensitive Area (μm^2)	Avg. Pulse Width (ps)
LET = 10, normal	1.4	160	0.9	160
LET = 10, 75°	9.3	360	2.7	80
LET = 40, normal	8.7	450	5.1	250

Both the sensitive areas and average pulse widths of the 75° and 40 MeV-cm^2/mg strikes show dramatic reduction from node X to node Y. As described above, this is due to pulse quenching by the output inverter. In fact, pulse quenching is more prominent for these strikes since charge is so readily shared between the NAND structure and output

inverter. For the 40 MeV-cm^2/mg normal strike, the high LET results in more deposited charge and a larger charge cloud, and the angled ion strike deposits charge directly underneath node X and node Y. The increased charge deposition is only partially responsible for the dramatic pulse quenching, the primary mechanism for charge sharing between pFETs is bipolar amplification caused by local depression of the n-well voltage, which is the base of the parasitic pnp transistor [21]-[22]. Both the 40-MeV-cm^2/mg and 75° strikes caused significant perturbation of the n-well potential, making it easy for the output inverter to collect charge via bipolar processes and result in pulse quenching. Although pulse quenching was experimentally demonstrated in inverter chains [11], these simulations show it also occurs in standard logic gates.

Logic state dependence

The previous results showed that pulse quenching can occur when node X is LOW and node Y is HIGH. If the logic state is changed such that node X is HIGH and node Y is LOW, then only node Y would collect charge to generate a voltage transient. Since the Y node is in the output stage, there is no structure to quench the pulse. The NAND gate plays no role in the response, and the SE is a simple inverter hit. To illustrate this point, normal 10-MeV-cm^2/mg strikes were simulated on the AND gate with inputs of '00'. The resulting pulse widths at node Y are shown in Fig. 56. The sensitive area for this strike is 0.9 μm^2, and the average pulse width is approximately 160 ps. No pulse quenching is observed for these strikes since node Y simply collects charge without the NAND gate interfering. The same results are obtained with inputs of '01'

and '10', since these inputs set node X HIGH and node Y LOW. In the AND gate, the only input combination that allows pulse quenching is '11'.

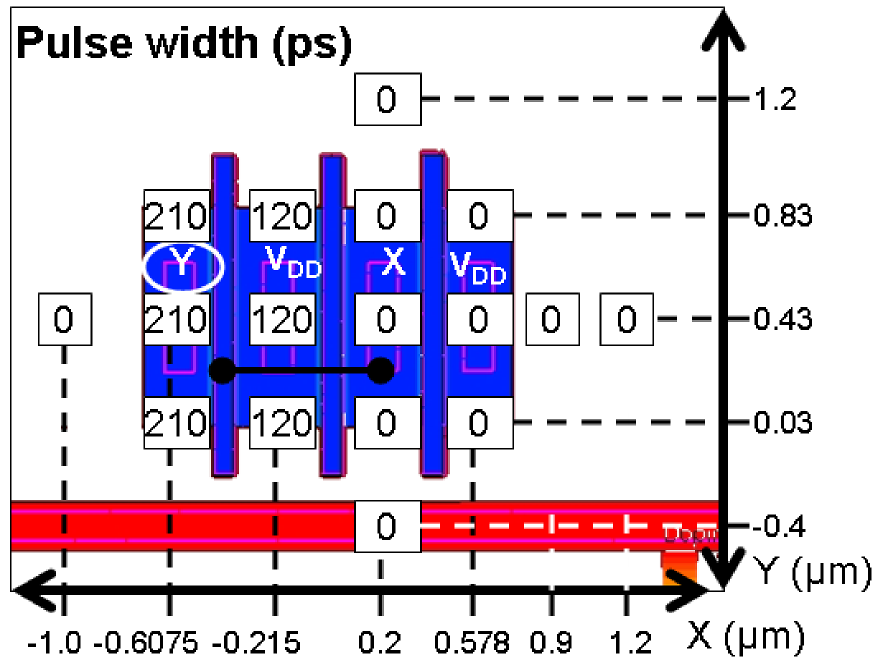

Fig. 56: SET pulse widths at node X for various strike locations. The logic state is X=HIGH, Y=LOW. (LET = 10 MeV-cm^2/mg)

7.3 Simulation results: nFETs

While pulse quenching was prominent in p-hits on the AND gate, it was not a significant effect in n-hit simulations. The TCAD model for the nFETs is shown in Fig. 57. The devices N1, N2, and N3 are connected in an AND gate configuration as shown in Fig. 51(a). The input state is set such that node X is high, making it vulnerable to n-hits, since n-hits result in HIGH-LOW voltage transitions. Normal strikes at LET of 10 MeV-cm^2/mg were simulated at various locations to estimate the sensitive area and average pulse width. The results in Fig. 57 show that the sensitive area is comprised of node X drain and the shared drain between N1 and N2. This is because N1 (turned ON

by the input state) electrically connects these two drain regions. Thus, strikes on either the X drain or the neighboring drain resulted in charge collection by node X.

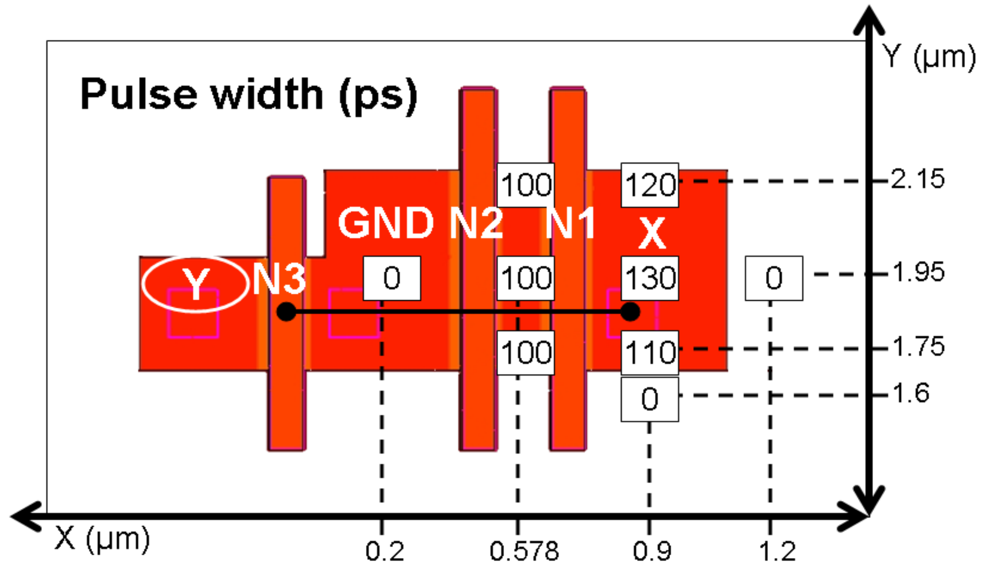

Fig. 57: SET pulses seen at node Y for various strike locations on nFETs of AND gate (LET = 10 MeV-cm^2/mg). Transistor labels correspond to Fig. 51(a).

For these simulations, the sensitive area was 0.32 μm^2 with an average pulse width of 110 ps in that area. Both sensitive area and average pulse width are smaller than the p-hit values, due to the larger size of the pFETs and parasitic bipolar amplification in the pFET structure [8]. It is interesting to note that the sensitive area of n-hits is limited to the drain regions, while the sensitive area of p-hits includes source regions as well. The SETs seen at node Y in Fig. 57 match the SETs seen at node X, which are not shown to avoid redundancy. In other words, the output inverter does not interfere with SETs generated in the NAND structure as it does in the pFETs. Pulse quenching is not observed in these n-hits because charge sharing between nFETs does not occur as readily as charge sharing between pFETs. The primary mechanisms for charge sharing between

nFETs are simply drift and diffusion, whereas the parasitic bipolar device in the pFET structure greatly enhances charge sharing. Past work indicates that increasing LET and angle of incidence would potentially result in some charge sharing between node X and node Y [8]. However, the amount of charge shared would only result in small modulation of the SET voltage pulses, so the effect on the sensitive area and pulse width would be radically less than that seen in p-hits.

7.4 Single-event transient mitigation using pulse quenching

The simulation results in Section 7.2 suggest a simple way to mitigate SETs in combinational logic. Due to pulse quenching between the NAND and inverter stages of the AND gate, both the sensitive area and average pulse width can be reduced dramatically. In the conventional layout of Fig. 51(b) the benefit of pulse quenching is only observed on the side of the layout with the inverter (P3). In this section, a design that promotes pulse quenching between the two logic stages of the AND gate is proposed.

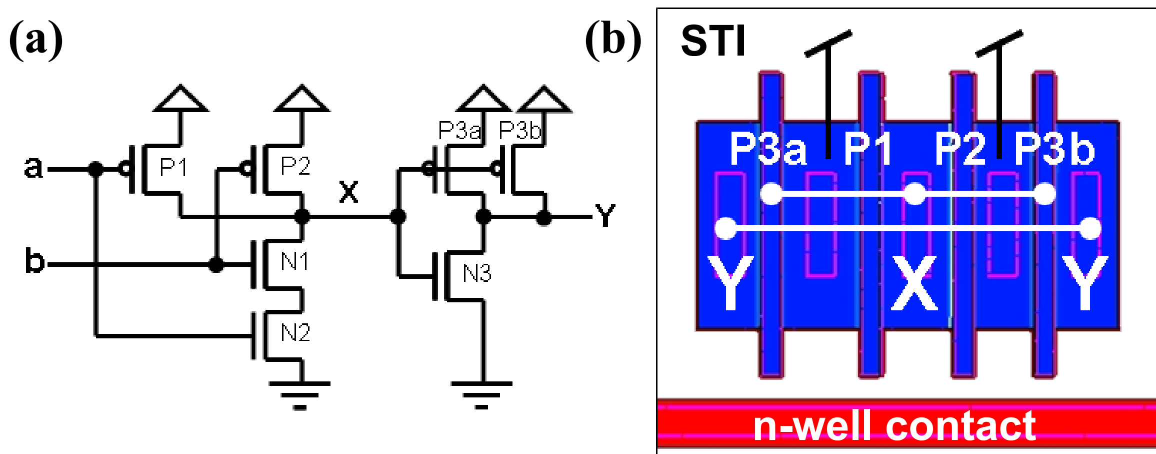

Fig. 58: (a) Schematic of proposed AND gate design that promotes pulse quenching. (b) Layout view of TCAD model of pFETs in AND gate design that promotes quenching. The only difference between this design and the conventional design of Fig. 51 is that P3 is copied on each side of the layout to increase the likelihood of pulse quenching between nodes X and Y.

Figure 58 shows the schematic and layout of the proposed AND gate design. The only change from the conventional design in Fig. 51 is that the transistor P3 is copied (as P3a and P3b) and placed on both sides of the layout. The symmetry allows node Y to more easily collect charge from an ion strike on node X, resulting in pulse quenching. In normal operation, the consequences of the extra parallel-connected pFET are larger nodal capacitance and a p-heavy output inverter, which yields a slower fall time than rise time. The proposed design increases the pFET area by 25%, so the overall area penalty is approximately 16%.

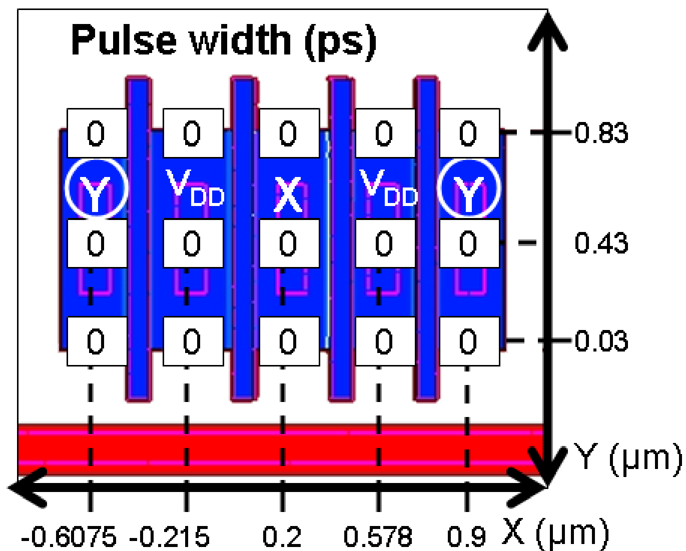

Fig. 59: Pulse widths seen at the output node Y due to 10-MeV-cm^2/mg normal strikes. Input state is X = LOW, Y = HIGH. Pulse quenching eliminates all transients for this type of strike.

As in Section 7.2, normal strikes with LET of 10 MeV-cm^2/mg are simulated at various locations on the TCAD model of the proposed design. Instead of comparing nodes X and Y, transients on the AND gate output (node Y) are compared for two

different input states. Figure 59 shows the SET pulse widths obtained when the input state sets node X to LOW and node Y to HIGH. In this state node X is the sensitive reverse-biased junction, so charge collection on both nodes X and Y results in pulse quenching. In fact, all the strike simulations in Fig. 59 result in pulse quenching, hence the sensitive area for this input state is zero. Having the output inverter pFET on each side of the NAND structure ensures that all pulses originating at node X are quenched.

The next set of simulations is with the input state such that node X is HIGH and node Y is LOW. Hence, node Y is the sensitve node, and the NAND structure does not interfere with any of the SETs generated at the Y node. In other words, pulse quenching does not occur in this input state. By designing the output inverter with two pFETs, the sensitive area in this input state is increased. In fact, the sensitive area 2.2 μm^2 is the area of all the pFETs, with an average pulse width of 150 ps in that area.

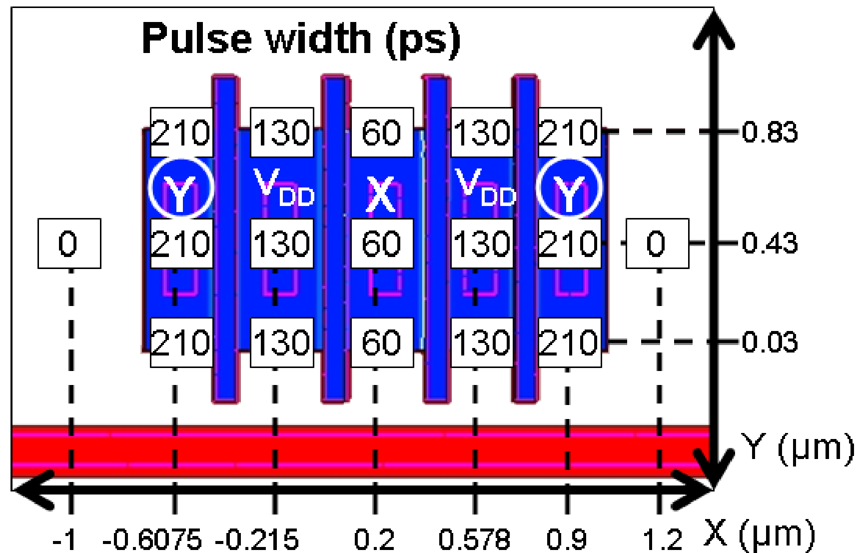

Fig. 60: Pulse widths seen at the output node Y due to 10-MeV-cm^2/mg normal strikes. Input state is X = HIGH, Y = LOW. Pulse quenching eliminates all transients for this type of strike.

To assess the SE vulnerability of the conventional and proposed designs, the sensitive area and average pulse widths must be weighted by the input state probability. From the AND gate's truth table, node X is LOW with node Y HIGH for one out of four possible input combinations, and node X is HIGH with node Y LOW for three out of four input combinations. Assuming each input combination is equally likely, pulse quenching can occur in an AND gate only 25% of the time. Since average pulse width and sensitive area indicate SE vulnerability, the product of pulse width and sensitive area can be used as a metric to compare the SE vulnerability of the conventional and proposed designs, as summarized in Table 5. The area-pulse-width product weighted by logic state is calculated by multiplying each of the area-pulse-width products by the probability of the respective logic state and summing these values. For example, 25% of the time the proposed design has an area-pulse-width product of 0 ps-μm^2, and it has a product of 330 ps-μm^2 75% of the time; so the weighted area-pulse-width product is 0*0.25 + 330*0.75 = 248 ps-μm^2. Since the weighted area-pulse-width product of the proposed design is higher than that of the conventional design, the proposed design actually renders the AND gate more vulnerable to SETs. The additional pFET increases the vulnerability of the AND gate in the most probable logic state, which can be achieved with inputs '00', '01', or '10'.

Table 5: Comparison of SE vulnerability (strike with LET = 10 MeV-cm^2/mg) of conventional and proposed AND gate designs

	X = LOW, Y = HIGH	**X = HIGH, Y = LOW**	
Design	Sensitive area * Avg. Pulse Width (ps-μm^2)	Sensitive area * Avg. Pulse Width (ps-μm^2)	Area-pulse-width product weighted by logic state (ps-μm^2)
Conventional	144	144	144
Proposed	0	330	248

Table 6: Truth table showing logic states of two stages of AND gate and OR gate. Highlighted portions indicate logic states in which pulse quenching is possible between nodes X and Y.

	AND gate		**OR gate**	
Input	NAND stage: X	Inverter stage: Y	NOR stage: X	Inverter stage: Y
00	1	0	1	0
01	1	0	0	1
10	1	0	0	1
11	0	1	0	1

Table 6 shows the truth tables of both an AND and OR gate. The logic values of the two stages of both gates are shown, and the highlighted portions indicate logic states where pulse quenching is possible. Since pulse quenching is only possible for 25% of AND gate inputs, it is not advantageous to promote it. If the proposed design were applied to an OR gate, then the result would be quite different. From the OR gate's truth table (Table 6), pulse quenching can occur for 3 of 4 possible input combinations. This reverses the weighting of area-pulse-width products used to evaluate the AND gate. Assuming the area-pulse width products for the OR gate are the same as the AND gate's and weighting them by logic state yields a weighted area-pulse-width product of 0*0.75 + 330*0.25 = 83 ps-μm^2 for the proposed design technique implemented in an OR gate, which is 40% less than the conventional design. In actuality, the values would be different, but the comparison reveals that pulse quenching can be used to reduce SE vulnerability of logic cells in which quenching can occur for the majority of the input states.

7.5 Conclusion

These p-hit and n-hit simulations illustrate the typical spatial distribution of SET pulse widths that can be observed in a logic gate. In the case of the p-hits, significant

differences due to pulse quenching were seen in sensitive area between the one-stage NAND gate and the two stage AND gate, especially for high LET and high angle of incidence. Since pulse quenching can occur in a two-stage circuit, the pulse widths can be much shorter in the AND gate than for the NAND gate. This phenomenon is significant in any logic gate that satisfies three conditions: (1) The gate has more than one logic stage in series, i.e., NAND followed by AND or NOR followed by OR. (2) The second stage electrically inverts the output of the first stage. (3) The output of the second stage is close enough to the second stage that charge collection can occur on the outputs of both stages from a single hit. Finally, the SET pulse distribution depends on the circuit input state. Some input states result in the conditions for pulse quenching, and others do not depending on the bias of the nodes of the logic stages.

These findings are significant because they illustrate a novel case in which charge sharing reduces both SET pulse width and SE sensitive area. This reduction comes for free in a number of ubiquitous logic gates that contain more than one stage, but the effect can be enhanced by judicious layout design, to further shrink sensitive area and SET pulse width. Due to the logic state dependence of the pulse quenching phenomenon, it can only be used to effectively mitigate SETs in multi-stage logic cells with truth tables that allow pulse quenching to occur for the majority of input combinations, e.g. OR gates.

CHAPTER VIII

CONCLUSIONS

This thesis has investigated parameters and mechanisms that govern the SE response of a digital library cell. In the basic single-event simulations, the function of each device electrode was discussed by looking at charge entering and exiting each one. A comparison of a p+/n-well diode and a pFET revealed how deposited charge is amplified by the bipolar process initiated by the source. This parasitic bipolar effect is incredibly important in all parts of this work.

In investigating the effect of transistor folding on SE response, it was seen that multiple drains of a single pFET easily collected charge from ion strikes of any angle. Conversely, charge is only collected on multiple nFET drains when the strike is angled. This difference is due to the different well structures of the devices. The confined n-well results in bipolar amplification of the charge, i.e. multiple sources inject minority carriers that can be easily collected by multiple drains. Consequently, increasing inverter size with folded devices is very effective for mitigating n-hit pulses, but only moderately effective for p-hits. These differing trends illustrate a complex relationship between collected charge and SET pulse width. As folded nFET size increases, the collected charge stays relatively constant, so the increased restoring current is able to remove charge at an increased rate. As folded pFET size increases, the collected charge increases dramatically due to bipolar processes, so the increased restoring correct results in only a moderate decrease in SET duration.

The three most critical factors in a cell's SE response have been identified as drain area, restoring current, and n-well contact scheme. As drain area increase, the area of the reverse-biased drain increase, so more SE charge is collected. Increasing drian area also increases the strike path length for angled strikes, resulting in more deposited charge being collected by the drain. It was shown that the drain area does not significantly affect charge collected from normal strikes. Since restoring current is the rate of SE charge removal, increasing it shortens SET pulses. An interesting trend seen here is that collected charge also increases with restoring current due to the higher limit on drain current. Finally, the n-well contact scheme shows little variation from cell to cell, so it determines the overall library response rather than the response of an individual cell.

The SE characterization of the digital cell library was performed using worst-case assumptions based on the critical factors previously discussed. It was seen that the longest SETs would most likely originate in the NOR gates and combinational logic cells due to the number of series-connected pFETs with merged source/drain diffusions that can collect charge. Analysis of variations in high-LET pulse widths and the n-well contact scheme revealed that the SET duration is dominated by the n-well response at high LETs owing to the well potential collapse and corresponding bipolar conduction of the parasitic pnp bipolar. This is because the well contacts are similar for all cells and the bipolar enhancement of charge is strongly dependent on the n-well contact.

By focusing on a single cell rather than many, information on the effects of various strike parameters was obtained. A case study of ion strikes in an AND gate revealed that, for certain strike locations, the pulse widths of p-hits were reduced

dramatically by pulse quenching. This, consequently, reduced the sensitive area in which a strike would generate an SET. This effect is a result of charge sharing between subsequent logic stages, and this SET mitigation can happen in many other types of logic cells. Furthermore, SETs can be mitigated in multi-stage logic cells which provide bias conditions for pulse quenching for the majority of input combinations. The pulse quenching effect was only seen in pFETs, since charge sharing between nFETs is not assisted by bipolar processes.

In order to efficiently characterize SETs in a digital cell library, the cell-level parameters and mechanisms that affect SE response were investigated. The knowledge gained in this work can not only aid in future library characterizations but can inform choices in SE-sensitive digital design. In closing, a list of design guidlelines based on the findings of this work is presented.

Design guidelines for mitigating SETs in a digital cell library

- Strip (continuous) n-well contacts should be used instead of widely spaced n-well contacts to mitigate the bipolar amplification of SE charge in pFETs. P-well contacts are less important because high conductivity between the p-well and p-substrate to ground helps to stabilize the well potential. (Note: in case of triple-well technology, strip contacts should be used for both wells.)
- In cell layouts, pFETs should be placed within minimum distance to n-well contacts.
- Inverters with drive strength greater than 1X should be designed with as few fingers as possible to mitigate amplification of SE charge by multiple bipolar

structures. Transistors may either be placed in wells large enough to accommodate the devices, or the transistor layouts can be rotated 90° to fit in smaller wells in technologies whose design rules allow rotation. Although the sensitive drain area will be larger than in the multiple-finger version, the n-well collapse will not encompass the entire device, so bipolar enhancement will be minimized.

- Since p-hits yield longer SETs than n-hits, cells should be designed to be n-heavy, meaning the nFET drive current should be greater than that of the pFET. With pull-down nFET drive on the order of double the pFET drive, significant p-hit mitigation can be achieved. Balanced versions of these n-heavy cells can also exist for cases where matched switching times is critical. Cells with stacked nFETs, such as NAND gates, require special attention to ensure sufficient restoring current to pFETs.
- Since the longest pulses are likely to come from complex logic cells, e.g. OAI21 or AOI22, synthesizing these functions with NAND gates and inverters when possible would reduce the pulse widths. Since such a synthesis typically requires multiple logic stages, additional SET mitigation would be gained from pulse quenching and logical masking.
- Layouts of multiple-stage cells (AND, OR, buffers, etc.) should be as compact as possible in order to promote pulse quenching. For more aggressive SET mitigation using pulse quenching, OR gates and other two-stage cells with more minterms than maxterms in their truth tables may be designed using the symmetric layout technique proposed in Chapter 7.

APPENDIX

A. Doping profiles of 3-D TCAD models

In this appendix, details of the doping profiles of the TCAD device models are discussed. The doping values were initially based on the data in [25] and [26], and an iterative calibration approach resulted in TCAD models that can be verified with the 9SF Spice models available from MOSIS [19]. Sample device and simulation scripts are included at the end of this appendix. The nFET model used in these figures has gate length of 80 nm and width of 280 nm. Figure 61 shows the cross section of the nFET model with two cutlines drawn. One-dimensional cuts are taken along cutlines 1 and 2 to plot doping profile versus depth in Figs. 64 and 65, respectively.

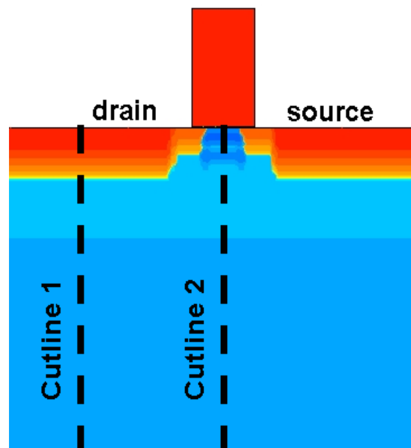

Fig. 61: Cross section of nFET TCAD model showing cutlines 1 and 2 used for Figs. 64 and 65

Figure 62(a) shows the layout view of the nFET model with a vertical cutline drawn. In Fig. 62(a) there is a rectangle cut out of the STI. This is simply where the pFET would be in the model for an inverter configuration, i.e. in an actual inverter STI

would not be present at this location. Figure 62b is the cross section of the model taken along the 2-D cutline in Fig. 62b. The dual-well structure is evident in this cross section .

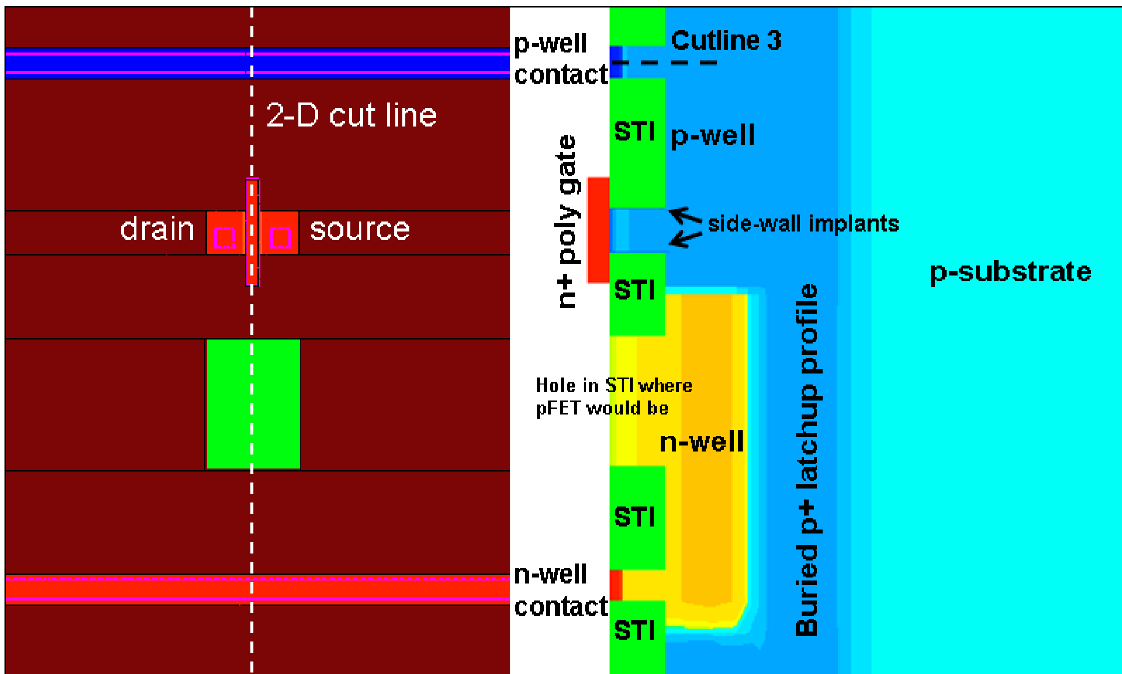

Fig. 62: (a) Layout view of nFET TCAD model with cutline for (b) shown. (b) Cross section of nFET TCAD model taken along cutline in (a). Doping profiles and cutline used for Fig. 66 are shown.

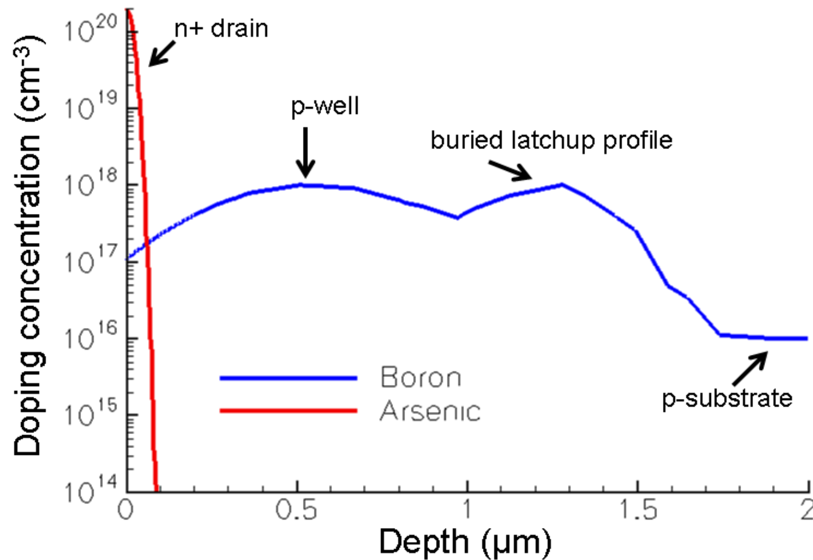

Fig. 63: Boron and arsenic doping concentrations of nFET drain along cutline 1 in Fig. 61.

The n+ drain doping profile is shown in Fig. 63, a 1-D cut along cutline 1 in Fig. 61. The profiles pictured are:

N+ drain/source: Gaussian arsenic profile with maximum concentration of 2e20 cm^{-3} at depth of 0 nm, with the concentration dropping off to 1e17 cm^{-3} at 60 nm.

P-well: Gaussian boron profile with maximum concentration of 1e18 cm^{-3} at depth of 0.55 µm, with the concentration dropping off to 1e17 cm^{-3} at 0.55 ± 0.55 µm.

Buried latchup profile: Gaussian boron profile with maximum concentration of 1e18 cm^{-3} at depth of 1.25 µm, with the concentration dropping off to 1e16 cm^{-3} at 1.25 ± 0.4 µm.

P-substrate: Constant boron concentration of 1e16 cm^{-3} throughout the model.

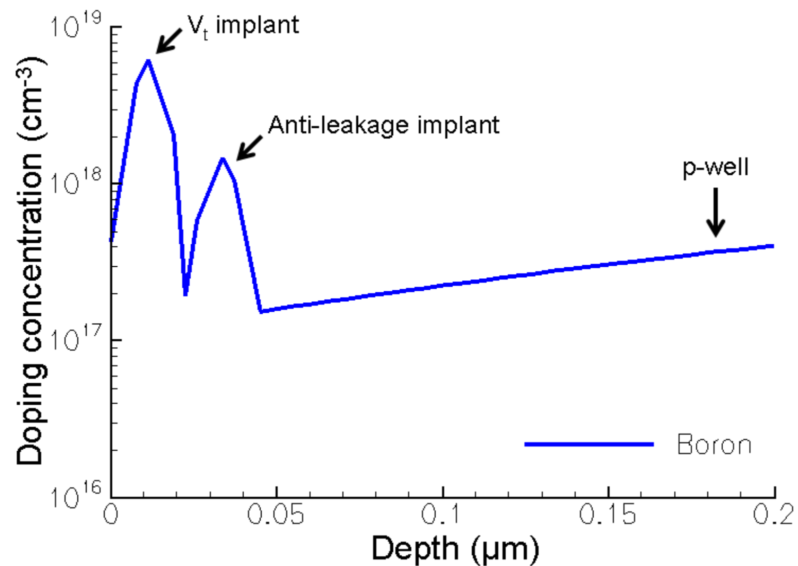

Fig. 64: Boron doping concentrations of nFET channel along cutline 2 in Fig. 61.

Figure 64 shows the doping in the channel region of the nFET, taken along cutline 2 in Fig. 61. The profiles shown are:

V_t implant: Gaussian boron profile with maximum concentration of 6.4e18 cm^{-3} at depth of 10 nm, with concentration dropping off to 3.2e17 cm^{-3} at 10 ± 10 nm.

Anti-leakage implant: Gaussian boron profile with maximum concentration of 9e18 cm^{-3} at depth of 30 nm, with concentration dropping off to 3 e17 cm^{-3} at 30 ± 5 nm.

There are other profiles not shown in the 1-D cuts but visible in Figs. 61 and 62(b):

Lightly doped drain (LDD): Gaussian arsenic profile with maximum concentration of 1e19 cm^{-3} at depth of 0 nm, with concentration dropping off to 1e17 cm^{-3} at 30 nm. Each LDD is 43 nm long (L dimension of transistor) and the space between LDDs is 50 nm.

Halo implants: Gaussian arsenic profile with maximum concentration of 2e20 cm^{-3} at depth of 30 nm, with concentration dropping off to 1e16 cm^{-3} at 30 ± 25 nm. Each halo is 5 nm long (L dimension of transistor) and the space between halos is 40 nm.

N+ polysilicon: Poly has constant arsenic concentration of 1e20 cm^{-3}.

Side-wall implants: Constant boron profile with concentration of 6e18 cm^{-3}. These implants are very thin sheets between the channel region and STI. The implants are 10 nm in the channel's L dimension and extend from 0 μm to 0.36 μm in depth. Arrows in Fig. 62(b) indicate the location of each implant.

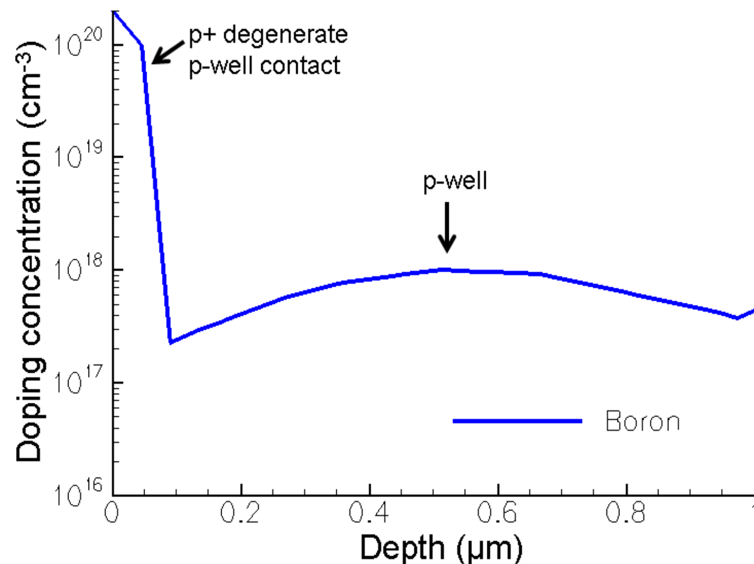

Fig. 65: Boron doping concentrations of p-well contact along cutline 3 in Fig. 62(b).

The final doping profile for the nFET is the p-well contact ohmic shown in Fig. A6. It consists of a Gaussian boron profile with maximum concentration of 2e20 cm^{-3} at depth of 0 nm, with concentration dropping off to 1e17 cm^{-3} at 80 nm.

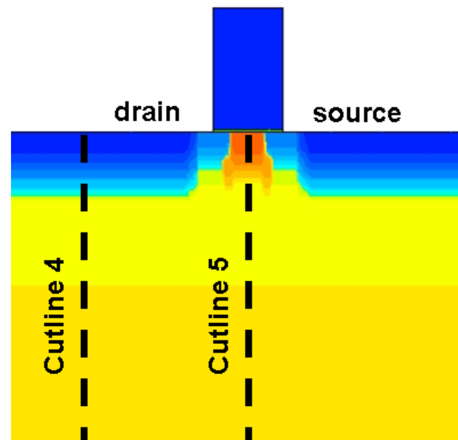

Fig. 66: Cross section of pFET TCAD model showing cutlines 4 and 5 used for Figs. 68 and 69.

Figure 66 shows the cross section of the pFET model with two cutlines drawn. One-dimensional cuts are taken along cutlines 4 and 5 to plot doping profile versus depth in Figs. 68 and 69, respectively. Figure 67(a) shows the layout view of the pFET model with a vertical cutline drawn. The cross section taken along this cutline is shown in Fig. 67(b).

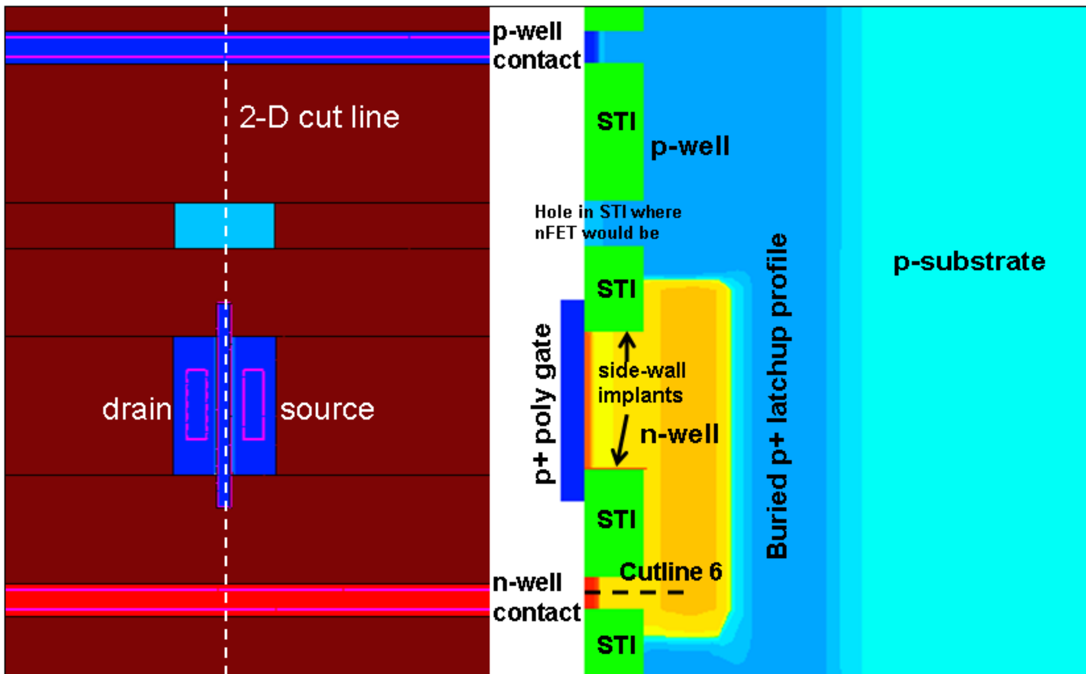

Fig. 67: (a) Layout view of pFET TCAD model with cutline for (b) shown. (b) Cross section of pFET TCAD model taken along cutline in (a). Doping profiles and cutline used for Fig. 70 are shown.

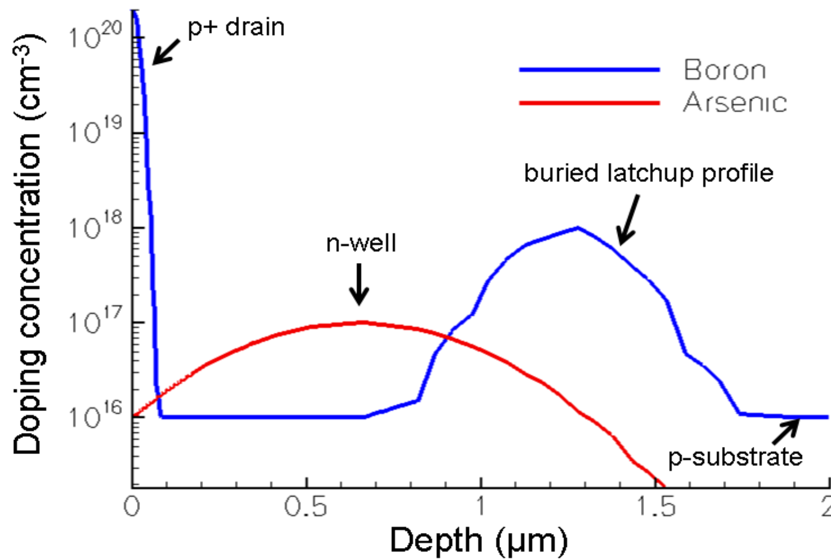

Fig. 68: Boron doping concentrations of pFET drain along cutline 4 in Fig. 66.

The p+ drain doping profile is shown in Fig. 68, a 1-D cut along cutline 4 in Fig. 66. The profiles pictured are:

P+ drain/source: Gaussian boron profile with maximum concentration of 2e20 cm^{-3} at depth of 0 nm, with the concentration dropping off to 1e17 cm^{-3} at 60 nm.

N-well: Gaussian arsenic profile with maximum concentration of 1e17 cm^{-3} at depth of 0.65 μm, with the concentration dropping off to 1e16 cm^{-3} at 0.65 ± 0.65 μm.

The buried latchup and p-substrate profiles are the same as previously described.

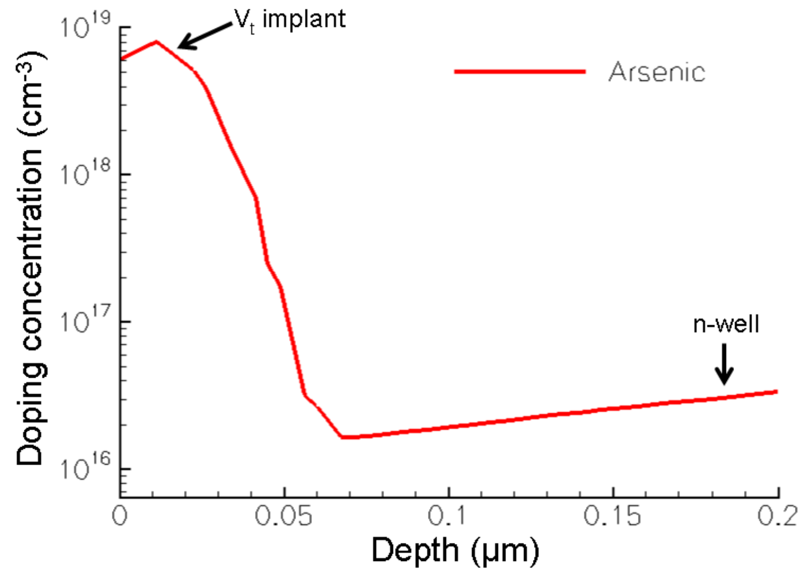

Fig. 69: Arsenic doping concentrations of pFET channel along cutline 5 in Fig. 66.

Figure 69 shows the doping in the channel region of the pFET, taken along cutline 5 in Fig. 66. The profile shown is:

V_t implant: Gaussian arsenic profile with maximum concentration of 8e18 cm^{-3} at depth of 10 nm, with concentration dropping off to 6e17 cm^{-3} at 10 ± 30 nm. Information regarding the absence of an anti-leakage implant is contained in Appendix C.

There are other profiles not shown in the 1-D cuts but visible in Figs. 66 and 67(a):

Lightly doped drain (LDD): Gaussian boron profile with maximum concentration of 4e18 cm^{-3} at depth of 0 nm, with concentration dropping off to 1e17 cm^{-3} at 30 nm. Each LDD is 47 nm long (L dimension of transistor) and the space between LDDs is 50 nm.

Halo implants: Gaussian boron profile with maximum concentration of 5e17 cm^{-3} at depth of 40 nm, with concentration dropping off to 1e15 cm^{-3} at 40 ± 35 nm. Each halo is 5 nm long (L dimension of transistor) and the space between halos is 40 nm.

P+ polysilicon: Poly has constant boron concentration of 1e20 cm^{-3}.

Side-wall implants: Constant arsenic profile with concentration of 5e19 cm^{-3}. These implants are very thin sheets between the channel region and STI. The implants are 8 nm in the channel's L dimension and extend from 0 μm to 0.36 μm in depth. Arrows in Fig. 69 indicate the location of each implant.

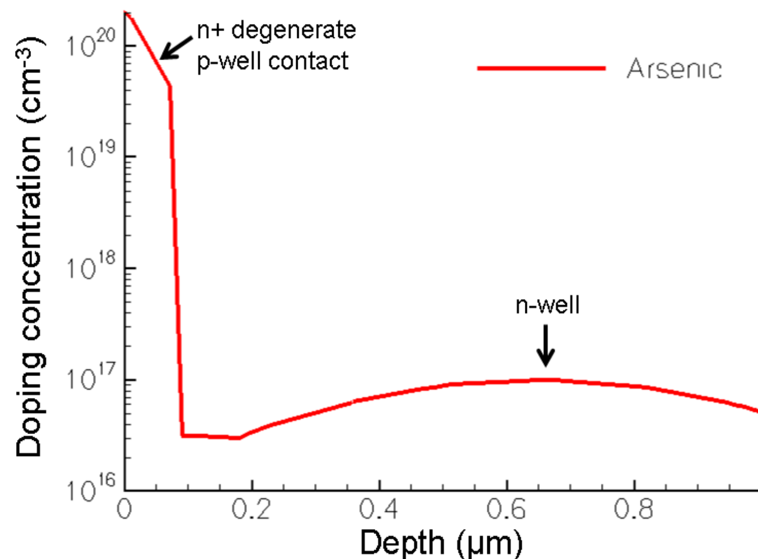

Fig. 70: Arsenic doping concentrations of n-well contact along cutline 6 in Fig. 67(b).

The final doping profile for the pFET is the n-well contact shown in Fig. 70. It consists of a Gaussian arsenic profile with maximum concentration of 2e20 cm^{-3} at depth of 0 nm, with concentration dropping off to 1e17 cm^{-3} at 80 nm.

The well and substrate profiles are used for both nFET and nFET models in order to capture all well effects. Below are sample Synopsys SDE scripts for an nFET model and a pFET model.

SDE script for nFET TCAD model

```
; Setting parameters

; - lateral
(define Ltot 3.5)   ; [um] Lateral extend total
(define Lg 0.08)   ; [um] Gate length

(define subzmin (/ 20 -2.0)); [um] Max. frontside extension in the z-direction
(define subzmax (/ 20 2)); [um] Max. backside extension in the z-direction

(define subxmin (/ 20 -2.0)); [um] Max. leftside extension in the x-direction
(define subxmax (/ 20 2)); [um] Max. rightside extension in the x-direction
(define wn 0.84); [um] width of the pmos device
(define Ls 0.27); [um] length of source
(define Ld 0.27); [um] length of drain
(define Con 0.08); [um] dimensions of square contacts
(define well_z 1); [um] the z height of well contact
(define sd_con 3);  the number of s/d contacts

(define Lgn 0.08)   ; [um] Gate length
(define wnn 0.28); [um] width of the nmos device
(define Lsn 0.26); [um] length of source - nmos
(define Ldn 0.26); [um] length of drain - nmos
(define n_offset (+ wn 0.535))

(define pwell_con (+ n_offset 1.22))

(define nwell_strip 20)

(define well_strip 1.6)
(define pwell_strip 20)

(define nwell_con -0.765)

; Layers
(define Ysub 20)   ; [um] Substrate thickness
(define Tox 14e-4) ; [um] Gate oxide thickness
(define Ypol -0.14)  ; [um] Poly gate thickness

; Substrate doping level
(define Dop 1e16) ; [1/cm3]

; Derived quantities
(define Xmax (/ Ltot 2.0))
(define Xg   (/ Lg   2.0))
(define Ygox (* Tox -1.0))

; Ion track variables
(define Yion 20.0)  ; mesh depth


;-----------------------------------------------------------------------------------------
-------
; Overlap resolution: New replaces Old
(isegeo:set-default-boolean "ABA")
;-----------------------------------------------------------------------------------------
-------
```

```
; CREATE REGIONS

; SUBSTRATE REGION
(isegeo:create-cuboid (position subxmin 0 subzmin) (position subxmax Ysub subzmax)
"Silicon" "region_1" )




; GATE OXIDE REGION - Main nmos
(isegeo:create-cuboid (position (* Xg -1.0) 0 n_offset) (position Xg Ygox (+ n_offset
wnn)) "SiO2" "region_2n")

; GATE OXIDE REGION - Front Extension
(isegeo:create-cuboid (position (* Xg -1.0) 0 (- n_offset 0.2)) (position Xg Ygox
n_offset) "SiO2" "region_22n")

; GATE OXIDE REGION - Back Extension
(isegeo:create-cuboid (position (* Xg -1.0) 0 (+ n_offset wnn)) (position Xg Ygox (+ (+
n_offset wnn) 0.2)) "SiO2" "region_222n")

; PolySi GATE - Main  nmos
(isegeo:create-cuboid (position (* Xg -1.0) Ygox (- n_offset 0.2)) (position Xg Ypol (+
0.2 (+ n_offset wnn))) "PolySi" "region_3n")




; STI REGION - I ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 wn) (position 2.28 0.36 n_offset) "Oxide"
"STI1" )

; STI REGION - 25 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ n_offset wnn)) (position 2.28 0.36 (- (-
pwell_con 0.02) (* Con well_z))) "Oxide" "STI25" )

; STI REGION - 26 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 n_offset) (position (- (* Xg -1) Ldn) 0.36 (+
n_offset wnn)) "Oxide" "STI26" )

; STI REGION - 27 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position (+ Xg Lsn) 0 n_offset) (position 2.28 0.36 (+ n_offset
wnn)) "Oxide" "STI27" )

; STI REGION - II ("behind" S/D, from the right edge of the gate extension to edge of
S/D)

; STI REGION - III ("to the right" of S/D)
(isegeo:create-cuboid (position (+ 0.04 Ls) 0 0) (position 2.28 0.36 wn) "Oxide" "STI3" )

; STI REGION - IV ("in front of" of S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ (+ nwell_con 0.02) (* Con well_z)))
(position (+ 0.02 (+ 2.3 Con)) 0.36 0) "Oxide" "STI4" )

; STI REGION - IX ("in front of" of nwell contacts, till the left edge of the gate
extension)
(isegeo:create-cuboid (position subxmin 0 subzmin) (position (+ 2.32 Con) 0.36 (- -4.12
(* Con well_z))) "Oxide" "STI9" )

; STI REGION - V ("in front of" of S/D, from the right edge of the gate extension to the
edge of S/D)

; STI REGION - VI ("to the left of" of S/D)
(isegeo:create-cuboid (position subxmin 0 0) (position (- -0.04 Ld) 0.36 wn) "Oxide"
"STI6" )

; STI REGION - VII ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 (+ (+ pwell_con 0.02) (* Con
well_z))) (position subxmax 0.36 subzmax) "Oxide" "STI7" )
```

```
; STI REGION - VIIc ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 (+ (+ nwell_con 0.02) (* Con
well_z))) (position subxmax 0.36 (- (- pwell_con 0.02) (* Con well_z))) "

; STI REGION - VIIb ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 (+ -4.08 (* Con well_z)))
(position subxmax 0.36 (- (- nwell_con 0.02) (* Con well_z))) "Oxide" "STI7b" )

; STI REGION - VIId ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 subzmin) (position subxmax 0.36 (-
-4.12 (* Con well_z))) "Oxide" "STI7b" )

; STI REGION - xii
(isegeo:create-cuboid (position 2.28 0 subzmin) (position (+ 0.02 (+ 2.3 Con)) 0.36 (- -
4.12 (* Con well_z))) "Oxide" "STI12" )

; STI REGION - xIII
(isegeo:create-cuboid (position 2.28 0 0) (position (+ 0.02 (+ 2.3 Con)) 0.36 (- (-
pwell_con 0.02) (* Con well_z))) "Oxide" "STI13" )


; STI REGION - XIV ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ (+ pwell_con 0.02) (* Con well_z)))
(position (+ 2.32 Con) 0.36 subzmax) "Oxide" "STI14" )



; STI REGION - xxi ("in front of" of nwell contacts, till the left edge of the gate
extension)
(isegeo:create-cuboid (position subxmin 0 (+ -4.08 (* Con well_z))) (position (+ 2.32
Con) 0.36 (- (- nwell_con 0.02) (* Con well_z))) "Oxide" "STI21" )

; STI REGION - xxii ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (- -4.12 (* Con well_z))) (position (/
well_strip -2.0) 0.36 (+ -4.08 (* Con well_z))) "Oxide" "STI22" )

; STI REGION - xxiv ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position (/ well_strip 2.0) 0 (- -4.12 (* Con well_z))) (position
subxmax 0.36 (+ -4.08 (* Con well_z))) "Oxide" "STI24" )

;-----------------------------------------------------------------------------------------
--------
; DEFINING AND PLACING CONTACTS

; SUBSTRATE CONTACT
(isegeo:define-contact-set "substrate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0 Ysub 0)) "substrate")


;NMOS
; GATE CONTACT nmos
(isegeo:define-contact-set "gate_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0 Ypol (+ n_offset 0.07))) "gate_nmos")

; DRAIN CONTACT nmos
(isegeo:create-cuboid (position -0.12 0 (+ 0.04 n_offset)) (position (- -0.12 0.12) -0.2
(+ (+ 0.04 0.12) n_offset)) "Metal" "Drainmetal")
(isegeo:define-contact-set "drain_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.2 0 (+ 0.1 n_offset))) "drain_nmos")
(isegeo:delete-region (find-body-id (position -0.2 -0.1 (+ 0.1 n_offset))))

; SOURCE CONTACT nmos
(isegeo:create-cuboid (position 0.12 0 (+ 0.04 n_offset)) (position (+ 0.12 0.12) -0.2 (+
(+ 0.04 0.12) n_offset)) "Metal" "Sourcemetal")
(isegeo:define-contact-set "source_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.2 0 (+ 0.1 n_offset))) "source_nmos")
(isegeo:delete-region (find-body-id (position 0.2 -0.1 (+ 0.1 n_offset))))



; n-WELL CONTACT 1 (this would be connected to Vdd, along with the source)
```

```
(isegeo:create-cuboid (position subxmin 0 (- nwell_con (* 0.12 0.5))) (position subxmax -
0.2 (+ nwell_con (* 0.12 0.5))) "Metal" "nwell")
(isegeo:define-contact-set "nwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -5 0 nwell_con)) "nwell")
(isegeo:delete-region (find-body-id (position -5 -0.1 nwell_con)))

; p-WELL CONTACT 9
(isegeo:create-cuboid (position subzmin 0 (- pwell_con (* 0.12 0.5))) (position subzmax -
0.2 (+ pwell_con (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -4 0 pwell_con)) "pwell")
(isegeo:delete-region (find-body-id (position -4 -0.1 pwell_con)))



; p-WELL CONTACT 11
(isegeo:create-cuboid (position -0.64 0 (- -4.1 (* 0.12 0.5))) (position (- -0.64 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.66 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.66 -0.1 -4.1)))

; p-WELL CONTACT 12
(isegeo:create-cuboid (position 0.64 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.64 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.66 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.66 -0.1 -4.1)))


; p-WELL CONTACT 4
(isegeo:create-cuboid (position 0.08 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.08 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.09 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.09 -0.1 -4.1)))

; p-WELL CONTACT 5
(isegeo:create-cuboid (position 0.36 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.36 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.37 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.37 -0.1 -4.1)))

; p-WELL CONTACT 6
(isegeo:create-cuboid (position -0.08 0 (- -4.1 (* 0.12 0.5))) (position (- -0.08 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.09 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.09 -0.1 -4.1)))

; p-WELL CONTACT 8
(isegeo:create-cuboid (position -0.36 0 (- -4.1 (* 0.12 0.5))) (position (- -0.36 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.37 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.37 -0.1 -4.1)))



;------------------------------------------------------------------------------------------
---------
; SET DOPING REGIONS AND PROFILES

; CONSTANT DOPING PROFILES

; SUBSTRATE REGION AND PROFILE
(isedr:define-constant-profile "region_1" "BoronActiveConcentration" Dop )
(isedr:define-constant-profile-region  "region_1" "region_1" "region_1" )

; PolySi GATE REGION AND PROFILE - Main    NMOS
```

```
(isedr:define-constant-profile "region_3n" "ArsenicActiveConcentration" 1e20)
(isedr:define-constant-profile-region "region_3n" "region_3n" "region_3n")

;-----------------------------------------------------------------------------------------
---------
; ANALYTICAL DOPING PROFILES

; SUBSTRATE (LATCHUP) PROFILE (IN BETWEEN THE n-WELL AND THE SUBSTRATE)
(isedr:define-refinement-window "Latchup.Profile.Region" "Rectangle" (position subxmin
1.25 subzmin) (position subxmax 1.25 subzmax))
(isedr:define-gaussian-profile "Latchup.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Latchup.Profile.Place" "Latchup.Profile"
"Latchup.Profile.Region" "Symm" "NoReplace" "Eval")


; n-WELL PROFILE OF THE PMOS DEVICE
(isedr:define-refinement-window "nwell.Profile.Region" "Rectangle" (position subxmin 0.65
-1.025) (position subxmax 0.65 1.1))
(isedr:define-gaussian-profile "nwell.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 1e17 "ValueAtDepth" 1e16 "Depth" 0.65 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "nwell.Profile.Place" "nwell.Profile"
"nwell.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL PROFILE behind the nwell
(isedr:define-refinement-window "pwell1.Profile.Region" "Rectangle" (position subxmin
0.55 1.15) (position subxmax 0.55 subzmax))
(isedr:define-gaussian-profile "pwell1.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.55 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwell1.Profile.Place" "pwell1.Profile"
"pwell1.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL PROFILE in front of the nwell
(isedr:define-refinement-window "pwell2.Profile.Region" "Rectangle" (position subxmin
0.55 subzmin) (position subxmax 0.55 -1.125))
(isedr:define-gaussian-profile "pwell2.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.55 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwell2.Profile.Place" "pwell2.Profile"
"pwell2.Profile.Region" "Symm" "NoReplace" "Eval")

; n-WELL CONTACT PROFILE (DEGENRATE DOPING FOR n-WELL CONTACT) 1
(isedr:define-refinement-window "nwelltap.Profile.Region" "Rectangle" (position subxmin 0
(- (- nwell_con 0.02) (* Con well_z))) (position subxmax 0 (+ (+ nwell_con 0.02) (* Con
well_z))))
(isedr:define-gaussian-profile "nwelltap.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "nwelltap.Profile.Place" "nwelltap.Profile"
"nwelltap.Profile.Region" "Symm" "NoReplace" "Eval")


; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT) 1
(isedr:define-refinement-window "pwelltap.Profile.Region" "Rectangle" (position subzmin 0
(- (- pwell_con 0.02) (* Con well_z))) (position subzmax 0 (+ (+ pwell_con 0.02) (* Con
well_z))))
(isedr:define-gaussian-profile "pwelltap.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap.Profile.Place" "pwelltap.Profile"
"pwelltap.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT) 4
(isedr:define-refinement-window "pwelltap4.Profile.Region" "Rectangle" (position (/
well_strip -2.0) 0 (- -4.12 (* Con well_z))) (position (/ well_strip 2.0) 0 (+ -4.08 (*
Con well_z))))
(isedr:define-gaussian-profile "pwelltap4.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap4.Profile.Place" "pwelltap4.Profile"
"pwelltap4.Profile.Region" "Symm" "NoReplace" "Eval")
```

```
;---------------------------------NMOS Profiles------------------------------------------
--
; SOURCE n
(isedr:define-refinement-window "sourcen.Profile.Region" "Rectangle" (position 0.068 0
n_offset) (position (+ 0.04 Ls) 0 (+ n_offset wnn)))
(isedr:define-gaussian-profile "sourcen.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcen.Profile.Place" "sourcen.Profile"
"sourcen.Profile.Region" "Symm" "NoReplace" "Eval")

; SOURCE HALO n
(isedr:define-refinement-window "HSimplantn.Profile.Region" "Rectangle" (position 0.02
0.03 n_offset) (position 0.025 0.03 (+ n_offset wnn)))
(isedr:define-gaussian-profile "HSimplantn.Profile" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HSimplantn.Profile.Place"
"HSimplantn.Profile" "HSimplantn.Profile.Region" "Symm" "NoReplace" "Eval")

; DRAIN n
(isedr:define-refinement-window "drainn.Profile.Region" "Rectangle" (position -0.068 0
n_offset) (position (- -0.04 Ld) 0 (+ n_offset wnn)))
(isedr:define-gaussian-profile "drainn.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainn.Profile.Place" "drainn.Profile"
"drainn.Profile.Region" "Symm" "NoReplace" "Eval")

; DRAIN HALO n
(isedr:define-refinement-window "HDimplantn.Profile.Region" "Rectangle" (position -0.02
0.03 n_offset) (position -0.025 0.03 (+ n_offset wnn)))
(isedr:define-gaussian-profile "HDimplantn.Profile" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HDimplantn.Profile.Place"
"HDimplantn.Profile" "HDimplantn.Profile.Region" "Symm" "NoReplace" "Eval")

; LDD - SOURCE n
(isedr:define-refinement-window "sourcelddn.Profile.Region" "Rectangle" (position 0.025
0.0 n_offset) (position 0.068 0 (+ n_offset wnn)))
(isedr:define-gaussian-profile "sourcelddn.Profile" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 1e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourcelddn.Profile.Place"
"sourcelddn.Profile" "sourcelddn.Profile.Region" "Symm" "NoReplace" "Eval")

; LDD - DRAIN n
(isedr:define-refinement-window "drainlddn.Profile.Region" "Rectangle" (position -0.025
0.0 n_offset) (position -0.068 0 (+ n_offset wnn)))
(isedr:define-gaussian-profile "drainlddn.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 1e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainlddn.Profile.Place" "drainlddn.Profile"
"drainlddn.Profile.Region" "Symm" "NoReplace" "Eval")

; Vt IMPLANT n
(isedr:define-refinement-window "implantn.Profile.Region" "Rectangle" (position -0.025
0.01 n_offset) (position 0.025 0.01 (+ n_offset wnn)))
(isedr:define-gaussian-profile "implantn.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 6.4e18 "ValueAtDepth" 3.2e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implantn.Profile.Place" "implantn.Profile"
"implantn.Profile.Region" "Symm" "NoReplace" "Eval")

; IMPLANT TO MITIGATE LEAKAGE (BELOW Vt IMPLANT) n
(isedr:define-refinement-window "limplantn.Profile.Region" "Rectangle" (position -0.025
0.03 n_offset) (position 0.025 0.03 (+ n_offset wnn)))
(isedr:define-gaussian-profile "limplantn.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 9e18 "ValueAtDepth" 3e17 "Depth" 0.005 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplantn.Profile.Place" "limplantn.Profile"
"limplantn.Profile.Region" "Symm" "NoReplace" "Eval") ; STI Implant - Front & Back
Extensions  n
(isedr:define-refinement-window "Window.FrontBn" "Rectangle" (position -0.05 0 n_offset)
(position 0.05 0.36 n_offset))
(isedr:define-refinement-window "Window.BackBn" "Rectangle" (position -0.05 0 (+ n_offset
wnn)) (position 0.05 0.36 (+ n_offset wnn)))
(isedr:define-constant-profile "Profile.ImplantBn" "BoronActiveConcentration" 6e18)
```

```
(isedr:define-constant-profile-placement "Place.Implant.FrontBn" "Profile.ImplantBn"
"Window.FrontBn")
(isedr:define-constant-profile-placement "Place.Implant.BackBn" "Profile.ImplantBn"
"Window.BackBn")



;-----------------------------------------------------------------------------------------
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; MESHING
; First pass is a doping dependent refinement that will generally do a good job
(sdedr:define-refinement-window "win.all" "Cuboid" (position subxmin 0.36 subzmin)
(position subxmax Ysub subzmax ))
(sdedr:define-refinement-size "size.all" 5.0 2 5.0  1.5 0.5 1.5)
(sdedr:define-refinement-function "size.all" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "place.all" "size.all" "win.all")


(sdedr:define-refinement-window "win.well" "Cuboid" (position subxmin 0.36 subzmin)
(position subxmax 3.0 subzmax))
(sdedr:define-refinement-size "size.well" 2.0 0.25 2.0 0.5 0.1 0.5)
(sdedr:define-refinement-function "size.well" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "place.well" "size.well" "win.well")

; STI IMPLANT n
(isedr:define-refinement-size "stin" 0.01 0.025 0.001 0.005 0.005 0.001)
(isedr:define-refinement-window "stin" "Cuboid" (position (* -1.0 Xg) 0 (+ n_offset -
0.001)) (position Xg 0.36 (+ n_offset 0.001)))
(isedr:define-refinement-function "stin" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "stin" "stin" "stin" )

; STI IMPLANT-I n
(isedr:define-refinement-size "sti1n" 0.01 0.025 0.001 0.005 0.005 0.001)
(isedr:define-refinement-window "sti1n" "Cuboid" (position (* -1.0 Xg) 0 (+ n_offset (-
wnn 0.001))) (position Xg 0.36 (+ n_offset (+ wnn 0.001))))
(isedr:define-refinement-function "sti1n" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sti1n" "sti1n" "sti1n" )

; CHANNEL REGION n
(isedr:define-refinement-size "R.Channeln" 0.01 0.05 0.05 0.005 0.02 0.005)
(isedr:define-refinement-window "R.Channeln" "Cuboid" (position -0.1 0 n_offset)
(position 0.1 0.1 (+ n_offset wnn)))
(isedr:define-refinement-function "R.Channeln" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "R.Channeln" "R.Channeln" "R.Channeln" )

; SOURCE/DRAIN REGION n
(isedr:define-refinement-size "sourcedrainn" 0.1 0.025 0.5 0.005 0.01 0.01)
(isedr:define-refinement-window "sourcedrainn" "Cuboid" (position (- (- (* -1 Lgn) Ldn)
0.06) 0 (+ n_offset -0.02)) (position (+ (+ Lgn Lsn) 0.06) 0.2 (+ (+ n_offset wnn)
0.02)))
(isedr:define-refinement-function "sourcedrainn" "DopingConcentration" "MaxTransDiff"
0.1)
(isedr:define-refinement-placement "sourcedrainn" "sourcedrainn" "sourcedrainn")

; pwell/nwell Junction between MOS's
(isedr:define-refinement-size "pnjunc" 5.0 1.0 0.5 0.5 0.5 0.05)
(isedr:define-refinement-window "pnjunc" "Cuboid" (position subxmin 0.36 1.025) (position
subxmax 1 1.225))
(isedr:define-refinement-function "pnjunc" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "pnjunc" "pnjunc" "pnjunc" )

; pwell/nwell Junction between MOS's
(isedr:define-refinement-size "pnjunc3" 5.0 1.0 0.01 0.5 0.5 0.005)
(isedr:define-refinement-window "pnjunc3" "Cuboid" (position -0.75 0.36 1.025) (position
0.75 1 1.225))
(isedr:define-refinement-function "pnjunc3" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "pnjunc3" "pnjunc3" "pnjunc3" )

; pwell/nwell Junction in front of PMOS
(isedr:define-refinement-size "pnjunc2" 5.0 1.0 0.5 0.5 0.5 0.1)
```

```
(isedr:define-refinement-window "pnjunc2" "Cuboid" (position subxmin 0.36 -0.925)
(position subxmax 1 -1.125))
(isedr:define-refinement-function "pnjunc2" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "pnjunc2" "pnjunc2" "pnjunc2" )


; n-WELL CONTACT REGION 1
(isedr:define-refinement-size "ntap" 4.0 0.2 0.5 0.75 0.05 0.1)
(isedr:define-refinement-window "ntap" "Cuboid" (position subzmin 0 (- (- nwell_con 0.02)
(* Con well_z))) (position subzmax 0.1 (+ (+ nwell_con 0.02) (* Con well_z))))
(isedr:define-refinement-function "ntap" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ntap" "ntap" "ntap" )

; p-WELL CONTACT REGION 1
(isedr:define-refinement-size "ptap" 4.0 0.2 0.5 0.75 0.05 0.1)
(isedr:define-refinement-window "ptap" "Cuboid" (position subzmin 0 (- (- pwell_con 0.02)
(* Con well_z))) (position subzmax 0.1 (+ (+ pwell_con 0.02) (* Con well_z))))
(isedr:define-refinement-function "ptap" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap" "ptap" "ptap" )

; p-WELL CONTACT REGION 4
(isedr:define-refinement-size "ptap4" 2.0 0.2 0.5 0.75 0.05 0.1)
(isedr:define-refinement-window "ptap4" "Cuboid" (position (- (/ well_strip -2) 0.1) 0 (-
-4.12 (* Con well_z))) (position (+ (/ well_strip 2) 0.1) 0.1 (+ -4.08 (* Con well_z))))
(isedr:define-refinement-function "ptap4" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap4" "ptap4" "ptap4" )

;@node@ is variable for swb (workbench)
(sde:save-model "n@node@_msh")
;---------------------------- THE END ----------------------------------------------------
--------
```

SDE script for pFET TCAD model

```
; Setting parameters

; - lateral
(define Ltot 3.5)   ; [um] Lateral extend total
(define Lg 0.08)   ; [um] Gate length
(define subzmin (/ 20 -2.0)); [um] Max. frontside extension in the z-direction
(define subzmax (/ 20 2)); [um] Max. backside extension in the z-direction
(define subxmin (/ 20 -2.0)); [um] Max. leftside extension in the x-direction
(define subxmax (/ 20 2)); [um] Max. rightside extension in the x-direction
(define wn 0.84); [um] width of the pmos device
(define Ls 0.27); [um] length of source
(define Ld 0.27); [um] length of drain
(define Ld2 0)
(define LsLeft 0)
(define LsRight 0)
(define Ld3 0)
(define LsR2 0)
; far left source LsLeft |F2| next drain Ld |F1| center source Ls |F3| next drain Ld2
|F4| far right source LsRight
(define Con 0.08); [um] dimensions of square contacts
(define well_z 1); [um] the z height of well contact
(define sd_con 3);  the number of s/d contacts

(define Lgn 0.08)   ; [um] Gate length
(define wnn 0.28); [um] width of the nmos device
(define Lsn 0.26);
(define Ldn 0.26); [um] length of drain - nmos

(define n_offset (+ wn 0.535))

(define nwell_strip 20)

(define pwell_strip 20)
```

```
(define well_strip 1.6)

(define nwell_con (- -0.1 0.665))
(define pwell_con (+ nwell_con 3.36))
(define nwellEdge (+ (- nwell_con 0.26) 2.15))
(define nwellBott (- nwellEdge 2.15))

; Layers
(define Ysub 20)   ; [um] Substrate thickness
(define Tox 14e-4) ; [um] Gate oxide thickness
(define Ypol -0.14)  ; [um] Poly gate thickness

; Substrate doping level
(define Dop 1e16) ; [1/cm3]

; Derived quantities
(define Xmax (/ Ltot 2.0))
(define Xg   (/ Lg   2.0))
(define Ygox (* Tox -1.0))

;----------------------------------------------------------------------------------------
-------
; Overlap resolution: New replaces Old
(isegeo:set-default-boolean "ABA")
;----------------------------------------------------------------------------------------
-------
; CREATE REGIONS

; SUBSTRATE REGION
(isegeo:create-cuboid (position subxmin 0 subzmin) (position subxmax Ysub subzmax)
"Silicon" "region_1" )

; GATE OXIDE REGION - Main
(isegeo:create-cuboid (position (* Xg -1.0) 0 0) (position Xg Ygox wn) "SiO2" "region_2")


; GATE OXIDE REGION - Front Extension
(isegeo:create-cuboid (position (* Xg -1.0) 0 -0.2) (position Xg Ygox 0) "SiO2"
"region_22")

; GATE OXIDE REGION - Back Extension
(isegeo:create-cuboid (position (* Xg -1.0) 0 wn) (position Xg Ygox (+ wn 0.2)) "SiO2"
"region_222")

; PolySi GATE - Main
(isegeo:create-cuboid (position (* Xg -1.0) Ygox -0.2) (position Xg Ypol (+ wn 0.2))
"PolySi" "region_3")


; STI REGION - I ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 wn) (position 2.28 0.36 n_offset) "Oxide"
"STI1" )

; STI REGION - 25 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ n_offset wnn)) (position 2.28 0.36 (- (-
pwell_con 0.02) (* Con well_z))) "Oxide" "STI25" )

; STI REGION - 26 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 n_offset) (position (- (* Xg -1) Lsn) 0.36 (+
n_offset wnn)) "Oxide" "STI26" )

; STI REGION - 27 ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position (+ Xg Lsn) 0 n_offset) (position 2.28 0.36 (+ n_offset
wnn)) "Oxide" "STI27" )


; STI REGION - III ("to the right" of S/D)
(isegeo:create-cuboid (position (+ 0.04 Ls) 0 0) (position subxmax 0.36 wn) "Oxide"
"STI3" )
```

```
; STI REGION - IV ("in front of" of S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ (+ nwell_con 0.02) (* Con well_z)))
(position subxmax 0.36 0) "Oxide" "STI4" )

; STI REGION - IX ("in front of" of nwell contacts, till the left edge of the gate
extension)
(isegeo:create-cuboid (position subxmin 0 subzmin) (position (+ 2.32 Con) 0.36 (- -4.12
(* Con well_z))) "Oxide" "STI9" )

; STI REGION - V ("in front of" of S/D, from the right edge of the gate extension to the
edge of S/D)
;;;;;;;;(isegeo:create-cuboid (position Xg 0 0) (position 0.62408 0.36 subzmin) "Oxide"
"STI5" )


; STI REGION - VI ("to the left of" of S/D)
(isegeo:create-cuboid (position subxmin 0 0) (position (- -0.04 Ld) 0.36 wn) "Oxide"
"STI6" )


; STI REGION - VI ("to the left of" of S/D)
(isegeo:create-cuboid (position subxmin 0 0) (position (- (- -0.04 LsLeft) Xgoff) 0.36
wn) "Oxide" "STI6" )


; STI REGION - VII ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 (+ (+ pwell_con 0.02) (* Con
well_z))) (position subxmax 0.36 subzmax) "Oxide" "STI7" )


; STI REGION - VIIc ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 wn) (position subxmax 0.36 (- (-
pwell_con 0.02) (* Con well_z))) "Oxide" "STI7c" )

; STI REGION - VIIb ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 (+ -4.08 (* Con well_z)))
(position subxmax 0.36 (- (- nwell_con 0.02) (* Con well_z))) "Oxide" "STI7b" )

; STI REGION - VIId ("to the right of n-well contact" of S/D)
(isegeo:create-cuboid (position (+ 0.02 (+ 2.3 Con)) 0 subzmin) (position subxmax 0.36 (-
-4.12 (* Con well_z))) "Oxide" "STI7b" )

; STI REGION - xii
(isegeo:create-cuboid (position 2.28 0 subzmin) (position (+ 0.02 (+ 2.3 Con)) 0.36 (- -
4.12 (* Con well_z))) "Oxide" "STI12" )

; STI REGION - xIII
(isegeo:create-cuboid (position 2.28 0 wn) (position (+ 0.02 (+ 2.3 Con)) 0.36 (- (-
pwell_con 0.02) (* Con well_z))) "Oxide" "STI13" )


; STI REGION - XIV ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (+ (+ pwell_con 0.02) (* Con well_z)))
(position (+ 2.32 Con) 0.36 subzmax) "Oxide" "STI14" )

; STI REGION - XV ("behind" S/D, till the left edge of the gate extension)
;(isegeo:create-cuboid (position subxmin 0 (- (- pwell_con 0.02) (* Con well_z)))
(position (/ pwell_strip -2.0) 0.36 (+ (+ pwell_con 0.02) (* Con well_z))) "Oxide"
"STI15" )

; STI REGION - XVIIc ("behind" S/D, till the left edge of the gate extension)
;(isegeo:create-cuboid (position (/ pwell_strip 2.0) 0 (- (- pwell_con 0.02) (* Con
well_z))) (position subxmax 0.36 (+ (+ pwell_con 0.02) (* Con well_z))) "Oxide" "STI17c"
)

; STI REGION - xxi ("in front of" of nwell contacts, till the left edge of the gate
extension)
(isegeo:create-cuboid (position subxmin 0 (+ -4.08 (* Con well_z))) (position (+ 2.32
Con) 0.36 (- (- nwell_con 0.02) (* Con well_z))) "Oxide" "STI21" )
```

```
; STI REGION - xxii ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 (- -4.12 (* Con well_z))) (position (/
well_strip -2.0) 0.36 (+ -4.08 (* Con well_z))) "Oxide" "STI22" )

; STI REGION - xxiv ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position (/ well_strip 2.0) 0 (- -4.12 (* Con well_z))) (position
subxmax 0.36 (+ -4.08 (* Con well_z))) "Oxide" "STI24" )

;-----------------------------------------------------------------------------------------
--------
; DEFINING AND PLACING CONTACTS

; SUBSTRATE CONTACT
(isegeo:define-contact-set "substrate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0 Ysub 0)) "substrate")


; GATE CONTACT
(isegeo:define-contact-set "gate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0 Ypol 0.175)) "gateA_pmos")

; DRAIN CONTACT
(define drainCon (* -1 (+ -0.02 (/ Ld 2))))
(isegeo:create-cuboid (position drainCon 0 (/ wn 4)) (position (- drainCon 0.12) -0.2 (*
0.75 wn)) "Metal" "Drainmetal")
(isegeo:define-contact-set "drain_pmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position (- drainCon 0.06) 0 (/ wn 2)))
"drain_pmos")
(isegeo:delete-region (find-body-id (position (- drainCon 0.06) -0.1 (/ wn 2))))

; SOURCE CONTACT
(define sourceCon (+ -0.02 (/ Ls 2)))
(isegeo:create-cuboid (position sourceCon 0 (* 0.25 wn)) (position (+ sourceCon 0.12) -
0.2 (* 0.75 wn)) "Metal" "Sourcemetal")
(isegeo:define-contact-set "source_pmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position (+ sourceCon 0.06) 0 (/ wn 2)))
"source_pmos")
(isegeo:delete-region (find-body-id (position (+ sourceCon 0.06) -0.1 (/ wn 2))))



; n-WELL CONTACT 1 (this would be connected to Vdd, along with the source)
(isegeo:create-cuboid (position subxmin 0 (- nwell_con (* 0.12 0.5))) (position subxmax -
0.2 (+ nwell_con (* 0.12 0.5))) "Metal" "nwell")
(isegeo:define-contact-set "nwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.09 0 nwell_con)) "nwell")
(isegeo:delete-region (find-body-id (position 0.09 -0.1 nwell_con)))


; p-WELL CONTACT 1
(isegeo:create-cuboid (position -5 0 (- pwell_con (* 0.12 0.5))) (position 5 -0.2 (+
pwell_con (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.09 0 pwell_con)) "pwell")
(isegeo:delete-region (find-body-id (position 0.09 -0.1 pwell_con)))

; p-WELL CONTACT 11
(isegeo:create-cuboid (position -0.64 0 (- -4.1 (* 0.12 0.5))) (position (- -0.64 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.66 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.66 -0.1 -4.1)))

; p-WELL CONTACT 12
(isegeo:create-cuboid (position 0.64 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.64 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.66 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.66 -0.1 -4.1)))
```

```
; p-WELL CONTACT 4
(isegeo:create-cuboid (position 0.08 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.08 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.09 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.09 -0.1 -4.1)))

; p-WELL CONTACT 5
(isegeo:create-cuboid (position 0.36 0 (- -4.1 (* 0.12 0.5))) (position (+ 0.36 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.37 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position 0.37 -0.1 -4.1)))

; p-WELL CONTACT 6
(isegeo:create-cuboid (position -0.08 0 (- -4.1 (* 0.12 0.5))) (position (- -0.08 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.09 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.09 -0.1 -4.1)))

; p-WELL CONTACT 8
(isegeo:create-cuboid (position -0.36 0 (- -4.1 (* 0.12 0.5))) (position (- -0.36 0.12) -
0.2 (+ -4.1 (* 0.12 0.5))) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.37 0 -4.1)) "pwell")
(isegeo:delete-region (find-body-id (position -0.37 -0.1 -4.1)))


;-------------------------------------------------------------------------------------------
---------
; SET DOPING REGIONS AND PROFILES

; CONSTANT DOPING PROFILES

; SUBSTRATE REGION AND PROFILE
(isedr:define-constant-profile "region_1" "BoronActiveConcentration" Dop )
(isedr:define-constant-profile-region  "region_1" "region_1" "region_1" )



; PolySi GATE REGION AND PROFILE - Main
(isedr:define-constant-profile "region_3" "BoronActiveConcentration" 1e20)
(isedr:define-constant-profile-region "region_3" "region_3" "region_3")

;-------------------------------------------------------------------------------------------
---------
; ANALYTICAL DOPING PROFILES

; SUBSTRATE (LATCHUP) PROFILE (IN BETWEEN THE n-WELL AND THE SUBSTRATE)
(isedr:define-refinement-window "Latchup.Profile.Region" "Rectangle" (position subxmin
1.25 subzmin) (position subxmax 1.25 subzmax))
(isedr:define-gaussian-profile "Latchup.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Latchup.Profile.Place" "Latchup.Profile"
"Latchup.Profile.Region" "Symm" "NoReplace" "Eval")


; n-WELL PROFILE OF THE PMOS DEVICE
(isedr:define-refinement-window "nwell.Profile.Region" "Rectangle" (position subxmin 0.65
nwellBott) (position subxmax 0.65 nwellEdge))
(isedr:define-gaussian-profile "nwell.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 1e17 "ValueAtDepth" 1e16 "Depth" 0.65 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "nwell.Profile.Place" "nwell.Profile"
"nwell.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL PROFILE behind the nwell
(isedr:define-refinement-window "pwell1.Profile.Region" "Rectangle" (position subxmin
0.55 (+ nwellEdge 0.05)) (position subxmax 0.55 subzmax))
(isedr:define-gaussian-profile "pwell1.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.55 "Gauss" "Factor" 0.0001)
```

```
(isedr:define-analytical-profile-placement "pwell1.Profile.Place" "pwell1.Profile"
"pwell1.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL PROFILE in front of the nwell
(isedr:define-refinement-window "pwell2.Profile.Region" "Rectangle" (position subxmin
0.55 subzmin) (position subxmax 0.55 (- nwellBott 0.05)))
(isedr:define-gaussian-profile "pwell2.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.55 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwell2.Profile.Place" "pwell2.Profile"
"pwell2.Profile.Region" "Symm" "NoReplace" "Eval")

; n-WELL CONTACT PROFILE (DEGENRATE DOPING FOR n-WELL CONTACT) 1
(isedr:define-refinement-window "nwelltap.Profile.Region" "Rectangle" (position subxmin 0
(- (- nwell_con 0.02) (* Con well_z))) (position subxmax 0 (+ (+ nwell_con 0.02) (* Con
well_z))))
(isedr:define-gaussian-profile "nwelltap.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "nwelltap.Profile.Place" "nwelltap.Profile"
"nwelltap.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT) 1
(isedr:define-refinement-window "pwelltap.Profile.Region" "Rectangle" (position subxmin 0
(- (- pwell_con 0.02) (* Con well_z))) (position subxmax 0 (+ (+ pwell_con 0.02) (* Con
well_z))))
(isedr:define-gaussian-profile "pwelltap.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap.Profile.Place" "pwelltap.Profile"
"pwelltap.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT) 4
(isedr:define-refinement-window "pwelltap4.Profile.Region" "Rectangle" (position (/
well_strip -2.0) 0 (- -4.12 (* Con well_z))) (position (/ well_strip 2.0) 0 (+ -4.08 (*
Con well_z))))
(isedr:define-gaussian-profile "pwelltap4.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap4.Profile.Place" "pwelltap4.Profile"
"pwelltap4.Profile.Region" "Symm" "NoReplace" "Eval")

; SOURCE
(isedr:define-refinement-window "source.Profile.Region" "Rectangle" (position 0.068 0 0)
(position (+ Xg Ls) 0 wn))
(isedr:define-gaussian-profile "source.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.Place" "source.Profile"
"source.Profile.Region" "Symm" "NoReplace" "Eval")

; DRAIN
(isedr:define-refinement-window "drain.Profile.Region" "Rectangle" (position -0.068 0 0)
(position (- (* -1 Xg) Ld) 0 wn))
(isedr:define-gaussian-profile "drain.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.Place" "drain.Profile"
"drain.Profile.Region" "Symm" "NoReplace" "Eval")

; LDD - SOURCE
(isedr:define-refinement-window "sourceldd.Profile.Region" "Rectangle" (position (/ 0.05
2) 0.0 0) (position 0.072 0 wn))
(isedr:define-gaussian-profile "sourceldd.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.Place" "sourceldd.Profile"
"sourceldd.Profile.Region" "Symm" "NoReplace" "Eval")

; LDD - DRAIN
(isedr:define-refinement-window "drainldd.Profile.Region" "Rectangle" (position (/ 0.05 -
2) 0.0 0) (position -0.072 0 wn))
(isedr:define-gaussian-profile "drainldd.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 4e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.Place" "drainldd.Profile"
"drainldd.Profile.Region" "Symm" "NoReplace" "Eval")
```

```
; DRAIN HALO
(isedr:define-refinement-window "HDimplant.Profile.Region" "Rectangle" (position -0.02
0.04 0) (position -0.025 0.04 wn))
(isedr:define-gaussian-profile "HDimplant.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 5e17 "ValueAtDepth" 1e15 "Depth" 0.035 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HDimplant.Profile.Place" "HDimplant.Profile"
"HDimplant.Profile.Region" "Symm" "NoReplace" "Eval")

; SOURCE HALO
(isedr:define-refinement-window "HSimplant.Profile.Region" "Rectangle" (position 0.02
0.04 0) (position 0.025 0.04 wn))
(isedr:define-gaussian-profile "HSimplant.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 5e17 "ValueAtDepth" 5e15 "Depth" 0.035 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HSimplant.Profile.Place" "HSimplant.Profile"
"HSimplant.Profile.Region" "Symm" "NoReplace" "Eval")

; Vt IMPLANT
(isedr:define-refinement-window "implant.Profile.Region" "Rectangle" (position (/ 0.035 -
2.0) 0.01 0) (position (/ 0.035 2.0) 0.01 wn))
(isedr:define-gaussian-profile "implant.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 8e18 "ValueAtDepth" 6e17 "Depth" 0.03 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.Place" "implant.Profile"
"implant.Profile.Region" "Symm" "NoReplace" "Eval")

; IMPLANT TO MITIGATE LEAKAGE (BELOW Vt IMPLANT)
;(isedr:define-refinement-window "limplant.Profile.Region" "Rectangle" (position -0.03
0.035 0) (position 0.03 0.035 wn))
;(isedr:define-gaussian-profile "limplant.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 8e18 "ValueAtDepth" 5e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "limplant.Profile.Place" "limplant.Profile"
"limplant.Profile.Region" "Symm" "NoReplace" "Eval")

; SIDEWALL IMPLANT
(isedr:define-refinement-window "Window.FrontB" "Rectangle" (position (* Xg -1.0)  0 wn)
(position  Xg  0.36 wn))
(isedr:define-refinement-window "Window.BackB" "Rectangle" (position (* Xg -1.0) 0 0)
(position Xg 0.36 0))
(isedr:define-constant-profile "Profile.ImplantB" "ArsenicActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontB" "Profile.ImplantB"
"Window.FrontB")
(isedr:define-constant-profile-placement "Place.Implant.BackB" "Profile.ImplantB"
"Window.BackB")



;-----------------------------------------------------------------------------------------
----------------------------------
; MESHING
; First pass is a doping dependent refinement that will generally do a good job
(sdedr:define-refinement-window "win.all" "Cuboid" (position subxmin 0.36 subzmin)
(position subxmax Ysub subzmax ))
(sdedr:define-refinement-size "size.all" 5.0 2 5.0  1.5 0.5 1.5)
(sdedr:define-refinement-function "size.all" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "place.all" "size.all" "win.all")

(sdedr:define-refinement-window "win.well" "Cuboid" (position subxmin 0.36 subzmin)
(position subxmax 3.0 subzmax))
(sdedr:define-refinement-size "size.well" 2.0 0.25 2.0 0.5 0.1 0.5)
(sdedr:define-refinement-function "size.well" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "place.well" "size.well" "win.well")

; STI IMPLANT
(isedr:define-refinement-size "sti" 0.05 0.025 0.01 0.005 0.005 0.001)
(isedr:define-refinement-window "sti" "Cuboid" (position (* -1.2 Xg) 0 -0.001) (position
(* 1.2 Xg) 0.36 0.001))
(isedr:define-refinement-function "sti" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sti" "sti" "sti" )

; STI-I IMPLANT
(isedr:define-refinement-size "sti1" 0.05 0.025 0.01 0.005 0.005 0.001)
```

```
(isedr:define-refinement-window "sti1" "Cuboid" (position (* -1.2 Xg) 0 (- wn 0.001))
(position (* 1.2 Xg) 0.36 (+ wn 0.001)))
(isedr:define-refinement-function "sti1" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sti1" "sti1" "sti1" )


; CHANNEL REGION
(isedr:define-refinement-size "R.Channel" 0.01 0.1 0.05 0.005 0.05 0.005)
(isedr:define-refinement-window "R.Channel" "Cuboid" (position -0.09 0 0) (position 0.09
0.08 wn))
(isedr:define-refinement-function "R.Channel" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "R.Channel" "R.Channel" "R.Channel" )


; SOURCE/DRAIN REGION
(isedr:define-refinement-size "sourcedrain" 0.1 0.025 0.5 0.005 0.01 0.01)
(isedr:define-refinement-window "sourcedrain" "Cuboid" (position (- (* -1 (+ (+ Lg Ld)
0.06)) 0) 0 -0.02) (position (+ (+ (+ Lg Ls) 0.06) 0) 0.15 (+ wn 0.02)))
(isedr:define-refinement-function "sourcedrain" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sourcedrain" "sourcedrain" "sourcedrain")


; pwell/nwell Junction between MOS's
(isedr:define-refinement-size "pnjunc" 5.0 1.0 0.5 0.5 0.5 0.05)
(isedr:define-refinement-window "pnjunc" "Cuboid" (position subxmin 0 (- nwellEdge 0.1))
(position subxmax 1.0 (+ nwellEdge 0.1)))
(isedr:define-refinement-function "pnjunc" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "pnjunc" "pnjunc" "pnjunc" )

; pwell/nwell Junction in front of PMOS
(isedr:define-refinement-size "pnjunc2" 5.0 1.0 0.5 0.5 0.5 0.1)
(isedr:define-refinement-window "pnjunc2" "Cuboid" (position subxmin 0 (- nwellBott 0.1))
(position subxmax 1.0 (+ nwellBott 0.1)))
(isedr:define-refinement-function "pnjunc2" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "pnjunc2" "pnjunc2" "pnjunc2" )

; n-WELL CONTACT REGION 1
(isedr:define-refinement-size "ntap" 4.0 0.2 0.5 0.75 0.05 0.1)
(isedr:define-refinement-window "ntap" "Cuboid" (position subxmin 0 (- (- nwell_con 0.02)
(* Con well_z))) (position subxmax 0.1 (+ (+ nwell_con 0.02) (* Con well_z))))
(isedr:define-refinement-function "ntap" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ntap" "ntap" "ntap" )

; p-WELL CONTACT REGION 1
(isedr:define-refinement-size "ptap" 4.0 0.2 0.5 0.75 0.05 0.1)
(isedr:define-refinement-window "ptap" "Cuboid" (position subxmin 0 (- (- pwell_con 0.02)
(* Con well_z))) (position subxmax 0.1 (+ (+ pwell_con 0.02) (* Con well_z))))
(isedr:define-refinement-function "ptap" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap" "ptap" "ptap" )

; p-WELL CONTACT REGION 4
(isedr:define-refinement-size "ptap4" 0.5 0.05 0.1 0.05 0.005 0.01)
(isedr:define-refinement-window "ptap4" "Cuboid" (position (- (/ well_strip -2) 0.1) 0 (-
-4.12 (* Con well_z))) (position (+ (/ well_strip 2) 0.1) 0.1 (+ -4.08 (* Con well_z))))
(isedr:define-refinement-function "ptap4" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap4" "ptap4" "ptap4" )



;@node@ is a variable for swb (workbench)
(sde:save-model "n@node@_msh")
;---------------------------- THE END -------------------------------------------------
--------
```

Sample SDevice script for mixed-mode inverter p-hit simulation (normal incidence with LET 40 MeV-cm^2/mg)

```
DEVICE pmos{
```

```
  #@grid@ and @doping@ are the .grd and .dat files kept track of by workbench
  File {
    Grid =  "@grid@"
    Doping = "@doping@"
  }

  Electrode {
    { Name="drain_pmos"               Voltage=0.0 }
    { Name="gateA_pmos"               Voltage=0.0 }
    { Name="source_pmos"      Voltage=0.0 }
    { Name="nwell"            Voltage=0.0 }
    { Name="pwell"            Voltage=0.0 }
    { Name="substrate"                Voltage=0.0 Resistor=1000 }
  }

  Physics {
      Recombination(SRH Auger) #TPA_gen
      Mobility( DopingDep HighFieldsat Enormal CarrierCarrierScattering)
      EffectiveIntrinsicDensity( OldSlotboom )
       HeavyIon(
              time=1e-10
              length=21
              wt_hi=0.05
              Location=(@Xion@,0,@Zion@)
              Direction=(0,1,0)
              LET_f=0.4
              Gaussian
              PicoCoulomb )
       }

Plot    {
       eDensity  hDensity
       Potential  SpaceCharge  ElectricField
       equasiFermi hquasiFermi
       Doping  DonorConcentration   AcceptorConcentration
       eCurrent/Vector hCurrent/Vector
       TotalCurrent/Vector
       HeavyIonChargeDensity
       }
}

Math    {
        WallClock
       Extrapolate
       Derivatives
       RelErrControl
       Iterations=15
       notdamped=100
       Newdiscretization
       Method=ILS
       RecBoxIntegr
       Transient=BE
       ExitOnFailure
       }

File {
  SPICEPath = "."
  Plot=   "n@node@_des.dat"
  Current="n@node@_des.plt"
  Output= "n@node@_des"
}

System {
  Vsource_pset Vdd (HIGH 0) {dc = 1.2}
  Vsource_pset Ground (GD 0) {dc = 0.0}

  pmos m1 ("drain_pmos"=Out "gateA_pmos"=In "source_pmos"=HIGH "nwell"=HIGH "pwell"=GD
"substrate"=GD)

  rvt_nfet m2 (Out In GD GD)
       {w = 0.28e-6   l = 0.08e-6
```

```
       pd = 1.095e-6  ps = 1.095e-6
       ad = 74.9e-15  as = 74.9e-15}

# input inv_1x with input of 0
  rvt_pfet mi2 (In GD HIGH HIGH)
       {w = 0.84e-6   l = 0.08e-6
       pd = 2.215e-6  ps = 2.215e-6
       ad = 224.7e-15 as = 224.7e-15}

  rvt_nfet mi1 (In GD GD GD)
       {w = 0.28e-6   l = 0.08e-6
       pd = 1.095e-6  ps = 1.095e-6
       ad = 74.9e-15  as = 74.9e-15}

# loaded with inv_1x
  rvt_pfet mL2 (Out2 Out HIGH HIGH)
       {w = 0.84e-6   l = 0.08e-6
       pd = 2.215e-6  ps = 2.215e-6
       ad = 224.7e-15 as = 224.7e-15}

  rvt_nfet mL1 (Out2 Out GD GD)
       {w = 0.28e-6   l = 0.08e-6
       pd = 1.095e-6  ps = 1.095e-6
       ad = 74.9e-15  as = 74.9e-15}

  Initialize (Out = 0.0)
  Initialize (In = 1.2)
  Initialize (Out2 = 1.2)

  Plot "n@node@_des_sys" (time() v(Out) v(In) v(Out2))

}

Solve {

Transient (
       InitialTime=0
       FinalTime=0.9e-10
       InitialStep=1e-11
       MaxStep=1e-10
        )
        {
       coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
       }

Transient (
        InitialTime=0.9e-10
        FinalTime=1.05e-10
        InitialStep=1e-13
        MaxStep=0.5e-12
         )
        {
        coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
        }

Transient (
        InitialTime=1.05e-10
        FinalTime=3.05e-10
        InitialStep=2e-12
        MaxStep=3e-12
         )
        {
        coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
       }

Transient (
        InitialTime=3.05e-10
        FinalTime=5e-10
        InitialStep=1e-11
        MaxStep=2e-11
         )
```

```
        {
        coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
        Plot (Time=(3.5e-10) FilePrefix="SE_Data250ps_@node@" NoOverwrite)
        }

Transient (
        InitialTime=5e-10
        FinalTime=1.1e-9
        InitialStep=1e-11
        MaxStep=2e-11
         )
        {
        coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
        }
Transient (
        InitialTime=1.1e-9
        FinalTime=3e-9
        InitialStep=1e-11
        MaxStep=5e-11
         )
        {
        coupled {m1.poisson m1.electron m1.hole m1.contact circuit}
        }
}
```

B. Carrier-carrier scattering models for SE simulation

When carrier concentrations become high enough, mobilities decrease due to carrier-carrier scattering effects. In [26], two commonly used carrier-carrier scattering models, the Philips model and the Dorkel-Leturcq model, were compared for applicability to SE simulation. The author states that in simulating the high-injection of a heavy ion strike, "the carrier-carrier model represents the largest source of uncertainty" [26]. This is because neither model has been calibrated up to the carrier concentrations that would be seen in an ion strike. The conclusion in [26] is that the Dorkel-Leturcq (which is basically the Conwell-Weisskopf model in SDevice) is preferred to the Philips model in SE simulation because to be valid, the Philips model requires device heating effects to be included. These effects are not supported by many device simulators, including SDevice. This is one of the reasons for using the Conwell-Weisskopf carrier-carrier model.

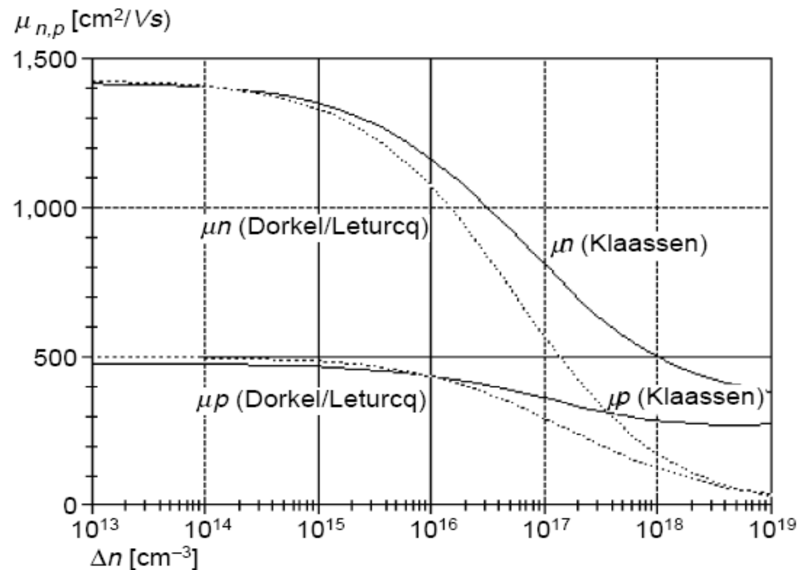

Fig. 71: Comparison of Dorkel/Leturcq (Conwell-Weisskopf in SDevice) and Klaassen (Philips in SDevice) carrier-carrier scattering models [27]

In addition, the actual mobilities calculated by these models are compared and plotted against carrier concentration in Fig. 71 from [27]. For both electrons and holes, the mobilities calculated by the Dorkel/Leturcq model are much lower than those calculated by the Klaassen model. In relating this to the SE response of a device, the Klaassen model would predict higher currents resulting in shorter SETs while the Dorkel/Leturcq model would predict lower currents resulting in longer SETs. Since the overarching goal of this work was to simulate worst-case SETs in a digital cell library, the model with lower mobility was chosen to produce longer SETs, thus ensuring the worst-case. For consistency, this model was also used for the simulations not directly involved in the library characterization.

There are four carrier-carrier scattering models available in the TCAD simulator SDevice: Conwell-Weisskopf (basically the same as the Dorkel/Leturcq), Brooks-Herring, Philips unified model using Klaassen, and Philips unified model using Meyer [17]. In order to understand how each model affects single events, a normal strike at LET of 40 MeV-cm^2/mg was simulated in the full 3-D 1x inverter. Strikes on both the nFET and pFET were performed using each physics model. Figure 72 shows the n-hit current and voltage waveforms. As described in the literature, the Klaassen model results in higher currents than the Conwell-Weisskopf model, due to the difference in mobilities at high carrier concentrations. The result of the Conwell-Weisskopf model's low mobility is a longer current and voltage transient; the SET pulse width is double the pulse without any carrier-carrier scattering. On the other hand, the Klaassen model decreases the SET pulse width, but not quite as noticeably.

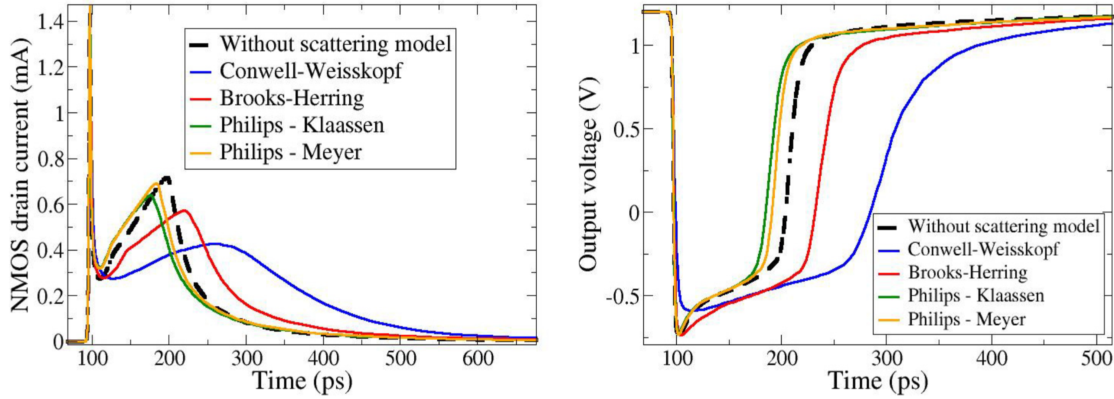

Fig. 72: SET (a) currents and (b) voltages resulting from n-hits on full 3-D 1x inverter using different carrier-carrier scattering models in SDevice

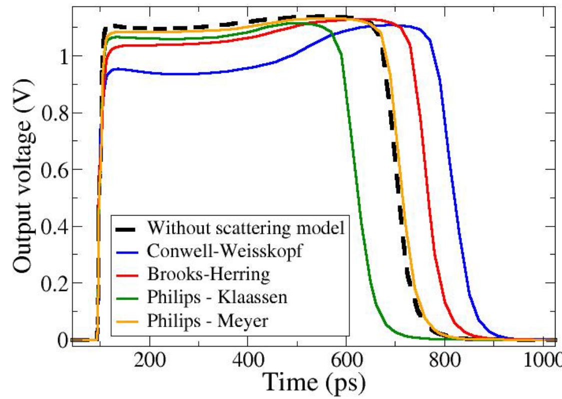

Fig. 73: SET voltage pulses resulting from p-hits on full 3-D 1x inverter using different carrier-carrier scattering models in SDevice

Figure 73 shows the effect of carrier-carrier model on p-hit voltage pulses in the same full 3-D inverter model. Instead of doubling the pulse width, the Conwell-Weisskopf only increases it by about 25%, but it still produces the longest pulse. The Klaassen model shortens the pulse by about 20%, as opposed to barely shortening it in the n-hit case. The percent change in pulse width is much more dramatic for the n-hit, but the absolute change (~100–150 ps) is quite similar for both strikes. Roughly speaking, the uncertainty in pulse width due to carrier-carrier scattering can be bounded by the variations seen in Figure 72. Since the Conwell-Weisskopf model produces the worst-case pulses, it is the model used for all simulations in this work. For further

reading on mobility modeling in single-event simulation, the reader is referred to [28]-[29].

C. Effects of doping variations on SETs

N-well doping profile

One very important issue encountered in this work was an uncertainty in the n-well doping profile. The original 90-nm device models were based on the IBM 8SF 130 nm doping information [25], and, in fact, the same well and substrate doping profiles were used. However, the n-well doping profile used throughout this work, with peak value at $1x10^{17}$ cm^{-3}, is actually low compared to the 130 nm process information, which peaks at $2x10^{17}$ cm^{-3} [25]. This appendix describes a sensitivity study of SET dependence on n-well doping profile.

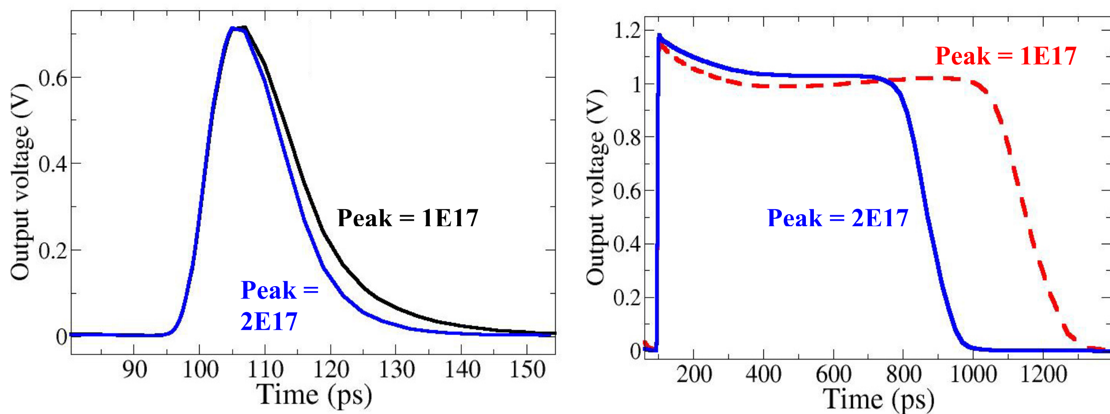

Fig. 74: SET voltage pulses resulting from 75° p-hits at (a) LET = 1 MeV-cm^2/mg and (b) LET = 40 MeV-cm^2/mg for two n-well doping profiles

The first set of simulations performed simply compared SET pulses obtained from models using two different n-well doping profiles. One model has a Gaussian doping profile with a peak of $1x10^{17}$ cm^{-3}, dropping down to $1x10^{16}$ cm^{-3} 0.65 µm away from the peak. The second model has the same Gaussian profile, but peaks at $2x10^{17}$ cm^{-3} and

drops down to 2×10^{16} cm^{-3} at 0.65 μm. For both profiles, the peak is 0.65 μm below the silicon surface (0.29 μm below the bottom of the STI). A 75° strike along the n-well is simulated on a pFET with W = 840 nm in a current-matched inverter. The effect of the well doping is different depending on LET, as shown in Figure 74.

The strikes at low LET of 1 MeV-cm^2/mg in Fig. 74(a) show very little difference between the two n-well profiles, while the high LET strikes of 40 MeV-cm^2/mg in Fig. 74(b) show a 30% decrease in pulse width when the n-well doping concentration is doubled. Since bipolar amplification is such a strong contributor to SE response of high-LET p-hits [21]-[22], these results suggest that the n-well doping may primarily affect the parasitic bipolar effect.

To test this hypothesis, a third n-well doping profile is created that has the low doping profile (peak of 1×10^{17} cm^{-3}) throughout the entire n-well except immediately below the n-well contact. Under the n-well contact, the higher doping profile (peak of 2×10^{17} cm^{-3}) is used. Thus, any effect the higher doping has on the actual device behavior is eliminated, while the impact of the doping on the resistive path to the n-well contact is included. The resistive path between the device and the n-well contact, which can be controlled by device-to-contact spacing or well-contact size, has a dramatic effect on pulse-width via bipolar amplification [21]. The higher doping immediately under the n-well contact is simply another way of reducing that resistance, which reduces the bipolar amplification, resulting in a shorter SET pulse.

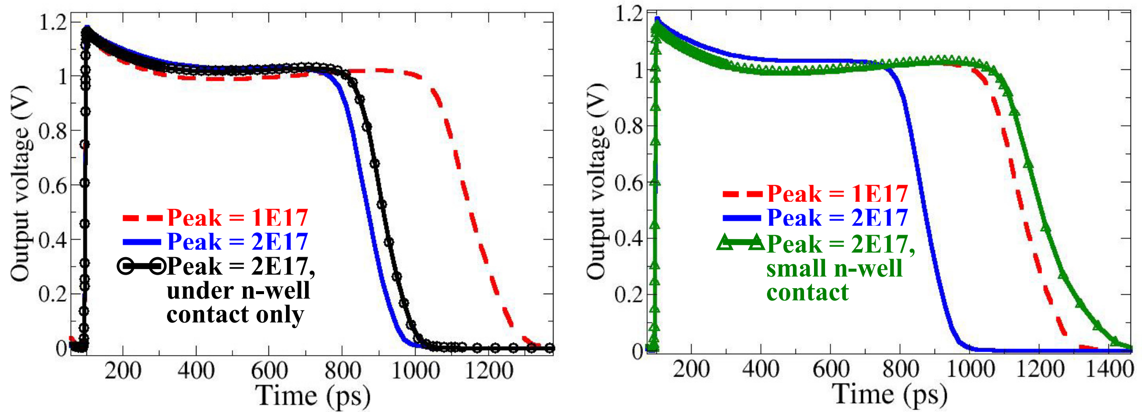

Fig. 75: (a) SET voltage pulses resulting from 75° p-hits at LET = 40 MeV-cm^2/mg for three n-well doping profiles. (b) SET voltage pulses resulting from 75° p-hits at LET = 40 MeV-cm^2/mg for two n-well doping profiles and one variation on contact size.

As the simulation results in Fig. 75(a) demonstrate, limiting the region of the higher doping profile to the region under the n-well contact produces nearly the same result as using the higher doping throughout the entire well. This result is because the primary effect of the higher n-well doping for single events is a decrease in the resistance between the device and the n-well contact. Since the resistance between the device body and V_{DD} through the well contact is the primary parameter, then the doping profile with a peak of 2×10^{17} cm^{-3} could be used throughout the n-well but with reduced n-well contact area. This decreased contact area would increase the resistance to the contact, counteracting the decreased resistance due to higher doping. The contact area used in prior simulations was 4 μm^2, so the n-well contact area is reduced to 1 μm^2 to test this theory. Figure 75(b) shows the result of this small n-well contact simulation compared to the simulations with the original contact area of 4 μm^2. As expected, the small contact essentially adds back the resistance that was reduced by the increased doping concentration, resulting in a pulse width within 5% of the strike with doping peak of 1×10^{17} cm^{-3}. This further confirms that n-well doping variations of this relatively small

magnitude primarily affect SE response by altering the resistive path from device to n-well contact. This, in turn, affects bipolar amplification in the pMOSFET which is a primary mechanism determining SET pulse width [21].

Anti-punch-through implant

Another source of uncertainty in the doping profiles is the presence of an anti-punch-through (APT) implant immediately under the source/drain diffusions. The simulations throughout this work have not used any such implant, although literature on modern processes suggests it may be present, as shown in Fig. 76 from [30]. To understand how an APT implant influences SE response, a brief sensitivity study was performed via simulation.

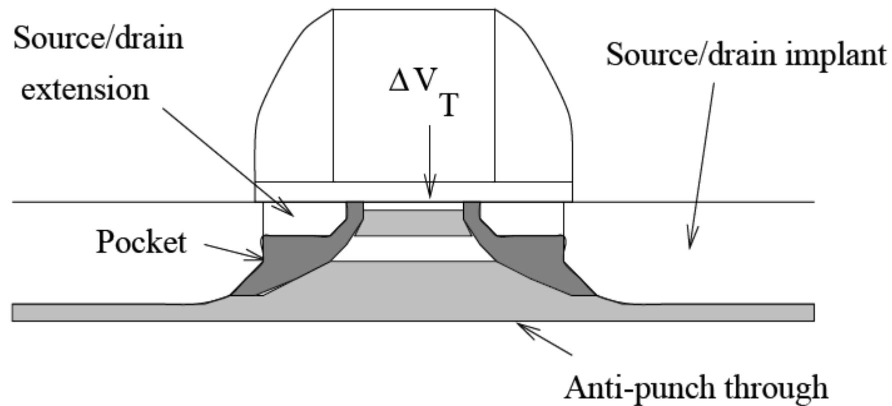

Fig. 76: Sketch of 180-nm device showing anti-punch-through implant [30]

The 1x inverter pFET was modeled both with and without an anti-punch through implant (Figures 77(a) and (b), respectively). The implant was simply modeled as a Gaussian profile with a peak concentration of 1×10^{18} cm^{-3} centered 120 nm below the silicon surface (roughly 60 nm below the drain bottom). The concentration 1×10^{18} cm^{-3} was chosen to be comparable to the V_T and halo implants. To illustrate the differences in

the models, 1-D cuts through the drains are taken along the cut-lines shown in Figure 77. Figure 78 shows the electron and hole concentrations along these cut-lines after biasing each device with gate, source, and n-well connected to V_{DD} (1.2 V) and drain connected to ground.

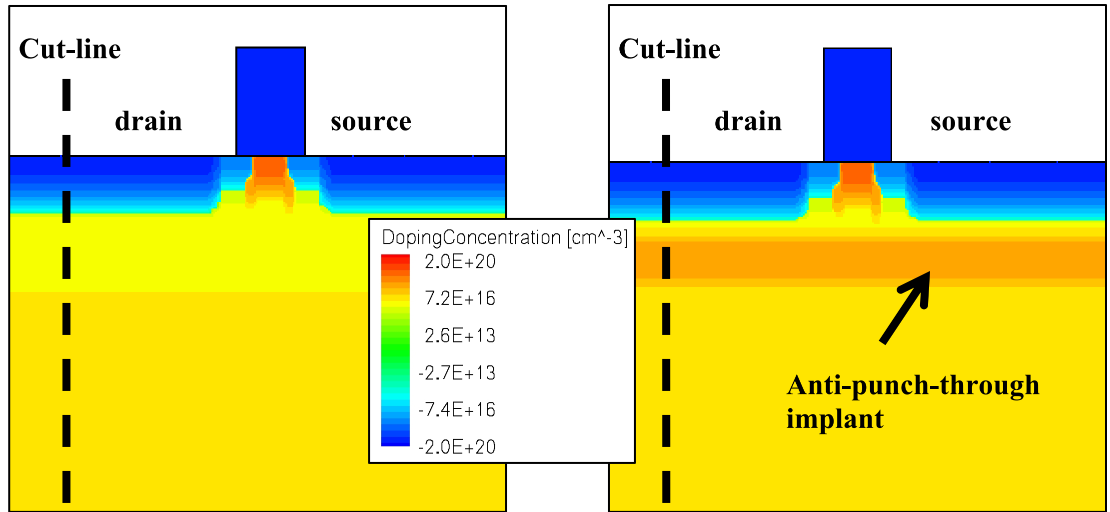

Fig. 77: Cross section of pFET TCAD model (a) without and (b) with anti-punch-through implant. Cut-line through drain for Fig. 78 is shown.

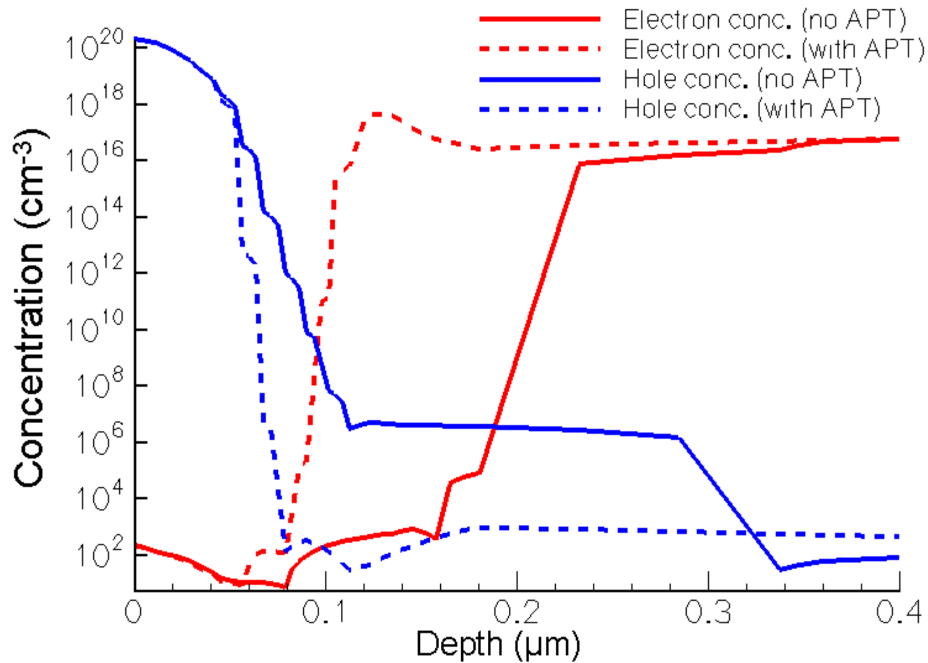

Fig. 78: Electron and hole concentrations of pFET with and without anti-punch-through (APT) implant. 1-D cutlines shown in Fig. 77

Ion strikes were simulated in both structures and compared. Mixed-mode inverter simulations were performed with the pFET of width 840 nm in TCAD and the nFET of width 280 nm in Spice. First, a normal strike with LET of 1 MeV-cm^2/mg was simulated through the drain in both models. The results in Fig. 79 show that, at low LET, the APT implant mitigates the voltage and current transient in both height and duration. This is due to the thinner depletion region between drain and n-well, since the APT implant increases the donor concentration immediately beneath the drain by several orders of magnitude. The thinner depletion region resulted in less charge separation and, therefore, less collection by the drain. At low LET the potential in the n-well does not drop dramatically, so the parasitic bipolar device does not turn on, leaving drift and diffusion as the primary charge collection mechanisms.

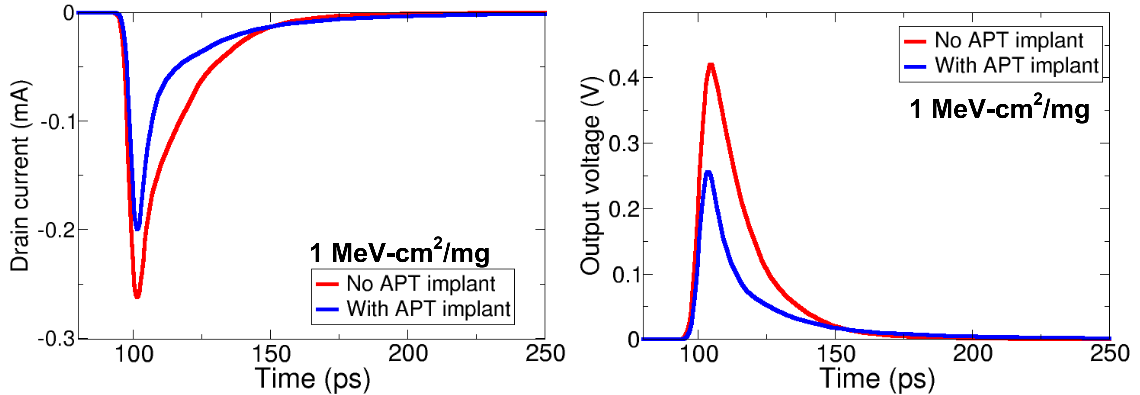

Fig. 79: Comparison of (a) SE drain currents and (b) voltage SETsresulting from normal strike on pFET with and without anti-punch-through implant. LET = 1 MeV-cm^2/mg

While the APT implant changes the low LET response, the response to a high LET strike of 40 MeV-cm^2/mg shows nearly no change with the addition of the APT implant. The current and voltage SETs of the two models shown in Fig. 80 are nearly identical. As the ion liberates electron-hole pairs, the carrier concentration exceeds the doping in the n-well, including the APT implant. Thus, the behavior of these high-

concentration carriers is relatively independent of the additional doping profile, resulting in the usual de-biasing of the n-well and bipolar amplification of SE current.

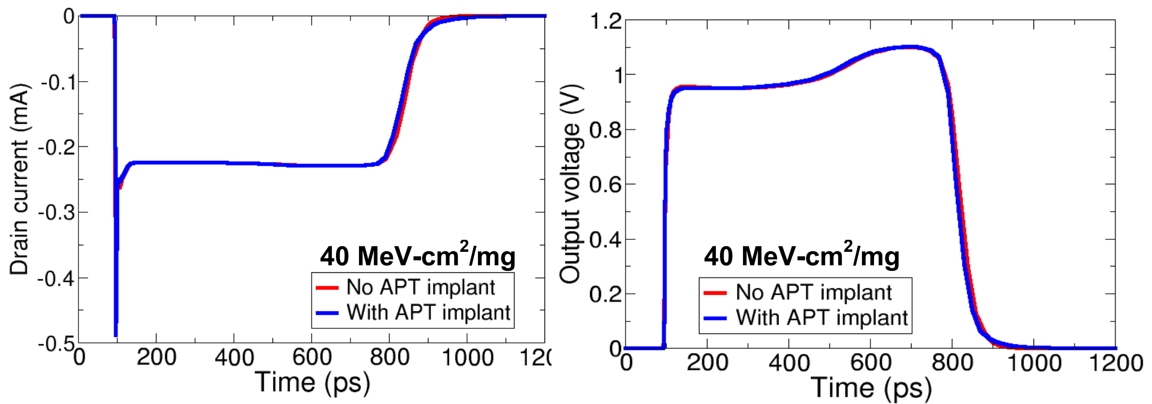

Fig. 80: Comparison of (a) SE drain currents and (b) voltage SETs resulting from normal strike on pFET with and without anti-punch through implant. LET = 40 MeV-cm^2/mg

These simulations show that the APT implant has the exact opposite effect as the n-well doping profile. An increase in doping immediately under the device only alters the SE response at low LETs where simple drift and diffusion processes regulate charge collection. Conversely, an increase in doping throughout the n-well has little effect on the charge collected after a low-LET ion strike. At high LET, the n-well de-biases and bipolar amplification becomes one of the dominant charge collection mechanisms, which renders the APT implant immediately under the device ineffectual in changing the SE response. Conversely, higher doping throughout the n-well reduces the resistive path to the n-well contact which stabilizes the well potential more effectively and reduces the charge collected via bipolar processes

<u>Anti-leakage implant</u>

The final source of uncertainty was the exact doping profile of the V_T and anti-leakage implants of the nMOS and pMOS devices in this process. In this work, it was

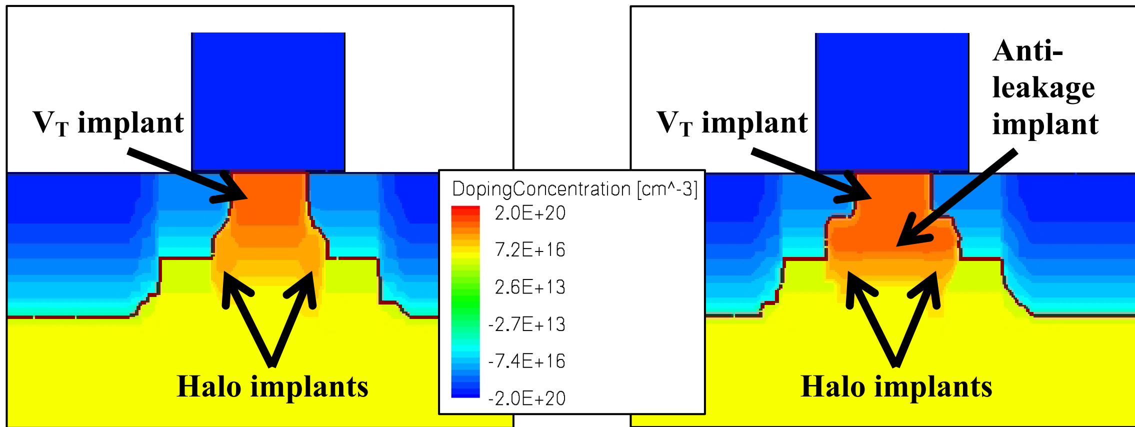

Fig. 81: PMOS device models (a) **without** and (b) **with** anti-leakage implant

found that in the high-injection situation of a single event, the device response is rather insensitive to variations in these implants. This is largely due to the struck device being simulated in the off state, where only leakage current is affected by these implants, and the single-event current greatly exceeds the leakage current. To illustrate this insensitivity, four comparative simulations are performed. Low- and high-LET strikes are simulated on pFET models with and without the anti-leakage implant, which resides directly below the V_T implant. Cross sections of each pFET model are displayed in Fig. 81.

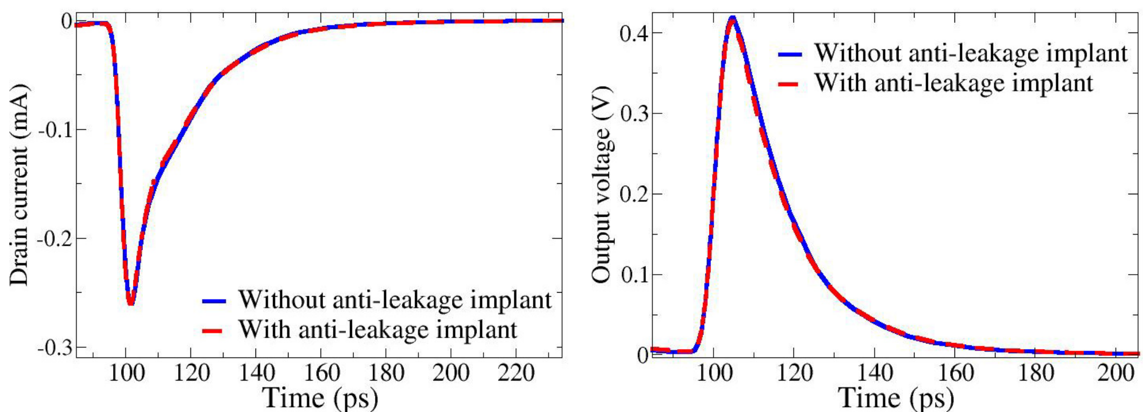

Fig. 82: SE (a) current and (b) voltage transients from normal strike with LET 1 MeV-cm^2/mg, with and without anti-leakage implant

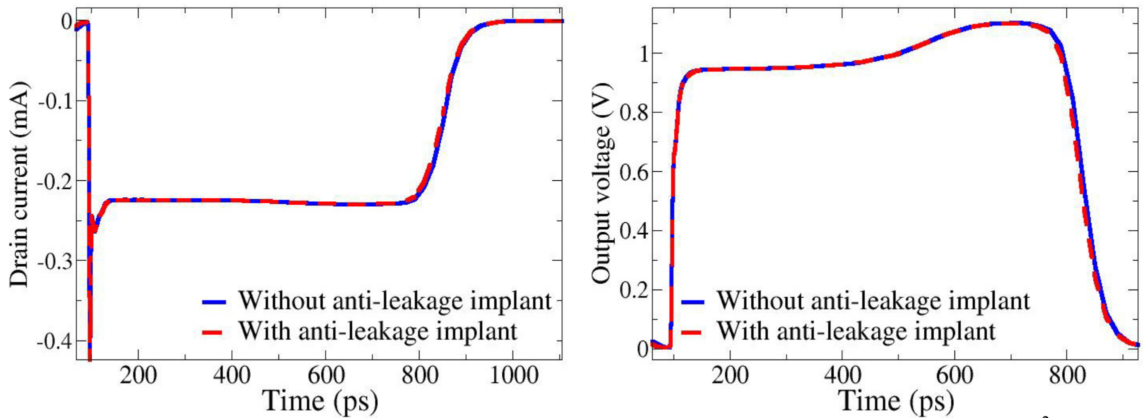

Fig. 83: SE (a) current and (b) voltage transients from normal strike with LET 40 MeV-cm^2/mg, with and without anti-leakage implant

Each of the models is simulated in a mixed-mode current-matched inverter, with the nFET compact model in Spice. Figure 82 shows the current and voltage transients resulting from a normal drain strike with LET of 1 MeV-cm^2/mg. The device response to this low-LET strike showed virtually no change due to the anti-leakage implant. Charge collected by drift and diffusion (low LET) was not affected by this doping profile. The same strike was simulated with LET of 40 MeV-cm^2/mg to investigate how this implant influences the parasitic bipolar amplification. Figure 83 shows the current and voltage transients, which again were virtually independent of the presence of the anti-leakage implant. Since the device model without the anti-leakage implant (Fig. 81) shows good agreement with MOSIS's 9SF Spice model, it has been used throughout this work [19]. These simulations suggest that inclusion of the anti-leakage implant would not change any of the results obtained.

REFERENCES

[1] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, “Comparison of error rates in combinational and sequential logic,” *IEEE Trans. Nucl. Sci*., vol. 44, no. 6, pp. 2209–2216, Dec. 1997.

[2] N. Seifert, X. Zhu, D. Moyer, R. Mueller, R. Hokinson, N. Leland, M. Shade, and L. Massengill, “Frequency dependence of soft error rates for sub-micron CMOS technologies,” *IEDM Tech. Digest*, pp. 323–326, Dec. 2001.

[3] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, T. Turflinger, P. E. Dodd, and G. Vizkelethy, “Heavy ion-induced digital single-event transients in deep submicron processes,” *IEEE Trans. Nucl. Sci*., vol. 51, no. 6, pp. 3480–3485, Dec. 2004.

[4] D. G. Mavis and P. H. Eaton, “Soft error rate mitigation techniques for modern microcircuits,” *Proc. Int. Reliability Physics Symp*., pp. 216–225, Apr. 2002.

[5] P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, and J. R. Schwank, “Production and propagation of single-event transients in high-speed digital logic ICs,” *IEEE Trans. Nucl. Sci*., vol. 51, no. 6, pp. 3278–3284, Dec. 2004.

[6] V. Ferlet-Cavrois, P. Paillet, M. Gaillardin, D. Lambert, J. Baggio, J. R. Schwank, G. Vizkelethy, M. R. Shaneyfelt, K. Hirose, E. W. Blackmore, O. Faynot, C. Jahan, and L. Tosti, “Statistical analysis of the charge collected in SOI and bulk devices under heavy ion and proton irradiation– implications for digital SETs,” *IEEE Trans. Nucl. Sci*., vol. 53, no. 6, pp. 3242–3252, Dec. 2006.

[7] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, Member, R. A. Reed, O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf, L. W. Massengill, “Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS,” *IEEE Trans. Nucl. Sci.,* vol 54, no. 6, pp. 2407-2412, Dec. 2007.

[8] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Flemming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, “Charge Collection and Charge Sharing in a 130 nm CMOS Technology,” *IEEE Trans. Nucl. Sci.,* vol 53, no. 6, pp. 3253-3258, Dec. 2006.

[9] B. D. Olson, D. R. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. Doyle, and D. McMorrow, “Simultaneous Single Event Charge Sharing and Parasitic Bipolar Conduction in a Highly-Scaled SRAM Design,” *IEEE Trans. Nucl. Sci.,* vol 52, no. 6, pp. 2132-2136, Dec. 2005.

[10] O. A. Amusan, L. W. Massengill, M.P. Baze, B. L. Bhuva, A. F. Witulski, S. DasGupta, A. L. Sternberg, P. R. Flemming, and C. C. Heath, "Directional Sensitivity of Single Event Upsets in 90 nm CMOS Due to Charge Sharing," *IEEE Trans. Nucl. Sci.,* vol 54, no. 6, pp. 2584-2589, Dec. 2007.

[11] J. R. Ahlbin, L.W. Massengill, B. L. Bhuva, B. Narasimham, M. J. Gadlage, and P.H. Eaton, "Single-Event Transient Pulse Quenching in Advanced CMOS Logic Circuits," *IEEE Trans. Nucl. Sci.*, vol 56, no. 6, Dec. 2009.

[12] M. P. Baze, W. G. Bartholet, J. C. Braatz, T. A. Dao, "Single Event Upset Test Structures for Digital CMOS Application Specific Integrated Circuits," *IEEE Trans. Nuc. Sci.*, vol. 40, no. 6, pp 1703-1708, 1993.

[13] M. P. Baze, J. Wert, J. W. Clement, M. G. Hubert, A. F. Witulski, O. A. Amusan, L. W. Massengill, D. McMorrow, "Propagating SET Characterization Technique for Digital CMOS Libraries," *IEEE Trans. Nuc. Sci.*, vol. 53, no. 6, pp. 3472-3478, 2006.

[14] C. Rusu, A. Bougerol, L. Anghel, C. Weulerse, N. Buard, S. Benhammadi, N. Renaud, G. Hubert, F. Wrobel, T. Carriere, R. Gaillard, "Multiple Event Transient Induced by Nuclear Reactions in CMOS Logic Cells" *13th IEEE On-Line Testing Symposium*, pp. 137-145, 2007.

[15] D. C. Ness, C. J. Hescott, D. J. Lilja, "Exploring Subsets of Standard Cell Libraries to Exploit Natural Fault Masking Capabilities for Reliable Logic" *Proceedings of the 17th ACM Great Lakes symposium on VLSI*, pp. 208-211, 2007.

[16] S. DasGupta, "Trends in Single Event Pulse Widths and Pulse Shapes in Deep Submicron CMOS." Master of Science Thesis in Electrical Engineering, Vanderbilt University, Nashville, Dec. 2007.

[17] Synopsys *User Manual Release 10*, Synopsys, Mountain View, CA. USA.

[18] Vanderbilt University, Nashville, TN, "ACCRE Computing Cluster," 2009. [Online]. Available: http://www.accre.vanderbilt.edu

[19] "The MOSIS Service", 2010, [Online], Available: http://www.mosis.com .

[20] J. D. Black, "Pattern Identification of Multiple Cell Upsets in Static Random Access Memories to Relate Experimental Test Results to Single Event Upset Mechanisms." Doctor of Philosophy Dissertation in Electrical Engineering, Vanderbilt University, Nashville, Dec. 2008.

[21] O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, J. R. Ahlbin, "Design Techniques to Reduce SET Pulse Widths in Deep Submicron Combinational Logic," *IEEE Trans. Nucl. Sci.,* vol 54, no. 6, pp. 2060-2064, Dec. 2007.

[22] B. D. Olson, O. A. Amusan, S. DasGupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, D. R. Ball, "Analysis of Parasitic PNP Bipolar Transistor Mitigation Using Well Contacts in 130 nm and 90 nm CMOS Technology," *IEEE Trans. Nucl. Sci.,* vol 54, no. 4, pp 894-897, Aug. 2007.

[23] E. H. Cannon and M. Cabanas-Holmen, "Heavy Ion and High Energy Proton-Induced Single Event Transients in 90 nm Inverter, NAND and NOR Gates," *IEEE Trans. Nucl. Sci.*, vol 56, no. 6, pp 3511-3518, Dec. 2009.

[24] "International Technology Roadmap for Semiconductors," [Online], Available: http://www.itrs.net/Common/2004Update/2004Update.htm

[25] "Nvidia GeForceFX 5700 Ultra Graphics Processor Structural Analysis," SAR-0408-002, CHIPWORKS, 2005.

[26] P.E. Dodd, F. W. Sexton, P.S. Winokur, "Three-Dimensional Simulation of Charge Collection and Multiple-Bit Upset in Si Devices," *IEEE Trans. Nuc. Sci.*, vol. 41, no. 6, pp.2005-2017, Dec. 1994.

[27] M. Isberg, P. Jonsson, N. Keskitalo, F. Masszi, H. Bleicher, "Physical models in device simulation of Si power pin-diodes for optimal fitting of simulation results to measured data," *COMPEL-The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol.16, no. 3, pp 144-156, 1997.

[28] D. J. Cummings, A. F. Witulski, H. Park, R. D. Schrimpf, S. E. Thompson, and M. E. Law, "Mobility Modeling Considerations for Radiation Effects Simulations in Silicon," *submitted to IEEE Trans. Nuc. Sci.,2010*.

[29] A. F. Witulski, "Carrier-Carrier Scattering and Mobility Modeling in TCAD," ISDE/Vanderbilt Internal White Paper, March 2009.

[30] J. Schmitz, Y. V. Ponomarev, A. H. Montree, P. H. Woerlee, "Study of pocket implant parameters for 0.18 μm CMOS," *Proceeding of the 27th European Solid-State Device Research Conference*, pp 224-227, 1997.