# SINGLE-EVENT EFFECTS IN DIGITAL CMOS CIRCUITS OPERATING AT ULTRA-LOW POWER

By

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*Around here, however, we don't look backwards for very long. We keep moving forward, opening up new doors and doing new things, because we're curious… And curiosity keeps leading us down new paths.*

– Walt Disney

So many people have helped to get me to this point, and I would like to take this opportunity to thank them and let them know how much I appreciate everything they have done for me. First and foremost, I want to thank my family for their unending support and encouragement. If not for them, this would not have been possible.

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# CHAPTER I

## INTRODUCTION

At each new CMOS technology node, there is a decrease in device dimensions, nodal capacitances, and supply voltage, while at the same time, the number of transistors on an IC, the operating frequency, and leakage currents increase. This leads to an overall increase in power consumption for each successive technology node. For space and military applications, available power is severely limited, and various options to decrease the power requirements are being explored.

Subthreshold circuit operation has been used for years as a simple approach to lowering power consumption; specifically, these kinds of circuits have often been used to ensure long battery life in implanted medical devices and wrist watches. However, in order to use these kinds of circuits in space and military applications, the effects of radiation must be addressed. Before this work, no research had been conducted on this topic.

Considerable research has been performed to accurately quantify single-event effects in digital circuits, but, until this point, the work has focused almost entirely on nominal supply voltage operation. When other supply voltages are considered, they are either slightly above or slightly below the nominal supply voltage (within a few hundred milli-volts). Research, specifically on single-event transient pulsewidths and charge collection, has never been conducted in or around the subthreshold region, which will be referred to in this work as operating at ultra-low voltages or at ultra-low power.

Technologies and circuits typically are characterized in single-event environments by the total amount of charge collected or by the single-event transient pulsewidths generated in transistors, but can also be characterized by single-event upsets, single-event functional interrupts, and single-event latch-up. Single-event transient pulsewidths are heavily dependent on the current drives of the transistors connected to the struck transistor. By reducing the supply voltages from the nominal values to operate at ultra-low power, the restoring currents of the transistors that comprise the circuit are orders of magnitude smaller. This leads to a corresponding increase the single-event transient pulsewidths. In contrast, operating at lower supply voltages results in lower frequency operation, where longer single-event transient pulsewidths are required to cause an upset. The effect of supply voltage on collected charge is much less obvious. In this work, all of these single-event metrics are discussed as a function of supply voltage. Additionally, it is no small task to measure signals at ultra-low voltages, or to characterize these circuits for their single-event susceptibility. To do so, for the first time, a new and innovative technique is explored in this work.

Therefore, recognizing the challenges at hand, it is imperative that ULP circuits are examined in radiation environments if they are to be used in space or military applications. In this dissertation, the radiation effects addressed are limited to single-event effects; however, references are provided for the interested reader regarding total ionizing dose and displacement damage.

# CHAPTER II

# SINGLE-EVENT EFFECTS BACKGROUND

The lowering of the power supply voltage of circuits to achieve ultra-low power (ULP) operation affects many aspects of circuit operation. One significant change is the reduction in the current drives of the transistors. Another major change is the substantial decrease of the electric fields in these transistors. These changes also will result in distinctively different radiation response of ULP circuits compared to circuits operating at nominal power supply voltages. Therefore, the unique radiation effects of these circuits are important to evaluate. In this chapter, the effects of radiation on devices and integrated circuits operating at nominal supply voltages are addressed.

In what follows, single-event effects for circuits operated at supply voltages suitable for ultra-low power operation are addressed. Radiation can affect microelectronic circuits through Displacement Damage (DD), Total Ionizing Dose (TID), and Single-Event Effects (SEEs); however, only single-event effects are discussed in this dissertation. For information on displacement damage, please refer to references [Sro88a], [Sro88b], [Sum92], [Bra94], [Mar99], [Sro03], [Len69]. Consult references [Emi96], [Ale96], [Ler99], [Sch02], [Hsu84], [Old03b], [Old03a], [Ale03], and [Bar05] for information on the effects of total ionizing dose.

## The First Transistors and Moore's Law

The concept leading to the development of the first field-effect transistor was formed in 1933 by Julius Lilienfeld [Lil33]. However, it was not until 1947 that John Bardeen,

Walter Brattain, and William Shockley [Bar48], [Sho51] successfully produced a bipolar junction transistor (BJT) with a feature size of 100 um. Their transistor can be seen in Figure 1. The next major development in the history of electronic circuits came in 1964, when Jack Kilby of Texas Instruments was issued two patents; one for what he described as a "miniaturized electronic circuit" [Kil64a] and one for the Integrated Circuit (IC) [Kil64b]. It should be mentioned though, that in 1959, Robert Noyce of Fairchild Semiconductor implemented four transistors on a single wafer of silicon (at this time germanium was the semiconductor used), which was the first silicon IC. Kilby was awarded the patent because his germanium IC was first implemented in 1958. The next major innovation came only three years later when, in 1967, Frank Wanlass of Fairchild

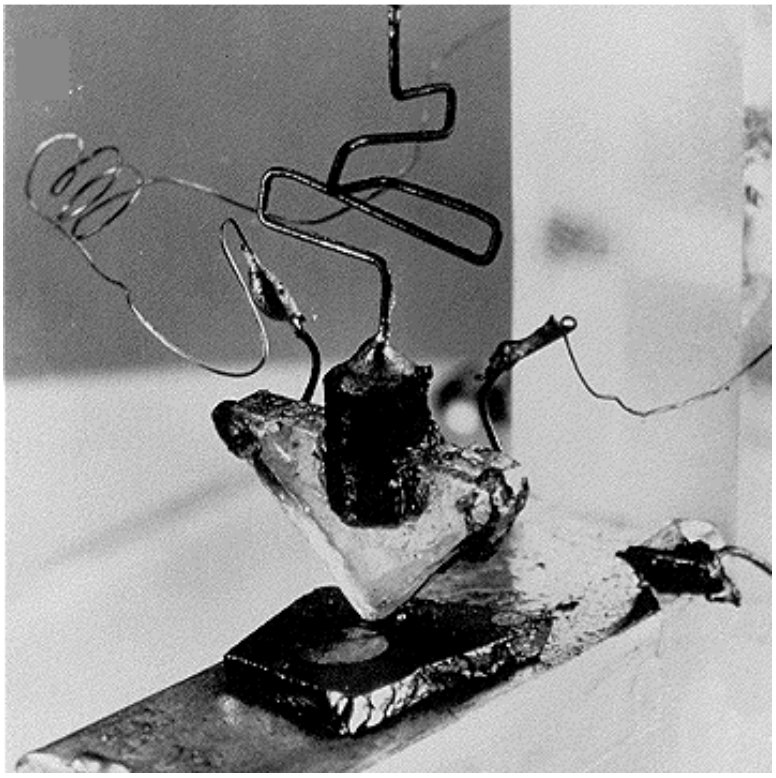


Figure 1. The first working transistor created in 1947 by Bardeen, Brittain, and Schockley..

Semiconductor received a patent for inventing Complementary Metal-Oxide-Semiconductor (CMOS) logic [Wan67].

After the use of transistors became standard, Gordon Moore proposed in 1965 [Moo65], [Moo75] that the number of transistors on a chip would double every two years for the next ten years, and this has come to be known as Moore's Law. To continue his forecast well beyond the ten years predicted, a number of process parameters had to be modified, in addition to the obvious device dimensions and device spacing. These parameters include the operating voltage, gate length, oxide thickness, and nodal capacitance, among others. These changes in process parameters lead to smaller ICs, higher packing densities, lower fabrication costs, and increases in speed and performance. In general, CMOS scaling has been a positive trend, as evidenced by the increased performance and reduced cost; however, scaling has worsened the effects of radiation [Old03a], [Tho05]. In particular, the decreased nodal capacitance and lower operating voltage have increased the likelihood of single-event upsets. The types of radiation responses and their mechanisms and origins will be discussed in the remaining portions of this chapter.

## The Space and Terrestrial Radiation Environment

In the space radiation environment, there exists radiation that includes protons, heavy ions, galactic cosmic ray (GCR) particles, and particles from solar events [Bar03], which include coronal mass ejections and solar flares. In the transient radiation environment, the GCRs follow the 11-year solar cycle and are at their peak during solar minimum. There are also belts of electrons, protons and heavy ions, which were discovered by Van Allen

and can be seen in the drawing in Figure 2. While not depicted in Figure 2, there also exists a bulge at the bottom of the inner belt where there is a change in the field around the Earth. This change is due to the tilt of the Earth's magnetic pole (with respect to the geographic pole) and the displacement of the magnetic field, and is called the South Atlantic Anomaly (SAA) [Bar03].

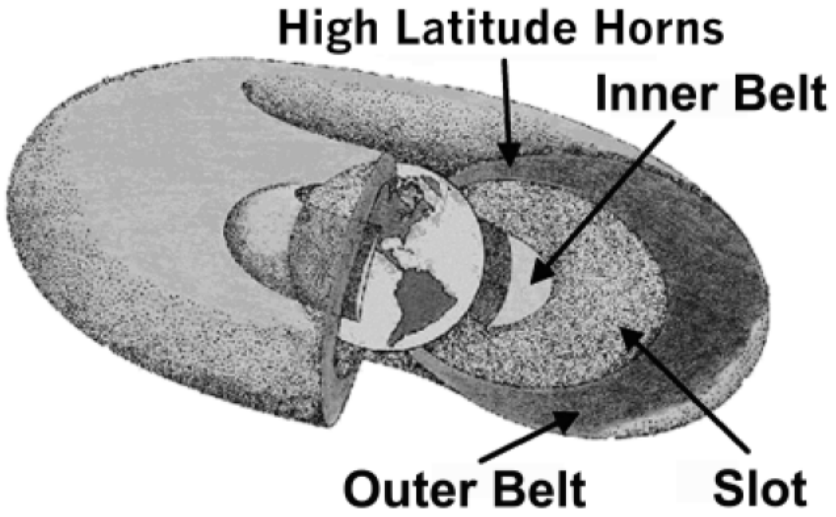



Figure 2. Drawing of the Earth's Van Allen belts [Bar03].

The Earth-bound radiation environment, which includes the Van Allen belts, consists of both natural and man-made radiation, with the natural radiation dominated by particles produced from terrestrial and galactic cosmic rays (GCRs) and solar events [Bar03]. The Earth's magnetic field then traps these particles, which include electrons, protons, and some heavy ions, and gyrate around the magnetic field as seen in Figure 3 [Sta88]. Single-event upsets at sea-level were first seen in 16 Kb DRAMs [May79], and were due to alpha particles being emitted from the ceramic packaging. This lead to speculation that GCRs also could cause upsets at ground level.

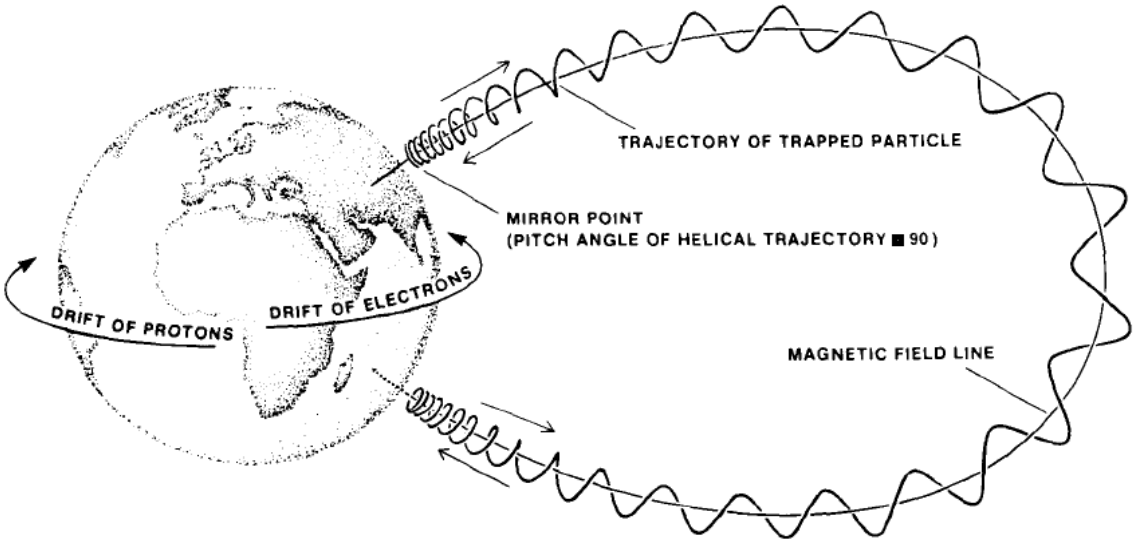



Figure 3. The Earth's magnetic field and the motion of particles around it. [Sta88]

## Introduction to Radiation Effects

There are two principal types of particles found in the space and terrestrial radiation environment, photons, neutrons, and charged particles [Sro88]. Charged particles include alpha particles, electrons, protons, and heavy ions (these are any ions with mass greater than hydrogen.) The type of interaction that occurs is determined by several properties of both the incoming particle (including mass, charge, and kinetic energy) and the target material (including mass, charge and density) [Eva55].

The types of reactions that can occur with photons, which have no mass and are not charged, include the photoelectric effect, Compton scattering, and electron-positron pair production [Sro88a]. The photoelectric effect is a phenomenon in which photons transfer energy to electrons in a material, and the movement of these electrons creates a current. Compton scattering occurs when the wavelength of a photon increases and the energy

decreases after interacting with matter. The photoelectric effect is the lowest energy interaction, and pair production occurs at the highest energies.

Protons interact with silicon in elastic and nonelastic processes. Elastic processes include Rutherford scattering, which is also known as Coulomb scattering due to static electric forces, and nuclear elastic scattering. Both types can result in displacement of atoms in silicon, but in nuclear elastic scattering, a larger amount of energy is transferred from the proton, and the resultant recoil atom subsequently deposits this transferred energy by ionization and displacement [Sro88a]. Nonelastic processes consist primarily of nuclear scattering and alpha particle production.

Charged particles, however, predominantly react by Rutherford scattering, but also can experience nuclear reactions[Sro88a]. The upset mechanism identified with heavy ions is direct ionization, while neutrons and protons experience ionization from a secondary reaction.

## Single-Event Effects

Single-event effects is a broad term used to classify the result of charge deposition from a single ionizing particle [Sch08]. Single-event effects can result in either transient or permanent damage. SEEs include single-event transients (SETs), single-event upsets (SEUs), single-event functional interrupts (SEFIs), and single-event latchup (SEL). As a general rule, with increasing clock frequency and decreasing device gate lengths, the effects of single-events worsen.

*Temporary Single-Event Effects*

A temporary SEE occurs when a Single-Event Transient (SET) is created due to the collection of charge at a p-n junction after a track of electron-hole pairs is generated. SETs are subcategorized into Analog (ASETs) and Digital Single-Event Transients (DSETs), based on the type of circuit in which the transient is generated. For digital circuits, when an SET is latched in a memory cell, it is then called a Single-Event Upset (SEU).

In older circuits comprised of transistors with features sizes greater than 1 micrometer, the processes that governed charge collection after a single-event strike and the resulting current transients were easily defined because the ion track was smaller than the struck transistors [Ree08]. At these technology nodes, after a track of electron-hole pairs is created by an ion incident on an IC, there are three processes that result in charge collection at circuit nodes. These processes are drift, diffusion, and funneling processes. The effects of diffusion and funneling processes are shown in Figure 4 [McL82].

The process of drift occurs almost immediately after the particle strikes due to the presence of a high electric field within the depletion region of an MOS transistor. Charge that is deposited in the substrate has little effect on charge collection, and a significant fraction recombines. The remaining is collected at a p-n junction due to diffusion. Electrons and holes that are deposited near a p-n junction are separated due to the electric field present in the depletion region, with the holes moving to p-regions (low voltage region) and electrons moving to n-regions (high voltage region, comparatively). This movement of charge is called photocurrent and is limited by the saturation velocity of the carriers.

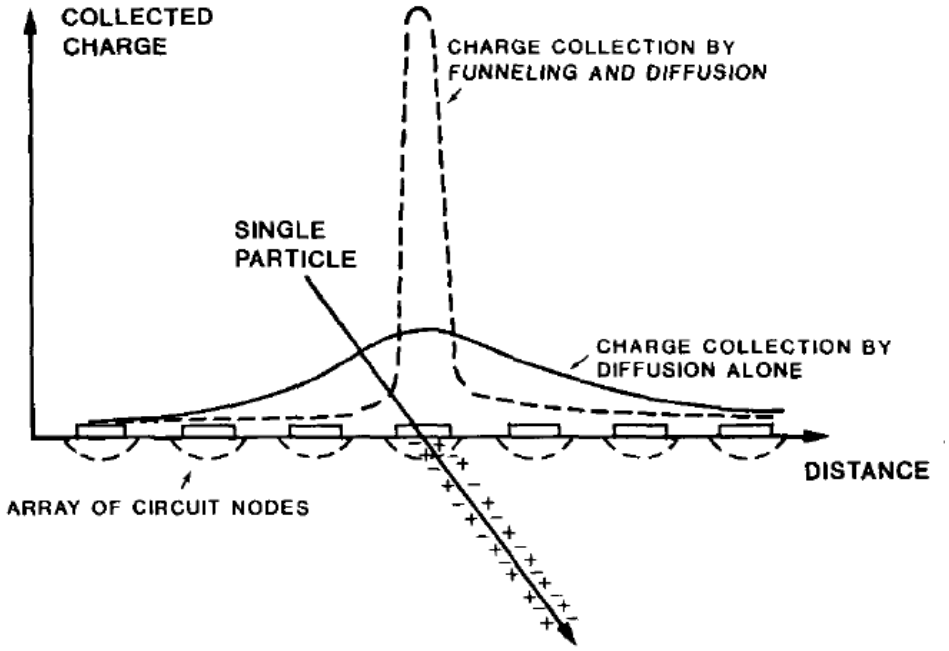



Figure 4. The amount of charge collected greatly increases over a small area when funneling is considered compared to collection by diffusion alone. [McL82]

Outside of the depletion region, charge is collected by diffusion. Diffusion results from charge movement due to gradients in the carrier concentration, but is limited by the diffusion length [Kir79]. Charge collection due to diffusion occurs after the drift process, because diffusion is a slower process.

In funneling [Hsi81], [Hsi83], [McL82], a trail of electrons and holes, called the charge track or funnel (indicated by the plus and minus signs surrounding the arrow in Figure 4), is created by the incident particle. The funnel changes the electric field lines in the transistor, allowing charge outside the original depletion region to be collected via drift when it otherwise would not have been. This results in an increase in total collected charge due to the drift process.

However, when feature sizes are comparable with the ion track size, the charge collection is less easy to describe [Ree08]. While ordinarily technology scaling is viewed

positively, for single-event effects, scaling exacerbates an already serious problem. With scaling, the nodal capacitances and transistor currents decrease and operating frequency increases. These factors reduce the amount of charge required to generate an SET/SEU in the circuit, resulting in increased vulnerability. Also, by increasing the packing density and decreasing the device spacing, the probability of charge collection on multiple nodes increases. The effect of multiple node charge collection can result in severely underestimated error cross-sections and threshold LETs [Mar87], [Dod94], [Ols05], [Bla08], [Cas08]. This can be due to charge diffusion between devices in proximity [Amu06a], [Amu06b], [Amu09], or nuclear reactions when an alpha particle or heavy ion strikes the nucleus of an atom [Tip06]. Decreased minimum dimensions on an IC also results in increased charge collection after a single-event hit due to parasitic bipolar amplification [Sun78], [Fu85], [Woo93], [Dod96], [Ols05], [Ibe06], [Amu06a].

Parasitic bipolar amplification was first observed in silicon-on-insulator (SOI) transistors, but also can occur in bulk transistors. Additionally, parasitic bipolar amplification has been shown to drastically increase the amount of charge collected by PMOS transistors. This effect occurs when a charge particle strikes a PMOS transistor and a potential gradient is formed between the source and drain [Ker89]. If this gradient is sufficiently large, minority carriers can be injected from the source to the drain due to the turn-on of the parasitic bipolar transistor, and the single-event current that is generated is amplified by the gain of the parasitic bipolar transistor.

*Permanent Damage Due to Single-Event Effects*

A single heavy ion also can cause permanent damage in a device by creating a highly conductive path to the substrate, effectively shorting a node to the substrate [Bla81],

[Pic85]. This conductive current path is created by ionization and quickly heats the device, eventually leading to thermal runaway. Other permanent effects include single-event burnout (SEB) [Was86] (occurs in power MOSFETs), and latch-up [Kog84], [Ste84] (occurs in bulk CMOS transistors). Latch-up can be prevented by fabricating devices on a process with either an epitaxial layer or on a silicon-on-insulator (SOI) process [Kog84], [Ste84].

## Conclusions

Armed with a solid understanding of the effects of a single charged particle on devices and integrated circuits operating at the nominal supply voltages, the effects of these same particles on ultra-low power circuits can now be investigated. The same mechanisms will exist, but the relative importance of diffusion versus drift charge collection is not obvious with the reduced electric fields and drive currents associated with operation at ultra-low voltages. Additionally, the effect of parasitic bipolar amplification, which plays a large role in the charge collected at nominal supply voltages, will not exist due to the low voltage differential that exists between the source and drain. The balance between these mechanisms necessitates the investigation of single-event effects for ultra-low power circuits, if they are to be used in space and military applications.

# CHAPTER III

## SUBTHRESHOLD CIRCUIT OPERATION

According to the 2007 International Technology Roadmap for Semiconductors (ITRS), power consumption is one of the top three concerns for the next five years, and is a key restriction in chip design [ITRS]. Specifically, a major focus is power consumption due to leakage. The expected trend in chip power consumption for portable consumer devices is shown in Figure 5. Likewise, Figure 6 shows the projected total power trend for consumer chips that will be used in stationary, non-portable electronics. These parts do not have the same battery constraints as portable devices, but other issues, such as cooling, begin to arise as power consumption continues to increase dramatically. Both

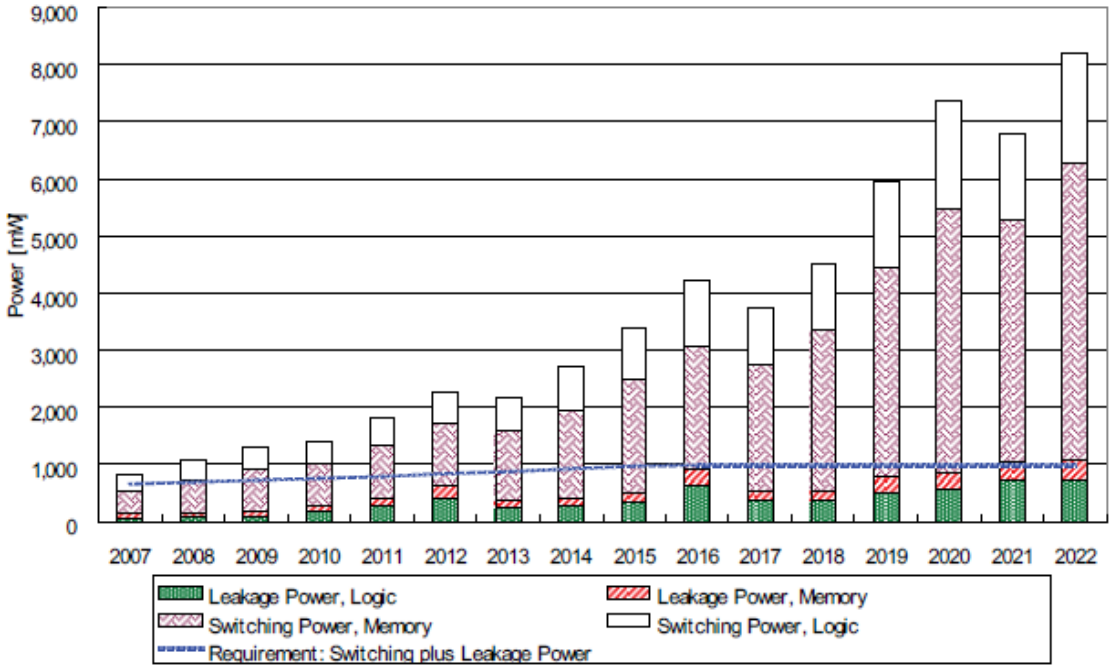



Figure 5. The expected trend in power consumption for logic and memory circuits in portable consumer devices, as reported by the 2007 ITRS [ITRS].

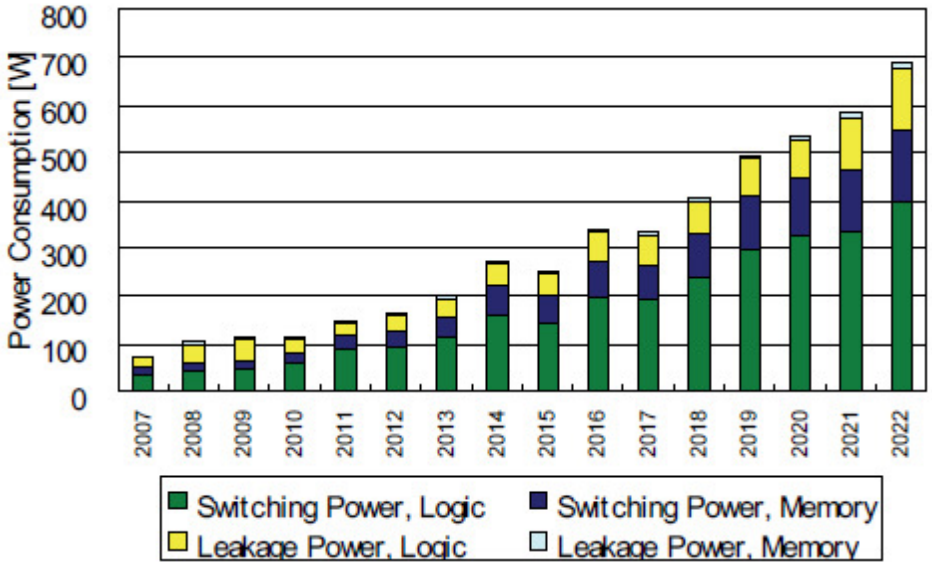



Figure 6. The expected trend in power consumption for logic and memory circuits in stationary consumer devices, as reported by the 2007 ITRS [ITRS].

types of circuits require steps to be taken to reduce power consumption and its effects. The changes necessary to reduce power consumption can be in the process parameters or at the circuit level.

Process changes to modify the threshold voltage will reduce the current drive and therefore, the power consumption. The relationship between power dissipation and transistor drive current can be seen in the following equations in this chapter. The standard equation for power is given as function of nodal capacitance, supply voltage, and the frequency of operation, and can be seen in Equation (1).

$$P = C \cdot V^2 \cdot f \qquad (1)$$

By changing the power supply voltage, the power increases or decreases with the square of the change. The other factors, capacitance and frequency will be examined individually in detail to understand the relationship between these factors and the supply

voltage. Additionally, in this chapter, the effect of power supply voltage on transistor drive current is also examined.

## Capacitance

The nodal capacitance ($C_{out}$) for an inverter (used throughout this chapter due to its simplicity and because inverters form the basis of the ring oscillator that will be used for most of this dissertation) can be estimated by summing the NMOS and PMOS gate-to-drain capacitance ($C_{GDn}$ and $C_{GDp}$), NMOS and PMOS drain-to-body capacitance ($C_{DBn}$ and $C_{DBp}$), interconnect capacitance ($C_{int}$), and fan-out capacitance ($C_{FO}$) [Uye99]. The approximation for the combined nodal capacitance is given by [Uye99]:

$$C_{out} = \left(C_{GD_n} + C_{GD_p}\right) + \left(C_{DB_n} + C_{DB_p}\right) + C_{\text{int}} + C_{FO} \tag{2}$$

The gate-to-drain capacitances for transistors are [Uye99]:

$$C_{GD_{n,p}} \approx \frac{1}{2}\left(\frac{\varepsilon_{ox}}{x_{ox}}\right) W_{n,p} L'_{n,p} \tag{3}$$

where $\varepsilon_{ox}$ is the oxide permittivity and is approximated by $(3.9)\varepsilon_0$. The permittivity of free space, $\varepsilon_0$, has a value of $8.854\times10^{-14}$ F/cm. Additionally, $w_{n,p}$ is the transistor width and $L_{n,p}'$ is the transistor length.

The drain-to-body capacitance changes as the transistor changes state, so the equations for these capacitances use linear, time-independent average values. The equation for drain-to-body capacitance is given by [Uye99]:

$$C_{DB_{n,p}} = \left( \frac{2\phi_0}{V_{DD}} \left[ \left( 1 + \frac{V_{DD}}{\phi_0} \right)^{1/2} - 1 \right] \right) \frac{\varepsilon_{Si}}{\sqrt{\frac{2\varepsilon_{Si}\phi_0}{q}\left( \frac{1}{N_a} + \frac{1}{N_d} \right)}} A_{D_{n,p}} + \left( \frac{3\phi_0}{2V_{DD}} \left[ \left( 1 + \frac{V_{DD}}{\phi_{0sw}} \right)^{2/3} - 1 \right] \right) C_{jsw_{n,p}} P_{D_{n,p}} \quad (4)$$

In this equation, $\phi_0$ is the built-in voltage that is determined by the process parameters; $\varepsilon_{Si}$ is the permittivity of Silicon and is approximately $11.7\,\varepsilon_0$; $N_a$ and $N_d$ are the acceptor and donor carrier concentrations for the process; $C_{jswn,p}$ is the sidewall capacitance per unit area; and $A_{Dn,p}$ and $P_{Dn,p}$ are, respectively, the area and perimeter of the NMOS and PMOS transistor drains. The equation for the interconnect capacitance is defined as [Uye99]:

$$C_{\text{int}} = \frac{\varepsilon_{ox}}{x_{\text{int}}} Dw \quad (5)$$

Where $x_{int}$ is the oxide thickness between the metal interconnect line and the substrate, and D and w are the length and width of the metal line. Finally, the fan-out capacitance is described by the equation [Uye99]:

$$C_{FO} = FO \cdot \left( \frac{\varepsilon_{ox}}{x_{ox}} W_n L_n' + \frac{\varepsilon_{ox}}{x_{ox}} W_p L_p' \right) \quad (6)$$

where FO is the number of inverters loading the node.

Therefore, as can be seen from these equations for nodal capacitance, there is no voltage dependence on capacitance (except slightly for $C_{DBn,p}$ and that effect is negated due to the average), so the effect of lowering the supply voltage to operate at ultra-low power will have no effect on the capacitance in these first order approximations.

## Frequency

While power consumption is directly proportional to the operating frequency, the equation for maximum operating frequency is highly dependent on power supply voltage. The equation for maximum frequency is given by the equation [Uye99]:

$$f_{\max} = \frac{1}{s_n \tau_n + s_p \tau_p} \tag{7}$$

In this equation, $\tau_n$ and $\tau_p$ correspond to the time constants for discharging and charging the output capacitance, and $s_n$ and $s_p$ are voltage-dependent scaling multipliers. The time constants are described by the equation for n- and p-channel transistors, respectively [Uye99]:

$$\tau_{n,p} = \frac{C_{out}}{k'_{n,p}\left(\frac{W}{L}\right)_{n,p}\left(V_{DD} - \left|V_{T_{n,p}}\right|\right)} \tag{8}$$

The scaling factors, $s_n$ and $s_p$, are expressed by the equation [Uye99]:

$$s_{n,p} = \left[\frac{2V_{T_{n,p}}}{\left(V_{DD} - V_{T_{n,p}}\right)} + \ln\left(\frac{4\left(V_{DD} - V_{T_{n,p}}\right)}{V_{DD}} - 1\right)\right] \tag{9}$$

Both of the time constants and the scaling factors show a strong relationship to the supply voltage.

## Transistor Drive Currents

Another equation for power is given by:

$$P = VI \tag{10}$$

which shows that power is also directly proportional to the transistor drive current. However, the effect of lowering the supply voltage complicates drastically the

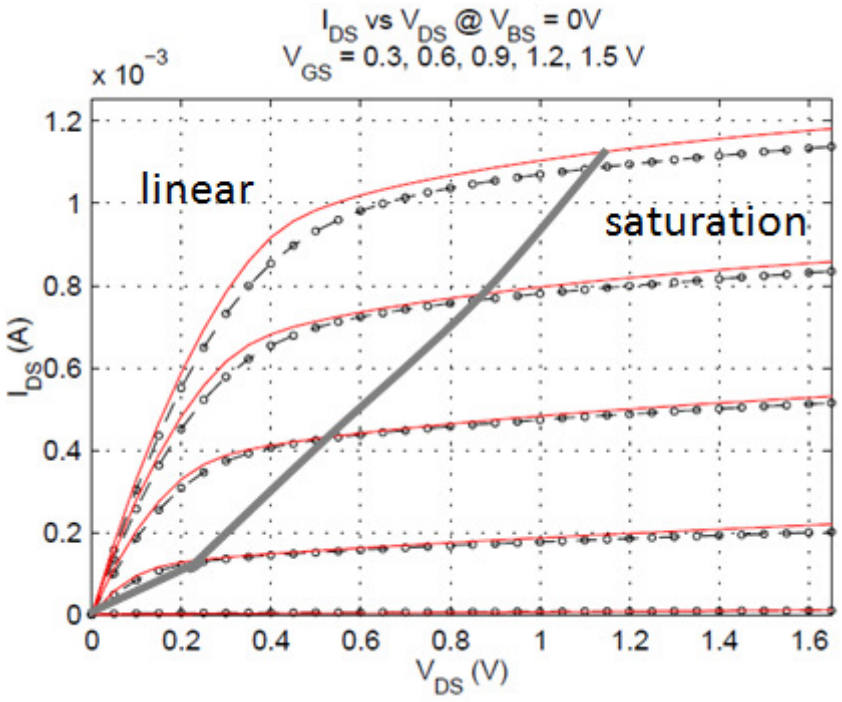
relationship between power consumption and transistor drive currents. This is due largely to the fact that the transistor drive current equations are dependent on the region of operation of the transistors, which in turn are dependent on power supply voltage.

Ordinarily, when circuits are operated at their nominal supply voltages, the transistors are operating in the saturation region, and the drive currents of the devices in the circuits are strong inversion currents that are dominated by drift [Han06]. However, when the power supply voltages decrease and are near the threshold voltages, the drive currents become weak inversion currents that are dominated by diffusion, and the devices operate in the linear and subthreshold region. Figures 7 and 8 show (a) the $I_D$-$V_D$ curves and (b) the $I_D$-$V_G$ curves for a minimum-sized NMOS and PMOS transistor, respectively, fabricated in the IBM CMRF8SF 130 nm bulk CMOS process. Also indicated on the figures are the regions of operation with the saturation and linear regions shown in the $I_D$-$V_D$ curves, and the subthreshold region illustrated by the grey shaded region in the $I_D$-$V_G$ curves. Additionally for the remaining discussion, the equations given will be only for NMOS transistors to simplify the discussion.

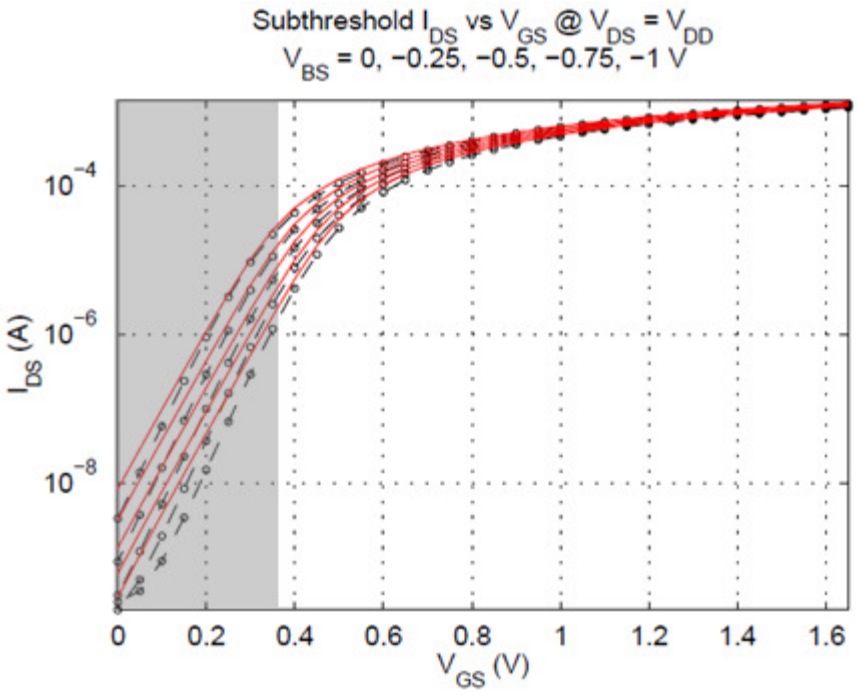
In the saturation region, the equation for drain current in the NMOS transistor is [Uye99]:

$$i_D = \beta \frac{(V_{GS} - V_T)^2}{2} \qquad 0 < V_{GS} - V_T \le V_{DS} \tag{11}$$

When the supply voltage is reduced to a value less than the threshold voltage and the transistors are said to be operating in the subthreshold region, the equation (to first-order) for drain current becomes [Uye99]:

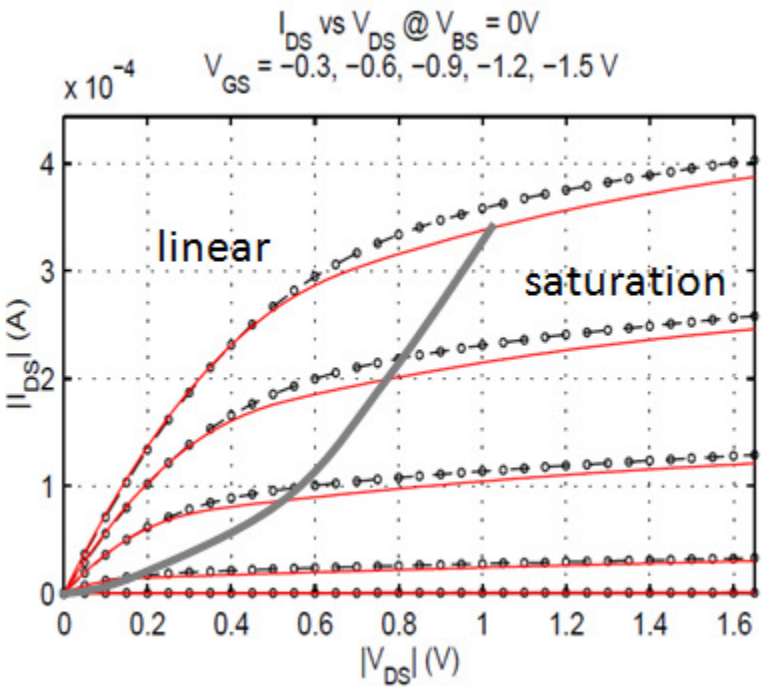



(a)

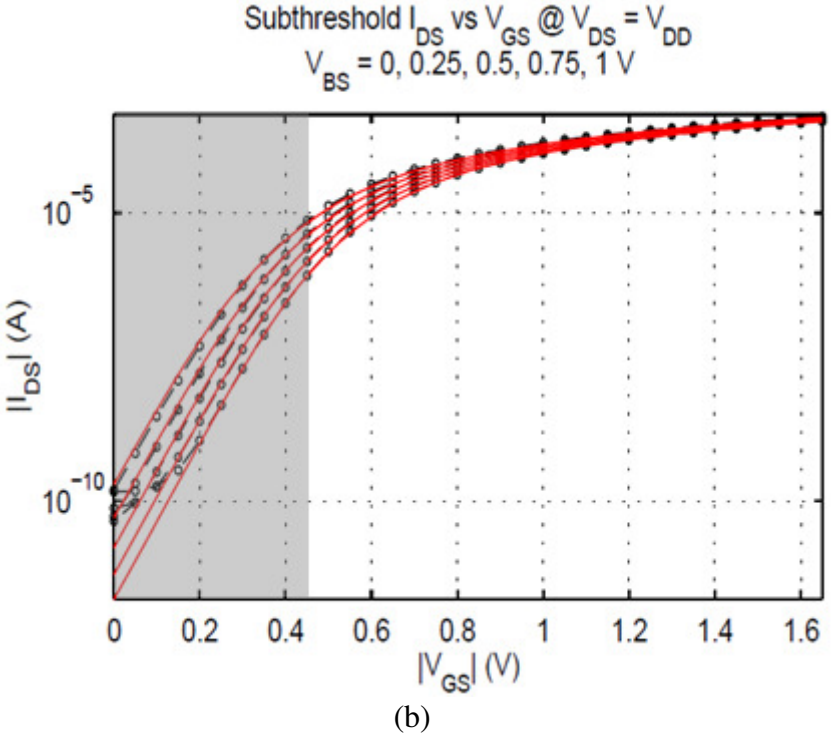



(b)

Figure 7. The (a) $I_D$-$V_D$ curves with the linear and saturation regions of operations indicated and (b) $I_D$-$V_G$ curves with the subthreshold region indicated for an NMOS transistor fabricated in the IBM CMRF8SF 130 nm bulk CMOS process [8SF].




(a)




(b)

Figure 8. The (a) $I_D$-$V_D$ curves with the linear and saturation regions of operations indicated and (b) $I_D$-$V_G$ curves with the subthreshold region indicated for an NMOS transistor fabricated in the IBM CMRF8SF 130 nm bulk CMOS process [8SF].

$$i_D \cong \frac{W}{L} I_{D_0} e^{\frac{V_{GS}}{n\left(\frac{kT}{q}\right)}}, \qquad V_{GS} < V_T + n\frac{kT}{q} \tag{12}$$

In this region, the power consumption is orders of magnitude lower because of the exponential dependence on gate-to-source voltage, as opposed to the square relationship in the saturation region. Between these two regions is the linear region, where the transistors are described as being in moderate inversion and the equation for drain current is given as [Uye99]:

$$i_D = \beta\left[\left(v_{GS} - V_T\right) - \frac{v_{DS}}{2}\right]v_{DS}, \quad V_T < v_{DS} \le \left(v_{GS} - V_T\right) \tag{13}$$

## Methods for Reducing Power Consumption

There are several approaches for reducing power consumption. Switching from standard MOSFET transistors to double-gate MOSFETS [Kim05] or FinFETs [Taw08] allows for reduced power consumption due to the decreased drive currents, but these devices are less well-known and implementation may require complete reworking of pre-existing circuit designs. Another approach is to shift from standard cell libraries to those designed specifically to reduce power consumption. Again in this case, considerable time, effort, and money must be invested for complete library redesigns. Modifying process parameters to lower the threshold voltage is another option. This in turn will lower the transistor drive currents, and therefore, the power consumption, but the small change in current that can be achieved does not merit the high cost of modifying process parameters. Additionally, by reducing the current drives, the operating frequency of the circuits that employ these transistors is also reduced.

By simply lowering the power supply voltage of standard circuit designs to voltages below the threshold voltage, the power dissipation can be reduced by orders of magnitude. At these low voltages, the circuits are still able to achieve a full-rail voltage swing, so all standard cell libraries can be used. However, as the supply voltages, and correspondingly the drive currents, are lowered, the maximum operating frequency also decreases. This results in low operating frequencies for subthreshold region operation [Cal04a]; the total power requirements, however, are on the order of nano-watts [Wan05].

The power savings and low operating frequencies are mainly due to the low device currents at these supply voltages, as described in the equations given above. Figure 9 shows the current draw for a string of 20 logic gates as a function of power supply

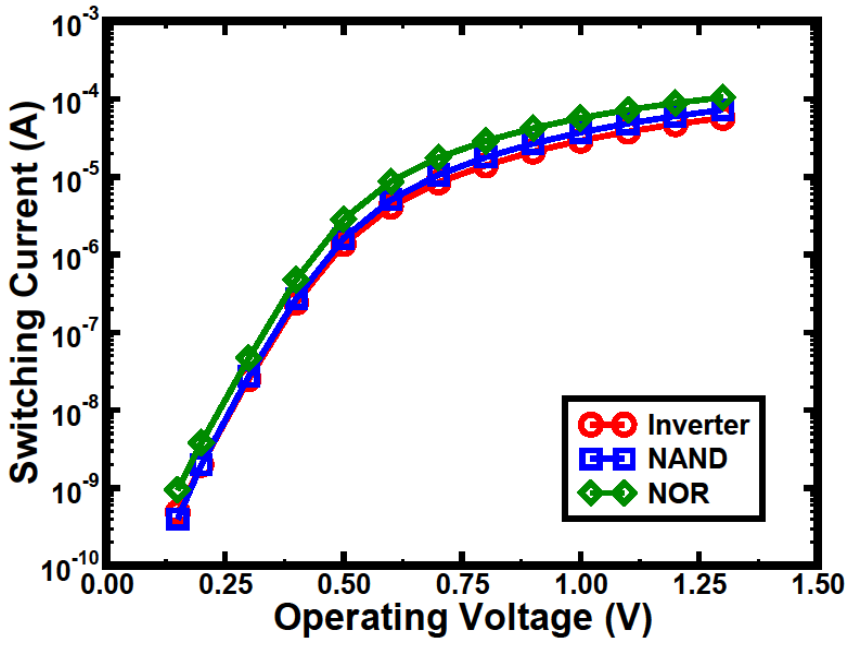



Figure 9. The current draw for different combinational logic gates over a wide range of power supply voltages as simulated using Cadence Spectre and the IBM 130 nm CMRF8SF bulk CMOS PDK.

voltage. The data plotted in these curves were calculated by simulating the strings of 20 logic gates in Cadence Spectre using the IBM CMRF8SF 130 nm process design kit (PDK) [8SF]. All input combinations were simulated and the largest current magnitude was recorded for a range of operating voltages between the subthreshold region and the nominal supply voltage of 1.2 V. The low transistor drive currents, and likewise, the low power consumption, shown in Figure 8 allow circuits with supply voltages below the nominal values to operate in remote environments, where it is not feasible to change batteries frequently. These advantages have led to the consideration of operating standard CMOS circuits at ultra-low power supply voltages in space and military environments.

Unfortunately, in the subthreshold region the drive currents are dominated by weak inversion currents, which require a trade-off in power consumption for performance. As the current decreases, the rise and fall times (and therefore, the propagation delay) of a logic gate increase, resulting in lower maximum operating frequencies. The propagation delay of a single inverter as a function of power supply voltage was simulated for the IBM CMRF8SF 130 nm bulk CMOS process using Cadence Spectre, and the resulting data are shown in Figure 10. Likewise, Figure 11 shows the maximum operating frequency as a function of power supply voltage for the same set of simulation conditions. The drive currents, though small, will be able to fully charge and discharge the nodal capacitances. Because the nodes can be driven to both rails, standard cell libraries can be used in the subthreshold region.

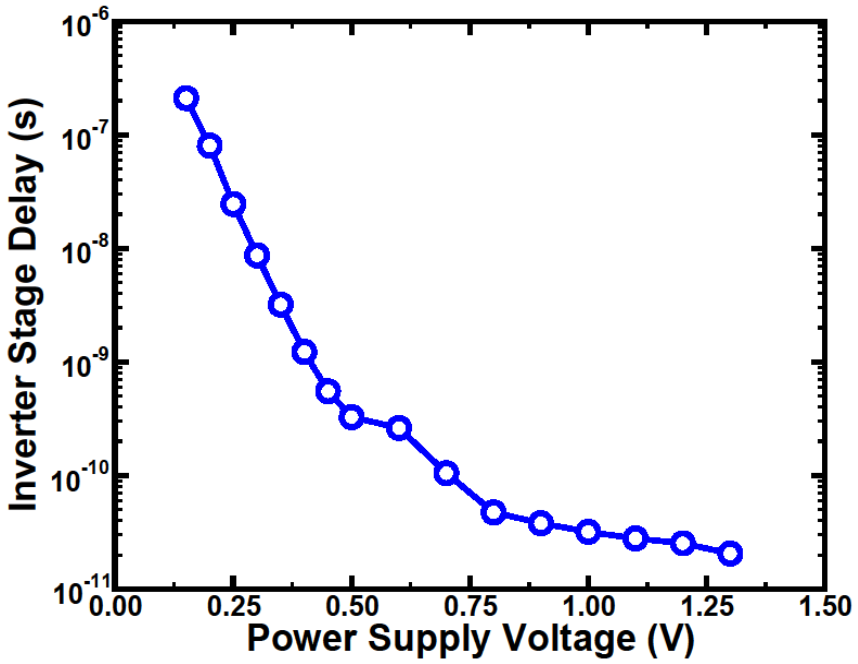



Figure 10. The stage delay for an individual inverter decreases as power supply voltage increases. The data plotted in this figure were found through simulation using Cadence Spectre and the IBM 130 nm CMRF8SF PDK.

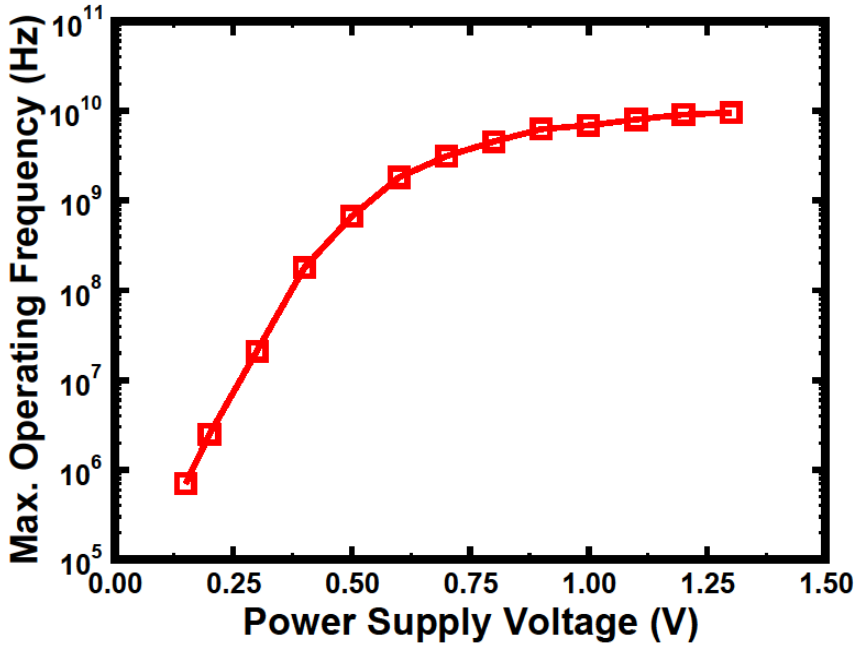



Figure 11. The maximum operating frequency of a circuit increases as the power supply voltage increases. The data plotted in this figure were found through simulation using Cadence Spectre and the IBM 130 nm CMRF8SF PDK.

## Problems Associated with Subthreshold Operation

Process-induced variations in threshold voltage can wreak havoc on circuits operating in the subthreshold region. The problems arise because there is an exponential dependence of threshold voltage on drive strength [Cal05]. Unfortunately, these variations only will worsen as devices continue to scale. The effects of the variations can be mitigated to some extent by using larger gate sizes [Han06], [Zha05], [Kwo06]. By increasing the gate width, designers can offset the effects of the extreme variations. However, the increased gate width also will increase the current and the nodal capacitance. By increasing the transistor gate widths at a given voltage, the capacitance and the operating frequency will increase. These changes will, to some extent, negate the purpose of subthreshold operation, which is reduced power consumption.

## Circuit Architecture for Improving Subthreshold Performance

The slow operating frequency that is a consequence of low supply voltages is unacceptable for many space and military applications. Often, to improve the speed and performance of subthreshold circuits, parallelism or pipelining are instituted [Cal04b]. Parallelism itself will not increase the frequency of a given circuit, but the number of operations completed in a given period of time will increase resulting in an *effective* overall increase in frequency. It should also be noted that parallelism requires additional circuitry, which will contribute to an increase in total power consumed; however, these increases are typically insignificant compared to the power requirements for operation at the standard supply voltage.

The effects of radiation on CMOS transistors operating at the nominal supply voltages have been well-studied, as discussed in Chapter I. However, little work has been done examining these effects in circuits with transistors operating outside of the saturation region. All of the changes in electric field, current drive, and operating frequency associated with ultra-low voltage operation require the examination of ULP circuits in radiation environments.

# CHAPTER IV

## RING OSCILLATORS AS A SINGLE-EVENT TEST STRUCTURE

In order to quantify the single-event effects in MOSFET transistors and CMOS integrated circuits, the amount of collected charge and the resulting single-event transient pulsewidths are often measured. There are several techniques for measuring charge collection including the ion-beam-induced charge collection (IBICC) technique [Bre93], [Hor97]; the time-resolved ion-beam-induced charge collection (TRIBICC) technique [Sch98], [Bre07]; and a charge collection measurement circuit based on sense amplifier, which was proposed by Amusan *et al.* [Amu08]. Each is unsuitable for ULP circuits for different reasons. For all single transistor charge collection measurement techniques, the transistors are nominally in the off-state, making it impossible to characterize the effect of supply voltage variation.

For single-event transient pulsewidth measurements, a temporal latch with variable delays technique [Eat04], a chain of latches [Nic03], and a self-triggering chain of latches [Nar06a] have all been introduced. There have also been pulsewidth measurement circuits proposed by Baze *et al.* [Baz06] and by Ferlet-Cavrois *et al.* [Fer06a], [Fer07], [Fer09]. When attempting to use these circuits for ULP circuit characterization, the temporal latch cannot be used, because would require an impractically long delay element to capture transients at the lowest supply voltages, or additional circuitry to step the voltages up to more manageable value that would require shorter delays. Similarly, the circuits proposed in [Nic03] and [Nar06a] would both require an infeasible number of latches to capture the full transient at the lowest supply voltages or additional “step-up”

circuitry. However, the circuits proposed by Baze and Ferlet-Cavrois can be used for ULP circuit characterization, but these circuits are not standard library elements, so additional design work would be necessary. Therefore, it is necessary to find a simple and common, on-chip method for characterizing single-event effects in ultra-low power circuits. Ring oscillators offer just such a technique and are readily available on all test chips used for process characterization, so no additional circuit design is necessary for single-event characterization. In this chapter, a unique response to single-events in ring oscillators is presented, and this response is used to characterize a given technology for ULP operation.

In ring oscillators (ROs), the natural, fundamental operating frequency is determined by number of stages in the ring oscillator, and by the transistor currents and nodal capacitances. The transistor currents charge and discharge the nodal capacitances, so the magnitude of the current limits how quickly this occurs. Likewise, as the amount of capacitance increase, the longer it will take (for a given current magnitude) for the capacitors to charge and discharge. Typically, an RO contains only a single pulse (described as the natural pulse) whose duration is equal to the cumulative delay of all the RO stages. To this pulse, the RO appears to be an infinite chain of inverters. Therefore, in addition to the natural pulse, any voltage introduced transient, with a sufficiently wide pulsewidth, should propagate through the RO. Additional pulses also can be introduced in a RO through supply voltage perturbation [Sas82], [Hou83].

ROs with large numbers of stages can have a unique (and unexpected) result on voltage perturbations, including voltage pulses that result from charge collection. Therefore, the single-event effects and effects of voltage perturbations in ring oscillators

can be used to monitor the vulnerability of ULP circuits to SE radiation. In this chapter, electrical and laser experiments and SPICE simulations showing the single-event vulnerability of RO circuits are presented.

## Simulation Results

When a transient with a sufficiently wide pulsewidth is inserted at a node in a 201-stage RO designed in the IBM CMRF8SF 130 nm bulk CMOS process, the transient is able to propagate freely and results in the RO operating at a frequency higher than the natural frequency. Because the logic delays are a function of supply voltage and technology, a "sufficiently wide" transient pulse is highly application dependent. Figures 12-14 show the effect of varying amounts of deposited charge on a 300-stage inverter chain, a 200-stage ring oscillator, and a 201-stage ring oscillator. For all simulations shown in Figures 12-14, the current pulses used to model the single-event were double-exponential with a rise time of 15 ps, a fall time of 150 ps, and a duration of 5 ps. The magnitude of each pulse is specified in the proceeding paragraphs with the description of the response.

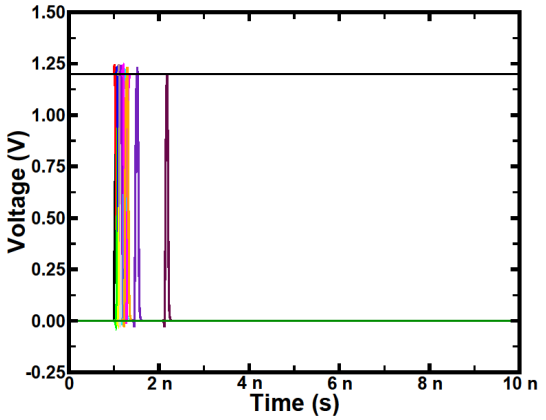
The inverter chain was chosen to identify any feedback effects, which would be seen when the output is compared to the output of one of the ring oscillators. This effect can be discerned because the ring oscillators are simply inverter chains with the input of the first inverter connected to the output of a 2-input NAND gate, and the inputs of the NAND gate are a DC voltage (identical to the input of the inverter chain) and the output of final inverter in the internal chain of the ring oscillator (which creates the feedback path between the output and input). The 200-stage ring oscillator was chosen to best

simulate an infinite inverter chain, because the outputs will be constant, unlike with the 201-stage ring oscillator in which the output of each individual inverter will switch output states from HIGH to LOW over time.

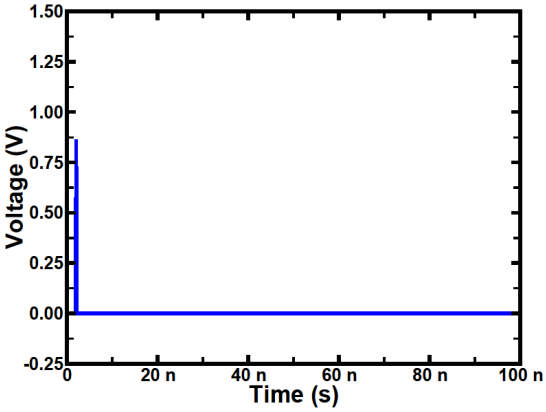
In Figure 12a, a transient generated by a current pulse with magnitude of 164 mA at the output of the first inverter in the string propagates through roughly fifty stages. As a result, the same single-event current pulse results in a transient that is generated at the output of the first inverter in the ring oscillators, shown in both Figures 12b and 12c. However, the transient is not wide enough to propagate through all 200 and 201 stages, respectively, which ultimately results in the ROs acting ideally.

When the single-event current magnitude, and therefore, the amount of deposited charge, is increased to 175 mA, the resulting transient is wide enough to propagate through the inverter chain and the voltage transient appears at the output of the $300^{th}$ inverter. This is shown in Figure 13a. Likewise, when the same current pulse is applied to the 200- and 201-stage ring oscillators, the transient propagates through multiple periods of oscillation in both ROs, as seen in Figures 13b and 13c.

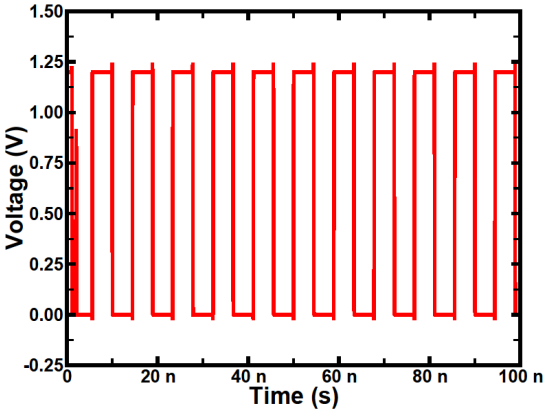
Finally, by increasing the magnitude of the single-event current pulse to 200 mA, the resulting voltage transient again is seen at the output of the $300^{th}$ inverter, as shown in Figure 14a. In this case, however, the voltage transient has a wider pulsewidth than in Figure 13a. As a result, with this current pulse, the voltage transients that are created in the ring oscillators are able to propagate indefinitely. This set of simulations indicates a csingle-event current pulse that results in higher harmonic oscillation in ring oscillators with an odd number of stages.




(a)

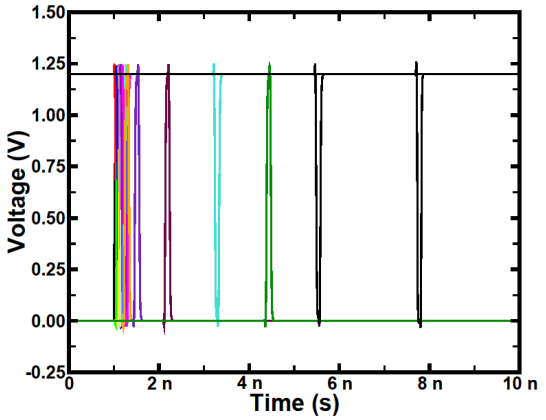



(b)

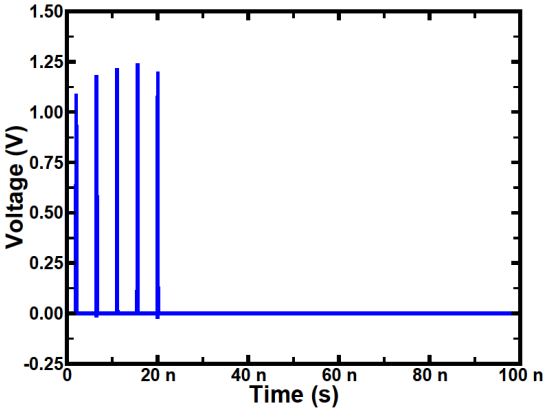



(c)

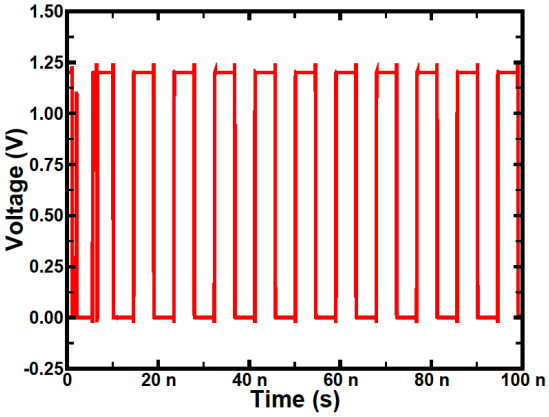
Figure 12. When a single-event strike is modeled by a current pulse with a magnitude of 164 mA, the resulting voltage transient (a) propagates through roughly fifty inverters of a 300-stage inverter string, but does not propagate back to the struck node in (b) a 200- or (c) 201-stage ring oscillator.




(a)

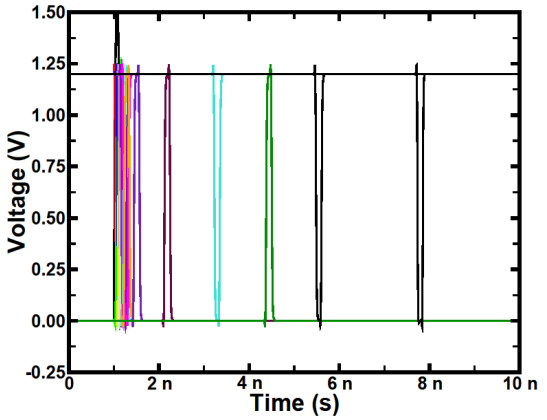



(b)

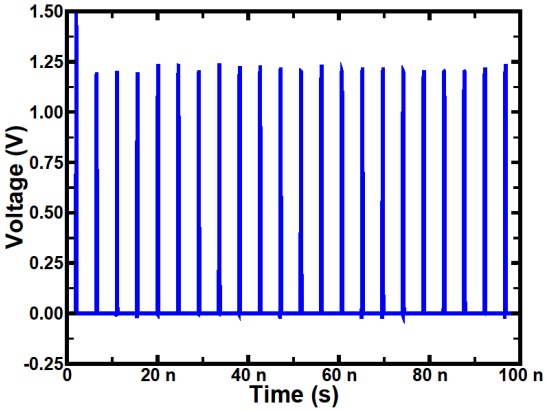



(c)

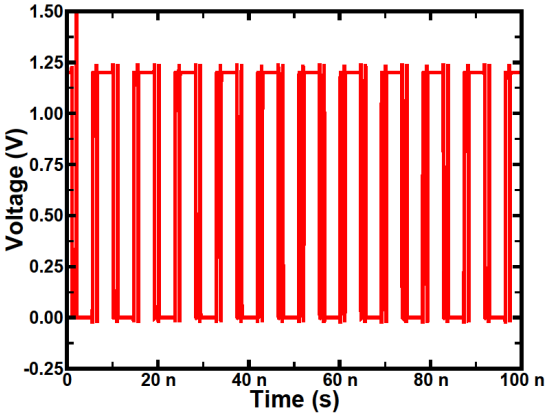
Figure 13. When a single-event strike is modeled by a current pulse with a magnitude of 175 mA, the resulting voltage transient (a) propagates through all 300 inverters of a 300-stage inverter string. However, the resulting transients only propagate back to the struck node (b) four times in a 200-stage ring oscillator and (c) one additional time in a 201-stage ring oscillator.




(a)




(b)




(c)

Figure 14. When a single-event strike is modeled by a current pulse with a magnitude of 200 mA, the resulting voltage transient (a) propagates through all 300 inverters of a 300-stage inverter string. In this case, the resulting transients propagate indefinitely through both (b) a 200- and (c) a 201-stage ring oscillator.

Simulation results conducted using Cadence Spectre with the IBM CMRF8SF 130 nm process design kit (PDK) are shown in Figure 15. Shown is an example of multiple single-event transients propagating in an RO after charge was collected at an internal circuit node. The power supply voltage in this simulation was 350 mV, but similar results were seen with power supply voltages from 200 mV to 1.2 V. The blue curve shows the fundamental operating frequency of RO, and the red curve shows the output of the ring oscillator after 200 fC of charge has been deposited by a double-exponential current source with a rise time of 10 ps and a fall time of 100 ps.

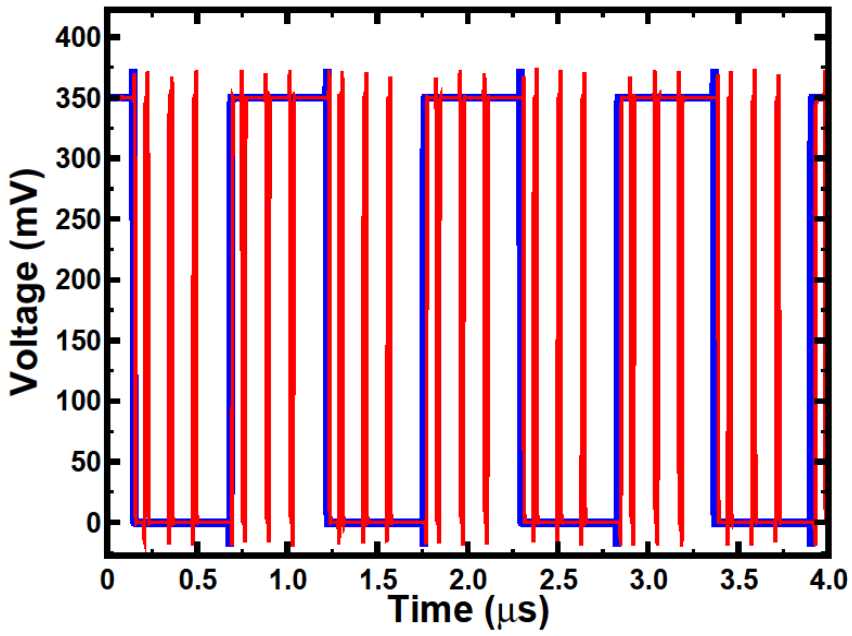



Figure 15. Depositing 200 fC of charge on a single node in a 201-stage RO simulated using the IBM CMRF8SF 130 nm bulk CMOS process forces the RO operate at a frequency six time greater than the fundamental frequency. The pre-strike (fundamental frequency) is shown in blue, while the harmonic oscillation is shown in red.

## Experimental Technique

To prevent interference from metallization layers, a method of backside optical irradiation has been introduced. These irradiations use two-photon absorption (TPA), rather than the single-photon absorption used in topside laser irradiations. This method of laser-induced carrier generation uses high-peak-power femtosecond pulses at sub-bandgap optical wavelengths. Using a 100x microscope objective, the laser is focused to a near-Gaussian beam profile and propagates through the wafer to the top surface of the die. The beam focuses to a diameter of approximately 1.6 µm, but because carrier deposition varies as the square of the irradiance [McM02], [McM04], [McM05], [Van85], [Bog86], the diameter of the Gaussian carrier density distribution is approximately 1.1 µm.

The through-wafer, backside TPA laser irradiation technique was used to examine the single-event effects on a 201-stage ring oscillator (RO) operating at voltages well below the nominal power supply of 1.2 V. The ring oscillator was fabricated by MOSIS using the IBM 130 nm CMRF8RF process. A near-infrared, through-wafer image of most of this structure can be seen in Figure 16. The threshold voltages of NMOS and PMOS transistors in this process are 375 mV and 435 mV, respectively. The power supply voltage for the ring oscillator was varied from 200 mV to 550 mV. All experiments were performed at room temperature.

## Experimental Results

Traditionally when charge is deposited in a RO due to a single-event, a temporary modulation in the frequency is seen, with the RO subsequently returning to its original

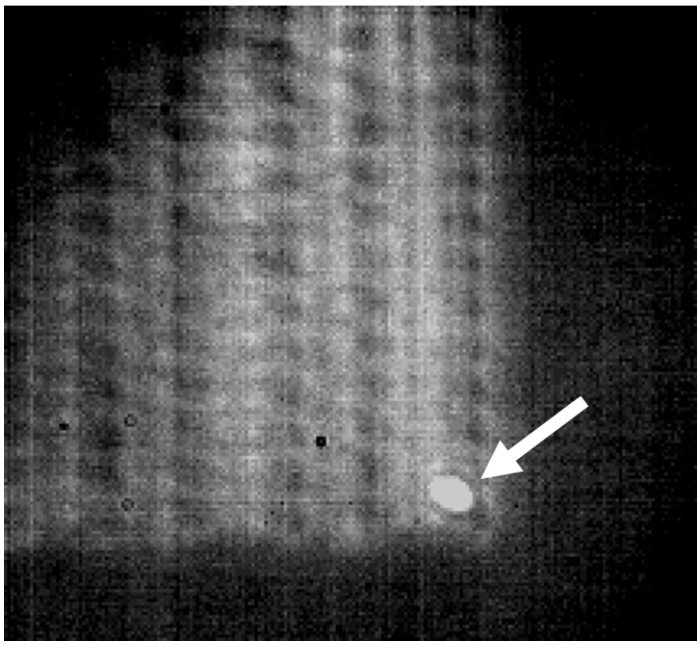


Figure 16. Near infrared (NIR) image of a laser strike location (indicated by the arrow) in the ring oscillator.

frequency. However, as devices scale, circuits can operate at multi-gigahertz frequencies, forcing circuit designers to fabricate ROs with large numbers of stages in order to obtain a stable signal that can be easily measured with standard test equipment. As the number of stages increases, it becomes progressively easier to induce higher harmonic frequencies in these ROs [Sas82]. However, for this set of experiments, the harmonic oscillation of ROs will be capitalized upon to characterize the single-event vulnerability of a given technology. The minimum laser pulse energy at which sustained harmonic oscillations occur will identified as the threshold for a given power supply voltage.

When the 201-stage RO is operated at the nominal power supply voltage of 1.2 V, the fundamental operating frequency is approximately 22 MHz. Figure 17 shows that after depositing charge on a device in the chain, the RO begins oscillating at a third harmonic of the fundamental frequency at roughly 66 MHz. These oscillations are sustained until the power is reset to the RO.

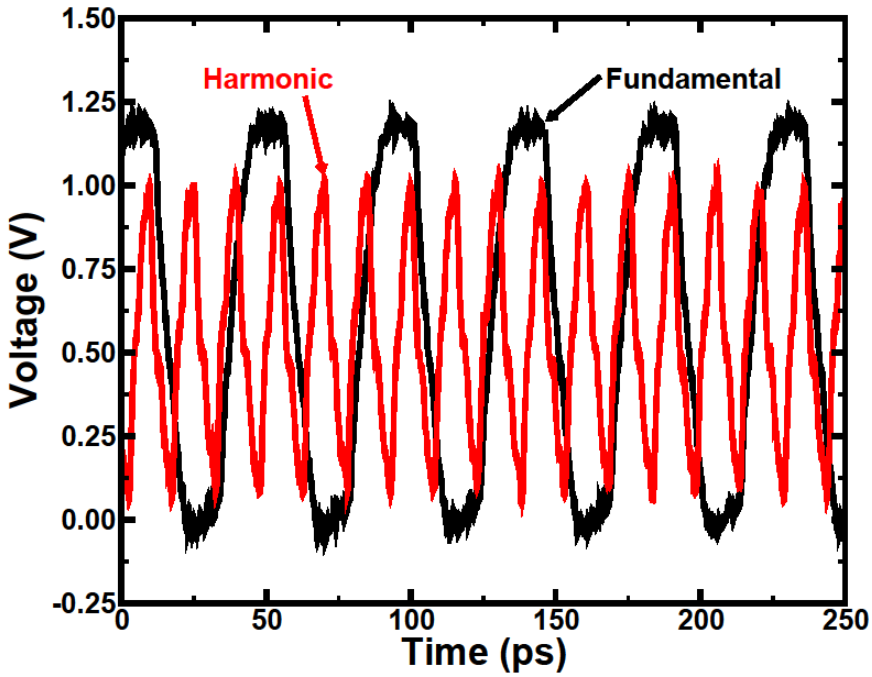
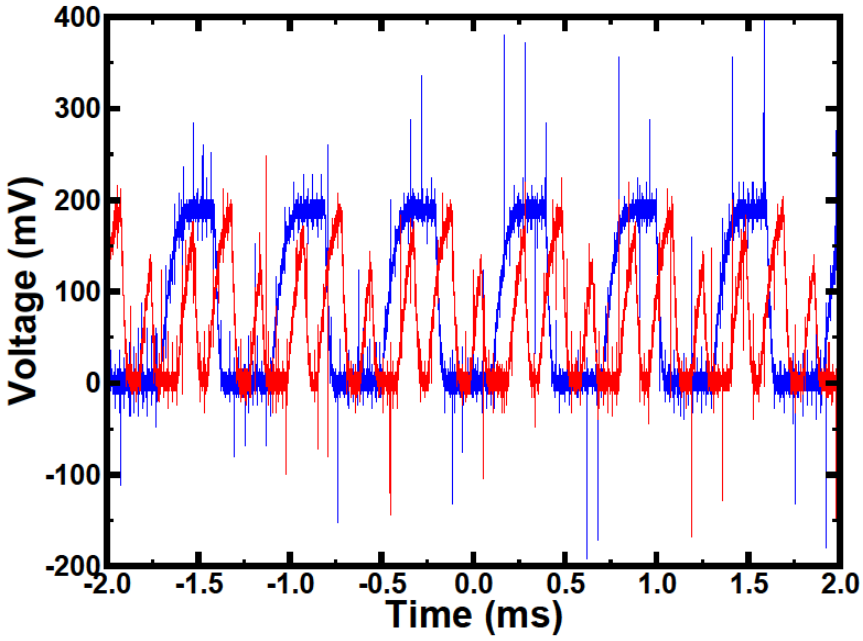
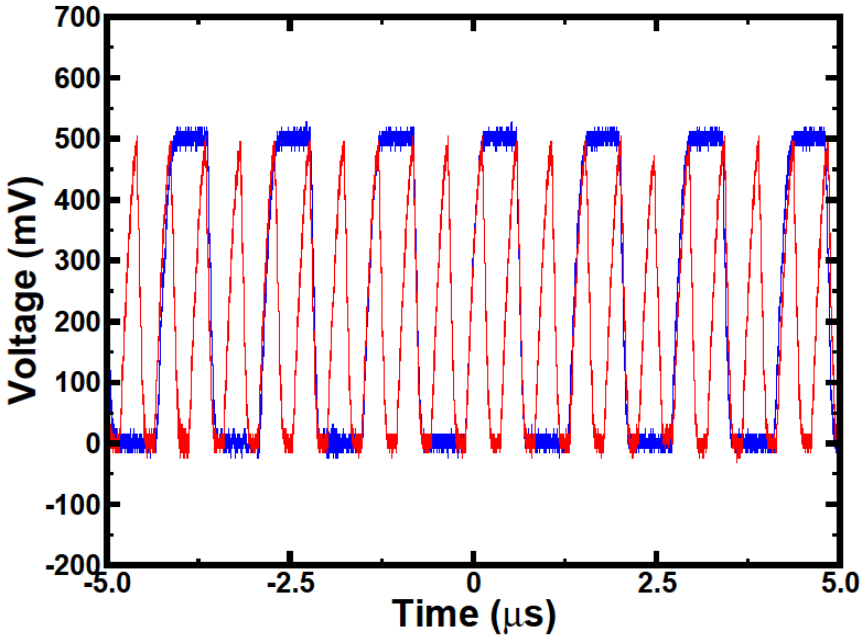



Figure 17. The fundamental frequency of a 201-stage ring oscillator operating at the nominal supply voltage of 1.2 V is roughly 22 MHz. After charge deposition from a laser strike, higher harmonic oscillation is induced and the ring oscillator operates at a third harmonic (66 MHz).

The fundamental frequency of the RO is determined by the rise and fall times of the inverters in the oscillator. The observed laser-induced error mode causes the RO to operate at a frequency higher than the fundamental frequency. Figures 18a and 18b show the original oscillation (blue curves) and the post-strike oscillation (red curves) of the ring oscillator when operating at 200 mV and 500 mV, respectively. For these particular examples, the same laser pulse energy of 5.8 nJ was used for both 200 mV and 500 mV supply voltages to induce the harmonics. It also should be noted that the change in frequency is not specifically a low voltage effect, as the higher harmonics also are seen at the nominal operating voltage (and an example is shown in Figure 17) and at every voltage in between.




(a)




(b)

Figure 18. Change of frequency due to laser strikes in a 201-stage ring oscillator operating at (a) 200 mV and (b) 500 mV. The blue curves are the oscillator pre-laser strikes and the red curves are the oscillator after the laser strikes.

The harmonics also could be induced by manipulating the power supply and enable voltage when the laser beam was blocked. The operation of ring oscillators forces most nodes to be either high or low, but there will always be at least one node that is in a transition state [Sas82]. It is the propagation of the transition state through each inverter that creates the oscillation. If there is only one transition state, the frequency of oscillation is fundamental. When there is more than one transition state that is separated by stable high and low nodes, then the frequency of oscillation will be a harmonic. A harmonic is more likely to occur in ring oscillators with a large, odd number of stages than with a small number of stages [Hou83].

However, recalling the output of the simulated ring oscillator shown in Figure 15, in simulation, charge deposition from a single-event results in independent transients that propagate indefinitely in the RO. Experimentally though, the RO instead operates at a harmonic with a frequency that is exactly some multiple of the fundamental frequency. By finding the x-intercepts of a Nyquist diagram, which shows the magnitude and frequency of a transfer function, the stable operating points in a system with feedback, like a ring oscillator, can be found. The transfer function of an RO is given by

$$G(j\omega) = \frac{1}{(j\tau\omega + 1)^N} \tag{14}$$

where N is the number of stages in the RO and $\tau$ is the inverter propagation delay [Chi09]. By depositing a small amount of charge on any inverter in the RO, a temporary modulation in the output frequency is seen, which corresponds to some phase error. The curve of the Nyquist diagram relates to the operating frequency, so this resultant phase error/frequency modulation moves the RO operation off the negative x-axis on the Nyquist curve, and away from the current (fundamental) stable operating point. The

points at which the curve intersects the negative x-axis are the only stable points of operation. By changing the phase temporarily due to charge deposition from a single-event or from perturbations in the power supply and enable voltages, the ring oscillator operation is moved along this curve to an unstable point, and the operation will eventually return to the stable operating point at the fundamental operating frequency. If the amount of charge is large enough to move the curve to another stable point (to another intersection along the x-axis), the RO will then operate at a harmonic. If the amount of charge deposited is not large enough to move to another stable operating point, then there will be a temporary modulation in the output frequency, but the ring oscillator output will settle back to the fundamental operating frequency. By experimentally determining the minimum laser pulse energy required to force a ring oscillator to operate at a higher harmonic frequency, the equivalent to the amount of charge required to force the RO from the fundamental stable point (m=0) to the next stable point on the Nyquist diagram is found.

The theoretical limit of the harmonics is determined by the number of stages, and is given by the equation

$$m = \left\lfloor \frac{N-3}{4} \right\rfloor \tag{15}$$

where N is the number of stages in the RO, and m is the order of the harmonics. Figures 19a-c show an example of a Nyquist diagram constructed in Mathematica, and using the transfer function for a ring oscillator as given in Equation (14). All three figures are of the same Nyquist diagram, but Figures 19b and 19c are zoomed-in views to show the x-intersects. The propagation delay for a single inverter used in these simulations was directly measured from the IBM 130 nm CMRF8SF process (112 ps) 201-stage RO used

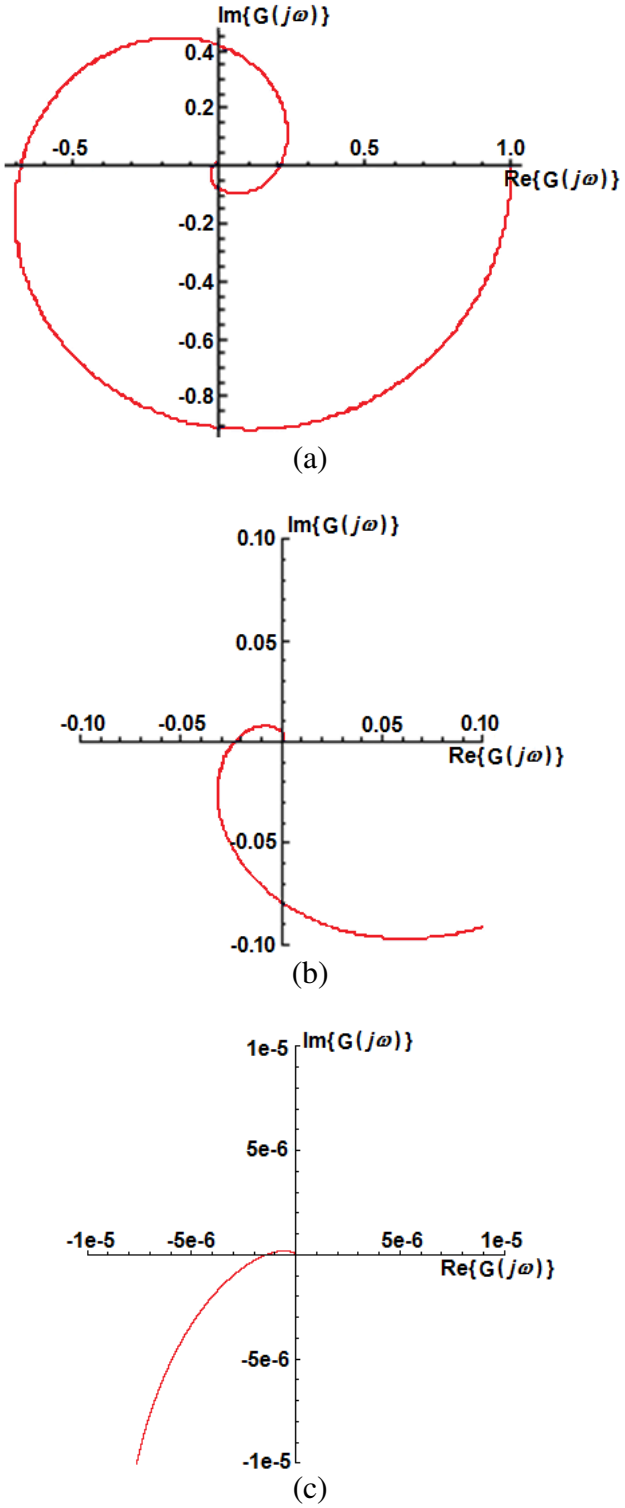



Figure 19. Nyquist diagram showing the transfer function [as given in Equation (14)] of a 13-stage (N=13) inverter-based ring oscillator with an inverter stage delay of 112 ps. The x-intercepts show to the stable operating points, which force the ring oscillator to operate at a frequency that is a multiple of the fundamental. The harmonics correspond to values of m of (a) 0, (b) 1, and (c) 2.

in the laser experiments when the power supply voltage was the nominal 1.2 V, but only 13 stages (N=13) were used for this particular simulation for the sake of simplicity. This results in a value of m of

$$m = \left\lfloor \frac{13-3}{4} \right\rfloor = \left\lfloor \frac{10}{4} \right\rfloor = \lfloor 2.5 \rfloor = 2 \qquad (16)$$

and the three intersections with the negative x-axis (corresponding to m=0, 1, 2) can be seen in Figures 19a-c.

Therefore, the presence of higher harmonic oscillation in an RO indicates the presence of an SET pulse that can propagate indefinitely through ULP circuits. These pulses are responsible for causing SEUs, and the minimum laser pulse energy required to introduce these types of pulses in the circuit is a very good indicator of the vulnerability of the circuit to single-events. By finding the minimum laser pulse energy required to induce harmonic generation in a ring oscillator, the single-event vulnerability for any technology can be found.

Previous work [Har01], [Sei01a], [Shi02], [Gad07] has shown that as power supply voltages are decreased, the soft error rate and error cross-section of combinational circuits increase. However, these studies have focused on supply voltages just a few hundred milli-volts lower than the nominal power supplies. Figure 20 shows that the minimum laser pulse energy required to upset a 201-stage RO fabricated in the IBM 130 nm process plotted as a function of the power supply voltage. For these experiments, an upset is assumed to have occurred when the multiple transient pulses discussed above are detected within the RO. For two-photon absorption laser experiments, the amount of charge deposited increases with the square of the laser pulse energy. At the same time, threshold deposited charge varies linearly with the supply voltage, while the deposited

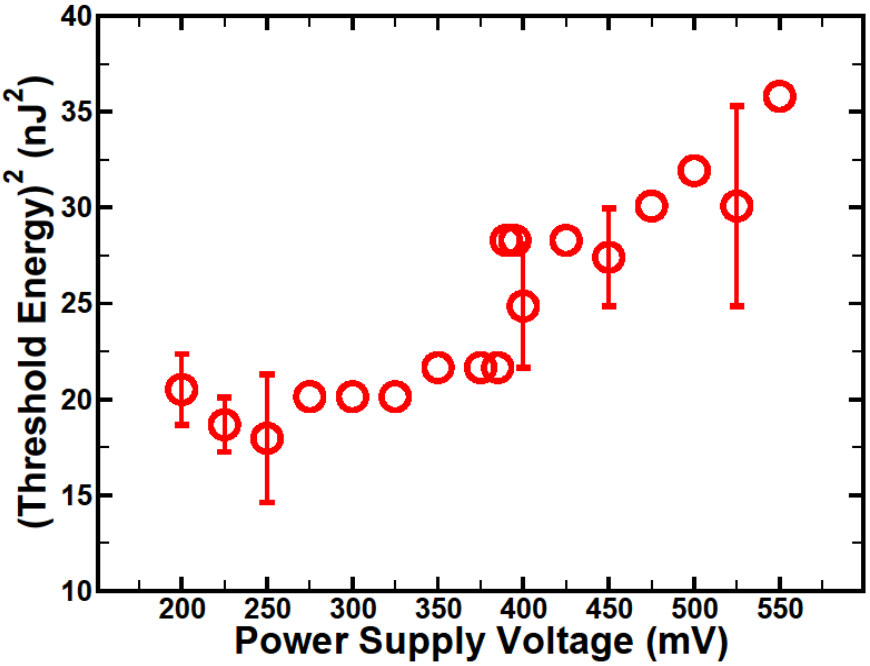


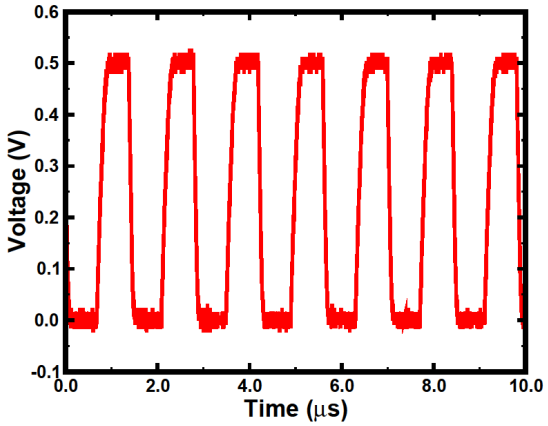

Figure 20. The minimum threshold laser pulse energy required to cause an upset in a 201-stage ring oscillator decreases linearly as power supply decreases, until the circuit enters the subthreshold region, at which point the threshold laser pulse energy remains constant.

charge varies quadratically with the laser pulse energy. Therefore, a plot of the square of threshold laser pulse energy versus the supply voltage will be a straight line outside of the subthreshold region (as is expected from previous work [Har01], [Sei01a], [Shi02], [Gad07].) However, when the supply voltage is lower than the threshold voltage, there is an inflection point at which the amount of charge required to upset the RO becomes independent of supply voltage. The difference in the average threshold laser pulse energy and the extremes is due in part to the mechanical drift in the laser spot position.

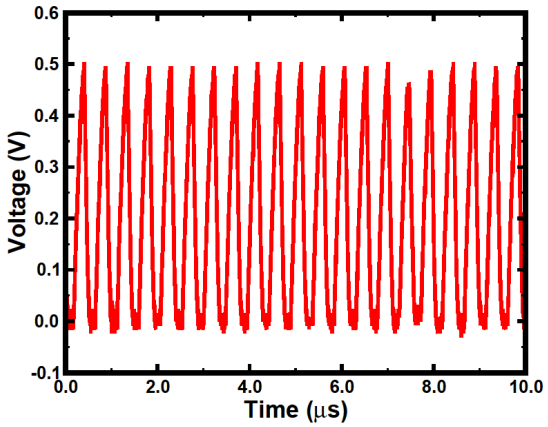
As power supply voltages decrease, the amount of charge required to generate an SET decreases, which means it is easier to induce oscillations at harmonics higher than those achieved at the nominal power supply voltages. At the nominal voltages, the time each node is held at either high or low is much shorter than when the devices are operated at

lower voltages. Therefore, there is less time for additional pulses to propagate. This makes it less likely that the oscillator will operate at any harmonic, let alone at multiple harmonics. Figures 21a-c show the fundamental frequency, a third harmonic (induced by a laser pulse energy of 5.8 nJ) and a seventh harmonic (induced by a laser pulse energy of 12.5 nJ) after charge was deposited by the laser in a 201-stage ring oscillator.

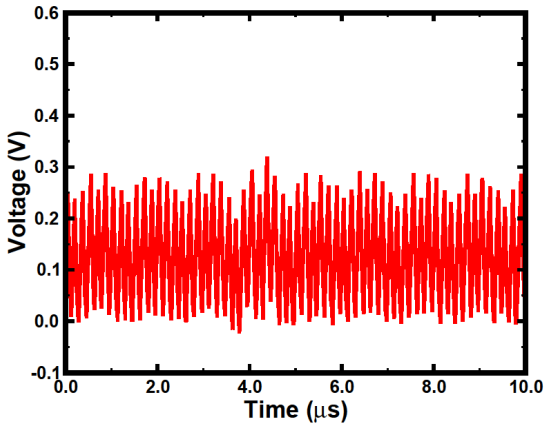
Ring oscillators with large numbers of stages allow for characterization of technologies by finding the minimum energy at which harmonic oscillation (an upset) occurs. Above the threshold voltages of the technology, the minimum energy required for upset decreases with decreasing power supply voltage (i.e., the single-event susceptibility increases). At power supply voltages below the threshold voltages, the single-event vulnerability is relatively constant. Simulations also were able to induce the higher harmonics seen during the laser experiments. The harmonics were able to be induced at every supply voltage from 200 mV to 1.2 V.




(a)




(b)




(c)

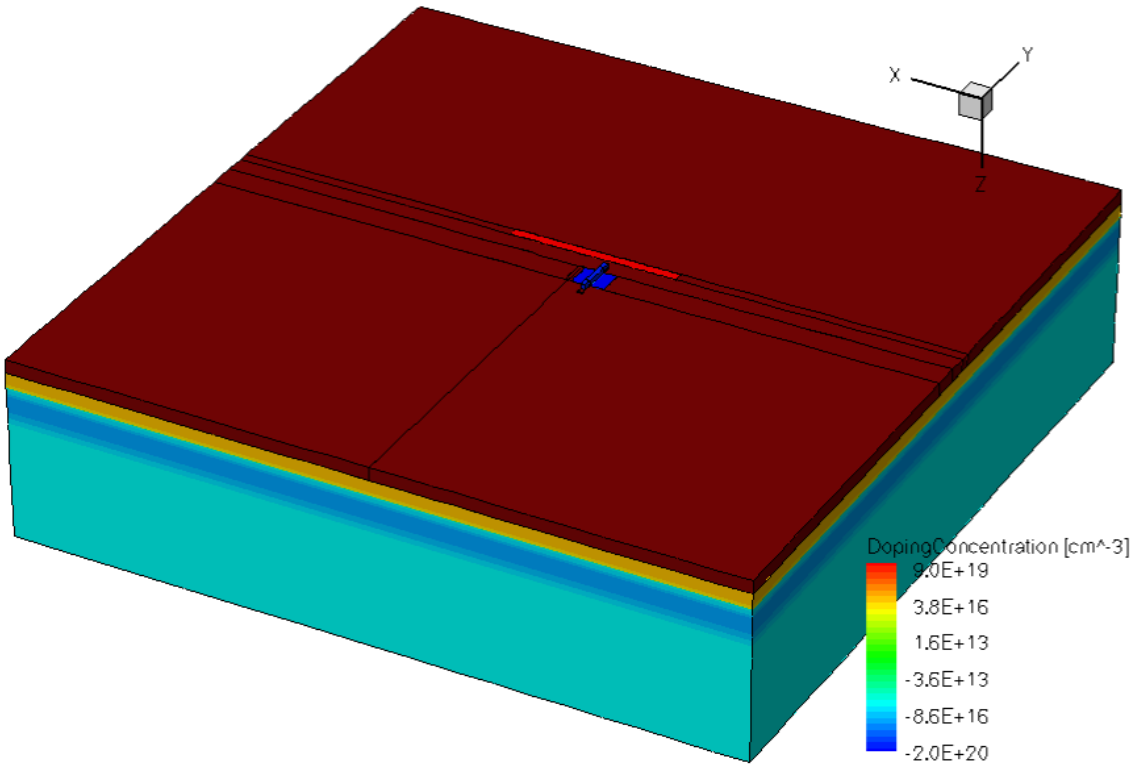
Figure 21. A 201-stage ring oscillator with a power supply voltage of 500 mV operates at (a) a fundamental frequency of 860 kHz. The ring oscillator operates at (b) a third harmonic frequency of 2.6 MHz after a laser strike with energy of 5.8 nJ, and (c) a seventh harmonic frequency of 6 MHz after a laser strike with energy of 12.5 nJ.

# CHAPTER V

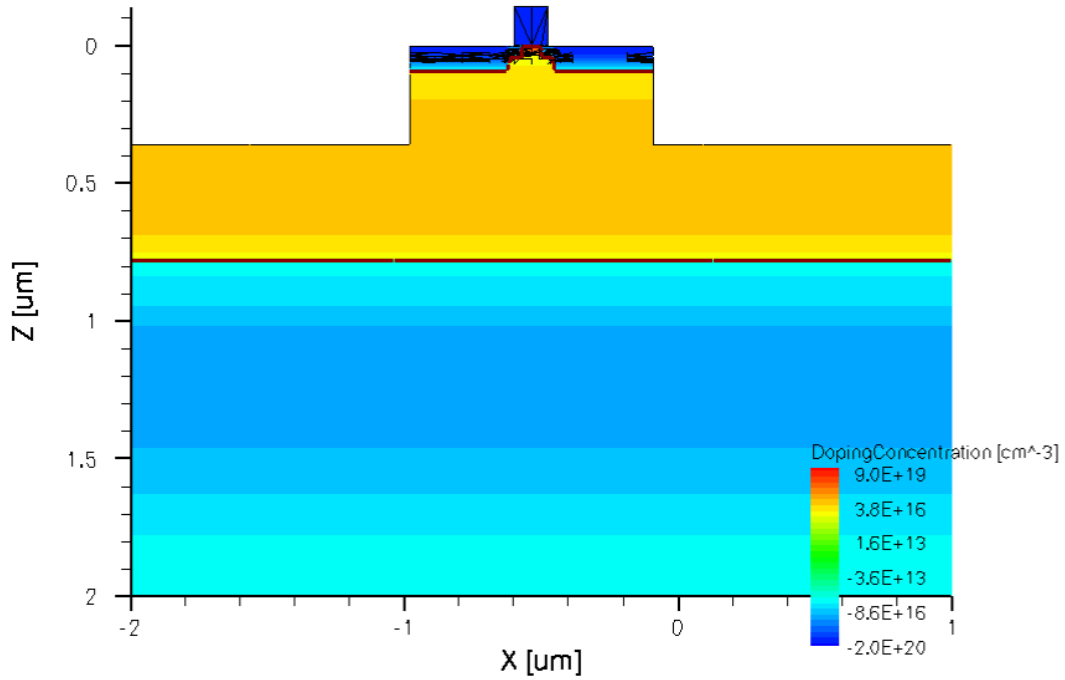
## SINGLE-EVENT EFFECTS IN ULP CIRCUITS

Low power supply voltages result in small electric fields within individual devices. Because the charge collection after a single-event hit at a node is a strong function of the electric fields present in the device, subthreshold operation may have different charge collection characteristics than those of devices operating at nominal supply voltages. Also, at subthreshold supply voltages, there is a small voltage differential between the transistor source and drain, making it difficult to turn-on the parasitic bipolar transistor by an ion strike. These factors may result in different charge collection values for ultra-low power circuits as compared to normal circuits. On the other hand, due to extremely low currents in the restoring devices, any charge collected at a node will take a much longer time to dissipate, resulting in single-event transient (SET) pulses orders of magnitude longer than those generated to nominal supply voltages.

This chapter presents results from simulations of CMOS circuits operating with power supply voltages in the subthreshold region, in order to examine SEEs on ULP circuits. The simulations were conducted in Cadence Spectre using the IBM 130 nm CMRF8RF PDK and using 3D transistor computer-aided design (TCAD) transistors calibrated to the same PDK. Figures 22a and 22b show the entire 3D TCAD PMOS structure, including shallow trench isolation, substrate, and well contact and a cross-sectional view of the PMOS transistor, n-well, and substrate. Likewise, Figures 23a and

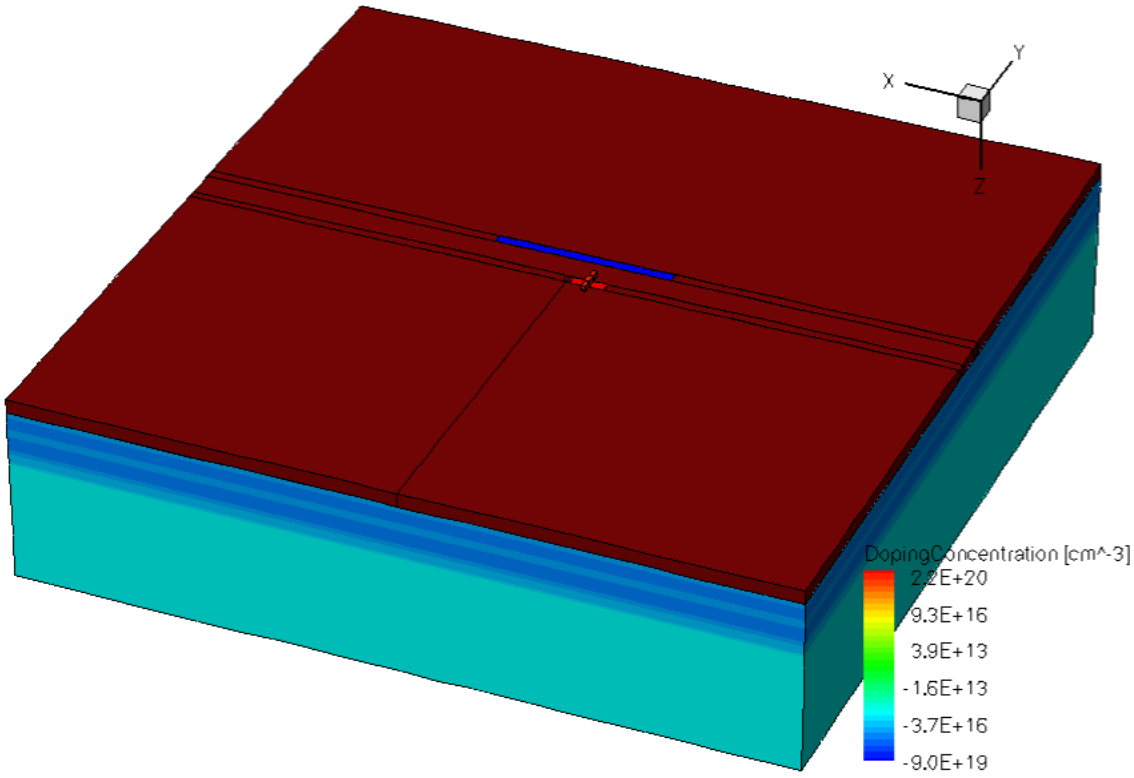



(a)

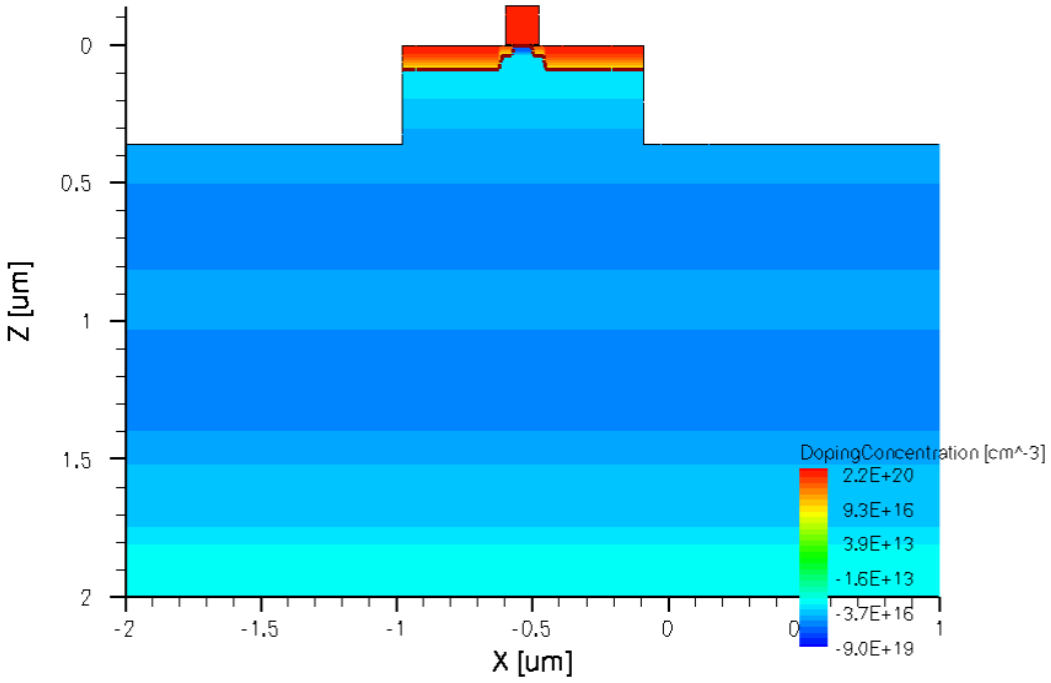



(b)

Figure 22. (a) 3D TCAD structure used for all single PMOS transistor simulations. The structure was calibrated to the IBM 130 nm CMRF8SF process. (b) The cross-sectional view of a single PMOS transistor.




(a)




(b)

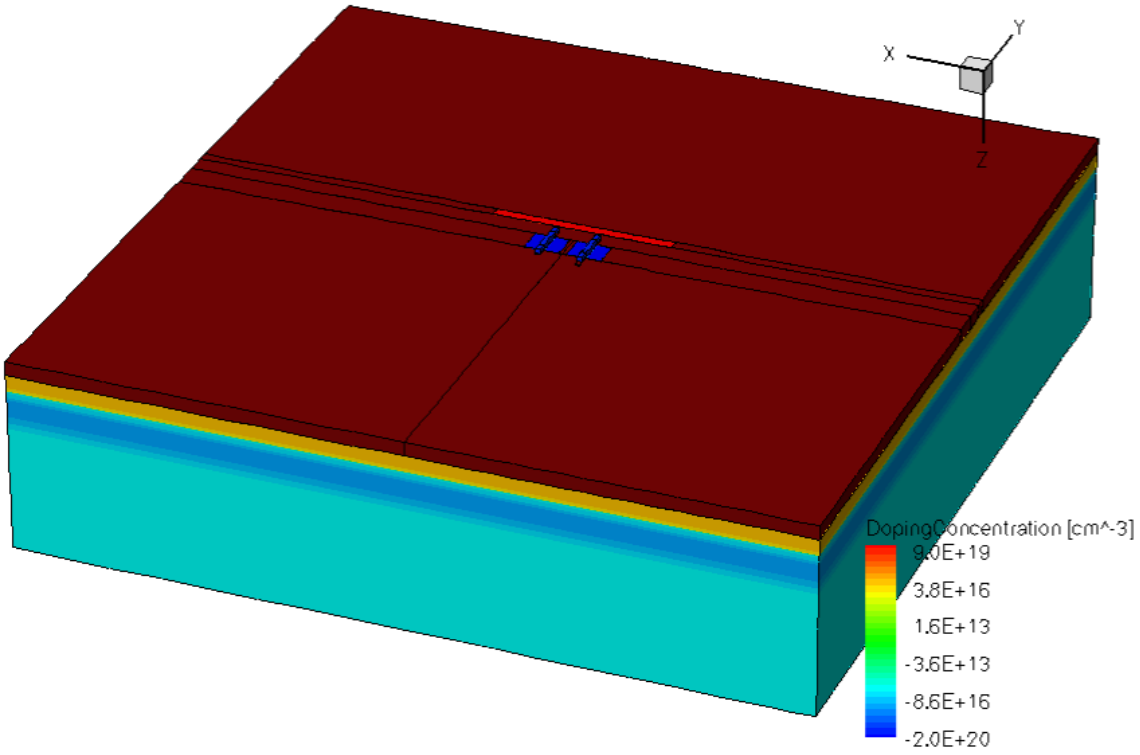
Figure 23. (a) 3D TCAD structure used for all single PMOS transistor simulations. The structure was calibrated to the IBM 130 nm CMRF8SF process. (b) The cross-sectional view of a single PMOS transistor.

23b show the entire 3D TCAD NMOS structure, with the STI and deep p-well contact, and a cross-sectional view of only the NMOS transistor and substrate.

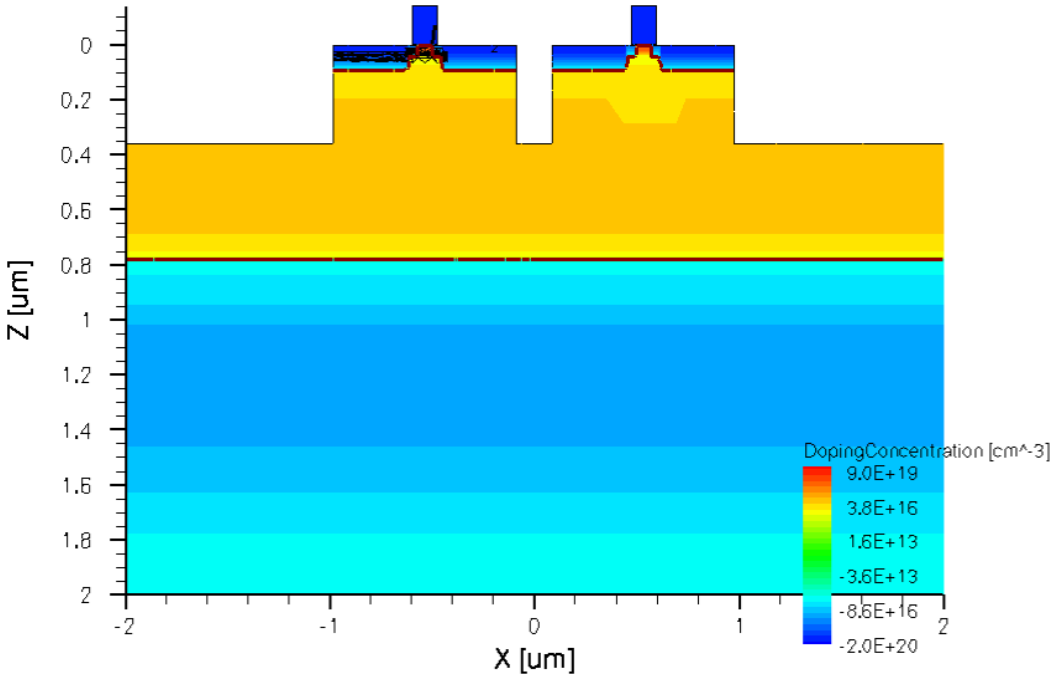
These structures were used for all single transistor simulations. Similarly, Figures 24 and 25 show the entire 3D TCAD structures used for two transistor simulations, as well as the cross-sections of the transistors to illustrate the device spacing. All simulations were conducted using Vanderbilt University's Advanced Computing Center for Research and Education (ACCRE) computing cluster [ACC].

## Simulation Set-up

Transistor current models are notoriously unreliable when operating in the subthreshold region [Sze81]. In order to verify the accuracy of the 3D TCAD models calibrated to the IBM 130 nm CMRF8RF CMOS process [Amu06a], the maximum operating frequency was simulated in Cadence using Spectre and the IBM 130 nm PDK. This was done by finding the rise and fall times of a single inverter over a range of power supply voltages from the deep-subthreshold regime to slightly above the nominal operating voltage. Next, the frequency of the 201-stage ring oscillator used in the laser experiments was measured over the same range of power supply voltages. The simulated maximum operating frequencies and the measured ring oscillator frequency (normalized to the number of stages) are shown as a function of power supply voltage in Figure 26. There is good agreement between the two curves, with the greatest deviation, a factor of 2.7, occurring at 200 mV. The fact that the largest deviation is deep in the subthreshold region is to be expected since that is where the current models are the most unreliable.

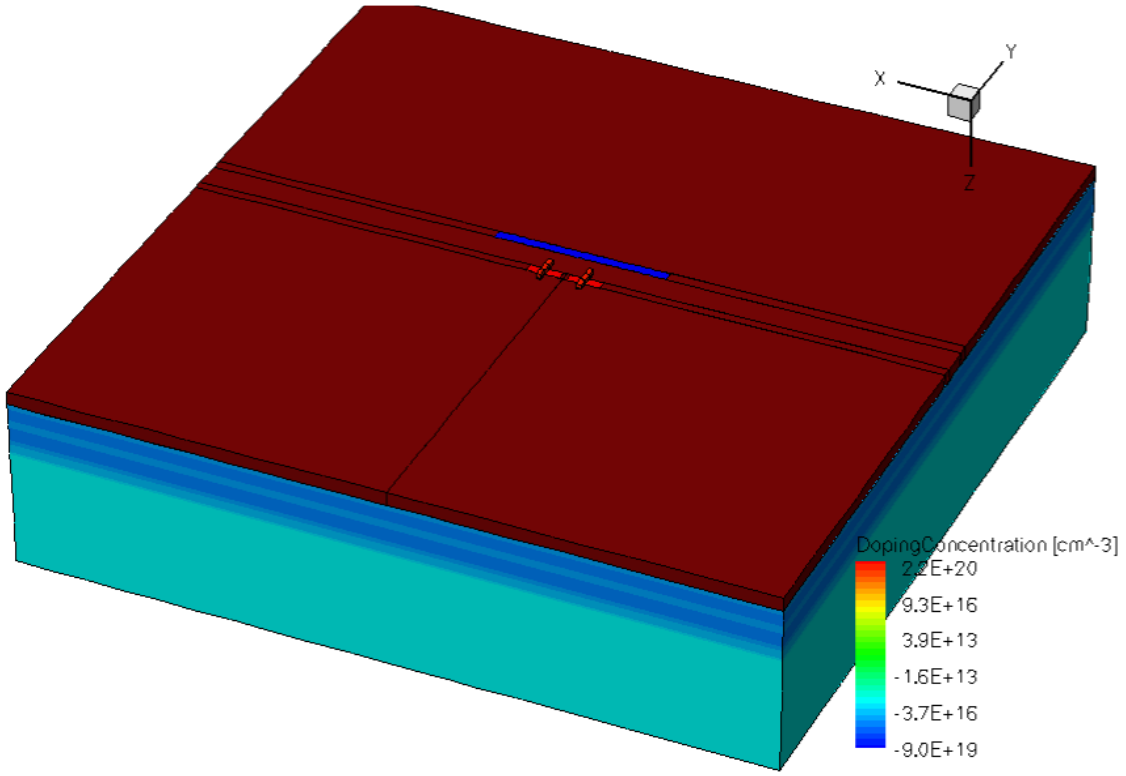



(a)

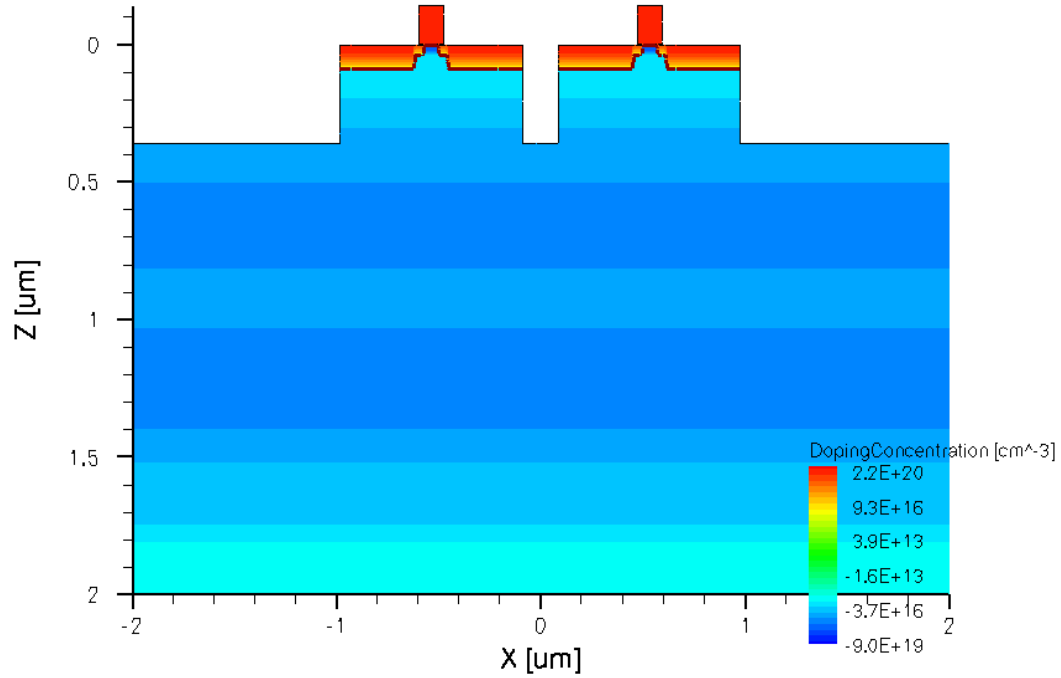



(b)

Figure 24. (a) 3D TCAD structure used for all simulations with two PMOS transistors. The structure was calibrated to the IBM 130 nm CMRF8SF process. (b) The cross-sectional view of two PMOS transistors with minimum device spacing.




(a)




(b)

Figure 25. (a) 3D TCAD structure used for all simulations with two NMOS transistors. The structure was calibrated to the IBM 130 nm CMRF8SF process. (b) The cross-sectional view of two NMOS transistors with minimum device spacing.

The maximum operating frequency directly relates to the current drive, so the close relationship between the simulated and measured frequencies also holds for current. To verify the calibration of the 3D TCAD models, the $I_D$-$V_D$ curves for an NMOS and a PMOS transistor [Amu06a] were simulated in Cadence using Spectre, as well as using TCAD mixed-mode simulations, and can be seen in Figure 27. No more than a 20 percent difference between the PMOS PDK and TCAD curves is observed (this difference occurred when the drain was biased at 1.2 V). A 12 percent difference between the NMOS PDK and TCAD curves (at 0.6 V) is obtained. Because of the excellent agreement between the measured and PDK-simulated operating frequencies, and the PDK- and TCAD-simulated $I_D$-$V_D$ curves, it is concluded that the models are sufficient for simulating in the subthreshold region.

In this chapter, transient pulsewidth simulations are performed as a function of power supply voltage. To find these transients, a string of five minimum-sized, matched current drive inverters are used. All of the transistors are modeled in SPICE and then one transistor is replaced with a 3D Technology Computer-Aided Design (TCAD) device (either NMOS or PMOS, as specified.) For all TCAD simulations, the heavy ion always entered at normal incidence and had a track length of 3 μm. This track length was chosen because it would penetrate deeper than the n-well in the PMOS transistors, but not so deep to short the struck transistor drain to the substrate. The full-width, half-rail transients that resulted were then measured at the end of the chain of inverters to examine the transients that would propagate to additional circuitry. The 3D TCAD transistor also allows for the measurement of a variety of semiconductor device characteristics, which

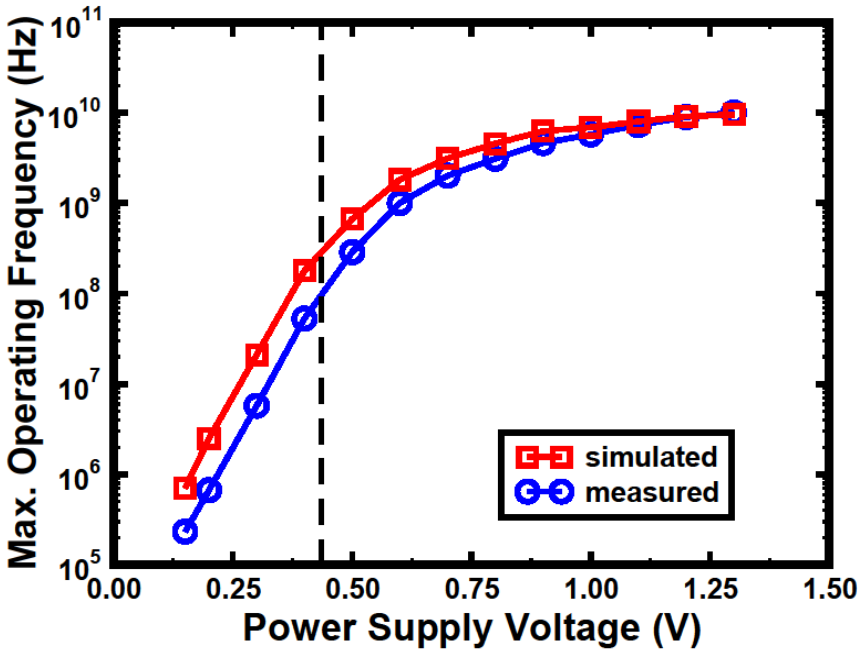



Figure 26. The maximum operating frequency as measured from a 201-stage ring oscillator fabricated in the IBM 130 nm 8RF process and simulated using the PDK for the same process. Dashed line represents the NMOS threshold voltage.

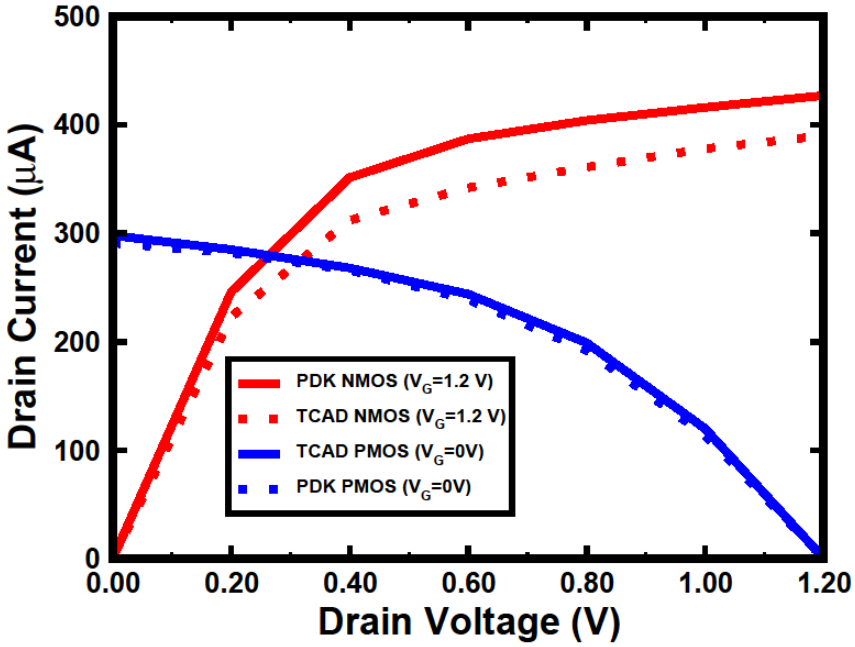



Figure 27. $I_D$-$V_D$ curves for NMOS (red curves) and PMOS (blue curves) transistors are simulated using Spectre and the IBM CMSF8RF 130 nm PDK (solid lines) and 3D TCAD models calibrated to the same PDK (dashed lines).

can be used to understand the movement of charge and its collection after a single-event strike.

The second set of 3D TCAD simulations have the same set-up as the single transistor implementations; however, for these simulations, two NMOS or two PMOS transistors are modeled in a single TCAD structure, with the remaining transistors are modeled using SPICE. The inclusion of multiple transistors in the 3D TCAD structure allows for additional charge collection mechanisms, such as charge sharing, which cannot be accounted for in a single transistor model. The full-width, half-rail transient pulsewidths reported are measured at the output of the last inverter in the string, again to provide the reported are measured at the output of the last inverter in the string, again to provide the transients that would be affecting any additional circuitry.

## Simulation Results

To support higher harmonic oscillation in ring oscillators with large numbers of stage, more than one transistor must be in a transition state (as discussed in detail in Chapter IV). Additionally, as the number of stages in the ring oscillator increases, the generated transient pulsewidth must also increase, because as the transient propagates through a chain of inverters, if it is not sufficiently wide, the pulsewidth attenuates [Baz97], [Mav02], [Dod04b], [Gad04], [Baz06], [Fer06b], [Nar06b], [Gai07]. Figure 28 shows the pulsewidth required to propagate through various inverter chain lengths. As is expected, with decreasing power supply voltage, an increase in the minimum transient pulsewidth is required.

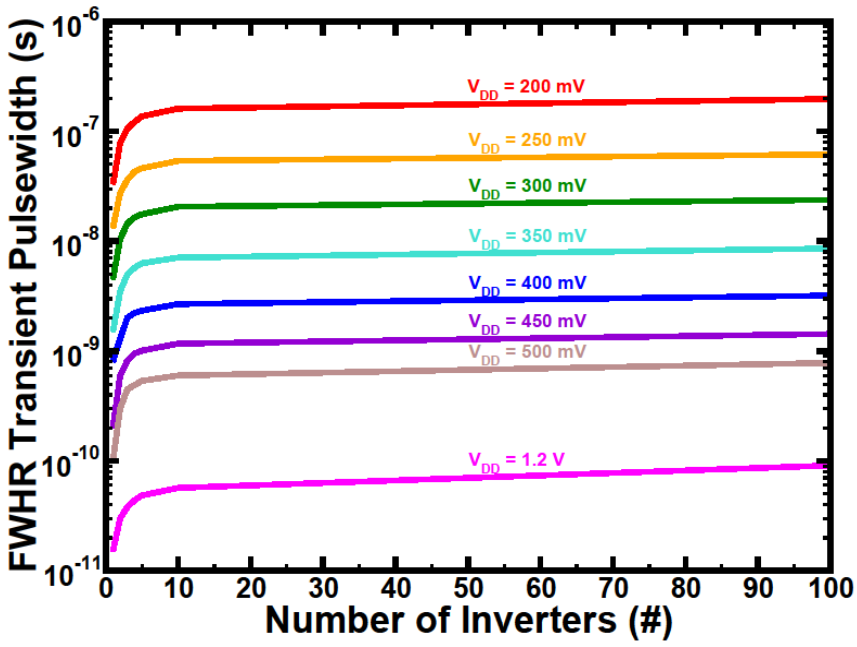


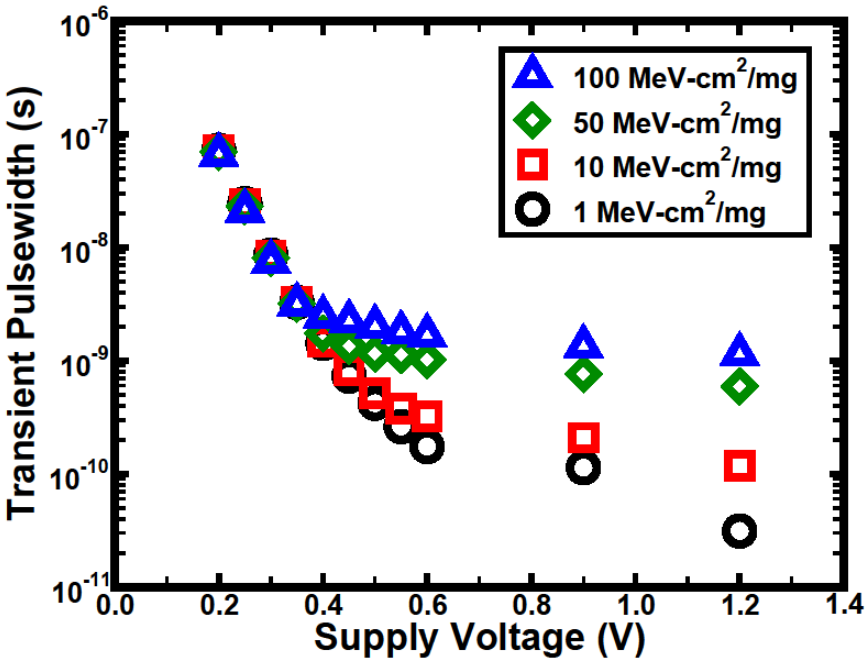

Figure 28. Simulation showing the minimum transient pulsewidth required to propagate through various lengths of inverter chains. The transient pulsewidth required for propagation increases as expected as the supply voltage decreases.

The number of inverters in the chain directly relates to the number of stages in a ring oscillator. If the pulsewidth is not wide enough to propagate through the entire oscillator back to the original hit node, the oscillator may temporarily operate at a higher harmonic, but due to the pulse attenuation, they will die out. For example, from Figure 28, a transient must have a pulsewidth greater than 20 ns to see sustained higher harmonic oscillation in an 11-stage ring oscillator operating at 300 mV. The decreased drive current associated with a lower supply voltage results in greater rise and fall times for each inverter, which then requires that pulsewidths must increase to propagate un-attenuated through the inverter string.

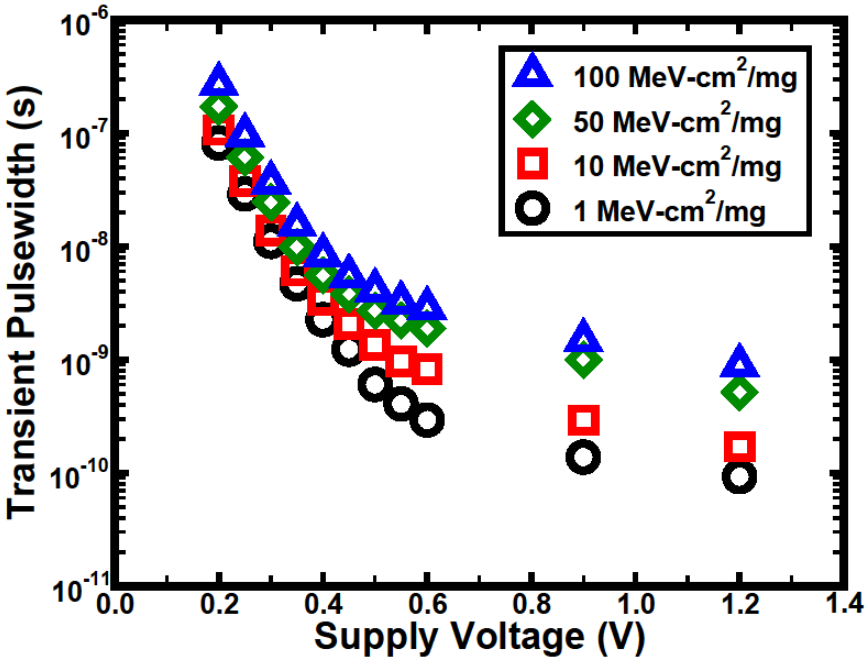
*Single 3D TCAD Transistor Simulations*

As seen previously in Figure 9 in Chapter III, lower supply voltages lead to lower drive currents. These currents can be several orders of magnitude lower in the subthreshold region than the drive currents of devices operating at the nominal voltage levels. Lower drive currents mean that nodal voltages will take longer to recover after a transistor is struck by a heavy ion, which in turn results in longer pulsewidths. Figures 29a and 29b show the full-width at half-rail transient pulsewidths created when simulating heavy ion hits at a variety of ion LETs values on a (a) p-channel and on a (b) n-channel transistor. The transients plotted were generated by striking one transistor in a string of five inverters. The inverter string was simulated in mixed-mode using one calibrated 3D TCAD transistor and the remaining transistors were modeled using SPICE parameters [Amu06a].

The transients generated in the inverter strings for a given ion LET show an increase in single-event transient pulsewidth as the supply voltage is lowered for both NMOS and PMOS transistors, as would be expected. In particular, the transient generated on the same calibrated 3D TCAD PMOS device by an ion with an LET 10 MeV-cm$^2$/mg when it is biased at 1.2 V (roughly 120 ps) is seven times narrower than the device biased at 450 mV (830 ps), and more than two orders of magnitude narrower (620x) than that of the device biased at 200 mV (72 ns). Likewise, for the NMOS transistor, when biased at the nominal supply voltage of 1.2 V, the transient pulsewidth that results from an ion with an LET of 10 MeV-cm$^2$/mg was roughly 170 ps, which is 12 times narrower than when the supply voltage is 450 mV (which results in a pulsewidth of 2.1 ns). When the




(a)




(b)

Figure 29. Simulated 3D TCAD (calibrated to the IBM 130 nm CMRF8SF process) full-width at half-rail single-event transient pulsewidths, generated by strikes on (a) a PMOS transistor and (b) an NMOS transistor as a function of power supply voltages and for a variety of ion LETs. As the supply voltage is lowered, the pulsewidths become independent of ion LET for strikes on the PMOS transistor.

inverter is biased at 200 mV, the resulting transient was 107 ns, which is 620 times wider than the pulsewidth resulting from the nominal supply voltage.

There are a few other interesting trends to be noted about the widths of the transients. Additionally, at the higher supply voltages, the transients that result from the ions with LETs of 50 and 100 MeV-cm$^2$/mg are slightly longer in the PMOS transistors than the NMOS transistors. These longer transients that result from high ion LET particles that strike PMOS transistors is to be expected due to parasitic bipolar amplification [Amu06b], [Amu07]. However, at supply voltages of 600 mV and less, ion strikes on PMOS devices create transients that are consistently narrower than those created on NMOS devices. This occurs because it becomes hard to turn on the parasitic bipolar on as a result of the small voltage differential between the source and drain, which is a consequence of the low power supply voltage. Therefore, the charge collection at the struck drain is dependent on 1) the charge collection depth due to the n-well (which for this process is about 1.1 μm deep) [Amu06b], 2) the absence of parasitic bipolar effects, and 3) the hole mobility (which is lower than the electron mobility). The combination of these three factors, translates to reduced charge collection (i.e., shorter SE pulsewidths) for PMOS transistors. Conversely, NMOS transistors collect significantly more charge due to the increased collection depth (due to the lack of n-well, which limits the charge diffusion) [Amu06b], [Tip06] and increased electron mobility; hence, an increase in diffusion charge and longer NMOS transient pulsewidths.

*Soft Error Rates*

Soft Error Rate (SER), which is defined as the rate at which a device or circuit experiences a soft error (a soft error is any random glitch in a signal output that is usually

not catastrophic or destructive, including SETs and SEUs), is related to a number of circuit and device characteristics. In particular though, SER is directly proportional to SET pulsewidth [Buc97] and operating frequency [Sei01b]. By lowering the power supply voltage, the operating frequency decreases (as seen in Figure 11) and longer SET pulsewidths are required to cause an upset (as seen in Figure 28.) At the same time, the decreased restoring currents lengthen SET pulses generated in the circuits. By multiplying these competing effects, decreased frequency and increased SET pulsewidth (the pulsewidth used for this figure were from strikes on PMOS transistors by ions with an LET of 10 MeV-cm$^2$/mg), the resulting effect on soft error can be seen. Figure 30 shows the pulsewidth-frequency product normalized to the nominal power supply voltage

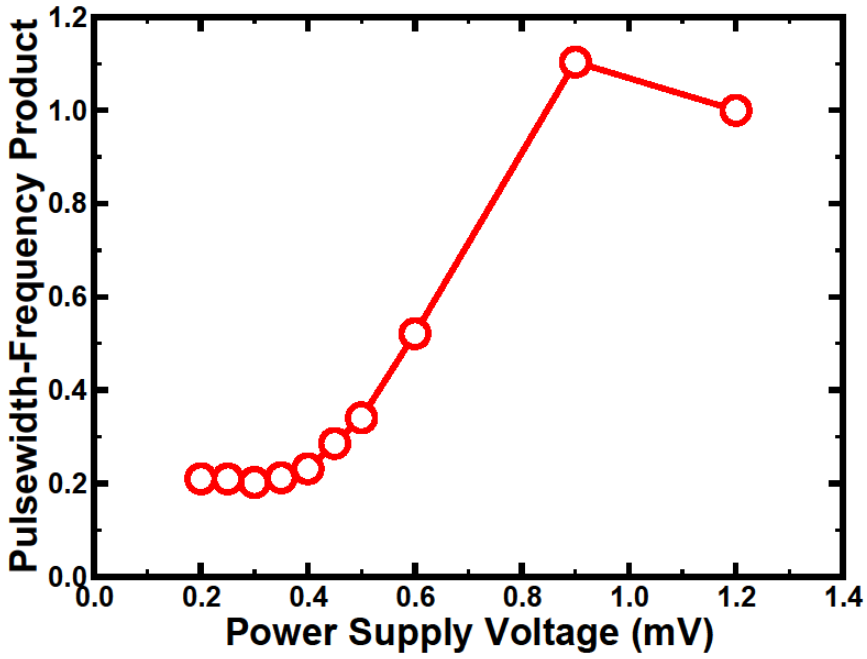



Figure 30. At ultra-low voltages, the pulsewidth-frequency product (normalized to the nominal supply voltage), which is proportional to the soft error rate, decreases due to the faster rate of decrease in operating frequency versus the rate of increase in minimum single-event transient pulsewidth required to upset a circuit at a given power supply voltage.

of 1.2 V as function of power supply voltage. The frequency decreases at a rate that is faster than the rate of decrease in the minimum pulsewidth required for upset, which results in an overall decrease in soft error rate when circuits are operated at ultra-low voltages. When the circuit operates at ULP voltages, the SER is five times lower than when operating at the nominal supply voltage.

*Charge Collection as a Function of Power Supply Voltage*

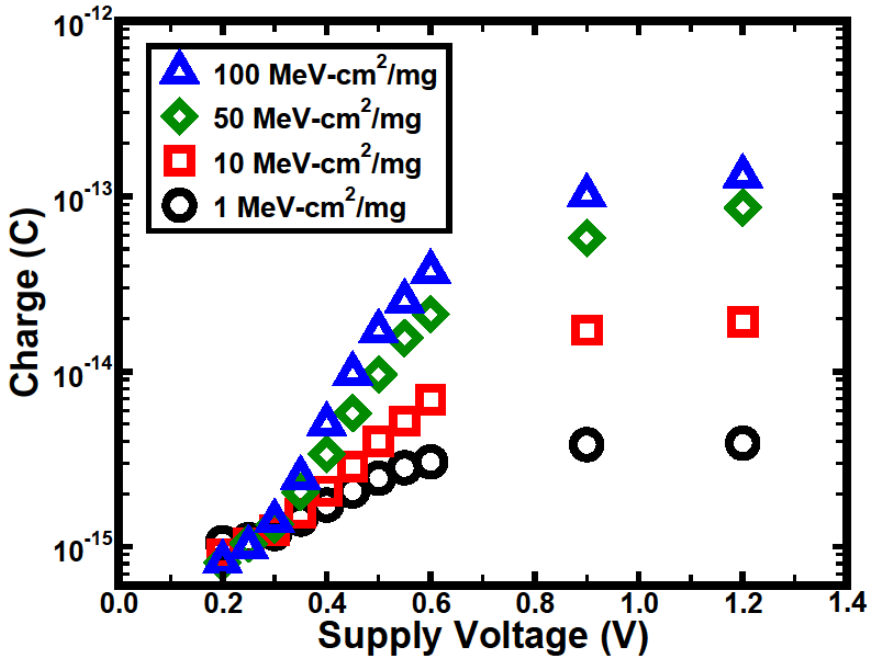
The 3D TCAD simulations also were used to understand the collection of charge as a function of power supply voltage. The currents that result due to the movement of the deposited charge from the heavy ion strike at each transistor contact were integrated to determine the amount of charge that was collected. In the case of the NMOS transistor, the contacts were the drain, gate, source, and p-well; for the PMOS transistor, the contacts were the drain, gate, source, n-well, and substrate. The full Synopsys DEVISE command files for each transistor can be found in Appendix A (NMOS) and B (PMOS), and an example of the mixed-mode command file can be found in Appendix C. This file must be modified for each ion LET, power supply voltage, and transistor type (NMOS or PMOS.)

Additionally, the charge recombined is estimated by finding the peak recombination rate at a variety of time slices. This rate is given in terms of $cm^{-3}/s$, so multiplying the sum of the Auger and Shockley-Reed-Hall maximum recombination rates (which occur along the ion track) by the collection volume (which for all simulations was a surface area of 20 μm by 20 μm, and a depth of 5 μm), the time elapsed between slices, and the charge per electron ($1.6 \times 10^{-23}$ C), the amount of charge that is recombined in a given time period can be found. Additionally, for a given ion LET, the amount of charge

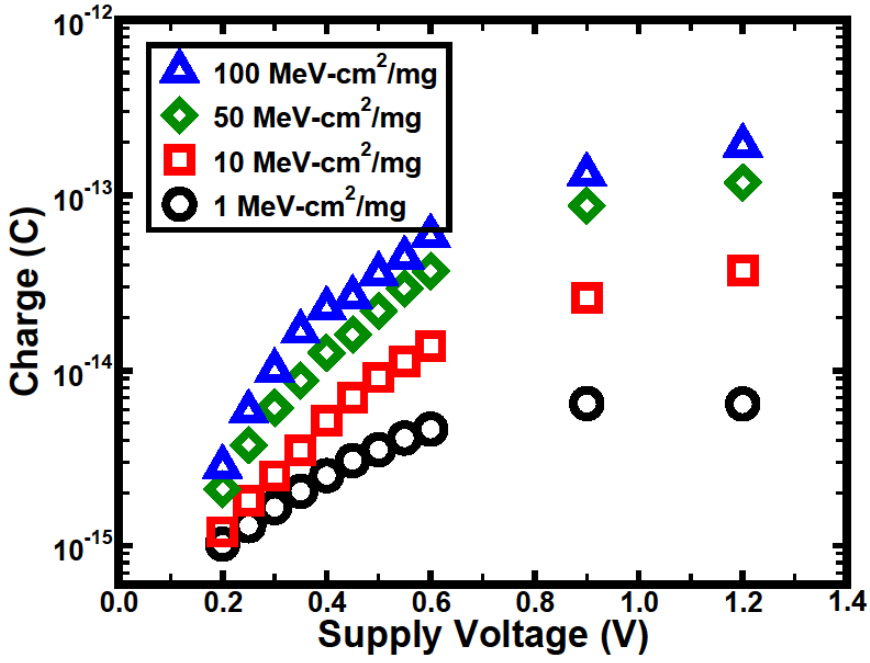
deposited is constant, the charge collected at each contact and the charge that recombined must sum to the total amount of charge deposited. Specifically, the ions with LET of 1 MeV-cm$^2$/mg deposit 30 fC of charge; 300 fC of charge is deposited from ions with LET of 10 MeV-cm$^2$/mg; 50 MeV-cm$^2$/mg LET ions deposit 1.5 pC of charge; and 3 pC of charge is deposited by ions with an LET of 100 MeV-cm$^2$/mg. By knowing the amount of charge deposited and tracking the charge collection at each contact and the charge that is recombined, a complete understanding of charge movement and removal after a single-event strike is possible.

Figures 31a and 31b show the amount of charge collected at the drain after a heavy ion strike at the drain of a PMOS and an NMOS transistor, respectively. With decreasing supply voltage, the amount of charge collected at the drain of the struck transistors decreases. The amount of charge collected decreases by more than two orders of magnitude between from 1.2 V to 200 mV. At the lowest supply voltages, the transistors are no longer conducting, so the amount of charge collected at the drain of the struck transistor becomes independent of ion LET. For all voltages, the PMOS transistor collects less charge than the NMOS transistor due to the n-well depth of the PMOS transistor.

At the same time, the amount of charge collected at the source of the struck transistors increases with decreasing supply voltage (when the heavy ion strike occurs at the center of the transistor drain), as can be seen in Figures 32a and 32b. The percent increase in charge collected at the source is less dramatic than the percent decrease in charge collected at the drain, but the amount of charge collected at the source is more than an order of magnitude greater than the amount collected at the drain. Similarly to the charge collection at the drain, the PMOS transistor also collects less charge at the source

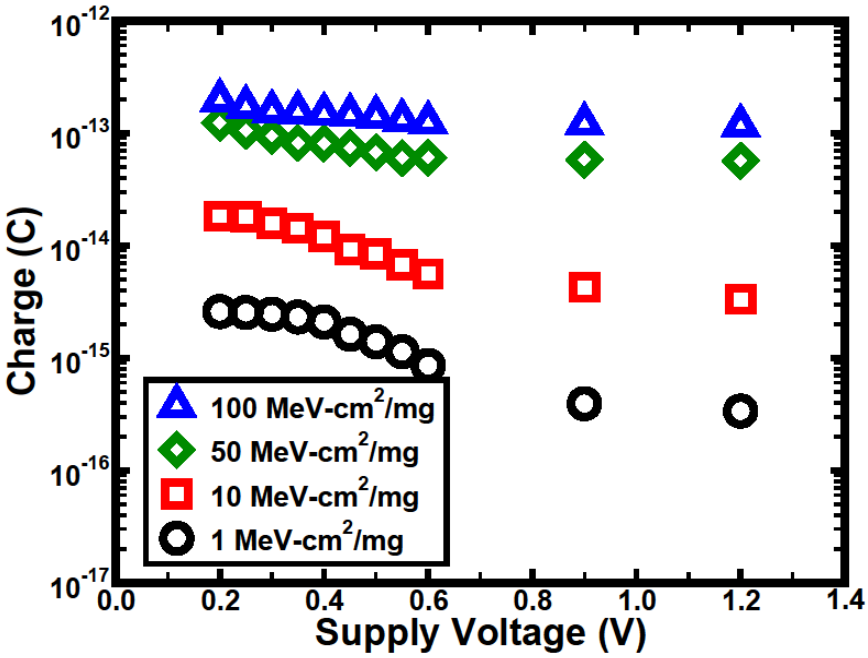



(a)

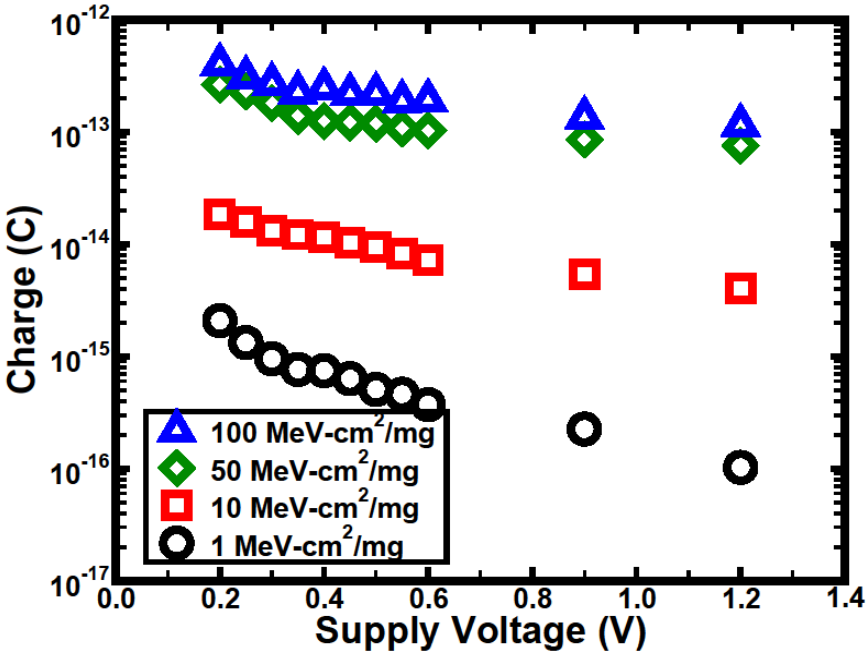



(b)

Figure 31. The charge collected at the drain of a struck (a) PMOS and (b) NMOS transistor calibrated to the IBM 130 nm CMRF8SF process as simulated in 3D TCAD as a function of power supply voltages and for a variety of ion LETs. As the supply voltage is lowered, the amount of charge collected at the drain decreases (by more than two orders of magnitude from 1.2 V to 200 mV.)




(a)




(b)

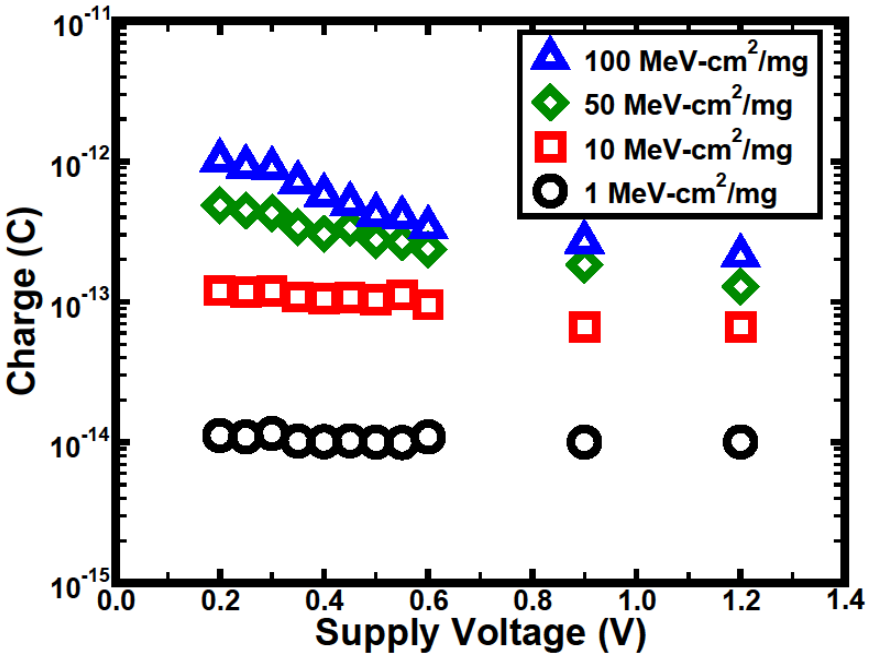
Figure 32. The charge collected at the source of a struck (a) PMOS and (b) NMOS transistor calibrated to the IBM 130 nm CMRF8SF process as simulated in 3D TCAD as a function of power supply voltages and for a variety of ion LETs. As the supply voltage is lowered, the amount of charge collected at the source increases.

for a given ion LET than the NMOS transistor, due to the smaller collection depth. Likewise, the amount of charge that is recombined after a strike on the center of the drain of a PMOS is less than the amount of charge that is recombined after a strike on the center of the drain of an NMOS transistor, as shown in Figures 33a and 33b.

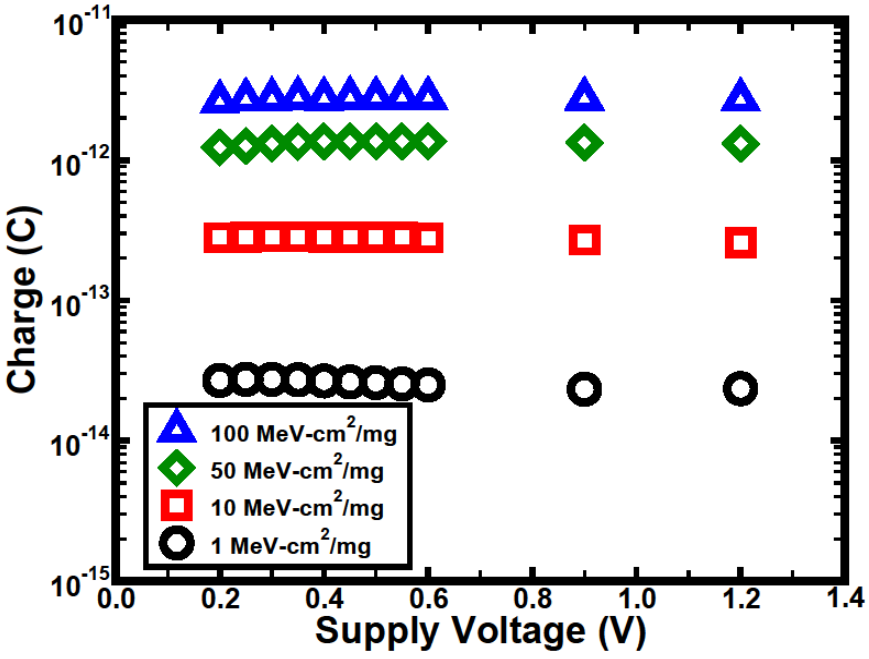
The NMOS transistor shows little increase in the amount of charge that is recombined, but the PMOS transistor shows a considerable increase in the amount of charge collected as the supply voltage decreases. The increase seen in recombined charge as the power supply voltage is reduced is due to the associated decrease in electric field along the channel and the decrease in transistor drive current. Because the electric field is smaller, the charge takes greater time to be collected at the contacts, which in turn allows for more charge to be recombined.

Finally, the substrate contact on the PMOS transistor collects less charge as the supply voltage decreases (Figure 34). The sum of the charge collected at each contact and the charge recombined for each supply voltage sums to the total amount of charge deposited.

The simulation results also show that for a given power supply voltage, at power supply voltages below 400 mV, the generated SET pulsewidths are nearly independent of LET, particularly in the PMOS transistors. This LET independence has not previously been observed in standard combinational logic circuits. For ion strikes on transistors operating at ultra-low supply voltages, the electric fields within the device are extremely small. As discussed above, these small electric fields result is smaller drift currents, and therefore, charge moves more slowly from the ion track to the contacts to be collected




(a)




(b)

Figure 33. The charge that is recombined after a strike on (a) a PMOS and (b) an NMOS transistor calibrated to the IBM 130 nm CMRF8SF process, as simulated in 3D TCAD as a function of power supply voltages and for a variety of ion LETs. The NMOS transistor sees little change with supply voltage, but strikes on the PMOS transistor show more charge is recombined at the lower supply voltages than the higher.

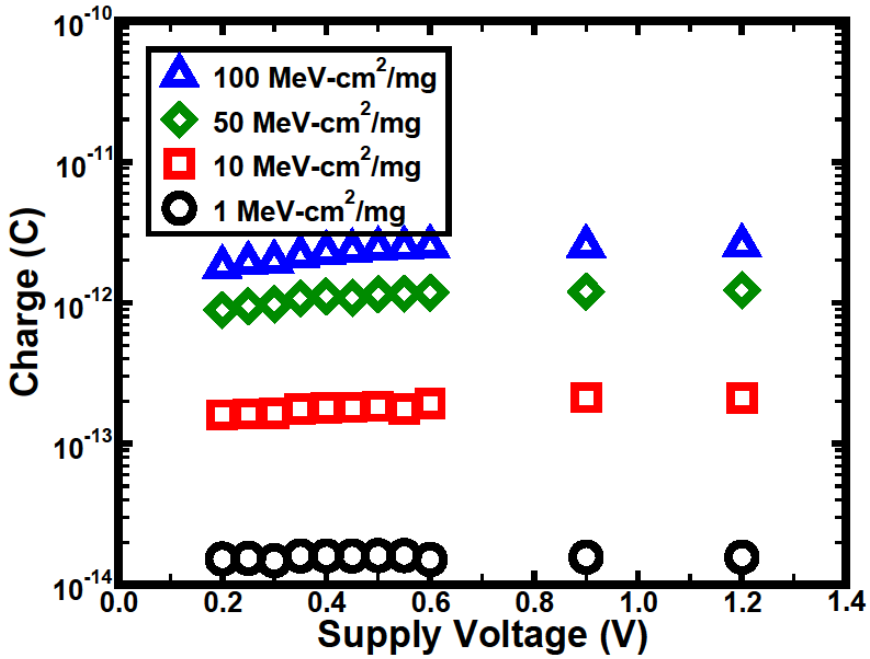



Figure 34. The charge collected at the substrate contact after a strike on a PMOS transistor calibrated to the IBM 130 nm CMRF8SF process, as simulated in 3D TCAD as a function of power supply voltages and for a variety of ion LETs. As the supply voltage is lowered, the amount of charge collected at the substrate contact decreases.

then when high electric fields exist under the transistor gate. This slower charge movement results in less charge collection at the drain and increases the time charge is located in the substrate, which allows for more to be recombined than when operated at the nominal power supply voltage. While the amount of charge collected by diffusion is low, the amount of charge needed for an upset is also low, resulting in SET pulsewidths strongly influenced by diffusion. As diffusion time constants are unaffected by LET particles, SET pulsewidths will be similar for most LET particles.

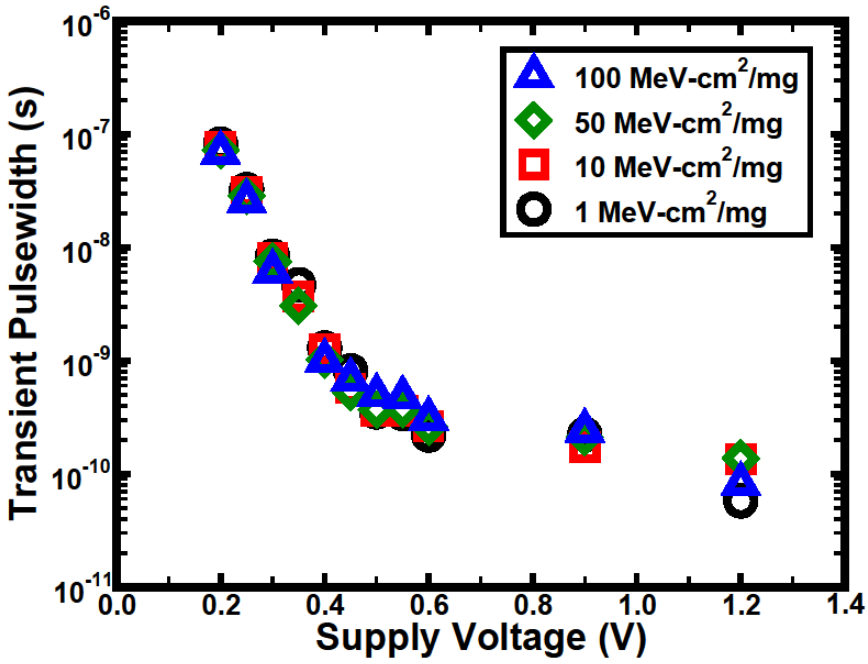
*Multiple 3D TCAD Transistor Simulations*

When multiple transistors are modeled in a single 3D TCAD device, the effects of charge collection at multiple circuit nodes (charge sharing) can be seen. When ions with large LETs strike a transistor and there is another transistor in proximity, a race condition

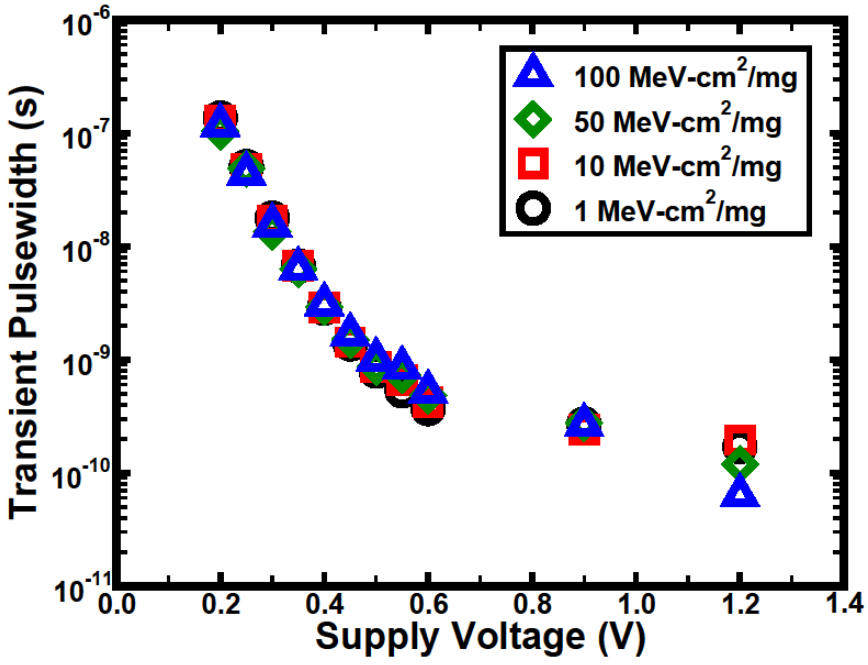
can exist that results in a phenomenon called pulse quenching [Ahl09]. A transient is created at the output node of the struck inverter and that transient propagates to the next inverter. However, because a transistor in the second inverter is also modeled in TCAD, simultaneously there is a second transient that is generated due to charge collection at the second inverter in the chain. This race condition can actually result in shorter single-event transient pulsewidths with larger ion LETs than with smaller LETs. Additionally, as the power supply voltage decreases, the reduced drive currents and electric field make pulse quenching more likely because the initial, electrical transient will last for a longer amount of time, which increases the amount of time for charge to collect on the second transistor. The charge on the second transistor generates its own charge-collection-based voltage transient and effectively negates the propagated electrical transient.

Figure 35 shows the transient pulsewidths as a function of power supply voltage for a variety of ion LETs as measured at the output of a string of five inverters when (a) two PMOS and (b) two NMOS transistors are modeled using 3D TCAD. When two NMOS transistors are modeled in TCAD, there is even less of a dependence on LET in the transient pulsewidth than when a single transistor is modeled. This decrease in SET pulsewidth indicates the presence of charge sharing, and therefore pulse quenching is observed. The PMOS simulations show decreased transient pulsewidths at all supply voltages for two transistors, as compared to the single PMOS TCAD transistor, but the effect is most dramatic at the nominal supply voltage of 1.2 V.

Overall, the PMOS trends are remarkably similar to the single transistor simulations, with a notable difference at 1.2 V, meaning that charge sharing has little effect at lower supply voltages. At the nominal voltage, the effects of charge sharing and pulse




(a)




(b)

Figure 35. Simulated 3D TCAD (calibrated to the IBM 130 nm CMRF8SF process) full-width at half-rail single-event transient pulsewidths generated by strikes on (a) a PMOS transistor and (b) an NMOS transistor as a function of power supply voltages and for a variety of ion LETs when two transistors are modeled in each TCAD structure. Charge sharing reduces the transient pulsewidths at all supply voltages, but pulse quenching is most noticeable at the nominal supply voltages and in the NMOS simulations.

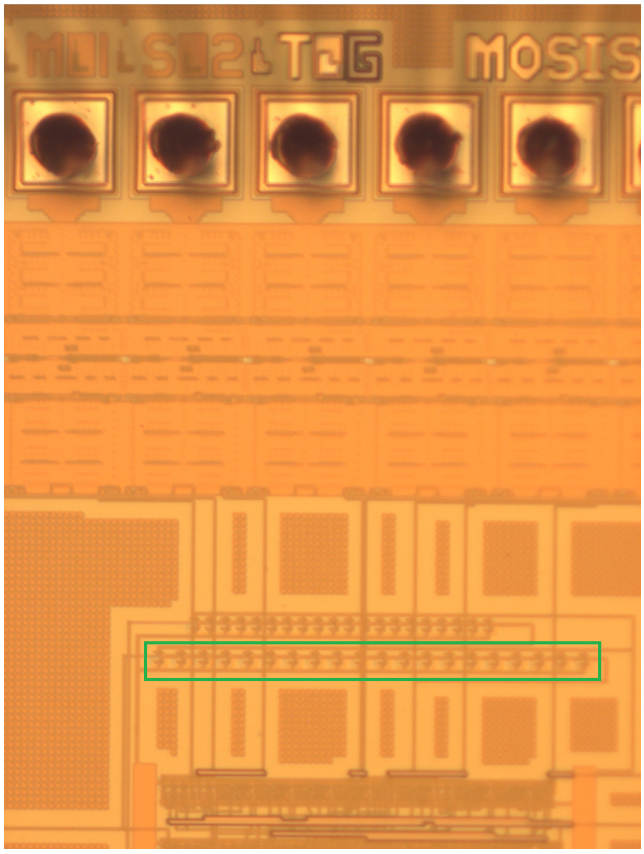
quenching are the most prominent in both the NMOS and PMOS transistor simulations, such that the single-event transients that result from the 50 and 100 MeV-cm$^2$/mg ions actually have a *shorter* pulsewidths than the 1 and 10 MeV-cm$^2$/mg ions. Overall, the single-event transient pulsewidths are narrower for all supply voltages when charge sharing is considered, and the transients show greater independence with LET in the NMOS transistor strikes.

## Experimental Set-up

While TCAD simulations are useful tools in understanding a variety of transistor and circuit mechanisms, experimental data is always necessary for validation. In order to truly understand the effects of supply voltage on single-event transient pulsewidths, a string of 20 inverters fabricated in the AMI 0.5 μm process through the MOSIS foundry [MOSIS] was irradiated at the Naval Research Laboratory using the single-photon, topside laser. Because this is an older process and interference from metal layers is not an issue, the topside laser is used, and therefore, charge is deposited directly on the transistor of interest from the top, instead of through the substrate as required with the high-density processes. With this laser technique, the laser spot is still roughly 1 μm in diameter, and the amount of charge generated is linearly proportional to the laser pulse energy.

Using an older process has other benefits for measuring transients. At the nominal supply voltage, the inverter stage delay is roughly 330 ns, which means that transients will be sufficiently large to measure with a 1 GHz oscilloscope. Also, because the feature sizes and transistor spacings are so large, the laser spot can be focused on a single transistor in order to distinguish between strikes NMOS and PMOS transistors.

A die photo of the parts that were tested can be seen in Figure 36, as well as a view of the individual inverter string alone. The charge was deposited by the laser on the last inverter in the string (the inverter closest to the output and the right most in Figure 36b), and the resulting transients were measured directly using an oscilloscope. For this process, the nominal power supply voltage is 5 V and the threshold voltages of the PMOS and NMOS transistors are 900 mV and 800 mV, respectively. The power supply voltage




(a)

(b)

Figure 36. (a) Die photo of the 20 stage inverter chain. The green box indicates the inverter string that was tested. (b) Zoomed in view of the 20 stage inverter string. The right most inverter was struck by the laser and transients were directly measured with an oscilloscope.

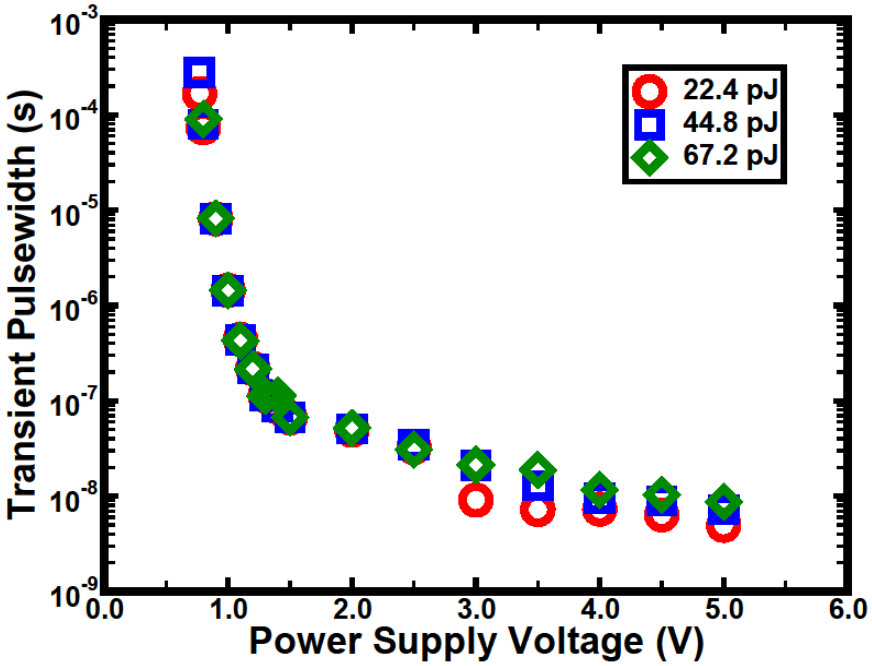
was varied from the nominal, down to 1.5 V at 500 mV intervals, and from 1.5 V to 800 mV at 100 mV intervals, and then an additional voltage of 770 mV was also tested. 2500 transients were captured for each power supply voltage and for each laser pulse energy. The large number of transients was necessary in order to eliminate uncertainty in the laser pulse energy. Because the laser will have some jitter, it is impossible to know exactly the laser pulse energy for any given transient, but by recording a very large number of transients and averaging their peak pulse energies and the resulting transients, the error bars for each data point will be small.

## Experimental Results

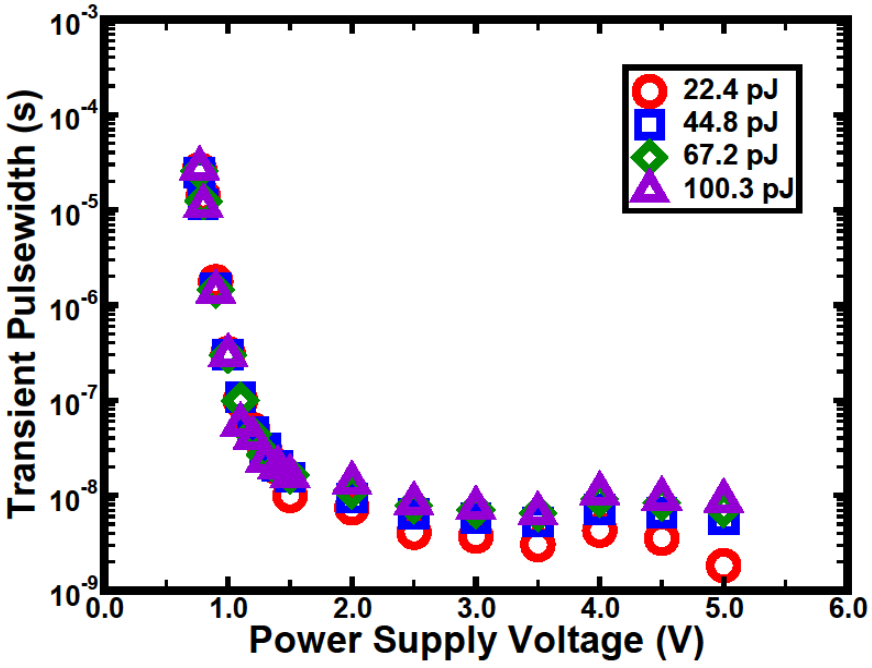
Figures 37a and 37b show the average transient pulsewidth versus power supply voltage across a range of laser pulse energies. In Appendices D and E, examples of the single-event transients can be found for each power supply voltage generated by the laser when the pulse energy was 67.2 pJ. Appendix F contains tables with the average, minimum, and maximum transient pulsewidth measured, and the standard deviation, for each set of experiments. The standard deviations, when plotted in Figures 37 and 38 as the error bars for the average transient pulsewidth, are within the symbols and, therefore, are excluded for simplicity.

As with the ion LETs in the 3D TCAD simulations, there is distinct laser pulse energy dependence at the higher supply voltages, but as the power supply voltage decreases, the single-event transient pulsewidths become independent of laser pulse energy. The transients generated on PMOS transistors are consistently wider than transients generated on NMOS transistors for all laser pulse energies, as would be expected due to parasitic

bipolar amplification (Figures 38a-c.) The power supply voltage was always higher than one diode drop (roughly 700 mV), so the voltage differential between the source and drain of the PMOS transistor also was large enough that the parasitic bipolar would be turned on. The voltage could not be lower than 770 mV because the slowest rate of repetition for the laser was 1 kHz. With supply voltages lower than 770 mV, the resulting transients were longer than the time period between laser strikes, so data could not be gathered at those voltages for this process.

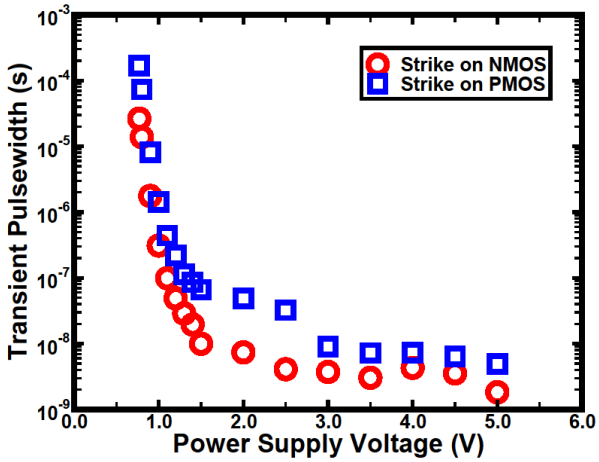



(a)

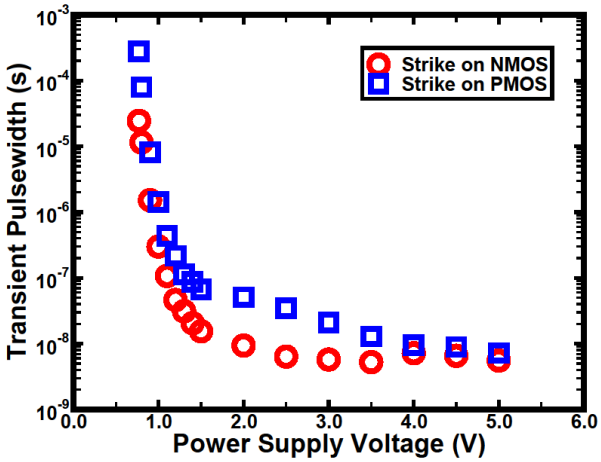



(b)

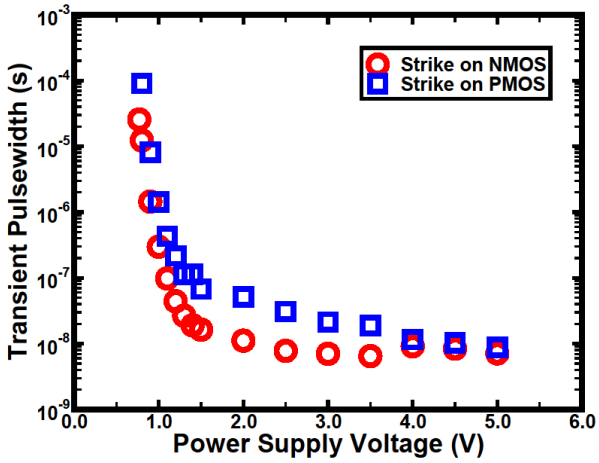
Figure 37. The single-event transient pulsewidths that result after charge is deposited by a laser on a single transistor in a 20 stage inverter chain fabricated in the AMI 0.5 μm process through the MOSIS foundry. Transients generated on (a) a PMOS transistor are consistently longer than transients generated on (b) an NMOS transistor, as is expected due to parasitic bipolar amplification. Additionally, as the supply voltage nears the threshold voltage, the pulsewidths become independent of laser pulse energy.




(a)




(b)




(c)

Figure 38. The transients that result on NMOS (red circles) and PMOS (blue squares) transistors after charge is deposited by a laser with pulse energy of (a) 22.4 pJ, (b) 44.8 pJ, and (c) 67.2 pJ. The transients generated on PMOS transistors are consistently longer than transients generated on NMOS transistors.

# CHAPTER VI

# CONCLUSION

With decreasing feature sizes, transistors are being added to ICs in consistently greater numbers, leading to dramatic increases in power consumption. Changing process parameters and redesigning circuits are complicated and expensive solutions to lower power dissipation. A simple and cost effective approach is to operate standard cell libraries at ultra-low power supply voltages. By lowering the supply voltage, the transistor current drives are decreased by orders of magnitude, resulting in dramatically lower power consumption. However, small transistor drive currents also result in slow operating frequencies, so a trade-off must be made between power and performance.

In this dissertation, the single-event effects of circuits, operated at voltages well below the nominal supply voltage, are investigated. The use of ring oscillators as a single-event test structure is introduced for the first time. Additionally, the effect of supply voltage on single-event transient is seen both in TCAD simulation and experimentally through the use of single-photon, topside laser irradiations.

Ring oscillators provide a convenient vehicle for single-event characterization of technologies by finding the minimum energy at which harmonic oscillation occurs. By finding the minimum laser pulse energy at which the ring oscillator enters a state of sustained harmonic oscillation for a range of power supply voltages, the behavior of the single-event susceptibility as a function of charge deposited by an ionizing event for a technology can be described. Experimental two-photon, backside laser irradiation results show that circuit operation at ultra-low power is more susceptible to single-events than

when operated at the nominal supply voltages, because the threshold laser pulse energy is the lowest in this region.

3D TCAD simulations show that transients created by ion strikes on a device operating in the subthreshold region have longer pulsewidths than those from a device operating at nominal voltages due to the decreased currents of the pull-up and pull-down devices connected to the struck nodes. Additionally, when the devices are operated at ultra-low voltages, the single-event transient pulsewidths generated from strikes on PMOS transistors are smaller than those generated from strikes on NMOS transistors. Normally, at the nominal supply voltage, the opposite is true, but when operating at ultra-low voltages, parasitic bipolar amplification does not occur. When two transistors were modeled in TCAD, the pulsewidths for both NMOS and PMOS transistor strikes decreased for every power supply voltage. The decrease in pulsewidths is due to a phenomenon known as pulse quenching, which is a product of charge sharing.

3D TCAD simulations also show that as the power supply voltage decreases, the amount of charge collected at the drain of the struck transistor also decreases. From the nominal supply voltage to the lowest simulated, the amount of charge collected decreased by more than two orders of magnitude. At the same time, the charge collected at the source of the struck transistor increases.

The increase in pulsewidths as a function of power supply voltage also is shown experimentally. Also seen in experiments is the independence of pulsewidth on laser pulse energy. At voltages outside of the ultra-low power region, the standard, expected response of increasing single-event transient pulsewidth with increasing laser energy is seen. These trends were seen after strikes on both NMOS and PMOS transistors.

In this dissertation, it has been shown both experimentally and through simulation that ultra-low power circuits can be used in radiation environments. Because the operating frequency decreases with power supply voltage at a much higher rate than the single-event transient pulsewidth increases, the soft error rate actually decreases. Therefore, with careful consideration of power supply voltage, ultra-low power circuits can be a viable solution to lowering power consumption in circuits destined for used in space and military applications.

# APPENDIX A

## NMOS DEVISE COMMAND FILE

```
(isegeo:set-default-boolean "ABA")
(isegeo:create-cuboid (position -10 10 5)       (position 10 -10 0)       "Silicon" "R.Bulk")
(isegeo:create-cuboid (position -0.595 0.13 0)          (position    -0.475    -0.13    -0.0025)
"SiO2"    "R.GateOxideA")
(isegeo:create-cuboid  (position  -0.595  0.13  -0.0025)  (position  -0.475  -0.13  -0.1425)
"PolySi"  "R.PolyGateA")

;Field oxide extensions
(isegeo:create-cuboid (position -0.595 0.13 -0.0) (position -0.475 0.36 -0.025) "SiO2"
"R.FieldOxideA1")
(isegeo:create-cuboid (position -0.595 -0.13 -0.0) (position -0.475 -0.36 -0.025) "SiO2"
"R.FieldOxideA2")

;Gate poly extensions
(isegeo:create-cuboid  (position  -0.595  0.13  -0.025)  (position  -0.475  0.36  -0.1425)
"PolySi" "R.PolyGateA1")
(isegeo:create-cuboid  (position  -0.595  -0.13  -0.025)  (position  -0.475  -0.36  -0.1425)
"PolySi" "R.PolyGateA2")

(isegeo:create-cuboid (position -10 0.13 0)   (position    -0.98    -0.13    0.36)       "SiO2"
"R.STI1")
(isegeo:create-cuboid (position 10 0.13 0)    (position    0.09    -0.13    0.36)        "SiO2"
"R.STI2")
(isegeo:create-cuboid (position  -10 0.89 0)  (position 10 0.13 0.36)   "SiO2" "R.STI3")
(isegeo:create-cuboid (position -10 1.17 0)   (position 10 10 0.36)     "SiO2" "R.STI4")
(isegeo:create-cuboid (position -0.09 0.13 0)          (position  0.0  -0.13  0.36)      "SiO2"
"R.STI5")
(isegeo:create-cuboid (position 0.09 0.13 0)  (position 0.0 -0.13 0.36)   "SiO2" "R.STI6")
(isegeo:create-cuboid (position -10 -0.13 0)  (position 0 -10 0.36)     "SiO2" "R.STI7")
(isegeo:create-cuboid (position 10 -0.13 0)   (position 0 -10 0.36)     "SiO2" "R.STI8")
(isegeo:create-cuboid (position -10 0.89 0)   (position -2.3  1.17 0.36) "SiO2" "R.STI9")
(isegeo:create-cuboid (position 10 0.89 0)    (position 2.3 1.17 0.36) "SiO2" "R.STI10")

;;contacts
(isegeo:define-contact-set "DrainA"    4.0  (color:rgb 1.0 0.0 0.0 ) "##")
(isegeo:define-contact-set "GateA"     4.0  (color:rgb 0.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "SourceA"   4.0  (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "Pwell"     4.0  (color:rgb 0.0 1.0 1.0 ) "##")
```

```
(isegeo:create-cuboid (position -0.595 0.13 -0.1425) (position -0.475 -0.13 -2) "Metal" "GateAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.535 0 -0.1425)) "GateA")
(isegeo:delete-region (find-body-id (position -0.535 0 -1)))

(isegeo:create-cuboid (position -2 1.12 0) (position 2 0.94 -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position 0 1.03 0)) "Pwell")
(isegeo:delete-region (find-body-id (position 0 1.03 -1)))

(isegeo:create-cuboid (position -0.8875 0.1 0) (position -0.6875 -0.1 -2) "Metal" "SourceAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.7875 0 0)) "SourceA")
(isegeo:delete-region (find-body-id (position -0.7875 0 -1)))

(isegeo:create-cuboid (position -0.3825 0.1 0) (position -0.1825 -0.1 -2) "Metal" "DrainAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.2825 0 0)) "DrainA")
(isegeo:delete-region (find-body-id (position -0.2825 0 -1)))

;Constant Doping in the poly
(isedr:define-constant-profile "Profile.Polyconst.Phos" "ArsenicActiveConcentration" 1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1" "Profile.Polyconst.Phos" "PolySi")

;-- Constant Doping in the silicon substrate region
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid" (position -10 10 0) (position 10 -10 5))
(isedr:define-constant-profile "Profile.Silconst.Bor" "BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor" "Profile.Silconst.Bor" "Window.Silconst.Bor")

;-- Boron doping in the silicon
;--   Assumes deep pwell implant goes through whole die
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle" (position -10 10 1.25) (position 10 -10 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1" "Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace" "Eval")

(isedr:define-refinement-window "Window.PWell.Bor.2" "Rectangle" (position -10 10 0.65) (position 10 -10 0.65))
```

```
(isedr:define-gaussian-profile "Profile.PWell.Bor.2" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth" 1e17 "Depth" 0.35 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.2" "Profile.PWell.Bor.2" "Window.PWell.Bor.2" "Symm" "NoReplace" "Eval")

;pwell contact doping
(isedr:define-refinement-window "Window.PWellCon.Bor.3A" "Rectangle" (position -2.3 1.17 0) (position 2.3 0.89 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3A" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth" 3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3A" "Profile.PWellCon.Bor.3A" "Window.PWellCon.Bor.3A" "Symm" "NoReplace" "Eval")

; STI Implant - Front & Back Extensions (Added 4/06/06)
(isedr:define-refinement-window "Window.FrontA" "Cuboid" (position -0.595 0.13 0) (position -0.475 0.115 0.36))
(isedr:define-refinement-window "Window.BackA" "Cuboid" (position -0.595 -0.13 0) (position -0.475 -0.115 0.36))
(isedr:define-constant-profile "Profile.STIImplant" "BoronActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontA" "Profile.STIImplant" "Window.FrontA")
(isedr:define-constant-profile-placement "Place.Implant.BackA" "Profile.STIImplant" "Window.BackA")

;-- Arsenic doping in the silicon
;  - DRAIN SIDE A
(isedr:define-refinement-window "drain.Profile.RegionA" "Rectangle" (position -0.446 0.13 0) (position -0.09 -0.13 0))
(isedr:define-gaussian-profile "drain.ProfileA" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceA" "drain.ProfileA" "drain.Profile.RegionA" "Symm" "NoReplace" "Eval")

;  - SOURCE SIDE A
(isedr:define-refinement-window "source.Profile.RegionA" "Rectangle" (position -0.624 0.13 0) (position -0.98 -0.13 0))
(isedr:define-gaussian-profile "source.ProfileA" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceA" "source.ProfileA" "source.Profile.RegionA" "Symm" "NoReplace" "Eval")

; LDD - DRAIN SIDE A
(isedr:define-refinement-window "drainldd.Profile.RegionA" "Rectangle" (position -0.496 0.13 0) (position -0.09 -0.13 0))
(isedr:define-gaussian-profile "drainldd.ProfileA" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2.5e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
```

```
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceA" "drainldd.ProfileA" "drainldd.Profile.RegionA" "Symm" "NoReplace" "Eval")

; LDD - SOURCE SIDE A
(isedr:define-refinement-window "sourceldd.Profile.RegionA" "Rectangle" (position -0.574 0.13 0) (position -0.98 -0.13 0))
(isedr:define-gaussian-profile "sourceldd.ProfileA" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2.5e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceA" "sourceldd.ProfileA" "sourceldd.Profile.RegionA" "Symm" "NoReplace" "Eval")

; Vt IMPLANT A
(isedr:define-refinement-window "implant.Profile.RegionA" "Rectangle" (position -0.565 0.13 0.0165) (position -0.505 -0.13 0.0165))
(isedr:define-gaussian-profile "implant.ProfileA" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 6e18 "ValueAtDepth" 1e17 "Depth" 0.0165 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceA" "implant.ProfileA" "implant.Profile.RegionA" "Symm" "NoReplace" "Eval")

;;bulk meshing
; Meshing Strategy:
(isedr:define-refinement-size "size.whole" 1.0 1.0 0.5 0.25 0.25 0.1)
(isedr:define-refinement-window "window.whole" "Cuboid" (position -10 10 0) (position 10 -10 2))
(isedr:define-refinement-placement "placement.whole" "size.whole" "window.whole" )

(isedr:define-refinement-size "size.whole2" 1.5 1.5 1.5 0.75 0.75 0.75)
(isedr:define-refinement-window "window.whole2" "Cuboid" (position -10 10 2) (position 10 -10 5))
(isedr:define-refinement-placement "placement.whole2" "size.whole2" "window.whole2" )

(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.05 0.05 0.05 0.05)
(isedr:define-refinement-function "size.dopingmesha" "DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position -2.3 0.89 0) (position 2.3 1.17 0.1))
(isedr:define-refinement-placement "placement.dopingmesha" "size.dopingmesha" "window.dopingmesha" )

(isedr:define-refinement-size "size.dopingmesh1b" 0.1 0.1 0.05 0.005 0.005 0.005)
(isedr:define-refinement-function "size.dopingmesh1b" "DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesh1b" "Cuboid" (position -0.09 0.13 0) (position -0.98 -0.13 0.1))
```

```
(isedr:define-refinement-placement "placement.dopingmesh1b" "size.dopingmesh1b"
"window.dopingmesh1b" )

(isedr:define-refinement-size "size.dopingmesh2b" 0.075 0.075 0.05 0.005 0.005 0.005)
(isedr:define-refinement-function "size.dopingmesh2b" "DopingConcentration"
"MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesh2b" "Cuboid" (position -0.605
0.13 0) (position -0.465 -0.13 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2b" "size.dopingmesh2b"
"window.dopingmesh2b" )

(isedr:define-refinement-size "size.ionstrike" 0.025 0.025 0.5 0.01 0.01 0.1)
(isedr:define-refinement-window "window.ionstrike" "Cuboid" (position -0.2325 0.05 0)
(position -0.3325 -0.05 5))
(isedr:define-refinement-placement "placement.ionstrike" "size.ionstrike"
"window.ionstrike" )

(ise:save-model "NMOS")
```

APPENDIX B

PMOS DEVISE COMMAND FILE

```
(isegeo:set-default-boolean "ABA")
(isegeo:create-cuboid (position -10 10 5)       (position 10 -10 0)       "Silicon" "R.Bulk")
(isegeo:create-cuboid (position -0.595 0.36 0)          (position    -0.475    -0.36    -0.0025)
"SiO2"    "R.GateOxideA")
(isegeo:create-cuboid (position -0.595 0.36 -0.0025) (position -0.475 -0.36 -0.1425)
"PolySi"  "R.PolyGateA")

;Field oxide extensions
(isegeo:create-cuboid (position -0.595 0.36 -0.0) (position -0.475 0.59 -0.025) "SiO2"
"R.FieldOxideA1")
(isegeo:create-cuboid (position -0.595 -0.36 -0.0) (position -0.475 -0.759 -0.025) "SiO2"
"R.FieldOxideA2")

;Gate poly extensions
(isegeo:create-cuboid (position -0.595 0.36 -0.025) (position -0.475 0.59 -0.1425)
"PolySi" "R.PolyGateA1")
(isegeo:create-cuboid (position -0.595 -0.36 -0.025) (position -0.475 -0.59 -0.1425)
"PolySi" "R.PolyGateA2")

(isegeo:create-cuboid (position -10 0.36 0)   (position    -0.98    -0.36    0.36)       "SiO2"
"R.STI1")
(isegeo:create-cuboid (position 10 0.36 0)    (position    0.09    -0.36    0.36)         "SiO2"
"R.STI2")
(isegeo:create-cuboid (position  -10 0.89 0)  (position 10 0.36 0.36)   "SiO2" "R.STI3")
(isegeo:create-cuboid (position -10 1.17 0)   (position 10 10 0.36)     "SiO2" "R.STI4")
(isegeo:create-cuboid (position -0.09  0.36 0)          (position  0.0  -0.36  0.36)      "SiO2"
"R.STI5")
(isegeo:create-cuboid (position 0.09  0.36 0) (position 0.0 -0.36 0.36)   "SiO2" "R.STI6")
(isegeo:create-cuboid (position -10 -0.36 0)  (position 0 -10 0.36)     "SiO2" "R.STI7")
(isegeo:create-cuboid (position 10 -0.36 0)   (position 0 -10 0.36)     "SiO2" "R.STI8")
(isegeo:create-cuboid (position -10 0.89 0)   (position -2.3  1.17 0.36) "SiO2" "R.STI9")
(isegeo:create-cuboid (position 10 0.89 0)    (position 2.3 1.17 0.36) "SiO2" "R.STI10")

;;contacts
(isegeo:define-contact-set "DrainA"    4.0  (color:rgb 1.0 0.0 0.0 ) "##")
(isegeo:define-contact-set "GateA"     4.0  (color:rgb 0.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "SourceA"   4.0  (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "Substrate" 4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "Nwell"     4.0  (color:rgb 0.0 1.0 1.0 ) "##")
```

```
(isegeo:create-cuboid (position -0.595 0.36 -0.1425) (position -0.475 -0.36 -2) "Metal" "GateAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.535 0 -0.1425)) "GateA")
(isegeo:delete-region (find-body-id (position -0.535 0 -1)))
(isegeo:create-cuboid (position -2 1.12 0) (position 2 0.94 -2) "Metal" "Nwellmetal")
(isegeo:define-3d-contact (find-face-id (position 0 1.03 0)) "Nwell")
(isegeo:delete-region (find-body-id (position 0 1.03 -1)))
(isegeo:define-3d-contact (find-face-id (position 0 0 5))  "Substrate")
(isegeo:create-cuboid (position -0.8875 0.11 0) (position -0.6875 -0.11 -2) "Metal" "SourceAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.7875 0 0)) "SourceA")
(isegeo:delete-region (find-body-id (position -0.7875 0 -1)))
(isegeo:create-cuboid (position -0.3825 0.11 0) (position -0.1825 -0.11 -2) "Metal" "DrainAmetal")
(isegeo:define-3d-contact (find-face-id (position -0.2825 0 0)) "DrainA")
(isegeo:delete-region (find-body-id (position -0.2825 0 -1)))

;------------- Lets add in some dopings for the device ------------------------------------------
;----- First, lets begin with all the constant doping profiles

;Constant Doping in the poly
(isedr:define-constant-profile "Profile.Polyconst.Phos" "BoronActiveConcentration" 1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1" "Profile.Polyconst.Phos" "PolySi")

;-- Constant Doping in the silicon substrate region
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid" (position -10 10 0) (position 10 -10 5))
(isedr:define-constant-profile "Profile.Silconst.Bor" "BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor" "Profile.Silconst.Bor" "Window.Silconst.Bor")

;-- Boron doping in the silicon
;--  Assumes deep pwell implant goes through whole die
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle" (position -10 10 1.25) (position 10 -10 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1" "Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace" "Eval")

(isedr:define-refinement-window "Window.NWell.Bor.2" "Rectangle" (position -10 10 0.45) (position 10 -10 0.45))
```

```
(isedr:define-gaussian-profile "Profile.NWell.Bor.2" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 1e17 "ValueAtDepth" 1e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWell.Bor.2" "Profile.NWell.Bor.2" "Window.NWell.Bor.2" "Symm" "NoReplace" "Eval")

;nwell contact doping
(isedr:define-refinement-window "Window.NWellCon.Bor.3A" "Rectangle" (position -2.3 1.17 0) (position 2.3 0.89 0))
(isedr:define-gaussian-profile "Profile.NWellCon.Bor.3A" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth" 3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWellCon.Bor.3A" "Profile.NWellCon.Bor.3A" "Window.NWellCon.Bor.3A" "Symm" "NoReplace" "Eval")

; STI Implant - Front & Back Extensions (Added 4/06/06)
(isedr:define-refinement-window "Window.FrontA" "Cuboid" (position -0.595  0.36 0) (position -0.475 0.345 0.36))
(isedr:define-refinement-window "Window.BackA" "Cuboid" (position -0.595 -0.36 0) (position -0.475 -0.345 0.36))

(isedr:define-constant-profile "Profile.ImplantA" "ArsenicActiveConcentration" 5e19)
(isedr:define-constant-profile-placement "Place.Implant.FrontA" "Profile.ImplantA" "Window.FrontA")
(isedr:define-constant-profile-placement "Place.Implant.BackA" "Profile.ImplantA" "Window.BackA")

;-- Boron doping in the silicon
;  - DRAIN SIDE A
(isedr:define-refinement-window "drain.Profile.RegionA" "Rectangle" (position -0.446 0.36 0) (position -0.09 -0.36 0))
(isedr:define-gaussian-profile "drain.ProfileA" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceA" "drain.ProfileA" "drain.Profile.RegionA" "Symm" "NoReplace" "Eval")

;  - SOURCE SIDE A
(isedr:define-refinement-window "source.Profile.RegionA" "Rectangle" (position -0.624 0.36 0) (position -0.98 -0.36 0))
(isedr:define-gaussian-profile "source.ProfileA" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceA" "source.ProfileA" "source.Profile.RegionA" "Symm" "NoReplace" "Eval")

; LDD - DRAIN SIDE A
(isedr:define-refinement-window "drainldd.Profile.RegionA" "Rectangle" (position -0.496 0.36 0) (position -0.09 -0.36 0))
```

```
(isedr:define-gaussian-profile "drainldd.ProfileA" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 2.15e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceA" "drainldd.ProfileA" "drainldd.Profile.RegionA" "Symm" "NoReplace" "Eval")

; LDD - SOURCE SIDE A
(isedr:define-refinement-window "sourceldd.Profile.RegionA" "Rectangle" (position -0.574 0.36 0) (position -0.98 -0.36 0))
(isedr:define-gaussian-profile "sourceldd.ProfileA" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 2.15e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceA" "sourceldd.ProfileA" "sourceldd.Profile.RegionA" "Symm" "NoReplace" "Eval")

; Vt IMPLANT A
(isedr:define-refinement-window "implant.Profile.RegionA" "Rectangle" (position -0.565 0.36 0.0165) (position -0.505 -0.36 0.0165))
(isedr:define-gaussian-profile "implant.ProfileA" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 5e18 "ValueAtDepth" 1e17 "Depth" 0.0165 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceA" "implant.ProfileA" "implant.Profile.RegionA" "Symm" "NoReplace" "Eval")

;;bulk meshing
; Meshing Strategy:
(isedr:define-refinement-size "size.whole" 1.0 1.0 0.5 0.25 0.25 0.1)
(isedr:define-refinement-window "window.whole" "Cuboid" (position -10 10 0) (position 10 -10 2))
(isedr:define-refinement-placement "placement.whole" "size.whole" "window.whole" )
(isedr:define-refinement-size "size.whole2" 1.5 1.5 1.5 0.75 0.75 0.75)
(isedr:define-refinement-window "window.whole2" "Cuboid" (position -10 10 2) (position 10 -10 5))
(isedr:define-refinement-placement "placement.whole2" "size.whole2" "window.whole2" )
(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.05 0.05 0.05 0.05)
(isedr:define-refinement-function "size.dopingmesha" "DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position -2.3 0.89 0) (position 2.3 1.17 0.1))
(isedr:define-refinement-placement "placement.dopingmesha" "size.dopingmesha" "window.dopingmesha" )
(isedr:define-refinement-size "size.dopingmesh1a" 0.1 0.1 0.05 0.005 0.005 0.005)
(isedr:define-refinement-function "size.dopingmesh1a" "DopingConcentration" "MaxTransDiff" 1)
```

```
(isedr:define-refinement-window "window.dopingmesh1a" "Cuboid" (position -0.09 0.36
0) (position -0.98 -0.36 0.1))
(isedr:define-refinement-placement "placement.dopingmesh1a" "size.dopingmesh1a"
"window.dopingmesh1a" )
 (isedr:define-refinement-size "size.dopingmesh2a" 0.075 0.075 0.05 0.005 0.005 0.005)
(isedr:define-refinement-function "size.dopingmesh2a" "DopingConcentration"
"MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesh2a" "Cuboid" (position -0.605
0.36 0) (position -0.465 -0.36 0.1))
(isedr:define-refinement-placement "placement.dopingmesh2a" "size.dopingmesh2a"
"window.dopingmesh2a" )
 (isedr:define-refinement-size "size.ionstrike" 0.025 0.025 0.5 0.01 0.01 0.1)
(isedr:define-refinement-window "window.ionstrike" "Cuboid" (position -0.2325 0.05 0)
(position -0.3325 -0.05 5))
(isedr:define-refinement-placement "placement.ionstrike" "size.ionstrike"
"window.ionstrike" )

(ise:save-model "PMOS")
```

APPENDIX C

PMOS MIXED-MODE COMMAND FILE

```
######################################################################

DEVICE PFET1{
File     {
       Grid    = "PMOS_msh.grd"
       Doping  = "PMOS_msh.dat"
       Param   = "dessis.par"
       }

Electrode {
       { Name="DrainA"         Voltage=0.0  }
          { Name="GateA"         Voltage=0.0  }
       { Name="SourceA"        Voltage=0.0  }
          { Name="Nwell"         Voltage=0.0  }
          { Name="Substrate"    Voltage=0.0  }
          }

Physics {
       Recombination(SRH Auger) #TPA_gen
       Mobility(Phumob HighFieldsat Enormal)
       EffectiveIntrinsicDensity( OldSlotboom )
          Fermi
          HeavyIon(
          time=0.6e-9
          length=3
          wt_hi=0.05
          location=(-0.2825,0,0)
          direction=(0,0,1)
          LET_f=0.01
          Gaussian
          Picocoulomb )
          }

Plot     {
       Potential Electricfield
       eDensity hDensity
       eCurrent/Vector hCurrent/Vector
       TotalCurrent/Vector
```

```
        eQuasiFermi hQuasiFermi
        DonorConcentration Acceptorconcentration
        Doping SpaceCharge
        HeavyIonChargeDensity
            }
}

Math    {
            WallClock
            Extrapolate
            Derivatives
            RelErrControl
            Iterations=15
            notdamped=100
            Newdiscretization
            Method=ILS
            RecBoxIntegr
            number_of_threads=2
            }

File    {
            Output = "inv_p200_log"
            SPICEPath = "." ###path where your spice models are ###
            Plot    = "inv_p200_plot.dat"
            Current = "inv_p200_current.plt"
        }

System{
            Vsource_pset  INPUT          (IN    0)          {dc = 0.2}

            Vsource_pset  VDD            (HIGH 0)        {dc   =   0.2}      ###voltage   source
(HIGH 0) are node names###

######## mosfet (drain gate source bulk)  ####################
###This is the TCAD device,I am referencing the device above, and connecting the
electrodes to spice nodes###
            PFET1 device1           ("DrainA"       = OUT1
                                    "GateA"         = IN
                                     "SourceA"      = HIGH
                                     "Substrate"    = 0
                                     "Nwell"        = HIGH)

###These are spice transistors, NMOS13 & PMOS13 are the names from the spice model
file, M0-M39 is the name I give it here (drain gate source bulk) ###
            NMOS13        MN0    (OUT1 IN 0 0)
                                    {w = 260e-9    l = 0.13e-6
```

```
                pd = 1.62e-6    ps = 1.62e-6
                ad = 1.43e-13   as = 1.43e-13}
        NMOS13  MN1    (OUT2 OUT1 0 0)
                {w = 260e-9     l = 0.13e-6
                pd = 1.62e-6    ps = 1.62e-6
                ad = 1.43e-13   as = 1.43e-13}
        NMOS13  MN2    (OUT3 OUT2 0 0)
                {w = 260e-9     l = 0.13e-6
                pd = 1.62e-6    ps = 1.62e-6
                ad = 1.43e-13   as = 1.43e-13}
        NMOS13  MN3    (OUT4 OUT3 0 0)
                {w = 260e-9     l = 0.13e-6
                pd = 1.62e-6    ps = 1.62e-6
                ad = 1.43e-13   as = 1.43e-13}
        NMOS13  MN4    (OUT5 OUT4 0 0)
                {w = 260e-9     l = 0.13e-6
                pd = 1.62e-6    ps = 1.62e-6
                ad = 1.43e-13   as = 1.43e-13}
#       PMOS13  MP0    (OUT1 IN HIGH HIGH)
#               {w = 720e-9     l = 0.13e-6
#               pd = 2.54e-6    ps = 2.54e-6
#               ad = 3.96e-13   as = 3.96e-13}
        PMOS13  MP1    (OUT2 OUT1 HIGH HIGH)
                {w = 720e-9     l = 0.13e-6
                pd = 2.54e-6    ps = 2.54e-6
                ad = 3.96e-13   as = 3.96e-13}
        PMOS13  MP2    (OUT3 OUT2 HIGH HIGH)
                {w = 720e-9     l = 0.13e-6
                pd = 2.54e-6    ps = 2.54e-6
                ad = 3.96e-13   as = 3.96e-13}
        PMOS13  MP3    (OUT4 OUT3 HIGH HIGH)
                {w = 720e-9     l = 0.13e-6
                pd = 2.54e-6    ps = 2.54e-6
                ad = 3.96e-13   as = 3.96e-13}
        PMOS13  MP4    (OUT5 OUT4 HIGH HIGH)
                {w = 720e-9     l = 0.13e-6
                pd = 2.54e-6    ps = 2.54e-6
                ad = 3.96e-13   as = 3.96e-13}

####this is initializes the node outright, look at the manual for more information###
Initialize (OUT1 = 0)
Initialize (OUT2 = 0.2)
Initialize (OUT3 = 0)
Initialize (OUT4 = 0.2)
Initialize (OUT5 = 0)
```

```
###this is for the spice .plt file###
        Plot "inv_p200" (time() v(OUT1) v(OUT2) v(OUT3) v(OUT4) v(OUT5))
         }

Solve{
   Load (FilePrefix="Biased_Device")

NewCurrentFile="transient_"

Transient (
        InitialTime=0
        FinalTime=0.09e-9
        InitialStep=1e-12
        MaxStep=7.5e-11 Increment=1.2)
     {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
     }

Transient (
        InitialTime=0.09e-9
        FinalTime=0.59e-9
        InitialStep=1e-12
        MaxStep=7.5e-11 Increment=1.2)
     {
        coupled {device1.poisson device1.electron device1.hole device1.contact circuit}
           Plot ( FilePrefix="start" Time=(0.51e-9) NoOverwrite )
     }

Transient (
        InitialTime=0.59e-9
        FinalTime=1.0e-9
        InitialStep=1e-12
        MaxStep=2.5e-12 Increment=1.2 )
      {
        coupled{device1.poisson device1.electron device1.hole device1.contact circuit}
        Plot    (    FilePrefix="imA"    Time=(0.59e-9;0.6e-9;0.65e-9;0.7e-9;0.75e-9;0.8e-
9;0.9e-9) NoOverwrite)
      }

Transient (
        InitialTime=1.0e-9
        FinalTime=200.5e-9
        InitialStep=1e-12
        MaxStep=7.5e-11
        Increment=1.2 )
      {
```

```
        coupled{device1.poisson device1.electron device1.hole device1.contact circuit}
        Plot    (FilePrefix="laterA"    Time=(1.0e-9;5.5e-9;10.5e-9;15.5e-9;20.5e-9;25.5e-
9;50.5e-9;100.5e-9;150.5e-9;200.5e-9) NoOverwrite)
}
}
```

APPENDIX D

EXAMPLE TRANSIENTS AS GENERATED ON AN NMOS TRANSISTOR

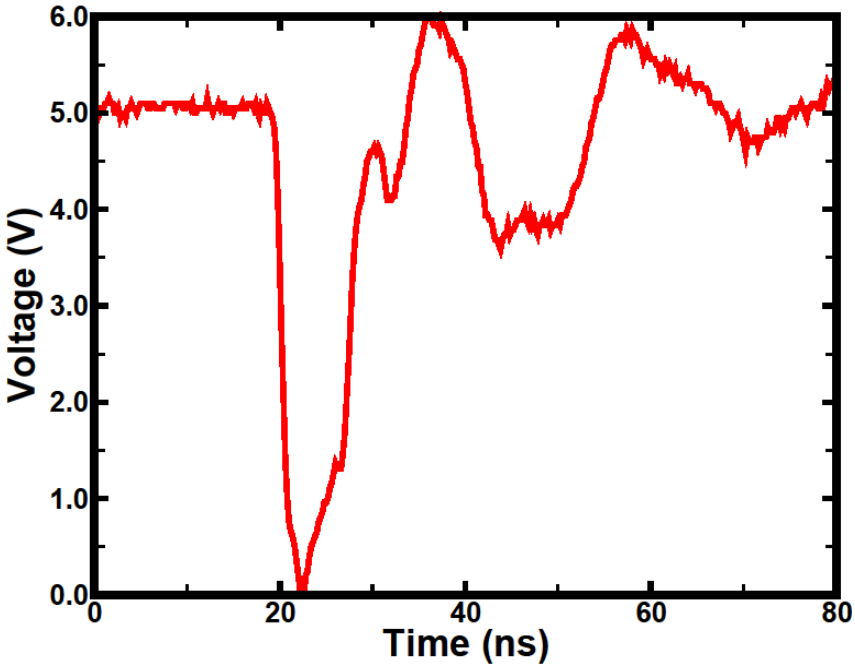



Figure 39. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a twenty inverter chain with a supply voltage of 5 V.

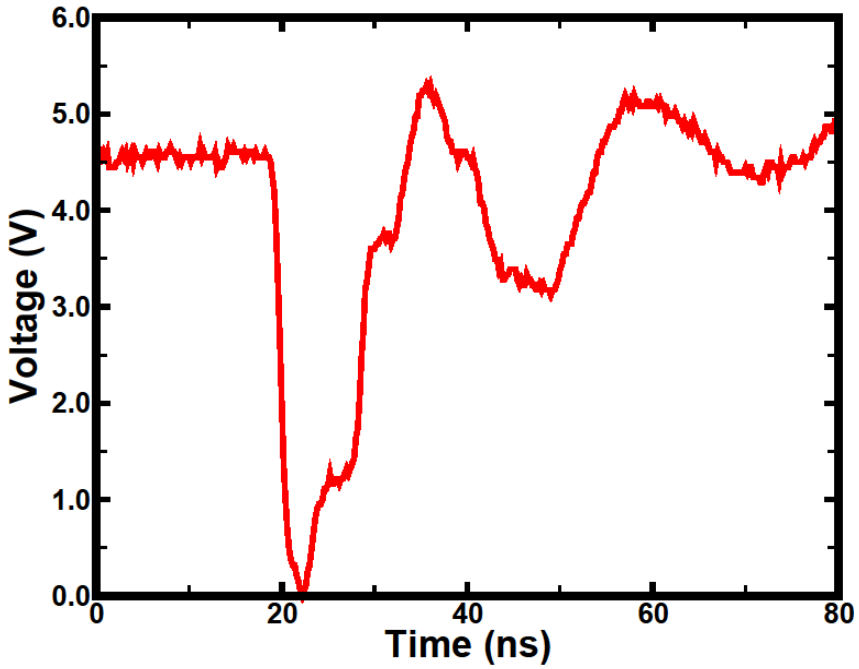



Figure 40. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 4.5 V.

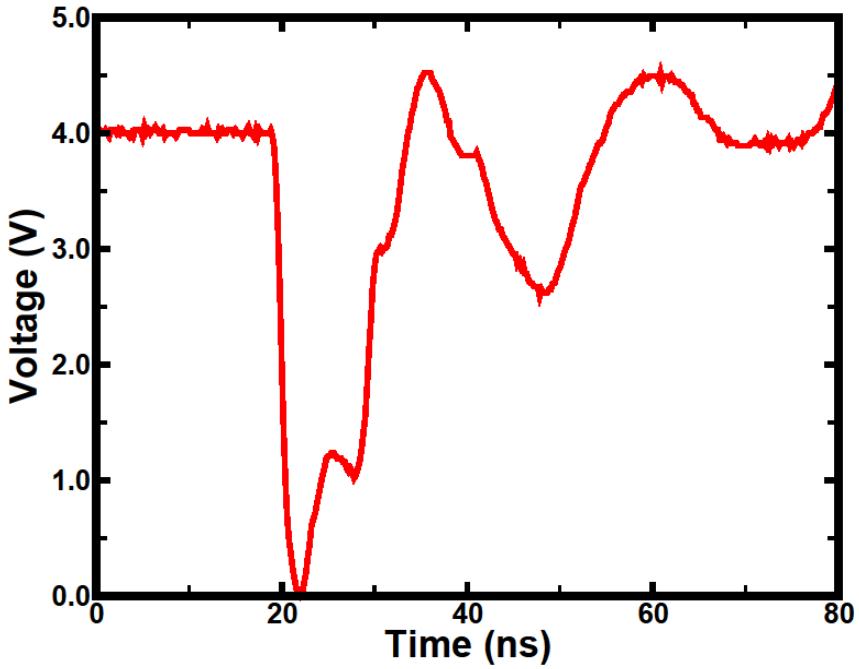



Figure 41. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 4 V.

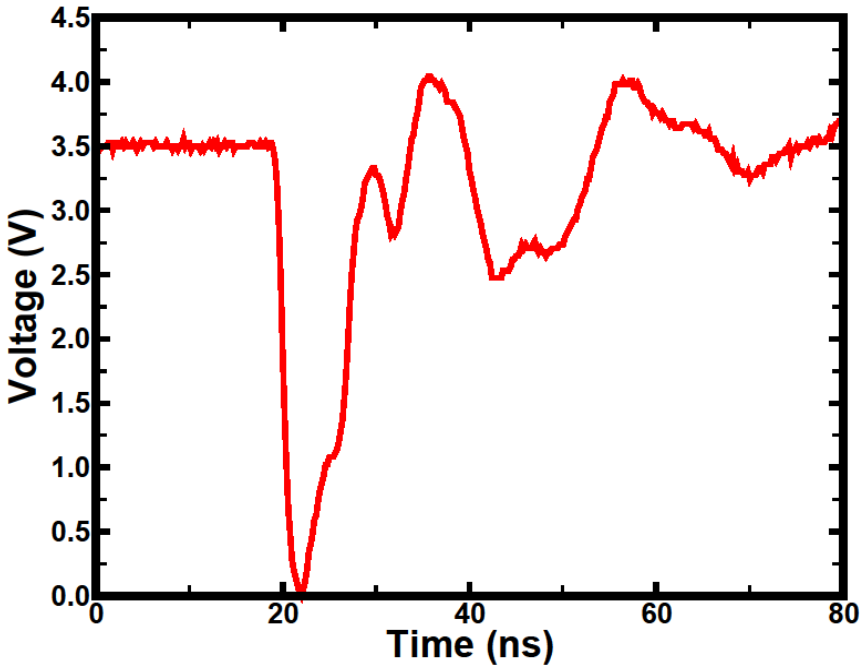



Figure 42. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 3.5 V.

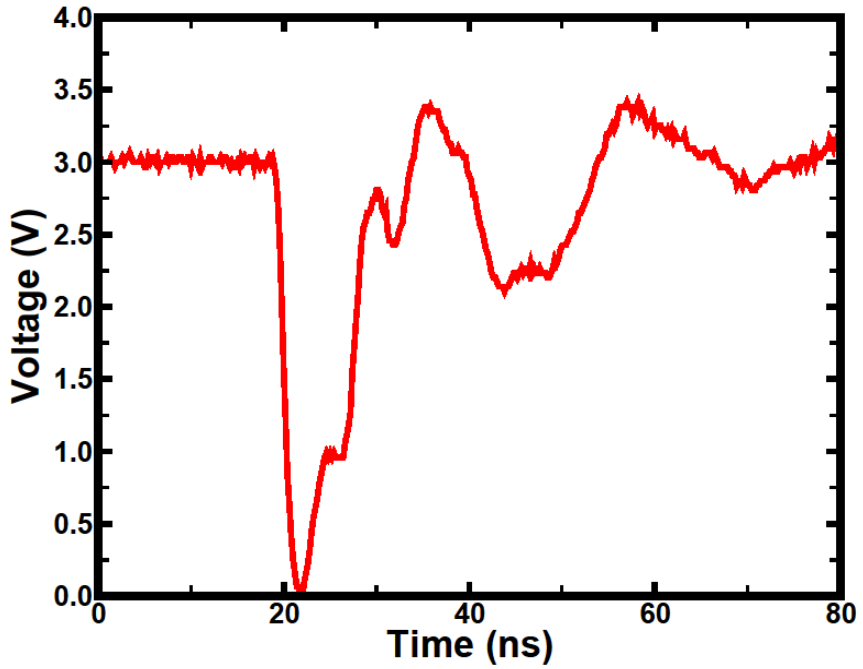



Figure 43. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 3 V.

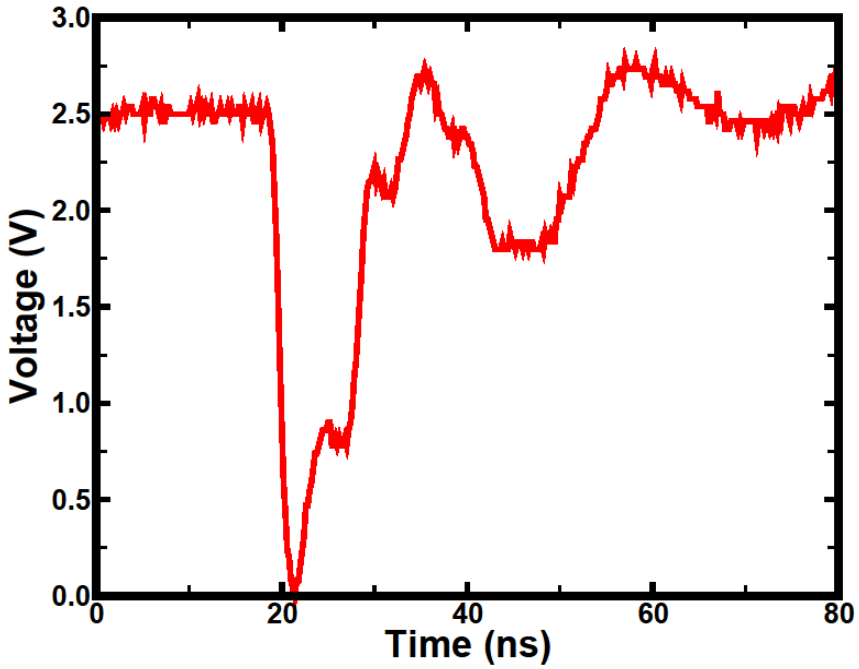



Figure 44. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 2.5 V.

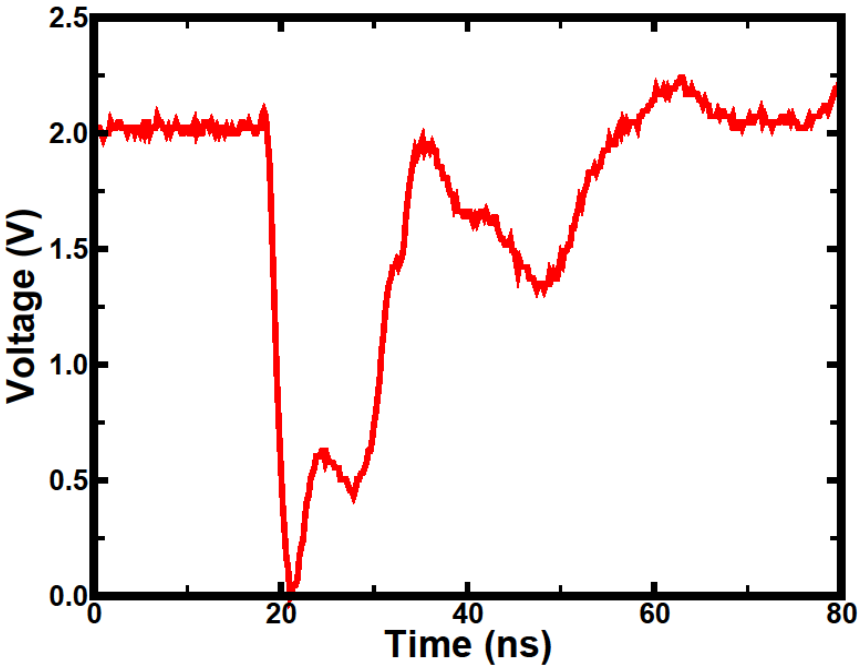



Figure 45. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 2 V.

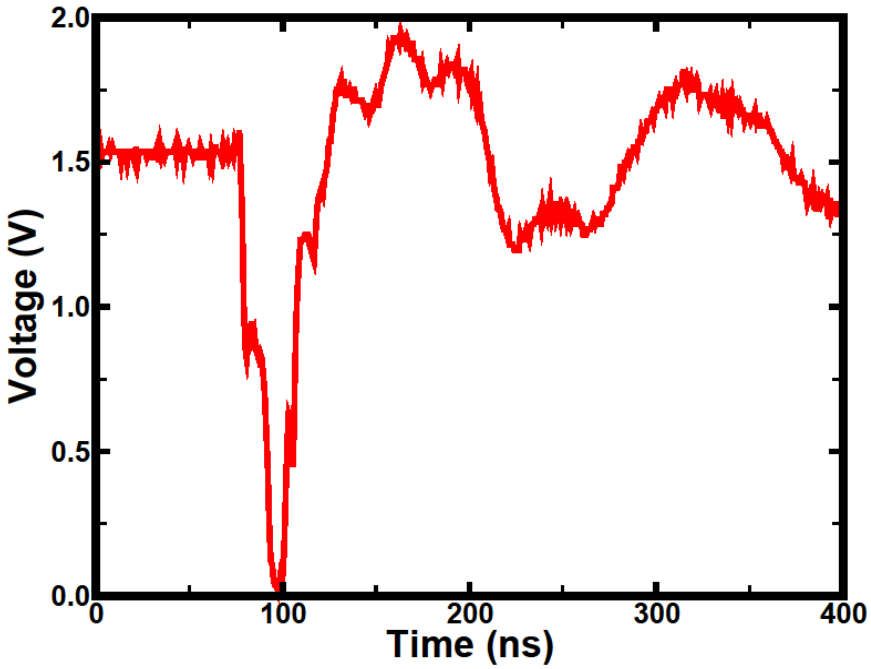



Figure 46. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.5 V.

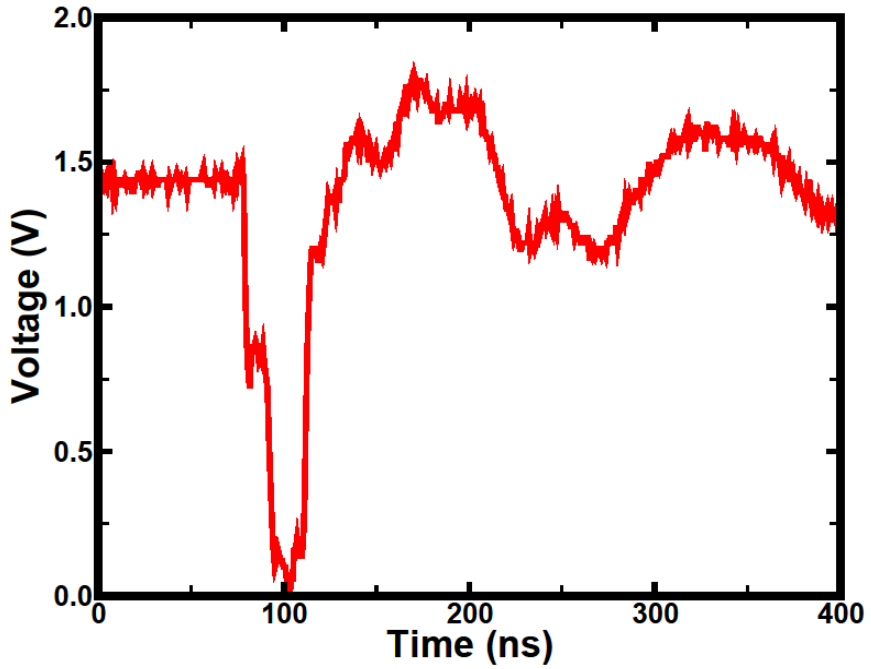



Figure 47. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.4 V.

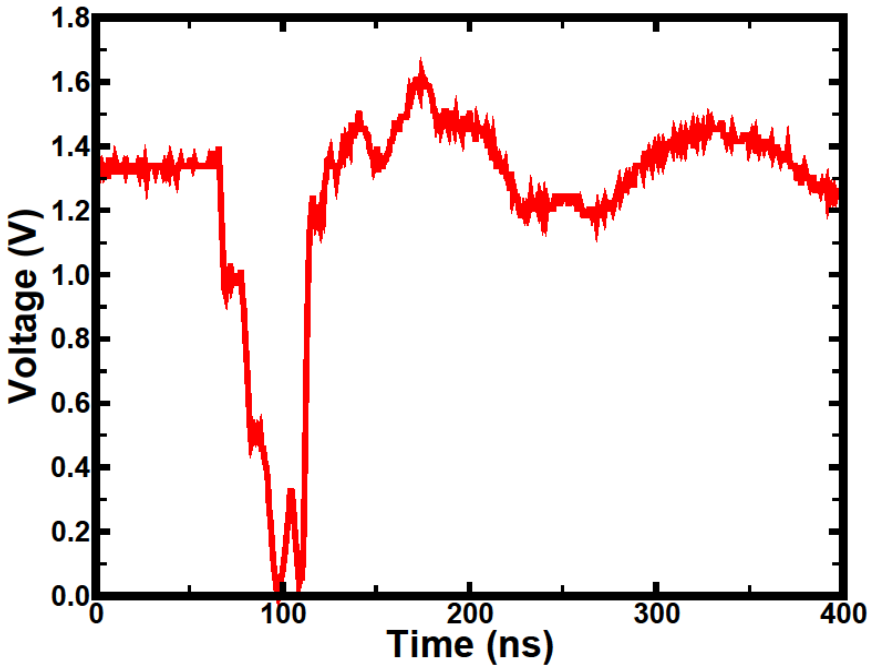



Figure 48. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.3 V.

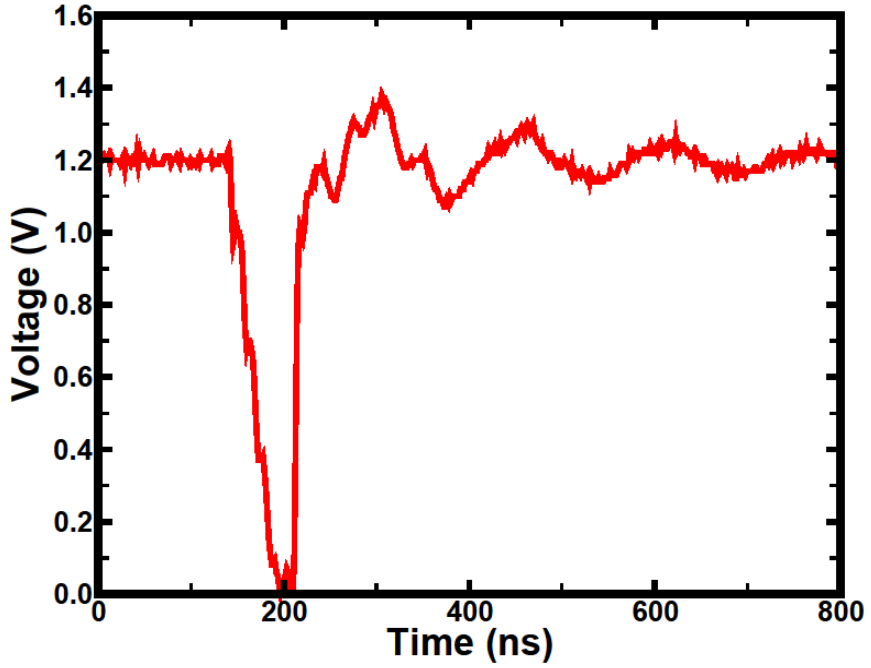



Figure 49. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.2 V.

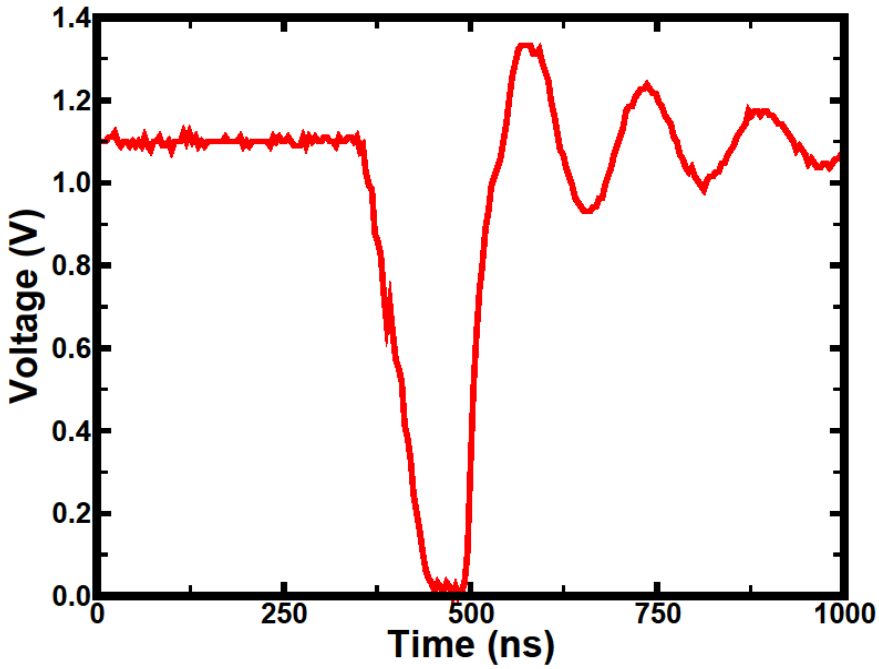



Figure 50. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.1 V.

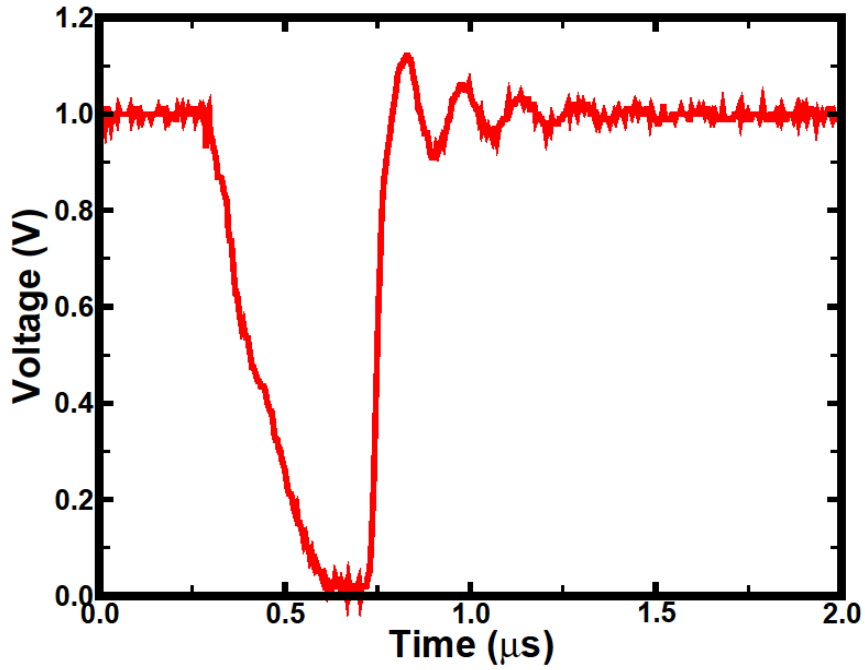



Figure 51. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1 V.

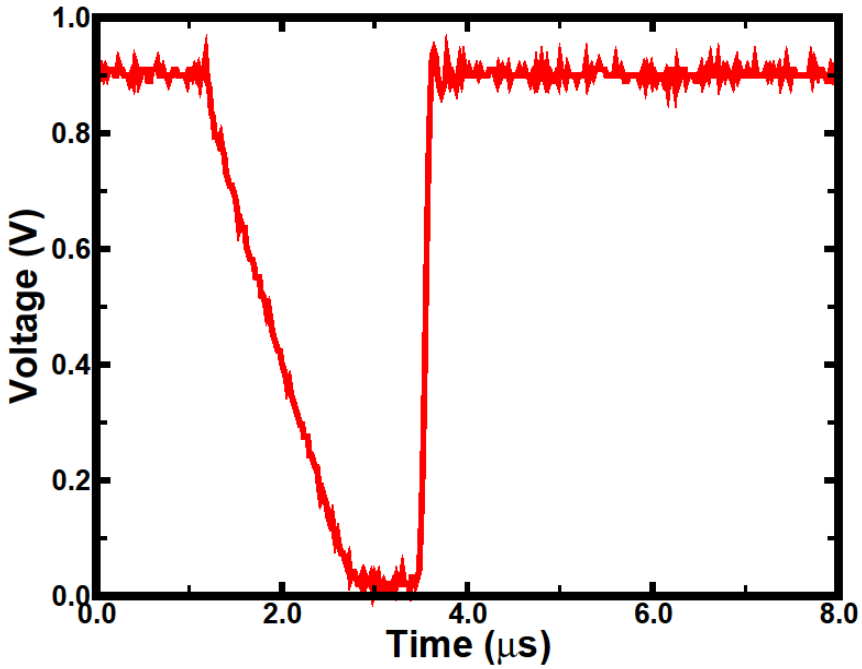



Figure 52. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 0.9 V.

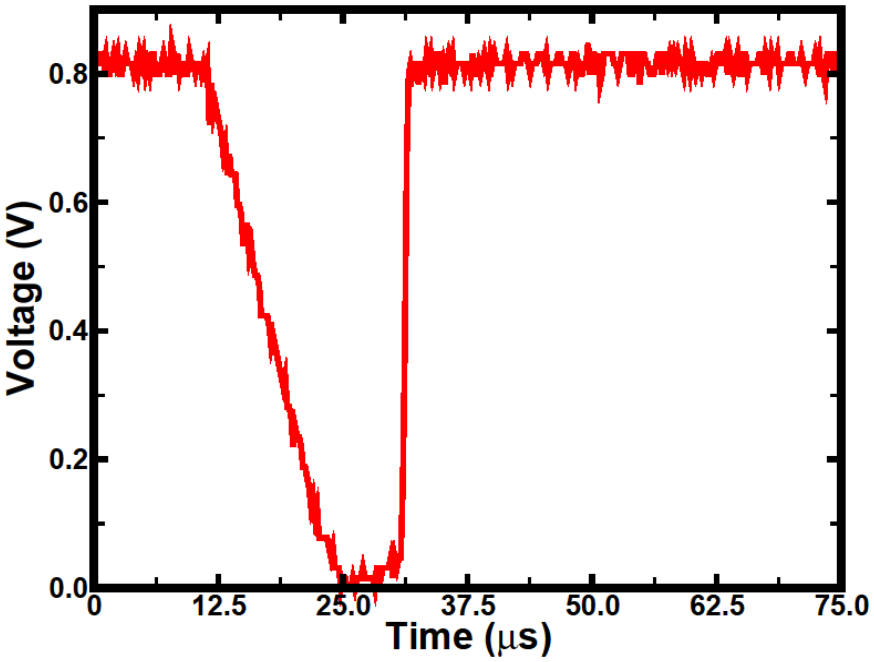



Figure 53. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 0.8 V.

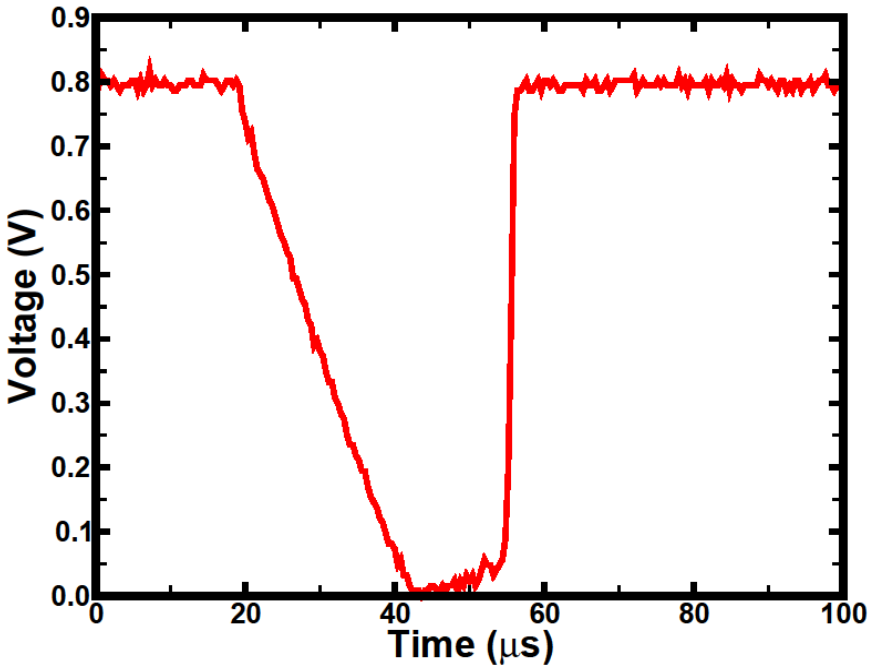



Figure 54. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a NMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 0.77 V.

APPENDIX E

EXAMPLE TRANSIENTS AS GENERATED ON AN PMOS TRANSISTOR

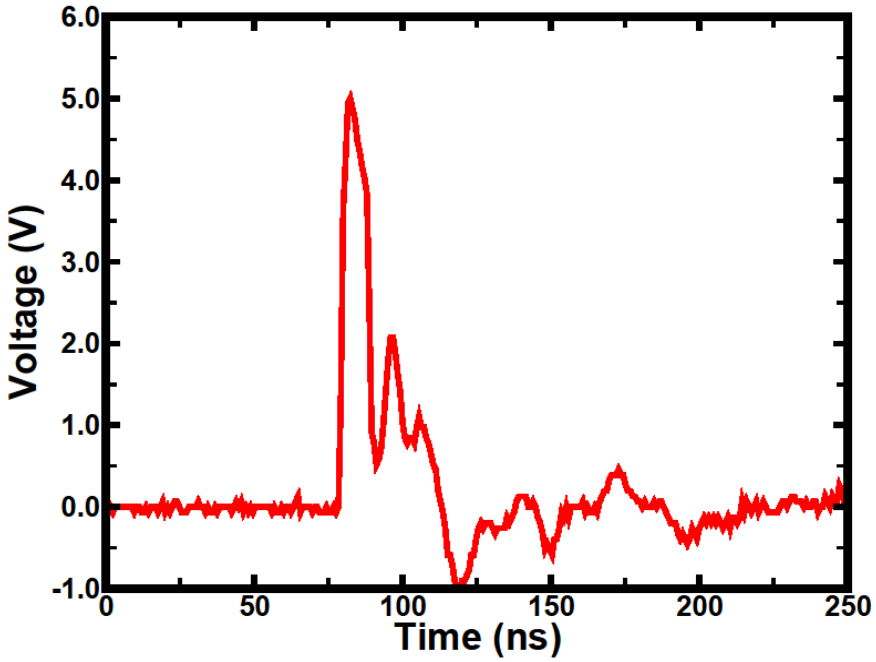



Figure 55. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 5 V.

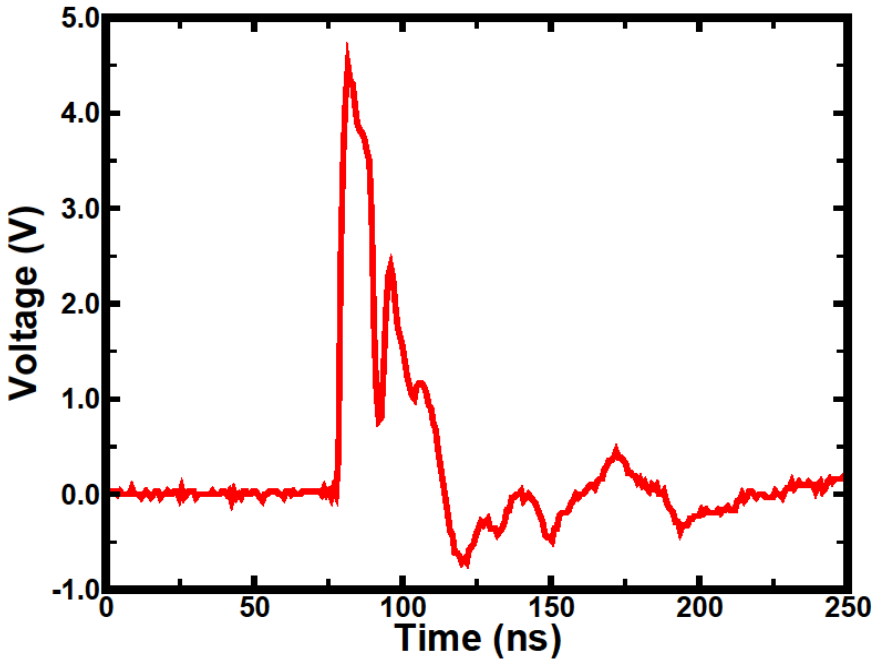



Figure 56. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 4.5 V.

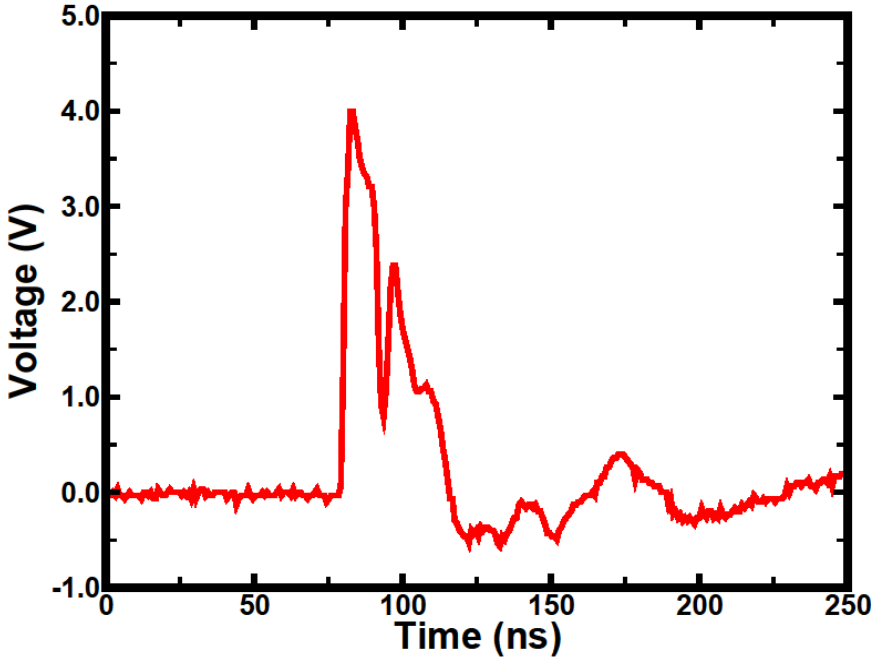



Figure 57. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 4 V.

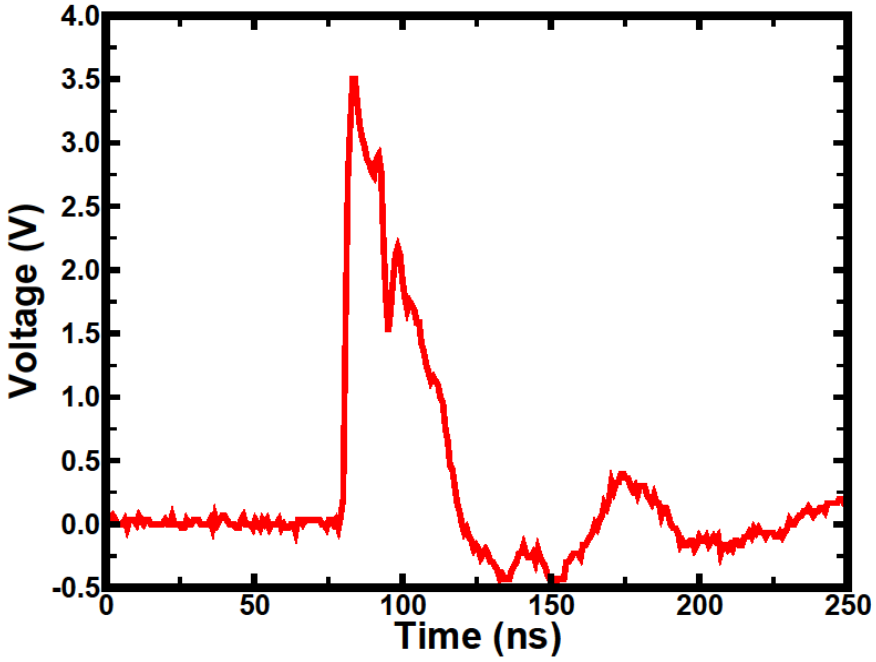



Figure 58. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 3.5 V.

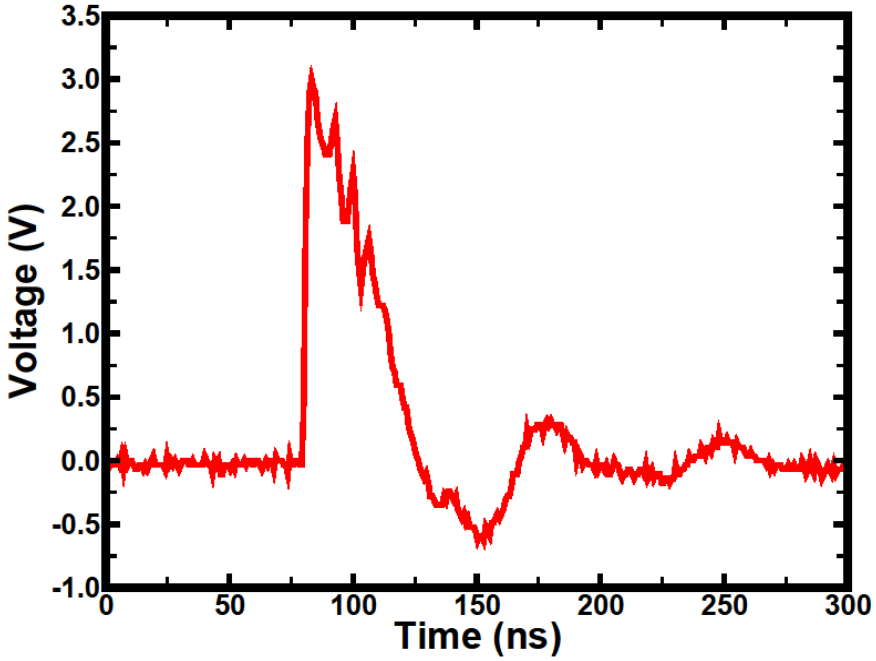



Figure 59. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 3 V.

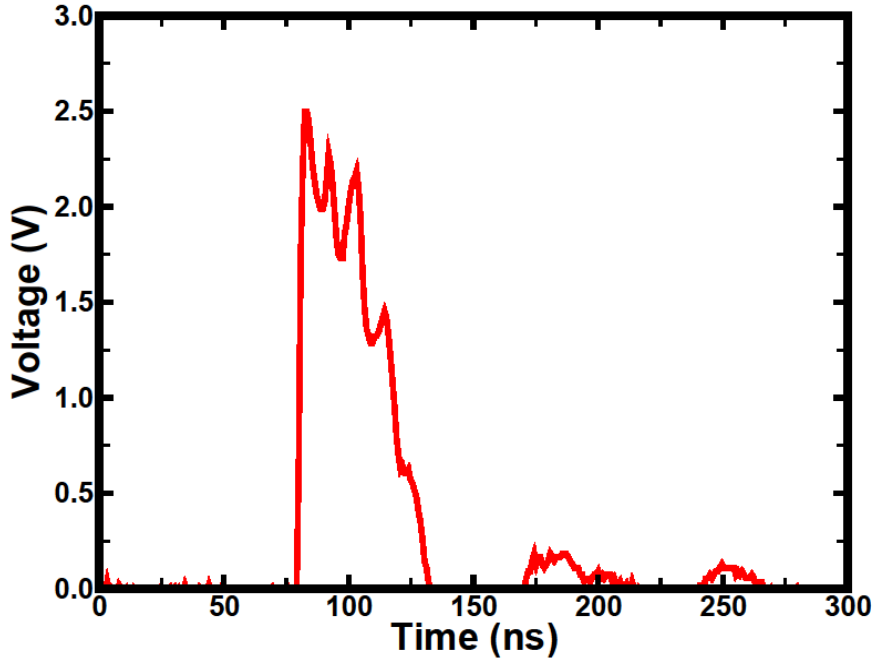



Figure 60. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 2.5 V.

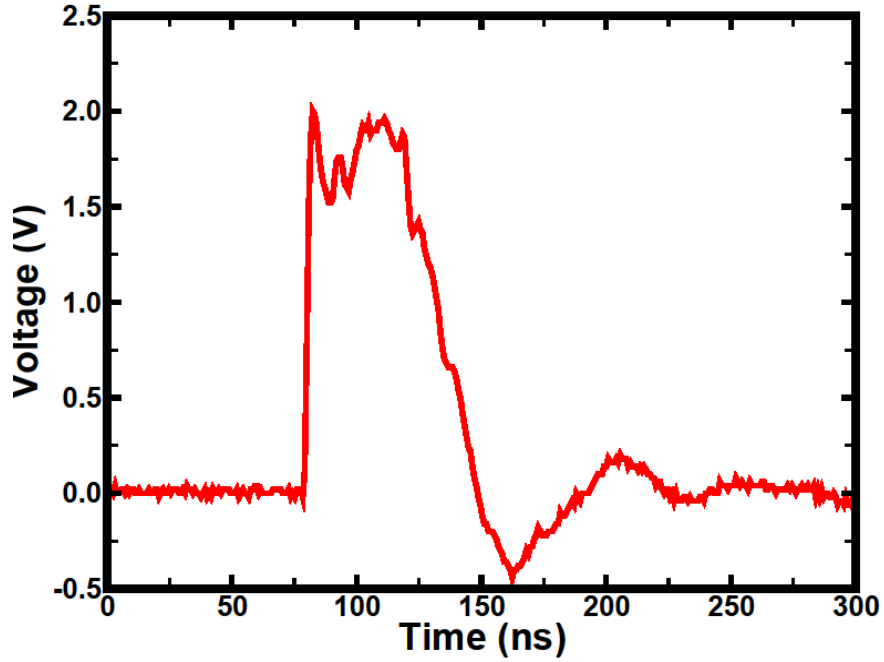



Figure 61. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 2 V.

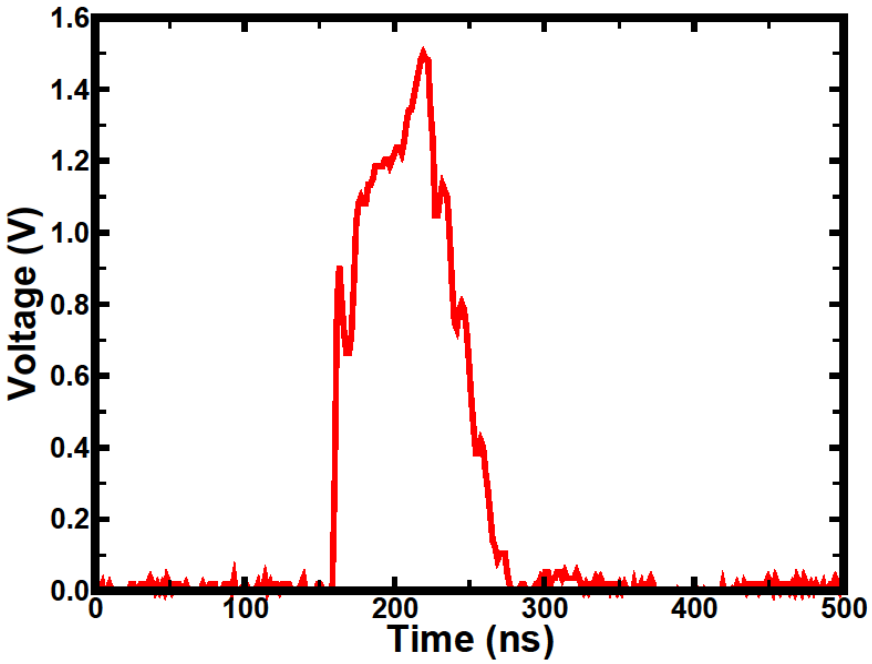



Figure 62. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.5 V.

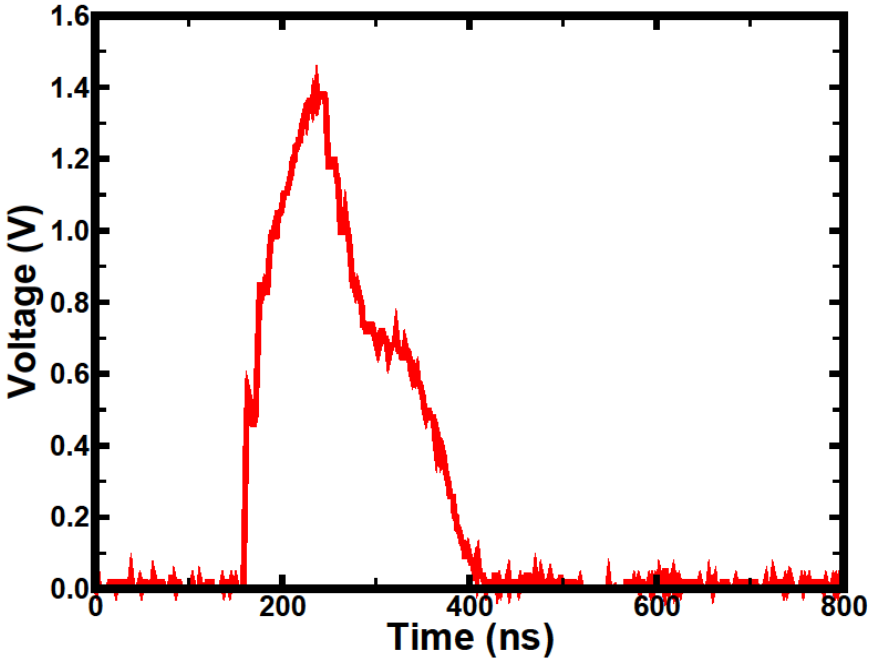



Figure 63. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.4 V.

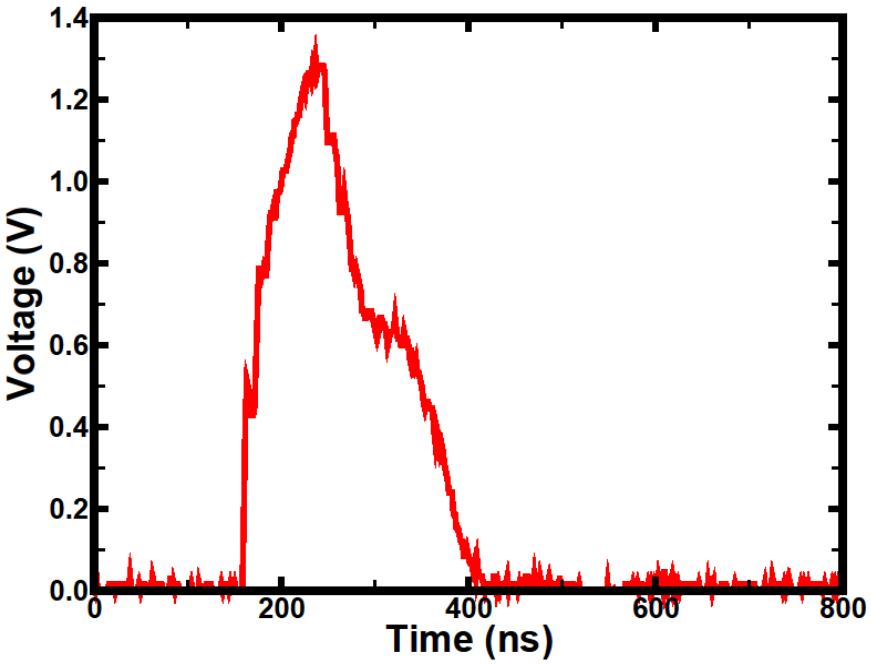



Figure 64. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.3 V.

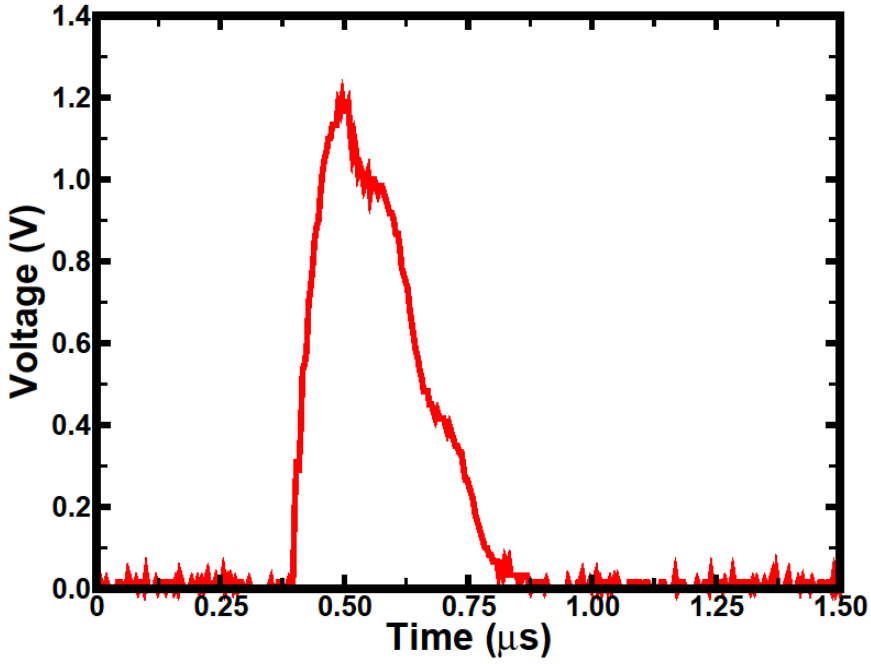



Figure 65. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.2 V.

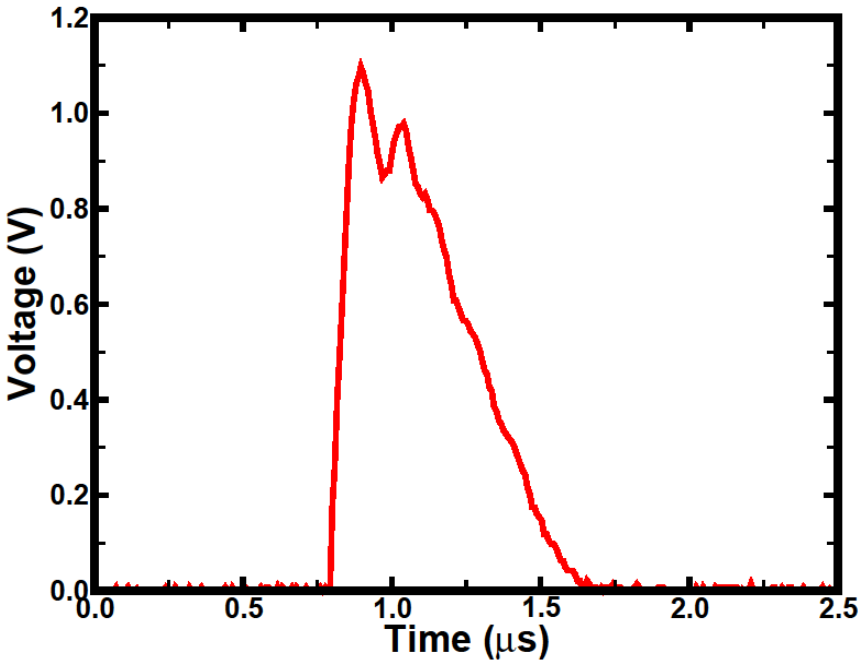



Figure 66. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1.1 V.

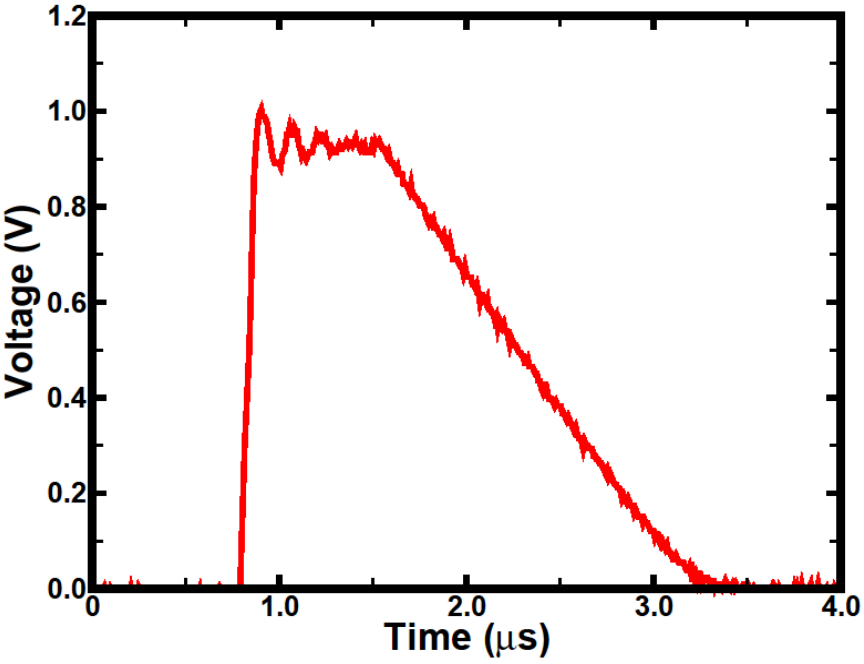



Figure 67. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 1 V.

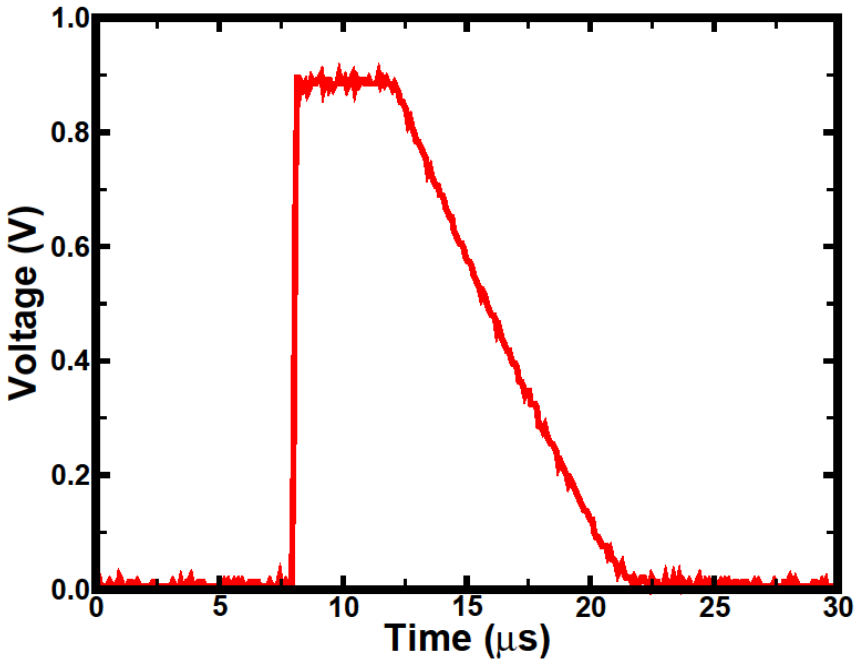



Figure 68. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a 20 inverter chain with a supply voltage of 0.9 V.

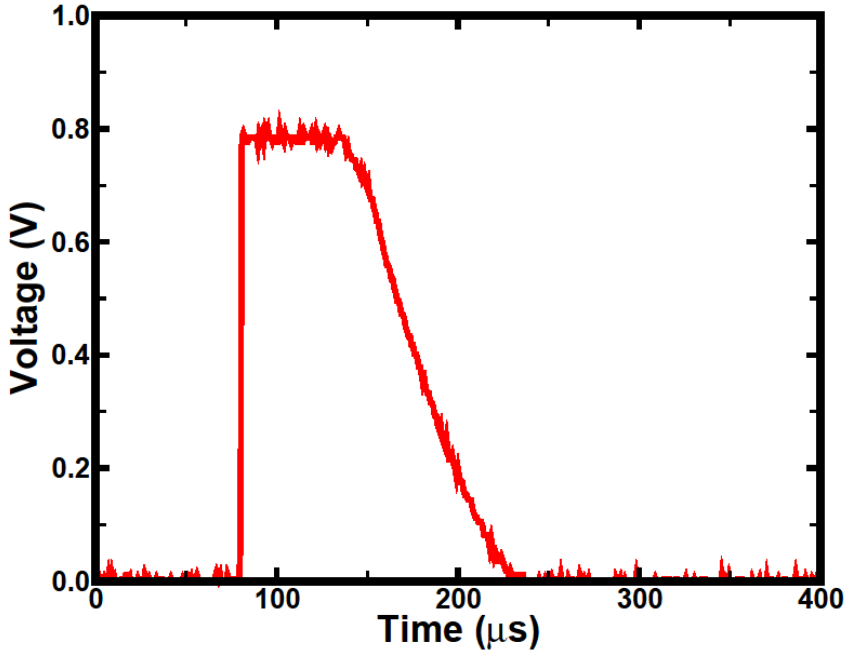



Figure 69. One of the 2500 transients captured after charge was deposited by a laser with a pulse energy of 67.2 pJ on a PMOS transistor in the last inverter in a twenty 20 inverter chain with a supply voltage of 0.9 V.

APPENDIX F

EXPERIMENTAL SINGLE-EVENT TRANSIENT PULSEWIDTH DETAILS

All tables presented in this Appendix show the average, minimum, and maximum single-event transient pulsewidths for a given set of experimental conditions. Additionally, the standard deviation in pulsewidths also is listed. The transients were generated by depositing charge from a laser on a single transistor in the last inverter in a string of 20 that were fabricated in the AMI 0.5 μm process.

Table 1. Transient pulsewidths as a function of supply for strikes on an NMOS transistor by a laser with a pulse energy of 22.4 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 2.64E-05 | 1.64E-05 | 3.16E-05 | 3.62E-06 |
| 0.8 | 1.39E-05 | 6.40E-06 | 1.60E-05 | 1.46E-06 |
| 0.9 | 1.76E-06 | 1.50E-06 | 1.88E-06 | 6.87E-08 |
| 1.0 | 3.10E-07 | 1.28E-07 | 3.64E-07 | 4.20E-08 |
| 1.1 | 9.90E-08 | 2.40E-08 | 1.20E-07 | 1.56E-08 |
| 1.2 | 4.90E-08 | 4.00E-08 | 5.12E-08 | 1.37E-09 |
| 1.3 | 2.88E-08 | 1.92E-08 | 3.20E-08 | 2.81E-09 |
| 1.4 | 1.95E-08 | 1.68E-08 | 2.24E-08 | 7.05E-10 |
| 1.5 | 1.00E-08 | 6.40E-09 | 1.52E-08 | 7.94E-10 |
| 2.0 | 7.38E-09 | 6.80E-09 | 8.00E-09 | 1.73E-10 |
| 2.5 | 4.10E-09 | 2.00E-09 | 4.80E-09 | 5.05E-10 |
| 3.0 | 3.73E-09 | 2.00E-10 | 4.60E-09 | 7.26E-10 |
| 3.5 | 3.04E-09 | 2.00E-10 | 4.00E-09 | 8.05E-10 |
| 4.0 | 4.30E-09 | 3.80E-09 | 4.80E-09 | 1.71E-10 |
| 4.5 | 3.54E-09 | 2.40E-09 | 4.20E-09 | 2.51E-10 |
| 5.0 | 1.83E-09 | 2.00E-10 | 3.20E-09 | 5.67E-10 |

Table 2. Transient pulsewidths as a function of supply for strikes on an NMOS transistor by a laser with a pulse energy of 44.8 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 2.44E-05 | 4.00E-07 | 3.00E-05 | 4.28E-06 |
| 0.8 | 1.15E-05 | 2.00E-07 | 1.54E-05 | 4.48E-06 |
| 0.9 | 1.52E-06 | 2.00E-08 | 1.82E-06 | 4.27E-07 |
| 1 | 3.00E-07 | 4.00E-09 | 3.36E-07 | 5.21E-08 |
| 1.1 | 1.07E-07 | 9.60E-08 | 1.16E-07 | 2.40E-09 |
| 1.2 | 4.63E-08 | 4.32E-08 | 4.96E-08 | 9.64E-10 |
| 1.3 | 3.11E-08 | 2.88E-08 | 3.28E-08 | 4.53E-10 |
| 1.4 | 2.05E-08 | 1.92E-08 | 2.24E-08 | 4.84E-10 |
| 1.5 | 1.55E-08 | 8.00E-10 | 1.84E-08 | 2.02E-09 |
| 2 | 9.37E-09 | 6.20E-09 | 1.02E-08 | 2.61E-10 |
| 2.5 | 6.38E-09 | 5.00E-09 | 7.20E-09 | 4.22E-10 |
| 3 | 5.76E-09 | 4.80E-09 | 6.40E-09 | 2.93E-10 |
| 3.5 | 5.26E-09 | 3.80E-09 | 6.00E-09 | 3.79E-10 |
| 4 | 7.17E-09 | 5.40E-09 | 7.60E-09 | 2.03E-10 |
| 4.5 | 6.57E-09 | 5.20E-09 | 7.20E-09 | 2.04E-10 |
| 5 | 5.55E-09 | 3.60E-09 | 6.20E-09 | 2.02E-10 |

Table 3. Transient pulsewidths as a function of supply for strikes on an NMOS transistor by a laser with a pulse energy of 67.2 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 2.56E-05 | 2.00E-05 | 3.20E-05 | 2.31E-06 |
| 0.8 | 1.23E-05 | 1.08E-05 | 1.56E-05 | 5.23E-07 |
| 0.9 | 1.45E-06 | 1.30E-06 | 1.82E-06 | 4.46E-08 |
| 1.0 | 2.98E-07 | 2.84E-07 | 3.28E-07 | 4.48E-09 |
| 1.1 | 9.84E-08 | 8.80E-08 | 1.08E-07 | 2.71E-09 |
| 1.2 | 4.42E-08 | 4.16E-08 | 4.80E-08 | 9.35E-10 |
| 1.3 | 2.66E-08 | 2.32E-08 | 3.60E-08 | 2.01E-09 |
| 1.4 | 1.91E-08 | 1.76E-08 | 2.32E-08 | 3.92E-10 |
| 1.5 | 1.64E-08 | 1.20E-08 | 1.76E-08 | 4.48E-10 |
| 2.0 | 1.11E-08 | 1.00E-08 | 1.24E-08 | 3.36E-10 |
| 2.5 | 7.78E-09 | 6.80E-09 | 8.60E-09 | 3.66E-10 |
| 3.0 | 7.04E-09 | 5.60E-09 | 7.60E-09 | 2.28E-10 |
| 3.5 | 6.48E-09 | 5.00E-09 | 7.40E-09 | 4.97E-10 |
| 4.0 | 9.11E-09 | 6.00E-09 | 9.60E-09 | 2.07E-10 |
| 4.5 | 8.40E-09 | 6.80E-09 | 9.00E-09 | 2.13E-10 |
| 5.0 | 7.12E-09 | 6.20E-09 | 7.80E-09 | 2.14E-10 |

Table 4. Transient pulsewidths as a function of supply for strikes on an NMOS transistor by a laser with a pulse energy of 100.3 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 2.73E-05 | 2.16E-05 | 3.88E-05 | 1.66E-06 |
| 0.8 | 1.09E-05 | 9.20E-06 | 1.60E-05 | 4.69E-07 |
| 0.9 | 1.38E-06 | 1.24E-06 | 1.68E-06 | 4.71E-08 |
| 1.0 | 2.96E-07 | 2.80E-07 | 3.20E-07 | 4.53E-09 |
| 1.1 | 5.53E-08 | 4.40E-08 | 8.40E-08 | 4.60E-09 |
| 1.2 | 3.99E-08 | 3.76E-08 | 4.40E-08 | 8.95E-10 |
| 1.3 | 2.31E-08 | 2.08E-08 | 3.20E-08 | 8.31E-10 |
| 1.4 | 1.97E-08 | 1.12E-08 | 2.16E-08 | 8.79E-10 |
| 1.5 | 1.59E-08 | 1.12E-08 | 1.68E-08 | 8.44E-10 |
| 2.0 | 1.35E-08 | 1.08E-08 | 1.58E-08 | 1.09E-09 |
| 2.5 | 8.23E-09 | 6.20E-09 | 9.60E-09 | 5.82E-10 |
| 3.0 | 7.40E-09 | 5.80E-09 | 8.80E-09 | 6.78E-10 |
| 3.5 | 6.44E-09 | 4.80E-09 | 8.40E-09 | 7.79E-10 |
| 4.0 | 1.05E-08 | 3.60E-09 | 1.16E-08 | 6.46E-10 |
| 4.5 | 9.27E-09 | 8.00E-09 | 1.02E-08 | 2.65E-10 |
| 5.0 | 8.78E-09 | 7.60E-09 | 9.60E-09 | 2.56E-10 |

Table 5. Transient pulsewidths as a function of supply for strikes on an PMOS transistor by a laser with a pulse energy of 22.4 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 1.67E-04 | 1.56E-04 | 1.78E-04 | 3.85E-06 |
| 0.8 | 7.33E-05 | 7.12E-05 | 7.60E-05 | 7.00E-07 |
| 0.9 | 8.11E-06 | 7.92E-06 | 8.32E-06 | 6.27E-08 |
| 1.0 | 1.44E-06 | 1.41E-06 | 1.46E-06 | 9.04E-09 |
| 1.1 | 4.41E-07 | 4.24E-07 | 4.56E-07 | 5.90E-09 |
| 1.2 | 2.18E-07 | 2.12E-07 | 2.24E-07 | 2.26E-09 |
| 1.3 | 1.13E-07 | 1.10E-07 | 1.25E-07 | 1.43E-09 |
| 1.4 | 8.60E-08 | 8.48E-08 | 8.80E-08 | 7.58E-10 |
| 1.5 | 6.64E-08 | 6.56E-08 | 6.72E-08 | 8.00E-10 |
| 2.0 | 4.91E-08 | 4.56E-08 | 5.12E-08 | 6.43E-10 |
| 2.5 | 3.24E-08 | 2.88E-08 | 3.36E-08 | 5.53E-10 |
| 3.0 | 9.11E-09 | 1.60E-09 | 2.64E-08 | 4.33E-09 |
| 3.5 | 7.25E-09 | 3.20E-09 | 1.04E-08 | 2.18E-09 |
| 4.0 | 7.31E-09 | 4.00E-09 | 8.80E-09 | 5.10E-10 |
| 4.5 | 6.37E-09 | 3.20E-09 | 8.00E-09 | 5.17E-10 |
| 5.0 | 4.95E-09 | 2.40E-09 | 6.40E-09 | 6.87E-10 |

Table 6. Transient pulsewidths as a function of supply for strikes on an PMOS transistor by a laser with a pulse energy of 44.8 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.77 | 2.79E-04 | 2.22E-04 | 3.46E-04 | 2.23E-05 |
| 0.8 | 7.93E-05 | 7.12E-05 | 8.24E-05 | 1.15E-06 |
| 0.9 | 8.14E-06 | 7.92E-06 | 8.32E-06 | 6.23E-08 |
| 1.0 | 1.42E-06 | 1.40E-06 | 1.46E-06 | 8.56E-09 |
| 1.1 | 4.37E-07 | 4.16E-07 | 4.48E-07 | 5.72E-09 |
| 1.2 | 2.17E-07 | 2.12E-07 | 2.24E-07 | 2.19E-09 |
| 1.3 | 1.14E-07 | 1.10E-07 | 1.25E-07 | 1.54E-09 |
| 1.4 | 8.70E-08 | 8.48E-08 | 8.96E-08 | 7.84E-10 |
| 1.5 | 6.72E-08 | 5.28E-08 | 6.88E-08 | 6.87E-10 |
| 2.0 | 5.09E-08 | 4.96E-08 | 5.20E-08 | 4.43E-10 |
| 2.5 | 3.48E-08 | 2.72E-08 | 3.68E-08 | 2.26E-09 |
| 3.0 | 2.08E-08 | 1.92E-08 | 2.80E-08 | 2.08E-09 |
| 3.5 | 1.29E-08 | 8.80E-09 | 2.16E-08 | 2.52E-09 |
| 4.0 | 9.53E-09 | 7.20E-09 | 1.20E-08 | 6.56E-10 |
| 4.5 | 8.94E-09 | 5.60E-09 | 1.04E-08 | 5.88E-10 |
| 5.0 | 7.23E-09 | 3.20E-09 | 8.80E-09 | 5.38E-10 |

Table 7. Transient pulsewidths as a function of supply for strikes on an PMOS transistor by a laser with a pulse energy of 67.2 pJ.

| VDD (V) | Avg PW (s) | Min PW (s) | Max PW (s) | Std Dev (s) |
|---|---|---|---|---|
| 0.8 | 9.06E-05 | 8.40E-05 | 9.60E-05 | 1.93E-06 |
| 0.9 | 8.18E-06 | 8.00E-06 | 8.40E-06 | 6.35E-08 |
| 1.0 | 1.44E-06 | 1.13E-06 | 1.47E-06 | 1.09E-08 |
| 1.1 | 4.30E-07 | 4.08E-07 | 4.48E-07 | 5.90E-09 |
| 1.2 | 2.16E-07 | 2.12E-07 | 2.24E-07 | 2.18E-09 |
| 1.3 | 1.13E-07 | 1.10E-07 | 1.23E-07 | 1.29E-09 |
| 1.4 | 1.13E-07 | 1.10E-07 | 1.23E-07 | 1.29E-09 |
| 1.5 | 6.76E-08 | 6.56E-08 | 7.04E-08 | 7.27E-10 |
| 2.0 | 5.18E-08 | 5.04E-08 | 5.28E-08 | 4.11E-10 |
| 2.5 | 3.09E-08 | 2.72E-08 | 3.68E-08 | 3.96E-09 |
| 3.0 | 2.13E-08 | 1.92E-08 | 2.32E-08 | 5.94E-10 |
| 3.5 | 1.89E-08 | 1.12E-08 | 2.56E-08 | 1.83E-09 |
| 4.0 | 1.16E-08 | 7.20E-09 | 1.52E-08 | 1.04E-09 |
| 4.5 | 1.04E-08 | 8.00E-09 | 1.20E-08 | 7.41E-10 |
| 5.0 | 8.73E-09 | 6.40E-09 | 1.04E-08 | 6.19E-10 |

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