

# **Portable Behavioral Modeling of TID Degradation of Voltage Feedback Op-Amps**

By

Srikanth Jagannathan

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Professor Lloyd W. Massengill

Professor Tim Holman

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## CHAPTER I

### 1 INTRODUCTION

With increase in complexity due to the ever decreasing device sizes of the modern day electronic components, their enhanced sensitivity to the radiation environment remains an ever greater source of concern. Simulators play a vital role in understanding the interactions between bombarding energetic particles and semiconductor devices. The simulation of radiation effects in integrated circuits (ICs) is generally performed using SPICE-like simulators. The transistor level model of a complex circuit (the complexity is in terms of types of analyses and number of components) used in SPICE simulators can result in very long, sometimes unaffordable, computing time. It has been shown that the memory and computing time required by SPICE grow super-linearly with the circuit size [1].

The purpose of behavioral models is to simulate circuit performance within acceptable accuracy limits without the requirement of a complete transistor-level model of an IC, and its associated development time and cost. The general approach of behavioral modeling is to represent circuit functions with abstract mathematical models that are weakly coupled to underlying circuit architectures or detailed transistor schematics. Once the operation of the IC is understood (from either hardware testing or detailed simulations), Hardware Description Languages (HDL) behavioral models enable the capture of this macro operation in a straightforward implementation conducive to high-level simulations. Such behavioral models can offer reasonable accuracy, coupled with increased simulation speed, for complex circuits incorporating many ICs (such as a board-level system).

This thesis presents a generic behavioral modeling technique for total-ionizing dose (TID) degradation using VHDL-AMS that is applicable to a wide range of voltage feedback amplifiers. We demonstrate the technique via an LM124 - a common, high gain, internally frequency compensated operational amplifier designed to operate over a wide range of voltages.



## CHAPTER II

### 2 RADIATION EFFECTS OVERVIEW

We live in a universe bombarded with radiation. Since semiconductor technology began to be used in space and military environments, extensive study has been done to understand the effects of radiation on the semiconductor devices and circuits. In many of the commercial or military space systems the ICs are required to be tolerant to high levels of ionizing or total-dose radiation. This type of radiation can result from space environment, nuclear reactor environment, nuclear weapon environment, controlled fusion environment or from high-energy physics accelerators. Also, the ICs are exposed to ionizing radiation during their fabrication process. Independent of its source, the exposure to these ionizing particles results in considerable damage to the IC materials. This damage can lead to circuit performance degradation, logic upset, and even catastrophic circuit failure. A brief introduction on the most important radiation environment – the space environment and the interaction of ionizing radiation with the semiconductor devices and circuits is discussed here.

#### **2.1 Space Environment:**

The space radiation environment consists of variety of energetic particles with energies varying from keV to GeV and beyond. There are three main categories of these particles.

1. *Trapped particles:* This consists of a broad spectrum of energetic particles that are trapped by the earth magnetic field called the Van Allen Belts. These divide into two belts, an

inner belt extending to 2.5 times earth radii and comprising of energetic protons up to 600 MeV together with electrons up to several MeV, and an outer belt comprising of mainly electrons extending to 10 times earth radii.

2. *Galactic cosmic rays*: This consists of low fluxes of energetic charge particle that originate outside of our solar system. These cosmic rays comprises of 85% protons (hydrogen nuclei), 14% alpha particles (helium nuclei) and 1% heavy ions with energies extending up to 1 GeV.
3. *Solar particle events*: This consists of sporadic bursts of radiation emitted by the sun, mainly protons and heavy ions. Energies typically range up to several hundred MeV to GeV.

The low energy particles are stopped by the layer of shielding material that is used to protect the IC. For a typical shielding depth of 1 to 5 mm, photons with energy above 20keV, electrons above 1 MeV and protons above 10MeV can penetrate into the semiconductor.

## **2.2 Interaction of ionizing radiation with semiconductor material:**

When the radiation particle present in the environment strikes the semiconductor material it generates secondary electrons that are very energetic when compared to the energies of the valence electrons. These energetic secondary electrons can in turn ionize the atoms, generating electron-hole pairs. As long as energies of the generated electrons and holes are greater than the minimal energy required for an electron-hole pair generation, they can in turn generate supplementary pairs. As a result, one single incident particle can create millions of electron-hole pairs. The total amount of energy deposited by a particle that results in electron-hole pair

production is commonly referred to as total ionizing dose (TID). The typical unit of TID that is used is rad, which denotes the energy absorbed per unit mass of  $\text{SiO}_2$ . A rad ( $\text{SiO}_2$ ) is 100 ergs per gram of  $\text{SiO}_2$ .  $\text{SiO}_2$  is specified because it is the material most sensitive to ionization damage in the devices and circuits. The basic degradation mechanism of ionizing radiation on MOS and BJT are different and is presented below.

### 2.3 Total-Dose Ionizing effects on MOS structures:

#### Mechanism:

The damage responsible for the total-dose degradation of MOS devices occurs in the  $\text{SiO}_2$  (insulator) layer of device. The radiation damage in  $\text{SiO}_2$  layers consists of three components: build up of trapped charge in the oxide, an increase in number of interface traps and an increase in number of bulk oxide traps. Fig. 1 depicts the total-dose radiation effects with the use of an MOS band diagram.

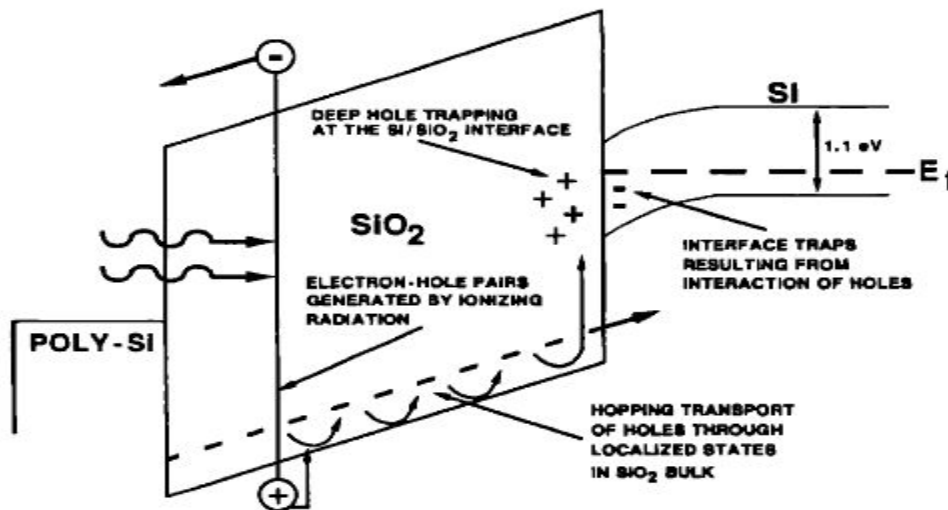


Figure 1. Band diagram illustrating the physical processes governing the response of MOS devices to total-dose ionizing radiation. (After F. B. McLean et al., Ref. [2])

When ionizing radiation is incident on the metal-oxide-semiconductor (MOS) structures, electron-hole pairs are generated along the track of the incident particle. Some fraction of these electron-hole pairs will recombine but that fraction is a complicated function of the material, the type of radiation and the applied bias. Since the generation of electron-hole pairs causes the change in threshold voltage of the MOS device, the fraction of electron-hole pairs that escape recombination can be determined experimentally. In SiO<sub>2</sub>, the rate of electron-hole pair creation is directly related to the electron-hole pair creation energy ( $\approx 17$  eV) [5-6]. Hence the total number of electron-hole pair created in SiO<sub>2</sub> is approximately equal to the total energy of ionizing radiation divided by 17 eV. The electron-hole pairs thus created are free to move under the applied bias. The electrons are very mobile in SiO<sub>2</sub> and under a positive gate bias it quickly moves to the contacts. In contrast the holes have a very low effective mobility and transport via a complicated stochastic trap-hopping process [7]. Some of the holes might get trapped inside the oxide leading to net positive charge. Others might move to the SiO<sub>2</sub>/Si interface where a certain fraction of it is trapped. Since the number of electron-hole pairs created is directly proportional to the amount of energy deposited by the radiation (or the energy absorbed by the material), the degradation of the device behaviors is also roughly proportional to the total dose of radiation received.

The incident radiation along with the creation of electron-hole pairs could break the chemical bonds in the oxide structure. Some of these bonds may be reformed during the electron-hole recombination, but others remain broken that leads to defect centers. These defect centers can serve as interface traps. The defects created by the radiation may themselves move to the strained region near the SiO<sub>2</sub>-Si interface and may also result in the formation of interface traps. There are many models predicting the holes trapping and annealing in SiO<sub>2</sub>-Si interface [8-9] and

buildup of radiation induced interface traps [10-11]. Radiation induced interface traps can either be of a donor or acceptor state. A donor trap level is in a neutral charge state when it is below the Fermi level, and becomes positively charge state by giving up an electron when it moves above the Fermi level. An acceptor trap level is in a neutral charge state when it is above the Fermi level, and becomes negatively charged by accepting an electron when it moves below the Fermi level. When an external bias is applied to the gate of MOS, the energy level of the interface traps moves either up or down relative to the Fermi level. The charge state of the traps changes when the energy state crosses the Fermi level.

The radiation-induced charge components mentioned above, affects the characteristics of MOS transistors. The oxide-trapped charge shifts the  $I_{DS}$ - $V_{DS}$  curve in the negative direction. The interface traps tends to “stretch-out” the  $I_{DS}$ - $V_{DS}$  curve, so that a greater change in applied bias is required to cause the same change in current [12]. Fig 2 shows the plot of the drain current of NMOS transistor with the gate bias before and after radiation.

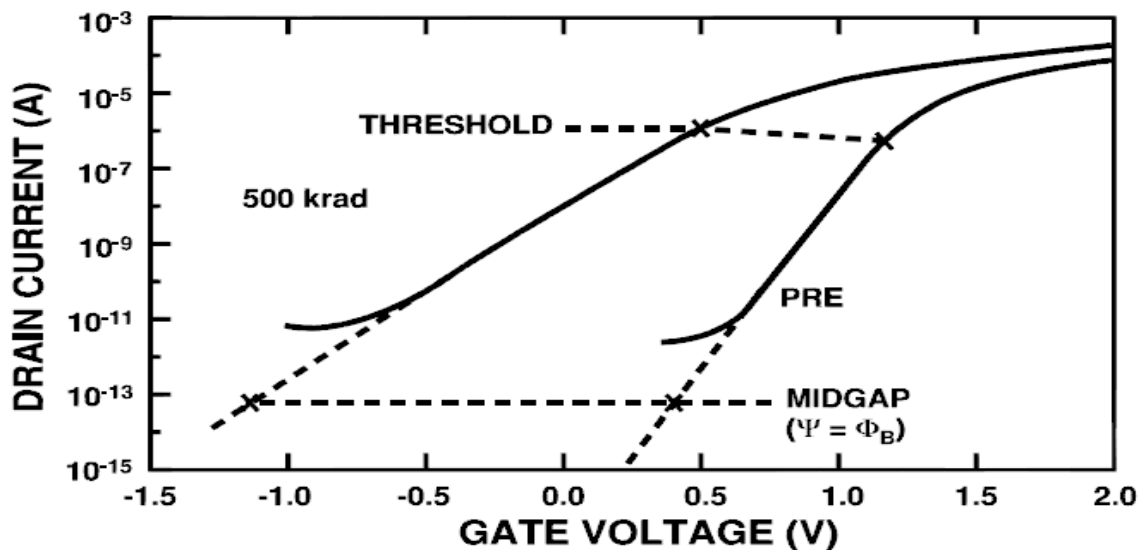


Fig. 2. Logarithmic function of drain current ( $I_d$ ) of NMOS with applied gate bias for pre-radiation and post-radiation [11].

We can see the curve shifts in the negative direction, just as in the case of MOS capacitor. This means that the threshold voltage of the NMOS has decreased, which implies that lesser gate voltage is required to turn on the device. Also, the curve is less steep compared to the pre-radiation case. This means that a greater change of applied bias is required for the same change in the drain current as before radiation.

The magnitude of the above changes depends on number of factors namely, the total dose of radiation, dose rate, applied bias, temperature during irradiation, type of transistor, length of time and temperature after irradiation. These changes in the properties of MOS integrated circuits could lead to profound changes in the circuit's characteristics, some which might be difficult to predict without extensive circuit simulations.

#### **2.4 Effect of total dose radiation on MOS devices and circuits:**

As discussed in the previous section, the generation of electron-hole pairs in the SiO<sub>2</sub> layer is the primary effect of ionizing radiation on MOS structures. The generated electron-hole pairs can either recombine or transport through the oxide. The electrons being very mobile, move quickly towards the gate contact and exit out of the oxide while the less mobile holes eventually become trapped within the oxide region. The electrons and holes that escape the initial recombination process can produce photocurrents and space charge effects in MOS devices and circuits. The buildup of space charge in the SiO<sub>2</sub> layer can cause the following effects:

- Voltage offsets
- Induced parasitic leakage currents

- Speed /mobility degradation.

#### 2.4.1 Effect of threshold voltage shifts on MOS transistors:

The threshold voltage of NMOS and PMOS transistors as a function of total-dose is illustrated in Fig. 3. The voltage shift is due to trapping of holes in the oxide and the buildup of interface traps [11]. In general, the effect of radiation-generated charge,  $\Delta\rho$ , on the threshold voltage shift,  $\Delta V_{th}$ , of a transistor is given by

$$\Delta V_{th} = (-1/C_{OX}) \int_0^{t_{OX}} \Delta\rho(x) (x/t_{OX}) dx \quad (1)$$

Where,  $t_{OX}$ : Thickness of the oxide  
 $C_{OX}$ : Capacitance of the oxide,  
 $x$  : Distance is measured from the gate of MOS.

We can deduce from Eq. (1) that the trapped positive charge (holes) in the oxide (i.e.  $\Delta\rho$  is positive) will cause will cause a negative shift in the threshold voltage of a device and negative charge will cause a positive shift in the threshold voltage. Generally, the initial response of an MOS transistor to radiation is a negative shift in the threshold voltage due to the buildup of trapped holes. The NMOS device may turn ‘ON’ at zero gate bias (no voltage applied to the gate) if sufficient amount of holes are trapped in the oxide. In this case, the device is said to have gone into ‘depletion mode’ and the device is permanently in the ‘ON’ state.

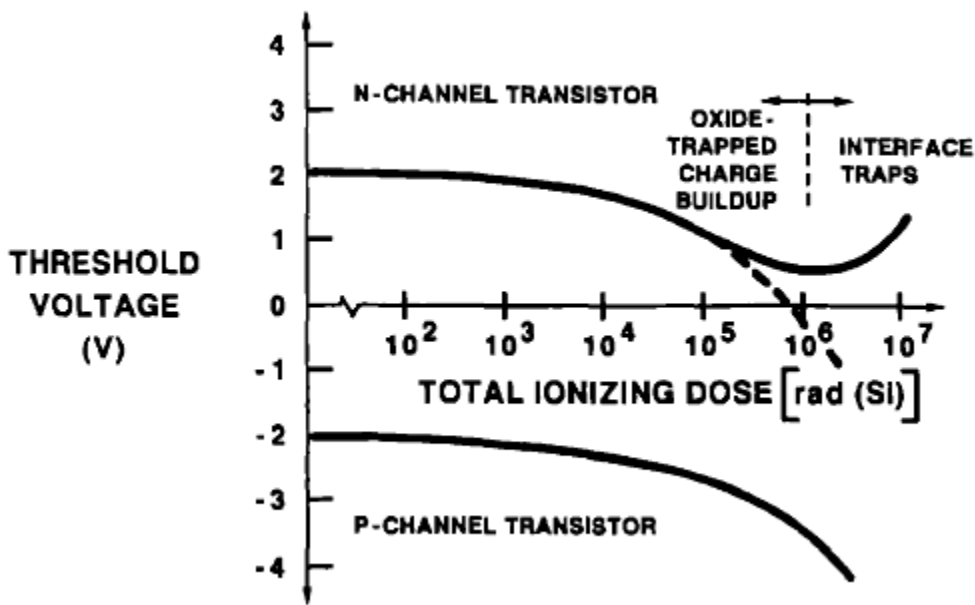


Fig. 3. Threshold voltage versus dose for irradiated n- and p-channel transistors [11].

After sometime, the acceptor-like (negatively charged) interface traps can shift the threshold voltage in the positive direction. This is termed as turn-around and can be attributed to negatively charged interface traps building up at a higher rate than trapped oxide charge. If sufficient negative charge is built-up in the interface traps then it is possible for the threshold voltage of NMOS device to increase to values more than the pre-irradiation (pre-rad) value. This condition is termed as “rebound” [11] or “super-recovery” [12] where most of the trapped holes are annealed leaving primarily the negative charge contribution of the interface traps. Hence we can say that the threshold voltage shift is time dependant, causing the shift at long times to be opposite to that observed at short times after irradiation. For the case of PMOS transistor, both the oxide trapped charge and interface trap charge (donor-like states) are positively charged. Hence the threshold voltage shift is negative and continues to increase in magnitude. The PMOS



can become permanently turned “OFF” if the magnitude of the threshold voltage increases more than the power supply voltage.

#### **2.4.2 Effects of threshold voltage shifts on ICs**

From the above section we can see that the threshold voltage shifts in NMOS and PMOS transistors can lead to functional failure of the IC when the threshold voltage of the NMOS transistor becomes lesser than 0V and/or the magnitude of threshold voltage of PMOS transistor becomes greater than supply voltage. During “rebound” of NMOS transistors, the increase of threshold voltage more than the pre-rad value causes the reduction of the drain current or the current drive of the transistor thereby slowing down the IC. “Rebound” has been observed to cause IC failure [9]. The threshold voltage shifts in PMOS transistors also reduce the current drive and lead to a degradation in speed or loss of TTL comparability. Finally, increased off-mode transistor leakage will be reflected by an increase in standby power supply current for an IC.

#### **2.4.3 Induced parasitic leakage currents**

The charge build-up in the isolation or the field oxide regions is the dominant effect of the ionizing radiation in the commercial CMOS process. Fig 5 shows the cross-section of a recessed field-oxide structure, specifically called local oxidation of silicon (LOCOS) that is used for device-to-device isolation. During the growth of a thick SiO<sub>2</sub> layer, a bird’s beak structure is formed as illustrated in the Fig 5. The incident radiation causes a buildup in positive charge in the field oxide and hence there is a parasitic leakage path between the source and the drain of

adjacent devices as shown in Fig 4. Hence there is an increase in leakage current when the device is off.

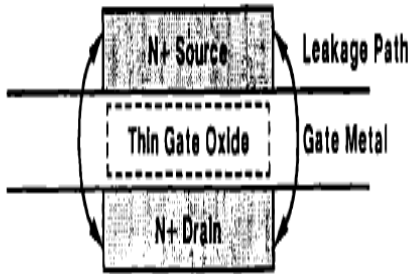


Fig. 4. Parasitic leakage path between source and drain (After F. B. McLean et al., Ref.[2])

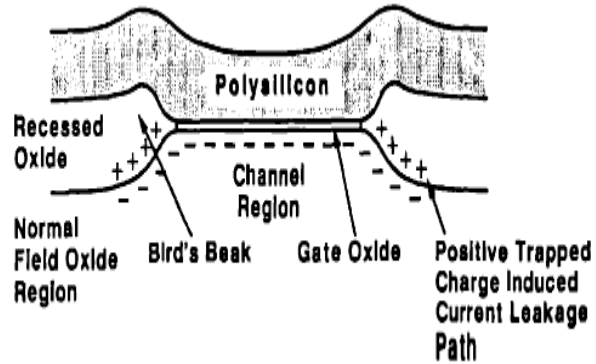


Fig. 5. Cross-section showing LOCOS isolation with bird's beak formation and radiation induced leakage paths [2].

#### 2.4.4 IC Speed/Mobility degradation

Interface traps results in undesirable threshold voltage shifts, degradation of channel mobility and transconductance of the device. This causes the parametric degradation of IC's speed, timing, drive etc. The interface traps generated due to radiation causes change in the shape of current-voltage characteristics. The interface traps are either filled or empty when the gate voltage of the MOSFET is swept. Hence, depending on the state of the traps, more (or less) charge (in turn, gate voltage) is needed at the gate to produce a given surface field in the device.

Fig. 6 shows the drain current ( $I_{DS}$ ) versus gate voltage ( $V_G$ ) at different regions of operation of the MOS device for varying total dose of radiation. There are two regions of operation that are of particular importance, namely the sub-threshold and saturation. At sub-

threshold, there are two characteristics of the curve that changes due to radiation. First, the shift of the  $I_D$ - $V_G$  curve towards the left for both NMOS and PMOS and this is due to the build-up of positive oxide trapped charges. Second, the decrease in the slope of the curve which is due to the radiation induced build-up of interface traps. The decrease in sub-threshold slope means that a larger gate voltage swing is needed to bring the device into strong inversion. Hence the interface traps decreases the switching speed of the device.

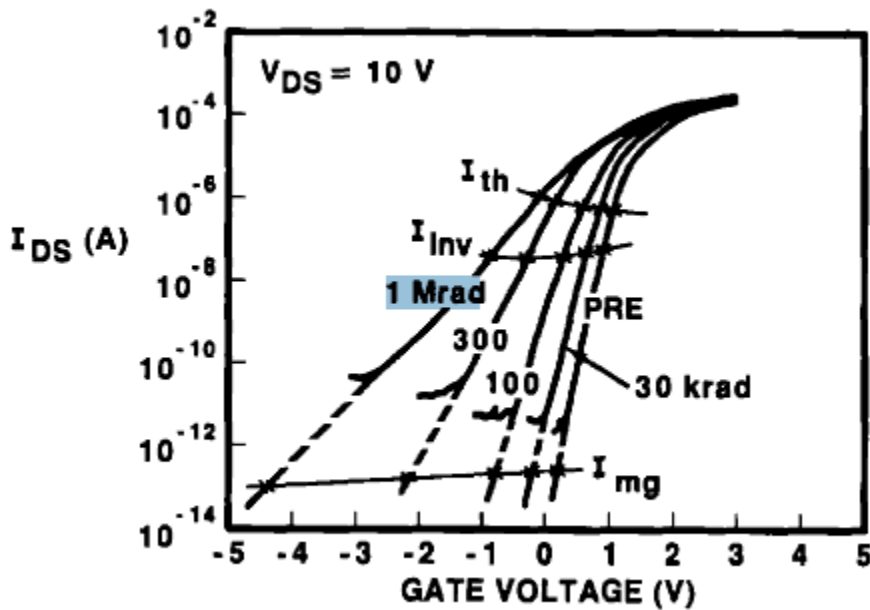


Fig. 6. Sub-threshold current-voltage curves for an MOS transistor before irradiation and at four different radiation levels [12].

Mobility degradation is another important effect of the build-up of interface traps. The increase in lattice and Coulomb scattering by charged interface traps results in the degradation of mobility [15-17]. Also, this reduction in mobility due to radiation leads to decrease in sub-threshold slope, transconductance and circuit speed.

All these degradation of IC behaviors discussed thus far could lead to the functional failure of ICs.

## **2.5 Total-Dose Ionizing effects on BJT structures:**

Bipolar junction transistors (BJTs) remain as important devices in the microelectronics industry, although the majority of products employ metal-oxide-semiconductor (MOS) transistors. Bipolar remains the dominant process for linear and mixed-signal circuits, and BiCMOS has become an important process for high-performance analog-to-digital converters (ADCs) and other mixed-signal microcircuits.

Bipolar is the dominant linear process due to performance advantages of higher voltage operation and current drive capability, lower noise, better linearity, and superior device matching. Bipolar microcircuits are the primary ICs used in the modern satellite power, signal processing, and control systems. BJT are commonly used in operational amplifiers, analog-to-digital converters, comparators, digital-to-analog converters, analog switches, multiplexer, voltage regulators, voltage references, and pulse width modulators.

There are different types of process that are used for fabrication of BJTs. The radiation response of the transistor is dependent on the type of process used and may vary significantly. Some of the factors that influence the radiation response are transistor vertical geometry, layout, presence of electrical fields due to field plates and other vertical fields, fringing fields, surface doping concentration, surface oxide quality and thickness. The most important factors that influences the total dose response out of the list specified above are the quality and thickness of the surface oxide (especially at the emitter base junction and over the base area) and the base and

emitter doping concentration at the Si-SiO<sub>2</sub> interface. The surface inversion and the gain degradation are the two important mechanisms due to total dose.

### **2.5.1 Substrate, Sidewall and Surface Inversion**

Inversion occurs where lightly doped p-type silicon is near to a thick field oxide. Inversion of p-type silicon at the SiO<sub>2</sub> interface is due to positive-type charge trapped in the SiO<sub>2</sub> next to the interface that depletes the p-type silicon surface to a maximum value. This causes channeling between the adjacent buried layers [19]. There are three major kinds of inversion, namely, the substrate, sidewall and surface inversion. In all cases of inversion, the formation of an inversion layer is strongly bias-dependent and is aided by a positive electric field. Many linear circuits operate at very low currents, for example in input structures and bias circuits that establish the operating conditions for the input stage. These circuits are inherently sensitive to small increases in leakage currents, such that even partial channeling due to inversion can have a major impact on circuit performance and parametric degradation.

### **2.5.2 Transistor Gain Degradation**

One of the key figures of merit for a BJT is the common emitter current gain ( $\beta$ ) which is the ratio of collector current to the base current ( $\beta=I_C/I_B$ ). It is desired to have a large  $\beta$  as possible in a forward biased BJT.

The degradation of the gain could be caused due to the increase in base current or a decrease in collector current. The base current has two main components, the bulk and surface components. The increase in surface component of the base current is the more important of the two. The bulk component is significant on wide-base structures such as lateral pnp and substrate

pnp transistors [20]. The surface component of the base current increase primarily due to the increase in interface states at the surface of the base and build-up of the positive charge in the emitter-base junction. This causes an increase in the base recombination current which results in increase in base current and decrease in gain. In most of the cases  $I_C$  remains constant, in some cases it increases with the dose, but the dominant mechanism is the increase in base current [21].

The dependence of increase in base current (or decrease in  $\beta$ ) with total dose as a function of process, device design and test parameters are given below:

*Transistor polarity:* In the case of npn transistors the positive oxide charge and interface states interact over the p-type base causing a significant base current increase. In the pnp case, the positive charge and interface traps offset and result in lesser base current. Hence with all other factors being equal, a pnp transistor will degrade less than an npn transistor [19].

*Oxide thickness:* The thicker the oxide is over the base and base-emitter junction areas, the greater the total trapped charge and the larger the increase in base current [20].

*Surface doping concentration:* The depletion effect of the trapped charges on the surface decreases with the doping concentration of base and emitter areas [19]. Hence, the more heavily doped base and emitter surfaces have lesser increase in base current.

*Emitter perimeter-to-area ratio:* The increase in base current occurs mainly in the base-emitter perimeter. Hence, decreasing the ratio of perimeter-to-area will result in lesser base current [19]. Also studies have shown that vertical pnp transistor has the least degradation; the substrate pnp transistor degradation is second; and the lateral pnp transistor has the most degradation.

*Transistor geometry:* A significant factor in the BJT total dose response is the transistor geometry (vertical, substrate and lateral transistors). It is determined by the ratio of lateral current flow to

the surface current flow in the base area [19]. It has been shown that the almost all the current flow in vertical device is in the vertical direction. Both the substrate and lateral devices have significant amount of current flowing in the surface. Hence vertical transistors have lesser degradation than the surface (substrate and lateral) transistors.

### **2.5.3 Effect of total dose radiation on bipolar integrated circuits**

This section will discuss the response of bipolar microcircuits to ionizing radiation. The response of digital microcircuits that are primarily fabricated in oxide-isolated processes will be discussed in the first section. The second section will discuss the response of linear ICs and introduce low rate effects.

#### **2.5.3.1 Bipolar Digital Circuits**

The bipolar digital microcircuits are primarily fabricated in recessed field oxide isolated process [21]. The failure modes of these processes are primarily associated with parasitic field-oxide leakage due to inversion associated with the recessed field oxide isolation. The recessed oxide is a field oxide which extends from the surface into the silicon as deep as the active components. This oxide provides lateral dielectric isolation, acts as a diffusion stop, and minimizes junction capacitances. Thus, recessed oxides allow much smaller feature size, increased packing density, and higher speed. However, when irradiated, several parasitic leakage paths can be formed including buried layer to buried layer channeling, collector to emitter channeling on walled emitters, and increased sidewall current [17]. The increased current associated with inversion of these parasitic MOS field transistors can lead to circuit failure as

low as 10 krad (Si) [17]. Also, the radiation response of bipolar circuits is highly sensitive to the bias conditions during the irradiation [18]

### **2.5.3.2 Bipolar Linear Circuits**

The radiation response of bipolar circuits is much more complex than the degradation of individual transistors. The interaction between transistors may cause offsetting effects, multiplicative effects or threshold effects [35]. Although the circuit response can be predicted based on the degradation of individual transistors, it is usually not possible to obtain device-level data for every transistor and bias condition in the circuit. The oxide-charge and interface-trap densities may depend on the bias of each particular device during irradiation and the gain also depends on the operating point. Changes in the characteristics of one device may result in changes to the bias points of other transistors. The problem is particularly difficult for technologies in which there are multiple types of transistors (*npn*, lateral *pnp*, substrate *pnp*, *n*-channel MOSFETs, *p*-channel MOSFETs, etc.). In addition, the gain degradation in bipolar transistors is a function of geometry [19] and it is rare to have test transistors available corresponding to all of the different device sizes used in a given circuit.

There have been numerous studies on the TID degradation of specific bipolar integrated circuits [30 – 34]. Few of the papers are discussed in this section. Johnston, et al. examined a variety of linear integrated circuits and found that in many ICs (at least at moderate total-dose levels) the input current is a good indicator of  $\beta$  degradation in the input transistors [22]. This paper was important in pointing out the high levels of degradation that may occur in integrated circuits that use lateral *pnp* BJTs and especially in pointing out the very significant ELDRS effects that may occur in these ICs.



Beaucour, et al. analyzed TID effects on LM137 voltage regulators from several different manufacturers [30]. Using circuit analysis and irradiation of individual transistors using a scanning transmission electron microscope, the failures were attributed to gain degradation in a multiple-collector lateral *pn*p transistor that supplies current to other parts of the circuit. Irradiating individual transistors within the circuit is a powerful technique for understanding the role of specific devices in determining the circuit-level degradation or the interaction between different devices.

The noise performance of bipolar linear integrated circuits also has been examined [35]. The increase in noise was attributed to increased recombination noise at the Si/SiO<sub>2</sub> interface and in the emitter-base depletion region. Radiation-induced changes in the bias point also may lead to changes in  $1/f$  noise due to the parasitic resistances.

In some cases, the radiation-induced changes in circuit parameters may not track the degradation of individual BJTs because of compensating effects in the circuit design. An example of this phenomenon has been analyzed for the LM111 voltage comparator [1]. At low total doses, the input bias current of the LM111 increases due to gain degradation in the circuit's input transistors. However, at high total doses, the input bias current decreases due to changes in the operating point of the input transistors caused by degradation in transistors elsewhere in the circuit.

Many complicated responses are possible in irradiated bipolar linear ICs and in general it is necessary to examine each circuit type in order to identify the critical transistors and failure mechanisms. In some cases, this task is simplified if a single transistor is responsible for the majority of the radiation-induced change. The most common example of this phenomenon is the relationship between input bias current and excess base current in input transistors [22].

The degradation of circuit parameters depends not only on the total dose but also on the dose rate. It has been demonstrated that many bipolar circuits are much more sensitive at low dose rates ( $<1$  rad/s) than at typical laboratory dose rates (50–300 rad/s) [24-25]. This dependence on low dose rate is known as the enhanced low dose rate sensitivity (ELDRS).

#### **2.5.4 Enhanced low dose rate sensitivity**

Bipolar linear circuits are in common use in space systems where they are exposed to ionizing radiation at very low dose rates. It has been demonstrated that many bipolar linear circuits exhibit a “true” dose rate effect that has become commonly known as enhanced low dose rate sensitivity. ELDRS is characterized by a low dose rate enhancement factor that is the ratio of the parametric degradation at a low dose rate to the degradation at a high dose rate for a fixed dose [25].

The total dose and dose rate response for circuits with large low dose rate enhancement depend on a number of factors, including processing, final passivation [26–28], pre irradiation thermal stresses during burn-in or packaging [29] and the amount of an external source of hydrogen, e.g. in the sealed package [30]. The largest low dose rate enhancement factors that have been observed occur in bipolar linear circuits that incorporate lateral and substrate pnp transistors [31].

ELDRS in bipolar linear circuits is characterized by the degradation of various circuit parameters such as input bias current, input offset voltage and output drive current. These parameters are often a combination of the degradation in several different types of transistors: vertical npn, substrate pnp and lateral pnp. In order to predict the ELDRS response of a circuit, the dose rate response of the various transistors used in the circuit must be known.

The parametric degradation of the circuit parameters discussed so far, for both MOS and bipolar circuits can be accurately captured in the behavioral model. Once captured, this behavioral model could be used to predict the behavior of the circuit at a given dose level. The basics of behavioral modeling are discussed in the next section.

## CHAPTER III

### 3 BEHAVIORAL MODELING TECHNIQUE

#### 3.1 Basics of Behavioral Modeling

The complexity of electronic systems being designed today is increasing in many dimensions. Designing to realize functionality while meeting a set of performance specifications requires the need for tools capable of overcoming relatively inaccurate and lengthy hand calculations. Circuit simulation with accurate and realistic models has been an invaluable tool for the verification of the performance of integrated circuits. Simulators hold a particularly important place in the world of analog and mixed-signal tools. The main objective of computer-aided-design (CAD) is the creation of methodologies and tools for design of engineering systems, helping the designers build functionalities while satisfying intended performance specifications. Primarily, the designers verify that the circuit designed will perform as expected. Over the past decades, the development of computer aids for the design of electronic systems has been the fastest growing areas of activity. Electronic ICs have grown rapidly from the relatively low complexity of the early days to the high sophistication of today. The task of circuit designers has become increasingly difficult, hence the need for more advance design aids.

Accuracy and speed of simulation are the two most important criteria for any simulator [1]. The complexity is in terms of number of components and of the types of analyses used. The transistor level model of a complex circuit used in SPICE simulators result in very long (sometimes unaffordable) computing time. It has been shown that the memory and computing time required by SPICE grow super-linearly with the circuit size [1]. Hence when complex

analog and mixed-signal systems are being designed, accurate circuit of the entire circuit is out of the question. In some cases, even if the circuit size is small, it might still be impossible to do a detailed SPICE simulation. For instance, in phased-locked-loop (PLL) circuits the period of the voltage-controlled-oscillator (VCO) is much smaller than the loop time constant. As a result, the simulation has to go through many cycles of the VCO to get an idea about the behavior of the circuit which makes SPICE simulation almost impractical [1].

Radiation effects simulations of microelectronics circuits are generally performed using SPICE-based simulators [38]. Unfortunately, transistor level simulations with SPICE are extremely time consuming and require a large amount of engineering work. Typical IC model development flow for total ionizing dose radiation enabled SPICE based models includes

- Designing, irradiating and testing transistor array structures manufactured with a particular fabrication process
- Characterizing SPICE transistor models and developing transistor parameter scaling with dose
- Constructing SPICE netlists representative of the actual circuit implementation
- Testing, tuning and validating against available macro circuit behaviors

An alternative that could be used to simulate analog/mixed signal design is the behavioral modeling technique. Behavioral IC models can be implemented without modeling the detailed transistor level implementation, and its associated development tasks and costs. Behavioral modeling offers excellent accuracy coupled with increased in simulation speed of complex circuits. The objective of behavioral modeling, in general, is to represent circuit functions with abstract mathematical models that are independent of circuit architectures or schematics. In top-

down design, designers can verify the system design before investing time in detailed circuit implementation, which enables them to explore the system design space rapidly [1]. In bottom-up design verifications, designers can verify complex system behavior efficiently, because evaluations of behavioral models are computationally cheap, resulting in fast system simulations [43].

The top-down design process implies a well-defined behavioral description of the analog function. The behavioral characterization of analog circuits is quite different from the digital one; the analog characterization is composed of not only the function the circuit is to perform, but also the second-order non-idealities intrinsic to analog operation. In fact, errors in the design often stem from the non-ideal behavior of the analog section, not from the selection of “wrong” functionality [1]. The behavioral modeling and simulation can help in selecting the correct architecture to implement the analog function with bounds (constraints) on the amount of non-idealities that is allowable given a set of specifications at the system level.

For digital circuits, behavioral modeling and simulation can be performed using hardware description languages like VHDL [44] or Verilog [45]. For analog and mixed-signal circuits, behavioral modeling and simulation can be performed using hardware description languages like MAST (Analogy, 1986), Verilog-AMS (Open Verilog International, under development) and VHDL-AMS (IEEE, 1999). VHDL simulations are computationally efficient compared to SPICE simulations because a VHDL simulator is event driven while SPICE is a node driven simulator [46].

The following are the features essential for the behavioral modeling of analog blocks [1]:

- The simulator and behavioral models have to be general. The behavioral model of a given analog block must describe the behavior of that block considered as a black box,

describing its input-output behavior in terms of a set of model parameters to be supplied by the designer. It also has to hide all the internal architectural details as much as possible, resulting in generic models.

- The simulation engine must be independent of any particular model, so that it is possible to simulate in different architectures in the same environment instead of having a different dedicated simulator for each of the architectures.
- The behavioral models for analog blocks must include not only the first-order behavior of the circuit, but also the analog second order effects, such as noise and distortion in order to get the realistic idea of the performance of the overall system.
- The behavioral simulation has to be done in time or frequency domain or in a mixture of both.

In order to realize a design having the features discussed above, the strategy is to first find the best abstract mathematical representations for specific types of analog circuits. This mathematical representation of the circuit functionality is referred to as the “Basis Functions”.

The basis function could be any of the following:

- Algebraic expressions
- Differential equations
- State-space representation
- Nodal equations using Kirchoff's voltage/current law
- s-domain or z-domain transfer functions
- Random process variables
- Look-up tables

Next step is to develop the behavioral simulation techniques to validate the model developed. Both time and frequency domain simulation has to be done in order to check the validity of the model in both the domains.

The behavioral model of this work was constructed using VHDL-AMS, a hardware description language. A brief introduction on VHDL-AMS is discussed below.

### **3.2 Overview of VHDL-AMS**

VHDL-AMS is the result of an IEEE effort to extend the VHDL language to support the modeling and simulation of analog and mixed-signal systems. It extends the digital HDL with new behavioral and structural language constructs and new simulation mechanisms [46]. VHDL-AMS is designed to fill a number of needs in the design process. First, it allows the description of the structure of a system, that is, how it is decomposed into sub-systems and how those sub-systems are interconnected. Second, it allows the specifications of the function of a system using familiar programming language and equations forms. Third, as a result, it allows the design of a system to be simulated before being manufactured, so that designers can quickly compare alternatives and test correctness without the delay and expense of hardware prototyping. Fourth, it allows the detailed structure of a design to be synthesized from a more abstract specification, allowing designers to concentrate on more strategic design decisions and reducing time to market.

A VHDL-AMS model consists of an entity and one or more architectures. The entity specifies the interface of the model to the outside world. It includes the description of the ports of the model (the points that can be connected to other models) and the definition of its generic parameters. The architecture contains the implementation of the model. It may be coded using a



structural style of description, a behavioral style, or a style combining structural, and behavioral elements. A structural description is a netlist; it is a hierarchical decomposition of the model into appropriately connected instances of other models. A behavioral description consists of concurrent statements to describe event-driven behavior and simultaneous statements to describe continuous behavior. Concurrent statements include the concurrent signal assignment for data flow modeling and the process statement for more general event-driven modeling.

When a VHDL-AMS model is instantiated in a structural description, the designer can specify which of several architectures to use for each instance. Alternatively, the decision can be postponed until immediately prior to the simulation. This allows for an easy and flexible reconfiguration of the model. For example, in top-down design, one architecture can describe a subsystem behaviorally with little detail, while another can add parasitic and a third can decompose the subsystem into lower level components [43].

A model of an analog system consists of the circuit nodes, analog unknowns to be calculated and the characteristic mathematical equation or the basis functions that specify analog behavior. In VHDL-AMS, terminals are used to represent the circuit nodes, quantities for the analog unknowns and simultaneous statements for the basis functions. The energy conservation laws apply at all the terminals. In electrical domain, the Kirchoff's current and voltage laws are applied at all the terminals.

The VHDL-AMS model is often tested using an enclosing model called the test bench. The test bench consists of an architecture body containing an instance of the component to be tested and processes that generate stimuli on signals, terminals and quantities connected to the component instance.

The simulation of the behavioral model developed in VHDL-AMS involves three stages: analysis, elaboration and execution. In the first stage, analysis, the VHDL-AMS description of the system is checked for various kinds of semantic and syntactic errors. If the analyzer finds no errors in the design, it creates an intermediate representation of the unit and stores it in the library. The second stage in simulating a model, elaboration, is the act of working through the design hierarchy and creating all the objects specified in the declarations. The ultimate result of the elaboration process is a collection of processes interconnected by nets and characteristic expressions, with each process possibly containing variables. The third stage of simulation is the execution of model. For digital portion of simulation, the passage of time is simulated in discrete steps depending on the events. Analog portions of the simulated system are evaluated by an analog solver at analog solutions points in continuous time.

The simulation starts with an initialization phase, followed by repetitive execution of simulation cycles. During the initialization phase, each signal and analog quantity is given an initial value depending on its type. The simulation time is set to zero, then each process instance is activated and its sequential statements executed. Execution of a process continues until it reaches a wait statement, which causes the process to be suspended. During the simulation cycle, the analog solver is first executed. Next, the simulation time is advanced to the next time at which a transaction on a signal has been scheduled. Then, all the transactions scheduled for that time is performed. When all the process have suspended again, the simulation cycle is repeated. Once the simulation gets to the stage where there are no further transactions scheduled, it stops since the simulation is then complete [46].

This thesis describes a generic behavioral modeling technique for total-ionizing dose (TID) degradation using VHDL-AMS that is applicable to a wide range of voltage feedback

amplifiers. All the functional simulation is done using SystemVision, a system modeling and analysis tool by Mentor Graphics. It provides a mixed-signal modeling and simulation environment using the power of VHDL-AMS and SPICE. We demonstrate the technique via an LM124 operational amplifier. A brief introduction on LM124 op amp is discussed below.

### **3.3 LM124 – A classic three stage operational amplifier**

LM124, is a high gain, internally frequency compensated operational amplifier which is designed specifically to operate over a wide range of voltages. Fig. 7 shows the simplified transistor level model (SPICE netlist also available) of the LM124 [39] op-amp, and illustrates the classic three stage op amp architecture [41]. The op amp contains an input or differential stage, an intermediate single-ended high-gain stage, and an output-buffering stage.

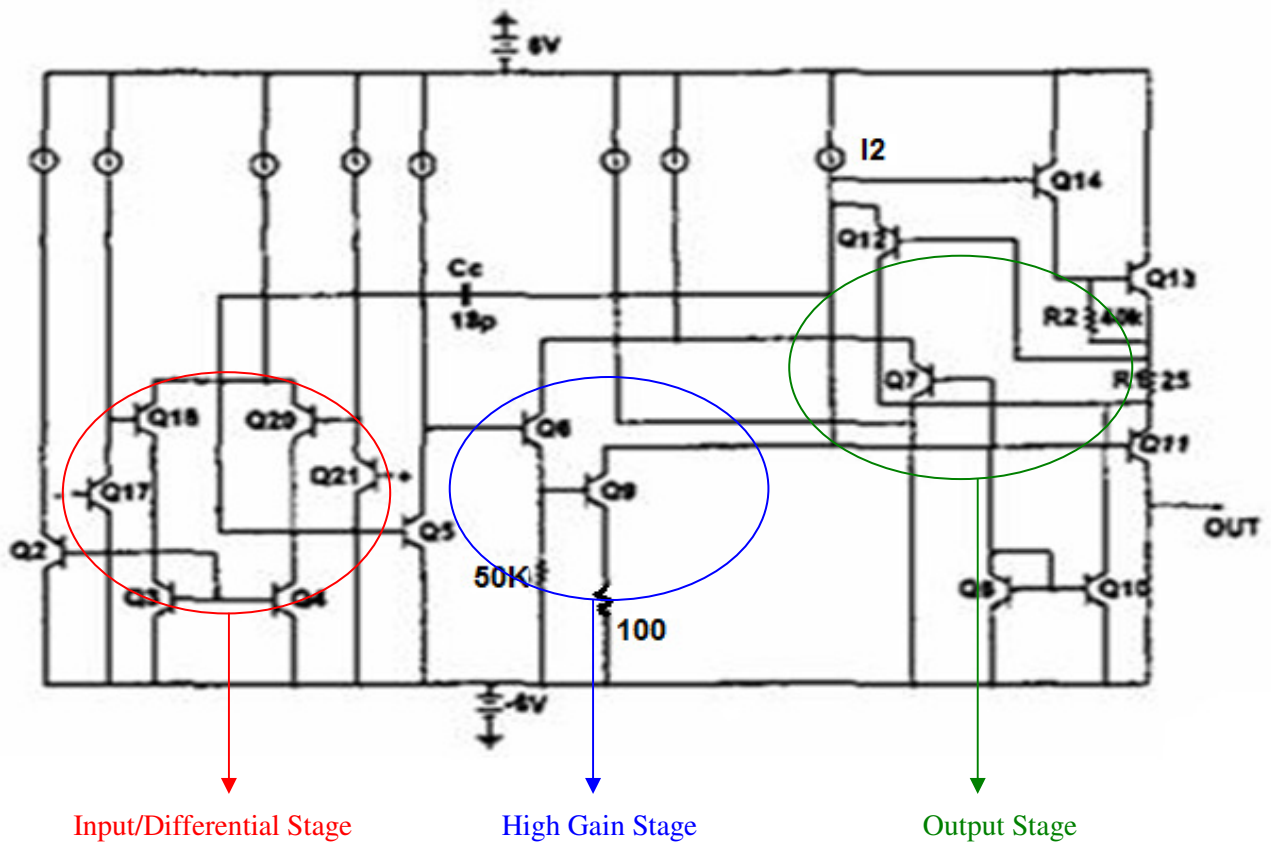


Fig. 7. Simplified schematic of LM124 [39]

### 3.3.1 Input Stage

The input stage consists of transistors Q17, Q18, Q20, Q21, Q3 and Q4 along with the biasing circuitry. It is a transconductance amplifier as it converts the differential voltage input into single-ended current output. Ideally, the input impedance of an op amp should be infinite, but in practice the input impedance of LM124 is about 10 MΩ and is dependent on frequency due to the capacitor component of the impedance. The output of the input stage is at the collector of Q5.

### 3.3.2 Second Stage

The second stage is the high gain trans-resistance amplifier that converts the current output from the input stage into voltage. It is composed of Q6, Q9, Q12, current source I2 and the 50 K $\Omega$  resistor connected to the emitter of Q6. Q6 acts as an emitter follower, thus giving the second stage a high input resistance. This minimizes the loading on the input stage and avoids loss of gain. Q9 acts as a common-emitter amplifier a 100  $\Omega$  resistor in the emitter. Its load is composed of high output resistance of current source I2 in parallel with the input resistance of the output stage (looking into the base of transistor Q22). Using the transistor current source as the load resistance (called active load) enables one to obtain high gain without resorting to the use of large load resistances, which would occupy a large chip area and require large power-supply voltages.

The output of the second stage is taken at the collector of Q9. Capacitor Cc is connected in the feedback path of the second stage to provide frequency compensation using the Miller compensation technique.

### 3.3.3 Output Stage

The purpose of the output stage is to provide the op amp with low output resistance. In addition, the output stage should be able to supply relatively large load currents without dissipating an unduly large amount of power in the IC. Transistor Q22, Q13, Q14, Q12 along with the resistances R2 and R1 form the output stage.

### 3.4 Functional Template of the Behavioral Model

The functional template of the behavioral model is built generically and captures the important macro behaviors of the three stage amplifiers. The approach taken in building the functional template is to identify the different stages of the circuit that has to be modeled, LM124 in this case. Once this is done, the stages are modeled and tested separately and then it is integrated to form the whole system. Since we know the stages that make up LM124, the functional template is build with five functional blocks as shown in Fig. 8. A brief functional description of each block is provided below.

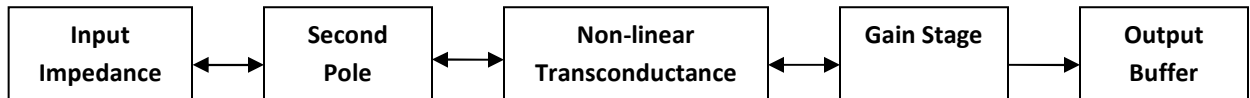


Fig. 8. Five stages in the behavioral model developed

The non-dominant, high-frequency pole of the op amp, also known as the second pole, is modeled in the second pole block. Other important non-ideal input behaviors such as input offset voltage and input offset/bias current are also implemented in this block. The non-linear transconductance block models slew-rate limiting. The gain stage blocks models open loop gain, gain-bandwidth product, Miller capacitance effect, and output voltage saturation. The output buffer block implements the output impedance of the amplifier.

#### 3.4.1 Input Impedance:

The input impedance block is used to model the frequency dependant impedances seen by the differential mode input signal and the common mode input signal. These are two separate

impedances, the differential mode input impedance and the common mode input impedance and is implemented using RC ladder networks.

### **3.4.2 Second pole:**

The second pole or the non-dominant, high-frequency pole due to parasitic capacitance in the circuit is modeled in this stage. It is implemented at the early stages of the behavioral model to be kind to the simulator so as to limit the nodes where higher frequency content must be simulated.

Other important non-ideal input op amp behaviors like input offset voltage, input offset current, input bias currents are also modeled in this stage.

### **3.4.3 Non-linear Transconductance:**

The non-linear transconductance block corresponds to the input stage of the 3-stage op amp where the input differential voltage is converted to the output current. This stage models the slew-rate limiting.

### **3.4.4 High-Gain:**

The high-gain block corresponds to the second stage of the 3-stage op amp which is the high gain stage. This block models open loop gain, gain-bandwidth product, Miller capacitance effect, and output voltage saturation.

### **3.4.5 Output Buffer:**

The output buffer block corresponds to the output stage of the op amp. This block implements the output impedance of the amplifier

Once the generic template was constructed, the next step was to extract and characterize the macro behaviors associated with each module of Fig. 9.



## CHAPTER IV

### 4 OP AMP PARAMETER EXTRACTION AND CHARACTERIZATION

With the development of the generic template of the behavioral model the next step was to characterize the op amps behaviors for pre-rad case and post-rad case. In general, the characterization process involves modeling of data-set available from hardware tests. Appropriate test structures have to be designed using the hardware parts. The degradation due to total dose radiation of the behaviors is measured by irradiating them to desired dose level.

In order to avoid this more tedious measurement of op amp behaviors using hardware test circuits and make use of the available SPICE netlist, the SPICE model was used for both the characterization processes. The SPICE model is considered as a black box and only the quantities related to the external terminals are used in the characterization process, hence it could well be replaced by hardware.

Before the characterization process, the SPICE netlist of LM124 was validated against a vendor data sheet [42] for pre-rad behaviors and the experiment results available from [40] for post-rad behaviors. All the op amp behaviors that were modeled were found to be in accordance with the data sheet. Table.1 compares the pre-rad values of the behaviors measured from the SPICE model with values provided in the data sheet.

Op Amp behaviors	SPICE model	Data Sheet			Unit
		Min	Typ	Max	
Input offset voltage	0.572		1	2	mV
Input bias current	28.2		20	50	nA
Input offset current	0.08		2	10	nA
Open loop gain	837	50	100		V/mV
Gain-bandwidth product	0.6		1		MHz
Output voltage swing	$(V_{DD} - V_{CC}) - 1.9$		$(V_{DD} - V_{CC}) - 1.5$		V

Table. 1 Comparison of values obtained from SPICE with data sheet

In the SPICE model, from the BJT model parameter (.MODEL) file, RB, ISE and IKF were chosen as the parameters that could be used to model the total dose degradation of the op amp. RB is the zero-bias base resistance of the transistor. ISE represents the base emitter leakage saturation current. IKF is the knee current used to model the drop in  $\beta$  due to high level injection. Changing the values of RB, ISE and IKF causes the change in  $\beta$  of the transistor. Total dose degradation was modeled using the first-order approximation of uniformly changing these parameter values in the transistor device models. The experimental results that are available from [40] were used to validate the results from the SPICE model.

Experimental results [40] are available for

- TID degradation of LM124 behaviors
- TID degradation of regulator output of voltage regulator using LM124 as the error amplifier

The TID degradation of the op amp behaviors of SPICE model was able to match the trend observed in the experimental results. The voltage regulator was built using the LM124 SPICE model. The SPICE model was able to accurately match degradation of voltage regulator output with the experimental results. Thus the SPICE model was validated for post-rad behaviors.

The characterization of the op amp model was performed independently in two parts: a pre-rad model and a post-rad model. The pre-rad model was built by incorporating the dependence of the op amp behaviors on the supply voltage and signal inputs via constructing and testing appropriate circuits using the SPICE model (or hardware tests if available). To obtain the dependence of behaviors with supply voltage, the behaviors were measured at the following 6 supply voltages:  $\pm 5V$ ,  $\pm 10V$ ,  $\pm 15V$ ,  $\pm 20V$ ,  $\pm 25V$ ,  $\pm 30V$ . Section 4.1 – 4.10 provides the results of these measurements.

Once the pre-rad behavioral model was developed, the next step was to capture the TID degradation of each of the op amp behavior. The dependence of op amp behaviors with TID was simulated using the SPICE model and appropriate basis functions were formulated. Thus, a TID aware behavioral model of LM124 was developed.

Since we know the pre-rad dependence of the parameters separately from TID dependence, the basis functions of the op amp behaviors are of the form:

$$\mathbf{Parameter} = \mathbf{f}(\mathbf{pre-rad}) [1 + \mathbf{g}(\mathbf{TID})] \quad (2)$$

Here the TID is assumed as an input parameter during the simulation and is known to the simulator at run-time. Since our experimental TID data set includes only a particular supply voltage ( $\pm 15V$ ) and temperature (300K), the amp behaviors under TID are assumed to scale with supply voltage and temperature with the same scaling as pre-rad. To include the degradation of

parameters due to TID under different supply voltages and temperatures (assuming a more complete data set is available) the same form of the basis function could be extended as

$$\text{Parameter} = f(\text{pre-rad}) [1 + g(\text{TID}, \text{Supply Voltage}, \text{Temperature})] \quad (3)$$

The form of some basis functions is directly related to the simulation speed; the simpler the function, the faster the simulator is able to resolve the function. Considering the trade-off between simplicity and the accuracy of simulation, a simple but reasonably accurate basis functions have been selected.

The following are the op amp behaviors that were implemented in the behavior model:

- Input Impedance
- Second Pole
- Input Offset Voltage
- Input Offset Current
- Input Bias Current
- Slew-rate Limiting
- Open Loop Gain
- Gain-bandwidth Product
- Miller Capacitance Effect
- Output Voltage Saturation
- Output Impedance

The modeling procedure used for each of the op amp behaviors is discussed below.

#### 4.1 Gain Bandwidth Product (GBW):

GBW is equal to the unity-gain frequency and is constant for a particular op amp. It not only tells us the upper useful frequency of a circuit, but allows us to determine the bandwidth for a given gain.

$$\text{GBW} = \text{gain} \times \text{bandwidth} = \text{unity-gain frequency.}$$

To measure the GBW of our op amp, the non-inverting amplifier configuration was used with a closed loop gain of 20 as shown in the fig. 9.

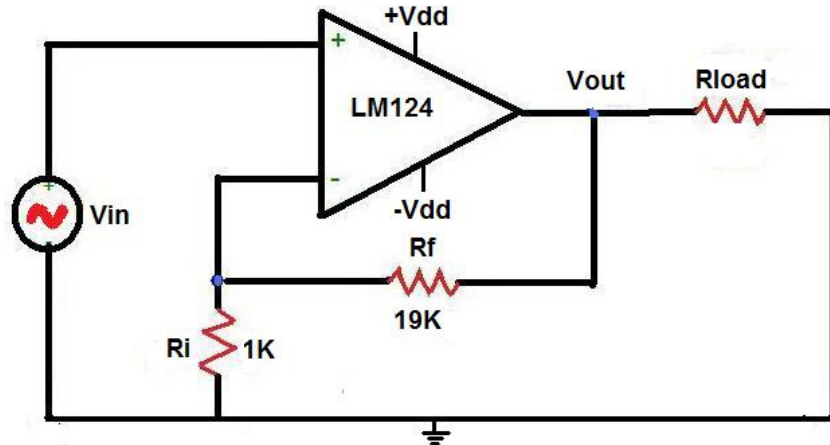


Fig. 9. Non-inverting op amp configuration with gain of 20 to measure GBW.

Fig. 10 shows the dependence of GBW with supply voltage ( $V_{\text{sup}}$ ) obtained from the SPICE model of LM124. GBW increases linearly with  $V_{\text{sup}}$ , hence the form of pre-rad basis function is:

$$\text{GBW (pre-rad)} = 26240V_{\text{sup}} + 313700 \quad (4)$$

From Fig. 11 we see that, initially the GBW falls off quickly with increase in total dose. As the total dose level increases the decrease in GBW becomes lesser (as seen from the decrease

in slope of the curve). This can be modeled using a log function, hence the form of the TID basis function is:

$$\text{GBW (TID)} = 545000[1 - 0.305185\text{Log}(1+ 9\text{TID})] \quad (5)$$

The final form of GBW is obtained as:

$$\text{GBW} = [\text{GBW (pre-rad)}] [1 + \text{GBW (TID)}] \quad (6)$$

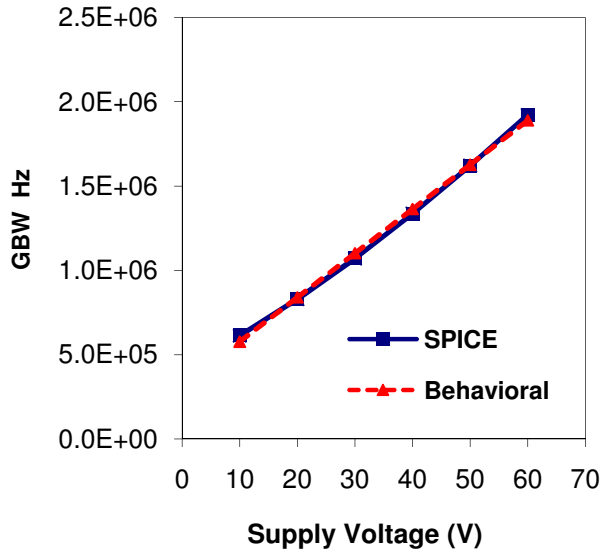


Fig. 10. Pre-rad dependence of GBW with supply voltage for SPICE and behavioral model.

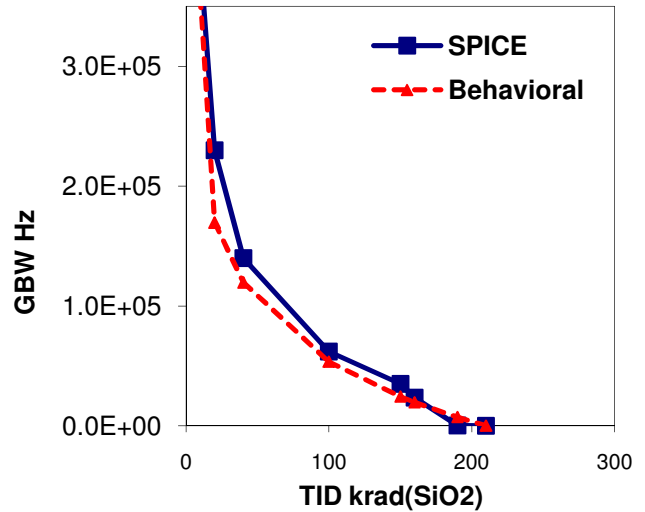


Fig. 11. Dependence of GBW with TID and for SPICE and behavioral model.

#### 4.2 Open Loop Gain ( $A_{vol}$ ):

Open loop gain is the ratio of the output voltage change to the input differential voltage change and it is dependent on the following parameters (quantities): differential input voltage ( $V_{indiff}$ ),  $V_{sup}$  and frequency of operation. This dependence of  $A_{vol}$  with  $V_{indiff}$  gives rise to the non-linearity in the model and is an important effect to be modeled.

$$A_{vol} = \partial V_{out} / \partial V_{in} \quad (7)$$

Open loop gain can be measured by applying a very small signal directly to the inputs of the op amp as shown in fig. 12. The input offset voltage normally will cause the output of the op amp to saturate, or lock-up at one of the power supply voltages when trying to measure open loop gain directly. Hence a dc sweep of the input voltage is done and corresponding output voltage is plotted. The first derivative of this output with respect to the input sweep is the open loop gain.

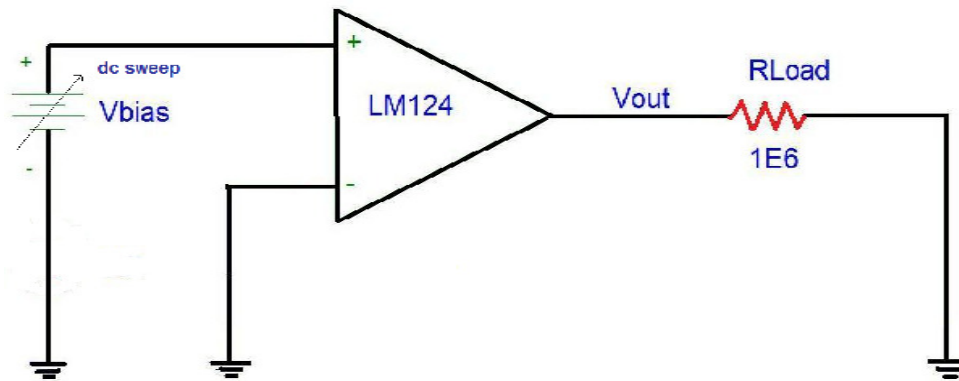


Fig. 12. To measure the open loop gain of op amp.

Fig. 13 shows the dependence of open loop gain with supply voltage ( $V_{sup}$ ) obtained from the SPICE model of LM124.  $A_{vol}$  increases linearly with both ( $V_{indiff}$ ) and  $V_{sup}$ , hence the form of pre-rad basis function is:

$$A_{vol}(\text{pre-rad}) = [(18550V_{sup} + 638500) - 10^{10} V_{indiff}] \quad (8)$$

From Fig. 14 we see that the open loop gain follows the trend observed with GBW. This can be modeled using a log function, hence the form of the TID basis function is:

$$A_{vol}(\text{TID}) = 837088.97 [1 - 0.11653 \text{Log}(1 + 2000000\text{TID})] \quad (9)$$

The final form of open loop gain is obtained as:

$$A_{vol} = [A_{vol} (\text{pre-rad})] [1 + A_{vol} (\text{TID})] \quad (10)$$

From the equation (9) we can see that when the value of TID is equal to 0 then we get the open loop gain of the pre-rad case.

From Figs. 13 and 14 we can see that the behavioral model corresponds well with the initial SPICE electrical model (less than 1% maximum error) and accurately predicts the TID degradation of the open loop gain to 5% maximum error. The percentage error method is used for the error calculations since we are measuring the accuracy of the behavioral model with respect to a known quantity (value from the SPICE model.)

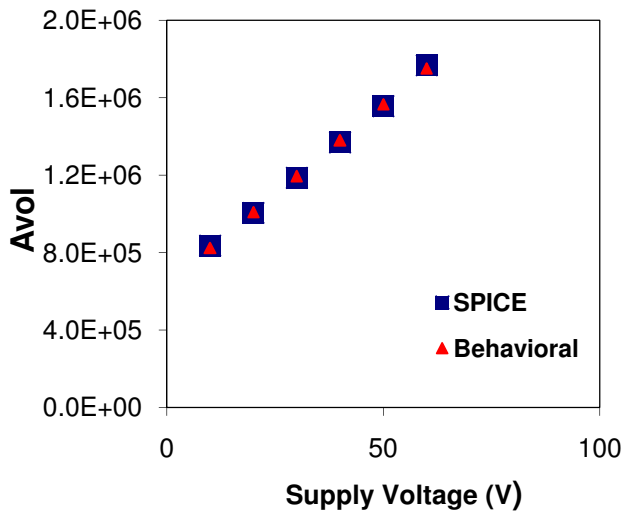


Fig. 13. Pre-rad dependence of  $A_{vol}$  with supply voltage for SPICE and behavioral model.

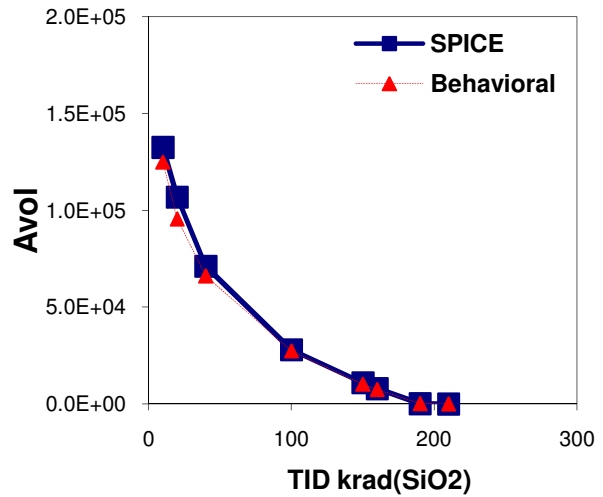


Fig. 14. Dependence of  $A_{vol}$  with TID and for SPICE and behavioral model.

### 4.3 Input Offset Voltage

The device mismatches present in the differential amplifier present in the input stage of the LM124 primarily causes the input offset voltage [41]. Even when both the inputs to the differential amplifiers are grounded there is a dc voltage  $V_o$  at the output of the op amp due to



disparity in the device parameters. The  $V_o$  is called the output dc offset voltage. If we divide  $V_o$  by the differential gain of the op amp,  $A_d$ , we obtain the quantity known as the input offset voltage.

$$V_{\text{off}} = V_o / A_d \quad (11)$$

Input offset voltage can be defined as the dc voltage that needs to be applied between the input terminals to cause 0V at the output. The op amp is connected in open loop configuration as shown in fig. 15. A dc sweep is done on the input voltage and the input voltage at which the output reaches 0V is determined as the offset voltage.

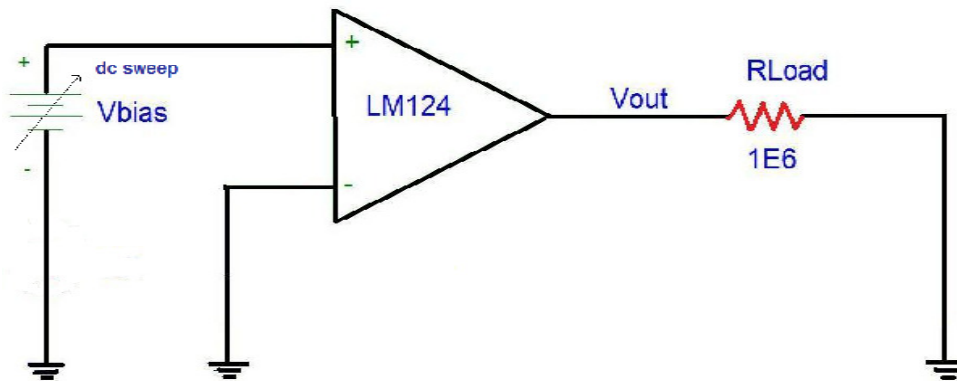


Fig. 15. To measure input offset voltage of op amp.

$V_{\text{offset}}$  is dependent on  $V_{\text{sup}}$  and the data obtained from the SPICE model of LM124 shows non-linear increase of offset voltage with  $V_{\text{sup}}$ . This dependence is best modeled by a quadratic function. Fig. 16 compares the offset voltage obtained from the SPICE model with the behavioral model.

$$V_{\text{off}}(\text{pre-rad}) = -9.107\text{E-}9V_{\text{sup}}^2 + 1.706\text{E-}6V_{\text{sup}} + 5.561\text{E-}4 \quad (12)$$

Fig. 17 shows the dependence of Offset voltage with TID. The offset voltage increases with TID until about 150 krad (SiO<sub>2</sub>) and then decreases to changes its polarity from positive to negative around. Combination of cubic equation with log function is used to model this.

$$V_{\text{off}}(\text{TID}) = 57\text{E-}6 [1+0.12\text{E-}3\text{TID}^3 + 0.025\text{TID}^2 - 0.85\text{TID} + 11.2 \text{Log} (1+\text{TID})] \quad (13)$$

The final form of offset voltage is obtained by as:

$$V_{\text{off}} = [V_{\text{off}}(\text{pre-rad})] [1 + V_{\text{off}}(\text{TID})] \quad (14)$$

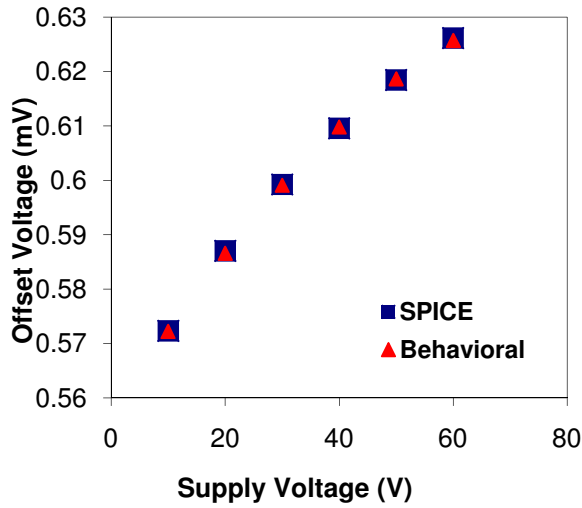


Fig. 16. Pre-rad dependence of  $V_{\text{off}}$  with supply voltage for SPICE and behavioral model.

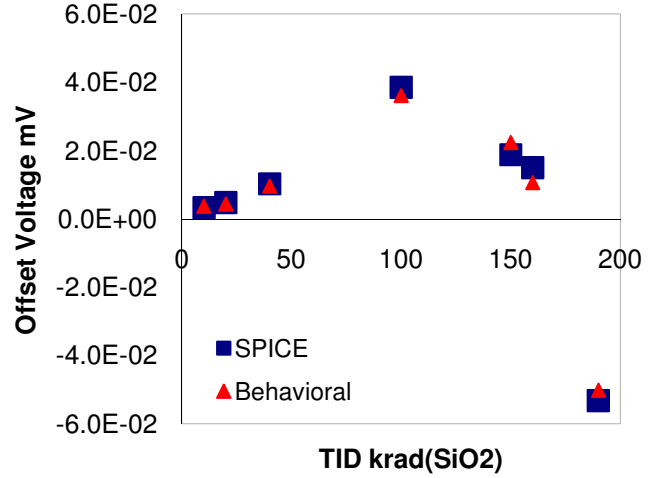


Fig. 17. Dependence of  $V_{\text{off}}$  with TID and for SPICE and behavioral model.

#### 4.4 Input Bias/Offset current

Theoretically, the input impedance is infinite; therefore, there should not be any input current into the op amp. However, there do exist, small input currents, of the order microamperes down to picoamperes. The average of these two currents (currents flowing through the input differential amplifier) is termed as the input bias current. This current causes an unbalance in the

op amp which can affect the output. Generally, the lower the input bias current, the smaller the imbalance will be. Op amps using BJTs generally have a higher input bias current than the FETs.

Both input currents should be equal to obtain zero output voltage. However, this is impossible; there will be an input offset current to maintain the output at zero volts. In other words, to set the output to zero volts, one input requires more current than the other. This may range from picoamperes to microamperes.

Fig. 19 shows the circuit used to measure the input bias and offset currents. The current flowing into the input differential amplifiers when the output voltage is 0V is noted as  $I_{b-}$  and  $I_{b+}$ . The input bias current ( $I_{bias}$ ) and input offset current ( $I_{offset}$ ) are calculated as follows:

$$I_{bias} = (I_{b+} + I_{b-}) / 2 \quad (15)$$

$$I_{offset} = I_{b+} - I_{b-} \quad (16)$$

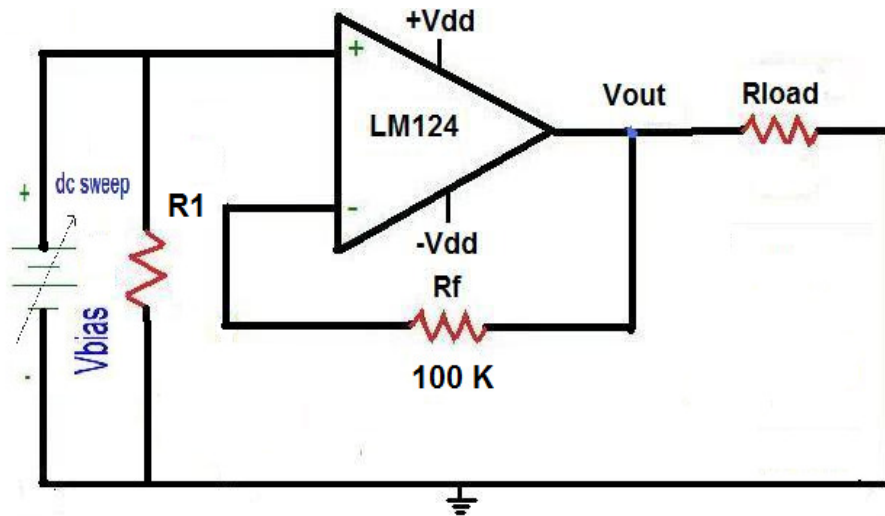


Fig. 18. To measure input bias/offset currents

Fig. 19 shows the dependence of  $I_{bias}$  with supply voltage ( $V_{sup}$ ) obtained from the SPICE model of LM124.  $I_{offset}$  was measured to be fairly constant with  $V_{sup}$ .  $I_{bias}$  increases linearly with  $V_{sup}$ , hence the form of pre-rad basis function is as given in (17):

$$I_{\text{bias}} (\text{pre-rad}) = (-0.1982\text{E-}9 V_{\text{sup}} - 0.12\text{E-}7) \quad (17)$$

$$I_{\text{offset}} (\text{pre-rad}) = 8.4\text{E-}11 \quad (18)$$

Fig. 20 shows the dependence of  $I_{\text{bias}}$  with TID.  $I_{\text{bias}}$  increases with TID and then saturates around 180 Krad ( $\text{SiO}_2$ ). This is modeled using a logarithmic function

$$I_{\text{bias}} (\text{TID}) = 282\text{E-}11 [1 + 209.678 \text{Log} (1 + 0.099\text{TID})] \quad (19)$$

The final form of offset voltage is obtained by combining (17) and (19):

$$I_{\text{bias}} = [I_{\text{bias}} (\text{pre-rad})] [1 + I_{\text{bias}} (\text{TID})] \quad (20)$$

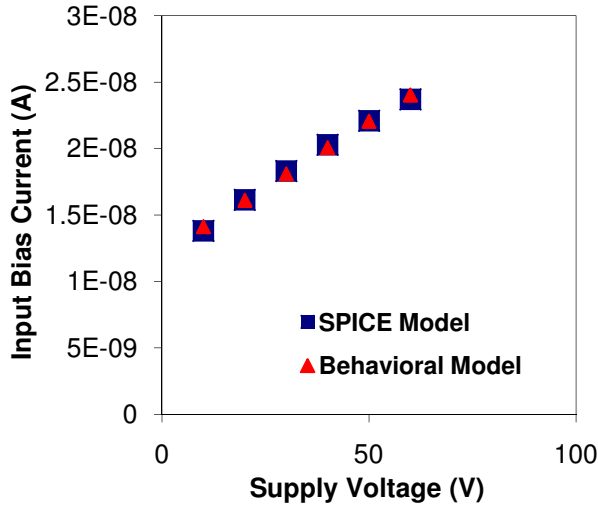


Fig. 19. Pre-rad dependence of  $I_{\text{bias}}$  with supply voltage for SPICE and behavioral model.

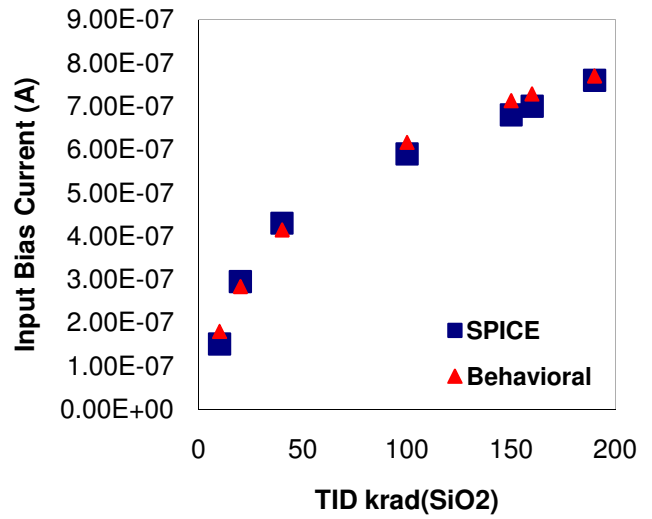


Fig. 20. Dependence of  $I_{\text{bias}}$  with TID and for SPICE and behavioral model.

#### 4.5 Maximum Output Voltage Swing ( $V_{\text{OM}}$ ):

The maximum output voltage swing is defined as the maximum positive or negative peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage

is zero. In an ideal op amp the output voltage can swing between V<sub>dd</sub> and V<sub>ee</sub> when operating with dual power supply (with supplies V<sub>dd</sub> and V<sub>ee</sub>) configuration and between 0V to V<sub>dd</sub> in single power supply (of V<sub>dd</sub>). However, the output voltage swing is limited by the output impedance of the amplifier, the saturation voltage of the output transistors and the power supply voltages.

The data obtained from the SPICE model of LM124 shows that the offset of V<sub>sat</sub> from V<sub>sup</sub> is relatively constant with V<sub>sup</sub>. The positive saturation voltage is about 1.35 V below V<sub>dd</sub> and negative saturation voltage is 0.65 V above V<sub>ee</sub>

$$V_{\max}(\text{pre-rad}) = V_{dd} - 1.4 \quad (21)$$

$$V_{\min}(\text{pre-rad}) = V_{ee} + 0.7 \quad (22)$$

$$V_{OM}(\text{pre-rad}) = V_{\max}(\text{pre-rad}) - V_{\min}(\text{pre-rad}) \quad (23)$$

Fig.21 shows the dependence of V<sub>OM</sub> with TID. It stays relatively constant at low TID levels and falls of steeply at higher TID levels. This behavior could be modeled by using either a log function or a polynomial function. For the sake of simplicity and hence better speed of simulation, the quadratic function is chosen.

$$V_{\max}(\text{TID}) = 4.35 (1 - 18E-4\text{TID}^2 + 665E-4\text{TID}) \quad (24)$$

$$V_{\min}(\text{TID}) = -3.65 (1 - 16E-4\text{TID}^2 + 665E-4\text{TID}) \quad (25)$$

$$V_{OM}(\text{TID}) = V_{\max}(\text{TID}) - V_{\min}(\text{TID}) \quad (26)$$

The final form of the maximum output voltage equation is written by combining (23) and (26)

$$V_{OM} = [V_{OM}(\text{pre-rad})] [1 + V_{OM}(\text{TID})] \quad (27)$$

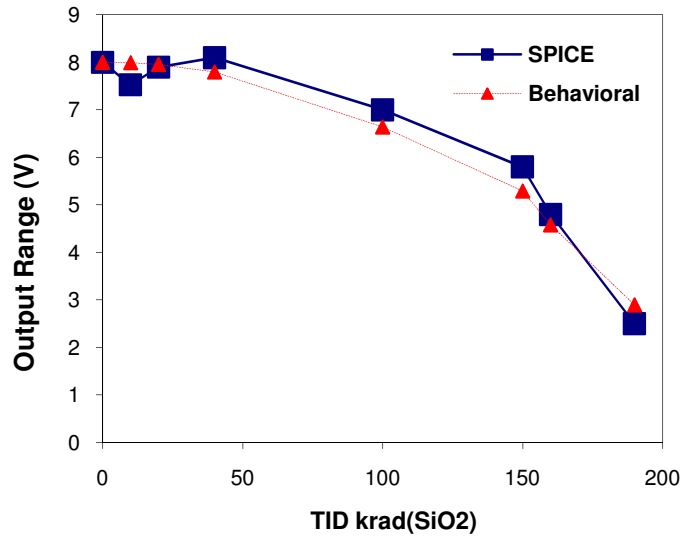


Fig. 21. Dependence of output range ( $V_{OM}$ ) with TID and for SPICE and behavioral model.

#### 4.6 Slew Rate Limiting

Slew rate is the maximum rate of change of the op amp output voltage and can be stated thus

$$\text{Slew rate} = \frac{\text{maximum change in output voltage}}{\text{Change in time}} = \frac{\Delta V_{\text{out}} (\text{max})}{\Delta t}$$

The slew rate of LM124 from the SPICE model is determined to be around  $0.5 \text{ V}/\mu\text{s}$  which means that the output voltage can change a maximum of  $0.5\text{V}$  in  $1 \mu\text{s}$ . Capacitance limits this slewing ability and the output voltage will be delayed from the input voltage. Most often, the frequency compensation capacitor (Mille capacitor  $CC$ ) causes the slew rate limiting in an op amp. at high frequencies or high rates of signal change, slew-rate limiting becomes more pronounced. Slew-rate limiting is a large-signal performance parameter. Slew rate is usually specified at unity gain. Op amps with higher slew rates have wider bandwidths.

Fig. 22 shows the circuit used to measure the slew rate. The ratio of  $dV/dT$  is the slew rate of the op amp.

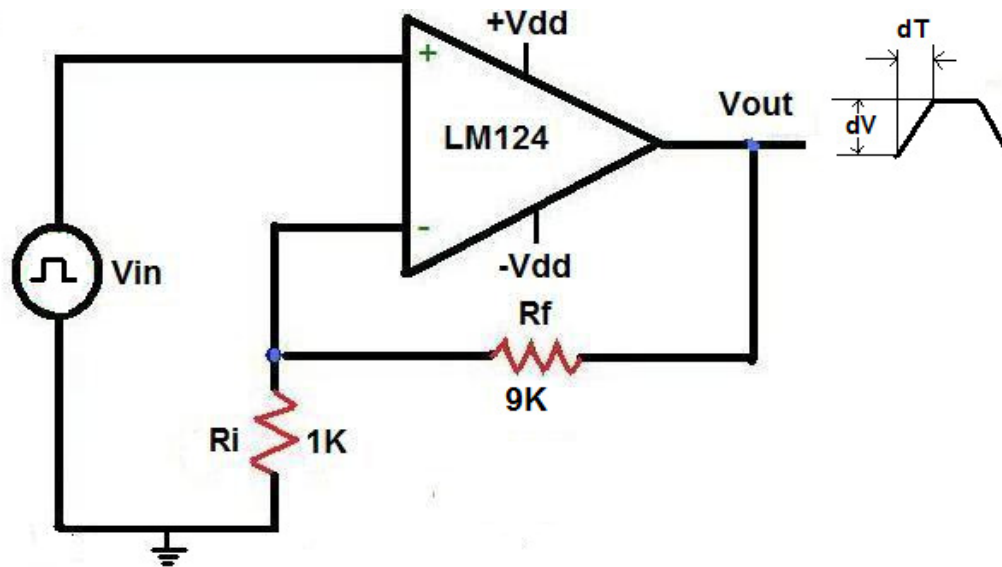


Fig. 22. To measure slew rate of the op amp

Fig. 23 shows the dependence of slew rate with supply voltage ( $V_{sup}$ ) obtained from the SPICE model of LM124. It increases linearly with  $V_{sup}$ , hence the form of pre-rad basis function is:

$$\text{Slew rate (pre-rad)} = (5632V_{sup} + 130000) \quad (28)$$

Fig.24 shows the dependence of slew limit with TID. It decreases exponentially with the TID and hence a exponential functions is chosen to model it.

$$\text{Slew rate (TID)} = 200000(e^{(-0.066TID+3.089E-4TID^2)}) \quad (29)$$

The final form of the maximum output voltage equation is written by combining (28) and (29)

$$\text{Slew rate} = [\text{Slew rate (pre-rad)}] \times [1 + \text{Slew rate (TID)}] \quad (30)$$

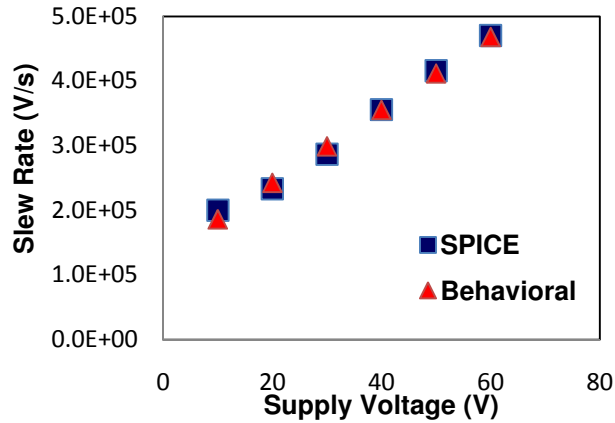


Fig. 23. Dependence of slew rate with supply voltage for SPICE and behavioral model.

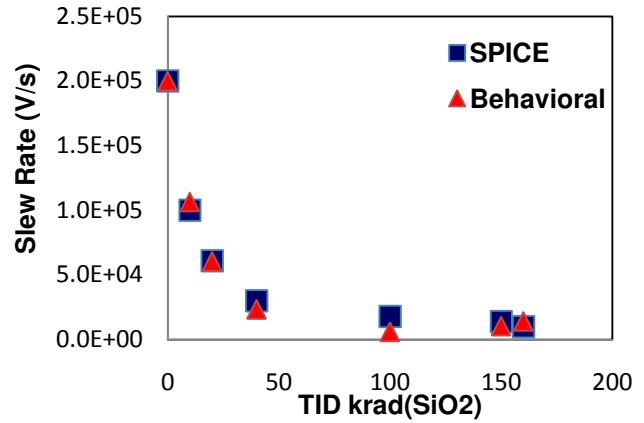


Fig. 24. Dependence of slew rate with TID and for SPICE and behavioral model.

#### 4.7 Miller Pole

Op amps generally have at least two poles associated with them. In a feedback configuration, an unfortunate consequence of this is that at some critical frequency, the phase of the amplifier's output equals  $-180^\circ$  compared to the phase of its input signal. The amplifier will oscillate if it has a gain greater than or equal to 1 at this critical frequency. This is because of two reasons:

- The feedback is implemented through the use of an inverting input that adds an additional  $-180^\circ$  to the output phase making the total phase shift  $-360^\circ$
- The gain is sufficient to induce oscillation ( $\text{gain} \geq 1$ ).

Hence the 2 main conditions for an op amp to oscillate at the frequency at which its open loop gain equals its closed loop gain if, at that frequency,

- The open loop gain of the amplifier is  $\geq 1$  and



- The difference between the phase of the open loop signal and phase response of the network creating the closed loop output =  $-180^\circ$ .

One technique used to avoid such a situation is to use Miller capacitance  $CC$  to introduce a new pole at sufficiently low frequency. From the SPICE netlist of the LM124 it is observed that there is a Miller compensation capacitor  $CC$  of 7 pF connected in the negative-feedback path of the second stage. The effect of  $CC$  on the frequency response of LM124 was simulated and it was observed that the dominant pole was located at around 3 Hz. Since  $CC$  and GBW are related to each other, modeling the GBW implements  $CC$  in the behavioral model.

The following behaviors are not dependent on supply voltages and hence are modeled as constants.

#### **4.8 Second Pole**

Apart from the dominant, low frequency pole introduced by the Miller capacitance, there are other non-dominant high frequency poles due to the parasitic capacitance in the op amp circuit. It is important to model these to preserve the important high frequency behaviors. Also, it has to be noted that it is not available in the data sheets provided by the vendor and hence has to be determined from the op amp.

Frequency analysis on the SPICE model showed that the op amp had two poles at high frequencies around 6 MHz and 14 GHz. Since op amps are almost never used at high frequencies such as GHz, only the pole at 6 MHz is modeled.

## 4.9 Input impedance

Ideally, the input impedance  $Z_{in}$  of an op amp should be infinite, but in practice it is about  $1\text{M}\Omega$  or more. The higher the input impedance the better the op amp would perform. This input capacitance of an op amp may become important at higher frequencies. Typically the capacitance is less than  $5\text{ pF}$ .

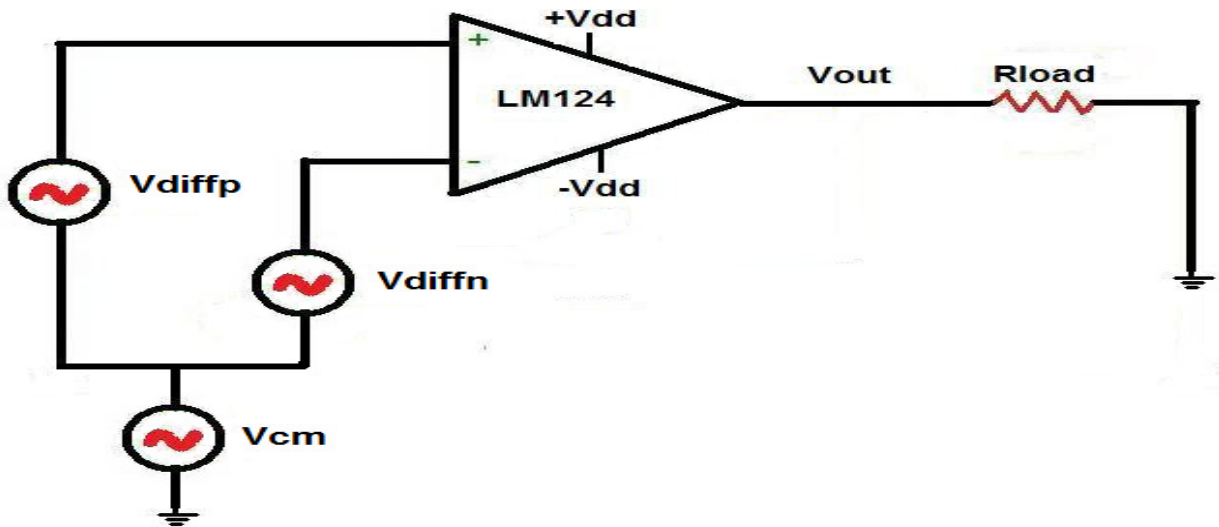


Fig. 25. To measure input impedance

Input impedance is constant with supply voltage but changes with frequency. The input impedance of the behavioral model represents the frequency dependant impedances seen by the differential mode input signal and the common mode input signal. These are two separate impedances, the differential mode input impedance and the common mode input impedance and is implemented using RC ladder networks. From the frequency analysis of the circuit in fig. 25, the number and location of poles and zeroes is determined from the SPICE model. RC network is constructed to match the number and location of poles and zeroes. This RC network is used to model the input impedance of the op amp. The following RC network in fig. 26 matches the input impedance of the SPICE model with less than 1%

percent error. The terminals  $V_{i\_nonInv}$  and  $V_{i\_Inv}$  are connected to the non-inverting and inverting terminal of the op amp

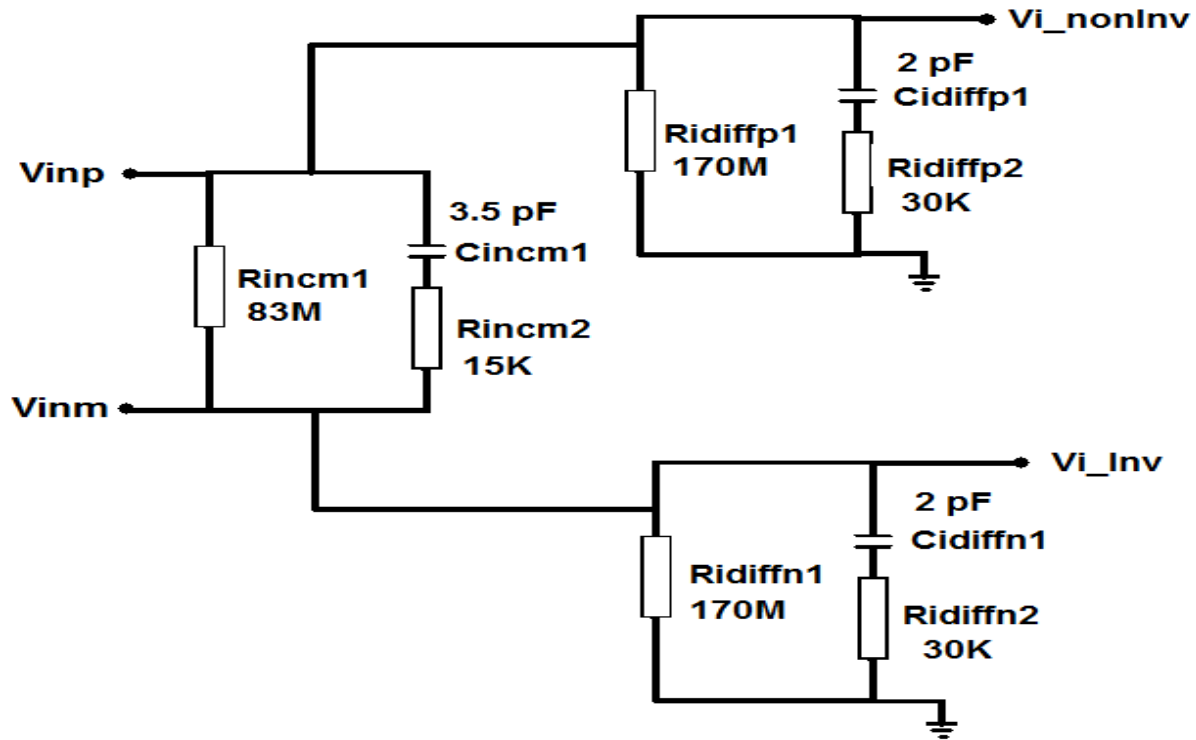


Fig. 26. RC network to model input impedance

#### 4.10 Output Impedance:

Ideally the output impedance of the op amp should be zero. In actuality, each op amp is different and its output impedance may range from 10 to several thousand ohms. The actual output impedance  $Z_o$  of the op amp network is dependent on the loop gain of the op amp circuit. The op amp is usually connected in close loop configuration which means that the feedback resistor is in parallel to the output impedance. For most applications, the output is assumed to be zero and will function as a voltage source capable of providing current for a wide range of loads.

The output impedance of the op amp was measured to be around 12  $\Omega$  and increases linearly with supply voltage as seen from fig. 27.

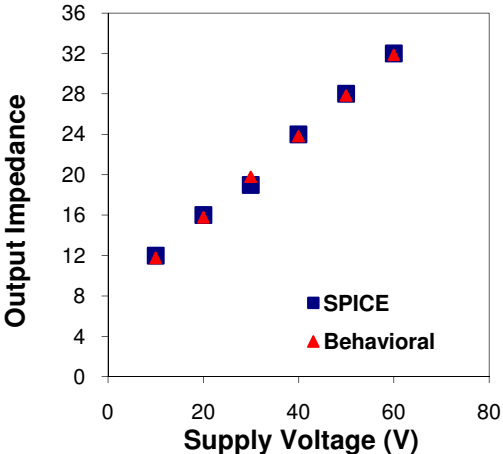


Fig. 27. Dependence of output impedance of op amp with supply voltage for SPICE and behavioral model.

## CHAPTER V

### 5 APPLICATION OF THE BEHAVIORAL MODEL

To test the validity and the accuracy of the behavioral modeling technique, the VHDL-AMS behavioral model for our LM124 op amp was used in the following circuits

- As an error amplifier in the feedback loop of a series voltage regulator (Fig. 29).
- As an inverting amplifier configuration in a Schmitt trigger relaxation oscillator

#### 5.1 Linear Voltage Regulator

The linear voltage regulator is basic the building block of nearly every power supply used in electronics. Every electronic circuit is designed to operate at some supply voltage, which is usually assumed to be constant. A voltage regulator provides this constant dc output voltage and contains circuitry that continuously holds the output voltage at the design value regardless of changes in load current or input voltage (this assumes that the load current and input voltage are within the specifies operating range for the part).

The linear regulator operates by using a voltage-controlled current source to force a fixed voltage to appear at the regulator output terminal. Fig. 27 shows the functional diagram of the regulator circuit. The control circuitry must monitor (sense) the output voltage, and adjust the current source, as required by the load, to hold the output value at the desired value. The design limit of the current source defines the maximum load current the regulator can source and still maintain regulation.

The output voltage is controlled using a feedback loop, which requires some type of compensation to assure loop stability. The behavioral model of the op amp developed was used as the sense/control device used for regulation operation.

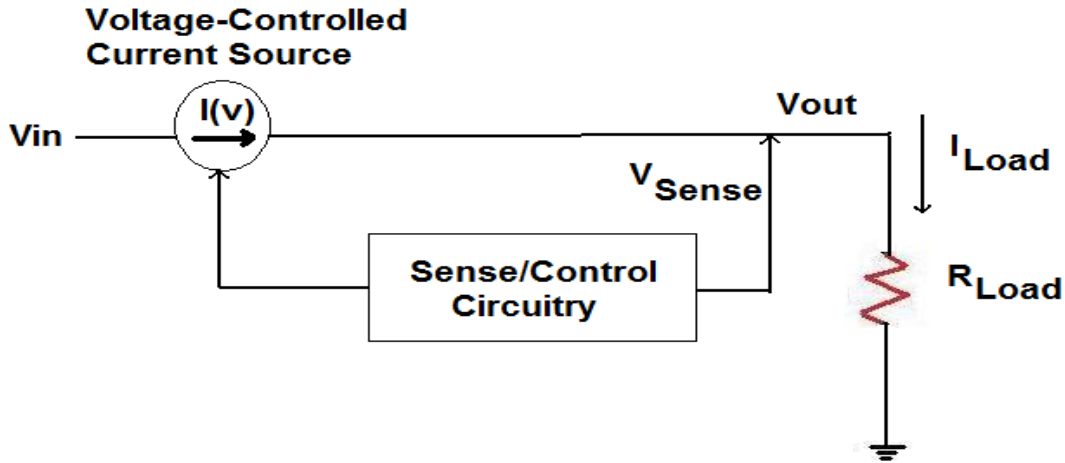


Fig. 28. Linear voltage regulator functional diagram

Fig. 29 shows the schematic of regulator circuit used. Basic operation of the linear regulator circuit is as follows. Transistor Q1 is the output series pass element while Q2 and  $R_e$  control the base current of Q1. The current flowing out of the emitter of Q1 is controlled by Q2 and the error amplifier. The current through R1 and R2 is negligible compared to the load current  $I_{Load}$ .

The feedback loop which controls the output voltage is obtained by using R1 and R2 to sense the output voltage, and applying this sensed voltage to the inverting input of the voltage error amplifier. The non-inverting input is tied to a reference voltage of 2.5 V, which means the error amplifier will constantly adjust its output voltage (and the current through Q1) to force the voltages at its inputs to be equal. Note that the op amp is connected in a non-inverting

configuration with a gain of 2, causing the output voltage to be 5V. The feedback loop action continuously holds the regulated output at 5V regardless of changes in load current.

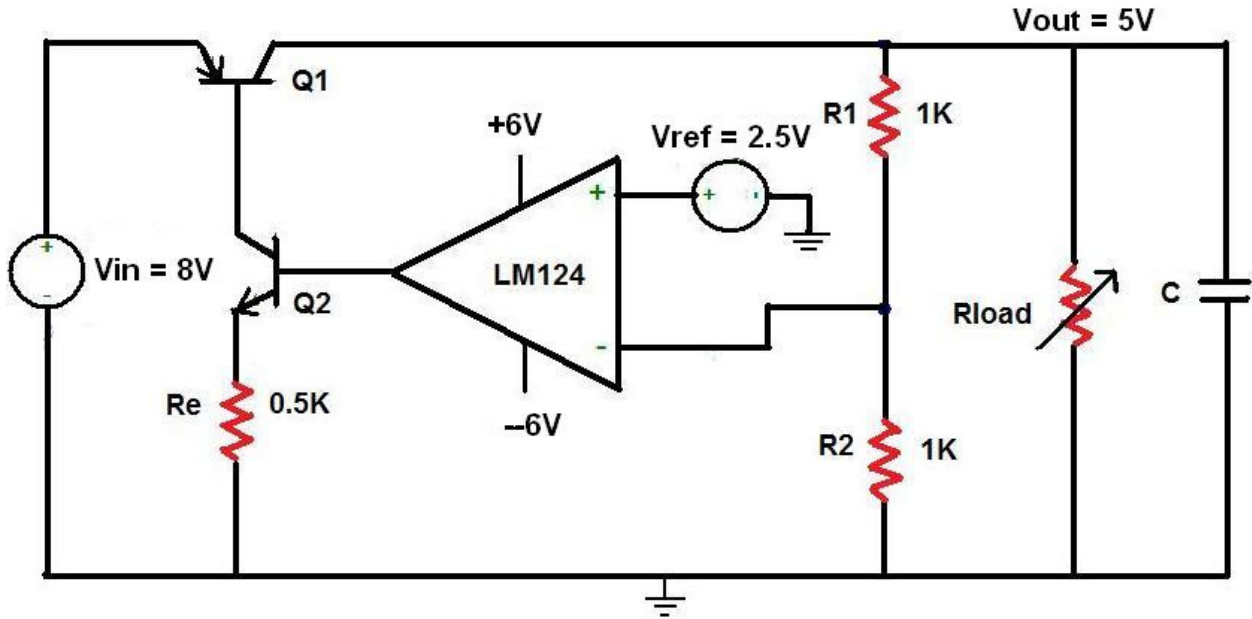


Fig. 29. Schematic of linear regulator circuit

It has been shown that the regulator output degrades significantly with TID due to the performance degradation of the LM124 [35]. Simulation results were compared to experimental observations from a linear regulator constructed using National Semiconductor LM-124 IC devices and discrete components, and tested at Vanderbilt University using an ARACOR 10keV X-ray source.

During TID exposure, the regulator output was observed at various TID levels. Fig.30 compares the results of the behavioral model predictions and the TID experiment. The regulator output voltage slowly decreased with increasing ionizing dose, from a pre-rad condition of 5V to about 4.8V at 210 krad ( $SiO_2$ ). Beyond 210 krad ( $SiO_2$ ), the output decreases steeply with increasing dose. At 225 krad ( $SiO_2$ ), the output voltage is reduced to 0V. As we can see from the figure, the behavioral model agrees well with the experimental results - the maximum deviation

was calculated as 4.4% (percentage error method used). Also note that even though the behavioral model TID dependence was characterized at supply voltages  $\pm 5V$ , the results shows that the model is able to match the response of the circuit at  $\pm 6V$ . This confirms that the scaling of macro behaviors with supply voltage have been well captured in the model.

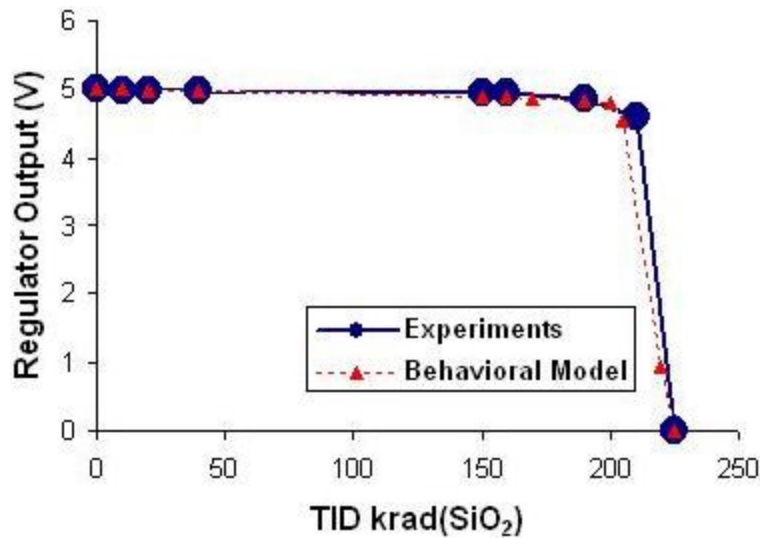


Fig. 30. Regulator output degradation due to TID radiation. The experimental results are from [40].

## 5.2 Schmitt Trigger Relaxation Oscillator

Op amps can be wired to serve as signal generators capable of a variety of output waveforms. A simple op amp square-wave generator is shown in Fig. 31. Its output repetitively swings between positive saturation  $V_{OMAX}$  and negative saturation  $-V_{OMIN}$ , resulting in square waveform output. The time period of oscillation  $T$  of each cycle is determined by the time constant of the components  $R$  and  $C$  and by the voltage divider formed by  $R_a$  and  $R_b$ .

This circuit operation can be analyzed as follows:

At the instant the dc supply voltages,  $V_{dd}$  and  $-V_{dd}$  are applied, zero volts of initially uncharged capacitor is applied to the inverting input 1, that is, input 1 is grounded. At the same



instant, however, a small positive or negative voltage  $V_b$  appears across  $R_b$ , and this voltage is applied to the non-inverting input 2. Voltage  $V_b$  initially appears because a positive or negative offset voltage  $V_{off}$  exists, even if no differential input voltage is applied to inputs 1 and 2. Since the inverting input 1 is initially grounded through the uncharged capacitor  $C$ , all of the voltage  $V_b$  initially appears across the inputs 1 and 2. If we assume that the offset voltage is positive, then the voltage  $V_b$  at the non-inverting input 2 is also positive. This  $V_b$  is initially amplified by the op amp's open loop gain,  $A_{vol}$  and drives the output to its limit,  $V_{OMAX}$ , that is, to positive saturation. The rise to  $V_{OMAX}$  is at the slew rate of the op amp. The resistors  $R_a$  and  $R_b$  form a voltage divider, a fraction of the op amp's output voltage is dropped across  $R_b$ . This voltage is given by  $\lambda V_{OMAX}$ , where  $\lambda = R_b/(R_a+R_b)$ .

With the op amp saturated, the capacitor charges through the resistor  $R$ . If the resistor  $R$  and  $C$  formed a simple RC circuit, the capacitor's voltage  $V_c$  would eventually rise to  $V_{OMAX}$ . In this case, however, the voltage  $V_c$  can rise to a value slightly more positive than  $\lambda V_{OMAX}$ . That is, as  $V_c$  becomes a little more positive than  $\lambda V_{OMAX}$ , the inverting input 1 becomes more positive than non-inverting input 2, driving the output to negative saturation  $-V_{OMIN}$ . After the op amp's output saturates at  $-V_{OMIN}$ , a fraction of this is dropped across  $R_b$ . Thus input 2 becomes much more negative than input 1 and holds the op amp in negative saturation, at least for a while. The capacitor  $C$  now starts to discharge. Now when capacitor's voltage  $V_c$  becomes a little more negative than  $-V_b$ , then the output is driven back to  $V_{OMAX}$  to start another cycle.

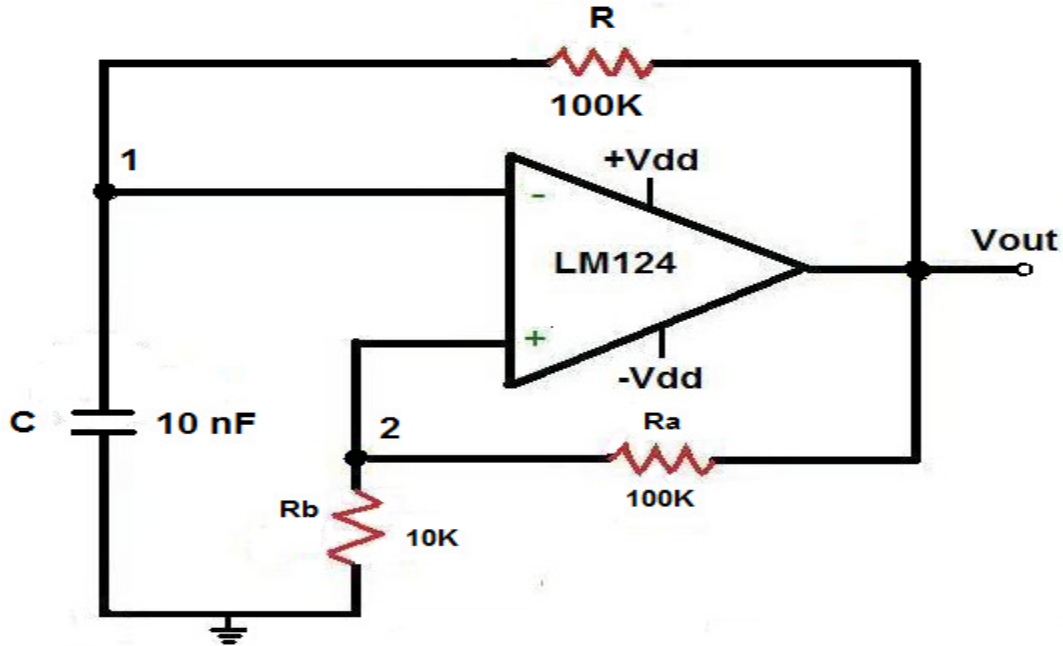


Fig. 31. Schmitt Trigger Relaxation Oscillator

To determine the time period of oscillation:

When  $V_1$  reaches  $\lambda V_{OMAX}$  then the switch to  $-V_{OMIN}$  occurs at the output. The capacitor that has charged to  $\lambda CV_{OMAX}$  begins to discharge. The general charging equation for a capacitor which already has an original charge is:

$$Q = CV [1 - \exp(-t/RC)] + Q_0 \exp(-t/RC) \quad (31)$$

Here  $V = -V_{OMIN}$  and  $Q_0 = \lambda CV_{OMAX}$ . Hence the equation becomes

$$Q = -CV_{OMIN} [1 - \exp(-t/RC)] + \lambda CV_{OMAX} \exp(-t/RC) \quad (32)$$

Now when  $Q$  gets to  $-\lambda CV_{OMIN}$  another switch would occur. This time is half the time period of the square wave, so it is represented by  $T/2$ . At this time

$$-\lambda CV_{OMIN} = -CV_{OMIN} [1 - \exp(-T/2RC)] + \lambda CV_{OMAX} \exp(-T/2RC) \quad (33)$$

Solving this equation for  $T$  gives

$$T = 2RC \ln[(1+\lambda)/(1-\lambda)] \quad (34)$$

Substituting  $R = 100 \text{ K}\Omega$ ,  $C = 10 \text{ nF}$ ,  $R_a = 100 \text{ K}\Omega$  and  $R_b = 10 \text{ K}\Omega$  we get

$$T = 3.65 \times 10^{-4} \text{ s and } f_0 = 2.74 \text{ KHz}$$

The circuit was constructed and simulated using the SPICE model and the behavioral model for pre-rad case and also at different TID levels with  $\pm 5\text{V}$  power supplies. The frequency of oscillation,  $f_0$  decreases with increase in TID and the oscillation stops at around 190 Krad ( $\text{SiO}_2$ ). The behavioral model agrees well with the SPICE model with maximum error less than 5.8%. Table 2 compares the frequency of oscillation of the 2 models.

<b>TID</b> <b>krad (<math>\text{SiO}_2</math>)</b>	<b><math>f_0</math> of SPICE Model</b> <b><math>f_{\text{OSP}}</math> (Hz)</b>	<b><math>f_0</math> of Behavioral Model</b> <b><math>f_{\text{OBM}}</math> (Hz)</b>	<b>%Error</b> <b><math>[(f_{\text{OBM}} - f_{\text{OSP}})/f_{\text{OSP}}] \times 100</math></b>
0 (Pre-rad )	1834.86239	1785.71429	-2.75
20	1402.52454	1379.31034	-1.68
40	1016.26016	1000.00000	-1.62
150	714.28571	675.67568	-5.71
160	549.45055	526.31579	-4.39
190	No Oscillation	No Oscillation	0

Table 2. Comparison of  $f_0$  between SPICE and behavioral model

Fig. 32 shows the plot of  $f_0$  versus TID for SPICE and behavioral model. We can see that the behavioral model matches well with the SPICE results.

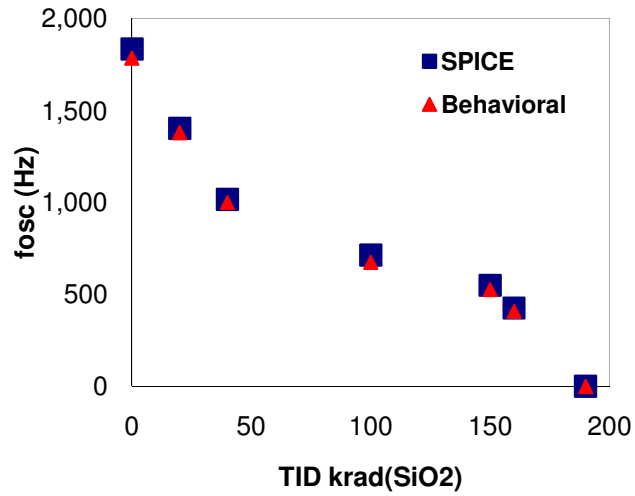


Fig. 32. Comparison of  $f_0$  between SPICE and behavioral model

### 5.3 Simulation Speed and Accuracy

Fig. 33 shows the square wave output of the SPICE and behavioral model. Both the simulation are run for 50 cycles. The SPICE simulation is run at default simulation error and the behavioral model is run at the maximum allowable simulation error, consistent with a good match to SPICE results.

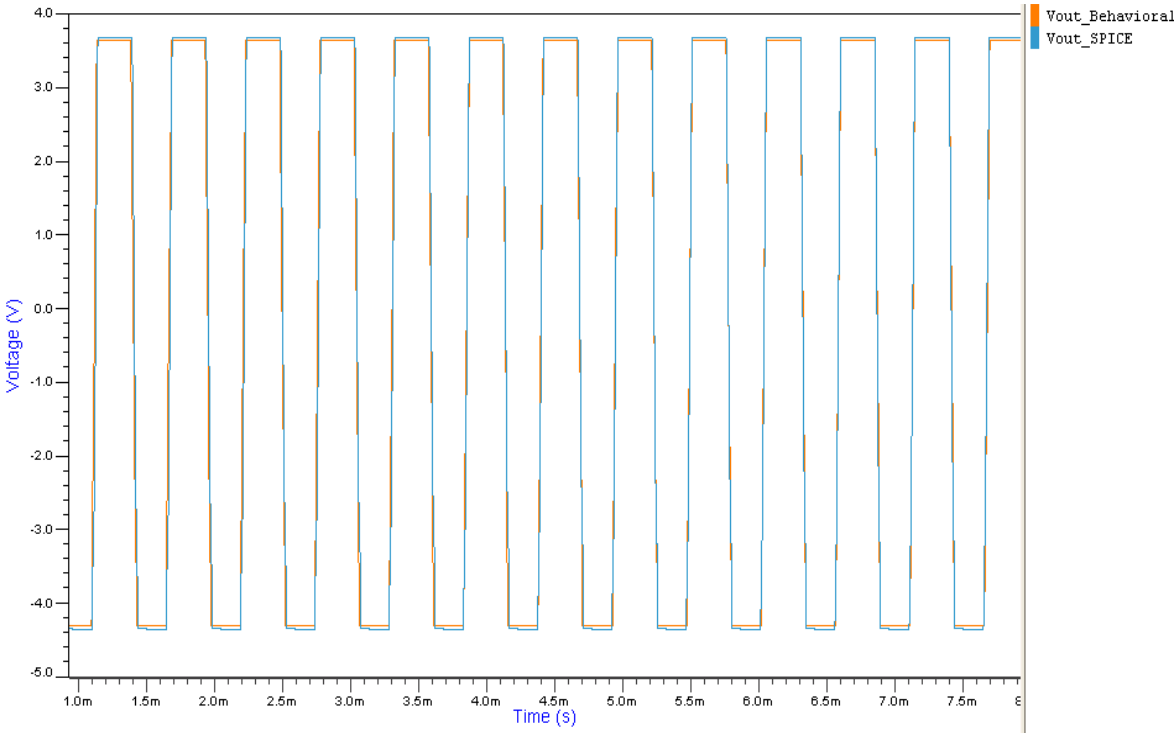


Fig. 33. Square wave output of SPICE and behavioral model.

<b>Simulation parameter</b>	<b>SPICE Model</b>	<b>Behavioral Model</b>
Memory size allocated	419705 bytes	290023 bytes
# of components	135	17
# of nodes	111	9
# of steps computed	22688	2441
Simulation time	402s 7ms	5s 9ms

Table 3. Comparison of simulation parameters for Schmitt trigger circuit for SPICE and behavioral model

Table 3 describes the simulation details obtained from the simulator. We can see that the number of components and nodes for the same oscillator circuit is drastically reduced in the case of the behavioral model. Also the simulation ran faster in the case of behavioral model by a factor of **79X**.

## CHAPTER V

### 6 CONCLUSION

A behavioral model of the LM124 op-amp was developed which captures the total ionizing dose characteristics of important macro behaviors with a high degree of accuracy. The maximum deviation of the behavioral model from a detailed, transistor-level SPICE model was 6% over all the behaviors modeled. The simulation of a voltage regulator circuit using this VHDL-AMS behavioral model for the LM124 op-amp resulted in accurate prediction of TID-induced failure. The simulation of a Schmitt trigger relaxation oscillator circuit using the behavioral model shows that they are much faster than SPICE while still achieving good simulation accuracy. A factor of **79X** increase in speed was obtained in the behavioral model when compared to the SPICE model. Also, a single continuous simulation could ideally cover the entire circuit response from normal electrical operation (pre-irradiation or pre-rad) to post-irradiation performance at different exposure levels to assess system failure or to qualify radiation tolerance.

This modeling technique demonstrates that if a rich data set is available from experiments, the resource-intensive construction of a transistor-level SPICE model can be bypassed. In addition, the behavioral model can be used to capture the essential behaviors of the op amp within a larger system simulation, without carrying the computational overhead of a full transistor-level, SPICE-like model.

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