ENHANCED DEFECT GENERATION IN GATE OXIDES OF P-CHANNEL MOS TRANSISTORS IN THE PRESENCE OF WATER

By

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CHAPTER I

INTRODUCTION

Low frequency noise is a major problem in analog circuits since it sets a limit on the magnitude of signals that can be detected and processed. $1/f$ noise ("one-over-f noise," occasionally called "flicker noise" or "pink noise") is a type of noise whose power spectral density as a function of the frequency f behaves like: $S(f) = 1/f^{\alpha}$, where the exponent α is very close to unity. $1/f$ noise deserves the often-used attribute, "ubiquitous;" it appears in widely different systems such as chemical systems, biology, fluid dynamics, astronomy, electronic devices, optical systems, network traffic and economics [1].

The subject of this work is low frequency noise in metal-oxide-semiconductor (MOS) field effect transistors. Ever since flicker noise in vacuum tubes was discovered by Johnson in 1925, it was found in a great variety of other components and devices. During the past 25 years, it has been demonstrated that the low frequency current noise of semiconductors and metals can be very sensitive to defects. For example, in a MOS transistor, the random capture and emission of charge carriers by traps at or near the Si/SiO_2 interface [2] can lead to fluctuations in the number of charge carriers in the device channel, and in the channel mobility, and thus to current noise. There is much evidence that the dominant current noise of MOS transistors is associated with defects that are very similar to those responsible for radiation-induced oxide trapped charge or interface traps in MOS structures [3,4,5,6].

Hydrogen or moisture present in ambient gases used during device fabrication has been correlated with radiation-induced charge buildup in both MOS and bipolar devices [7,8,9,10,11,12]. This can have a significant impact on device radiation hardness since devices exposed to hydrogen over long periods of time may be susceptible to increased radiation-induced degradation. The radiation response of devices exposed to humidity is important from the long term aging point of view, since such devices operate in systems

that require them to function in high radiation environments (e.g., in space) after long term storage.

This work discusses the effects of hydrogen/moisture exposure on radiation-induced charge buildup in MOS transistors. Non-hermetically sealed MOS devices were exposed to hydrogen using Highly Accelerated Stress Tests (HAST) and irradiated using a 10 keV x-ray source. Transistors were mainly characterized by two techniques: low frequency ($1/f$) noise measurements and current-voltage (I-V) measurements. N-channel and P-channel MOS transistors manufactured using Sandia National Laboratories' 4/3-μm technology are studied.

The remainder of this thesis is organized into five chapters. Chapter II discusses the mathematical background and physical origins of $1/f$ noise. Chapter III describes the $1/f$ noise measurement system and the equipment configurations. In Chapter IV, the results of I-V measurements on the devices that underwent HAST and control transistors are discussed. Chapter V discusses the results of low frequency noise measurements on the MOS transistors that underwent HAST treatment and control transistors that did not, and also discusses the mechanisms responsible for these observed effects. Chapter VI presents conclusions and recommendations for future work.

CHAPTER II

LOW FREQUENCY (1/*f*) NOISE IN MOS TRANSISTORS

In this chapter, low frequency noise in MOS transistors is discussed. We start with a brief mathematical introduction to the basic theory of noise. This is followed by a discussion of the physical origin of low frequency noise in MOSFET transistors.

Mathematical Background:

Noise in an electronic device is a random, spontaneous perturbation of a signal inherent to the physics of the device. Noise cannot be eliminated completely, but it is possible to reduce it by proper design of devices and circuits.

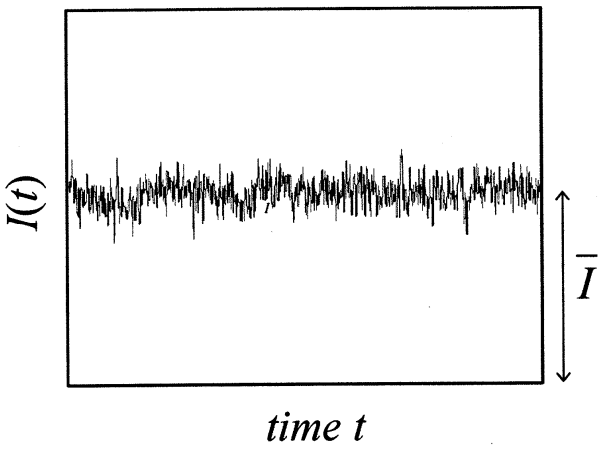

Figure 1. A typical noise waveform is illustrated [1].

Figure 1 illustrates how an electronic signal fluctuates randomly due to noise. The current through the device can be written as

$$I(t) = \bar{I} + i_n(t), \tag{1}$$

where $\bar{I}$ is the average bias current and $i_n(t)$ is a randomly fluctuating current [13]. The value of $i_n(t)$ is random at any point in time and cannot be predicted. Instead, noise is described with averages; the average of $i_n(t)$ measured over a long time is always (by definition) equal to zero. The study of noise is built on the mathematical methods from probability theory, which allows us to define appropriate averages for the random variables to describe the magnitude of the fluctuations of the signal around its mean level of zero.

A common and powerful method to characterize and describe noise is by converting the problem from the time domain to the frequency domain by Fourier transformation. At a given time, there is a probability dP that the wanted signal will be disturbed by noise with an amplitude in the interval [X, X+dX], where X is a random variable. One can define a probability density function f(X) of X and write

$$dP = f(X)dX\,. \tag{2}$$

If f(X) is independent of time, the random process is said to be stationary. For random variables, several ensemble averages are defined. The mean value and variance are defined as:

$$\begin{aligned} \bar{X} &= \int_{-\infty}^{+\infty} Xf(X)dX \\ \operatorname{var} X &= \overline{\left(X-\bar{X}\right)^2} = \int_{-\infty}^{+\infty}\left(X-\bar{X}\right)^2 f(X)dX = \overline{X^2} - (\bar{X})^2 \end{aligned} \tag{3}$$

The ensemble averages can be calculated using the probability density function. Practically all fluctuating currents and voltages in electrical devices follow the normal (Gaussian) distribution due to the central limit theorem, which states that the sum of a large number of independent random variables has a normal distribution. The probability density function for the normal distribution is given as

$$f(X) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{(X-m)^2}{2\sigma^2} \right] \tag{4}$$

where $\overline{X} = m, \operatorname{var} X = \sigma^2$.

Because the time average of noise voltage or noise current equals zero if integrated long enough, squared quantities typically are used to describe the noise. One such squared quantity is the power spectral density S(*f*), which is given from the autocorrelation function R(s) according to the Wiener-Khintchine theorem [14,15]:

$$S(f) = 4\int_0^\infty R(s)\cos(2\pi fs)ds \tag{5}$$

S is the Fourier transform of R(s), which is given by

$$\begin{aligned} R(s) &= \overline{X(t)X(t+s)} = \lim_{T->\infty} \frac{1}{T}\int_0^T X(t)X(t+s)dt \\ R(s) &= \int_0^\infty S(f)\cos(2\pi fs)df \end{aligned} \tag{6}$$

Obviously, if s = 0 one obtains the noise "power"

$$\overline{X^2(t)} = \int_0^\infty S(f)df = \lim_{T->\infty} \frac{1}{T}\int_0^T X^2(t)dt \tag{7}$$

The power spectral density (PSD) is measured with a spectrum analyzer. 1/*f* noise is a type of noise whose power spectral density $S(f) \sim 1/f^{\alpha}$, where the exponent α is very close to unity. Noise with constant *S*(*f*) for all frequencies is said to be white. It is usually observed that the noise PSD depends on frequency at low frequencies, and becomes white at high frequencies. The low frequency noise may consist of superimposed 1/*f* like noise and generation-recombination (g-r) noise in case of semiconductor devices.

1/*f* Noise in MOSFETs:

The low frequency noise generated in electronic devices is a key problem in analog circuits and systems since it sets a limit on the lower end of the amplitude range of signals that can be detected and processed in the circuits. Since MOS transistors are used in a wide range of digital and analog circuits, the low frequency noise of CMOS devices is an important concern.

The origin of 1/*f* noise in MOS transistors has been debated for several decades. In particular, there has been a longstanding debate whether number fluctuation noise due to traps in the gate oxide or bulk mobility fluctuations dominate the 1/*f* noise. The drain current in a MOSFET is confined to a narrow surface channel under the gate oxide. The current transport is sensitive to traps at the interface. Number fluctuations are generally believed to be the dominant 1/*f* noise mechanism in n-channel MOSFETs. However, many authors have considered the mobility fluctuation noise model to be a better explanation of the 1/*f* noise in pMOS transistors. A wide range of studies has been performed in an attempt to determine the dominant source of noise in MOS transistors [16,17,18,19,20], as we now discuss.

Number Fluctuations:

In 1957, A.L. McWhorter [21] presented a 1/*f* noise model based on tunneling transitions between channel electrons and traps in the gate oxide [21]. The oxide traps dynamically exchange carriers with the channel causing a fluctuation in the surface potential, giving rise to fluctuations in the inversion charge density. The fluctuating oxide charge density is equivalent to a variation in the flat-band voltage. The tunneling time varies exponentially with distance, thus the required distribution of time constants to produce 1/*f* noise is obtained for a trap density that is uniform in both energy and distance from the channel interface. The McWhorter model is well known for its simplicity and general agreement with experiments. We will use this model in this thesis to analyze the noise. Other popular models, including the bulk mobility fluctuation model that was developed

by Hooge and Vandamme [22] and criticized effectively by Weissman [13], will not be discussed.

Figure 2 demonstrates how in a MOS transistor, the near-interface traps interact with the carriers in the conducting channel, and the capture and emission of carriers can lead to fluctuations of both the number and the mobility of the carriers. The mobility fluctuations shown here are the result of the different scattering rates of charged and uncharged traps, and not the bulk mobility fluctuations described by Hooge and Vandamme. For simplicity, we neglect the contributions of these mobility fluctuations to the (larger) number fluctuations [2,13], when we parameterize the noise.

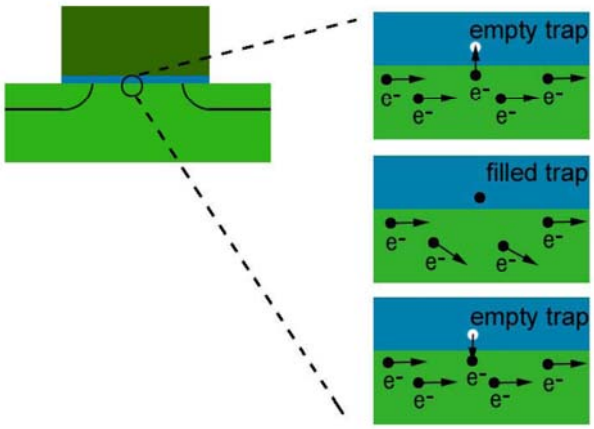

Figure 2. 1/*f* noise is generated when carriers interact with traps in the near-interfacial oxide.

Figure 3 shows a log-log plot of a typical measured drain voltage noise spectrum S_{Vd} versus frequency for an unirradiated device. The figure shows two separate drain voltage noise spectra with a zero bias current, which is the background noise. The background noise spectrum is mainly due to random thermal motion of the charge carriers in the channel, preamplifier noise, and 60 Hz line frequencies. The upper trace was measured for an average drain voltage of 100 mV. The traces shown represent raw data. The background noise was subtracted from the curves before calculating the frequency exponent α. The resulting expression is:

$$S_{Vd}(f) = S_{Vd}(f, \mathrm{Id}) - S_{Vd}(f, 0) \quad (8)$$

Background noise is due to interfering electromagnetic signals, which consist of time dependent electric and magnetic fields that can have a wide range of frequencies. The "spikes" at 60 Hz and its multiples are caused by the power line fundamental and higher harmonics. The background noise data were excluded from calculations of α.

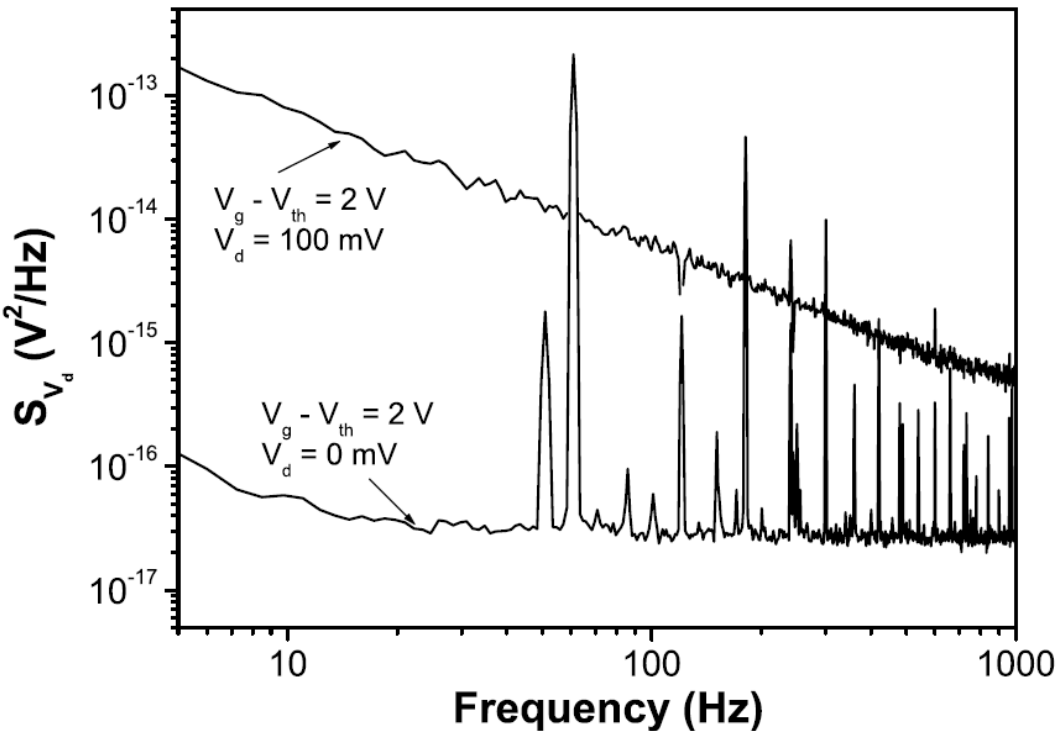

Figure 3. 1/*f* noise power spectral density for an unirradiated n-channel transistor.

When a n-MOSFET is operated in the linear region in strong inversion, the number fluctuation model gives [2]:

$$S_{V_d}(f) = \frac{K}{f^{\alpha}} \frac{V_d^2}{(V_g - V_{th})^2} \quad . \quad (9)$$

K is the "noise level" of the device. K has units of V^2, and corresponds to the room temperature value of S_{Vd} at any frequency for $V_d = 1$ V and $V_g - V_t = 1$ V.

In the simple trapping model developed by Christenson, Lundstrom, and Svensson (CLS) [17], traps are assumed to exist in the oxide, uniformly distributed in energy and in space. Charge carriers tunnel in and out of these traps with a probability that decreases exponentially with distance into the oxide. The spatial distribution of traps results in a distribution of trap times, and a corresponding frequency spectrum for the excess noise [23],

$$S_{V_d}(f) = \frac{q^2}{(LWC_{ox})^2} \frac{V_d^2}{f(V_g - V_{th})^2} \frac{k_B T L W D_t(E_F)}{\ln(t_{\max} / t_{\min})} \tag{10}$$

Here S_{Vd} is the excess drain voltage noise power spectral density (after correction for background noise), V_{th} is the threshold voltage, and V_g and V_d are the gate and drain voltages during the noise measurement. C_{ox} is the oxide capacitance per unit area, $D_t(E_F)$ is the oxide trap density per unit energy per unit area at the trap quasi-Fermi level E_F, and L and W are the transistor channel length and width, respectively. Also, q is the magnitude of the electronic charge, k_B is the Boltzmann constant, and t_{min} and t_{max} are the minimum and maximum tunneling times, respectively. The above spectrum is valid at frequencies $1/ t_{max} < f < 1/ t_{min}$. The noise level K can be correlated to the oxide trap charge density by [23]:

$$K = \frac{q^2 k_B T t_{OX}^2 D_{ot}(E)}{LW\varepsilon_{OX}^2 \ln(\frac{t_{\max}}{t_{\min}})} \tag{11}$$

Here $D_{ot}(E)$ is the areal oxide trap density; t_{OX} is the oxide thickness; *and* ε_{OX} is the dielectric constant of SiO_2.

Total Ionizing Dose (TID) Effects:

MOS transistors form integral components of numerous digital and analog circuits used in spacecraft that are exposed to high ionizing radiation environments in space. The MOS oxides are most vulnerable to damage by such radiation. This affects the current-voltage characteristics of the MOS transistors. As we have seen above, the low-frequency noise in MOS devices is due to interaction of charge carriers in the channel with traps in the oxide, so as more traps are created by radiation, the low frequency noise characteristics will also change. Figure 4 [24] shows a schematic energy band diagram of a MOS structure, where positive bias is applied to the gate, so that electrons accumulate at the silicon/silicon dioxide interface under the gate, forming an inversion layer, and the region of the substrate near the interface is depleted of holes. There are four major physical processes that contribute to the total-ionizing-dose radiation response of a MOS device [24]. They are:

(1) Electron/hole pairs generated by ionizing radiation.
(2) Hopping transport of holes through localized states in the SiO_2 bulk.
(3) Deep hole trapping near the Si/SiO_2 interface.
(4) Formation of radiation-induced interface traps within Si band gap.

The most sensitive parts of a system to the long-term effects of ionizing radiation are the oxide insulators. When radiation (10 keV x-rays from an ARACOR source in our case) passes through a gate oxide, electron/hole pairs are created by the deposited energy. In SiO_2, the electrons are much more mobile than the holes, and they are swept out of the oxide typically in picoseconds for large positive biases at room temperature. Some fraction of the electrons and holes will recombine depending on the energy and type of the incident particle [24].

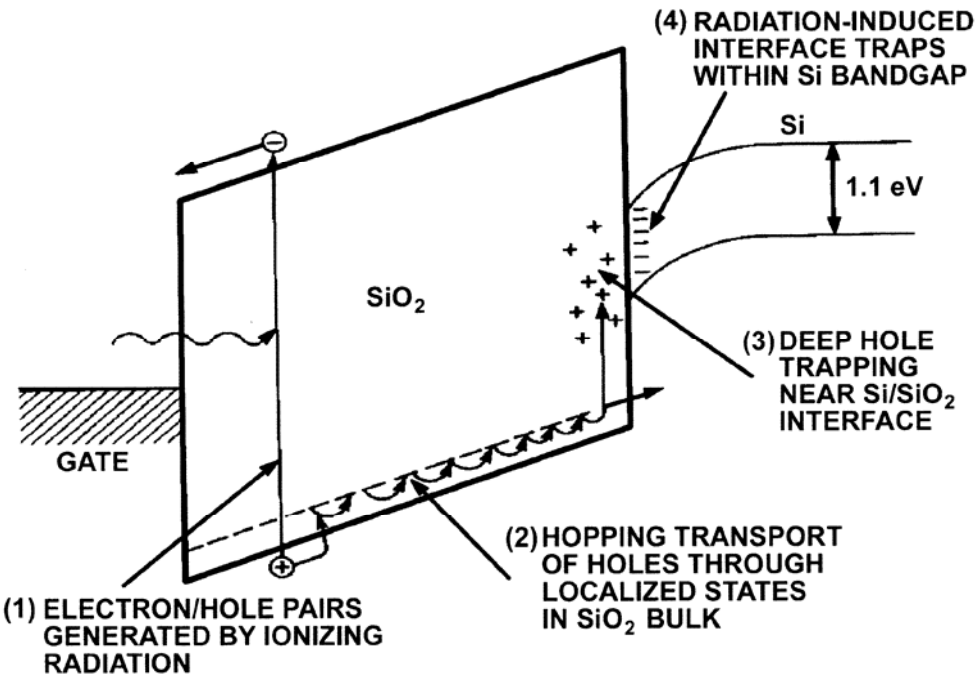

Figure 4. Schematic energy band diagram for a MOS structure, indicating major physical processes underlying radiation response [24].

The second process in Figure 4 is the transport of the holes to the Si/SiO_2 interface. This process is dispersive, meaning that it takes place over many decades in time [24]. The third process in Figure 3 is that, when the holes reach the Si interface, some fall into relatively deep trap states with long characteristic emission times [24]. The fourth major component of MOS radiation response is the buildup of interface traps at the Si/SiO_2 interface [24]. These traps are localized states with energy levels in the Si band gap.

Oxide Traps (ΔN_{ot}):

A primary oxide defect in SiO_2, which leads to hole trapping, is known as an *E'* center, which is associated with an oxygen vacancy. It is identified as a trivalent silicon atom with an unpaired electron, back-bonded to three other oxygen atoms [25,26,27]. These positively charged defects cause the threshold voltage to shift negatively. This causes nMOS devices to be turned on at lower voltages, while increasing the magnitude of voltage necessary to turn on pMOS devices.

Interface Traps (ΔN_{it}):

Interface trap formation was described as a two-stage process by McLean [10]. He proposed that during the first stage, the radiation-generated holes free hydrogen ions in the SiO_2 bulk. In the second stage, these protons undergo dispersive hopping transport to the interface. When they reach the interface, they react, and break the SiH bonds already there, forming H_2 and a trivalent Si defect [10]. In most MOS devices, interface traps above the midgap energy of Si are acceptor-like, while those in the lower half of the band gap are donor-like. Including both the donor-like and acceptor-like traps, the interface traps are charge neutral when the surface potential is at midgap [26].

Border Traps:

The term "border traps" was first introduced by D. M. Fleetwood in 1992 [28]. They are described as near-interfacial oxide traps that are able to exchange charge with the underlying silicon on the time scale of the measurements. The location of these traps is very close to the interface and their response to the electrical sweep can make them look like slow interface traps [3,29,30].

Hydrogen and Moisture:

Hydrogen plays a key role in radiation-induced charge buildup in MOS devices [7]–[10]. Hence, the presence of hydrogenous species can have a significant impact on device radiation hardness. In this work, we have studied the effects of humidity exposure at elevated temperatures on radiation induced charge build-up in oxides of MOS transistors by current voltage measurements and low-frequency noise measurements, as will be discussed in the following sections of this thesis.

CHAPTER III

EXPERIMENTAL SET-UP AND MEASUREMENTS

Devices Under Test:

The MOS transistors under test were manufactured in the 1980s using Sandia's 4/3-μm technology [31] and came from two different process lots, G1916A and G1928A. The devices from G1916A were taken from wafers 10 and 21, and those from G1928A were taken from wafers 16 and 28. Wafer 21 devices have a gate oxide thickness of 32 nm; wafer 10 transistors have an oxide thickness of 37 nm. The poly-Si was doped n+ with P by phosphene diffusion at 900 ^{o}C, after deposition. After polysilicon deposition, the G1916A transistors received a 30-minute, 1100 °C N_2 post-oxidation anneal. This anneal is known to create numerous oxygen vacancies in the oxide [32,33]. Wafer 16 devices have an oxide thickness of 25 nm; wafer 28 devices have an oxide thickness of 68 nm. Phosphorus doped glass was used for the final passivation layer for these transistors [34]. These devices experienced a full CMOS manufacturing flow. Sandia's 4/3-μm technology uses p+ guard bands for transistor isolation. For this technology, radiation induced charge buildup in the gate oxides normally dominates the radiation response. The MOS transistors used in this study have dimensions L = (3.45 ± 0.10) μm and W = (16 ± 0.5) μm.

We have classified the transistors used in this study into four different groups (Groups A, B, C and D) based on their wafer number and processing lots (and hence their oxide thicknesses). Devices from these four different groups were studied in order to identify the similarities and dissimilarities, if any. The four groups are described in Table 1.

TABLE I:

Device groups:	Wafer No.	Lot No.	Gate Oxide thickness (t_{ox}) (nm)
A	21	G1916A	32
B	10	G1916A	37
C	16	G1928A	68.2
D	28	G1928A	25.4

The I-V measurements and the 1/*f* noise measurements in this work were made on n-channel and p-channel transistors belonging to the four device groups.

Highly Accelerated Stress Test Experiments:

In this study, the effects of hydrogen/moisture on radiation induced charge buildup are studied by exposing the MOS devices to moisture or hydrogen at elevated temperatures using Highly Accelerated Stress Test (HAST) experiments. The HAST exposures were performed on MOSFETs with all pins shorted at 85% relative humidity at a temperature of 130 °C, for times up to 3 weeks. There were two types of devices, one non-hermetically sealed (or de-lidded) and exposed to HAST, described as "Exposed" in this study, and the others were hermetically sealed and not exposed to HAST. These were used as controls in this study. These devices were then irradiated with a 10 keV x-ray source. Some of these devices were then also subjected to long term anneal at room temperature.

The transistors were characterized both before ["Pre"] and after ["Post"] irradiation for both controls and the HAST exposed devices. All the transistors were characterized by two techniques:

(A) I-V measurements

(B) Low frequency 1/*f* noise measurements

1. Current-Voltage Measurements:

(a) I_D-V_G Measurements

For a MOS transistor operating in the linear region, the drain current is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_G - V_{th} - \frac{V_D}{2})V_D] \tag{12}$$

All the device terminals are connected to the four SMUs of an Agilent 4156B semiconductor parameter analyzer. In order to extract threshold voltage, V_T, for the MOSFETs, the drain bias is kept constant at ±0.1 V (depending on n-channel or p-channel transistor), whereas the gate bias is swept from below threshold to inversion in small steps. The threshold voltage can be extracted by drawing a tangent to the linear part of the I_D-V_G curve using the parameter analyzer. The intercept that this tangent makes at the V_G axis is then corrected by $V_D/2$ to obtain the threshold voltage. After extracting the pre-irradiation threshold voltage values for both the control and the humidity exposed transistors, the MOSFETs were characterized by 1/*f* noise measurements. Then some of them were irradiated using an ARACOR Model 4100 10-keV X-ray irradiator at a dose rate of about 31 krad(SiO_2)/min to study how the oxide traps and interface traps that were created change the low-frequency noise characteristics and the current-voltage characteristics of the MOS transistors. The shifts in threshold voltages due to oxide traps and interface traps can be determined using charge-separation techniques as described below.

(b) Charge Separation Techniques:

The midgap method [35, 36] is used to separate the overall radiation response of a device or test structure into its components due to oxide trapped charge and charged interface traps:

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \tag{13}$$

where the right-hand terms are the threshold voltage shifts due to oxide trapped charge and interface traps, respectively. Since the interface traps are net neutral at midgap, ΔV_{MG} is a measure of oxide hole trapping:

$$\Delta V_{MG} = \Delta V_{ot} = -q\ \Delta N_{ot} / C_{ox.} \tag{14}$$

Here, C_{ox} is the oxide capacitance per unit area and ΔN_{ot} is the areal density of oxide traps, projected to the Si/SiO_2 interface. The shift due to interface traps is:

$$\Delta V_{it} = \Delta V_{th} - \Delta V_{MG}. \tag{15}$$

The midgap method requires the extrapolation of the subthreshold region of the *I-V* curve down to the midgap current. The subthreshold current for a MOSFET [36] is given by:

$$I_d = \sqrt{2} C_m (qN_a L_D / \beta)(n_i / N_a)^2 \exp(\beta\phi_s)(\beta\phi_s)^{-1/2}. \tag{16}$$

Here ϕ_s is the band bending at the surface, given by $\phi_s = (kT/q)ln(N_a/n_i)$ at midgap, N_a is the channel doping, n_i is the intrinsic carrier concentration, L_D is the Debye length, $\beta = q/kT$ and $C_m = \mu_{eff}(W/2L)$, where μ_{eff} is the effective mobility. The Debye length is defined as

$$L_D = [\varepsilon_s / (\beta q N_a)]^{1/2}, \tag{17}$$

Here ε_s is the permittivity of silicon. The effective mobility is defined as

$$\mu_{eff} = \frac{I_D L}{C_{ox} W (V_G - V_{th}) V_D} \tag{18}$$

Using these values, the midgap current is determined and the *I-V* curve is extrapolated to where it intersects the midgap current to get V_{MG}.

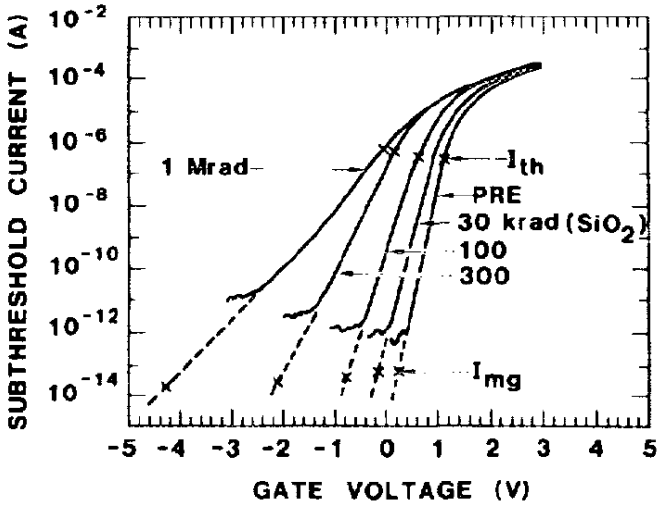

Figure 5. An illustration of the midgap method. Subthreshold current curves are shown before irradiation and also after each dose. The midgap and threshold currents are marked on each curve [36].

2. Low Frequency Noise Experiments:

The noise measurements were performed with MOSFETs operated in their linear regimes with both the source and the substrate at ground. The 1/*f* noise measurement circuit is shown in Figure 6. The drain current I_D was measured with a constant voltage source V_A in series with a resistor R_B. The value of R_B was 20 kΩ in our circuit. A second constant voltage source V_B was connected directly to the gate, $V_B = V_G$. The two voltages V_A and V_B were supplied by a Hewlett Packard (HP) model 4140A constant voltage source/picoammeter. In this work, typical bias across the drain is 100 mV and the gate is biased such that $V_G - V_{th} = 1$ V unless stated otherwise.

The drain voltage fluctuations were amplified with a Stanford Research (SR560) low noise preamplifier with a voltage gain of 10^2. The drain to source voltage was AC

coupled to a Stanford SR560 low noise preamplifier since V_{ds} can be very low and the fluctuation of the drain-source voltage is too small to measure directly. The low-pass filter of the preamplifier was set to 0.3 Hz. For a measurement bandwidth of 1 kHz, the high-pass filter of the preamplifier was set to around 1 kHz. The preamplifier was connected to a Stanford Research (SR760) spectrum analyzer. The spectrum analyzer converts the time domain signal to a power spectral density in the frequency domain.

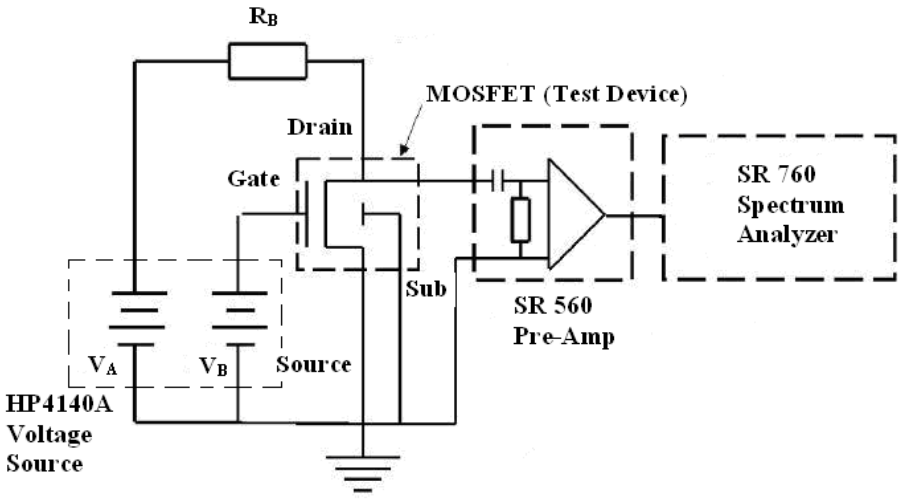

Figure 6. 1/*f* noise measuring circuit diagram.

Most equipment in this system is connected to the general purpose instrument bus (GPIB) controller; these include the SR 760 spectrum analyzer, HP 4140 voltage source, and HP 3478A digital multimeter. Codes were written in C language to send commands to each piece of equipment through a GPIB-ENET controller. An example of the control source code can be seen in Appendix A.

CHAPTER IV

CURRENT-VOLTAGE MEASUREMENT RESULTS

I-V Measurement Results:

Figure 7 plots the radiation-induced voltage shift due to interface traps, ΔV_{it} , and oxide trapped charge, ΔV_{ot} for 3 μm gate length control and HAST-exposed G1916A n-channel transistors during irradiation and long term room temperature anneal phases. These devices have a gate oxide thickness of 32 nm (Group A). The 3-week HAST exposures were performed to investigate the effects of long-term exposures to moisture. The transistors were first subjected to a HAST exposure for 1 or 3 weeks (with all pins grounded), irradiated to a total dose of 500 krad(SiO_2), and then annealed at room temperature for times up to 5 x 10^6 s. After HAST exposure before irradiation, there is increase in S_{Vd} value by almost an order of magnitude in p-channel transistors which can be correlated to oxygen vacancies in SiO_2. The transistors were irradiated and annealed post irradiation with a gate to source bias of V_G = 4 V. The hermetically sealed control devices were not exposed to HAST but irradiated and annealed under the same conditions as for the HAST exposed transistors. After irradiation to 500 krad(SiO_2) (time = 900 s), ΔV_{it} is 0.87 V and ΔV_{ot} is –1.2 V. At around 3 x 10^5 s, ΔV_{it} begins to increase during the later stages of room temperature anneal for both 1-week and 3-week HAST exposures. After 5 x 10^6 s, ΔV_{it} increased to ~1.8 V. There was a much smaller increase in ΔV_{it} for the control transistors. Some increase is observed for interface-trap buildup after a long term anneal [37]. ΔV_{ot} was similar for all devices for the first 10^5 s. After that, during the later stage of room-temperature annealing, ΔV_{ot} begins to increase in magnitude for the 3-week HAST-exposed transistors. The increase in ΔV_{ot} in 3-week HAST-exposed transistors is greater compared to the 1-week HAST transistors and the control transistors.

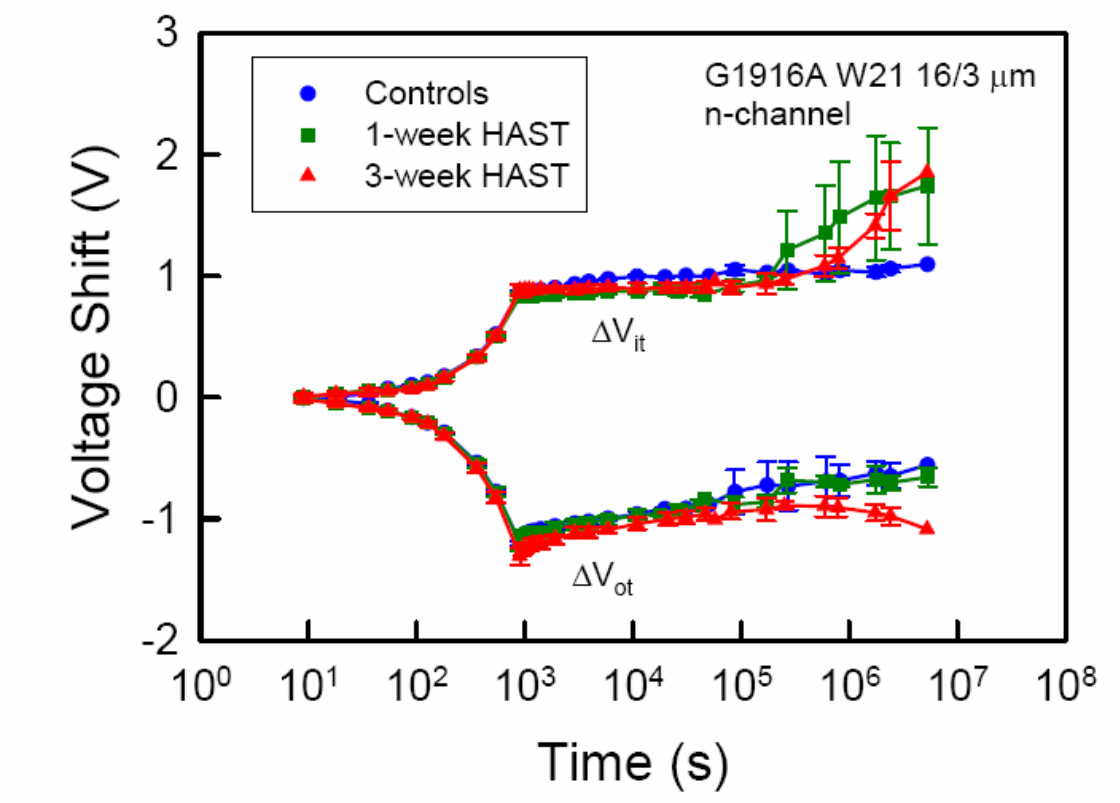

Figure 7. ΔV_{it} & ΔV_{ot} for 3 µm nMOS transistors from Group A irradiated to 500 krad(SiO_2) and annealed at room temperature [34].

Figure 8 plots the radiation-induced voltage shift due to interface-trap, ΔV_{it}, and oxide trapped charge, ΔV_{ot} for 3 µm gate length control and HAST-exposed G1916A n-channel transistors during irradiation and long term room temperature anneal phases. These devices have a gate oxide thickness of 32 nm (Group C). The transistors were irradiated and annealed with a gate to source bias of V_{GS} = 12.5 V. Clearly, the trends in irradiation and annealing response are similar for the Group A devices in Figure 7 and the Group C devices in Figure 8.

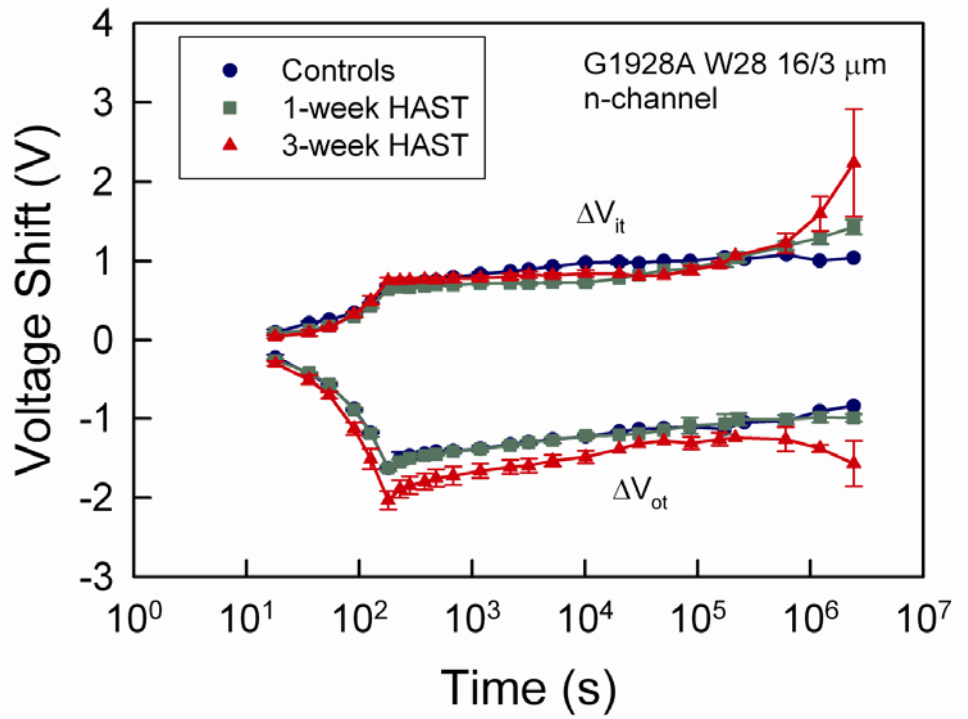

Figure 8. ΔV_{it} and ΔV_{ot} for 3 μm nMOS transistors from Group C irradiated to 100 krad(SiO_2) and annealed at room temperature.

The increase in magnitudes of ΔV_{it} and ΔV_{ot} during later stages of room temperature annealing suggests that these results may be important from a long-term aging point of view. Moisture can have a significant impact on devices used and/or stored for long periods of time in non-hermetic environments. This is consistent with the results of Rodgers et al. [38], which shows exposure to water or moisture during 17 years of aging can cause enhanced interface trap buildup during post-radiation annealing. Thus, exposure to hydrogen in the form of water vapor can affect long-term buildup of radiation-induced charge.

Figure 9 shows the radiation-induced change in ΔV_{ot} for 3 μm gate length p-channel transistors subjected to 3 week HAST from Group B, having a gate oxide thickness of 68.2 nm. The transistors were irradiated and annealed with a gate to source bias of V_{GS} = –12.5 V (typical bias condition for a p-channel transistor biased in the ON condition). For this bias condition, as expected, the control devices showed no significant buildup in

radiation-induced interface-trap charge and a small increase in magnitude of ΔV_{ot} of ~ 0.2 V after irradiation to 100 krad(SiO_2). However, the 3 week HAST-exposed p-channel transistors showed extremely large shifts in ΔV_{ot} during irradiation. After irradiation to 100 krad(SiO_2), ΔV_{ot} was ~ –4.2 V. Thus the HAST exposure resulted in a 20 times increase in ΔV_{ot}. These large p-channel voltage shifts are considerably more than the 3 μm n-channel voltage shifts observed in Figure 7 and n-channel voltage shifts observed in previous work after hydrogen exposure [39].

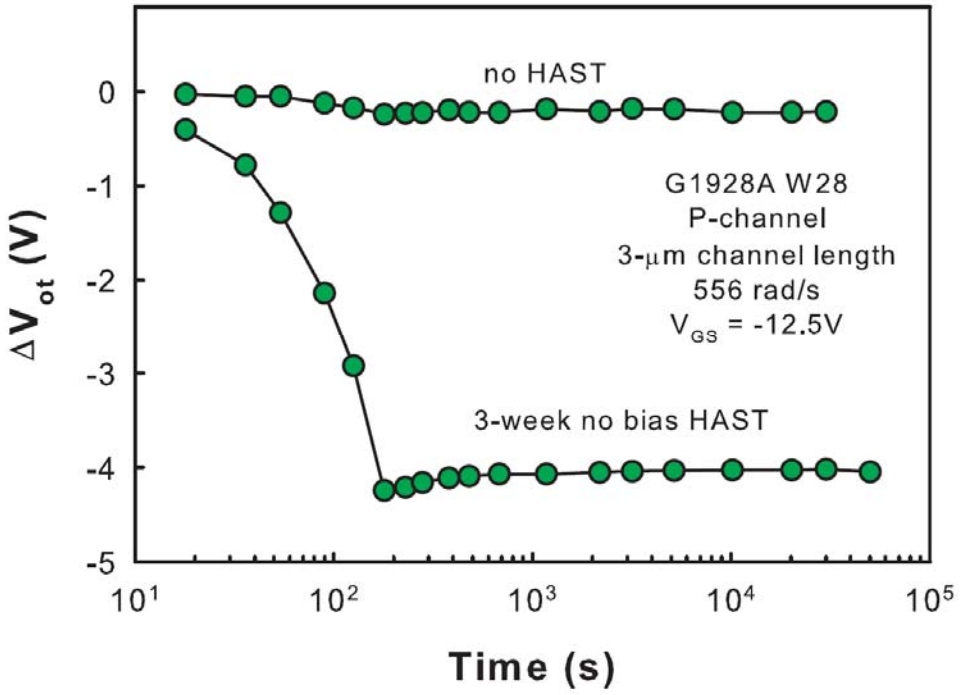

Figure 9. ΔV_{ot} for 3 μm pMOS transistors from Group C irradiated to 100 krad(SiO_2) and annealed at room temperature [34].

Figure 10 shows the voltage shifts due to radiation-induced oxide trapped charge, interface trapped charge, and threshold voltage shifts of both control and HAST-exposed n-channel transistors after irradiation to 1 Mrad(SiO_2) for Group A, with a gate oxide thickness of 32 nm. The voltage shift due to interface trap charge, ΔV_{it}, oxide trapped charge, ΔV_{ot} and hence the threshold voltage shift, ΔV_{th} are quite close for both control and HAST-exposed n-channel transistors. These results and other experiments on several

devices from the different groups suggest a relatively weak dependence of nMOS radiation response on moisture exposure for the devices and experimental conditions of this study.

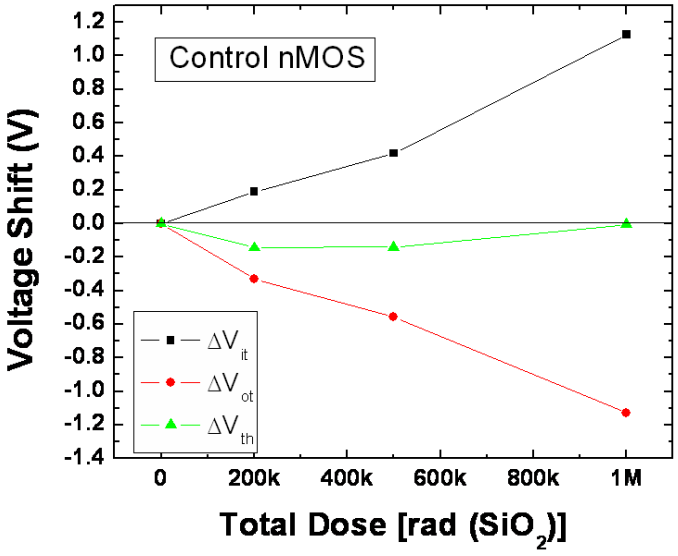

Figure 10. (a) Voltage shifts of Control nMOS devices from Group A.

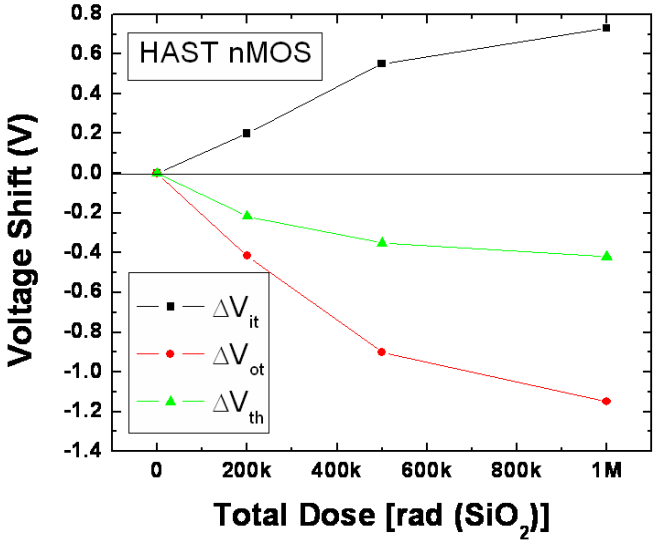

Figure 10. (b) Voltage shifts of HAST exposed nMOS devices from Group A.

Figure 11 shows the voltage shifts due to radiation-induced oxide trapped charge, interface trapped charge, and threshold voltage shifts of both control and HAST-exposed p-channel transistors after irradiation to 1 Mrad(SiO_2) for Group A. There are larger voltage shifts due to interface trapped charge, ΔV_{it} and oxide trapped charge, ΔV_{ot}. Hence the shift in threshold voltage, ΔV_{th}, of the HAST-exposed p-channel transistor is much larger than for the non-HAST-exposed p-channel transistor. This is in sharp contrast to the n-channel transistors, where both the HAST-exposed and the non-HAST n-channel transistors showed comparable voltage shifts. Similar increases in radiation-induced defect densities were observed for other pMOS transistors from the four groups studied in this work. This demonstrates that there are larger changes in post-irradiation defect densities for p-channel transistors with humidity exposure than nMOS transistors, for these devices and humidity exposure and irradiation conditions.

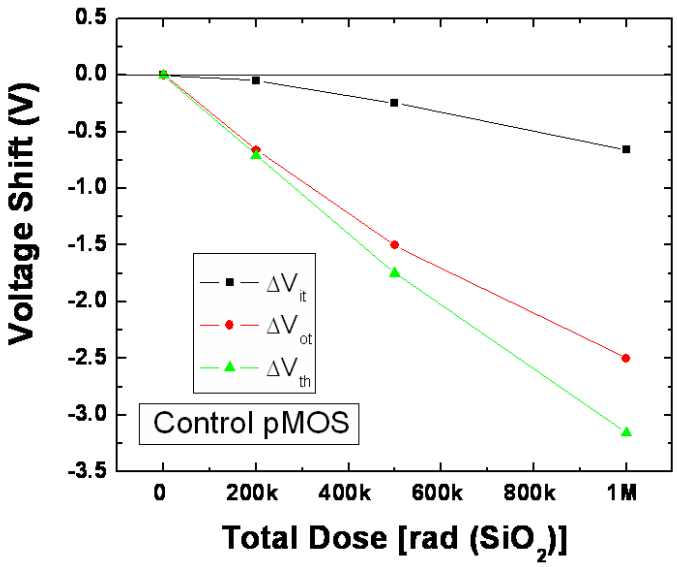

Figure 11(a). Voltage shifts of Control pMOS devices from Group A.

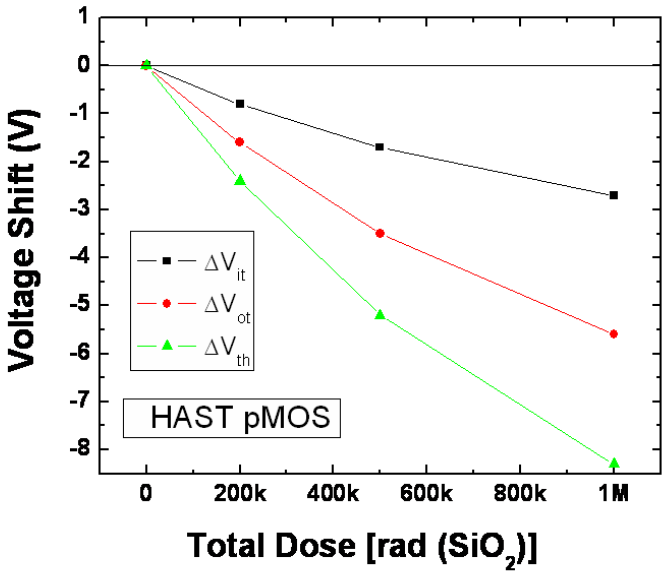

Figure 11(b). Voltage shifts of HAST exposed pMOS devices from Group A.

The large shift in p-channel transistor threshold voltage shown in Figures 9 and 11 will decrease p-channel transistor drive and degrade the timing properties of an IC, and can potentially cause functional failure. It also has been seen for SRAMs exposed to HAST that there is a very large increase in read-access time, t_{rd}, versus total dose, consistent with these results [34]. Similar effects were also observed in other devices with thinner oxides, and in parasitic field oxides [34]. These results show that exposure to humidity (hydrogen) can lead to enhanced radiation-induced degradation of device parameters and lower the functional failure levels for some IC technologies.

CHAPTER V

LOW-FREQUENCY NOISE MEASUREMENT RESULTS

Figure 12 shows typical 1/*f* noise spectra as a function of drain bias while keeping the gate bias constant at 1 V for n-channel control transistors from Group A. The figure shows five separate traces with V_{ds} varying from 50 mV to 250 mV. As expected, the noise magnitude increases with increasing drain bias.

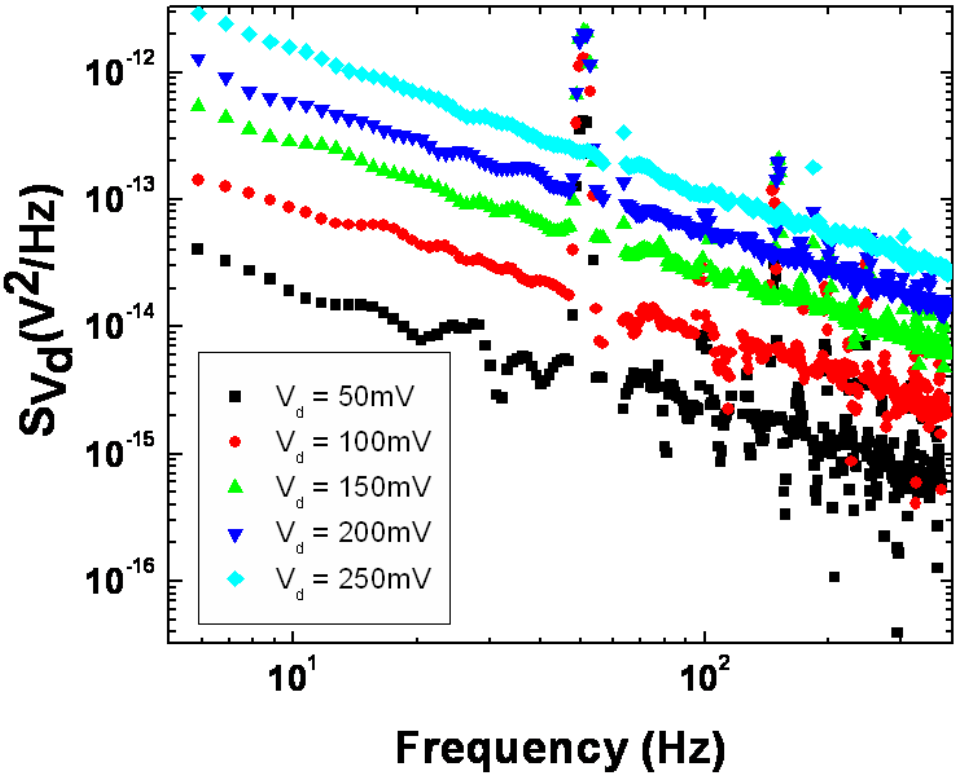

Figure 12. 1/*f* noise spectra S_{Vd} for an unirradiated n-channel transistor are plotted as a function of frequency. There are 5 traces corresponding to different drain bias. The gate bias is constant at 1 V during the measurements.

If the values of the power spectral density at f = 10 Hz from each trace of Figure 12 are plotted as a function of V_d^2, according to the number fluctuation model, the power spectral density of drain-voltage fluctuations associated with capture and emission of charge carriers is expected to vary as

$$S_{V_d}(f) \propto V_d^2 . \tag{19}$$

Hence, the slope of a log-log plot of S_{Vd} vs.V_d^2, as in Figure 13(b) is expected to be close to unity. The slope of the best fit straight line shown in 13(b) is ~ 1.18.

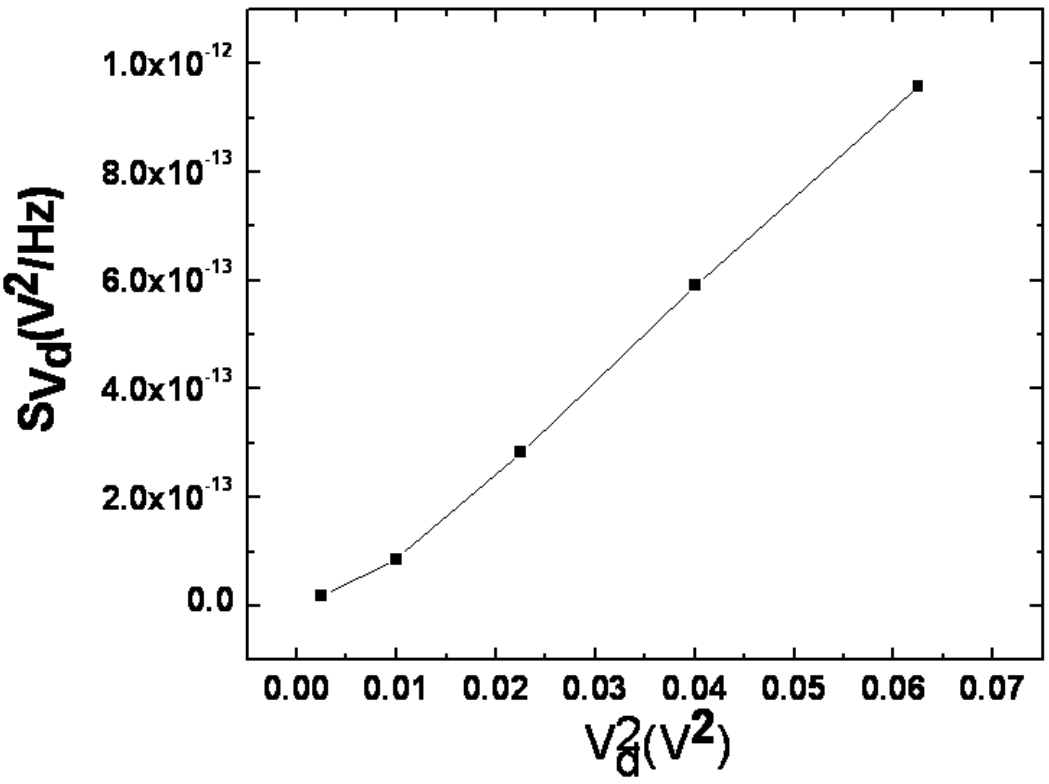

Figure 13. (a) S_{Vd} @ 10 Hz vs. V_d spectrum.

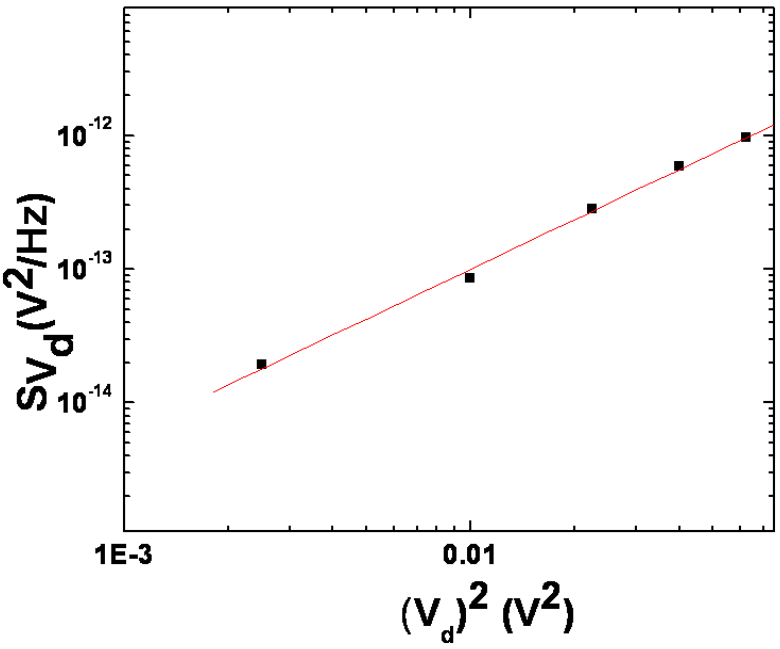

Figure 13. (b) Best linear fit of the data shown in (a).

Figure 14 shows the noise spectrum as a function of gate bias with the drain bias set at 100 mV. The figure shows six traces with V_{gs} varying from 1 V to 8 V. As expected, the noise magnitude decreases with increasing gate bias.

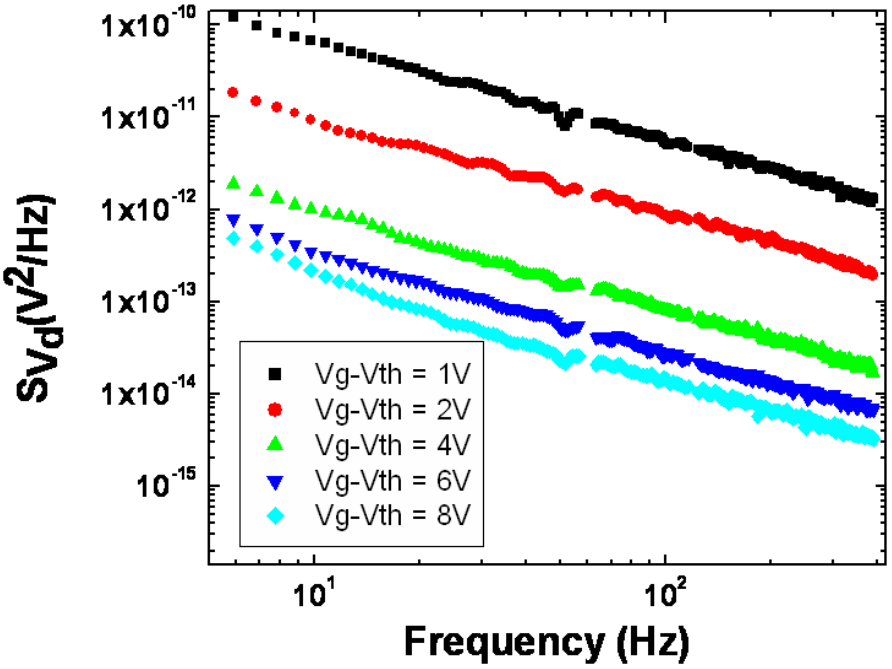

Figure 14. Noise spectrum for an unirradiated n-channel transistor with the drain bias set at 100 mV. The figure shows 5 traces with V_g varying from 1 V to 8 V.

In Figure 15(a) we plot the power spectral density at f = 10 Hz as a function of $(V_g - V_{th})^{-2}$. According to the number fluctuation model, the power spectral density of drain-voltage fluctuations associated with capture and emission of charge carriers is expected to vary as

$$S_{V_d}(f) \propto \frac{1}{(V_g - V_{th})^2}, \qquad (20)$$

Hence, the slope of a log-log plot of S_{Vd} vs. $(V_g - V_{th})^{-2}$, as in Figure 15(b) is expected to be close to unity. We calculated the slope of the best fit straight line in 15(b) to be ~ 0.85.

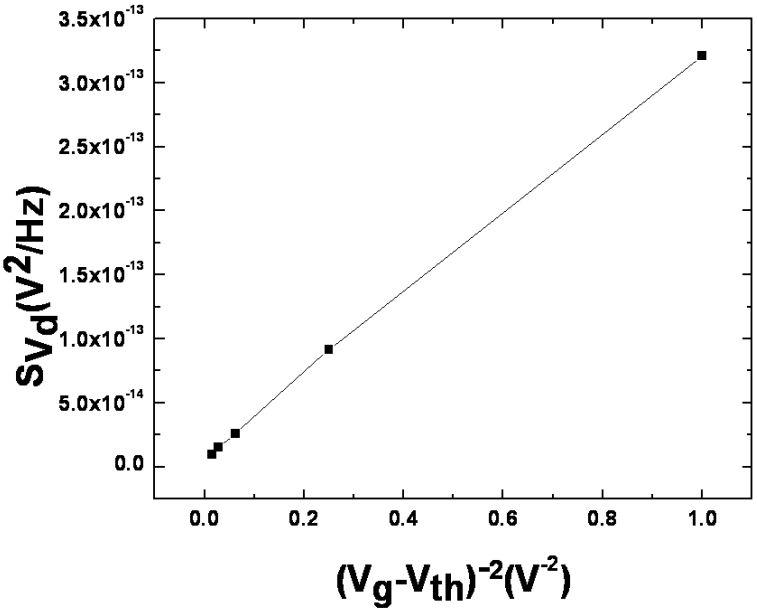

Figure 15. (a) S_{Vd} @ 10 Hz vs. (V_g-V_{th}) spectrum.

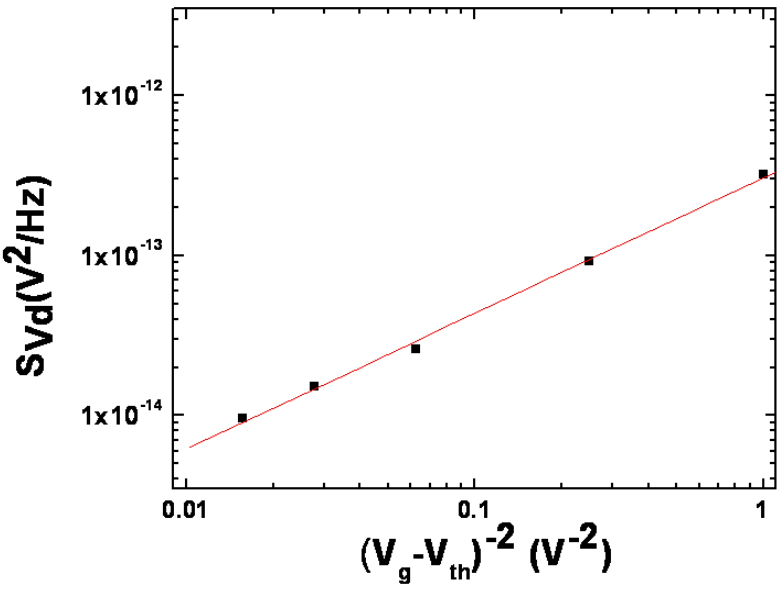

Figure 15. (b) Best linear fit of the data shown in (a).

In order to study the effects on these MOS transistors when these devices are exposed to high radiation environments in space, both the control (control-post) and the HAST-exposed transistors (exposed-post) were subjected to irradiation to total doses of 1 Mrad(SiO_2) (Group A), 500 krad(SiO_2) (Groups B and C), and 100 krad(SiO_2) (Group D) and then low-frequency noise measurements were performed on them. The HAST exposures were performed with all pins shorted and the irradiations were performed with V_{gs} = 6 V for all transistors shown in this work. The "Pre" and the "Post" values of the normalized noise level *K*-value for both the control and the HAST-exposed transistors before and after irradiation are shown below.

The excess drain-voltage noise power spectral density S_{Vd} (corrected for background noise), versus frequency *f* plot for a 3 μm gate length n-channel MOS transistor from Lot G1916A having an oxide thickness of 32 nm (Group A) is shown in Figure 16. During the noise measurement, the n-channel MOS transistor is biased so that V_{gs} - V_{th} = 1 V and V_{ds} = 100 mV. The value of the normalized noise level (*K*-value) before irradiation for the control nMOS device is 2.0×10^{-11} V^2 and for the nMOS device exposed to moisture is 2.6×10^{-11} V^2. After irradiation to 1 Mrad(SiO_2), the *K*-value for the control nMOS device is 33×10^{-11} V^2, whereas for the nMOS device exposed to moisture, the *K*-value is 52×10^{-11} V^2. Thus, exposing the n-channel transistors to HAST resulted in less than a factor of 2 difference in S_{Vd} for these transistors. Irradiating the transistors to 1 Mrad(SiO_2) led to an increase in S_{Vd}, but the HAST exposure did not significantly impact S_{Vd} postirradiation. This is consistent with the small impact of HAST exposures on ΔV_{ot} and ΔV_{it} as shown in Figure 7. This relatively small change (less than a factor of 2 change in noise magnitude with HAST exposure) is typical of results observed for other nMOS transistors from all of the four groups.

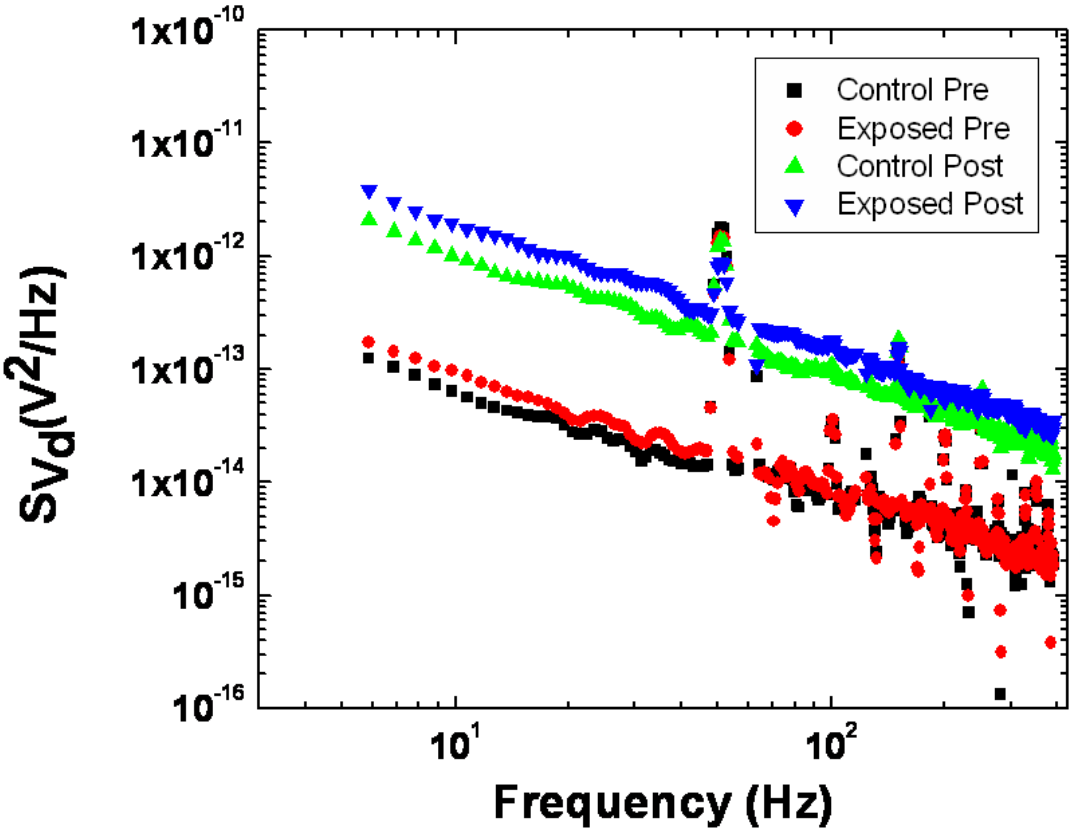

Figure 16. The S_{Vd} vs. frequency spectrum and summary of results of low frequency noise measurements on (a) n-channel from Group A.

The excess drain-voltage noise power spectral density S_{Vd} (corrected for background noise), versus frequency f plot for a 3 μm gate length p-channel MOS transistor from Group A is shown in Figure 17. The K-value prior to irradiation for the control pMOS device is 0.2×10^{-11} V^2 and for the pMOS device exposed to moisture is 2.7×10^{-11} V^2, which is more than an order of magnitude increase in noise with moisture exposure. After irradiation to a total dose of 1 Mrad(SiO_2), the K-value for the control pMOS device is 7.2×10^{-11} V^2, whereas for the pMOS transistor exposed to moisture, it is 235×10^{-11} V^2. Thus, after irradiation, S_{Vd} was approximately two orders of magnitude larger for p-channel transistors exposed to HAST than for p-channel transistors not exposed to

HAST. Similar increases in noise were observed for pMOS transistors from all of the groups studied exposed to HAST, both before and after irradiation.

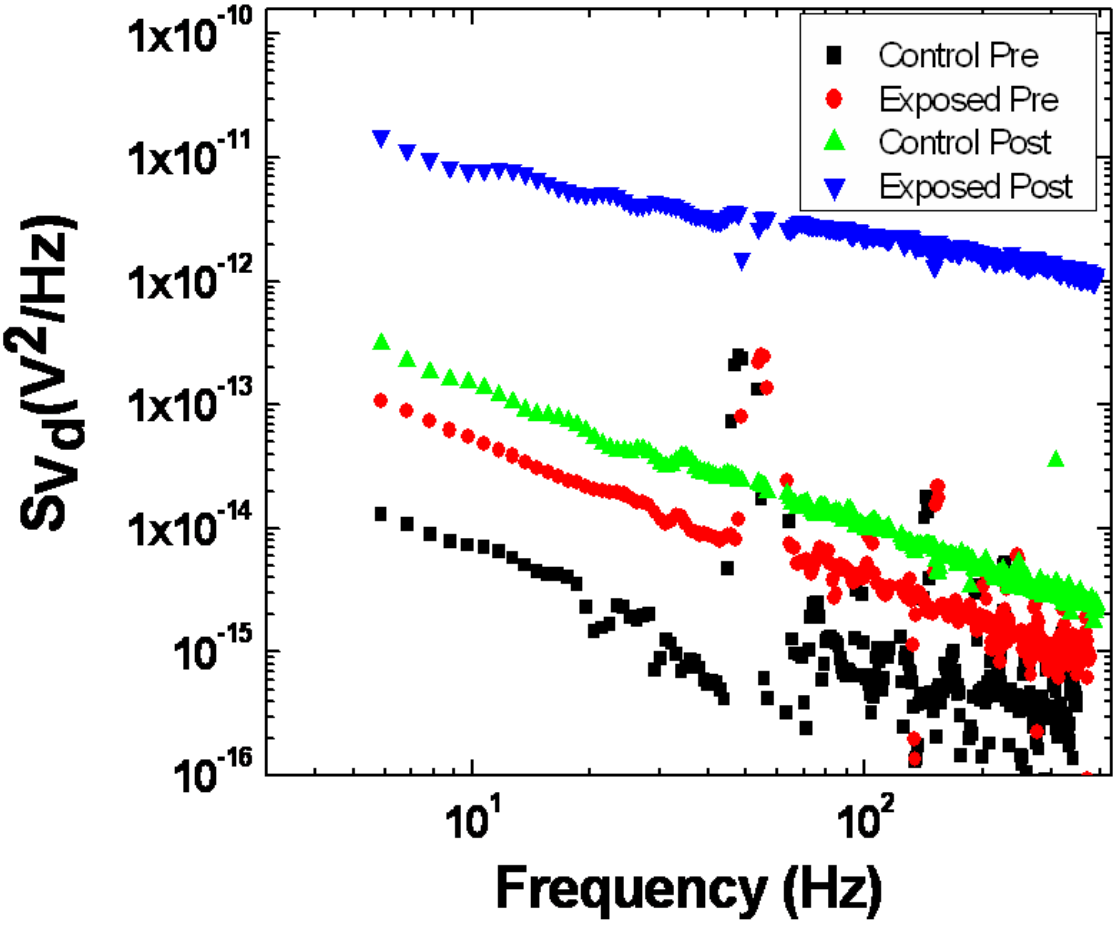

Figure 17. The S_{Vd} vs. frequency spectrum and summary of results of low frequency noise measurements on p-channel MOS transistors from Group A.

Reasons for Enhanced Degradation of HAST Treated p-channel MOSFETs:

Water molecules first diffuse into the field oxide (FOX) (in the shaded region) and then diffuse into the gate oxide laterally (as shown) from the FOX regions, as illustrated schematically in Figure 18. (This is a generic representation of a MOS transistor surrounded by field oxide, and not an actual diagram of the devices used in this study, for which a similar diagram is not available.)

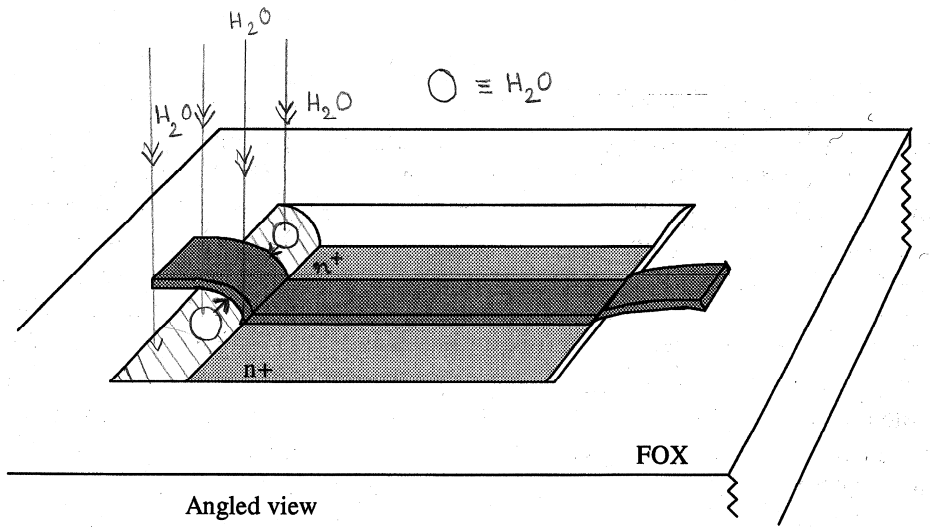

Figure 18: Water diffusion in MOSFET.

It has been observed that more O vacancies are formed in SiO_2 in the presence of water [34, 40]. Water can diffuse through Si-O rings as an interstitial or react with the Si-O ring network to form a silanol complex (-Si-OH) [41]. When these devices are exposed to irradiation, electron-hole pairs are created. The trapping of the holes in O vacancies leads to an increase in the oxide trapped charge. The new silanol (Si-OH) complex formed due to presence of water in SiO_2 also becomes a source of H that can be released as H^+ in the presence of holes [41]. The process has an activation energy of 0.8 eV [41]. A mobile proton migrating to the interface can encounter an intact water molecule and attach itself to form a H_3O^+ ion. This process has forward reaction energy of 0 eV in the presence of

holes after irradiation [42]. The H^+ and H_3O^+ may also act as positive oxide-trap charge in addition to oxygen vacancies. Also, under positive bias, H^+ ions can migrate to the Si-SiO_2 interface, where they can cause enhanced interface trap creation by depassivating Si-H bonds. Higher threshold voltage shifts due to oxide trapped charge and interface traps and higher 1/*f* noise were observed in HAST treated p-channel transistors post-irradiation. However, the n-channel transistors are less sensitive to the presence of water or moisture. We now consider the reasons for the differences in these responses.

Phosphorus (boron) dopant atoms are present in the field oxides of the n-channel (p-channel) transistors because of source and drain implant steps, as shown in Figure 19. This is a schematic representation of a field oxide layer formed by local oxidation; the field oxides in Sandia's 4/3 μm are planar oxide layers that are otherwise similar to this sketch. (A cross section of the Sandia process is not available.)

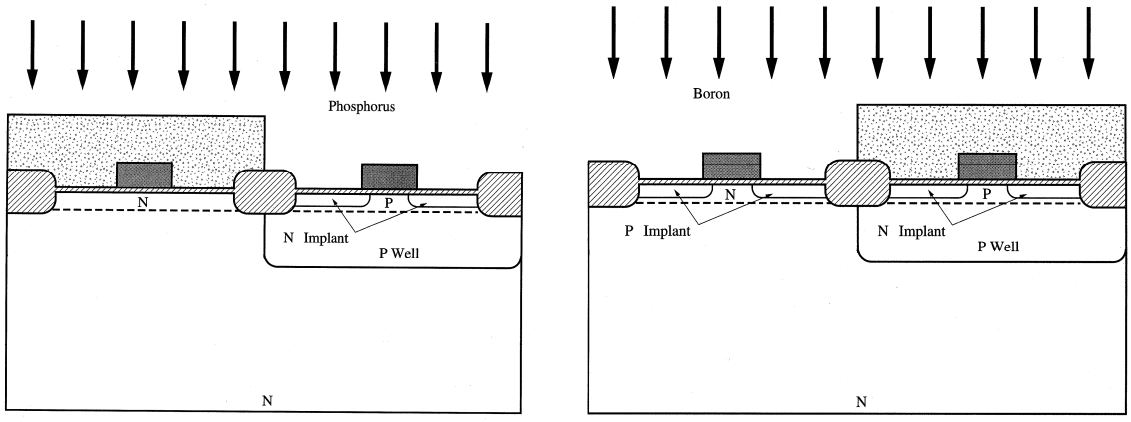

Figure 19. Phosphorus (boron) atoms are present in field oxide regions of nMOS (pMOS) transistors during source/drain implants.

Studies report that boron accelerates water penetration and phosphorus suppresses water penetration in oxides (compared to undoped SiO_2) [43, 44]. These results are based on FTIR and Secondary Ion Mass Spectrometry (SIMS) experiments done under PCT conditions (saturated water vapor at 120 °C) [43]. Similar results have been reported in doped films that were exposed to atmospheric moisture during storage at room temperature (aging) [44]. Boron increases the number of molecular water adsorption sites

without interacting chemically with water. Phosphorus reduces the number of molecular adsorption sites and reacts with water chemically to prevent water penetration deep into the film. A detailed mechanism for these interactions was proposed in [44]. Phosphorus forms a stronger complex with H_2O in SiO_2 because the H in the resulting -P–OH bonds forms hydrogen bonds with the O of the Si-O ring network. This hydrogen bonding is not seen in the B-OH complex because of the different polarities of B-O bonds and P-O bonds as shown in Figure 20.

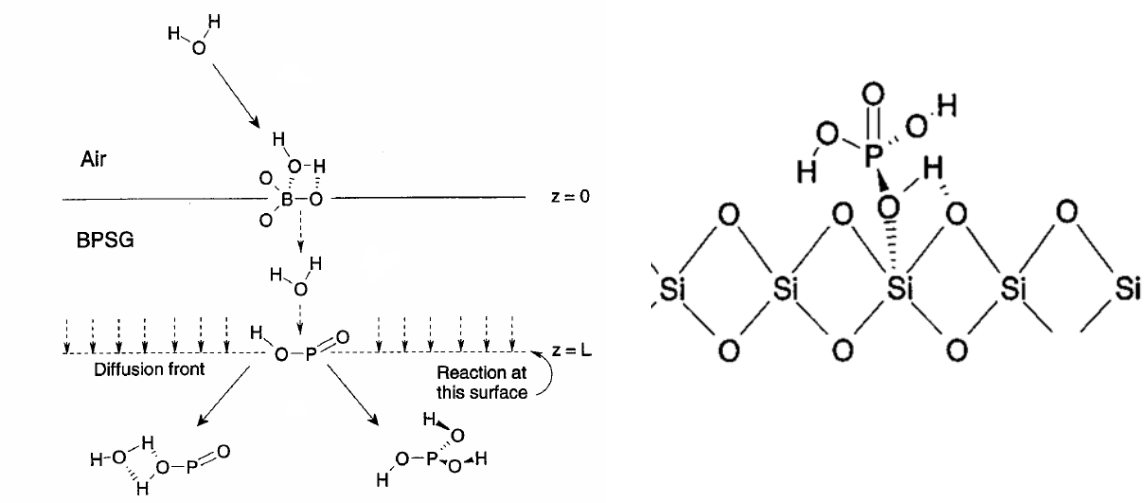

Figure 20. Proposed mechanism for suppressed water diffusion in SiO_2 in the presence of phosphorus [44].

The above discussion strongly suggests that H_2O diffusion through the FOX towards the gate oxide of nMOS transistors can react with P atoms, and their penetration into the gate oxide will be suppressed. In case of p-channel transistors, H_2O diffusing through the FOX will encounter B atoms, and their penetration into the gate oxide will be enhanced. Increased defect formation as a result of extra water penetration therefore occurs in pMOS oxides in this process technology, relative to nMOS transistors.

To check the plausibility of this mechanism, we calculated the diffusivity of water in undoped SiO_2 based on Fick's law:

$$D(T) = D_0 e^{\frac{-E_a}{kT}} \tag{21}$$

For H_2O in pure SiO_2, $D_0 = 10^{-6}$ cm^2/sec and the activation energy $E_a = 0.79$ eV [45, 46] at room temperature. The distance through which the water molecules can diffuse is given by $\sqrt{4 * D(T) * \tau}$ [47], where τ is the time. In pure SiO_2 at 130 ^oC, moisture can diffuse a distance of ~ 0.18 μm in a week. It has been reported that the diffusivity *D(T)* of water at room temperature in SiO_2 in which boron dopant atoms are present is ~ 10^{-14} cm^2/s [44, 48], which is much higher than the diffusivity of water in undoped SiO_2. At the HAST temperature (130 ^oC), this is enhanced further still. We estimate that water molecules with this diffusivity in the field oxide regions of p-channel transistors (shaded regions shown in Figure 18) can diffuse in a week to distances up to ~ 2 μm to ~ 7 μm under these conditions. Hence, it is quite plausible that moisture diffusion in the presence of B can lead to the effects observed above.

We expect similar results for other technologies with similar source/drain and field-oxide technologies, as verified in a recent study by Schwank et al. [34]. In this work, transistors from several process technologies were found to exhibit enhanced pMOS charge trapping after first moisture exposure, and then irradiation. Hence, the results reported here are expected to occur for a wide range of process technologies, owing to the common use of P and B in source and drain implants, and the requirements for device isolation using field oxide structures similar to those depicted and described above.

The above results suggest that some MOS device technologies may be considerably more sensitive to moisture exposure than originally believed. As a result, devices operating in systems that require devices to function in radiation environments (e.g., space) after long-term storage may fail at considerably lower than expected total dose levels. The large p-channel voltage shifts for devices exposed to HAST raise the concern that devices

packaged in plastic packages may suffer from degraded reliability. This is because if H_2O can penetrate the plastic packages used for some kinds of commercial technologies, H_2O exposure over long time periods may lead to enhanced radiation-induced degradation.

CHAPTER VI

CONCLUSIONS

We have found that moisture exposure affects pMOS transistors of the Sandia 4/3 μm technology much more significantly than nMOS transistors. The magnitudes of the n-channel MOS gate oxide voltage shifts for transistors exposed to moisture at elevated temperatures and then irradiated with 10-keV x-rays are consistent with previous work. However, extremely large gate oxide voltage shifts were observed for the pMOS transistors. The low frequency noise for the n-channel transistors changed only a small amount with HAST. However, for pMOS transistors, the noise magnitude changed by almost an order of magnitude during the HAST exposures and by up to two orders of magnitude post-irradiation. The increased vulnerability of the pMOS transistors can be attributed in part to the absence of phosphorus in the field oxide regions of the pMOS transistors, which allows more moisture diffusion into and defect formation in these gate oxides than for the oxides of the nMOS transistors. Enhanced diffusion of moisture in the presence of B in pMOS field oxides during HAST also may enhance the resulting oxide-trap creation in those structures.

These results are significant for models of 1/*f* noise, radiation response and long term reliability, especially for devices that are not hermetically sealed, or for devices with large densities of hydrogenous species incorporated during device processing. Hydrogen and moisture can lead to extremely large radiation-induced charge buildup and hence cause IC failure at lower total dose levels than may be anticipated from test results that do not include moisture effects. More detailed studies need to be done to identify the particular microscopic origins of the defects causing the noise. In addition, it is very important to determine whether similar effects are also found in submicron scale MOS technologies that are more typical of present day radiation-hardened and commercial microelectronics technologies.

APPENDIX A

CONTROL SOURCE CODE EXAMPLES

This is the example code written in BASH shell script for low frequency noise measurement.

```
#!/bin/sh

dir=/home/antoine/noise                 # Directory where the measurement data is stored

c=`./guiOneTime2.pl`

device=`./applica.pl 1 $c`              # Set the Device name

numbAve=`./applica.pl 3 $c`             # Set the number of averages

amplFact=`./applica.pl 2 $c`            # Set the amplification parameter from the Low
                                        # Noise Amplifier

freqSpan=`./applica.pl 4 $c`            # Set the frequency span of noise measurement.

vth=`./applica.pl 5 $c`                 # Set the threshold voltage of the MOSFET

#tempMax=`./applica.pl 6 $c`            # Set the temperature.

echo "DATA: $device, $numbAve, $amplFact, $freqSpan, $tempMax"

for increment in 1 #  Set the gate voltage such that Vgs–Vth = 1 V.

do
```

```
echo "vth=$vth"

echo "Device: $device" >> $dir/current

echo "Vth=$vth, Vgs-Vth=1V, designed drain voltage=$Vdrain " >>$dir/current

Vgate=`echo "$vth+$increment" | bc`

echo "Vgate=$Vgate"

./voltb $Vgate                  #  Set the proper bias across the gate of the MOSFET


./volta 1                       # Apply a test voltage of 1 V across the drain and the control
                                #  resistor

sleep 20

VDS=`./multimeter`          # Check the the value of V_DS using the multimeter

VA=`./voltage-convert 1 $VDS 0.1`     # Set the voltage on the drain V_A such that
                                      # V_DS = 100 mV

echo "va=$VA"

./volta $VA                     # Set the proper bias on the drain

sleep 30

A=`./multimeter`
```

```
echo "VDS= $A"


echo "Va=$VA, Vdrain= $A" >>$dir/current

echo "      " >>$dir/current

echo "Finishing applying bias, beginning counting"      # measure the foreground noise

./newDevInit2 $numbAve $freqSpan >tmpdata-fg        #  Configure the SR760 Spectrum
                                                    #  Analyzer
                                                    # Set the desired average
                                                    # Set the desired frequency span
echo "Finished Fg noise measurement."                # measure the background noise

./volta 0                                           # apply 0 V  on the drain.

sleep 20

./newDevInit2 $numbAve $freqSpan >tmpdata-bg     # Save the background noise data

echo "Finish the Bg noise measurement."

./convert1.pl $freqSpan $amplFact >$dir/$device-$Vgate

./voltb 0

cat >tmpdata <<EOF

set data style points                          # Plot the data using GNU plot
```

```
set logscale
set xlabel "f(Hz)"

set ylabel "Svd(V^2/Hz)"

plot '$dir/$device-$Vgate' using 1:2          # Plot SVd vs. f power spectrum
EOF

gnuplot -persist tmpdata

read Vlower                          # Prompt use to enter the lower limit for the linear fit
read Vupper                          #  Prompt use to enter the upper limit for the linear fit


cat >tmpdata <<EOF
set data style points

set logscale
#set terminal png
set xlabel "f(Hz)"
set ylabel "Svd(V^2/Hz)"
fit [$Vlower:$Vupper] a*x+b '$dir/$device-$Vgate' using 1:2 via a,b
plot '$dir/$device-$Vgate' using 1:2, a*x+b  “    # Parameter extraction for the best linear
                                                  # fit
print a
print b
EOF
sleep 2
gnuplot -persist tmpdata
gnuplot tmpdata >& gnuplotout
```

```
a=`cat gnuplotout | tail -2 |head -n 1`
b=`cat gnuplotout | tail -1 |head -n 1`
k1=`/home/antoine/noise/power 10 $b`
s=`/home/antoine/noise/abs $a`
echo "a=$a, b=$b, k=$k1, s=$s"
echo "$k1 $s $Vgate" >> $dir/noise$device
done
rm tmpdata-fg
rm tmpdata-bg
rm tmpdata
```

This is an example of the code written in C to control the Stanford Research Systems' SR760 spectrum analyzer.

```
#include<stdio.h>                    # User GPIB include file

#include<stdlib.h>

#include<string.h>

#include<unistd.h>

#include "ni488.h"

#define PAD 10                       # GPIB primary address of the SR760 spectrum
                                     # analyzer

#define SAD 0                        # GPIB secondary address
```

```
void wait(int ud)
{
   char serPol;
   do
   {
      ibrsp(ud,&serPol);
   }while ((serPol&1)==0);
   //printf("\nScan Finished; Acquiring Spectrum");
}


int send(int ud,char *command)              # Subroutine used to talk to the instrument
{
   char serPol;
   ibwrt(ud,command,strlen(command));
   do{
         ibrsp(ud,&serPol);      //poll for IFC RDY to insure command completion
         } while ((serPol&2)==0);
}

int main(int argc, int *argv)
{
   int id,rd,handle,ud, preampGain;
   short lnf;
   char readbuf[100000];
   char rsp;
   double buf;
   char count[3];
   char trace[30];
   handle=ibfind("gpib0");                  # Find the GPIB controller
   ibpad(handle,0);
```

```
    ibrsc(handle,1);                    # Board handle is made system controller
    ibsic(handle);                      # Reset GPIB bus for at least 100 μs
    ibsre(handle,1);                    # Set remote enable board "handle" must be
                                        # the System controller

    ud=ibdev(0, PAD, SAD, 13, 1, 0);    # Open the equipment with the primary address

    send(ud,"*RST\n");                  # Reset SR760 spectrum analyzer
    send(ud,"STOP\n");                  # Stop data acquisition
}
```

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