SINGLE EVENT LATCHUP IN A DEEP SUBMICRON CMOS TECHNOLOGY

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But there's no sense crying
over every mistake.
You just keep on trying
till you run out of cake.
And the science gets done.
And you make a neat gun
for the people who are
still alive.

-Still Alive,
Jonathan Coulton

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CHAPTER I

INTRODUCTION

One of the most important aspects in the study of radiation and its effects on microelectronic devices is the influence of device scaling on the error rates and vulnerability to phenomena such as single event latchup (SEL). In the space radiation environment, which includes the Earth's radiation belts, solar winds, and galactic cosmic rays, a satellite system needs to operate reliably with a manageable error rate that can be reduced through software or circuit-level correction techniques. Errors are caused by energetic particles passing through the semiconductor devices. Energy transferred by these particles results in generates charge in the form of electron-hole pairs. This charge creates extraneous current or voltage pulses in a circuit by changing electrostatic potentials and currents in devices. These pulses can cause errors by being falsely perceived as data by the circuit or by flipping the stored data value on a node. While it is preferable to have a process-hardened circuit for a spaceborne system that includes guard rings, extra well and substrate contacts, and buried doping layers or other layout-implemented radiation hard by design (RHBD) techniques, commercial off the shelf (COTS) parts and commercial processes are becoming more appealing. Some of the reasons for this desirability include lower development cost, quick turnaround, and higher performance. Because of the desirability of using COTS devices in space systems, it is crucial that the effects of the radiation environment on these parts are understood and for experimental procedures to properly bound device response. As a benefit of understanding radiation effects on devices from contemporary technology nodes, insights can be gleaned with regards to dominant error mechanisms and error rates in future

technologies. Relatively few experimental or simulation results have been shown on devices from newer (65 nm and below) commercially available technology nodes [1-7].

Specifically of concern in this work is the hazard of single event latchup in a radiation environment. Latchup generally occurs in a complementary metal oxide semiconductor device (CMOS) when deposited charge from a single event turns on one of the two parasitic bipolar transistors present in the CMOS structure. These two bipolar transistors are naturally in a feedback loop. If the gain of this loop is greater than unity, then a high-current latching state can occur that renders the affected devices inoperable and can cause a large increase in system power usage or permanent damage. Figure 1.1 shows an example of this effect occurring in an ASIC test chip. As different areas of the chip latch up, the current draw on the system power supply increases dramatically. In most circumstances a full system restart is used to alleviate this potentially damaging high current state.

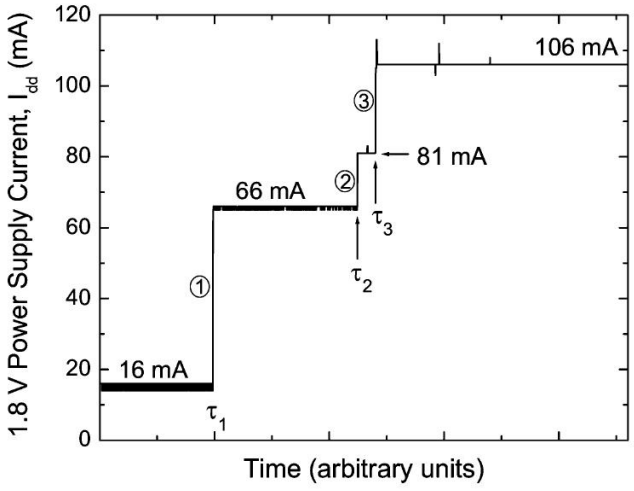


Figure 1.1. Current draw on a 1.8V power supply for three subsequent latches in three different on-chip locations. The latchups are induced by a pulsed laser in sensitive areas of the device. It can be seen that the power draw for the device is 6x normal operating current [8].

Because of the vulnerability of microelectronics to ionizing radiation, it is imperative to test potential components for radiation environment applications. One way this is done at ground level is by operating the component in question under exposure to heavy ions or protons using an accelerator beam. For this type of single event effect (SEE) testing, the Joint Electronic Devices Engineering Council (JEDEC) test standard is typically followed [9]. This test method will be examined in Chapters VI and VII and the adequacy of the test standard for SEL will be discussed.

This work focuses on the SEL response of test devices fabricated in a commercial 65 nm (0.065 μm) CMOS technology, particularly a silicon-controlled rectifier (SCR) and synchronous random access memory (SRAM) test devices. Available information for these parts includes layouts, doping profiles, and test memories as well as layout and experimental data. With experimental testing, knowledge of technology characteristics, and simulations, a thorough examination of SEL in this deep-submicron technology follows.

Latchup is simulated in both the large SCR test part and the SRAMs at the 65nm technology node. The SCRs help provide a baseline understanding for latchup in this technology through both simulations and experimental work. The 65 nm SRAMs are examined for latchup using heavy-ion testing.

Chapter II covers single event effects (SEE) and the space radiation environment. Chapter III covers the basic physics of SEL and the implications of scaling for that failure mechanism. Chapter IV covers the calibration of technology parameters for TCAD SEL simulations. Chapter V examines SEL through technology computer-aided design (TCAD) simulation of the large SCR test parts and discuses an angular orientation

dependence of latchup that is unaccounted for by current test protocols. Chapter VI provides test results and analysis reinforcing the angular dependence theory from Chapter V using 65 nm SRAMS. Finally, Chapter VII summarizes the most important aspects of this work.

CHAPTER II

THE SPACE RADIATION ENVIRONMENT AND SINGLE-EVENT EFFECTS

To understand the significance of this work, the reader needs a basic understanding of the space radiation environment and the effects that the highly energetic particles therein (protons, neutrons, alpha particles, heavy ions) can have on electronic circuits. There are many thorough guides on this topic and much of the information presented here is extracted from those sources [10-26]. Single-event effects (SEE) are the result of the aforementioned particles striking sensitive regions of microelectronic devices and/or sensitive nodes of a circuit. The effects of incident particles depend on strike location, angle of incidence, particle energy, particle species, and timing of the strike. Additionally, secondary particles can be created via nuclear reactions with a primary incident particle and the component materials of the microelectronic devices. These effects range from being non-observable to causing permanent physical and operational damage to the device. Of particular interest to this work is single-event latchup (SEL), but the basic physics of particle interaction with devices for all single event effects are similar. To begin, a brief introduction to the space radiation environment will be provided, followed by a detailed look at the physical mechanisms behind radiation-induced events.

The Space Radiation Environment

The constituents of the space radiation environment are geomagnetically trapped radiation, particles from solar events, and galactic cosmic radiation.

Trapped Particles

The earth's magnetic field can be approximated as a dipole field. The orientation of field lines around the earth allows particles entering the field to become trapped, creating radiation belts. The earth's radiation belts are referred to as the Van Allen radiation belts after Dr. James Van Allen, who oversaw the original Explorer missions in 1958.

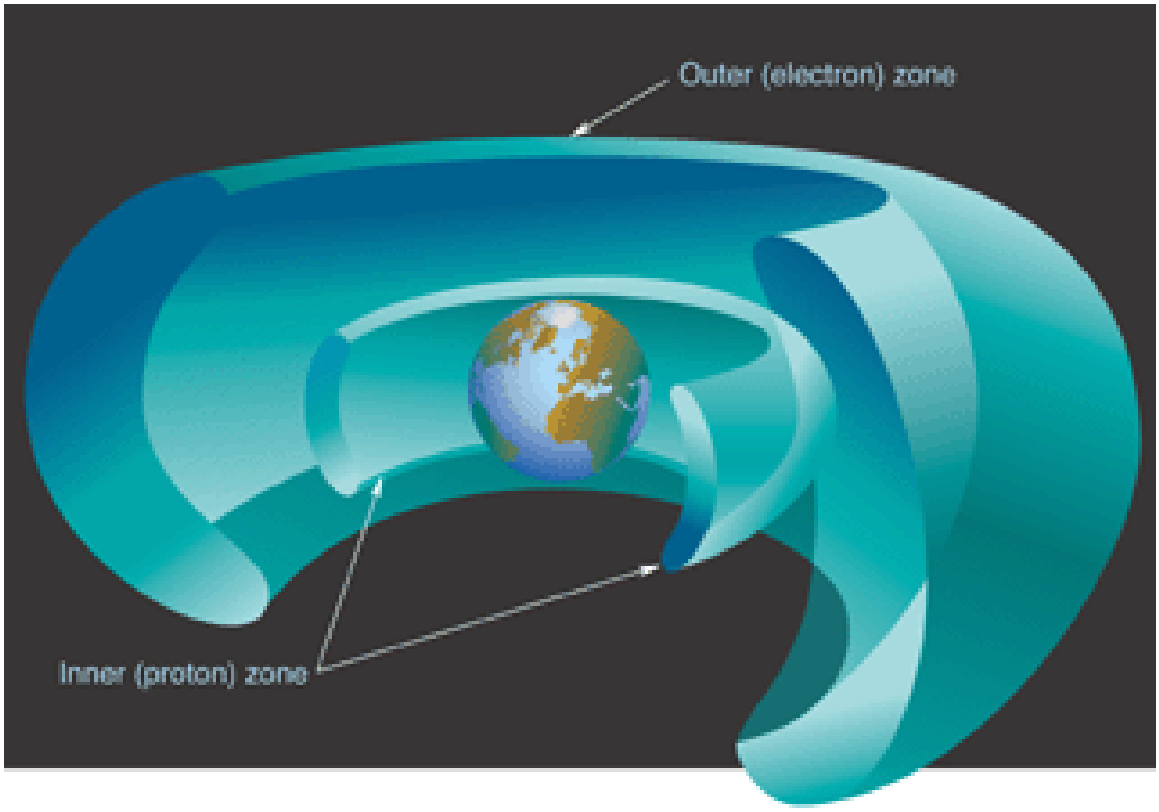


Figure 2.1. Diagram of the Van Allen belts. Trapped protons are trapped closer to the earth while trapped electrons form the outer shell [17].

It is interesting to note that while passing through the areas of highest radiation particle density, the instruments on the early Explorer spacecrafts actually reported zero particle flux as they were overwhelmed by the radiation environment. The data taken by

these spacecraft confirmed the existence of the radiation belts. Figure 2.1 is a depiction of these belts. Particles trapped in these belts include protons, alphas (hydrogen and helium nuclei), electrons, neutrons, and some heavier ions. These particles rotate around the field lines and reflect between the magnetic poles. In addition to bouncing between the poles, particles also drift around the planet with electrons moving to the east and protons (and other positively charged particles) moving to the west. This motion is depicted in figure 2.2.

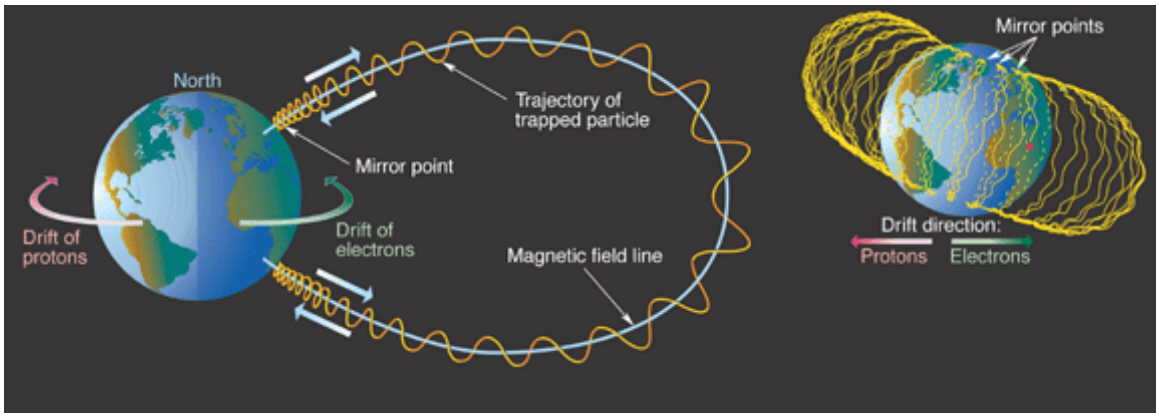


Figure 2.2. Motion of trapped particles in the Earth's magnetosphere. Particles can be seen to spiral around the field lines as well as bouncing back and forth at the mirror points. Drift direction of particles is also shown [17, 20].

Because electrons do not contribute to SEE (they do contribute to total dose and charging effects), only the effects of protons and heavier ions will be considered here. For a thorough treatment of total dose effects, see [27-29].

Of the particles of concern for SEEs, the most abundant are protons. This abundance also makes them the largest contributor for single-event upsets (SEUs), which are SEEs that cause a change in a data bit through charge deposition and collection processes. The region from about 1.15 Earth radii to about 2.4 Earth radii is the region

where the highest energy (and therefore of greatest concern) protons of > 30MeV energy are trapped. Protons with these energies easily penetrate spacecraft shielding and can affect the electronics within. Figure 2.3 shows the energy ranges of protons as a function of the distance from the planet's center in Earth radii.

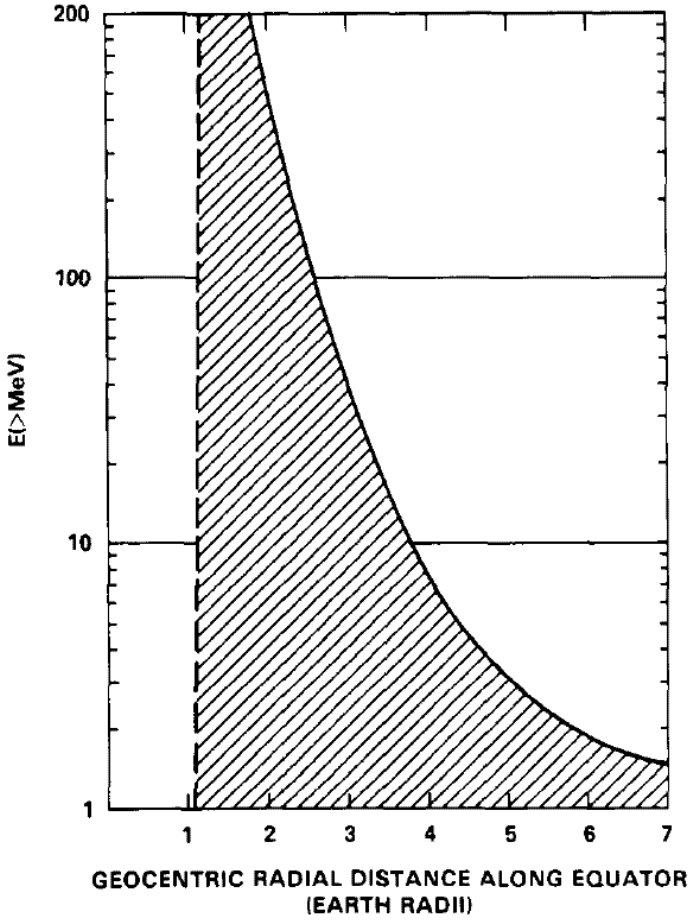


Figure 2.3. Trapped proton energies as a function of distance from the Earth's core in Earth radii. Peak proton energy falls off with distance from the earth [20].

One of the characteristics of the geomagnetic field that is important for modeling the space radiation environment is the South Atlantic Anomaly (SAA). This is the result of the displacement of the center of Earth's magnetic field from its geographical center

by about 280 miles as well as the displacement between the Earth's magnetic and geographic poles.

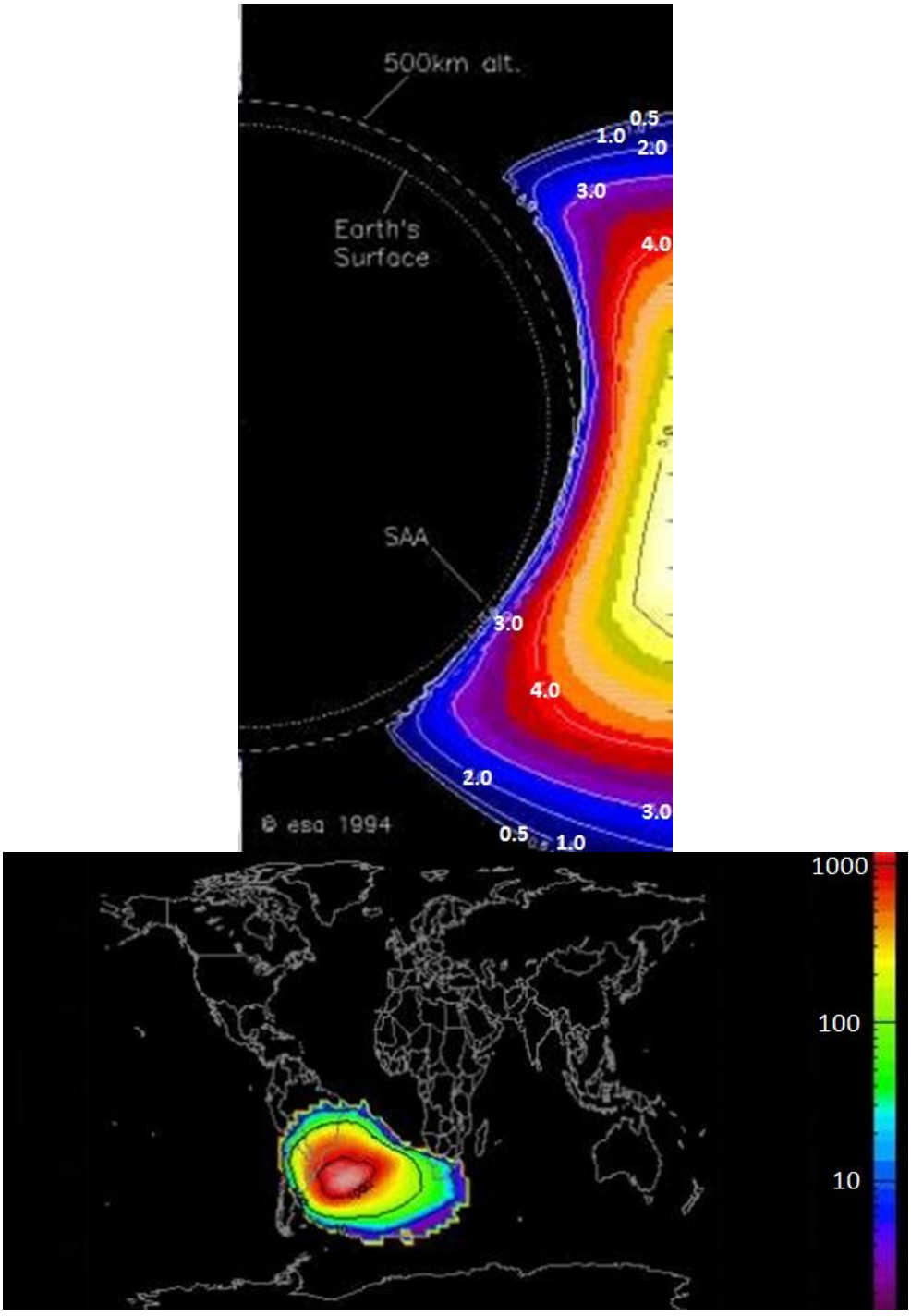


Figure 2.4. (a) The South Atlantic Anomaly. Proton flux can be seen to increase considerably at low altitudes in the South Atlantic. Flux is shown for powers of ten in cm^2/s for protons > 10MeV. After [24] (b) Contour plot of proton fluxes > 10 MeV in the SAA at a 500 km altitude during solar maximum. Flux is shown in units of cm^2/s. After [30].

This pole offset creates a depression in the magnetic field over the south Atlantic causing charged particles to be trapped at a lower altitude (< 1000 km) [12]. The result is a much higher flux of protons (~ 10^4× greater) for a spacecraft passing through the anomaly compared to other locations in the orbit. This has a profound effect on the operation of low Earth-orbit (LEO) satellites at inclinations affected by the anomaly. The International Space Station must also take these effects into account by using extra shielding. Figure 2.4 shows the geographic location of the SAA and the effect of the weaker electromagnetic field in the South Atlantic Ocean.

The Van Allen belts consist primarily of trapped protons and electrons. However, heavy ions can also be trapped in the geomagnetic field. These ions are believed to be the result of cosmic rays (neutral interstellar atoms) that become ionized and trapped. These ions have a similar distribution to trapped protons and like protons, have an increased presence in the SAA. Because of the fairly low energy of these ions, they are of less concern than the more plentiful and potentially more energetic trapped protons.

Transient Particles

Transient particles come from two sources, solar events and galactic cosmic rays. The frequency of significant solar events varies depending on the temporal location within the sun's activity cycle, which has been observed to be between 9 and 13 years. The difference in proton fluence between a "quiet" year and an "active" year can vary by as much as three orders of magnitude. Gradual solar events are events seen as a raised particle flux that slowly decreases over a period of several hours or days. These events can account for a large fluence of protons (10^9/cm^2) in a few days and have been correlated with coronal mass ejections (CMEs). Figure 2.5 plots major proton events for

three previous solar cycles. More abrupt impulsive events lasting a few hours are seen as large increases in the fluence of heavy ions.

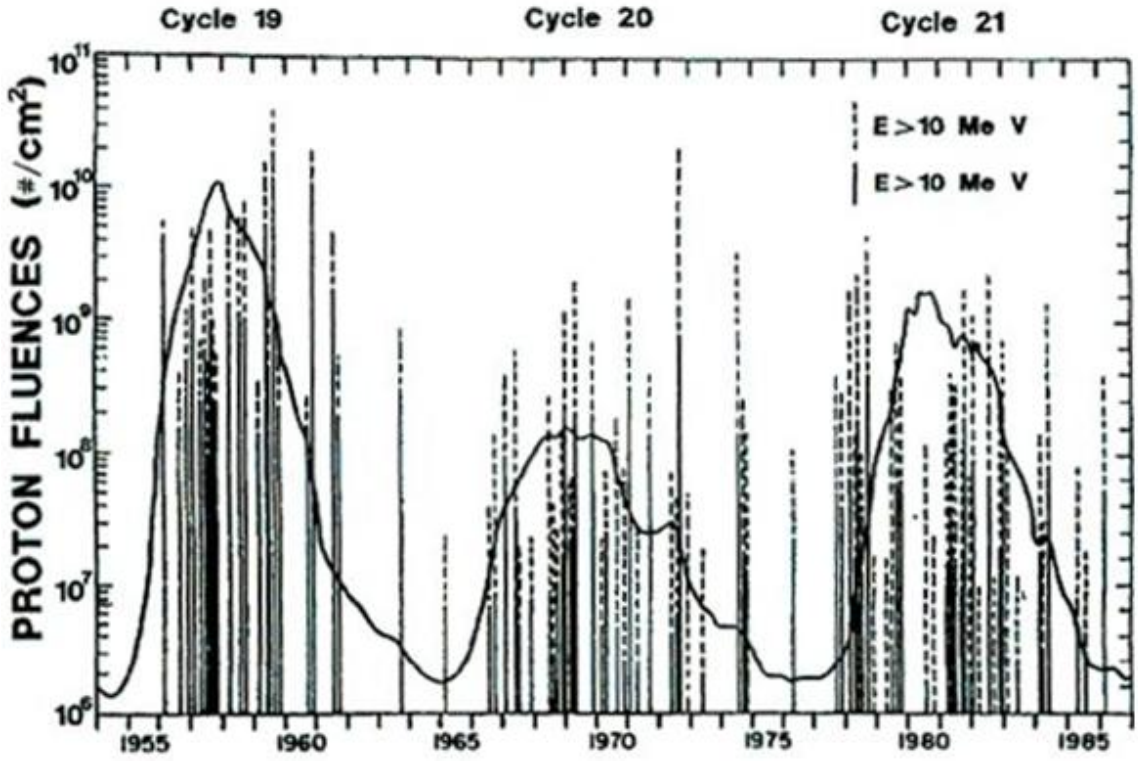


Figure 2.5. Solar activity and solar proton events for cycles 19-21. Multiple events exceeding fluences of 109 protons over 10 MeV in energy are shown for each active sun cycle. The right Y-axis maps these events to the Zurich (or Wolf) Sunspot Number which gauges solar activity [31, 32].

Whereas solar events are responsible for the ebb and flow of particle flux seen by a spacecraft, galactic cosmic rays (GCRs) form the backdrop of the radiation environment. Because cosmic rays come from multiple sources outside of our solar system, they are more of a constant presence. The variance in the fluence of heavy ions due to galactic cosmic rays is much less dramatic than what is seen by proton fluence in a given year. The variance in GCRs that is observed is created by solar winds that serve to prevent some of the encroaching cosmic rays from entering our solar system. Thus,

radiation received from GCRs is reduced during active periods in the solar cycle and increased during quiet periods. The particle composition of GCRs is shown in figure 2.6.

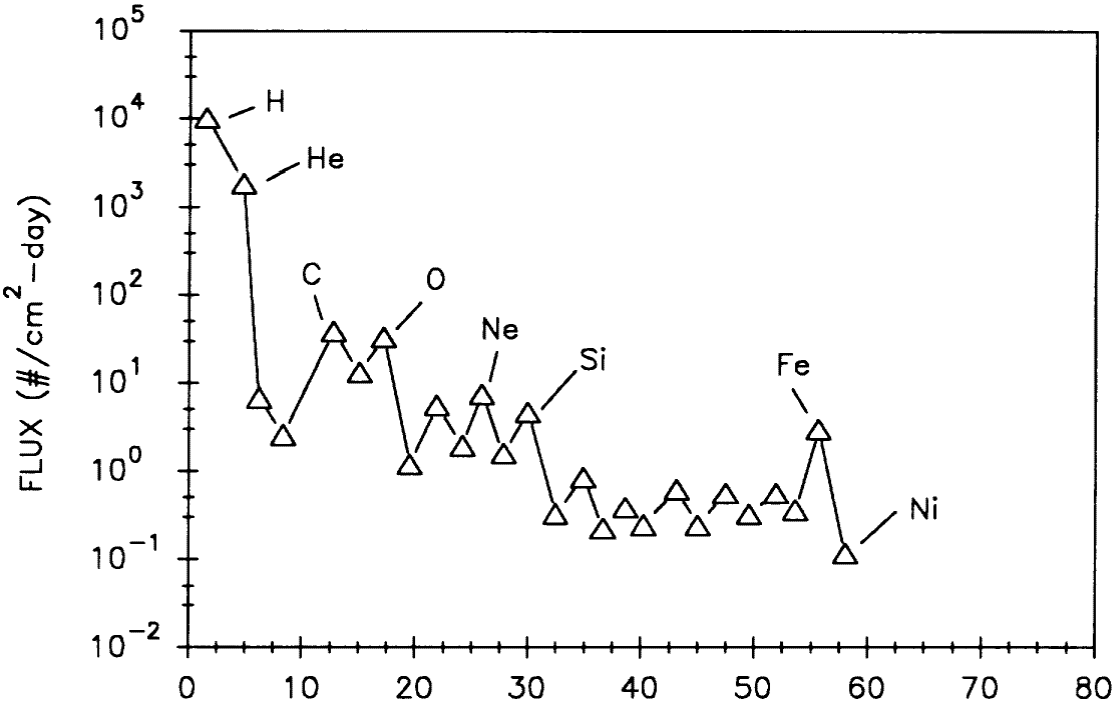


Figure 2.6. Flux of the different particles comprising galactic cosmic rays [10].

The vast majority of these particles are protons and alphas with about 1% of the particles being heavy ions. Although they compose such a small percentage of GCRs, these heavy ions are important because they can deposit large amounts of energy and are therefore very ionizing. Note that ions above the mass of iron have significantly reduced flux and are therefore of less concern when radiation hardening a system.

Mechanisms for Single-Event Effects

The single-event effects that are of concern for this work all are related to the same primary mechanism: collection of charge by the various transistor and circuit elements after an energetic particle passes through a device. The process of this charge

deposition, collection, and transport in semiconductor devices will be covered in this section.

Charge Deposition

There are two basic ways that ionizing particles deposit charge in a device. The first is direct ionization from the primary incident particle and the second is ionization from secondary particles that are created via nuclear reactions of the primary particle and the atoms in the materials of the semiconductor device. When a charged particle passes through the semiconductor material, it deposits energy along its track until it loses all its energy and comes to rest inside the device or exits the device. This deposition of energy manifests itself as electron-hole pairs that are freed along the track of the charged particle by the deposited energy. The standard is to refer to this energy loss as a linear energy transfer (LET) along the route of the ionizing particle. The standard units of LET (and the ones that will be used in this work) are MeV-cm^2/mg. This can be thought of as the energy deposited for unit length (MeV/cm) normalized by the density of the target material (mg/cm^3). A convenient conversion for silicon technology is that an LET of 97 MeV-cm^2/mg corresponds to charge deposition of 1pC/μm. This factor of ~100 makes for quick conversions between particle energy transfer and charge deposition.

Direct and Indirect Ionization

To properly understand the interactions of a particular charged particle with electronic devices, the LET of the particle needs to be understood at various locations as the particle passes through the material of the device. Examples of these curves are shown for different ions in figure 2.7. The figure plots the instantaneous dE/dx of the four ions listed in table 7.2 in silicon in LET units of MeV-cm^2/mg.

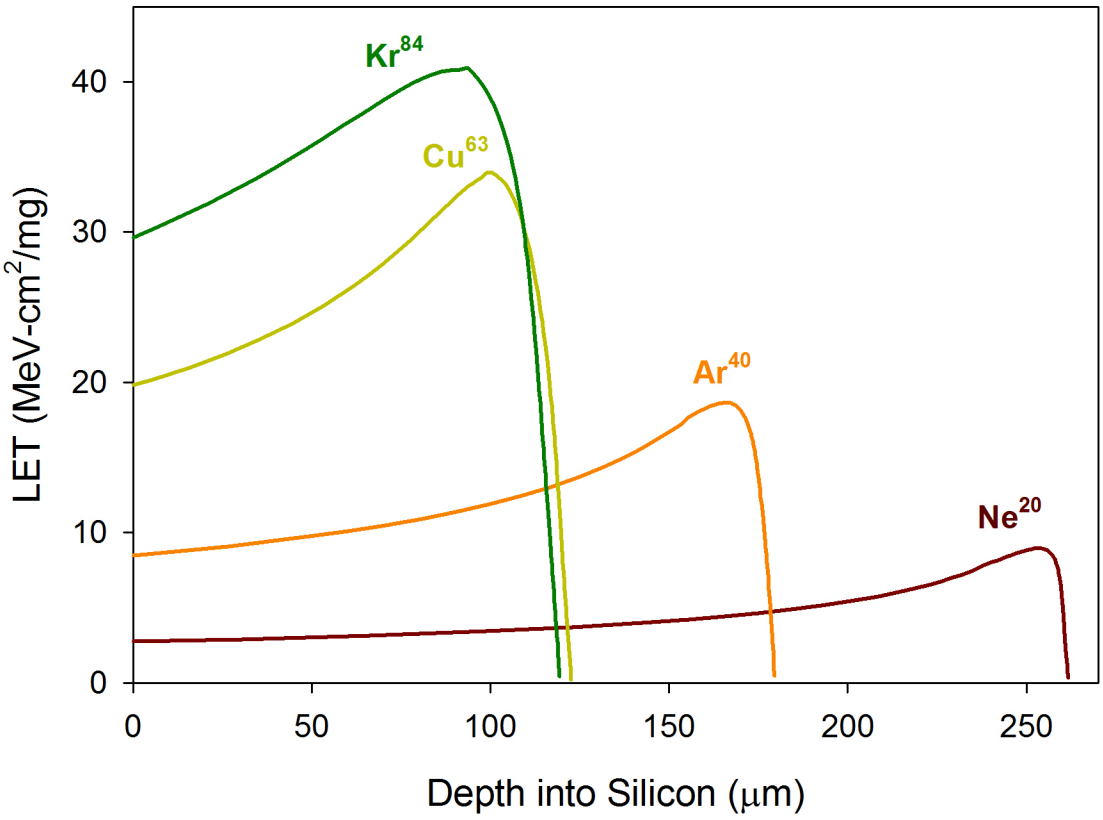


Figure 2.7. Plots of the four ion species listed in table 7.2 in Chapter VI on a silicon target. Instantaneous dE/dx is plotted in units of MeV-cm^2/mg vs. depth into the silicon target [33].

These curves are obtained through computer codes created through the work of Ziegler *et al.* [33] and are referred to as the TRansport of Ions in Matter (TRIM) and Stopping and the Range of Ions in Matter (SRIM).

The direct ionization that would take place due to the energy transfer functions exhibited by the curves shown in figure 2.7 is primarily the domain for single event effects caused by the heavy ions that comprise GCRs. Heavy ions are typically defined as any ion with $Z \geq 2$. Particles lighter than this (such as protons) usually do not cause latchup by direct ionization as their LETs are incapable of producing sufficient charge to induce latchup in most devices. As devices continue to scale to smaller sizes and the

critical charge of devices decreases, this may cease to be true. 10 MeV protons have a peak LET of ~0.5 MeV-cm^2/mg at a range 30 μm in silicon. Proton LET is around 0.05 MeV/-cm^2/mg for the first 20 μm of pathlength [33].

While lighter particles generally do not have a high enough LET to induce latchup in most devices, they still cause errors by depositing charge through indirect ionization mechanisms. For example, a high-energy proton can enter a semiconductor lattice and impact a nucleus in the semiconductor lattice. Two examples of possible resulting inelastic collisions from protons are shown in figure 2.8 [34]. Other examples of potential reactions can be found in [35, 36].

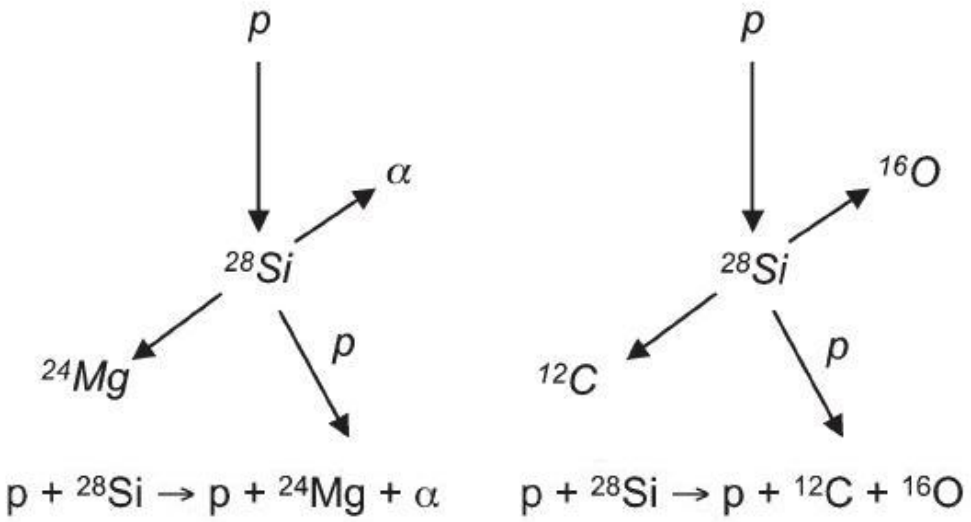


Figure 2.8. Examples of indirect ionization processes for protons in silicon [34].

The first example in figure 2.8a shows the emission of an alpha particle and a Mg nucleus recoil. Figure 2.8b shows one example of a spallation reaction where the impacted silicon nucleus is split into multiple fragments, in this case an oxygen ion recoil and a carbon ion recoil. Most of these products (the alpha and heavy ions) have much

higher LETs than the original incident proton and for purposes of charge deposition can often be thought of and modeled as the independent heavy ions would be.

Charge Transport and Collection

Once charge is deposited in the body of a device as electron-hole pairs, one of three things can occur. The charge can move along electric fields present in the device via drift mechanisms, it can move from areas of higher concentration to lower concentrations via diffusion mechanisms, or it can recombine with other available carriers in the device. This movement of charge in devices creates currents that are seen by the circuit. These currents can result in voltage pulses on circuit nodes (single-event transients, SETs) that are not intended by the circuit. If an erroneous voltage is present at the input to a memory element at the time data is latched, the faulty value will be propagated along the data path. For SEUs as well as SETs, the most sensitive regions are typically reverse-biased p-n junctions. Due to the field placed across those junctions, these junctions are very efficient at collecting charge that is deposited in or near the depletion region. Ion strikes near depletion regions can also collect significant amounts of charge as carriers diffuse to the depletion region and are swept up and collected. For SEL, the issue is not so much the charge collected on a node as it is the current that is generated in a well or substrate. If this current is high enough to drop the potential underneath a source enough to turn a diode on, the part can latch. For SEL the most sensitive regions are typically N-well/P-substrate junctions far away from well and substrate contacts and near source diffusions. More in-depth coverage of charge collection physics is given by Dodd [34]. This includes experimental methods like broad-beam charge collection spectroscopy [37] and measurement of charge-collection transients using ion microbeams or lasers with high

speed sampling oscilloscopes [38]. In other works, microbeams and lasers have been used to map integrated charge collection as a function of position in circuits [39, 40]. The physics of charge collection has also been studied in detail using 2-D and 3-D TCAD simulations [41, 42].

CHAPTER III

LATCHUP IN CMOS DEVICES

Latchup in CMOS devices is a reliability concern for both terrestrial and space applications. Because the basic mechanisms for electrically-induced latchup (circuit-level) and single event latchup are the same, electrical latchup will be considered first without the complication of ionizing radiation.

Electrical Latchup

In bulk CMOS, vulnerability to latchup is created by the presence of a parasitic silicon controlled rectifier (SCR) or thyristor between the power rails. This parasitic device is present whenever NMOS and PMOS transistors are placed next to each other in a circuit layout. When activated, this SCR structure creates a low impedance path across the power supply that can generate very high currents in the structure. These high currents can destroy metal interconnects due to electromigration, a phenomenon where the current passing through a metal line is so high that the metal atoms are displaced by current flow [43-47]. Even in the case of non-catastrophic failures, melting and electromigration from high current pulses have been shown to be a long-term reliability concern to circuit operation [48-52]. Figure 3.1 shows two examples of metallization lines in a circuit after the occurrence of latchup. Figure 3.1a is an example of a catastrophic failure where the circuit is destroyed by the failure of a metal interconnect due to high current from a latchup. Figure 3.1b shows a similar degradation of a metal line where the circuit remains functional after a latchup event, but may have reduced reliability and lifetime. The results from Miyahira et al. [49] shown in figure 3.1 should serve as a warning for the testing and qualification of parts for a radiation environment.

Just because a device seems to survive several latchup events during testing does not mean that all latchup events will be non-destructive or that there is no permanent damage to the device.

Figure 3.1. (a) SEM photograph of metallization failure induced by latchup after the silicon nitride layer was removed. (b) SEM photo of a region damaged from current during latchup where the metallization line remains conductive even though metal has been ejected from over 90% of the conducting metal line. [49].

The parasitic SCR structure is formed by two bipolar junction transistors (BJTs). Both NPN and PNP bipolar devices are present as parasitic elements in a conventional CMOS structure. Because of the requirements for dense packing of paired transistors (NMOS and PMOS) in SRAM cells, latchup can figure prominently in those devices [48]. The electrically-induced turn-on of these parasitic devices can occur in vulnerable devices through device over-voltage or improper power supply sequencing. In a typical P-substrate CMOS technology, lateral NPN parasitic bipolar transistors are created by the N-source, P-substrate, and N-well configuration as well as the N-drain, P-substrate, and N-well configuration. Vertical PNP parasitic transistors are created by the P-source, N-well, and P-substrate configuration as well as the P-drain, N-well, and P-substrate configuration. Because of the typical biasing conditions in a CMOS digital application,

the parasitic transistors involving the PMOS and NMOS transistor drains are ignored. This simplification can be made for an SRAM since adjacent drains are always held at the same potential, creating a biasing situation where it is impossible for both the PNP and NPN parasitic bipolar transistors from being in forward active mode at the same time. This simplified latchup structure is shown in figure 3.2. During normal operating conditions, these parasitic transistors are both off. This PNPN (SCR) device created as a result of the configuration shown in figure 3.2 can be activated and switch from a high impedance state (low current) to a low impedance state (high current). In the SCR device, the PMOS transistor source is the anode and the NMOS source is the cathode.

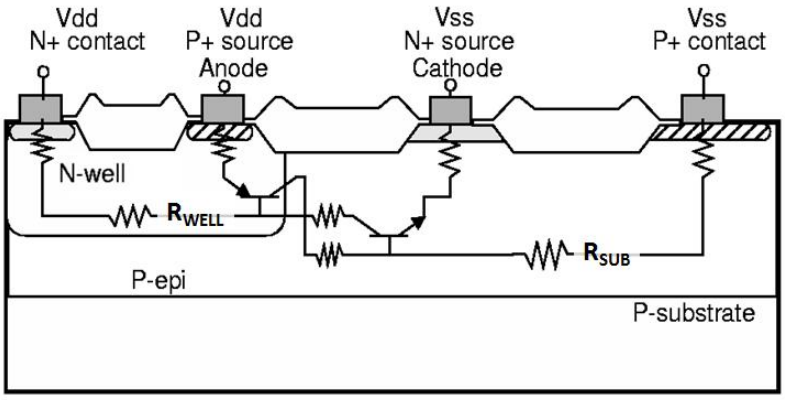


Figure 3.2. Typical CMOS structure showing parasitic components and latch-up path. Well and substrate resistances are added for comparison to inset in figure 3.3. After [53].

An example of the operational curve with a simplified circuit schematic is shown in figure 3.3. This curve shape will change based on doping concentrations, applied voltages, the gains of the parasitic transistors, distances from anode/cathode to well/substrate contacts which modulate resistances, and temperature. The curve shown is for positive injection, with current being forced at the anode (PMOS transistor source) of

the device. Point (V_{TR}, I_{TR}) is the transition between the high impedance region and the negative differential resistance region. These will be referred to as the trigger voltage and trigger current herein. In other literature, they are also referred to as the switching current and switching voltage. V_H and I_H are referred to as the holding voltage and holding current. (V_H, I_H) marks the point where the parasitic device transfers to the low impedance region (seen by the rapidly increasing current.)

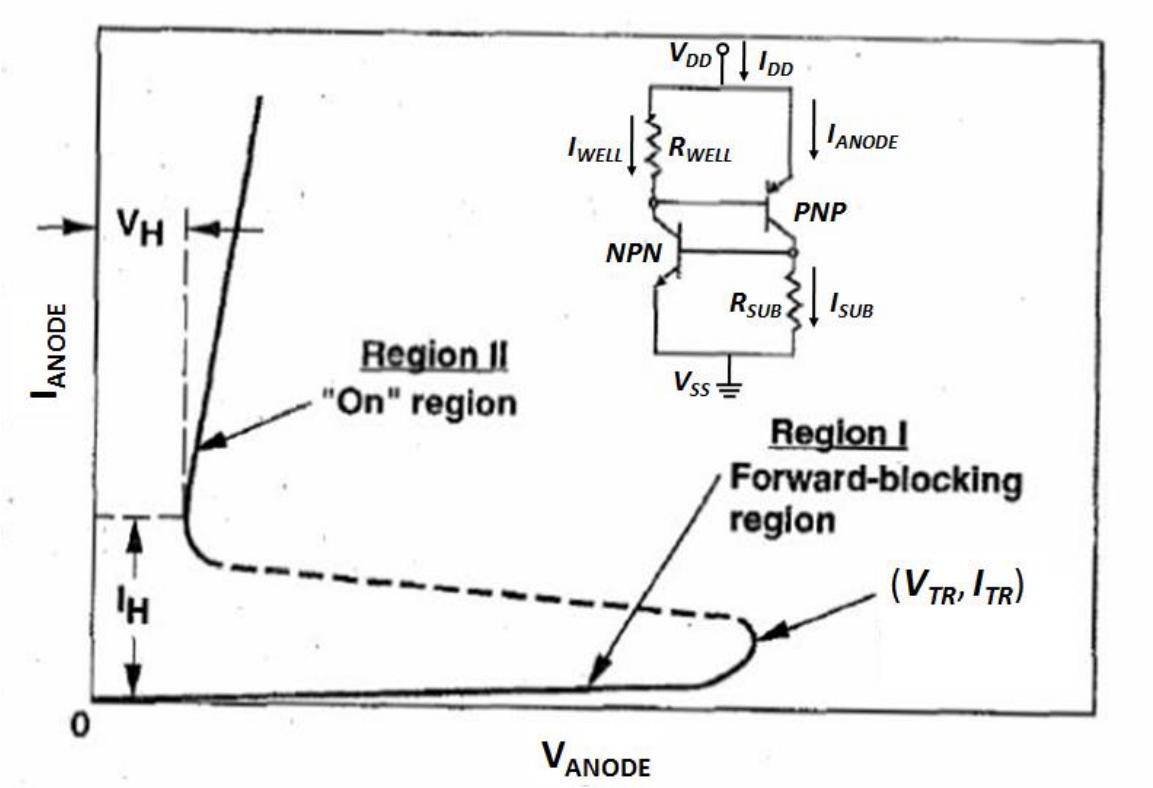


Figure 3.3. Typical I-V characteristics for forward injection of a PNPN structure [54]. Inset: circuit layout of parasitic BJTs with well and substrate resistances from figure 3.2.

For the positive injection curve seen in figure 3.3, there are several distinct sections. At low currents and voltages, the vertical PNP transistor has not yet turned on. For the curve shown in figure 3.3, the N-well is at V_{DD} and the cathode and the substrate

(or P-well) contact are grounded. The anode voltage is increased from zero. Note that under normal device operation, the parasitic CMOS has the above operating conditions with the addition that the anode is also held at V_{DD}. This condition is noted in the inset of figure 3.3. When the voltage on the anode reaches a diode drop past the well voltage (V_{EB} of the PNP bipolar transistor approximately $\geq$ 0.7 V at room temperature) it becomes forward-biased. In the forward-biased condition, increasing anode voltage causes more current flow at the collector of the PNP bipolar transistor, which is the substrate of the device. As the substrate current increases, the voltage drop, V_{BE}, of the lateral NPN increases due to the current across R_{SUB}. When this reaches a diode-drop (V_{BE} of the NPN bipolar transistor approximately $\geq$ 0.7 V at room temperature), the lateral transistor is forward-biased and the SCR device enters a low impedance state seen by the rapid decrease in anode voltage. At this point, the device is in latchup and large increases in current can be seen with minimal increases in anode voltage. A similar curve exists for negative injection, which is the complement of the curve seen in figure 3.3. For negative injection, the lateral NPN bipolar transistor is turned on first followed by the activation of the vertical PNP bipolar transistor.

In order for sustain latchup in a circuit, several conditions must exist. First, the holding voltage for the parasitic structure must be below the supply voltage (V_{DD}). If the operating voltage is below the holding voltage, it is not possible to sustain the low impedance latchup state even if the device is temporarily placed into that state by a fluctuation in voltage or current. There is only one solution for the current value of the SCR structure for $V_{ANODE} < V_H$ in figure 3.3 and it lies in the high-impedance (normal operation) section of the curve noted as the forward-blocking region.

The second requirement is another circuit biasing condition. If the circuit is unable to supply a current of I_H, the parasitic device will not be able to enter the low impedance state. Thus, compliance limits for current are often set when operating devices where latchup is a concern. This often prevents the device from entering a latched state and prevents damage to interconnects from high currents.

Third, the total gain of the feedback loop created by the parasitic devices (shown as a circuit schematic inset in figure 3.3) has to be greater than one. This feedback is created by the fact that the base of each of the transistors is the collector of the other transistor.

$$\beta_{npn}\beta_{pnp} > 1 \qquad (3.1)$$

If this product is below unity, any current due to a single event strike will die out instead of creating latch up. In addition to this, the currents in the N-well and substrate must be sufficient to create the voltage drops necessary to place the parasitic bipolar transistors into forward active mode. This creates the following (approximate) requirements for latchup at room temperature:

$$I_{WELL}R_{WELL} \geq 0.7\,\mathrm{V} \qquad (3.2)$$

and

$$I_{SUB}R_{SUB} \geq 0.7\,\mathrm{V} \qquad (3.3)$$

where R_{WELL} and R_{SUB} are the resistances seen between the well contact and the anode and the substrate contact and the cathode. I_{WELL} and I_{SUB} are the currents flowing

through the well and substrate. Voldman [55] and others [56, 57] give a more stringent beta product requirement based upon the needed potential drops in Eq. 3.2 and 3.3. This is equation (3.4) seen below

$$\beta_{npn}\beta_{pnp} \geq \frac{I_{ANODE} + I_{SUB}\beta_{npn}}{I_{ANODE} - I_{WELL}\dfrac{\beta_{npn}+1}{\beta_{npn}} - I_{SUB}} \tag{3.4}$$

where I_{ANODE} is the supply current. It is an important detail that many of these parameters are strongly related to device temperature. This will be discussed later in this chapter. Due to the aforementioned conditions for latchup, the layout, biasing conditions, and temperature are of the utmost importance in the determination of whether latchup can occur. These factors will be discussed in the section covering design concerns and current mitigation techniques for latchup.

Single Event Latchup

Ionizing particles can produce transient currents in analog and digital CMOS structures that can be amplified by parasitic devices inherent in the CMOS topology. This form of latchup is referred to as single-event latch-up (SEL) This phenomenon was observed as early as 1979 [58] and was originally considered in papers centered on examining the creation of latchup [59-61] and followed by those centered on explaining the effect through physics and modeling [48, 62, 63]. Other thorough reviews have covered SEL [48, 51, 54, 56-58, 64-88] and much of the information here is drawn from those discussions. SEL was initially observed only with heavy ions and bulk CMOS technology. Since then, it has been observed on epitaxial processes [65, 89], and has been

seen to be caused by both protons [66, 68, 70, 73, 76, 84, 90-92] and neutrons [80, 81, 86, 93] on newer technologies.

It should be noted that latchup and SEL do not occur in silicon-on-insulator (SOI) technology as the NMOS and PMOS transistors are isolated in separate volumes of silicon. SOI fabrication technology by its nature prevents the presence of the parasitic PNPN structure.

As mentioned previously, the triggering process for SEL is very similar to the process for electrical latchup. Johnston [54, 64, 76] and Troutman [48, 62] describe this as a four step progression. The process is initiated by a particle strike that deposits charge in the body or well of the SCR device. The diffusion or drift of this charge is current in the device. Current across the resistance in either the well and/or the substrate of the device creates a voltage drop between the base and emitter of one of the parasitic bipolar transistors. If this voltage drop is large enough to place one of the transistors into forward-active mode, additional current will flow into through the base of the other parasitic bipolar transistor (the collector of the forward-biased transistor). If this in turn causes a large enough voltage drop to place the other parasitic transistor into a forward-active state, the parasitic SCR device will go into latchup, granted it meets the previously stated conditions.

Specially designed structures can be used to test for latchup vulnerability, such as SCR devices that produce curves similar to figure 3.3. However, these types of tests cannot usually be performed on highly integrated parts to check for latchup. It is important to not the differences between electrically induced latchup and single event latchup. While the former is usually handled by preventing improper voltage sequencing

or large currents from ESD, these same techniques do not prevent extraneous charge from being placed directly into a latchup vulnerable device via ionizing radiation.

Environmental Influences on Latchup Sensitivity

When testing a CMOS device for use in a radiation environment, it is important to not overlook the unique issues that the target environment creates. In particular, the issues of concern here are the temperature extremes of the environment, the energies and types of particles the devices are exposed to in that environment, and the different directions from which the particles (or secondary particles from reactions) can intersect sensitive areas of the devices. An understanding of all of these issues is necessary to direct test procedures for qualification of parts. The general goals of single event testing are to (if possible) enable a prediction of device error/failure response in the chosen environment and to bound the response of the part in the environment with a worst case analysis. In this section, several test standards for single event effects are discussed and the factors influencing CMOS latchup sensitivity are covered.

SEE Test Standards

There are several single-event effect test standards designed to account for the aforementioned environmental issues. These are JEDEC test standard JESD57 [9], ASTM standard F1192 [94], and ESA/SCC specification #25100 [95]. The JEDEC test standard JESD57 is only valid for heavy ions ($Z > 2$). The ESA/SCC 25100 is applicable for both heavy ions and protons testing. A summary of the main points of the JEDEC and ESA/SCC test standards similar to Poivey's [96] follows:

- Due to the limited penetration range of ions available at ground level, test devices must be de-lidded for heavy ion testing.

- The ESA/SCC test requires heavy ions with sufficient energy to have a particle range in silicon greater than 30 μm to insure ions can penetrate through the many overlayers in modern processes as well as to account for long collection lengths in some devices.
- Both test standards allow for testing at angle and the JEDEC standard requires an angle of at least 60° from normal incidence.
- Minimum fluence levels for heavy ions are $1x10^6$ ions/cm^2 (ESA/ICC) or at least 100 events above threshold LET (JEDEC). For devices that are more radiation hard, fluence of $1x10^7$ ions/cm^2 are recommended. For protons, the ESA/SCC standard recommends a fluence of up to $1x10^{10}$ ions/cm^2 as well as commenting on the potential need for additional devices due to total dose effects.
- A minimum of 5 exposures (at different LET or proton energies) is required in order to get an accurate measurement of the cross section curve.
- The ESA/SCC standard calls for a sample size greater than 3.
- The ESA/SCC standard requires temperature to be strictly monitored while the JEDEC standard more specifically requires the device to be tested at temperatures covering the expected range of environmental temperatures.

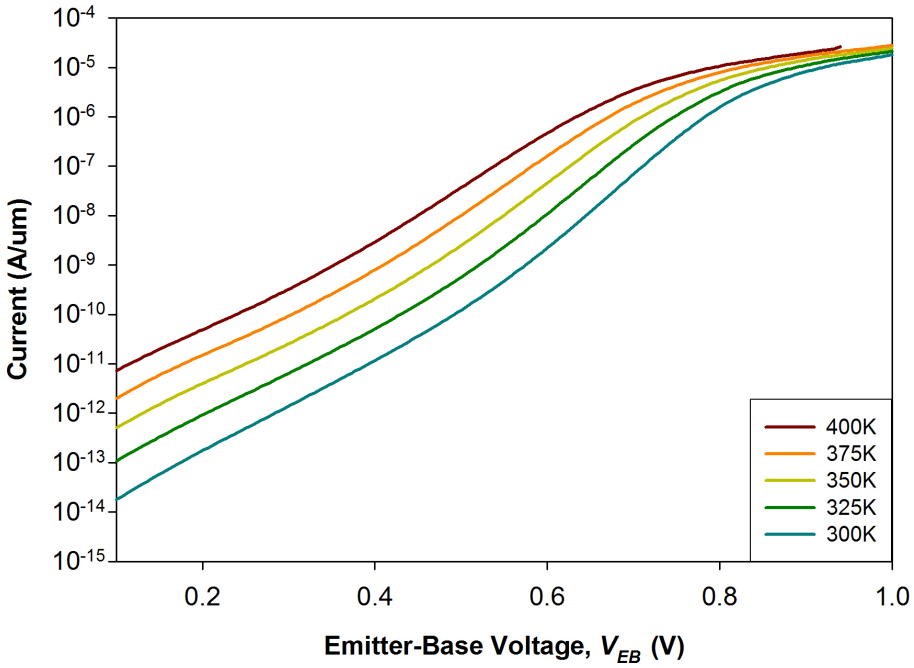
For examining the sensitive cross section of a device with heavy ions or protons the test is typically performed similarly to the following: Initially, the ion or proton beam is oriented with the particles entering into the device perpendicular to the surface of the circuit (normal incidence) and at room temperature. As the test proceeds, the device under test (DUT) is oriented so that particles impinge on the surface at an increasingly grazing angle. The JEDEC test standard requires this angle be at least 60° from normal incidence. In addition to this, the JEDEC standard requires that this test is repeated for

increasing temperatures, up to the maximum target environmental temperature. Both the angular and temperature components of the test are vital and must not be excluded when checking for SEL vulnerability. This work focuses on some of the shortcomings of these test standards and these issues are discussed in both Chapters V and VI.

Effects of Temperature on Single Event Latchup

Researchers have shown that elevated temperatures and higher operating voltages cause higher sensitivity to SEL [54, 86, 87, 97-99]. The increase in well or substrate resistance reduces the current required to achieve a diode drop in the N-well or substrate and initiate the latchup process due to increased resistivity from thermal scattering (See equations 4.3 and 4.4). The resistivity in silicon scales as $T^{3/2}$ within the operational temperature range for most silicon devices. In addition to this, increasing temperature reduces the voltage necessary to turn on the emitter-base junctions of the parasitic bipolar transistor. Figure 3.4a shows a 2D TCAD simulation of the diode formed by the P-source/N-well junction in an SCR device using the 65 nm technology examined in this work. Increasing the temperature generates more current at lower emitter-base voltage, V_{EB}. Similarly, figure 3.4b shows the diode formed by the P-substrate/N-source junction in the SCR device. Current is plotted vs. the base-emitter voltage, V_{BE}. Both plots in figure 3.4 indicate that the voltage drops required to turn on (place in forward-active mode) the parasitic bipolar transistors decrease with increasing temperature. The result of this is a decrease in the voltage between the anode and the cathode necessary (the holding voltage) to maintain latchup. The combination of: 1. increased current from an identical biasing condition (resulting in lower holding voltages) and 2. increased well and substrate resistances that lead to larger voltage drops for an identical single event combine to

significantly increase SEL vulnerability with increasing temperature. In many cases, the temperature environment will determine whether latchup is observed or not. Additionally, for a given temperature where a device is SEL vulnerable, increases in operating voltage (V_{DD}) create a larger difference between the operating voltage and the holding voltage. Non-SEL-vulnerable devices at a given temperature can also become vulnerable to latchup by increasing the operating voltage above the holding voltage.



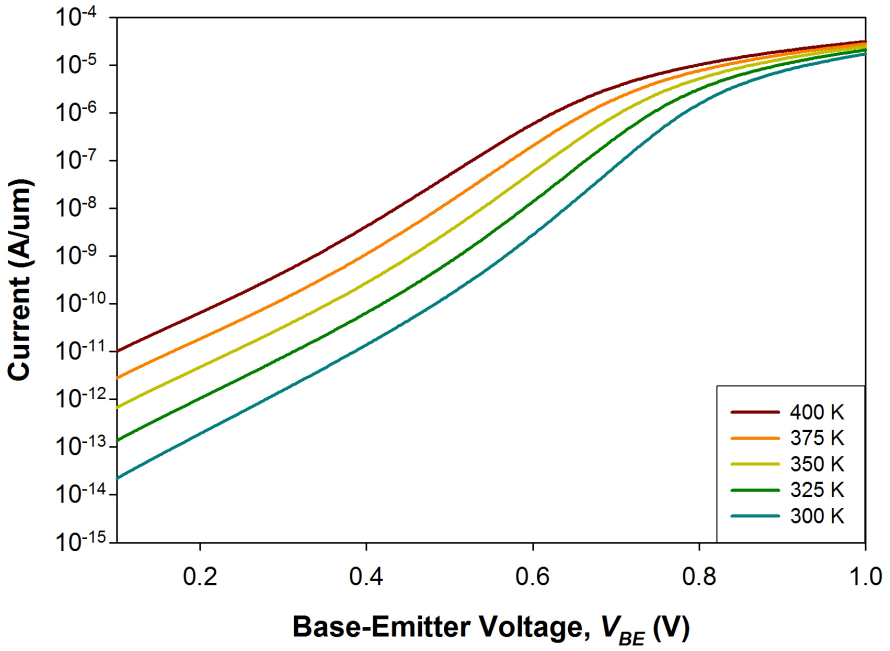


Figure 3.4. I-V curves for (a) an emitter-base (P-source/N-well) junction and (b) a base-emitter (N-source/P-well) junction in 65nm CMOS technology. Changing the environment temperature results in exponential changes in current, allowing the parasitic bipolar transistors to turn on at lower voltages.

Figure 3.5 shows these combined effects of temperature on SEL in the form of a SEL cross-section for a device. In this example, the change from room temperature to 125 °C results in an order of magnitude increase in SEL cross-section. Also, the threshold LET at which the part becomes vulnerable is halved. Reducing the threshold LET increases the range of ion LETs in the GCR spectrum that the part is vulnerable to (see figure 2.6). For a similar reason, the reduction in threshold LET can make the part more sensitive to the proton environment as it increases the range of LET from secondary particles from nuclear reactions that can latch the device (for example, the middle-left and middle-right of figure 3.10. More on this in the next section).

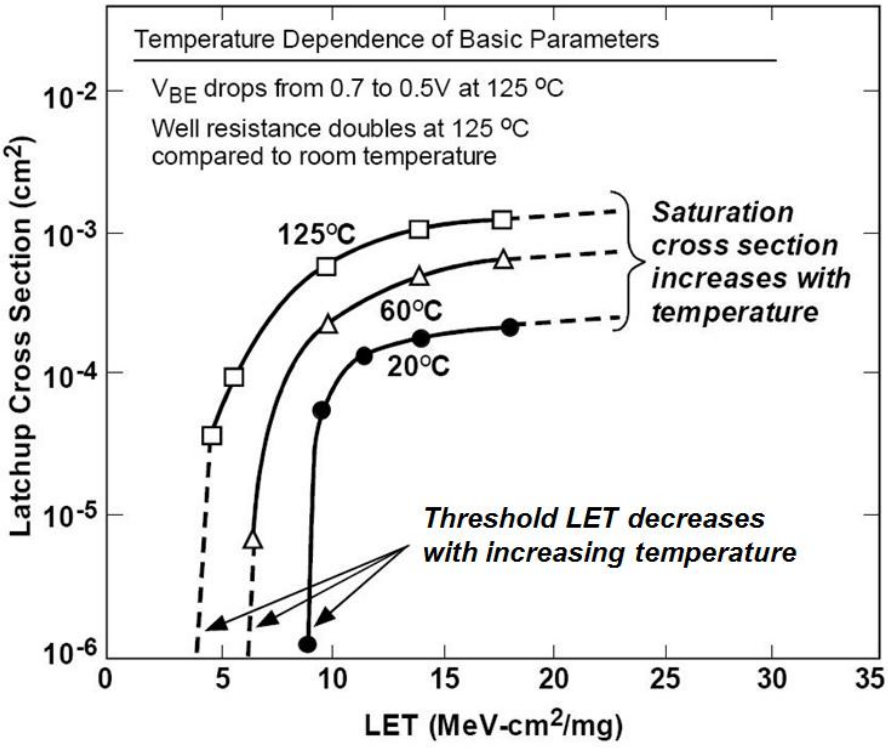


Figure 3.5. Temperature-dependence of SEL cross sections for heavy-ion tests. Cross-section increases and threshold LET decreases with increasing temperature. The cross section increases by more than an order of magnitude and the threshold LET is halved changing from room temperature to 125 °C [100].

Effects of Particle Angle of Incidence on Single Event Latchup

When considering the effects of angle of incidence for testing with ionizing particles, it should be understood that in the space environment, the flux of particles will be approximately isotropic (sans shielding). The volumes of semiconductor material that are sensitive to upset via charge deposition and collection processes are determined by the circuit and individual transistor layouts of a device. In many cases, increasing the angle of incidence from normal (perpendicular to the surface of the device) of an ionizing particle increases the amount of charge that can interact or be collected by those devices. Several models for dealing with the effects of angle are described in this section.

During ion strike SEE testing, it is common practice to use angled ion strikes to mimic normally incident particles with a higher LET [101-103]. This practice is based on the concept of a thin and wide sensitive volume in a device. This model is used to create an *effective* LET during beam testing. Changing the angle at which a particle passes through the thin sensitive volume increases the path length through that volume, thus depositing more energy. This ratio is 1/cos(θ) where θ is the angle from normal incidence [101]. Example thin volumes and calculations of effective LET with changing path lengths due to angle are shown in figure 3.6. The path length of an ion through the thin sensitive region increases as $L_{eff} = L / \cos\theta$ where L_{eff} is the pathlength of the ionizing particle through the sensitive volume, L is the thickness of the sensitive volume, and θ is the angle of incidence. As the pathlength of an ion through sensitive regions increases, so does the total energy deposited in the sensitive volume. The effective LET is similar with $LET_{eff} = LET / \cos\theta$ where LET_{eff} is effective LET of the particle through the thin sensitive volume and, LET is the linear energy transfer of the particle in the material.

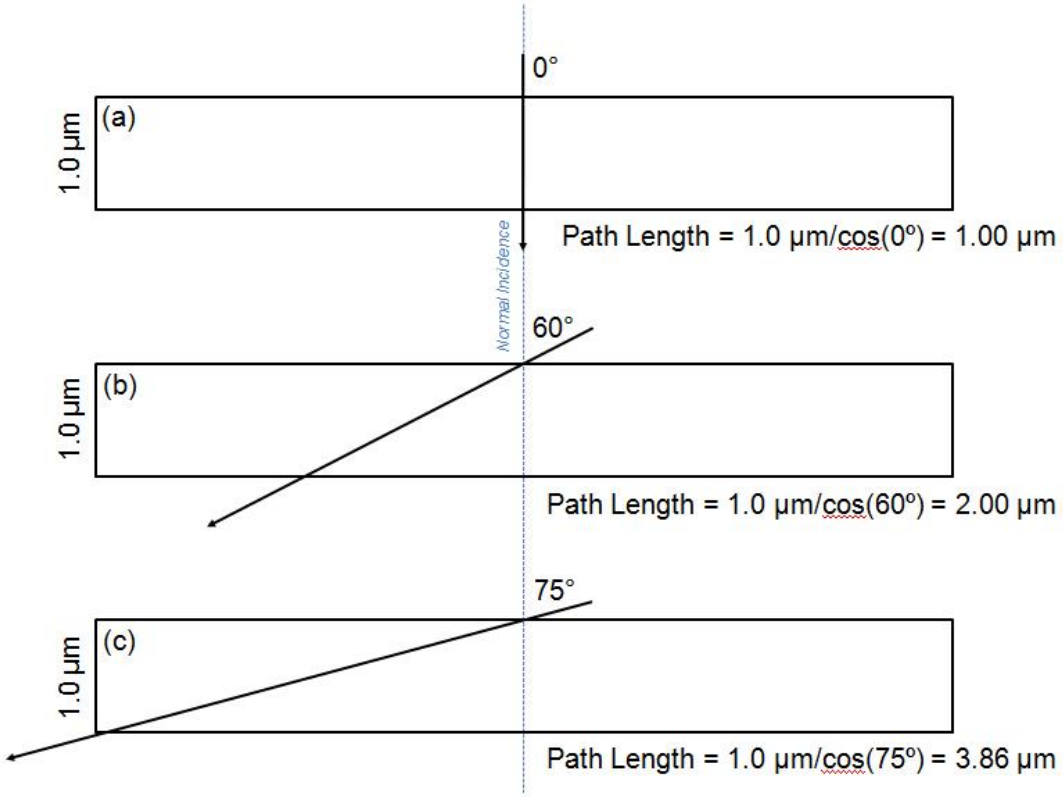


Figure 3.6. Demonstration of ion path lengths through shallow 1.0 µm deep thin sensitive volume structures at varying angles of incidence. The increasing path length with increasing angle of incidence (and thus increasing energy deposition can be seen. The 60º incidence strike shown in (b) is twice as long as the normal incidence strike. The 75º incidence strike shown in (c) is almost four times as long as the normal incidence strike.

There are known shortcomings of the effective LET model [101, 104-109]. While this model accurately describes the change in charge deposition in the semiconductor material with variations in angle of incidence, many sensitive volumes are not thin or wide and flat when compared to their depth. The effective LET model cannot be used to model effects where there is 1) a difference in SEE sensitivity based on lateral orientation [110], 2) a device with a large collection depth relative to the lateral dimensions (often due to longer diffusion collection times for SEL [64]), or 3) geometry that constrains charge collection/interaction depending on lateral orientation, e.g., the sensitive volume is

more box-shaped than flat [106]. All of these are true of the SRAM structures examined in this work.

A more flexible approach is to approximate sensitive volumes in devices using rectangular parallelepipeds (RPPs) of variable shape. The RPP model for a sensitive volume has been used to understand many single event phenomena in devices. These models approximate the response of a small number of sensitive devices in a circuit by using collection volumes in regions where devices are sensitive to errors from deposited charge. Models similar to this have been used extensively over the last 20 years [64, 104, 111-123] to explain the angular effects seen in sensitive device cross-sections. More advanced versions of these models often use multiple weighted volumes to model charge collection efficiency [124, 125]. The RPP model has also been used for SEL [91] and while a single sensitive volume approximation may be an oversimplified fit to existing data, the model gives a good understanding of how energy deposited in sensitive regions varies with angle of incidence.

Due to the fact that ionizing particles intersecting device structures at different angles can generate differing amounts of charge, it is important to consider the effects of beam orientation relative to a device under test (DUT). Without examining the effects of radiation from different angles, the sensitivity of the DUT can be under- or over-estimated. Even the JEDEC and ESA/SCC test standards are often not thorough enough in this area of concern when determining SEL susceptibility. Whereas unexpected SEUs can often be dealt with through error detection and correction systems (EDAC), the destructive nature of SEL often means that even a single latchup cannot be tolerated by the system. Specifically, two vulnerabilities are present in these test regimens. First,

assuming an isotropic environment, testing at only up to a 60° angle from normal incidence only covers 50% of the particles in the environment. This is demonstrated in figure 3.7. For a device that is located in the center of the sphere, ions incident at only up to 60° from normal incidence cover only the green portion of the sphere. Angles from 60° to 90° from normal incidence are in the red portion of the sphere and are unaccounted for when testing only the range of 0° to 60° from normal incidence.

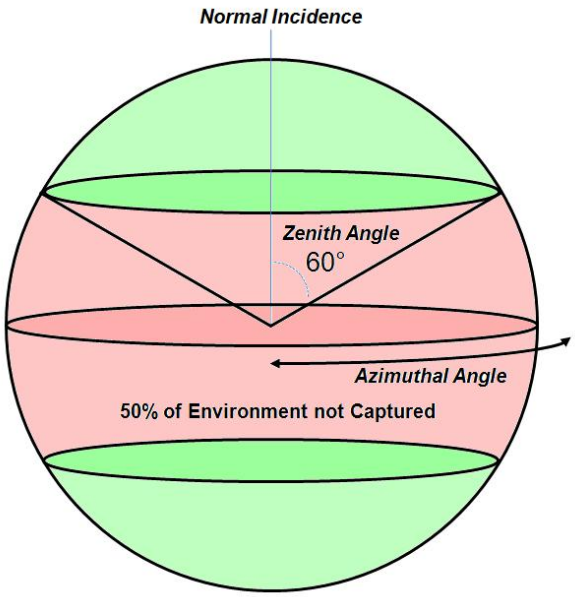


Figure 3.7. Conceptual graphic of an isotropic environment and coverage by testing 60° from normal incidence. It can be seen that testing at only up to 60° from normal incidence only covers 50% of the solid angle from an isotropic environment. Effects from the top are similar to those entering from the bottom. After [126]. Variance along the azimuthal angle noted in the figure is also not considered by JEDEC test JESD57.

Second, the test standard assumes no variance in susceptibility with changes in the lateral orientation of the beam. More precisely, if the normal incidence is parallel to the Z direction in the device, the test standard does not account for rotation of the DUT in

the XY plane. In polar coordinates, the only angle of rotation in the test standard is the polar angle and changes in the azimuth are not accounted for. This is noted in figure 3.7.

Proton Induced Single Event Latchup

While an RPP method can be used for determining the energy deposition in sensitive volumes from heavy-ions, it alone is not sufficient for dealing with the effects of protons. Protons don't typically have a high enough LET to cause SEU or SEL by direct ionization. Instead protons cause upsets by creating secondary particles with higher LETs than that of the protons. Because of the involvement of the nuclear reaction, changing the angle at which protons intersect the device does not directly change the deposition path of the resulting secondary ions. More precisely, changing the angle of the protons does not uniquely define the direction of the secondary particles. In addition, because of the very short range of the secondary products (at least those capable of producing SELs or SEUs), the secondaries may not penetrate into the sensitive areas of the device and the angular effects for protons may be very different than those seen for heavy ions. The effects of angle for proton testing also may vary depending on the device type or technologies. Adams et al. observed a 5x increase in SEL cross section for 60 MeV (an energy where the secondaries are mostly forward directed in silicon, see figure 3.10) protons in a 64K memory when switching from a 0° to a 85° angle of incidence [66]. This result is shown in figure 3.8.

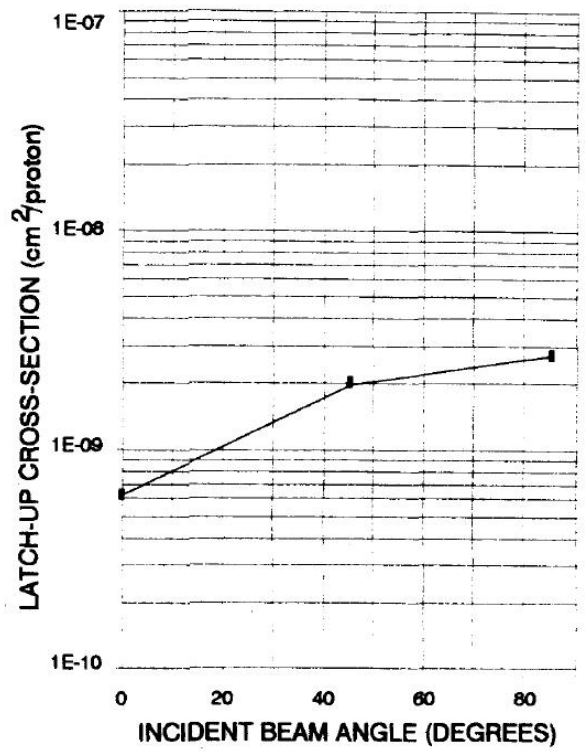


Figure 3.8. (a) 5x increase in SEL cross-section for a 64 K memory when going from normal incidence to grazing angle for 60 MeV protons [66].

Levinson et al. saw less than a 20% change between normal and grazing angles for both SEU and SEL [92] and Johnston predicted that in highly scaled devices, angular effects would be less than a factor of 2x for p-substrate devices due to the small sensitive volume sizes [76]. Recent work by Schwank et al. that covers SRAM technology nodes from 0.14 μm to 0.35 μm shows significant effects of both angle and temperature for protons. Other work by Schwank et al. [87, 127] demonstrated the need for testing at the maximum proton energies that would be seen in the given environment. An example of this is seen in figure 3.9. The cross section for two different SRAM parts is shown to change with increasing proton energies from normal incidence protons.

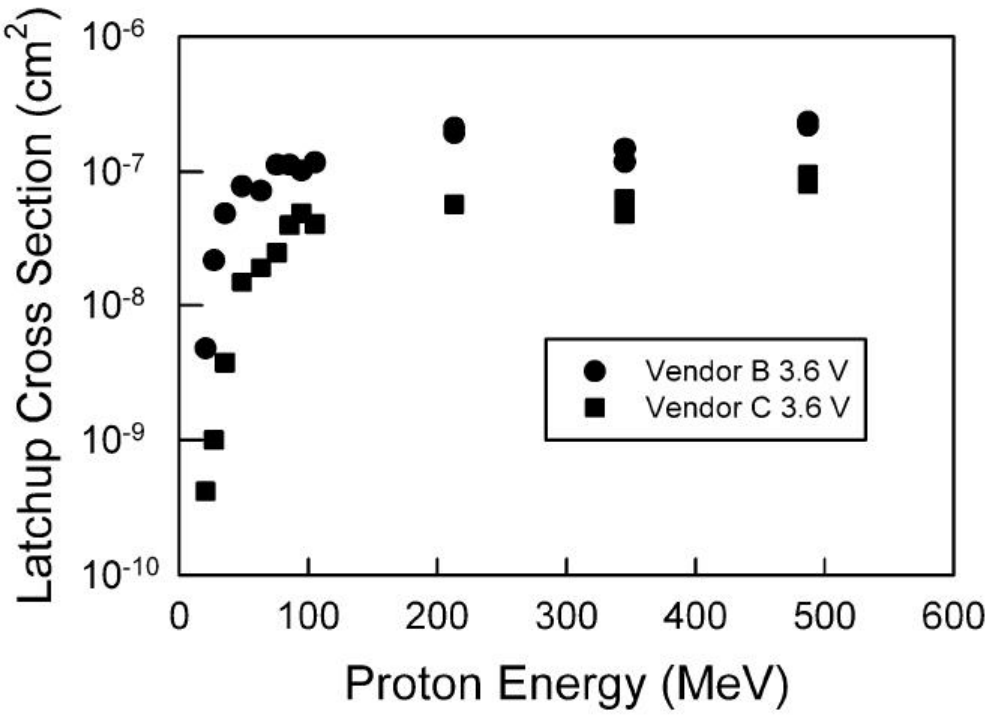


Figure 3.9. Latchup cross section of two memories vs. proton energy at normal incidence [127]

In both plots in figure 3.9, a dip can be seen in the cross section. This is likely due to the different scattering statistics with changes in proton energy. Work by Reed *et al.* [120] can be used to interpret these results. In that study, a different angular effect was seen depending on the energy of the protons. Figure 3.10 shows the result of simulations using the GEANT tool [128].

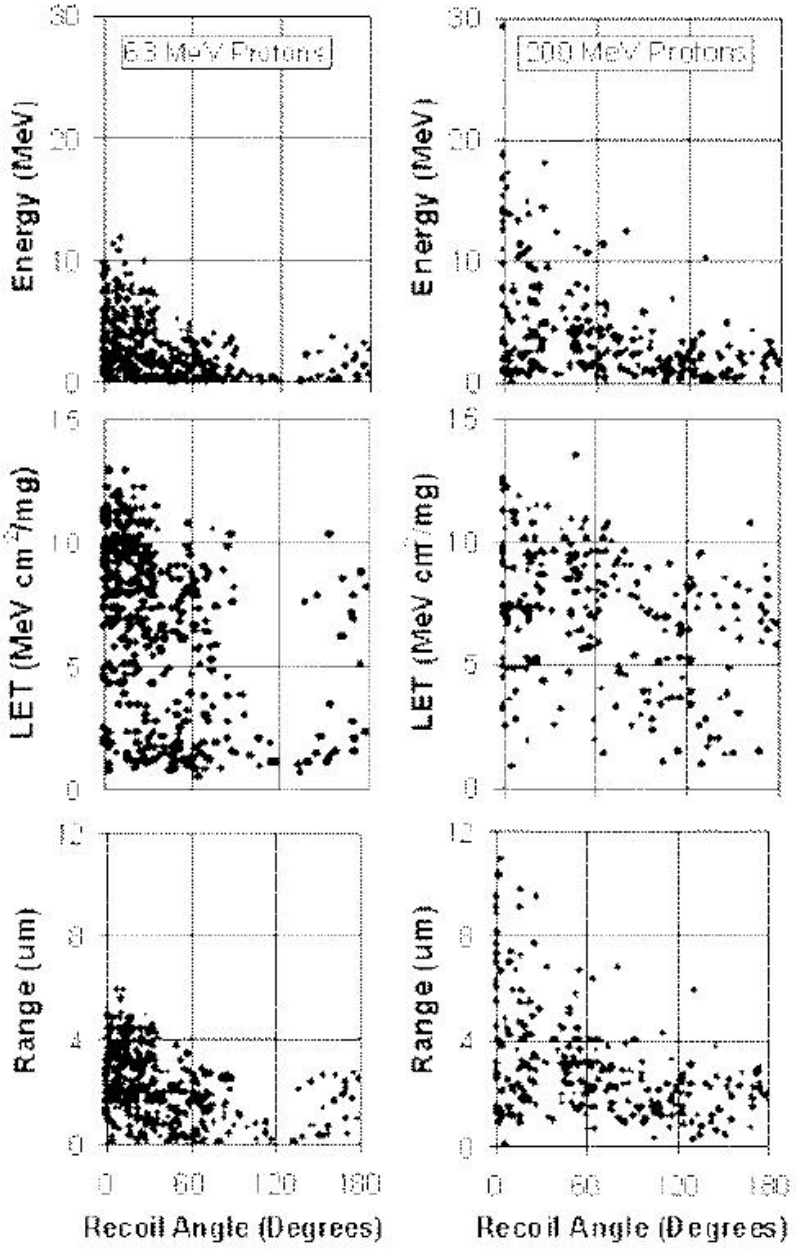


Figure 3.10. Simulated distribution of spallation recoil energy, LET, and range in silicon for 63- and 200-MeV protons [120].

The six panels in figure 3.10 are as follows: The left side if for 63-MeV protons and the right side is for 200-MeV protons. For each side, the top panel is the angular distribution of the energy of the recoiling nucleus (relative to the original proton

trajectory). The middle panel shows the LET distribution of the recoil fragments (in Si) vs. recoil angle and the bottom two panels show the range or the recoil fragment in Si vs. the recoil angle. For both proton energies, the most energetic recoils (longest range, highest LET) are forward-directed and occur more frequently. Lower energy recoils tend to be more isotropic. For Reed's work, a higher upset cross section was seen at grazing angle for 63-MeV protons compared to 200-MeV protons. Schwank asserts [87, 127] that devices need to be tested at the highest proton energy seen in the application environment. While this is true, the work by Reed suggests that a range of proton energies that are seen in the environment should be examined in order to predict device response.

Two more plots are shown here that demonstrate both the impact of proton energy, temperature, and angle on latchup cross sections for SRAMs using modern technology. Figure 3.11 shows the latchup cross sections for a modern 0.16/0.14 μm SRAM with varying proton energy and at two different temperatures. Changing from 25 °C to 85 °C results in roughly a factor of 10 increase in cross section. Many (if not most) modern ICs are within specification operating at 100 °C or above. Figure 3.12 shows the latchup cross sections for a modern 0.14 μm SRAM with varying angle of incidence and at two different temperatures for 105 MeV protons.

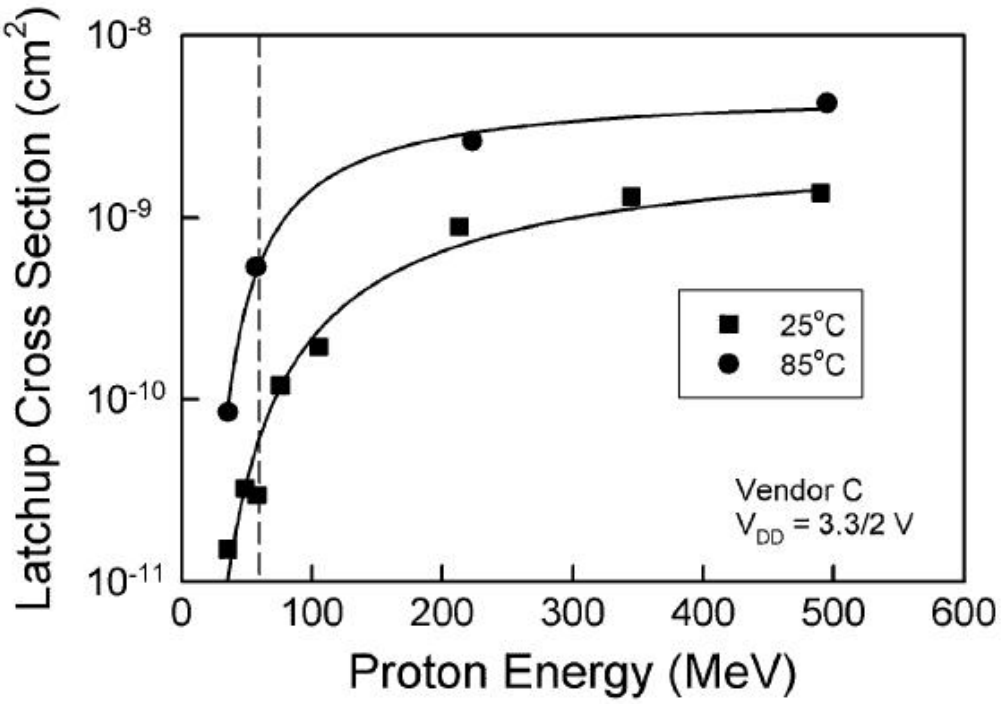


Figure 3.11. Latchup cross section vs. proton energy for 0.16/0.14 µm SRAMs measured at room temperature and 85 °C [87].

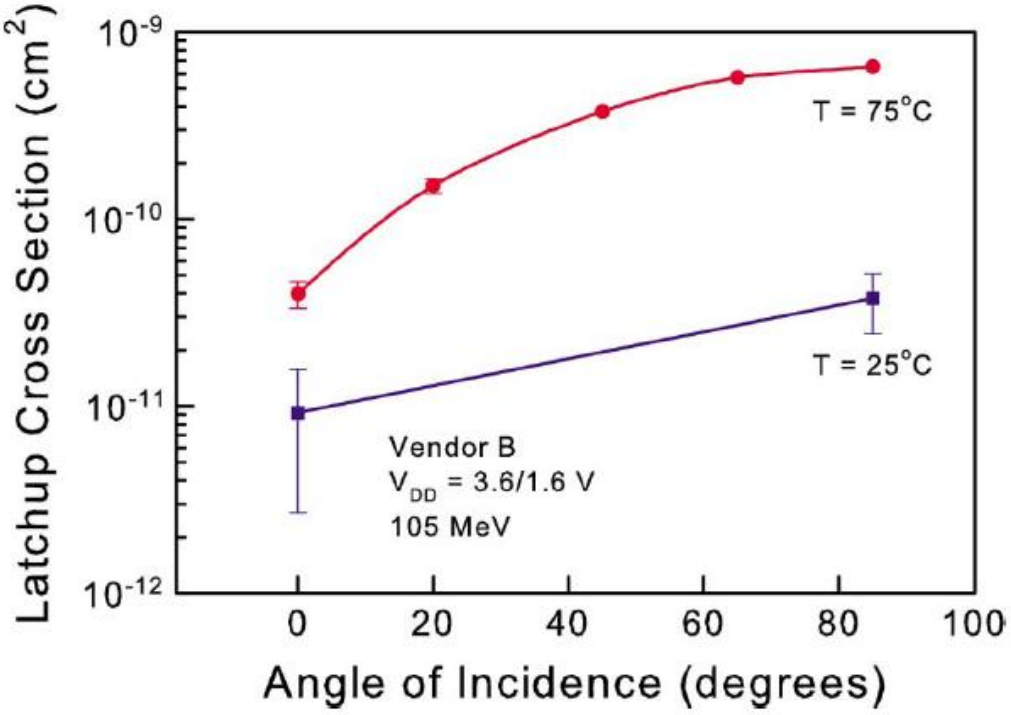


Figure 3.12. Latchup cross section for 105 MeV protons vs. angle of incidence for 0.14 µm SRAMs measured at room temperature and 75 °C [86].

Effects of Scaling on Latchup

Very little work has been reported in the literature describing the effects of scaling on single event latchup. In most cases, each study that has been undertaken only demonstrates the effects of latchup and the sensitivity (or lack thereof) on the current parts that are being studied. One work examined the sensitivity of parts with differing epitaxial thicknesses, which did cover several generations of technology [79]. These technologies are now obsolete and there is not a significant amount of insight that can be gained for current and future technologies. Because of the absence of any studies charting the effects of scaling, the general trends will be summarized here. To aid in these observations, Boselli's work on electrical latchup trends [129] and a recent study by Page and Benedetto on modern 1M and 4M SRAMS [130] will be relied upon.

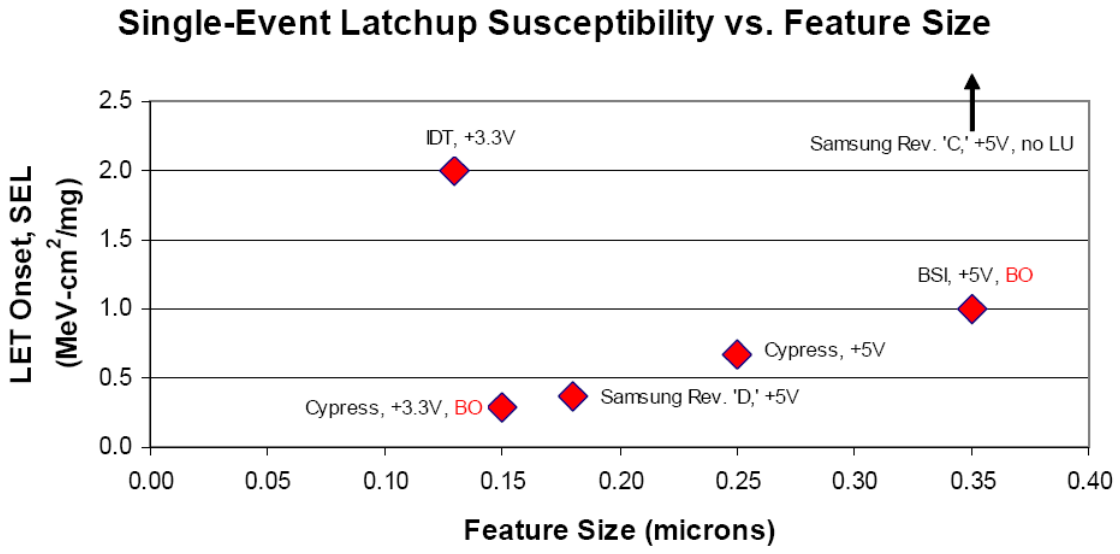


Figure 3.13. SEL susceptibility vs. device feature size for commercial-off-the-shelf 1M and 4M SRAMS. BO indicates a part burn-out (non-recoverable damage) due to latchup [130].

Figure 3.13 is a plot from Page's work. The plot shows the LET threshold for latchup in a number of different SRAMs vs. feature size. For this data set, the general trend is towards increasing vulnerability to latchup as devices get smaller. This should be expected as the amount of charge necessary to latch the two parasitic BJTs in a CMOS SRAM layout should decrease as the devices become smaller and more closely spaced. In addition to this, it can be seen that SEL is still destructive in many devices. The two parts marked with "BO" indicate those memories experienced a burnout from SEL and were permanently damaged. Boselli's work examined SCR structures fabricated at multiple technology nodes with their respective design rules. Several figures of note from that work are replicated here. Figure 3.14 plots the difference in holding voltage and operating voltage for four technologies with minimum (for each technology) anode-cathode design rule spacing at room temperature.

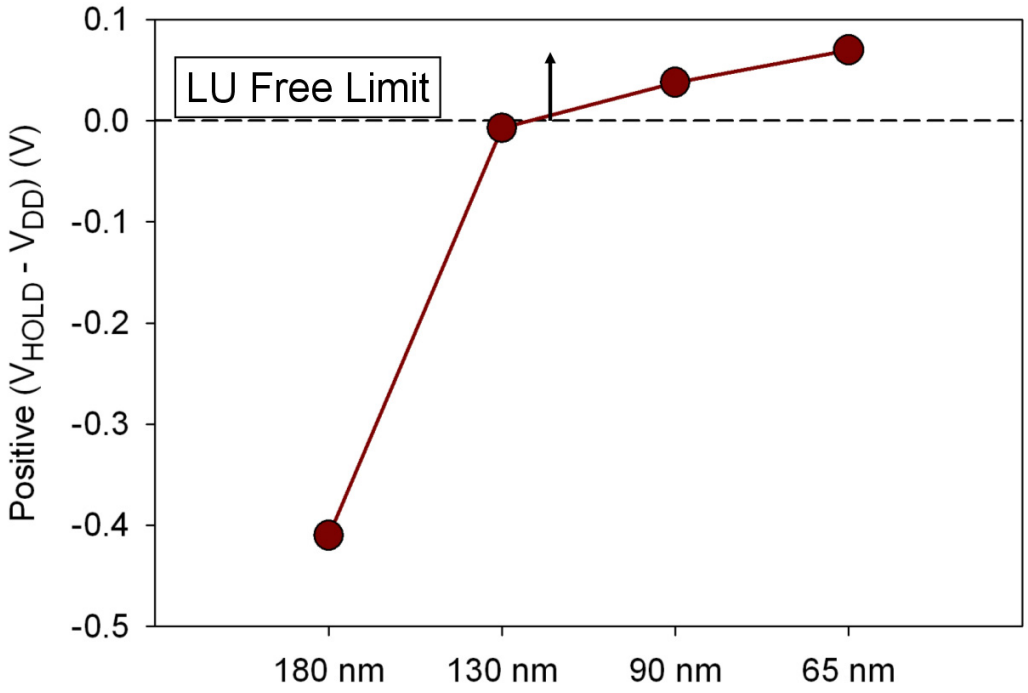


Figure 3.14. Holding voltage minus supply voltage for four technology nodes for positive injection at room temperature. This value increases as technology scales, making latchup harder to achieve [129].

It can be seen that for room temperature the 90 nm and 65 nm technology nodes should become latchup-immune as the supply voltage is unable to sustain the holding voltage necessary for latchup. Figure 3.15 shows the same plot for negative injection of the SCR structures. Here, the same trend is seen with the devices unable to achieve latchup at room temperature due to negative injection at the 130-, 90-, and 65 nm technology nodes.

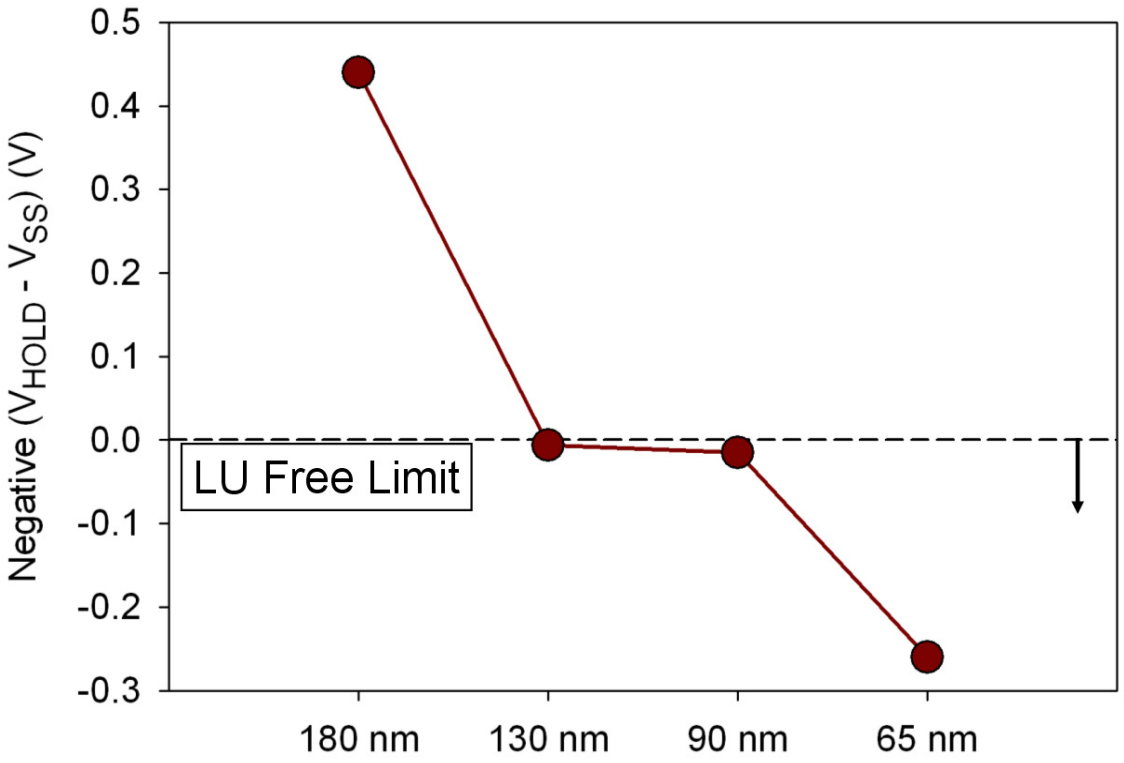


Figure 3.15. Holding voltage minus supply voltage for four technology nodes under negative injection at room temperature. This value decreases as technology scales, making latchup harder to achieve [129].

As discussed in the section covering electrical latchup, the gain product of the two parasitic bipolar transistors must satisfy Eq. 3.4. Figure 3.16 plots the lateral NPN gain of the SCR devices as well as the beta product of the two transistors at room temperature for various technologies. As the technologies get smaller, the product appears to be decreasing below unity, but could also be saturating. In all the technologies covered in figure 3.16, the beta product is large enough for latchup. This leads to the conclusion that for technology nodes as low as 65 nm, latchup is unlikely at room temperature but still possible at increased temperatures.

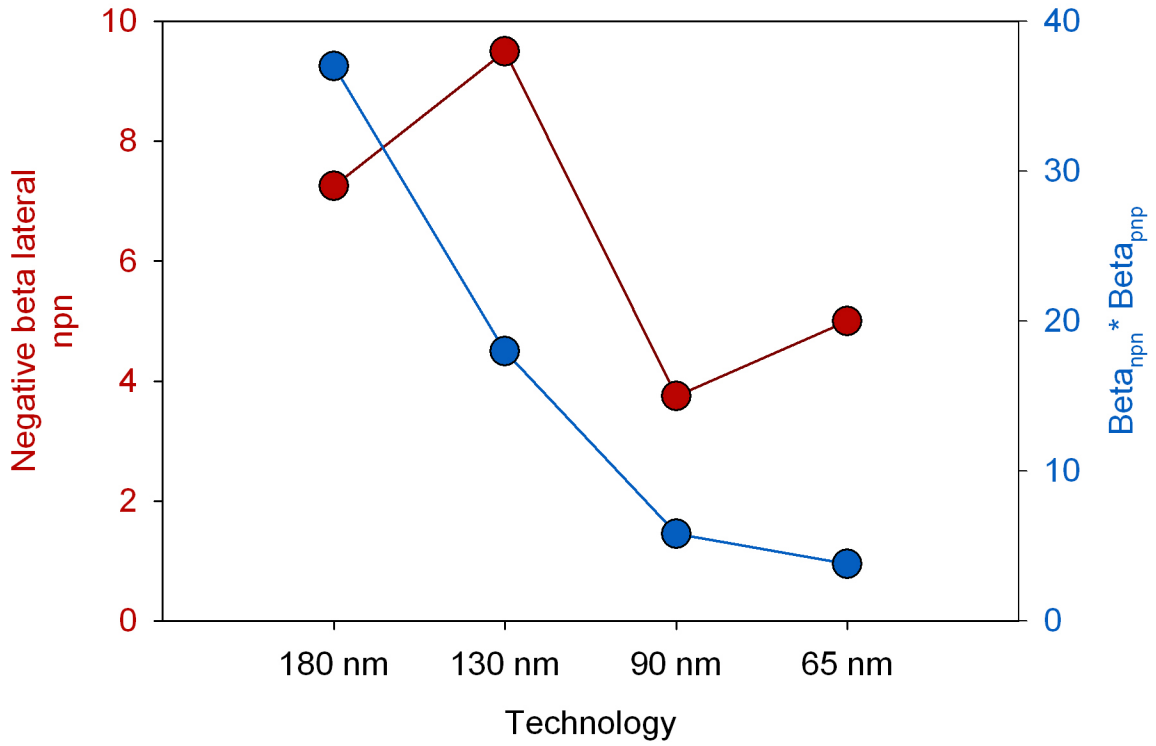


Figure 3.16. Gain of the lateral parasitic NPN transistor (left) and the beta product (right) vs. technology node for SCR devices at room temperature. The beta product decreases as technology scales, making latchup harder to achieve [129].

Figure 3.17 examines the temperature sensitivity of latchup in these devices. This figure shows the rate of change of the holding voltages for both positive and negative injection with temperature. Plots like this also correlate well with the previously shown data of increasing SEL cross sections with increasing temperature. This plot indicates (when combined with figures 3.14 and 3.15) that the 90 nm and 65 nm SCR parts will be immune to latchup below ~325 K and ~340 K, respectively. This observation is significant as it indicates two different scaling trends. As devices get smaller, it takes less deposited charge to see single event effects (including latchup). However, due to the decreases in operating voltages for these smaller technologies, deep submicron devices

are more likely to be immune to latchup at room temperature. These two competing trends would seem to be a reasonable explanation of the decrease in sensitivity observed at the 130 nm node (shown in figure 3.13) of Page's study if the device holding voltage was only slightly below the operating voltage at room temperature. If nothing else, the data show the need for more investigation of latchup sensitivity on deep submicron parts using the entire range of potential operating temperatures.

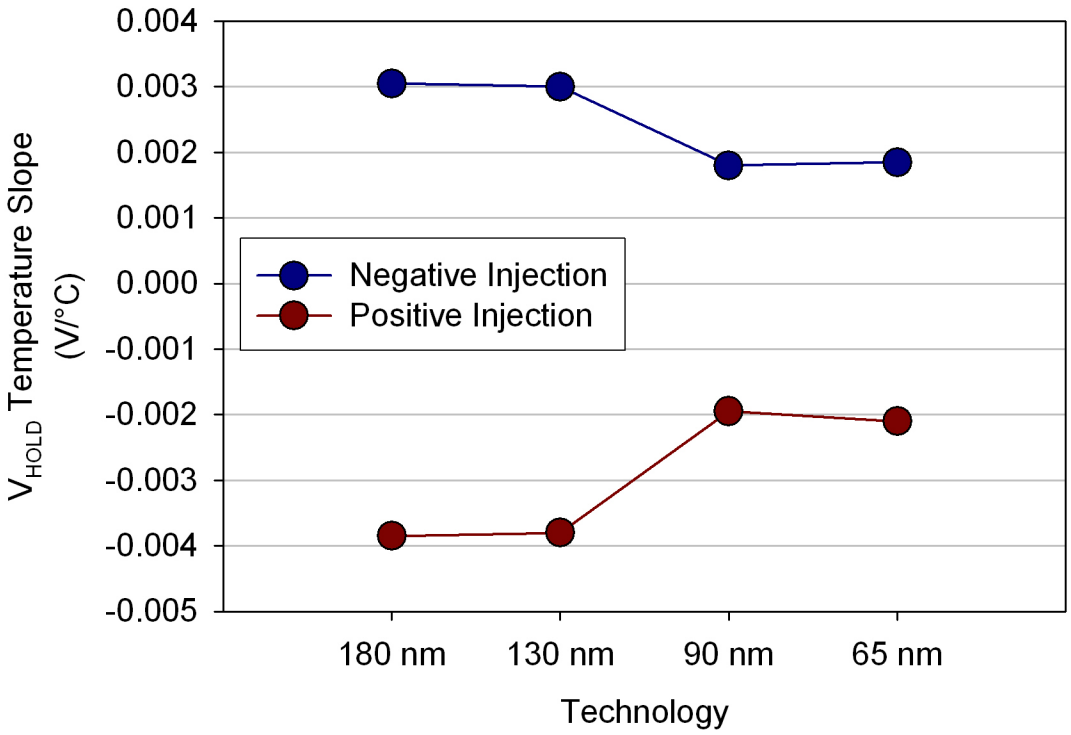


Figure 3.17. Holding voltage (positive and negative) temperature slopes vs. technology node [129]. This data represents the rate at which the value of the holding voltage changes with temperature for SCR devices in four technology nodes.

Single Event Latchup Mitigation

There are a number of techniques that are implemented in an attempt to prevent the occurrence or mitigate the effects of latchup in CMOS devices. Most of the SEL-specific mitigation techniques are aimed at reducing base resistances of the parasitic bipolar transistors or reducing the gains of those transistors. Techniques that try to limit the amount of charge collected in sensitive areas of the devices are also used and are part of a more universal approach to reduce multiple kinds of single event effects in a circuit. One of these techniques, guard rings, is shown in figure 3.18. Figure 3.18a shows the layout for guard rings surrounding both the NMOS and the PMOS transistors along with the cross section for the layout in 3.18b [131]. Amusan [132] describes guard rings as follows:

"Guard rings are p+ or n+ diffusions placed around the well or substrate (i.e., n+ guard rings are placed around the N-well, and p+ guard rings are placed around the P-substrate). Guard rings act as a carrier sink that helps remove the carriers that otherwise would be available to initiate the latchup process. Thus, current flow is interrupted in the positive feedback loop, preventing latchup from ever occurring. There are two types of guard rings:

(1) Majority carrier guard rings which are aimed at mitigating latchup by collecting the majority carriers injected across the well-substrate junction [133].

(2) Minority carrier guard rings which are aimed at mitigating latchup by collecting the injected minority carriers before they are collected by a reversed biased well-substrate junction [77].

Guard rings can be biased or unbiased. Biased guard rings are connected to a power supply and not just the substrate, whereas unbiased guard rings are connected only through the substrate. Unbiased guard rings have been shown to give better performance up to the transition current when it comes to latchup mitigation [134]. They also are preferable because they do not have the power consumption or crosstalk issues of biased guard rings. They are not, however, as well understood as biased guard rings [134]."

Resistance-reducing techniques usually involve increasing the number or size of well and substrate contacts in the chip layout. Studies have shown this to be an effective method in reducing the threshold LET for latchup and in some cases, latchup has been eliminated for test cases with this technique [48]. Increases in doping concentration and reductions in the distances between well/substrate contacts and sources in microelectronics due to scaling also help reduce these resistances [48, 129]. Various techniques are employed to reduce the gains of the parasitic transistors. This is done by increasing the total recombination that can take place in the base of the parasitic BJT. The recombination can be increased by either increasing the recombination rate or by increasing the width of the base of the parasitic transistor. Post-process methods involving irradiating devices to create more recombination centers with displacement damage in the base have been proposed [135, 136] although this could be expensive for mass production of devices.

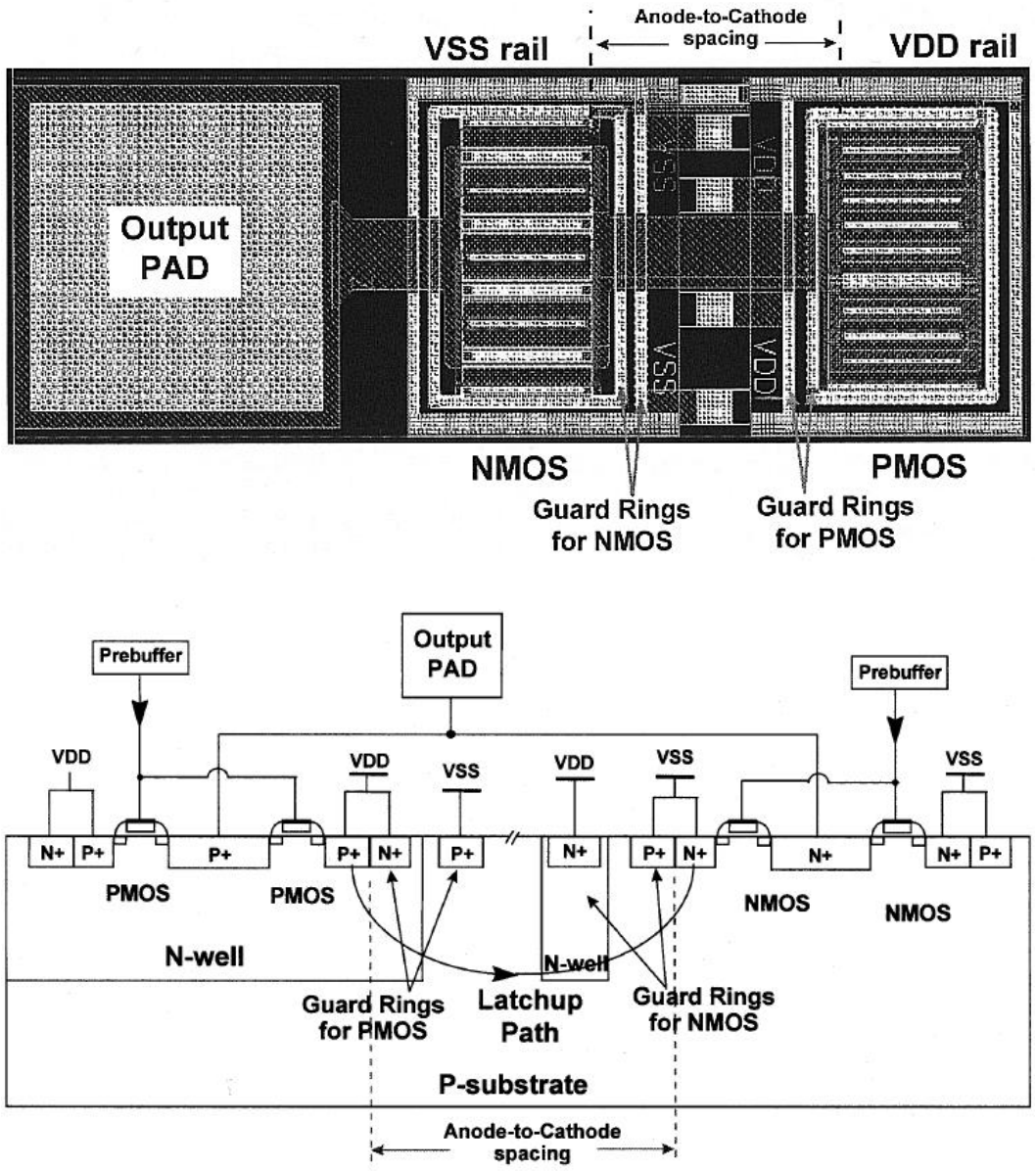


Figure 3.18. (a) Layout example of an inverter output buffer in the I/O cell with double guard rings to prevent latchup in a 0.5μm nonsilicided bulk CMOS process (b) Cross-section of the above device showing the double guard rings around both PMOS and NMOS devices [131].

In many cases, it works in the system designer's favor that CMOS circuits are not meant to have good bipolar performance, so surface recombination (from rough STI/silicon interfaces) and Auger recombination (from highly doped emitters [137]) are usually both much higher than they would be in an analog/bipolar device design.

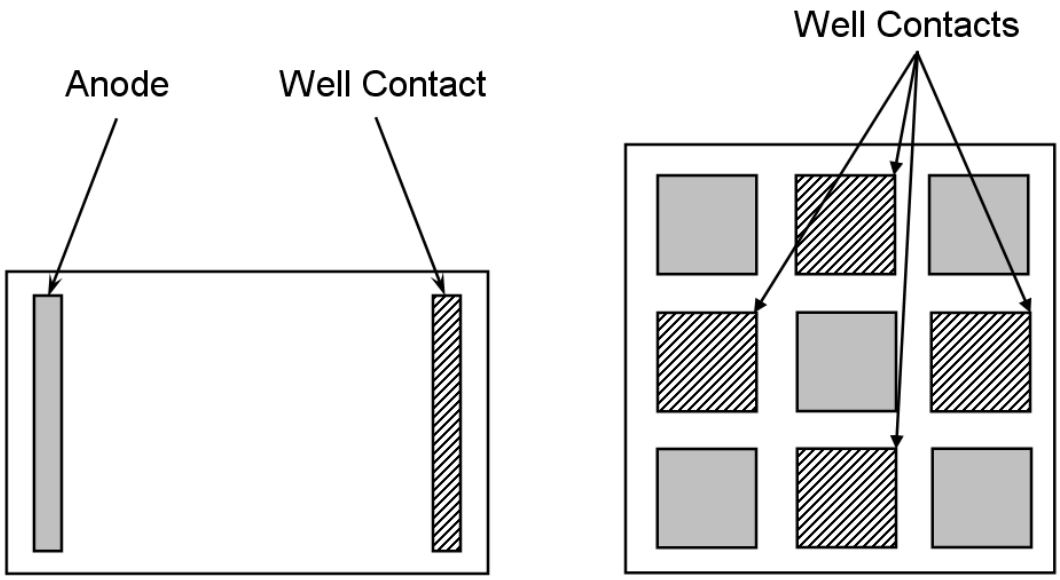


Figure 3.19. (a) Sparsely-placed well contacts and (b) Densely placed well contacts. Modeled after [76].

Figure 3.19 shows two examples of a well structure with different anode and contact spacing. The layout in figure 3.19a would show greater sensitivity for the area near the anode and would decrease in sensitivity as deposited charge from a particle was placed nearer the well contact. The layout in figure 3.19b would exhibit a much more starkly defined sensitive area (if latchup was not eliminated) around the anodes due to the close spacing of the well contacts. The penalty for this kind of mitigation is extra die area.

Layouts where PMOS and NMOS transistor sources are placed further away from N-well/substrate boundaries (and thus further apart from each other) can also prove effective in the reduction of latchup occurrences [54, 75, 82]. This again comes at the cost of layout area, but can be implemented without changing the process.

Other studies have also shown that there is a reduction in latchup threshold and transistor betas (due to increased base length) when using different STI depths [82]. Since it is a drastic process change, it is somewhat unlikely that this technique would be widely used but could be considered if a manufacturer was specifically trying to create a rad-hard process. Increases in STI depths have also been shown to reduce charge collection volumes and aid in the reduction of SEUs.

In some cases, latchup-susceptible devices are flown and SEL events are dealt with by cycling the power and restarting the system. This is usually done in situations where 1) full system uptime is not a critical requirement, 2) SEL events are expected (from ground testing and prediction) to not occur frequently enough to endanger the mission, and 3) testing and lifetime modeling have shown SEL in the susceptible system components to be non-destructive.

Related Phenomena

There are two high-current effects that can be initiated by heavy ions that are related but distinct from SEL, snapback and second breakdown. Neither of these requires the four-region structure that latchup does, but they can be difficult to differentiate from latchup. Johnston [54] describes the two effects as follows:

"1) *Snapback:* Snapback can occur in N-channel MOSFET structures. It is caused by parasitic action of the bipolar transistor formed by the source, well (or substrate), and drain within an individual MOSFET, which affects the avalanche breakdown characteristics [138, 139]. Snapback occurs when minority carrier injection from the source junction, due to avalanche current from the drain junction, reduces the avalanche breakdown voltage. The injected current is amplified by the parasitic bipolar transistor.

The net effect is a negative-resistance region in the drain breakdown voltage characteristics which can result in avalanche breakdown at a much lower voltage, and produce a stable, high-current condition. Unlike latchup, changing the gate voltage can bring a device in snapback out of the high-current mode, so it is often possible to restore normal operation without resetting the power supply.

Snapback in P-well technologies is considerably more complex because of the presence of three different parasitic transistors. Snapback conditions depend on several parameters, including the P-well depth and gate length. P-well devices are more susceptible to snapback than bulk N-well (P-substrate) devices because of the added complexity of additional parasitic structures in P-well technology [140]. Snapback has also been investigated for silicon-on-insulator structures, which can be particularly susceptible to snapback because of floating body effects. This can be a particular problem in partially depleted SOI devices without body ties [34, 141, 142].

Snapback has been observed in heavy-ion tests of several types of devices [143]. Unlike latchup, the minimum LET required to induce snapback is only weakly dependent on temperature as the snapback voltage is dependent on carrier concentrations which do not vary significantly with temperature changes. Additionally, snapback can be alleviated by toggling the gate voltage. These two differences can be used to distinguish between latchup and snapback mechanisms in CMOS devices. Optical techniques can also be used as diagnostic tools to monitor infrared light that is emitted during snapback. Snapback is confined to a single transistor, and equilibrium currents that occur after snapback are generally much smaller than equilibrium currents after latchup because the current flow is confined to a much smaller region, with a higher internal resistance path. It is highly

likely that ‘microlatches’ observed during tests of complex integrated circuits, which affect only limited regions of a circuit and produce equilibrium current changes a few milliamps, are caused by snapback rather than latchup.

2) *Second Breakdown:* Second breakdown can occur in bipolar structures. It is caused by localized heating in a filamentary structure (mesoplasma) in a reverse-biased junction. The lateral dimensions of the mesoplasma are on the order of one micrometer. The mesoplasma occurs because of the in-homogeneities in the silicon, and causes a very localized current to flow within the narrow mesoplasma region. Once the mesoplasma is formed, there is an abrupt drop in the breakdown voltage, creating a high current condition under bias voltage conditions that are well below the rated breakdown voltage. This also results in a negative resistance region that is qualitatively very similar to the negative resistance that is present during latchup.

Even though second breakdown is usually associated with power transistors or high-voltage structures, it can occur in integrated circuits. Recent tests by Koga *et al*., showed that a high-current condition with characteristics similar to second breakdown could be initiated by heavy ions in a high-speed bipolar analog circuit with a 5-V power supply [144]. Although this phenomenon first appeared to be caused by latchup, the threshold LET was unaffected by temperature, suggesting some other mechanism was involved. The current densities they observed were consistent with theoretical predictions of currents from second breakdown.”

CHAPTER IV

CALIBRATION OF TCAD MODELS

From the outset of this work, it is important to insure that the TCAD models used in this work have good quantitative agreement with devices created within the same process technology. For this 65 nm Texas Instruments technology, both layouts and the output of process simulation were provided. Before TCAD devices could be created, doping profiles from the process simulation of a 2D JEDEC latchup structure were extracted as follows. 1D cuts were taken of the doping in six different locations: 1) The N-Well Contact, 2) The middle of the N-Well, 3) The Anode, or P-Source, 4) The Cathode, or N-Source, 5) The middle of the P-Well, and 6) Substrate Contact. These cuts are shown in figure 4.1a. For each of these cuts, profiles for Phosphorus, Arsenic, Boron, and Antimony were extracted. Comparing the profiles side-by-side allowed for the de-coupling of wafer background doping, N-ell doping, and P-Well doping from the profiles for the Source/Drain depositions and the Well and Substrate contact depositions.

Once these profiles were extracted, they were used to create TCAD devices that were as close as possible to the original process simulation output that was provided. An example of one of these devices is shown in figure 4.1b. Once created, lateral and vertical doping concentrations cuts were used to verify the TCAD device's similarity to the process output. These extracted doping profiles provide the foundation for the all of the TCAD work in this 65 nm technology.

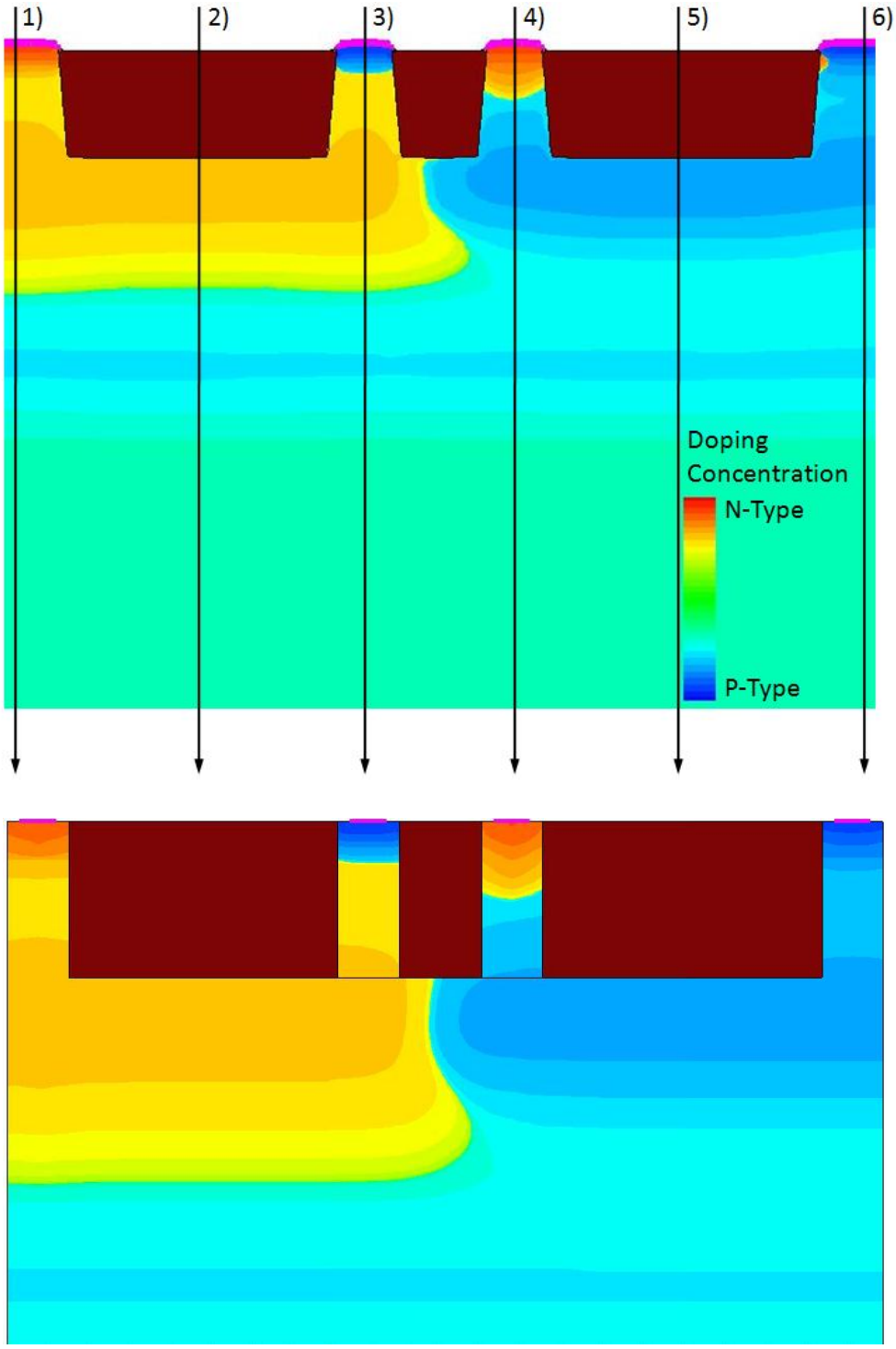


Figure. 4.1. (a) Original process output for SCR device showing doping cut lines used for profile extraction 1) The N-Well Contact, 2) The middle of the N-Well, 3) The Anode, or P-Source, 4) The Cathode, or N-Source, 5) The middle of the P-Well, and 6) Substrate Contact. (b) A TCAD device created using the doping profiles extracted from (a). The same X-Y scales and doping scales are used in both figures for comparison.

After doping profiles were extracted and separated from each other, parameters for simulating the 65 nm TCAD devices were determined by comparison to experimental data from the 65 nm latchup devices collected by Boselli [129]. The layout, a 3D representation, and a cross-section of the TCAD device used for calibration (the same device as used in Chapter V) are shown in figure 4.2. To cut simulation time, half of the device in the layout of figure 4.2a is simulated. The simulated 3D device and a cross-section along the cut-line in figure 4.2a are shown in figures 4.2b and 4.2c.

Because of the time involved for calibration of a 3D TCAD device, the device was only calibrated to beta values at room temperature (Table 4.1) and to closely match the crossover temperature for latchup vulnerability (where $V_{HOLD} = V_{DD}$). Beta values are taken experimentally by comparing N-well and P-well currents at $V_{P\text{-}source}$ (or V_{Anode}) = V_{DD} + 0.7 V for positive injection and $V_{N\text{-}source}$ (or $V_{Cathode}$) = -0.7 V for negative injection.

Table 4.1. Comparison of Beta values at room temperature for the simulated TCAD device and results from [129].

Room Temperature Beta Comparison	**Positive Injection (PNP) Values at V_{ANODE} = 1.9 V**	**Negative Injection (PNP) Values at $V_{CATHODE}$ = 0.7**
TCAD N-well Current (A)	1.210E-06	1.360E-06
TCAD P-well Current (A)	5.700E-07	3.440E-07
TCAD Beta	0.47	3.95
Measured [129]	0.5	5

Parameters for Auger recombination and Shockley-Reed-Hall recombination were adjusted to get close to experimental transistor gains and the crossover temperature for positive holding voltage.

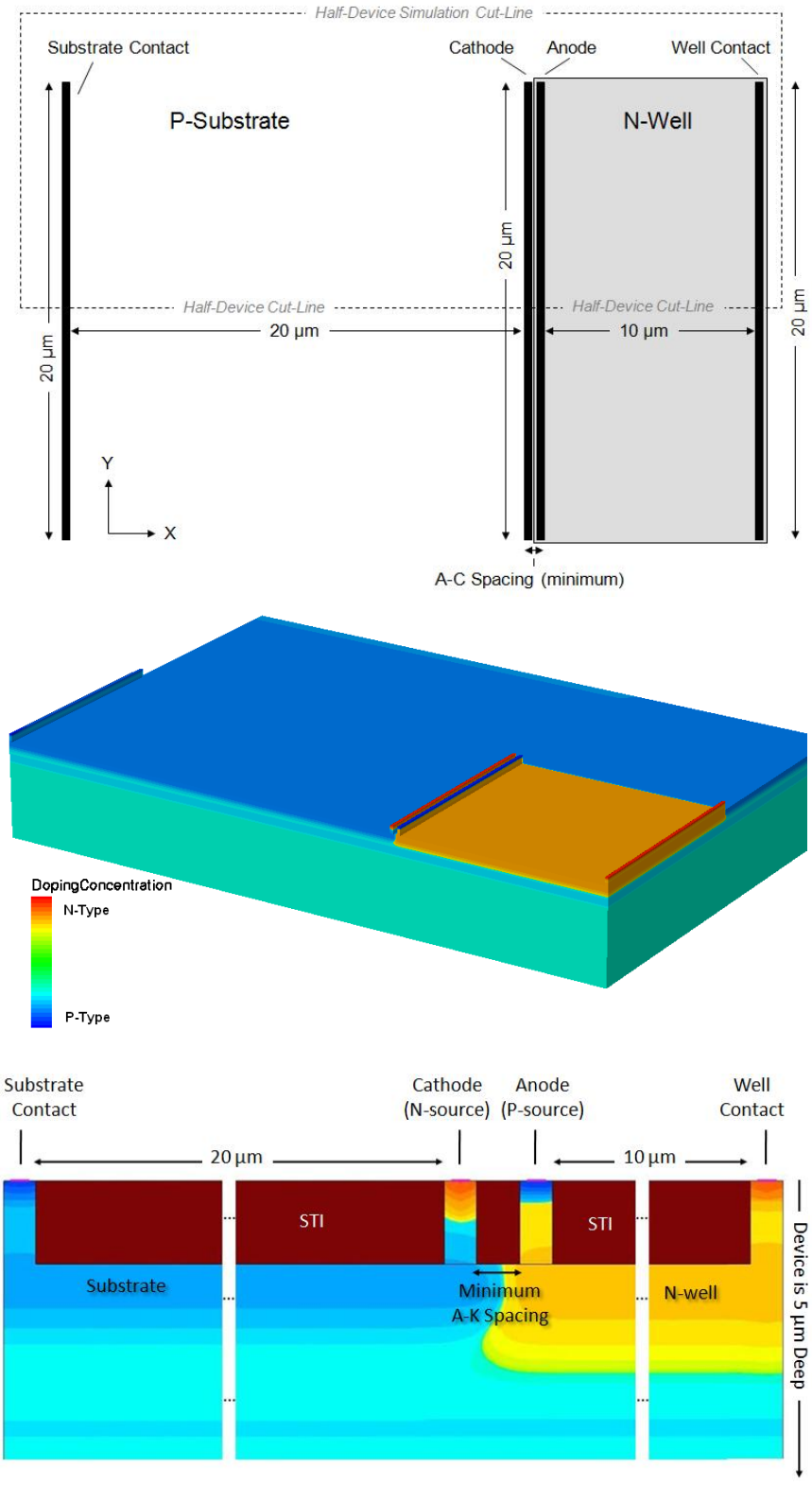


Figure. 4.2. (a) Layout for SCR device showing spacings and half-device cut line (b) 3D TCAD device created from 4.1a using extracted doping profiles (c) Cross-section along half-device cut line. Lateral breaks are included to show well and substrate contacts.

The calibration focus on positive injection is due to positive injection being the more sensitive of the two latchup triggering mechanisms. For positive injection, $V_{HOLD} - V_{DD}$ for TCAD simulation is compared to the experimental linear prediction of $V_{HOLD} - V_{DD}$ from Boselli [129] (See figures 3.14 and 3.17) and shown in figure 4.3.

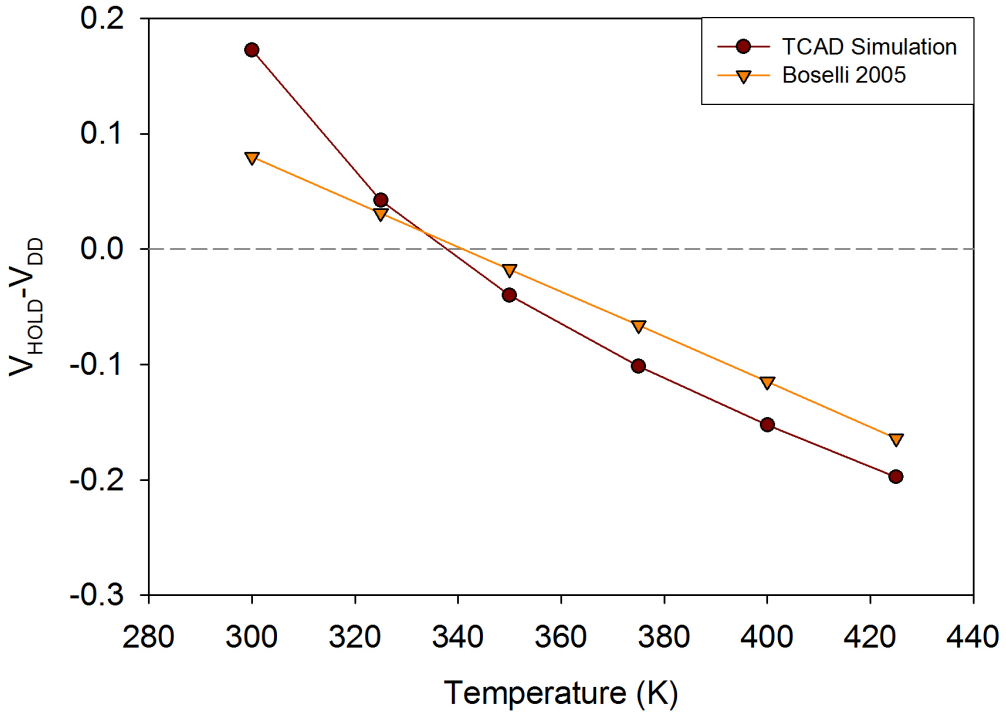


Figure. 4.3. (a) $V_{HOLD} - V_{DD}$ comparison between TCAD 65 nm SCR model and experimental data from [129]. $V_{HOLD} - V_{DD}$ for both TCAD and experimental work are plotted as a function of temperature.

The matching of holding voltages allows for a good approximation of the device sensitivity (±30 mV for T > 320 K) across the desired simulation temperature range. The TCAD parameters used to obtain the fit are used in all the TCAD simulations described in Chapter V.

CHAPTER V

TCAD MODELING AND ANALYSIS OF 65 NM SCR DEVICES

Single event latchup (SEL) has been a significant reliability concern for CMOS devices in radiation environments for the last twenty to thirty years [54, 58, 66, 68, 71, 76, 80, 81, 145]. As devices have scaled to smaller dimensions, with a concomitant decrease in the amount of deposited charge necessary to perturb electric fields into a possible latching condition, there is the concern that circuits may become more susceptible to SEL [8, 16, 81, 85, 87]. In contrast to this trend toward increasing vulnerability, the scaling trend of electrical characteristics relevant to latchup for new technology nodes works in the system designer's favor [129]. With the reduction in the gain product of the two parasitic transistors involved in the latchup process and with the supply voltage scaling below the electrical holding voltage, latchup may be of less concern in future technologies. As previously noted, for reliability concerns, a simple test of the electrical holding voltages, gain products, and holding currents at room temperature may not be sufficiently rigorous to allay all concerns about latchup [86, 99, 146]. For a given application, the range of environment temperatures must be considered.

Recent publications have examined the effects of temperature and angle of incidence on proton- and heavy ion-induced latchup in SRAMs [86, 87]. The results showed both the influence of temperature and angle of incidence on latchup cross-section in SRAMs. Latchup cross-section was seen to increase with both increases in temperature and incident angle rotation towards a more grazing angle. These phenomena are covered in detail in Chapter III. In these tests and other typical tests [86, 87, 147], devices are tested at two temperatures and the angle of incidence is rotated along only one axis to

achieve a grazing angle. As will be seen in this chapter, SRAMs are very asymmetric in their layout and grazing angle tests in only one lateral direction are insufficient to characterize device latchup vulnerability fully.

This chapter presents the results of SEL simulations of a 65 nm structure recommended for use in determining latchup sensitivity. The effects of both temperature and heavy ion angle of incidence are examined. Additionally, a second device with a different width is also characterized for SEL vulnerability. Devices were found to have strong SEL threshold dependence on the orientation of grazing angle strikes. A discussion regarding the impact of a high-aspect-ratio sensitive volume on SEL rates follows the simulation results.

Device Structure

The device examined in this chapter is an NPNP structure from a test chip fabricated in a 65 nm CMOS technology. This device was created using the IEEE standard for latchup characterization [148]. Devices of this type use long strip-contacts across a wide device that allow for easy high-current DC measurements and minimize edge effects that may dominate smaller devices. This is an interesting device because the fundamental mechanisms for latchup in a process can be studied without interference from other active devices. The understanding from the standard test device can then be applied to more highly integrated devices, as will be seen in Chapter VI. The anode (P-source) to cathode (N-source) spacing in devices of this type is the minimum design rule spacing allowed by the process. A cross section of the active part of the device is shown in figure 5.1. The layout is shown in figure 5.2a with the 3D TCAD device shown in figure 5.2b.

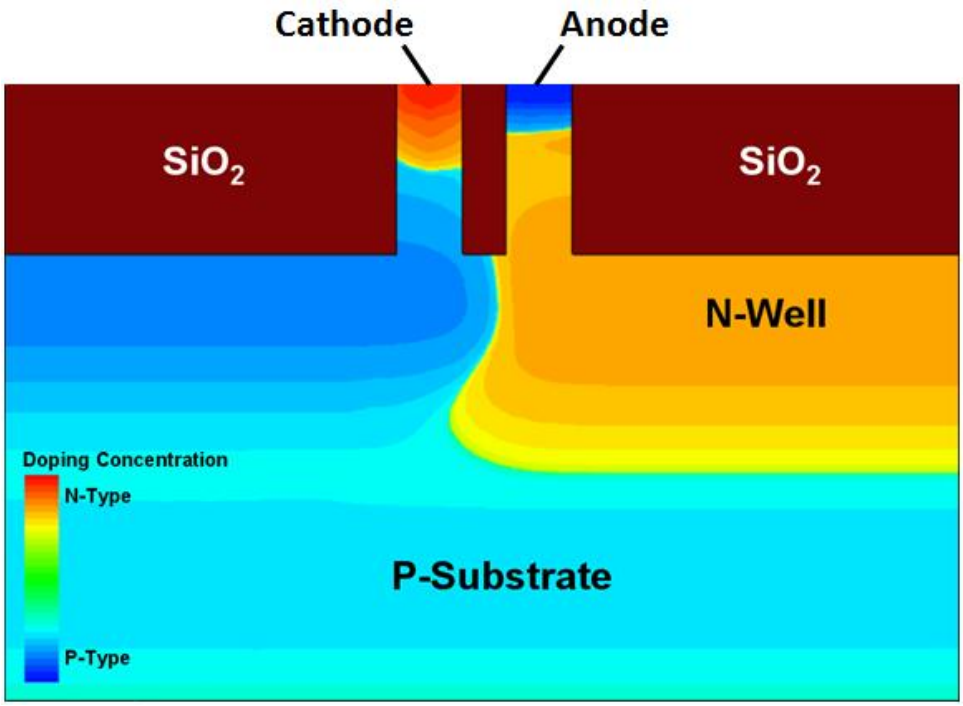


Figure 5.1. Zoomed-in cross-section of active parts of the SCR structure from figure 5.2b. The cross-section is taken in the Z direction on the half-device cut line to show the anode, cathode, and well/substrate junction.

The device was simulated and calibrated using measured electrical characteristics and doping profiles from vendor process simulations (see Chapter IV). The well contact is 10 µm from the anode and the substrate contact is 20 µm from the cathode. The anode and cathode represent the P-source and N-source in a CMOS structure, respectively. The N-well and the contacts for the N-well, P-anode, N-cathode, and P-substrate are 20 µm wide. Figure 5.2b shows the corresponding 3D TCAD device. To reduce computational time and memory constraints, the device is cut in half in TCAD to take advantage of the symmetry of the structure. For all the biasing and temperature conditions in these simulations, the product of the two bipolar transistors' current gains is above unity. With that (approximate) requirement for latchup satisfied, holding voltage and holding current are examined.

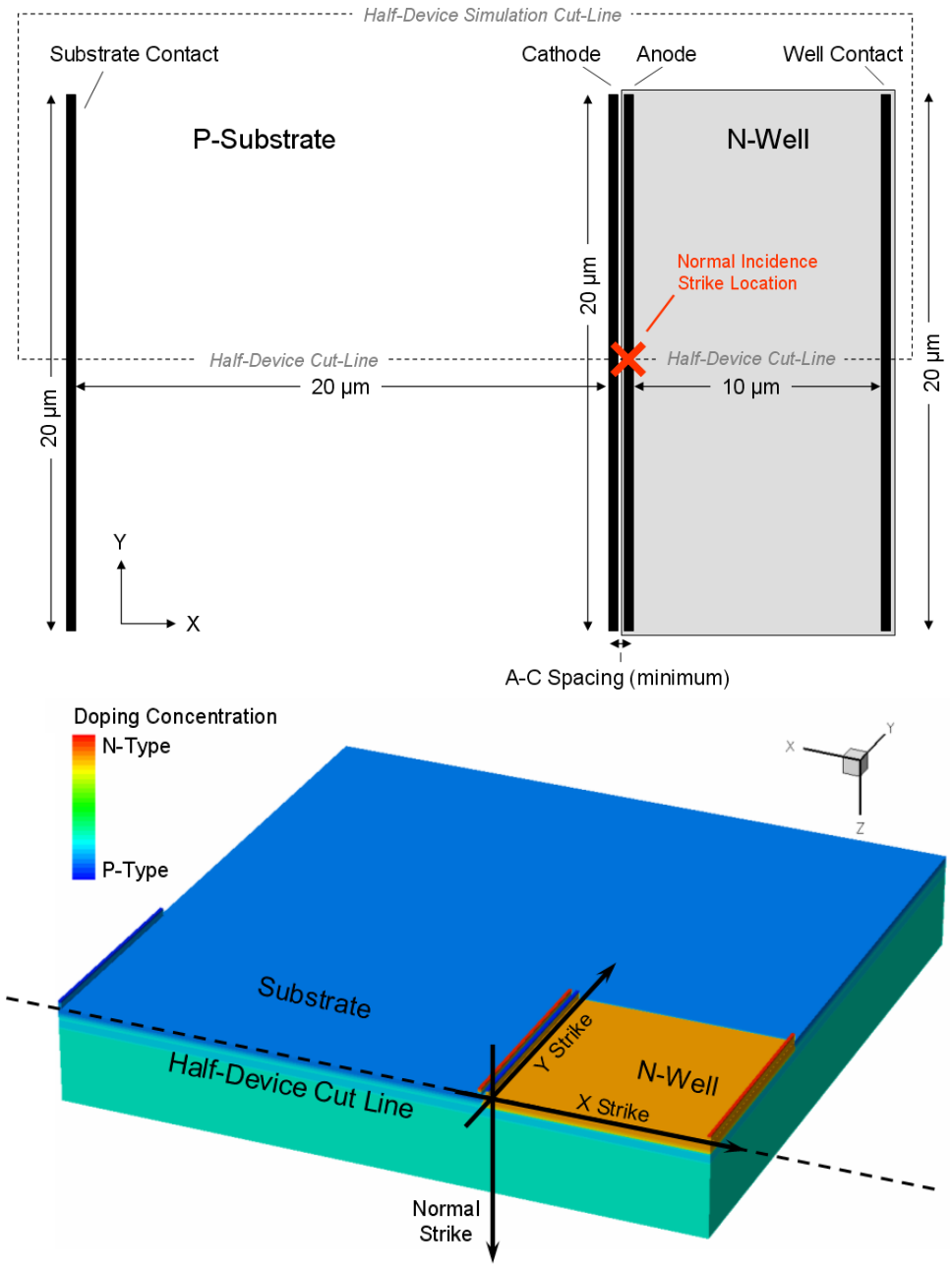


Figure. 5.2. (a) Layout of physical 20 µm wide SCR structure in 65nm technology with a 10 µm long N-well and 20 µm cathode-P-tap spacing. The cut-line for the TCAD device simulation in shown. (b) TCAD structure for simulations. Only half of the full device is simulated to save on memory and computation time. The cut line from figure 5.2(a) is noted in the figure. Strike orientations for SEL TCAD simulations are indicated.

TCAD Simulation: Results and Discussion

Boselli et al. have shown that for the 65 nm technology examined here, holding voltage exceeds the nominal operating voltage at room temperature [129]. However, modern commercial processors can operate within specifications up to almost 400 K and military specifications require devices to be tested up to 425 K. Figure 5.3 presents simulation results that show how the positive injection curves change with increasing temperature.

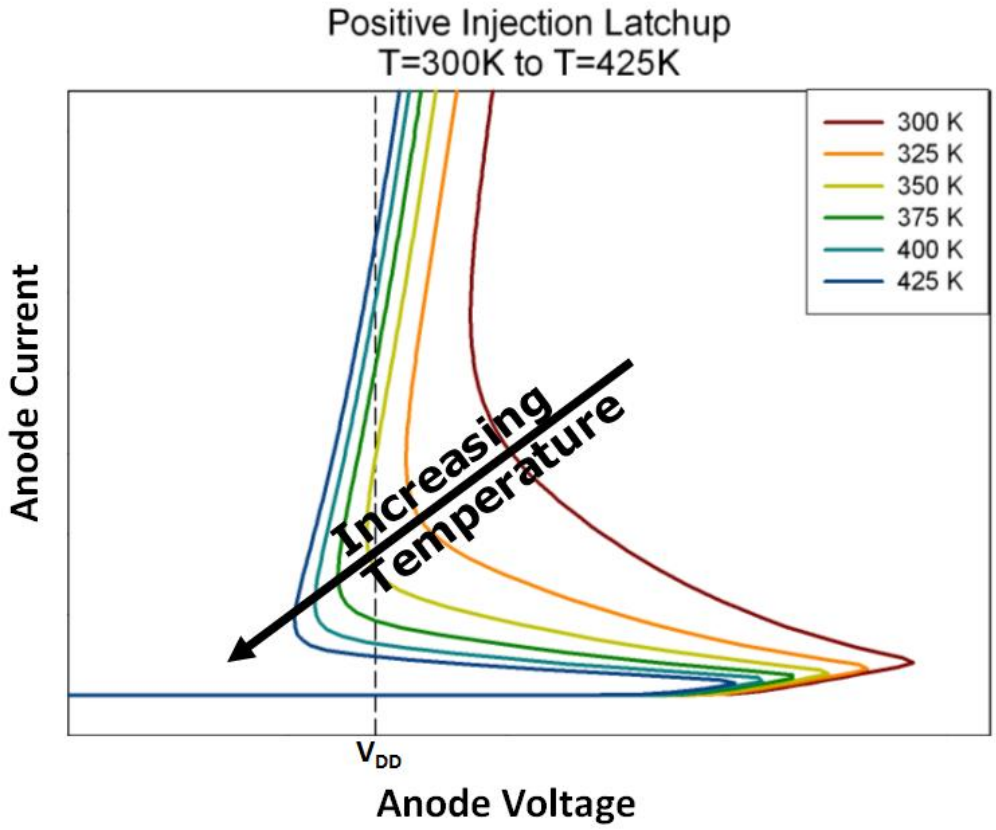


Figure 5.3. Positive injection DC latchup curves showing a decrease in holding voltage with increasing temperature. V_{DD} is marked on the plot. Data is from simulation of the TI ESD TCAD device.

The extracted holding voltages and currents from simulation curves like those in 5.3 are plotted in figures 4.3 and 5.4. Figure 4.3 shows the difference between holding

voltage and operating voltage for positive injection and figure 5.4 shows the holding currents for positive and negative injection vs. device temperature for the simulated structure operated at the nominal core voltage of 1.2 V. Figure 5.4 shows that the holding current, that is, the current at the anode for positive injection needed to sustain latchup, decreases with increasing temperature.

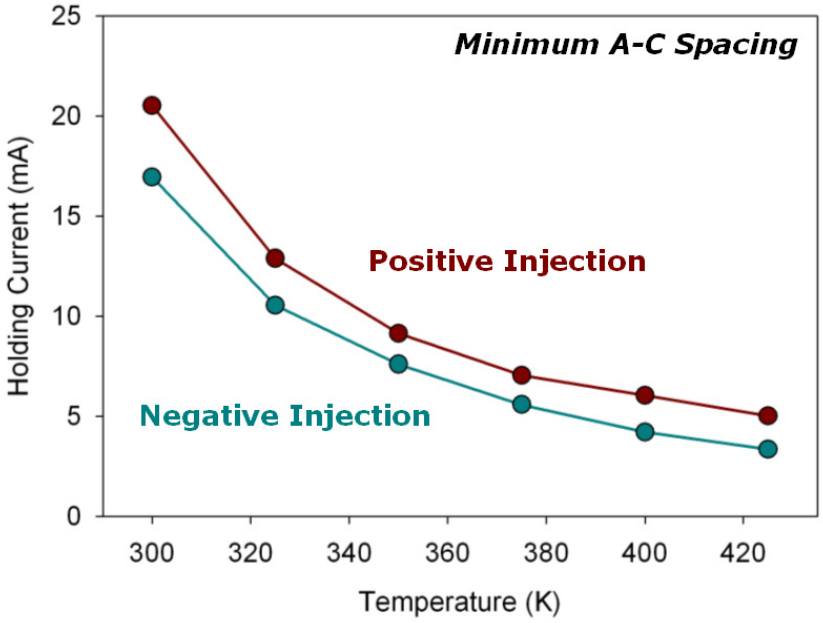


Figure 5.4. Holding current vs. temperature for 65 nm NPNP device with minimum anode-cathode spacing: Holding current can be seen to decrease with increasing temperature.

It is important to understand how these electrical characteristics relate to the single event latchup vulnerability. Response from localized interactions at the junction inside the structure due to collected charge are potentially quite different from the electrical response created from voltages and currents at the terminals of the structure. As discussed in Chapter III, with single events, the charge can be deposited directly into a device, forgoing injection at electrical contacts.

To examine SEL, initial ion-strike simulations were carried out using a constant charge deposition of 0.80 pC/μm, normally incident to the surface at the edge of the simulated region (corresponding to the middle of the physical device) and directly through the anode contact. This location was chosen as it has been shown that the portion of the N-well farthest away from the well contact is the most sensitive region of the structure for initiating latch-up [54, 76].

The ion strikes in the simulator are represented by the linear charge generation in units of pC/μm. For a comparison to typical LET units, 0.01 pC/μm ≈ 1.0 MeV-cm^2/mg for LET in silicon (See charge deposition, Chapter II). All simulated ion track lengths in this chapter are 20 μm long. This length was chosen as it is the longest physical dimension of the device and long strikes with constant charge deposition per unit length are useful for characterizing the change in device sensitivity as charge is placed in different areas within the volume of the N-well.

For simulations with varying temperature, the temperature is uniformly set across the entire device at the desired operating temperature. This is useful for examining trends due to device self-heating, but does not capture a detailed thermal profile of the device that includes increased temperatures at active junctions. Local self-heating at active junctions creates further increases in device susceptibility, so these simulations produce a lower bound for device vulnerability at a chosen die temperature.

The simulation boundary conditions are reflective, which is necessary to preserve the symmetry along the half-device cut line. Because the main interest is charge interaction in the N-well near the anode contact, the reflective conditions near the N-well contact and the edges of the P-substrate (10 μm away from the N-well) do not result in a

tangible change in latchup sensitivity. These single-event simulations were performed at the nominal voltage for the technology (1.2 V) over a range of temperatures. The results are presented in figure 5.5, which displays the supply current vs. time following the ion strike.

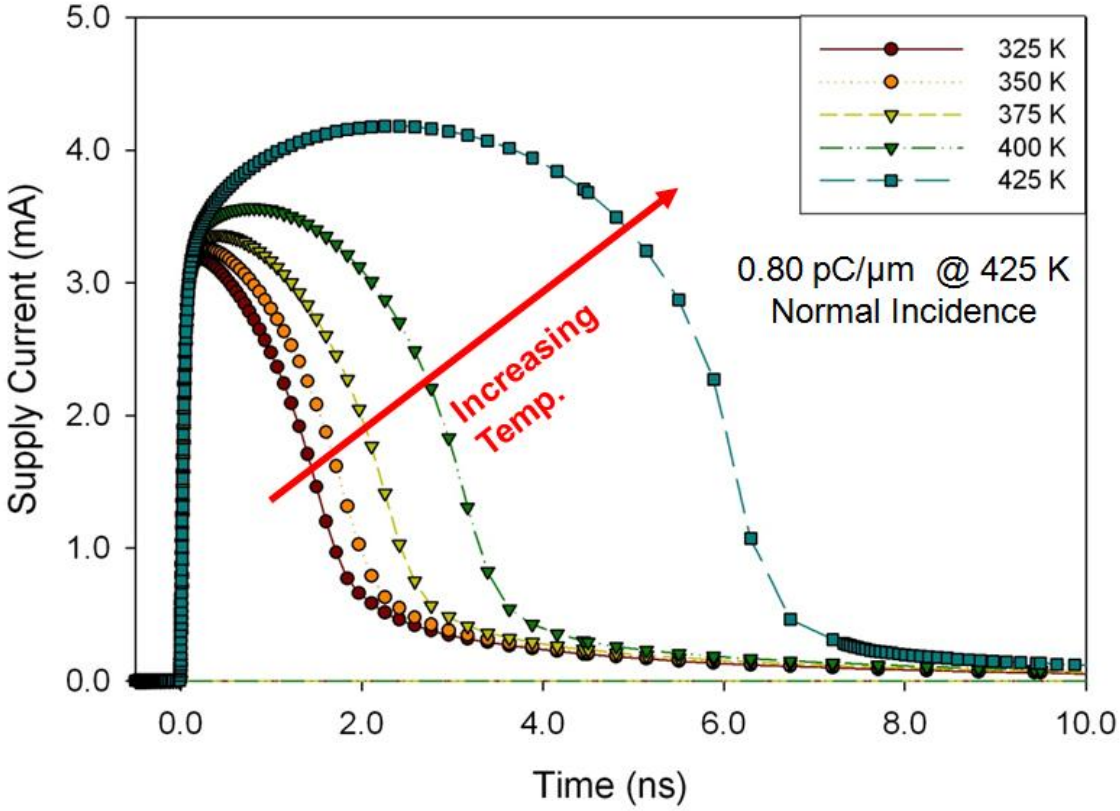


Figure 5.5. Single event response current vs. time for varying temperatures at nominal operating voltage (1.2 V). The current at the tied anode/N-well V_{DD} rail is plotted

Figure 5.5 shows that the structure does not latch up even for 0.80 pC/µm normally incident strikes, since the current always returns to its prestrike value. At first glance, this could be assumed to be because the device currents are below the holding currents for their respective operating conditions. The very long pulse seen in the 425 K test at nominal (1.2 V) operating voltage is an example of the structure almost reaching the potentials required to enter a latching state. However, examination of the potentials

for that event shows that about two-thirds of the width of the structure (closest to the strike) reaches a potential sufficient to cause latchup.

Figure 5.6 shows the potential in the N-well referenced from the N-well contact 2.0 ns after the 0.80 pC/µm particle strike. It can be seen that even for this very high charge density strike, the structure does not reach the potential necessary for latchup along the entire junction and can recover. The feedback in the regions of the structure where the device has the proper potentials for latchup contribute to the long pulse seen in figure 5.5. Normally incident strikes at 0.90 pC/µm are sufficient to latch the structure.

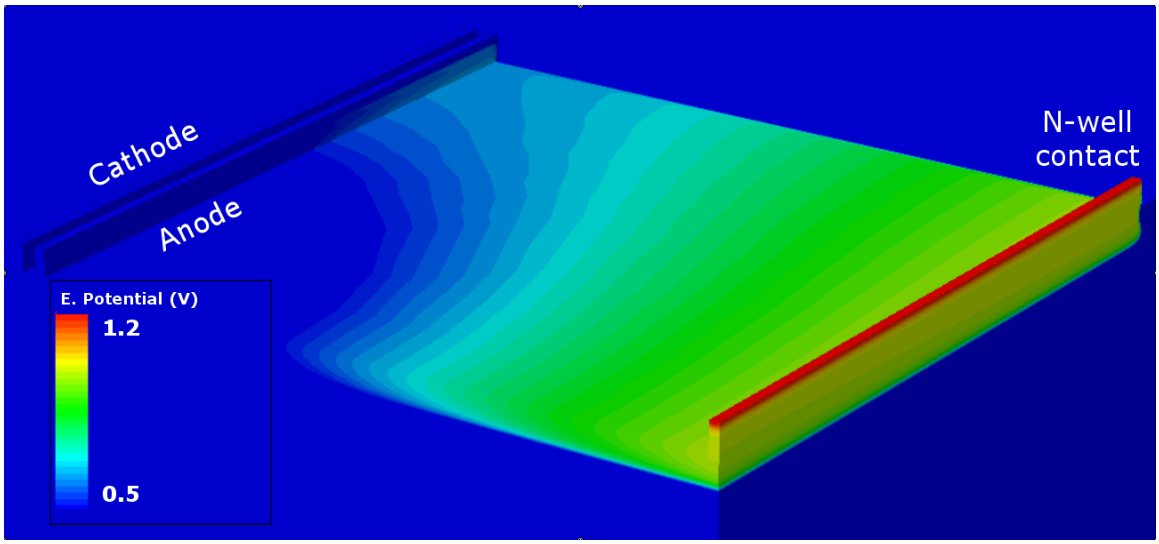


Figure 5.6. Potential plot for 425K temperature pulse seen in figure 5.5 at t = 2.0 ns. In dark red is the potential of the N-well contact. Dark blue is a 0.7 V potential difference (diode drop) from that contact. About 6 µm (out of 10 µm) of the width of the device have the proper biasing for latchup.

To further investigate the vulnerability of the structure, an extreme grazing angle simulation was performed. For these tests, an ion strike parallel to the surface (90° from normal) was placed either in the X or Y direction (identified in figure 5.2a and 5.2b)

directly below the STI layer. These simulations were performed at 425K and nominal (1.2 V) voltage.

Figure 5.7 presents the results for strikes in the X direction along the length of the N-well. For this orientation, lower LET particles than the normally incident ions discussed above are sufficient to latch the device. The latchup threshold is between 0.25 and 0.275 pC/µm. The 0.25 pC/µm strike does not latch the device, as the holding current seen in figure 5.4 is not achieved. This result is reasonable since the N-well tends to be the most sensitive region with regards to latchup and the majority of the charge deposition from the strike goes directly into the N-well.

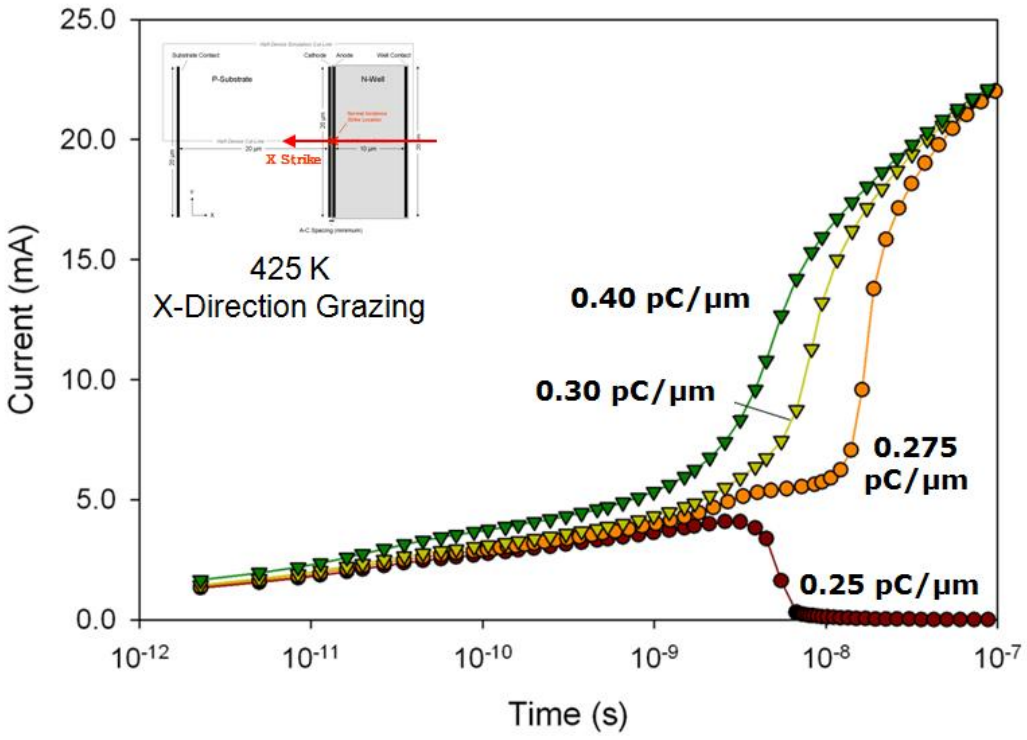


Figure 5.7. Single event response current vs. time for varying temperatures at nominal operating voltage (1.2 V) and 425K for varying charge density strikes at 90° grazing angle perpendicular to the anode (X direction in figure 1b). The current at the tied anode/N-well contacts is plotted.

Second, a strike was simulated in the Y direction parallel to the orientation of the anode. Figure 5.8 displays this result. It can be seen that the structure is substantially more sensitive to latchup in this direction, with the latchup threshold between 0.03 and 0.04 pC/µm. The majority of the charge is deposited directly under the anode at the furthest distance possible from the N-well contact while still remaining in the N-well.

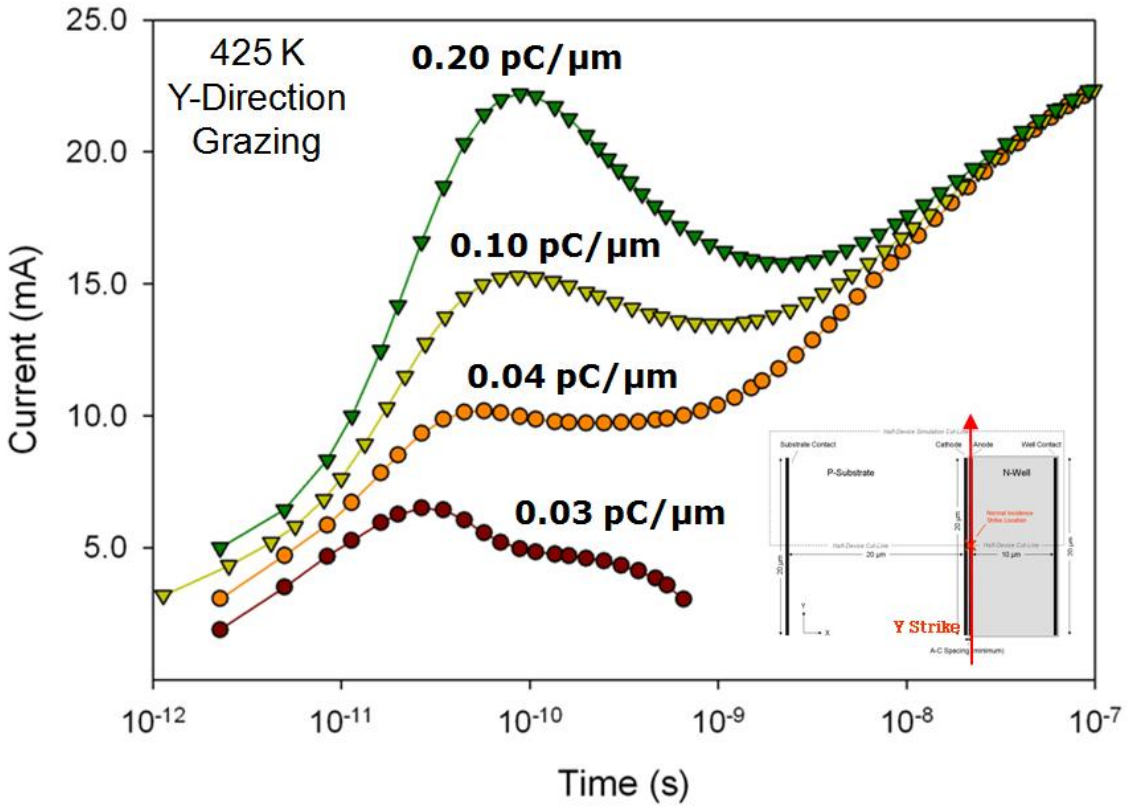


Figure 5.8. Single event response current vs. time for varying temperatures at nominal operating voltage (1.2 V) and 425K for varying charge density strikes at 90° grazing angle parallel to the anode (Y direction in figure 1b). The current at the tied anode/N-well contacts is plotted.

This marked increase in sensitivity can be explained in two ways that are interrelated. First, with a long (narrow and shallow) sensitive volume underneath the length of the anode with the distance from the STI to the N-well/Substrate boundary as

the vertical dimension, even a low charge density strike of 0.04 pC/μm at a grazing angle deposits more energy over the 10 μm width than a normally incident strike with a charge density of 0.80 pC/μm. This is also true for the grazing angle strike in the X direction. If the sensitive volume is near the anode, most of the charge is deposited in the N-well outside of the sensitive volume. The second explanation is that latching is a localized phenomenon. While a 0.80 pC/μm strike can deposit a significant amount of charge even in a shallow N-well, it only reaches the potential required to latch the PNPN structure within several micrometers of the strike. The Y-direction strike requires the minimum amount of deposited charge to provide the potential drop needed to forward bias the vertical PNP bipolar transistor and initiate latchup. The result is that the device is 6-7× more sensitive to strikes that are oriented along the N-well/P-substrate junction near the anode contact than to strikes with the same LET that are incident in the X-direction along the length of the N-well. Not only does it matter how much energy is deposited in a sensitive volume, the spatial distribution of that energy is critical in determining whether latchup occurs.

Although the test structure considered here has a more extreme aspect ratio than those considered in other studies, the results in figure 5.8 are consistent with studies showing large increases in latchup cross section with temperature and angle [66, 86, 91]. For proton radiation, nuclear reactions with device materials (particularly higher Z metals and vias) may be the dominant mechanism for SEL [66, 76, 86, 87, 92, 149]. Reed et al. examined the relationship between proton energies and the directionality and range of spallation products from nuclear reactions [120]. In [86], significant increases in cross section at grazing angle are seen at proton energies where the reaction products are

forward directed. The results described above demonstrate that reaction products with low LETs do not latch the SRAMs unless they are oriented along the N-well/Substrate boundaries near the P-source contacts. Therefore, for predictive TCAD simulations it is crucial to understand and correctly model the physical processes and statistical distribution of proton fragmentation products at varying energies.

Due to the large aspect ratio of the sensitive volume in these structures, the change in SEL threshold is more pronounced with angle than the results in [86], but the trend is the same. This leads to the conclusion that the magnitude of the change in SEL threshold with angle is related to the width of the devices. This conclusion can be substantiated by performing tests on a narrower device. Another simulation structure was created with N-well width and contacts 5 μm wide instead of the previous 20 μm. Again, only half of the device was simulated and tests were performed at 425 K and 1.2 V to maintain a consistent simulation methodology. Figure 5.9 plots the change in the charge density of strikes needed to induce SEL between normal incidence to the surface and grazing strikes for both device widths.

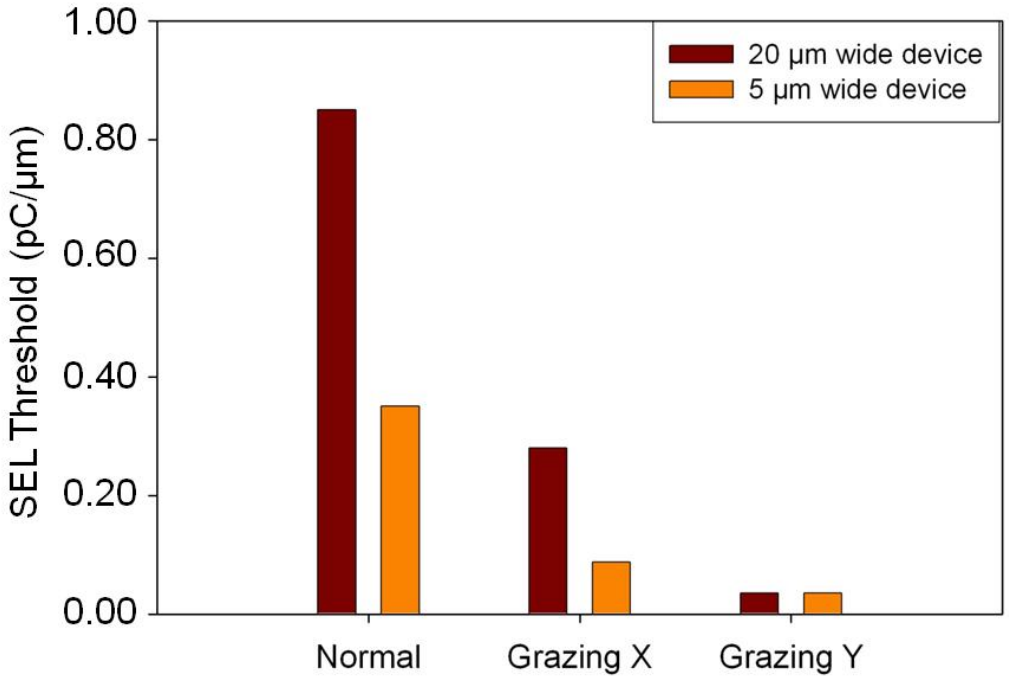


Figure 5.9. Plot of threshold LETs for TCAD devices of different width. Both devices show a difference in sensitivity between grazing angle strikes in different directions as well as a greater sensitivity between normal incident and grazing angle strikes. In both cases, strikes oriented along the N-well/P-substrate junction near the anode require minimum charge deposition for latchup.

Both devices are much more sensitive to the X-direction grazing angle strike that occurs parallel to the N-well/Substrate boundary underneath the anode than to a grazing angle strike perpendicular to the anode contact. While the numerical difference in threshold between grazing angle strikes in the X- and Y-directions is reduced for the smaller device, there is still more than a factor of 2 difference between the threshold charge density of the strikes. This suggests that an extra axis of rotation is needed in SEL tests to characterize the effects of angle properly. Simply tilting the device under test to grazing angle will usually orient ions and forward directed secondary particles either parallel or normal to the longest component of the individual sensitive volumes in an SRAM. Given a typical layout for an SRAM, there is a clear sensitive orientation if the most sensitive areas of the device lie along the N-well/P-substrate boundaries. This is

exhibited by the simple layout of multiple SRAM cells in figure 5.10. From this it would be expected that when a beam is oriented at a grazing angle to the test device, rotating the test fixture laterally by 90° will change the threshold and cross section.

For most deep submicron technologies, such a test will also need to be performed with the die above room temperature in order to see latchup. It is important to note that even when latchup is observed at room temperature, elevated temperatures within the operating range of the device must still be tested. Many structures operate using a dual voltage scheme: a higher voltage for I/O circuitry and a lower core voltage. Due to the higher voltage, I/O circuitry is typically more sensitive to SEL. It is likely that the I/O circuitry of modern highly-scaled devices may be the only SEL-sensitive area (if any) of a device at room temperature. Thus, a significant increase in the SEL cross-section of a part could be observed at a temperature where the areas of the device with lower operating voltages become vulnerable.

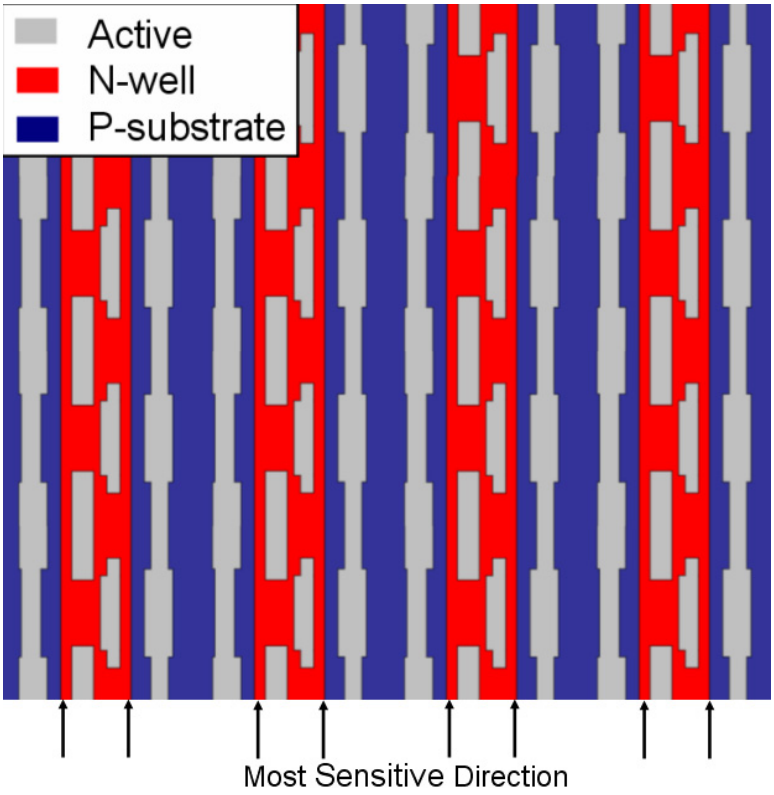


Figure 5.10. Example of a typical CMOS SRAM layout. Active, P-substrate, and N-well regions are marked. The N-wells arranged in long columns present a likely most sensitive lateral directionality for SEL.

SEL Rate Issues

The device used in this chapter has a sensitive volume with an extraordinarily high aspect ratio (the N-well) in both lateral dimensions. The top view can be seen in figure 5.1a with the dimensions of the N-well being 10 μm × 20 μm. The depth of the most sensitive region (from the STI to the bottom of the N-well) is on the order of 0.5 μm. In order to cause latchup with anything but the highest LET particles, the energy deposition from all but the highest LET particles must be distributed primarily in the lateral direction. Ions in an isotropic space environment have a considerable probability of intersecting devices at severe grazing angles. As discussed in Chapter III and shown in figure 3.8, approximately 50% of ions in an isotropic environment intersect a device at

60° or greater from normal incidence. The ions with these trajectories are the most likely to trigger a SEL. When considering the effects of ions passing through such a long, wide, and shallow sensitive volume, basic assumptions for ions depositing charge along their trajectory will likely be invalid.

A large portion of the cosmic ray spectrum contains ions whose path lengths in Si are shorter than the lateral dimensions of the sensitive volume. The complications involved in the energy distributions from ions that actually stop in the sensitive volume must be considered and a Monte Carlo tool is necessary for these calculations. Nuclear reactions caused by ion and proton interactions with device materials also demonstrate the need for such a tool. Dodd et al. show that ion-ion nuclear reactions with high Z materials in devices strongly affect the SEL rate [147]. As discussed in Chapter III, the energy of protons plays a role in the directionality and path length of spallation products from reactions with high Z materials in devices. To predict a SEL rate accurately, both these effects require correct physical modeling and realistic statistical distribution in a Monte Carlo simulation.

Summary

The effects of temperature and angle in determining the vulnerability of PNPN structures to SEL are demonstrated in this chapter. A significant change in threshold LET is observed as the lateral angle of incidence is varied for simulated heavy ion strikes. It is suggested that two axes of rotation should be used in latchup testing as particles not moving parallel to the edges of the N-well near P-sources have a reduced probability of instigating latchup.

CHAPTER VI

ANALYSIS OF SINGLE-EVENT LATCHUP IN 65 NM SRAMS

Introduction

Single event latchup (SEL) has been observed on a range of different devices over the past three decades [54, 58, 66, 68, 71, 76, 80, 81, 145]. With devices scaling to smaller dimensions, there are competing factors influencing device SEL susceptibility. These factors have been discussed in the previous chapters.

TCAD tools are useful in understanding electrical and single event latchup phenomena as they relate to the 65-nm technology used here. In particular, the regular repeating layout of an SRAM provides a valuable opportunity to examine the effects of temperature, LET, and charge interaction on SEL in a highly integrated device. Additionally, TCAD simulations of ESD test devices [110] shown in Chapter V indicate a strong directionality based on the lateral orientation of the beam (the azimuthal angle instead of the more prominently used zenith, or polar angle). Those simulations show that for a P-source and N-source pair, or an anode and cathode for a parasitic silicon-controlled rectifier (SCR) device, charge placed along the substrate/N-well boundary is the most efficient method of inducing SEL.

For the ESD test devices, simulated ion strikes oriented along the substrate/N-well interface had a critical LET 7-9 times lower than strikes rotated 90° laterally at the same angle of incidence from normal. The results of those simulations motivate the experimental work shown in this chapter.

Test results show that the 65 nm SRAMs are sensitive to SEL from heavy ions and validate the hypothesis set forth in the previous chapter [110] that SEL should have a

strong directionality with changes in azimuthal angle of the beam orientation. This chapter presents the first experimental observations of single-event latchup in 65-nm CMOS SRAMs.

As a result of the issues with effective LET discussed in chapter III, effective LET, effective fluence, and effective cross-section are not used for analysis and all LET, fluence and cross-section values given in this work are unmodified.

Device Structures

The SRAM device used for these experiments consists of eight separate 1-Mbit memory banks: 4 high density banks, 2 high performance banks, and 2 normal banks. The normal banks are also relatively high density, but lower than the four high density banks. The spacing and worst-case resistances (for source/source pairs equidistant from a row of well/substrate contacts) are shown in table 6.1. These parameters are normalized to values from the normal banks. To allow accurate SEL characterization, no I/O buffers were used except for a small amount of decoding circuitry. The SRAM was operated with a nominal 1.2 V V_{DD} and a 1.8 V well bias, both of which were provided by external supplies. The decoding circuitry was operated with 1.2 V V_{DD} and a 1.2 V well bias.

Table 6.1. Comparison of important properties for SEL characterization of SRAM 1-Mbit banks. Parameters are normalized to the normal SRAM banks

Bank Property	High Density	Normal	High Performance
A-K Spacing*	90.8%	100.0%	114.4%
P-well Resistance	97.7%	100.0%	54.5%
N-well Resistance	101.3%	100.0%	82.5%

**ESD Latchup device in figure 6 and [110, 129] are at 130.7% anode-cathode spacing for the 65 nm node.*

Experimental Setup

All tests were performed on the SRAM structures using the 15 MeV/u cocktail at the Cyclotron Institute at Texas A&M University [150]. Values of the particle energies and LETs at the device under test (DUT) used in this work are shown in Table 6.2, taking a 52 mm air gap into account. For the initial heavy-ion SEL tests, the DUT was exposed to 11.3 MeV/u ^{84}Kr ions with a peak LET of 28.9 MeV-cm^2/mg at three different angles (0° (normal), 45°, and 78.5°). For these tests, the die was held at one of two temperatures (50 °C or 84 °C). The second set of tests was designed to find the temperature thresholds at which the DUT becomes sensitive to SEL for the specific combination of ion and strike orientation. In the second set of tests, either normal incidence or grazing angle strikes (78.5° from normal) were used. The grazing angle strikes were directed either perpendicular or parallel to the long direction of the N-well and are referred to as the X-grazing and Y-grazing directions, respectively. These beam orientations with respect to the DUT and SRAM layouts are shown in figure 6.1. It should be noted that the Y-grazing beam orientation runs parallel with the N-well and P-substrate columns. For each ion/temperature combination at normal incidence, the DUT was exposed to a maximum fluence of 1×10^7 particles/cm^2 or until SEL was observed. For each ion/temperature combination at X- and Y-grazing angles, the DUT was exposed to a maximum fluence of 5×10^7 particles/cm^2 or until SEL was observed. This test was repeated at incrementally higher temperatures until latchup was observed. An external power supply was used to monitor for large increases in current that indicated a latching condition.

Table 6.2. List of ions and energies used for SEL testing at the Texas A&M Cyclotron Facility [150]. Energies and LETs are adjusted for the 52 mm air gap between the beam aperture and the DUT.

Ion	Energy at DUT (MeV/u)	LET (MeV-cm^2/mg)
Ne	13.5	2.8
Ar	12.6	8.6
Cu	11.5	20.4
Kr	11.3	28.9

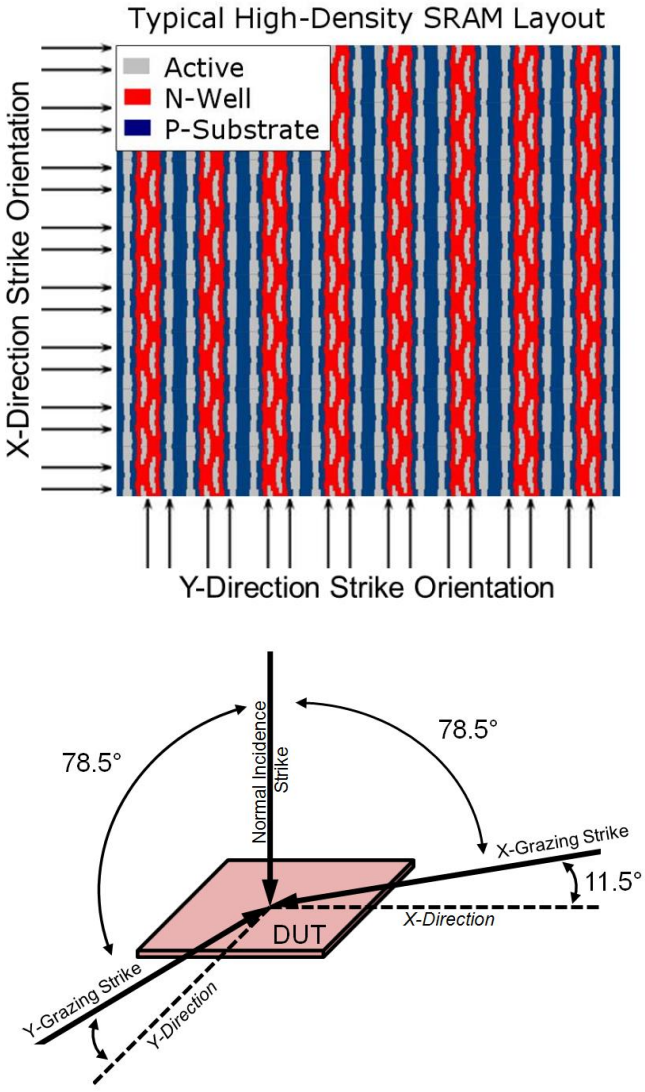


Figure 6.1. (a) Layout of a typical SRAM with notation for strike directions; (b) Graphical representation of the three beam orientations relative to DUT for SEL temperature threshold testing. Y-grazing orientation runs parallel to the N-well long dimension and X-grazing orientation runs perpendicular to the N-well long dimension.

Experimental Results

Cross Section Tests with ^{84}Kr

The SEL cross-section for 28.9 MeV-cm^2/mg krypton ions is plotted vs. angle at two temperatures in figure 6.2. During initial SEU/MBU testing at room temperature, no latchup was observed at room temperature. At normal incidence, latchup was first observed at 50 °C with increasing chip cross section at 45° and 78.5°. For testing at 84 °C, the chip latched very quickly, even at the lowest available flux. For the grazing angles (45°, 78.5°) the total fluence to cause latchup is a minimum estimate because the beam was not automatically shut off when latchup was observed. Since the cross-section and total fluence are reciprocally related, the cross sections for the last two data points on the 84 °C cross-section curve are lower bounds.

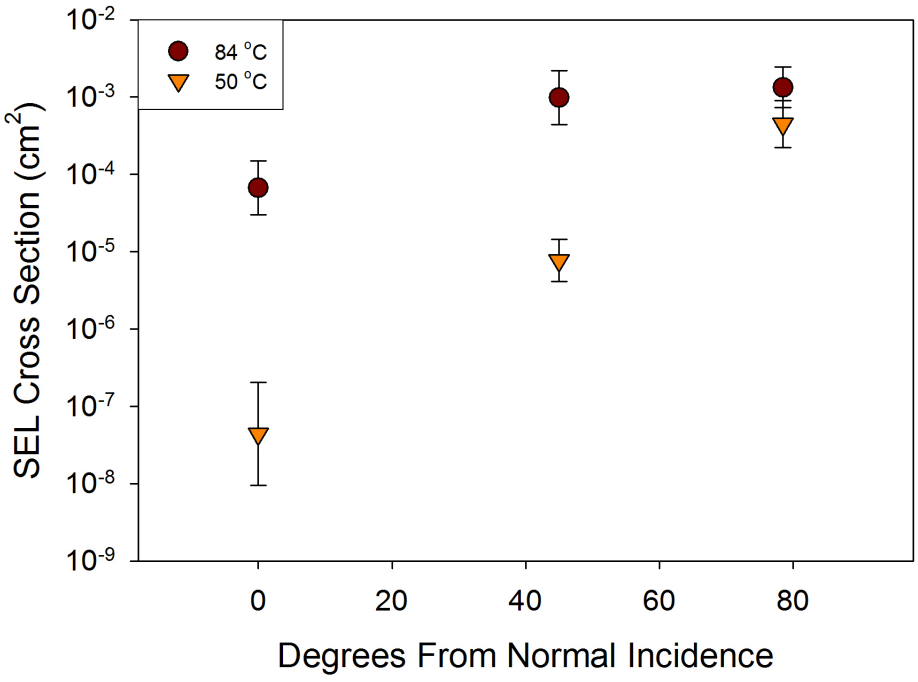


Figure 6.2. SEL cross-section of an array of 65 nm SRAMs. An increase in temperature is seen to increase the SEL cross-section. The devices did not latch at room temperature. Testing was done with X-grazing orientation

Results showing large increases in latchup cross section with increasing temperature and angle of incidence are consistent with work by other authors [66, 86, 91].

Temperature and LET Thresholds

Figure 6.3 shows the measured temperature thresholds for latchup using the four ion species listed in Table 6.2. Note that the plotted values are *not* effective LET, but are the LETs of the ions without adjustment for angle.

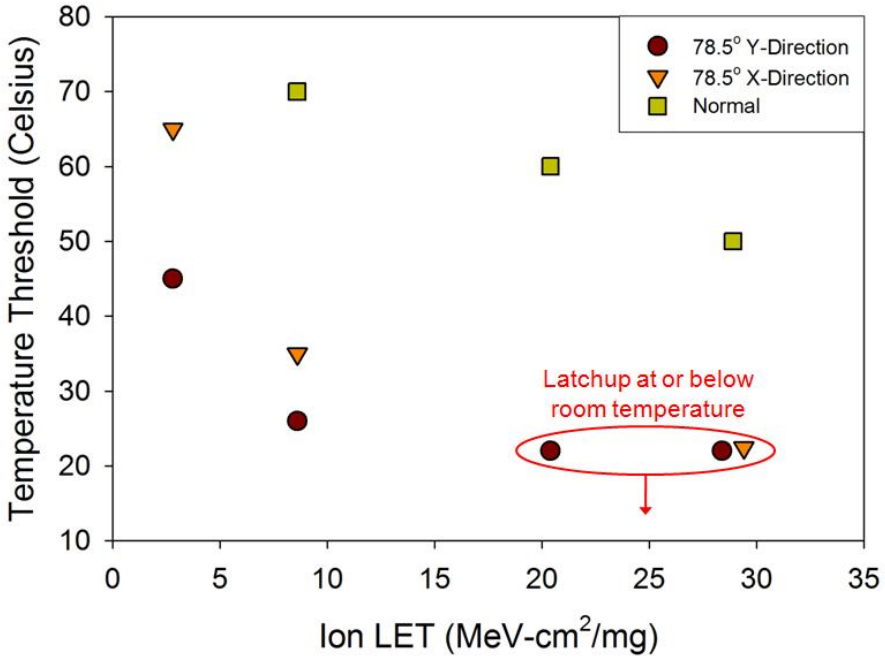


Figure 6.3. SEL temperature thresholds vs. particle LET. The LETs are not adjusted for angle of incidence. The circles with arrows indicate thresholds that are at or below the plotted values.

For the two lower LET particles (neon and argon), there was a significant temperature difference (20 °C and 6 °C, respectively) for the onset of SEL between X- and Y-grazing directions. For both of these particles, the SEL threshold temperature was greater for the X-grazing direction. This points to increased SEL sensitivity for the SRAMs when ions are oriented along the Y-grazing direction, which is parallel to the

well columns. For the highest energy krypton ions, the temperature threshold difference cannot be discerned because both X- and Y-grazing strikes for these particles latched the DUT at room temperature (22 °C), which is denoted by the circle and downwards arrow. The X-grazing orientation was not tested with copper ions. For normal incidence strikes, the threshold temperature for SEL decreases steadily with increasing LET.

Angular Effect on SEL Fluences

Due to the methodology for finding temperature thresholds at each ion/angle, there are not statistically significant data to show latchup cross sections for the test SRAMs. As described in the experimental setup, the DUT was exposed to a fluence of 5×10^7 ions-cm^{-2} (5×10^7 ions-cm^{-2} for normal incidence) before increasing the die temperature and exposing the DUT to another 5×10^7 ions-cm^{-2}. Figure 6.4 shows the fluence needed to latch the test part as a function of die temperature for 2.8 MeV-cm^2/mg Ne ions. Circled data points indicate that the DUT did not latch at the given temperature.

As expected, the necessary fluence to latch decreases with increasing temperature. The two data points at 65 °C and 70 °C for the X-grazing strikes are indistinguishable due to experimental error in measuring the fluence and statistical error resulting from a single measurement for each point.

Plotting the data for the 8.6 MeV-cm^2/mg Ar ion tests yields figure 6.5. For the Y-grazing beam orientation, a significant increase in device sensitivity occurs due to an increase of only 8 °C. A 10 °C increase in die temperature results in a smaller increase in device sensitivity for X-direction grazing orientation. For the normal incidence argon ions, SEL was detected at 70 °C with a fluence of 9×10^6 cm^{-2}.

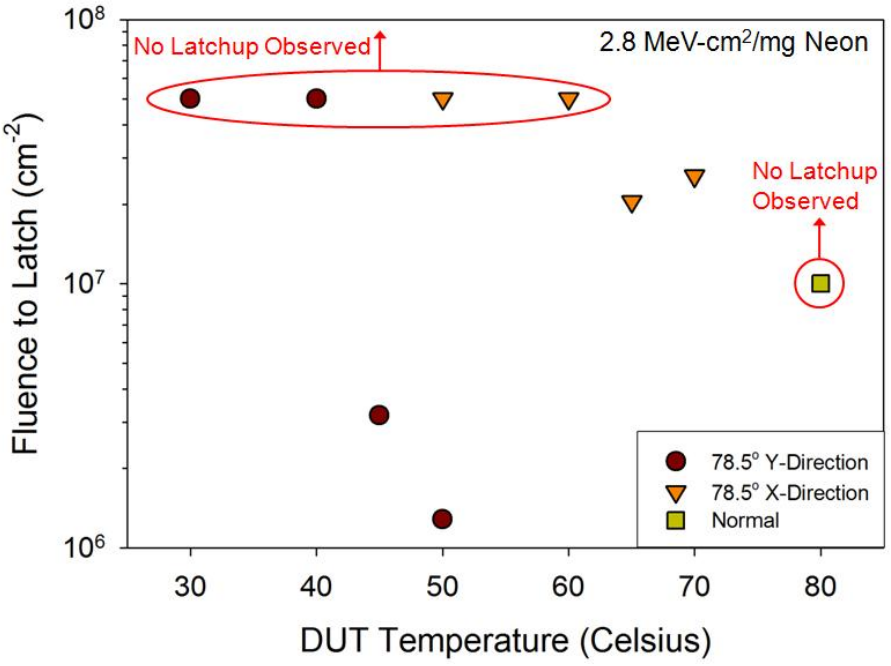


Figure 6.4. Fluence to SEL vs. die temperature for 2.8 MeV-cm^2/mg Ne. Y-grazing beam orientation is shown to be significantly more susceptible to SEL.

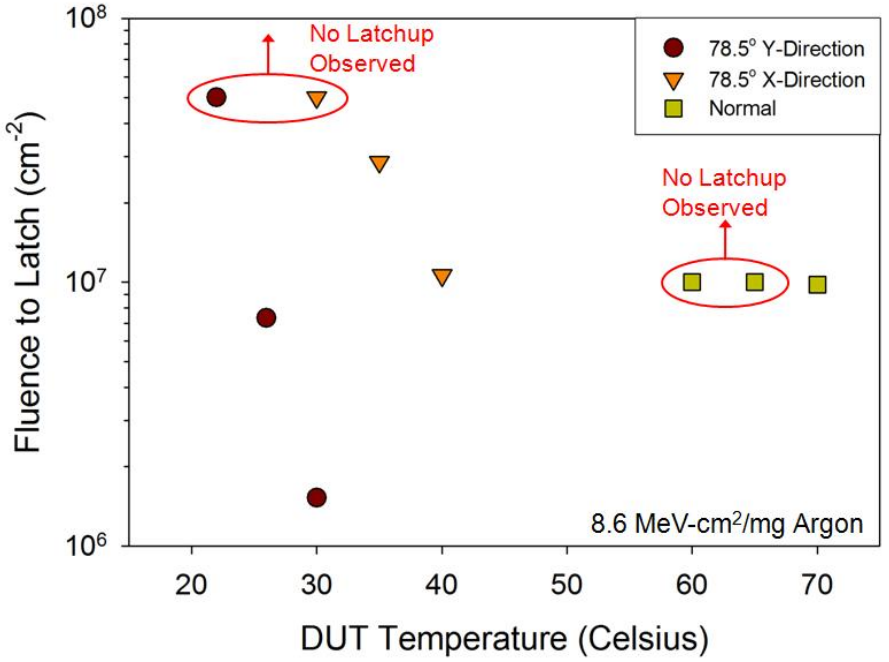


Figure 6.5. Fluence to SEL vs. die temperature for 8.6 MeV-cm^2/mg Ar. Y-grazing beam orientation is shown to be significantly more susceptible to SEL. Both Y-grazing and X-grazing beam orientations become much more susceptible to latchup with small increases in die temperature.

It should be noted that while SEL is observed for these heavy ion tests, these memories also were tested extensively with varying temperature using neutrons and protons, with no observation of SEL. For those particles, secondary fragments with sufficient LET to cause latchup may not have the range necessary to reach the sensitive regions of the devices or deposit enough charge (due to short path lengths) to initiate SEL.

Discussion

These experiments support the hypothesis [110] that the current JEDEC test standard for SEL [9] is insufficient to characterize device response for SEL completely. Using the current test protocols, these devices could be tested and confirmed to be latchup-immune for 2.8 MeV-cm^2/mg neon below 65 °C if only one grazing angle orientation is tested. Not testing for SEL at multiple grazing angles can underestimate the SEL rate and, in some instances, could result in a part that is SEL-vulnerable being declared latchup-immune.

From TCAD simulations [15] and electrical characterization techniques [129] discussed in Chapter V, both using the same 65 nm technology as in this experiment, it would be expected that no latchup would be observed at room temperature. For that plot of holding voltage versus temperature, the reader should refer again to figure 4.3. The simulations in Chapter V utilized minimum design-rule source-to-source (anode-cathode for parasitic latchup) spacing for the technology. The TCAD simulations and Boselli's work [129] shown in figure 4.3 predict onset of latchup susceptibility at ~340 K, or 67 °C. While the simulation/experimental holding voltage in Figure 5.4 explains the increases in cross sections and lower LET thresholds with increasing temperature, it does

not explain the SELs observed using 20.4 MeV-cm^2/mg Cu and 28.9 MeV-cm^2/mg Kr ions at room temperature using high grazing angles. However, this is because the source-source spacing in the high density SRAM cells is only 70% of the minimum design rule spacing for digital circuitry. It should be noted that it is common practice to pack devices more tightly in regularly repeating memory arrays than allowed in logic-circuitry design. In addition, the well and substrate resistances seen by sources in the SRAMs are much higher than those seen in the Chapter V structures as those devices were 20 μm wide. Given the 30% reduction in the base length of the parasitic bipolar transistors in the feedback path (anode-cathode spacing) and a more favorable biasing condition with increased resistances, the most sensitive devices in the SRAM arrays are vulnerable at room temperature. This explains the sensitivity of the high density arrays as well as sensitivity in the normal arrays with a small additional increase in temperature. As previously stated, the high performance banks are less sensitive to latchup due to wider anode-cathode spacing and greatly decreased resistances.

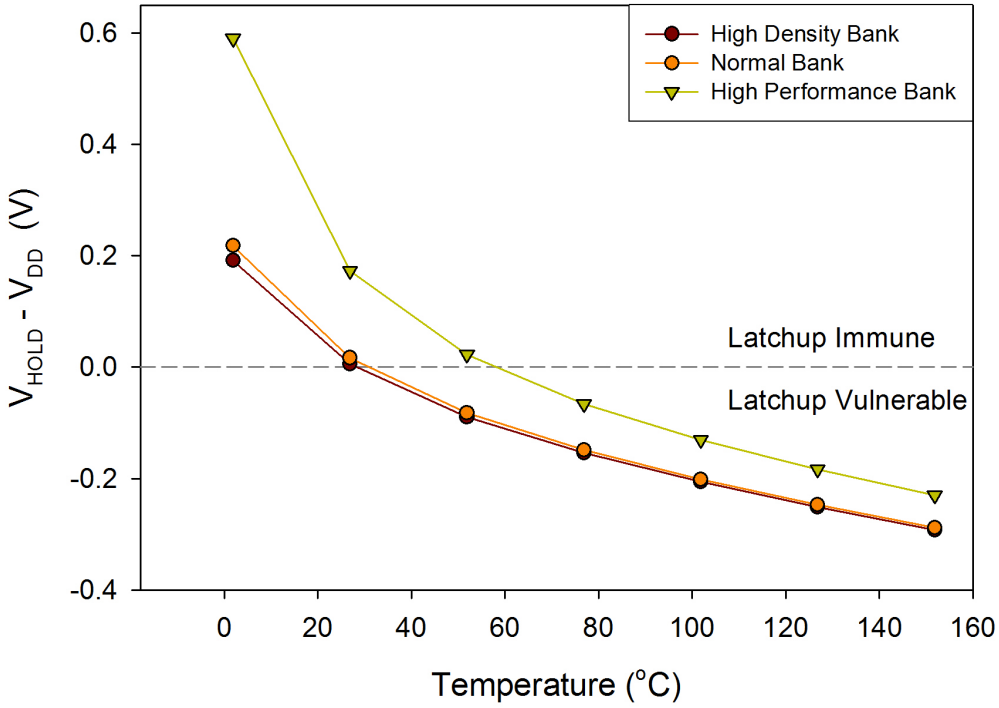


Figure 6.6. Approximation of latchup vulnerability for three different SRAM banks on the DUT vs. temperature from TCAD simulation. The difference in holding voltage and V_{DD} is plotted versus device temperature. Points above the line intersecting a Y-value of 0.0 are latchup-immune as indicated on the plot.

Figure 6.6 shows 2D TCAD simulations used to approximate holding voltage at a range of temperatures for a worst case anode-cathode pair (highest resistance to well/substrate contacts) in each of the three types of memory banks. This approximation is done by matching the A-K spacing in the chosen SRAM bank type and scaling the distances to the N- or P-well contacts to match the resistances seen by the anode-cathode pair in the center of the N and P-well columns. The simulation does not account for resistances created by the presence of the other SRAM cells in the columns. To emphasize the temperature threshold where the devices become vulnerable to latchup, the difference between the operating voltage V_{DD} and the holding voltage is plotted as a

horizontal line. This approximation indicates the temperature vulnerability threshold to be near room temperature and helps to explain the SELs seen during testing by comparing the different SRAM banks. As speculated, TCAD simulations suggest the high density and normal SRAM banks are the main contributors to observed latchup cross sections at 50 and 84 °C. While simulations show the high performance banks to be vulnerable at 84 °C, the much larger difference in holding voltage and V_{DD} for high density and normal banks results in a much lower LET threshold and larger cross section.

Ion-generated currents can change well potentials and trigger the latchup process. Charge not deposited directly into one of the well columns will still be collected and induce currents in the columns, albeit on a longer time scale. The deposited charge interacts most strongly with the nearest N- or P-well columns. For charge deposition close to a sensitive junction, there is high latchup sensitivity. Increased currents or potential changes in either well can contribute to the turn on of the complimentary bipolar transistor. The collector of each parasitic BJT is the base of the other.

The Y-grazing orientation is much more vulnerable to SEL than the X-grazing orientation. The high angle and Y-grazing orientation allow a large amount of charge to be deposited close to the sensitive junction, throughout a sensitive region that is strongly related to the length and shape of the N-well/P-well structure (see figure 6.1a). Figure 6.7 shows a section of an N-well/P-well column pair with grazing angle X-Direction and Y-Direction ion strikes depicted. Only a small portion of the column in the Y-Direction can be shown, as the columns in the SRAMs extend for tens of micrometers between well contacts. The ratio of the column height to the column width in the SRAMs is over 40:1. The P-well is wider than the N-well as there are four NMOS transistors to every two

PMOS transistors in a standard SRAM cell. Figures 6.8a and 6.8b show cut-planes of figure 6.7, depicting the grazing angle strikes in the X-Direction and Y-direction, respectively.

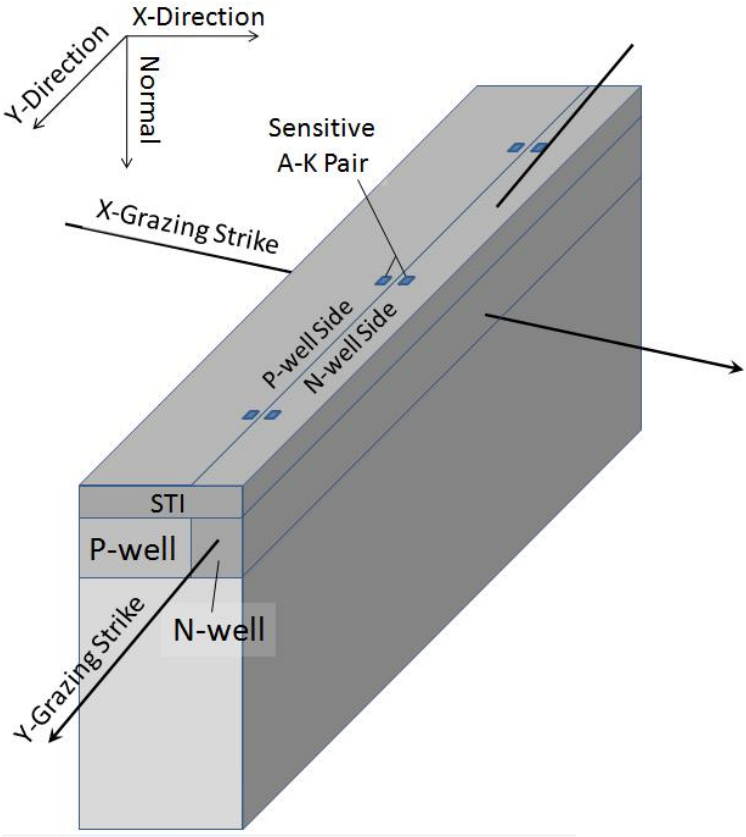


Figure 6.7. Depiction of a N-well/P-well column in an SRAM bank. Grazing angle strikes oriented along the X- and Y- lateral directions are included. Sensitive anode-cathode pairs occur regularly along the well boundaries and are included in the plot. Well contacts lie out of the frame of the figure in the Y-direction at the top and bottom of the columns.

When plotted as in figure 6.8, the geometric issues affecting the lateral dependence of SEL become clear. For the X-Direction strikes (figure 6.8a), the amount of charge deposited in and beneath a chosen N-well/P-well pair is constrained by the narrowness of the SRAM columns. In contrast, the Y-direction strikes (figure 6.8b) deposit more charge in the well, in addition to depositing charge close to the sensitive junction in the same well. As discussed in chapter III, the X-grazing strikes are not well

described by the effective LET conventions, as the pathlength through a particular well pair is quite short, even at grazing angles. In fact, at increasingly large angles the charge deposited in a particular N-well/P-well pair decreases.

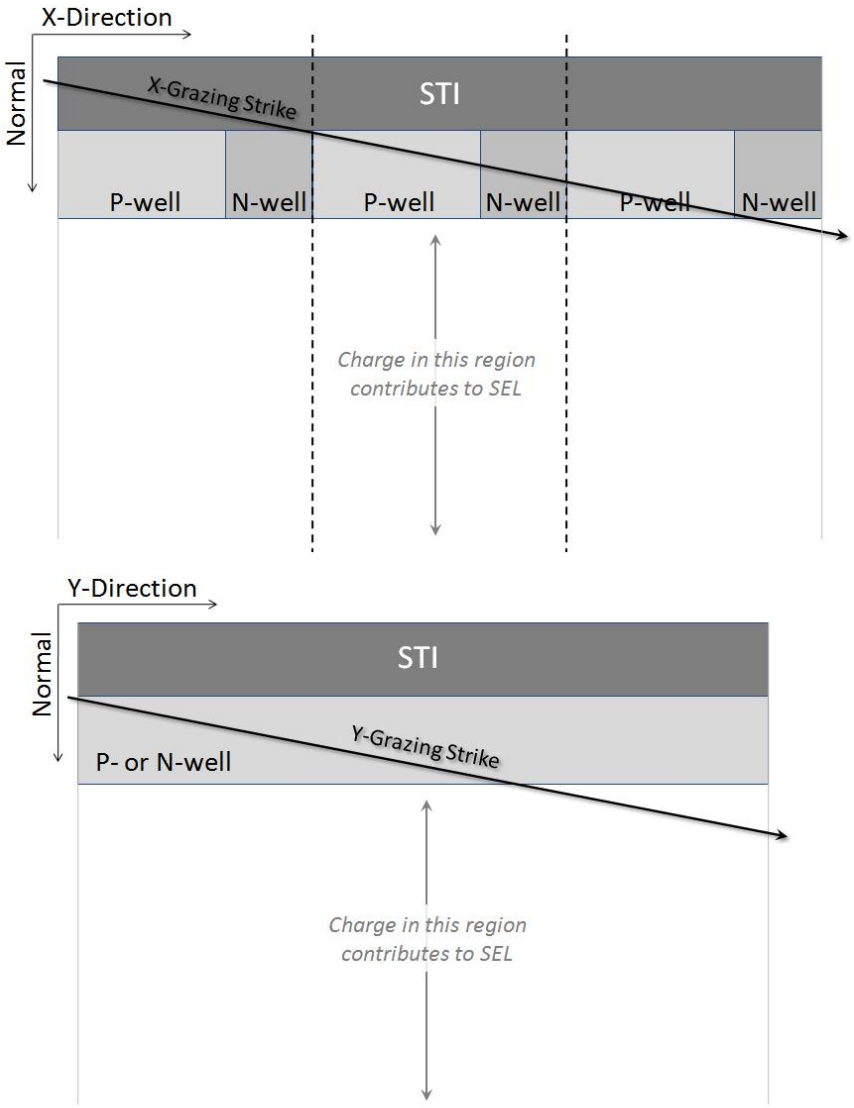


Figure 6.8. (a) Cross-section of an SRAM taken in the Normal-X-Direction plane. For strikes in the X-Direction, charge collection/interaction is constrained by the edges of the N-well/P-well column pair marked by the dotted lines (b) Cross-section of an SRAM taken in the Normal-Y-Direction plane. For strikes in the Y-Direction, charge collection/interaction is unconstrained and more charge will interact with a single P- or N- well column.

In addition to the strong effect of device geometry on constraining charge collection/interaction on a well pair in the X-direction, there is also the simulated evidence from Chapter V indicating higher SEL susceptibility for charge deposited along the N-well/P-well (or substrate) interface. Those interfaces are all oriented parallel to the Y-direction in the SRAM banks. The combination of this effect with the geometric effects explains the observed lateral sensitivity for SEL.

Summary

This chapter demonstrates single-event latchup due to heavy ions in a 65-nm CMOS technology, as well as experimentally- and simulation-based explanations for the change in susceptibility observed as the temperature increases. The experimental results validate the previously published theory presented in Chapter V that lateral orientation of incident particles can have a significant effect on device sensitivity. This is a clear example of why SEL testing needs to be performed at multiple lateral orientations during grazing angle tests in order to achieve an accurate picture of device vulnerability.

CHAPTER VII

SUMMARY AND CONCLUSIONS

This work has demonstrated the first observed SEL in 65 nm technology. While it has been speculated that SEL will cease to be an issue with continued scaling, that is not the case with this 65 nm technology for some operating conditions. From the properties of the devices seen in this work (holding voltage more than 0.3 V below operating voltage at high temperature, high resistances, and gain products above unity at room temperature) and the expected 1.0 V operating voltages at the 45 nm node, it is likely that SEL will be observed (at least with high temperatures) in that process node as well.

The results of this work, both simulation and experiments, show that the lateral beam orientation plays a major role in SEL sensitivity, particularly in highly directional geometries like the SRAMs tested and shown in Chapter VI. At the time of this writing, the widely-used JEDEC and ESA test standards for SEE testing do not account for these lateral variations in sensitivity. The importance of not qualifying parts for spaceflight or orbit using only these standards cannot be understated. Experimental results for the SRAMs in Chapter VI demonstrate a scenario where the cross-section, LET threshold, and temperature threshold for SEL could all be underestimated by significant amounts. With these kinds of variations in sensitivity due to lateral orientation, it is quite possible that a SEL-sensitive device could be validated as totally latchup-free if the additional recommended test steps are not undertaken. While this may create an addition burden in terms of beam test time, the ion and proton beam test time needed to check for these vulnerabilities is much less expensive than a non-functional system in orbit. Additionally, if the layout of the device is known, an educated decision to test in the most sensitive

direction (such as along the columns of the SRAM) could be used as a bounding case to reduce test time.

When validating parts for flight, observed SEL does not always prevent final qualification. If the SEL cross section is low enough to yield a very low expected SEL rate in the chosen environment, the part may still be integrated into the system. In the cases where this is done, it is imperative that there be some understanding of the effects of an SEL on the lifetime and reliability of a part. As shown in figure 3.1b, just because a part is still working after a single SEL (or several) does not mean that it will survive the rest of the mission lifetime. In these cases, an understanding of how much current is generated by the SEL and where that current is flowing is necessary. Lifetime modeling for affected interconnects after large current pulses caused by SELs should be used to determine whether the risks are acceptable for the chosen application.

In summary, this work provides insight into previous work covering the fundamentals of single event latchup as well as providing simulation, experimental, and theoretical foundations for understanding and properly testing for SEL in the deep-submicron regime.

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