# PATTERN IDENTIFICATION OF MULTIPLE CELL UPSETS IN STATIC RANDOM ACCESS MEMORIES TO RELATE EXPERIMENTAL TEST RESULTS TO SINGLE EVENT UPSET MECHANISMS

By

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To my wife, Dolores, without whom I would never be successful.

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LIST OF ABBREVIATIONS

| | |
|---|---|
| 2-D | Two Dimensional |
| 3-D | Three Dimensional |
| ALPEN | Alpha Particle Source-Drain Penetration |
| BAE | British Aerospace |
| BJT | Bipolar Junction Transistor |
| BL | Bit Line |
| $\overline{BL}$ | Bit Line Complement |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| DRAM | Dynamic Random Access Memory |
| EHP | Electron-Hole Pairs |
| FET | Field Effect Transistor |
| FPGA | Field Programmable Gate Array |
| LBNL | Lawrence Berkeley National Laboratories |
| LET | Linear Energy Transfer |
| LOCOS | Local Oxidation of Silicon |
| MCU | Multiple Cell Upset |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| NASA-GSFC | National Aeronautics and Space Administration Goddard Space Flight Center |
| nMOSFET | n-Channel Metal-Oxide-Semiconductor Field Effect Transistor |
| PBE | Parasitic Bipolar Enhancement |
| pMOSFET | p-Channel Metal-Oxide-Semiconductor Field Effect Transistor |
| SEE | Single Event Effects |
| SEL | Single Event Latchup |
| SET | Single Event Transient |
| SEU | Single Event Upset |
| SOI | Silicon-on-Insulator |
| SRAM | Static Random Access Memory |
| STI | Shallow Trench Isolation |
| TCAD | Technology Computer Aided Design |
| TAMU | Texas Agricultural and Mechanical University |
| TI | Texas Instruments |
| TID | Total Ionizing Dose |
| WL | Word Line |

# CHAPTER I

# INTRODUCTION

The objective of this research is to develop an understanding of the properties of multiple cell upsets (MCUs) in static random access memory (SRAM) fabricated in highly scaled geometries (< 250 nm). Early work in MCU properties on SRAMs [Mu96] categorized the observed upset cross sections in terms of single-cell upsets and double-cell upsets. As the deposited energy increased, the amount of double-cell upsets of MCUs increased, but the amount of single-cell upsets decreased. Techniques for error rate prediction apply standard failure curves that monotonically increase [Pe97]. So, categorizing SRAM single event upsets (SEUs) into n-tuples (e.g., single, double, triple) leads to failure analysis that does not always monotonically increase or fit standard failure models. This type of categorization still exists today, though the number of MCUs observed has significantly increased. This research has evaluated the underlying soft error mechanisms of an individual SRAM cell and an SRAM array and has developed a modeling and simulation approach to determine the MCU characteristics. This research enables the categorization of MCUs observed in SRAM radiation effects testing so that the fundamental theories of failure can be applied to estimate soft error rates in a given radiation environment.

This dissertation is composed of ten more chapters. Chapter II, Background, will introduce basic concepts which are the buildings blocks for the remainder of the document. In this chapter, some basic concepts in semiconductor physics and single event

physics, as well as approaches for modeling single events in semiconductors, are presented.

Chapter III, Single Event Charge Collections Mechanisms, and Chapter IV, Well-Collapse Source-Injection, provide a description of the previously known charge collection mechanisms and the mechanism identified in this research. The mechanism, well-collapse source-injection, is introduced in Chapter III, but is the sole subject of Chapter IV.

Chapter V and Chapter VI discuss the SRAM cell and SRAM array, respectively. In Chapter V, the SRAM cell is described along with the application of the charge collection mechanisms. Chapter VI extends this discussion to an SRAM array. In this chapter, the relationship of the charge collection mechanisms to MCU observations will be made.

Chapter VII, Modeling and Simulation of SRAM, describes the single event models for SRAM cells and arrays that were developed and applied to this research. These models enabled the determination of the well-collapse source-injection mechanism and the determination of how many SRAM cells in the array were affected.

Chapter VIII, Experimental Results of Single Event Effects in SRAM, describes experiments performed with heavy ions. These data are correlated to the array upset mechanisms and used to assess the range of the well-collapse source-injection mechanism.

Chapter IX and Chapter X extend the discussion of the mechanism beyond SRAM. Chapter IX, Implications of Well-Collapse Source-Injection Mechanism, shows that this mechanism is applicable to several different research areas currently pursued in

single event effects. Chapter X, Well-Collapse Mitigation Approaches, presents some hardening approaches that can be applied to retard the well-collapse and reduce the specific number of MCUs per single event.

Finally, Chapter XI concludes the document. This will summarize the major contributions of the research and highlight the future extensions of this work.

# CHAPTER II

# BACKGROUND

## Semiconductor Physics

### Carrier Physics

This section briefly presents the fundamental physics of semiconductor carriers (electrons and holes) in terms of mobility, resistivity, and current densities. The equations discussed in this section will be used later in this dissertation. This section is largely based on Chapter 1 on Muller and Kamins [Mu03], which provides a more detailed discussion of the topic.

Mobility describes how easily a carrier will move in response to an applied electric field. As seen in the following two equations, the carrier drift velocity is directly related to its respective mobility and the applied electric field. In equations 1 and 2, $v_d$ is the drift velocity (with subscript e or h for the type of carrier), $\mu_n$ is the electron mobility, $\mu_p$ is the hole mobility, and $\xi$ is the electric field.

$$v_{d_e} = -\mu_n \xi \tag{1}$$

$$v_{d_h} = \mu_p \xi \tag{2}$$

The mobilities depend upon the carrier charge, mean scattering time, and the effective mass. Electrons typically have higher mobilities, by a factor of 2-3 times. Also, carrier mobilities tend to decrease with either increased carrier density or increased temperature.

The current density in an applied electric field is a function of the number of carriers that pass through a unit volume per unit time and is related to the equations for drift velocity. The total current density due to electrons and holes is given in equation 3, where $J$ is the current density, $n$ is the number of electrons/cm$^3$, $p$ is the number of holes/cm$^3$, and $q$ is the electron charge.

$$J = (nq\mu_n + pq\mu_p)\xi \tag{3}$$

Equation 3 is a form of Ohm's law where the quantity in the parentheses is the conductivity of the material. Since resistivity is the inverse of conductivity, the material's resistivity is calculated by equation 4.

$$\rho = \frac{1}{(nq\mu_n + pq\mu_p)} \tag{4}$$

Even though carrier mobility decreases with carrier density, the general trend in resistivity is to decrease with increased carrier density. In this research, carrier mobilities and densities will be taken from simulation results, and equation 4 will be used to calculate the material resistivity. Equation 5 will then be applied to calculate the resistances in the semiconductor layout. In this equation, $l$ is the length between resistor ends, and $A$ is the area that the carriers traverse.

$$R = \frac{\rho l}{A} \tag{5}$$

Besides the motion of carriers in an electric field, the other important concept related to single event effects (SEE) is diffusion current (i.e., the diffusion of carriers). The diffusion of carriers is based on a gradient of carrier concentration, namely, a change in carriers per unit distance. Equation 6 gives the diffusion current density due to carrier gradients. In this equation, $k$ is Boltzmann's constant, and $T$ is temperature in Kelvin.

$$J = q(\frac{kT}{q}\mu_n)\frac{dn}{dx} - q(\frac{kT}{q}\mu_p)\frac{dp}{dx} \tag{6}$$

The quantities inside the parentheses in equation 6 can be replaced with the diffusion constants $D_n$ and $D_p$, respectively.

P-N Junction Diode Characteristics

Diodes formed by p-n junctions in semiconductors play an extremely important role in the determination of single event effects. In reverse bias, the diodes have an electric field to move carriers from one type of doping to the next. In forward bias, the diodes inject minority carriers into the semiconductor. The first p-n junction diode characteristic to be discussed is the built-in potential, which is related to the material dopings. This term is important in this research for two reasons: (1) to help interpret the technology computer aided design (TCAD) output plots and (2) to know when a p-n junction diode has been maximally forward biased. $\Phi_n$ is the potential at the neutral edge of the n-doped material, $\Phi_p$ is the potential at the neutral edge of the p-doped material, and $\Phi_i$ is the built-in potential. All three potentials are calculated using the following three equations.

$$\Phi_n = \frac{kT}{q}\ln\frac{N_d}{n_i} \tag{7}$$

$$\Phi_p = \frac{-kT}{q}\ln\frac{N_a}{n_i} \tag{8}$$

$$\Phi_i = \Phi_n - \Phi_p = \frac{kT}{q}\ln\frac{N_d N_a}{n_i^2} \tag{9}$$

In these equations, $N_d$ is the doping density in the n-type material, $N_a$ is the doping density in the p-type material, and $n_i$ is the intrinsic carrier density.

In reverse bias, the important diode characteristics are the depletion region width and the maximum electric field in the depletion region. Equation 10 provides the calculation of the depletion region width as a function of applied voltage, $V_a$. In this equation, $x_d$ is the depletion region width, and $\varepsilon_s$ is the permittivity of the semiconductor.

$$x_d = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(\Phi_i - V_a)} \tag{10}$$

Note that in reverse bias, the applied voltage is negative and only serves to increase the depletion region width. The maximum electric field can be calculated from equation 11. This equation is derived for step junctions, but it does serve to show the trend of the electric field versus applied voltage.

$$\xi_{\max} = \frac{2(\Phi_i - V_a)}{x_d} \tag{11}$$

It is easy to see that, even in the absence of an applied voltage, there still is an electric field to cause carrier drift. There just tends to be no current flow without an applied reverse bias voltage.

In forward bias, the p-n junction diode will become a source of minority carriers. For small forward bias, equations 12 and 13 will demonstrate this basic concept for low-level carrier injection. In these equations, $n_p$ means the electron density in the p-type material at the edge of the depletion region, and $n_{p0}$ means the equilibrium electron density when there is no applied voltage. $p_n$ and $p_{n0}$ are the hole densities in the n-type material.

$$n_p = n_{p0}(e^{\frac{qV_a}{kT}} - 1) \tag{12}$$

$$p_n = p_{n0}(e^{\frac{qV_a}{kT}} - 1) \tag{13}$$

The equations for high-level injection, where the injected carrier densities are at or above the doping density, are not presented. The research will rely on the TCAD tools to solve for the carrier densities in that case. Equations 12 and 13 are only valid at the edge of the depletion region. If the diode were to remain in a constant forward bias, the minority carrier concentration would exponentially decrease as the carriers get farther away from the depletion region edge. The exponential decay is then a function of the carrier lifetimes. Once again, this research will make use of the TCAD tools to provide the carrier distributions, but the physics presented here provides the underlying principles.

## Single Event Physics

### Carrier Generation

Radiation environments consist of charged particles (electrons, protons, alphas, and heavy ions) and neutral particles (neutrons). In space orbits around the Earth, there are proton and electron belts with significant abundance of those charged particles. Galactic cosmic rays and solar flares produce heavy ions. Alpha particles are emitted from radioactive impurities found in microelectronics packaging material. Neutrons are secondary radiation particles resulting from the interaction of heavy ions with atmospheric particles [Ba01].

Radiation particles can interact with all materials or regions in a microelectronics device. As radiation particles pass through a semiconductor material, they lose energy by Coulomb scattering with the nuclei of the lattice. Energy is transferred from the particle to bound electrons which are ionized into the conduction band, thus leaving a track of electron-hole pairs (EHPs). This is referred to as direct ionization and is demonstrated in Figure 1. The figure shows a charge track down through the silicon after some initial charge transport with charge generation of approximately $2x10^{19}$ carriers/$cm^3$ in the center of the track with a radius of approximately 0.5 μm. The radius of the charge track is the result of the initial charge transport. This plot is an example from a TCAD simulation where the charge generation in charge/length and a track radius are input parameters. EHPs generated in the metal layers of the microelectronics are generally of no consequence. EHPs generated in the oxides typically contribute to total ionizing dose (TID) effects. The EHPs generated in the semiconductor regions contribute to single event effects. Incident radiation particles can also create a nuclear interaction between the target nuclei and the incident ion, such as the Si, O, doping elements, metallization materials, and processing impurities. A nuclear interaction can result in an ionized heavy ion, which can then create EHPs through direct ionization. The incident radiation particle then creates EHPs through indirect ionization.

The rate of this energy loss to EHP creation is often expressed as stopping power or linear energy transfer (LET), which has the dimensions of energy per unit length along the path of the particle. The LET of an ion depends on the charge of the ion, as well as the density of the target material. Thus, units of LET are usually MeV-$cm^2$/mg, or converted to MeV/μm in a specific target material. In Si, the charge generation is

approximately 0.01 pC/μm for an LET of 1 MeV-cm$^2$/mg. So, in Figure 1, the charge track is simulating a heavy ion with LET of approximately 20 MeV-cm$^2$/mg. It is important to note that the charge generation along an ion's track is random in nature; these approximations are averaged over long path lengths.

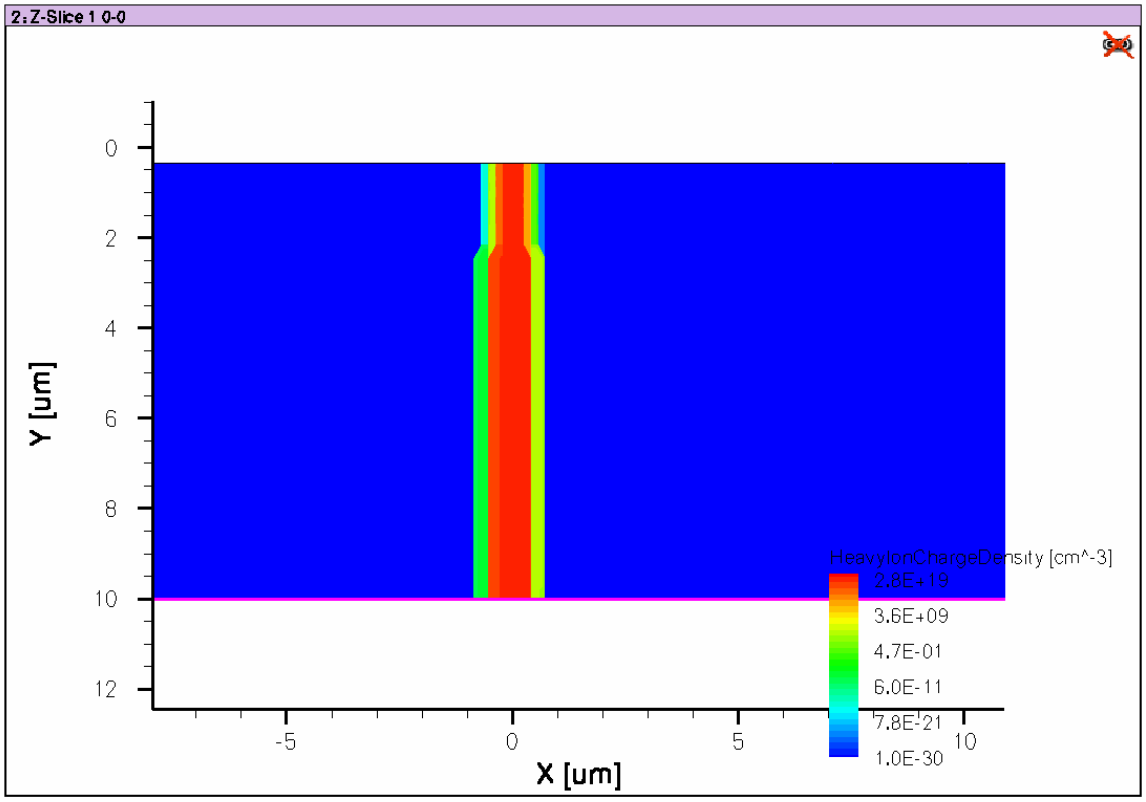



Figure 1. Example of heavy ion charge generation track, (charge deposition = 0.2 pC/μm).

## Equilibrium Recovery

The previous section discussed how a single event can generate excess carriers (EHPs) in the semiconductor material. This section briefly discusses the physical processes that return the material to equilibrium carrier concentrations. The excess carriers, like the carriers already present in the material, are governed by the same

principles of motion. In the presence of an electric field, the carriers will drift, and in the presence of a carrier gradient, they will diffuse. Note that the initial EHP generation on the ion track will automatically create a carrier gradient for both electrons and holes. In general, the minority carrier gradient is much higher, resulting in increased disbursement from the original ion track. An example of this is shown in Figure 2 from the same charge track given in Figure 1. In the example, the charge track was in a highly doped p-substrate, where the holes are the majority carriers. In the image on the right, there is a small gradient near the top of the silicon where the substrate is more lightly doped, but the gradient is still only about two orders of magnitude. However, in the image on the left, the gradient for electrons is about 20 orders of magnitude and will diffuse more rapidly. This is why it is not important to match the radius of the heavy ion charge track in simulation, since the immediate carrier motion due to diffusion will overwhelm any difference in the radius.

The excess carriers will be reduced in the semiconductor material by encountering and interacting with another region of the microelectronics device or through recombination. Carriers that encounter a semiconductor-oxide interface typically do not move into the oxide. So, the semiconductor-oxide interface can be interpreted as a reflecting boundary. Carriers that encounter a metal boundary can cross the boundary and be removed from the semiconductor region. The last process governing the return to equilibrium is recombination. It is noted that the time scale for recombination is typically much longer than the single event responses seen in this document, so it does not play a role in the single event response.

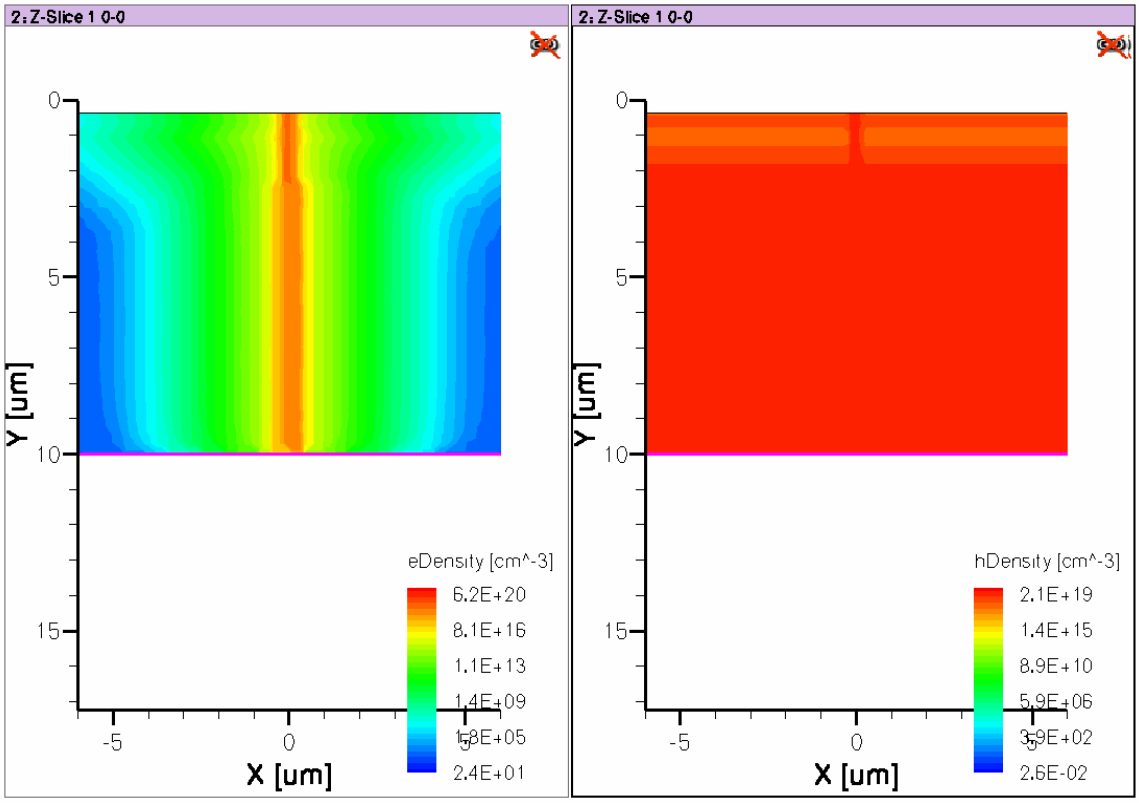



Figure 2. Examples of minority (electron) carrier densities and majority (holes) carrier densities 1 ps after the charge generation.

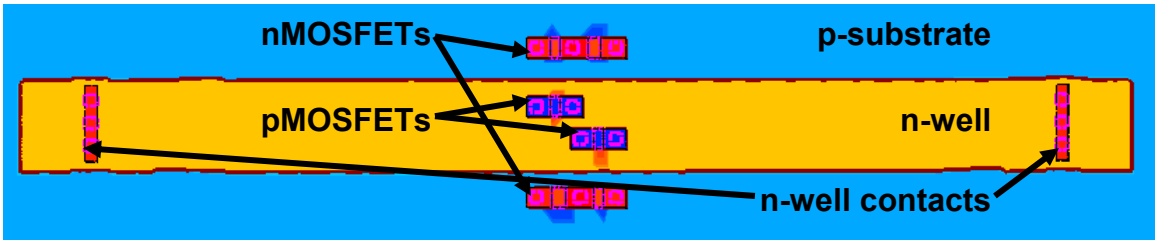
## Single Event Modeling

In the previous section, the charge generation by a single penetrating ion was discussed as well as the guiding physics that control the charge motion and the return to equilibrium. This section will briefly introduce the modeling approaches used in this research. The goal is to model the relationship between the single event charge generation and the response of the microelectronics circuit. These models can then be used to: (1) assess the response of an individual circuit to specific heavy ions, (2) assess the single event response of multiple circuits placed in close proximity in the microelectronics design, (3) develop and simulate the effectiveness of hardening schemes, and (4) predict

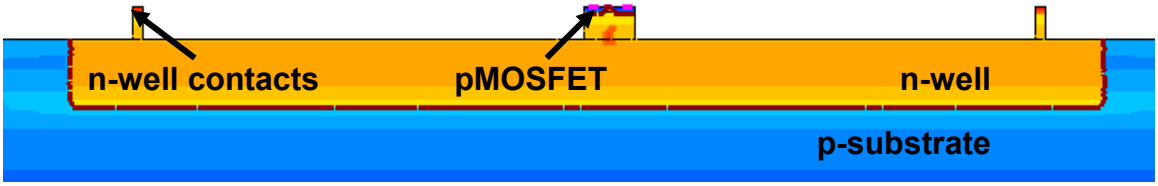
the single event response for particles that cannot be easily evaluated in ground-based testing facilities.

## Device Single Event Modeling and Simulation

Tools that solve the transport equations for carriers (electrons and holes) by applying the semiconductor physics equations in a spatial rendering are called device simulations and are part of a TCAD set of tools. Device tools typically support both two-dimensional (2-D) and three-dimensional (3-D) modeling. These tools numerically solve the Poisson and carrier continuity equations for specified device conditions. The user provides the spatial information about the layout of the circuit to be modeled (e.g., transistor size), builds the circuit using process information (e.g., shallow trench isolation (STI) depth and doping profiles), and applies circuit connectivity through contact boundary conditions. The user then must mesh spatial nodes for the simulator to perform numerical solutions. This last step is critical to the results; using too many mesh points can result in long simulation times, while using too few mesh points can result in inaccurate results [Bu01, Law06]. An example of a 3-D device model is shown in Figure 3. This full SRAM cell model was used in this research. In Figure 3b, note the difference in height of the Field Effect Transistors (FETs) and well contacts from the well. This is typical of advanced processes using STI. In this model, the STI is modeled as air, which, in simulation, is a reflective barrier to both the electrons and holes. An example of mesh points is shown in Figure 4. The FETs are highly meshed (points are indistinguishable in the figure), the n-well and p-substrate around the FETs are meshed with lower density, and the rest of the model receives the lowest meshing.




(a) Top view




(b) Side view

Figure 3. Sample 3-D device circuit model rendered in 2-D showing (a) top view and (b) side view.

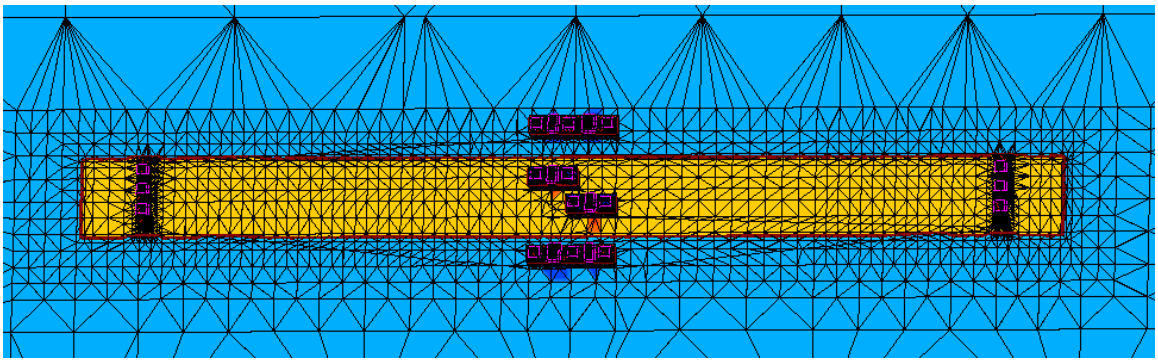


Figure 4. Sample 3-D device circuit model showing mesh points in top view.

For single events, these device tools are used to model the collection dynamics of the charge deposited by a heavy ion. The single event is described as a charge deposition in units of pC/μm. TCAD modeling has many advantages for single event simulation. All of the single event mechanisms discussed in the next section are typically modeled. In fact, the use of TCAD modeling enabled the identification of the advanced mechanisms

described in this dissertation. Device single event modeling and simulation has one severe limitation. The size of the circuit to be implemented is fairly limited. The most useful device simulation will be 3-D; however, a small SRAM circuit would require hundreds of thousands of nodes to process. The computational time needed to process that number of nodes for two nanoseconds of simulation time can be quite large.

### Compact Single Event Modeling and Simulation

Compact tools model the electrical responses of elements (e.g., transistors, diodes, resistors) in a circuit. The models of the transistors can vary from very simple to very complex, depending on the source of the model. Transistor models from the process foundry will typically fall into the complex category and include many inherent parasitic resistances and capacitances within the modeled device. Subcircuits are created by wiring the components either by writing a 'netlist' or graphically developing a schematic circuit diagram [Bu01].

At this level of SEE modeling, the specific locations of transistors and their respective distances to well contacts are not known. Thus, it is difficult to model and simulate the exact charge generation from the ion strike, especially given the potential charge generation near two or more components. Another disadvantage of compact modeling is that the transistor model lumps parameters together so that the charge generation mechanism cannot be physically implemented. Though it may be difficult to model and simulate the charge generation as it would actually occur (i.e., as the initial single event circuit response propagates through transistors and circuit elements), this type of modeling becomes much more useful. The transistor models are designed to

simulate time-dependent and frequency-dependent transfer functions. So, if one can accurately represent the initial circuit response, then the propagated outputs or circuit responses will represent the actual response. Although compact modeling does not play a direct role in this research, it is included in the background because the research makes use of many previous efforts that developed compact models for SEE simulation.

## Mixed-Mode Single Event Modeling and Simulation

The term mixed-mode refers to a simulator that combines device modeling with compact modeling to create a unified simulation environment in which the effects of single events on a particular circuit element can be studied at the circuit level. Early mixed-mode simulation tools were developed for circuits in which a device model existed for a critical component, but for which compact circuit models were unavailable or difficult to create for a physical characteristic or interaction of interest [Rl88]. The SPICE and PISCES simulation engines were bridged with appropriate software to permit a PISCES device model to run in conjunction with simple SPICE-level models for the remainder of the circuit elements. The advantages of this technique quickly became apparent in the radiation effects community, and today many commercial TCAD simulators support mixed-level simulations for single event effects.

There is one primary difficulty with compact circuit SEE modeling and simulation, namely, the generation of an accurate circuit response. But, once that response is generated within the circuit, these tools become a lot more accurate in propagating the signals. Device simulators can much more accurately represent the circuit response due to the single event charge generation, but are limited by the size of a circuit

that can be modeled. Mixed-mode SEE modeling and simulation it is widely used because it removes these two limitations.

In a mixed-mode simulation of SEE, the struck device is modeled in the "device domain" (i.e., using 3-D device simulation), while the rest of the circuit is represented by compact circuit models, as illustrated in Figure 5. The two regimes are tied together by the boundary conditions at contacts, and the solution to both sets of equations is rolled into one matrix solution [Rl88, My93]. The advantage is that only the struck transistor is modeled in multiple dimensions, while the rest of the circuit consists of computationally-efficient compact models. This decreases simulation times over multiple-transistor device models and greatly increases the complexity of the external circuitry that can be modeled.

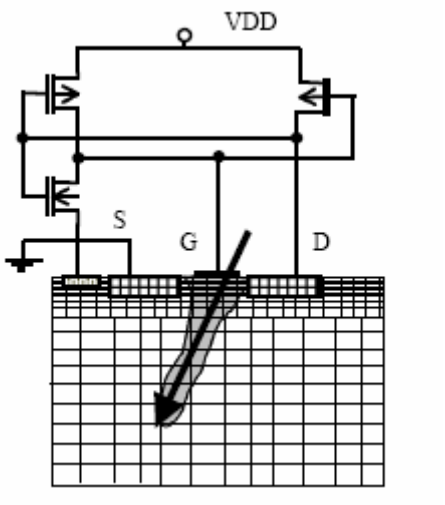



Figure 5. Mixed-mode simulation example of cross-coupled inverters (after [Bu01]).

A potential drawback of the mixed-mode method is that coupling effects between adjacent transistors have been shown to exist at the device level using 2-D simulations [Fu85] and later in 3-D simulations [Bl05, Ol05]. These effects cannot be taken into

account when only one transistor, the struck transistor, is modeled at the device level. To consider multiple node charge generation in mixed-mode simulation, more than one transistor needs to be simulated. One method, and the method generally applied in this research, is to simply model an entire cell in a 3-D device tool. Roche et al. performed mixed-mode modeling with a full 3-D device model of an SRAM cell. The authors compared the results to standard mixed-mode simulations and found that, in cases where no coupling effects between transistors existed, mixed-mode simulations were adequate to reproduce the full SRAM cell results. For some strike locations; however, coupling effects were observed between adjacent transistors. Mixed-mode simulations with a single transistor device in the device simulator are incapable of predicting such effects [Ro98]. Although this research modeled an entire SRAM cell in 3-D TCAD, it also used mixed-mode modeling through the addition of passive components to model radiation hardening techniques.

# CHAPTER III

# SINGLE EVENT CHARGE COLLECTION MECHANISMS

Chapter II introduced the concept of charge generation and deposition in a semiconductor region. These excess carriers will move through drift and diffusion mechanisms. Charge deposition deep into the bulk of the semiconductor is typically of no consequence; it will eventually recombine. However, charge that is deposited at the top of the semiconductor, near p-n junctions, can lead to unintended charge collection and single event currents. There are several mechanisms for this single event charge collection; these are divided into direct and indirect processes.

## Direct Charge Collection

Direct charge collection processes that lead to a prompt single event current include depletion region drift collection and field-assisted funnel collection. Another process, diffusion collection, can lead to a delayed single event current.

### Prompt Charge Collection

Figure 6 shows an ion penetrating the depletion region of a p-n junction. The built-in electric field causes electrons to be swept to the n-doped region, while holes move to the p-doped region. All p-n junctions will have a depletion region and an electric field, so carriers will be swept, whether forward or reversed biased. However, current pulses typically occur only when there is an applied reverse bias in addition to the built-in

voltage. Early on in the investigations of ionizing particle effects on junctions, Hsieh et al. recognized [Hs81] that the creation of a highly-concentrated free carrier track within a junction depletion region perturbs the region itself. Therefore, the simplified depletion current density calculation in equation 3 does not adequately describe the actual charge collection. Hsieh showed that the generated carrier track created as an alpha particle penetrates a junction severely distorts the potential gradients along the track length, creating a field funnel. As a result, the prompt current from a single event through a depletion region is the combination of the depletion region drift charge collection and the field-assisted funnel collection as shown in Figure 7.

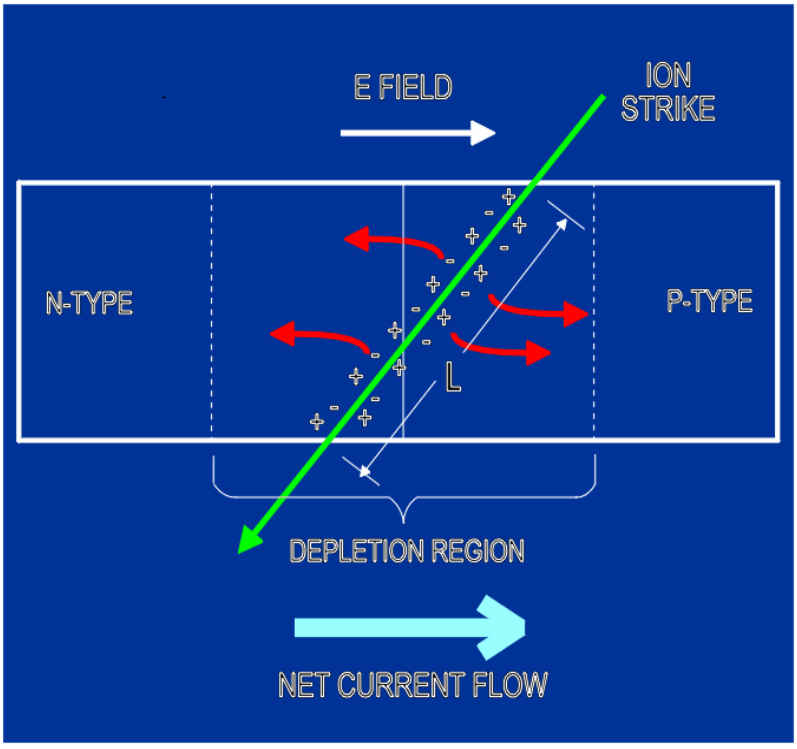



Figure 6. Depletion region drift charge collection in a p-n junction (after [Ma93]).

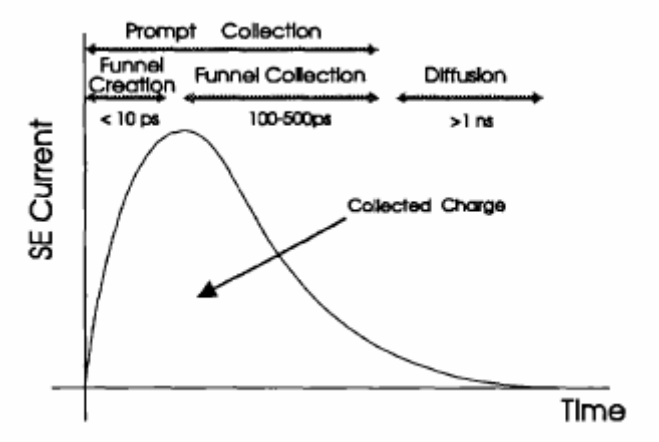



Figure 7. Typical shape of the total direct charge collection single event current at a p-n junction.

Delayed Charge Collection

Charge generated outside the funnel region, but within a diffusion length of a p-n junction, can diffuse to the junction and then be swept across the depletion region, leading to another direct charge collection mechanism [Ki79]. Diffusion charge collection will occur in the struck p-n junction, but may also occur in other neighboring p-n junctions, as shown in Figure 8. Diffusion is a much slower process, so this current component is delayed with respect to the prompt mechanisms illustrated in Figure 7. Typical time domains are hundreds of picoseconds to nanoseconds for diffusion collection. Because of the complex, three-dimensional nature of the diffusion charge transport, charge collection by this method depends strongly on the geometry of the circuit layout and the distance from the strike location to junctions in close proximity.

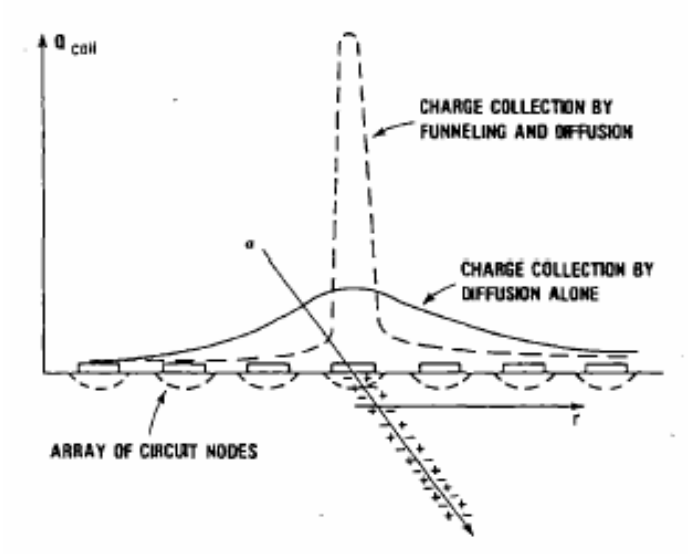



Figure 8. Diffision of charge to neighboring circuit nodes (after [Mc82]).

## Charge Collection Enhancements and Indirect Charge Collection

Along with the direct charge collection mechanisms, there are a few indirect charge collection mechanisms and enhancements. Many of these have been discovered through the use of TCAD device modeling of the charge deposition and collection, as was the field-assisted funnel charge collection process. While the direct charge collection mechanisms exist in all semiconductor types, some indirect charge collection mechanisms are only prominent in certain types of semiconductors. The charge collection enhancements discussed are the Alpha Particle Source-Drain Penetration (ALPEN) effect and parasitic bipolar enhancement. The indirect charge collection mechanisms discussed are ion shunt and well-collapse source-injection. The last of these is a finding in this research effort.

Alpha Particle Source-Drain Penetration (ALPEN) Effect

The ALPEN charge collection mechanism results from a disturbance in the channel potential that Takeda et al. referred to as a funneling effect [Ta88]. The effect is illustrated in Figure 9, and was based upon an ion strike that passes through both the source and the drain. Immediately following the ion strike, there is no longer a potential barrier between the source and channel. This can lead to significant source-drain conduction current, which mimics the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) device being on. This mechanism was revealed by 3-D alpha-particle simulations and has been experimentally verified [Do99, Ta88].

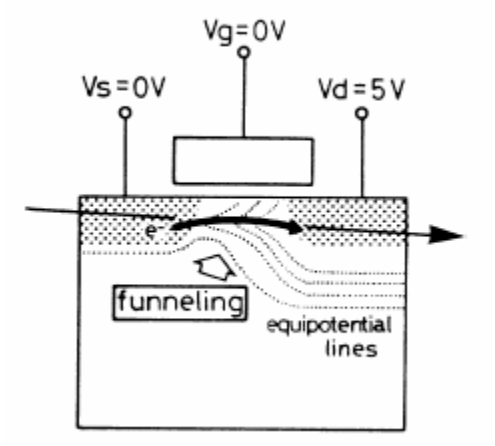



Figure 9. Illustration of the ALPEN effect (after [Ta88]).

Parasitic Bipolar Enhancement

An effect first observed in Silicon-on-Insulator (SOI) MOSFET devices, which now can also be important in bulk MOSFET devices, is parasitic bipolar enhancement. If the potential near the hit is large enough to cause minority carrier injection across the body source junction, then parasitic bipolar action can be created between the source and

drain. The current created by the ion strike is in effect the base current for this parasitic bipolar transistor; this base current can be amplified to create a large collector current at the sensitive node. Thus, the single event current is amplified with the gain of the parasitic bipolar transistor [Ke89]. The interesting item of note in this mechanism is that direct charge collection processes are the sources of the base current. So, the parasitic bipolar action tends to amplify the direct charge collection [Wo93].

Ion Shunt

Figure 10 shows a unique and interesting phenomenon that had become important in modern, dense integrated circuits where geometries are scaled to small dimensions. This indirect charge collection mechanism is called ion shunt, but in current state-of-the-art microelectronics processing generations (e.g., 65-nm, 90-nm, 130-nm), ion shunting appears no longer important. In this figure, an ion track of free carriers has penetrated two proximal junctions. Since the ion track, while it exists with a high carrier concentration, acts as a conductive path, the path between the two n regions in the figure can act as a current conduit, or resistive connection, between the regions. Charge that was not even generated by the ion hit can move through this conduit just as current through a wire [Ha85, Zo87].

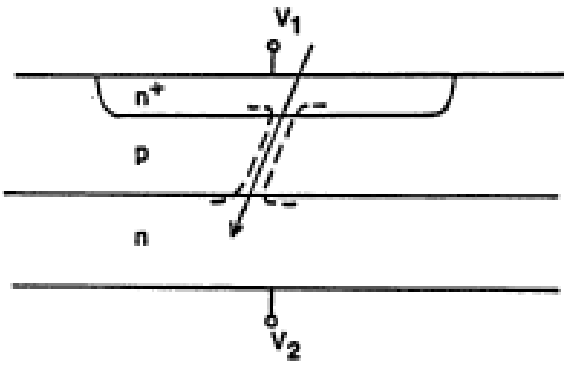



Figure 10. Simplified view of the ion shunt effect (after [Ha85]).

There are many possible reasons why the ion shunt mechanism does not apply for the current state-of-the-art microelectronics generations. However, this research focuses on one main reason. In order for the ion shunt to form and maintain a conduit for current, the n+-doped drain must start at a low potential, the p-doped well must start at a low potential, and the n-doped substrate must start at a high potential. Also, when the ion strike occurs, the potentials of the well and substrate must remain relatively constant, keeping the p-n junctions reversed biased. Thus, the well and substrate region near the strike must have a low resistance connection to power, $V_{DD}$, or ground, $V_{SS}$. Consider the single event current generated at the well/substrate p-n junction as a current sink. This current must be supplied from the $V_{DD}$ or $V_{SS}$ contact(s). This current is limited by Ohm's law as demonstrated in equation 14. In this equation, $I_{p,limit}$ is the limit of single event current that can be supplied through these contact(s), and $R_c$ is the resistance from the well/substrate strike to the contact.

$$I_{p.limit} = \frac{V_{DD}}{R_c} \tag{14}$$

Any single event current draw approaching the limit will result in a significant potential drop from the contact to the well/substrate charge collection location. So, in order to maintain the well or substrate potential, either $V_{DD}$ must be high or $R_c$ must be low or a combination of the two. These are both challenges in current state-of-the-art microelectronics technology generations. $V_{DD}$ is about 1 V and $R_C$ is high due to processing with STI. This will be demonstrated with more detail later in this document.

Well-Collapse Source-Injection

Indirect charge collection from the well-collapse source-injection mechanism is one key finding of this research. It is introduced here to discuss the similarities and differences with the ion shunt mechanism. The next chapter provides additional details of the mechanism.

Like the ion shunt mechanism, the well-collapse source-injection mechanism requires charge collection at a well/substrate p-n junction. The second similarity is that the effect is related to the single event current limit given in equation 14. The main difference is that this mechanism requires the well potential to collapse, whereas the ion shunt requires the well potential to remain constant.

For the example to follow, the substrate is p-doped and contacted to $V_{SS}$ and the well is n-doped and contacted to $V_{DD}$. Also, the contact resistance for the substrate is considered small. If the single event current draw due to a well/substrate charge collection approaches its limit, then the potential near the charge collection will be close to $V_{SS}$. Any p+-doped sources in the n-well near this charge collection region will observe a forward bias and a resistance. This forward-biased diode will supply some of

the needed single event current through the resistor. But, the diode will also inject holes into the n-doped well [Wo93]. This increase in carriers can reduce the resistance as seen by the source. In essence, the p+-doped sources are seen as an almost limitless source of single event current, since they can modulate the resistance to the well/substrate charge collection area. As the single event current needs increase with increased charge collection, the forward-biased sources become the dominant suppliers of current and significant sources of carriers. In fact, the amount of carriers near the source of a transistor can become much higher than what could possibly diffuse to that location. Therefore, this mechanism does not require and may not receive any direct charge collection.

# CHAPTER IV

# WELL-COLLAPSE SOURCE-INJECTION

## Well/Substrate P-N Junction Charge Collection

In modern complementary metal-oxide-semiconductor (CMOS) circuits, there are many p-n junctions for the collection of single event current. To fabricate an n-channel metal-oxide-semiconductor field effect transistor (nMOSFET), n+-doped source/drain regions are placed on a p-doped body region. The source/body and drain/body junctions each form a p-n junction. To fabricate a p-channel metal-oxide-semiconductor field effect transistor (pMOSFET), p+-doped source/drain regions are placed on an n-doped body region, once again creating two p-n junctions: source/body and drain/body. But, the overall circuit needs to have two types of bodies for the formation of both transistors. To provide both types of bodies, the manufacturing process begins with one type of doped substrate, e.g., p-type to form the nMOSFETs, and then add n-doped wells where the pMOSFETs are located. The n-doped well and p-doped substrate boundaries then form very large p-n junctions for charge collection. An example of the amount of area that n-wells occupy in a sample design is given in Figure 11. Note that this is a very substantial portion of the design, and is much more area than the source/body or drain/body junctions.

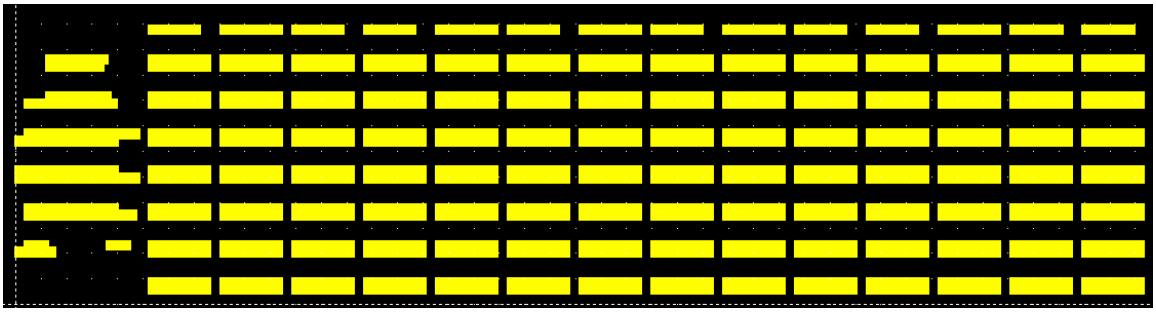


Figure 11. Sample CMOS circuit top view showing location of n-well implant in yellow. Each n-well contains ~24 pMOSFETs. The circuit is built in 90-nm CMOS technology and the dimensions of the layout are ~225 μm x ~65 μm.

Not only do well/substrate p-n junctions consume a lot of surface area when examining a typical CMOS design in the layout view, they also have a large volume with respect to drain or source volumes. Figure 12 shows a sample 3-D drawing of two n-wells in a p-substrate. N-wells are typically long in one dimension of the layout, though it is possible to have shorter wells. The n-well has a couple of important dimensions, height (*wh*) and width (*ww*). In general, the top of the well is the STI and the bottom is the depth of the n-well implant. In a 90-nm process, *wh* is approximately 700 nm. The well length is based on the need to encompass all pMOSFETs and/or well contacts. In 90-nm SRAM, *ww* is approximately 900 nm, and in 65-nm SRAM, *ww* is approximately 500 nm. In standard cell CMOS layouts, the well length is typically greater than the well width, on the order of two to four times larger. The other dimension provided on Figure 12 is the well spacing, *ws*. This dimension describes how close the wells are to each other. In SRAMs, *ws* will be about the same as *ww*. However, in standard cell CMOS layouts, *ws* is usually less than *ww*.

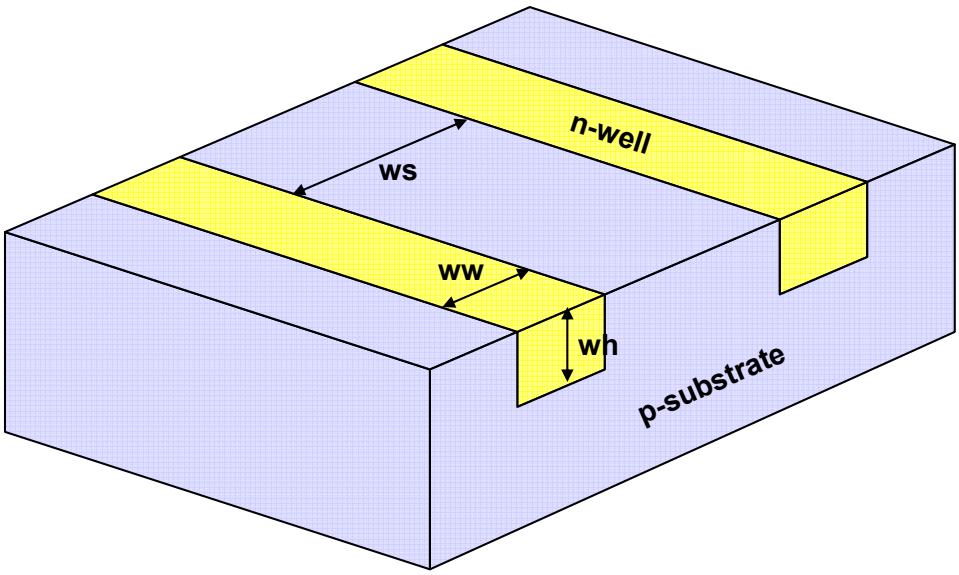



Figure 12. Example of a 3-D drawing of two n-wells in a p-substrate.

Charge collection in a p-n junction depends on the number of carriers generated in the depletion region or nearby, typically within one diffusion length. It also depends on the volume of the depletion region where the charge collection occurs. Based upon the structure of the n-well, it has a large volume inside for the generation of carriers. It also has very large volumes of depletion region within one diffusion length of just about any ion strike through the n-well. The magnitude of charge collection at the well/substrate p-n junctions is typically much higher in the denser layout of SRAMs than in less dense layouts like standard cell, since *ww* and *ws* are relatively small. Electrons generated outside of the well can also collect at the well/substrate p-n junctions. However, only one or two sides of the well/substrate p-n junctions will collect charge via a strike outside of the well. If *ws* is small, it is possible to collect charge on multiple well/substrate junctions due to the diffusion of the electrons. So, in modern microelectronics processes, the

well/substrate p-n junctions have the highest probability of charge collection, and they can contribute to the largest single event currents.

## Supplying Current to the Single Event Charge Collection

The charge collection at the well/substrate p-n junction is viewed as a current sink and not as a supply. Thus, the current has to be supplied from the power and ground connections in the design. There are two ways to supply the current: (1) through the well contacts and (2) through p+-sources. Each method of current supply has a resistance from its respective contact to the strike location in the well/substrate p-n junction.

### Well Resistance

A well from Figure 12 can be viewed as a long rectangular box as drawn in Figure 13. If the two ends are considered the two terminals of the resistor, then the well resistance can simply be calculated from equation 4 and equation 5. The model of the well resistance used in this research is a series of resistors per unit of well length as shown in Figure 13. For example, if the well was doped n-type with $N_D = 7.8\text{x}10^{17}$ cm$^{-3}$ and $\mu_n = 318$ cm$^2$-V/s, then the well resistivity is calculated by equation 4.

$$\rho = \frac{1}{(nq\mu_n + pq\mu_p)}$$

$$\rho = \frac{1}{(7.8x10^{17}\,cm^{-3})(1.6x10^{-19}\,C)(318cm^2 - V - s^{-1})}$$

$$\rho = 0.025\Omega - cm$$

Then, taking *ww* = 900 nm, *wh* = 700 nm, and a unit well length of 1 μm, the resistance per unit length is calculated from equation 5.

$$R = \frac{\rho l}{A}$$

$$R = \frac{(0.025\Omega - cm)(1x10^{-4}\,cm)}{(900x10^{-7}\,cm)(700x10^{-7}\,cm)}$$

$$R \approx 400\Omega\,(per\,unit\,length)$$

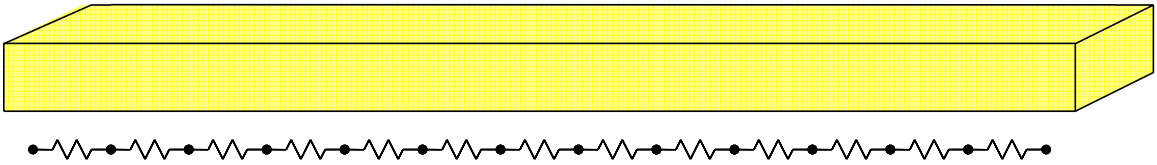


Figure 13. Model of the well resistance.

Well Contacts

The well is contacted to metal by implanting a highly doped region near the surface of the semiconductor, with the same doping type as the well. In the era when local oxidation of silicon (LOCOS) was used to isolate transistors and well/substrate contacts, the well contact implant was virtually at the top of the well (Figure 14). The implant extended down below any isolation oxide, leaving a very low resistive path from the contact to the well. But, in the current era of STI, the top of the well is some distance from the top of the semiconductor, where the transistors are formed. Figure 15 shows a drawing of two well contact semiconductor regions that are surrounded by STI. This structure essentially forms a vertical resistor. The model of this resistor, including the well resistance and the connection to $V_{DD}$, is also shown in Figure 15.

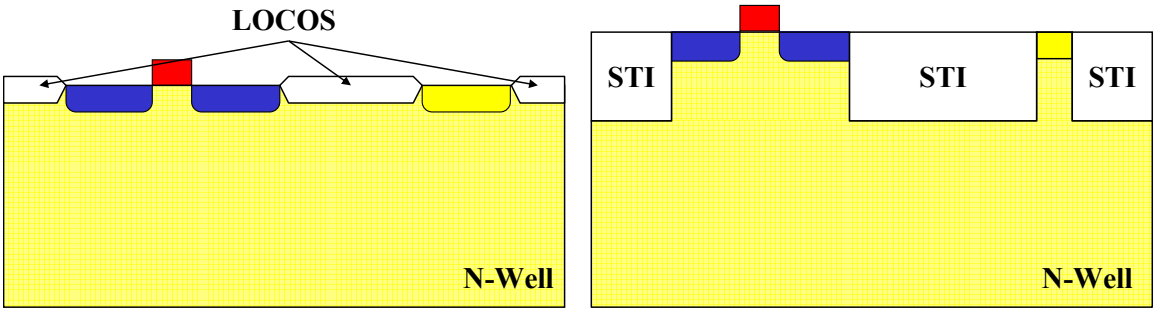



Figure 14. Side view of pMOSFET (gate - red, source/drain – blue) and n+-body contact (yellow) in both LOCOS and STI microelectronics processes.

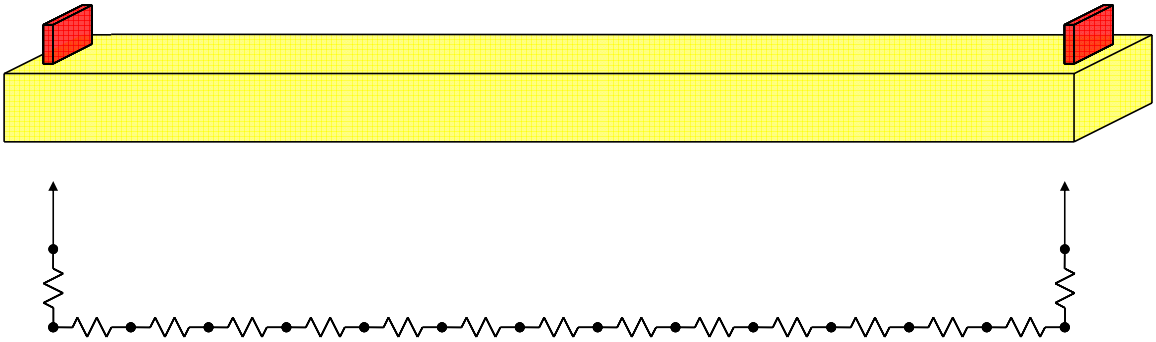


Figure 15. Model of well contacts to $V_{DD}$.

The resistance of each well contact is calculated similarly to the well resistance, except that it is from top to bottom rather than from left to right. It is assumed that the very highly doped implant has very low resistance, so it is not included in the resistance calculation. This is done by subtracting the STI depth from the implant depth. If $N_D$ = 6.6 x $10^{16}$ $cm^{-3}$, $\mu_n$ = 743 $cm^2$-V/s, STI depth = 360 nm, implant depth = 100 nm, and well contact area = 120 nm x 800 nm, then the well contact resistance can be calculated using equation 4 and equation 5.

$$\rho = \frac{1}{(nq\mu_n + pq\mu_p)}$$

$$\rho = \frac{1}{(6.6x10^{17}\,cm^{-3})(1.6x10^{-19}\,C)(743cm^{2} - V - s^{-1})}$$

$$\rho = 0.127\Omega - cm$$

$$R = \frac{\rho l}{A}$$

$$R = \frac{(0.127\Omega - cm)(360x10^{-7}\,cm - 100x10^{-7}\,cm)}{(120x10^{-7}\,cm)(800x10^{-7}\,cm)}$$

$$R = 3.44k\Omega$$

As defined in equation 14, the single event current provided by the well contacts is current-limited. Figure 16 shows the current limits of the well contacts developed using the examples from this section. For the context of the figure, one well contact is located at x = 0 μm (left) and another is located at x = 10 μm (right). Given $V_{DD}$ = 1.2 V, the figure shows the current limit for the well contact on each side and the total current limit provided by both of them. The figure includes some rough approximations, such as the locations of the single event current sinks at the top of the well, rather than at the bottom or along the sides. However, the figure does demonstrate that the resistance of the well contact(s) to the well is the dominant factor.

The resistance associated with well contacts generally increases with scaling. Thus, the ability of a well contact to supply the current for well/substrate p-n junction charge collection decreases with scaling. The change from LOCOS to STI has an obvious impact by adding resistance from the well contact to the well itself. Also, scaling can decrease the length of the resistor by the scaling factor, but the area can decrease by the scaling factor squared (equation 5). So, the resistances are increasing with scaling. Scaling should only further limit the well contacts as a current source. However, the

current produced from a single event is not decreasing, so other sources must be contributing to this response.

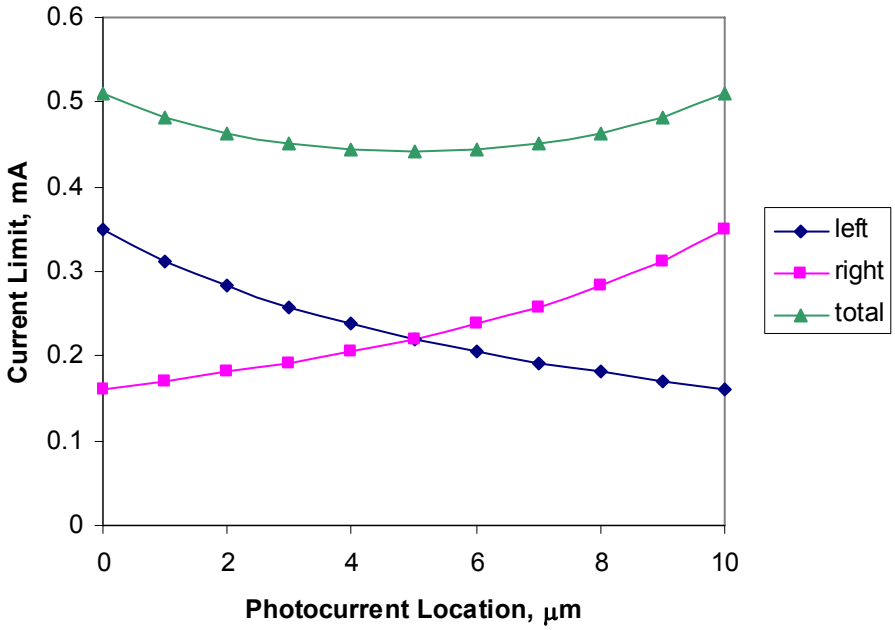



Figure 16. Example of current limiting of well contacts to supply single event current.

MOSFET Sources

Besides the well contacts, the other supplies for the well/substrate single event current are MOSFET sources inside the n-well. If the current drawn from the single event is significant with respect to the limit of the well contacts, then the well potential will have a large current-resistor (IR) drop from the well contact to the well/substrate charge collection region. This could drop the well potential from $V_{DD}$ to near $V_{SS}$. P+-sources in an n-well near the well/substrate charge collection region can then become forward biased. A drawing of the well with some transistor implants is given in Figure 17. This figure shows 12 regions where one p+-source is shared with two p+-drains (though the

actual source/drains are not specified). The layout is indicative of the 90-nm SRAM layout of 12 SRAM cells between the two well contacts. The figure also shows the full model for supplying single event current to the well/substrate charge collection region. In STI, the implants for the source/drains are surrounded by STI, much like the well contacts. Also, the p+ implant is about the same depth, so the resistor in series with the diode in the model is very similar to the well contact resistor except for the area term.

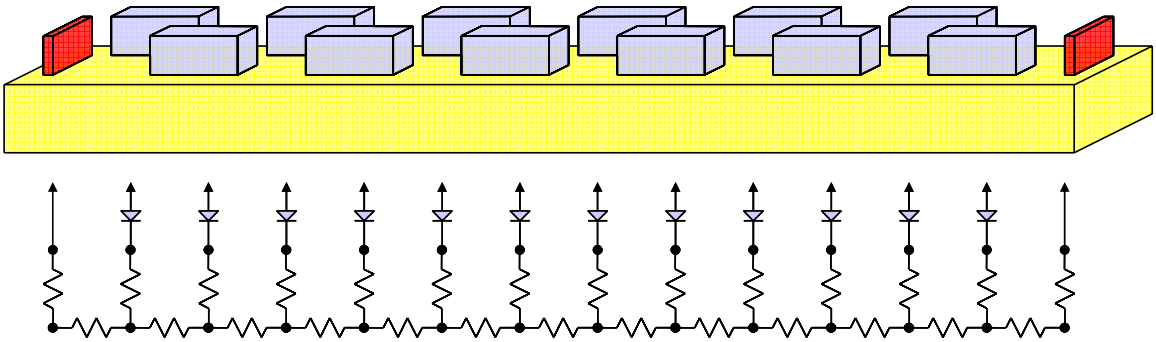


Figure 17. Full model of single event current supply to a well/substrate p-n junction charge collection.

The resistance from the p+-n source/body diode to the well is calculated in the same manner as the well contact resistance. Again, it is assumed that the resistance in the p+ region is insignificant and that the length of the resistor extends from the bottom of the implant to the top of the well. If $\rho$ = 0.027 Ω-cm, STI depth = 360 nm, implant depth = 100 nm, and source/drain area = 200 nm x 920 nm, then the well contact resistance can be calculated.

$$R = \frac{\rho l}{A}$$

$$R = \frac{(0.127\Omega - cm)(360x10^{-7}\,cm - 100x10^{-7}\,cm)}{(200x10^{-7}\,cm)(920x10^{-7}\,cm)}$$

$$R = 1.79k\Omega$$

If the resistance is considered fixed and there is a nominal 0.7 V forward bias drop through the diode, the maximum current that the p+-source can supply is calculated by subtracting the forward bias drop from $V_{DD}$ and dividing by the resistance. This is about 0.28 mA, which is very similar to the amount of current that can be provided from each well contact, but less than the sum of both of the well contacts. However, the resistance in this path is not constant in the forward bias condition, as discussed in subsequent sections.

## Resistivity Modulation

A TCAD simulation is presented to demonstrate the supply of the single event current to a well/substrate p-n junction charge collection. A top view of the transistors simulated is given in Figure 18. There are two pMOSFET transistors in an n-well on p-substrate. The well extends a little more than five μm both to the left and the right where the well contacts are located. The resistance parameters match all the examples calculated in the previous section except for the p+-source diode to well resistance. Note that in this figure, there is only one p+-drain, and not two as in the calculation. The reduction in the one dimension from 920 nm to 680 nm increases the resistance from 1.79 kΩ to 2.43 kΩ. The ion strike is shown with the X and proceeds at an angle of 60 degrees from normal to the surface in the direction shown. The simulated charge deposition was 0.12 pC/μm.

A current versus time plot for the n-well contacts and the two p+-sources is given in Figure 19. It is noted that p+-source 1 is the one on the bottom of Figure 18 nearer the well/substrate charge collection region. The ion strike is initiated at 1 ns in simulation

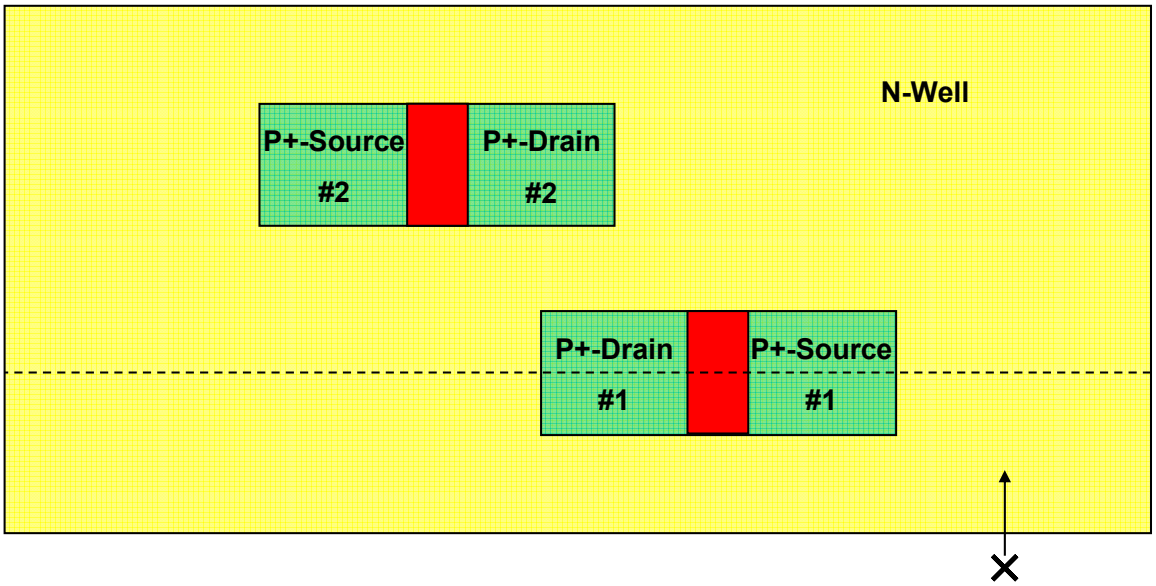



Figure 18. Top view of 3-D TCAD design to demonstrate well/substrate p-n junction single event current supply.

time. This figure clearly demonstrates a current limit on the well contacts of about 0.2 mA. This differs from the 0.44 mA predicted by the resistance calculations. The main reason for the difference is that the resistivity is not constant due to the retrograde well. With respect to the current supplied by the p+-sources, one peaks at 1.4 mA and the other just above 0.6 mA. The predicted maximum is approximately 0.20 mA for a p+-source near the charge collection. It is observed that the p+-source near the charge collection is providing significantly more current than possible given the assumption that the resistance is constant.

The next series of figures show the well potential and the hole density near the p+-source on the bottom of Figure 18, as shown by the dashed cut line. The first two figures show the equilibrium condition where the n-well and p+-sources are at 1.2 V and the substrate and n+-source are at 0 V. Figure 20 shows the potential in the equilibrium condition. This plot is included as a reference for how to read the outputs from the TCAD

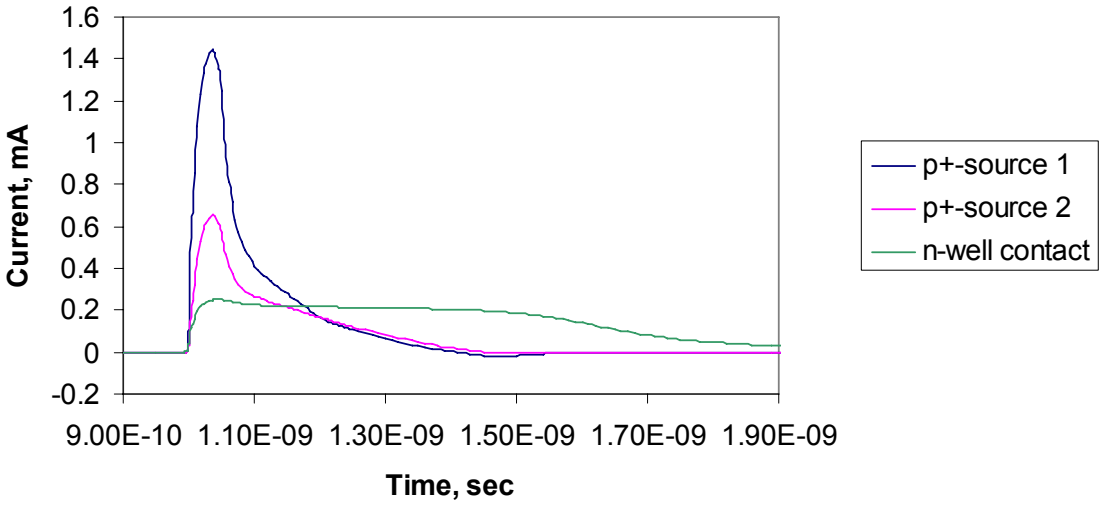



Figure 19. Supply current versus time for sample TCAD simulation on two p+-sources and two n-well contacts.

simulator, since the potential everywhere is exactly 1.2 V. The p+-source/drain regions at the top are shown as $V_{DD}$ plus $\Phi_p$, where $\Phi_p$ is defined by equation 8. The n-well region in the rest of the figure is shown as $V_{DD}$ plus $\Phi_n$ (defined by equation 7). Figure 21 shows the equilibrium hole density. Figure 22 and Figure 23 capture the device state 5 ps following the ion strike, and show the potential and the hole density, respectively. The potential demonstrates that the p+-n source/body diode has become forward biased, since it is difficult to distinguish much color difference in the figure. In comparing Figure 22 to Figure 20, it is observed that the p+-source remains at 1.2 V. Since the color is the same in the n-region below the source, it means that $\Phi_n$ less $\Phi_p$ is essentially dropped across the diode. This is the same as saying the diode has a forward bias of approximately $\Phi_i$ per equation 9. In Figure 23, the hole density mainly shows the initial diffusion of carriers from the ion strike.

The potential and the hole density are also examined at the height of the current draw. The potential, shown in Figure 24, still shows a forward bias of $\Phi_i$ on the source/body diode, as would be expected. Figure 25 shows that the hole density is highest at the edge of the diode. This is expected, as a forward bias diode injects minority carriers as seen in equations 12 and 13. But, the most interesting item is that the density of the minority carriers is higher than originally generated by the single event. The carrier densities were found to be $n = 1.85\text{x}10^{18}$ cm$^{-3}$ and $p = 1.65\text{x}10^{18}$ cm$^{-3}$ at a point sampled near the source in the n-well. Both of these densities are more than an order of magnitude higher than the doping level. Using these carrier densities along with mobilities of $\mu_n$ = 603 cm$^2$-V/s and $\mu_p$ = 273 cm$^2$-V/s, the resistance from the source to the well can be recalculated.

$$\rho = \frac{1}{(nq\mu_n + pq\mu_p)}$$

$$\rho = \frac{1}{(1.85x10^{18})(1.6x10^{-19})(603) + (1.65x10^{18})(1.6x10^{-19})(273)}$$

$$\rho = 0.004\Omega - cm$$

$$R = \frac{(0.004\Omega - cm)(360x10^{-7}\,cm - 100x10^{-7}\,cm)}{(120x10^{-7}\,cm)(800x10^{-7}\,cm)}$$

$$R = 77\Omega$$

This value of resistance is significantly different from the equilibrium case. So, as a result of the forward bias, the source injects minority carriers into the well, which in turn, modulates its resistivity by a significant amount. This allows the p+-sources in the well to supply much more single event current than the well contacts, since they can overcome the implant-to-well resistance.

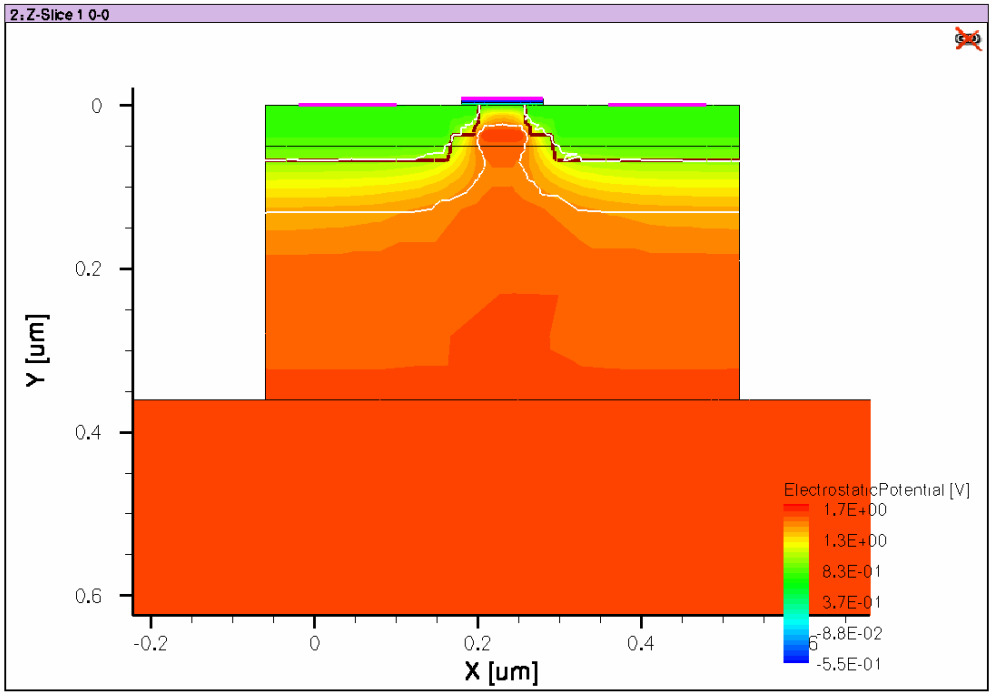



Figure 20. Plot of the equilibrium potential of the TCAD simulation along the cut line shown in Figure 18.

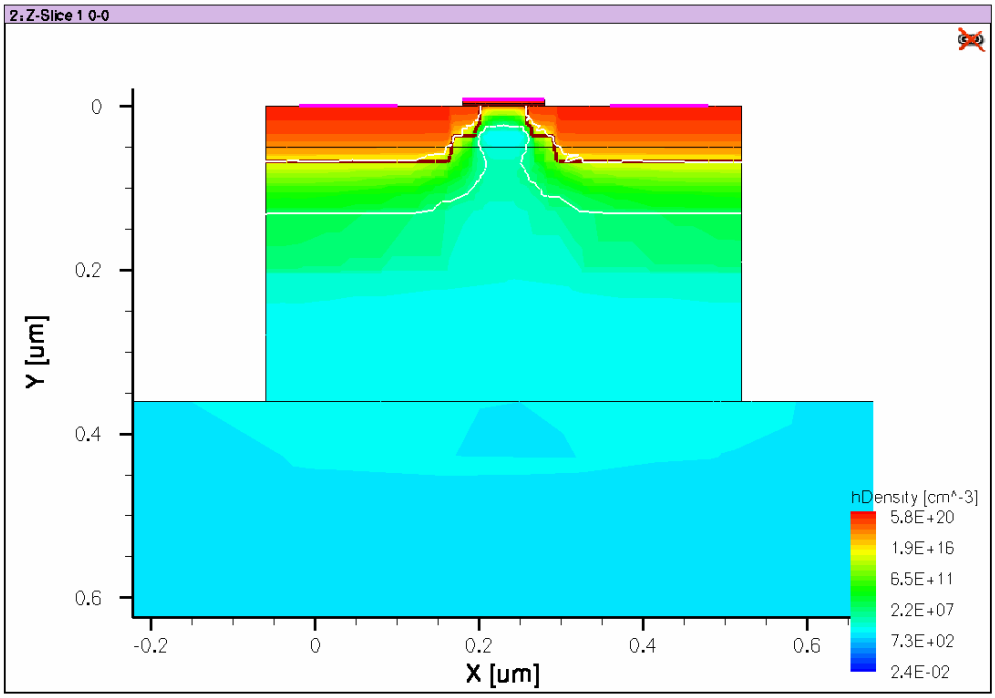



Figure 21. Plot of the hole density of the TCAD simulation along the cut line shown in Figure 18.

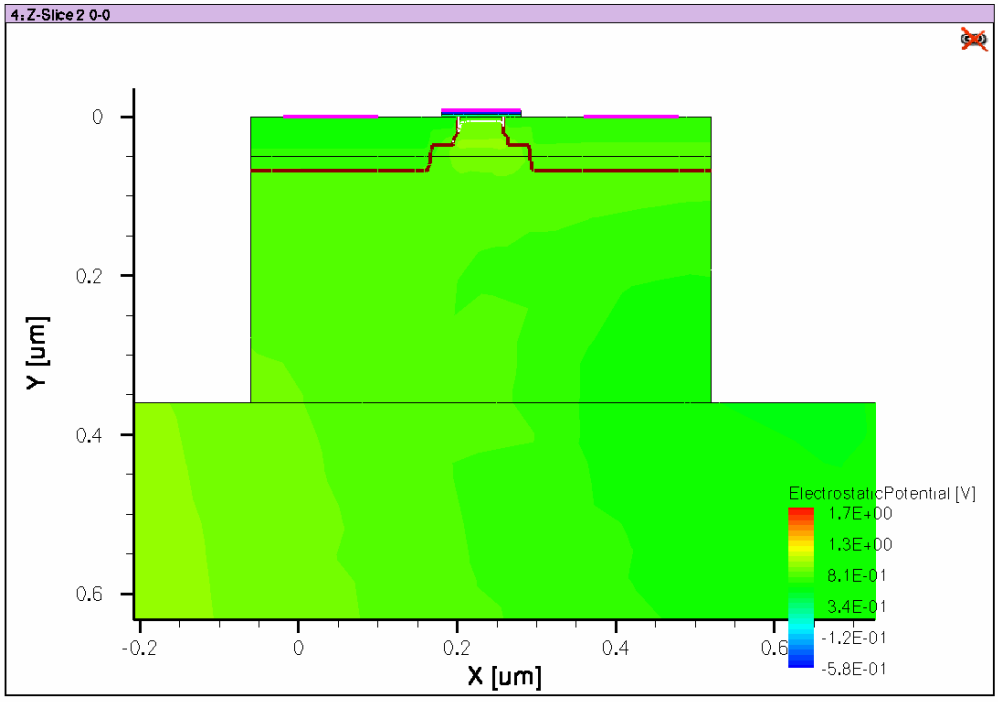



Figure 22. Plot of the potential just after the ion strike.

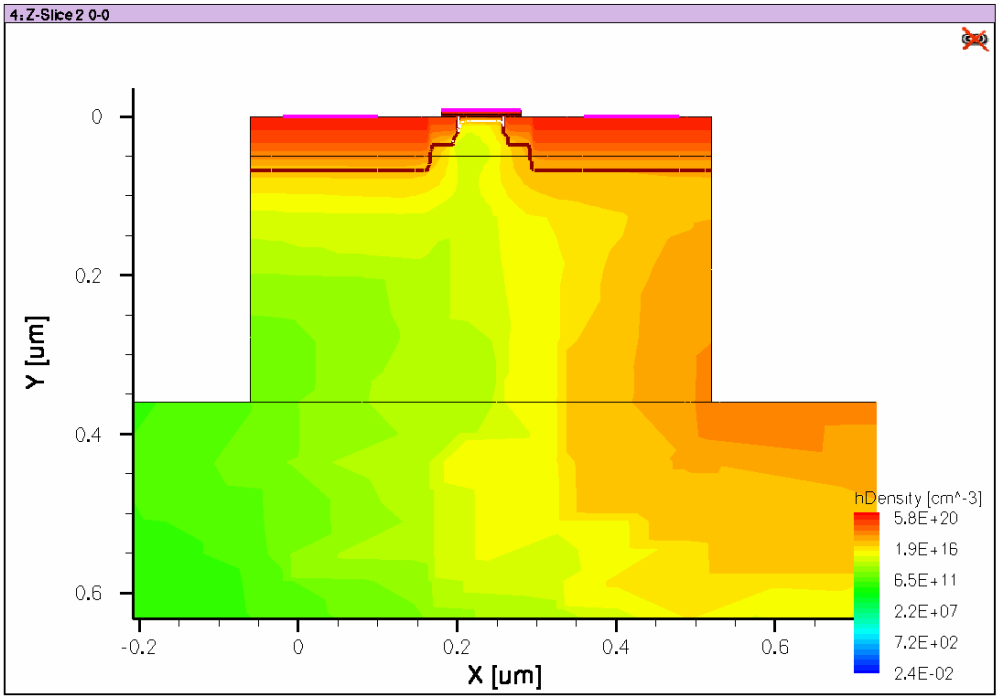



Figure 23. Plot of the hole density just after the ion strike.

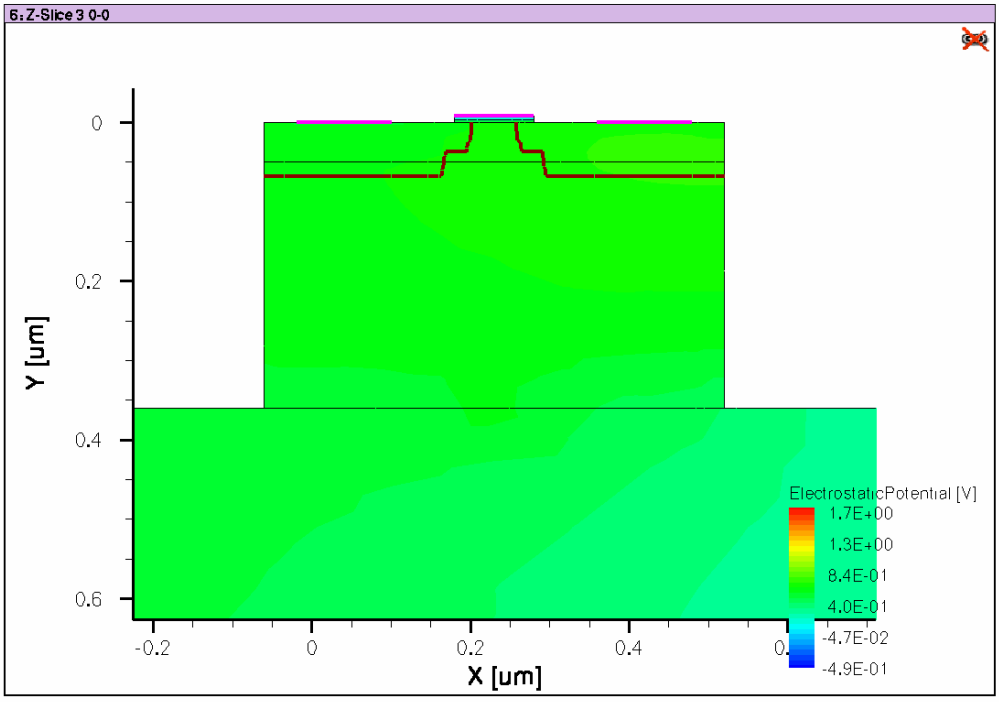



Figure 24. Plot of the potential at the height of the single event current draw.

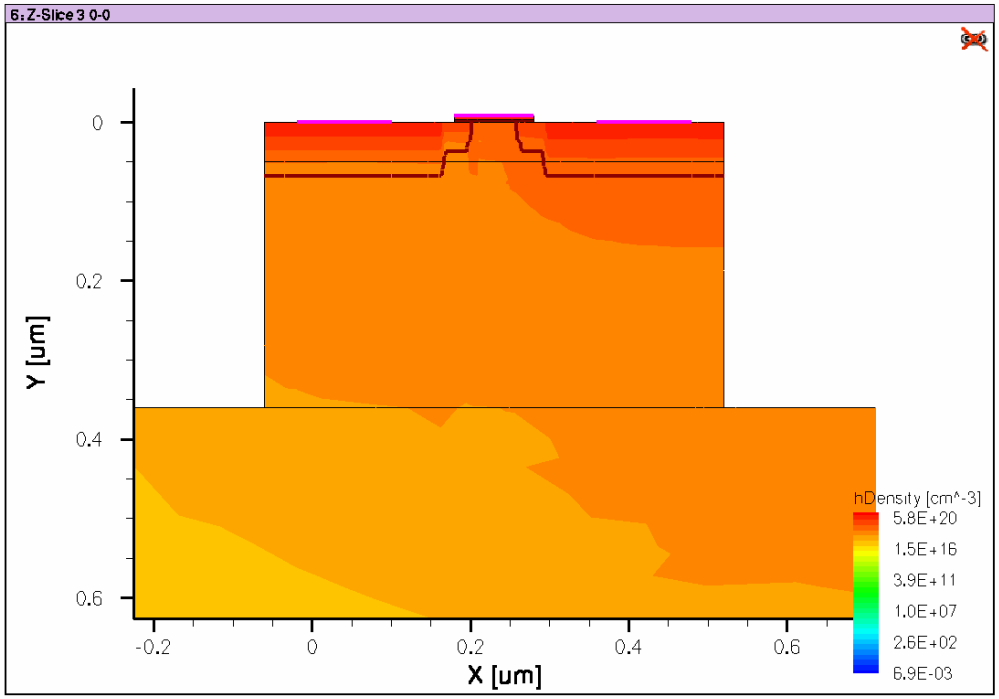



Figure 25. Plot of the hole density at the height of the single event current draw.

## MOSFET Response

When the source/body p-n junctions become forward biased due to well/substrate charge collection, the next question is the response of the MOSFET in this condition. The answer is that the transistor ceases to operate as a FET and reverts to acting as a lateral bipolar junction transistor (BJT). Standard MOSFET operation does not have either the drain/body or source/body diodes in forward bias. These diodes either have no applied voltage or have a reverse bias applied. However, if the source/body p-n junction is forward biased while the drain/body p-n junction has no applied voltage or a reverse bias is applied, then the voltage describes a bipolar forward active operation.

The lateral p-n-p BJT for a pMOSFET in an n-well is shown in Figure 26. The source becomes the emitter, the drain becomes the collector, and the well contact becomes the base. The physical base of the device is actually the body of the MOSFET between the source and drain. As the source/body or emitter/base diode increases in forward bias, the BJT will enter the saturation operating point. As a result, the emitter/collector potential, $V_{EC}$, will become $V_{EC,sat}$, which is typically on the order of 0.1-0.2 mV.

## Comparison to Other Radiation Effect Responses

The well-collapse source-injection charge collection mechanism is similar to a couple of radiation effects responses. It is similar to the parasitic bipolar enhancement (PBE) single event charge collection response. The ion strike in both cases causes the source/body p-n junction diode to enter a forward bias condition [Wo93]. However, there are a few distinctions. First, the charge collection responsible for the initiation of PBE is

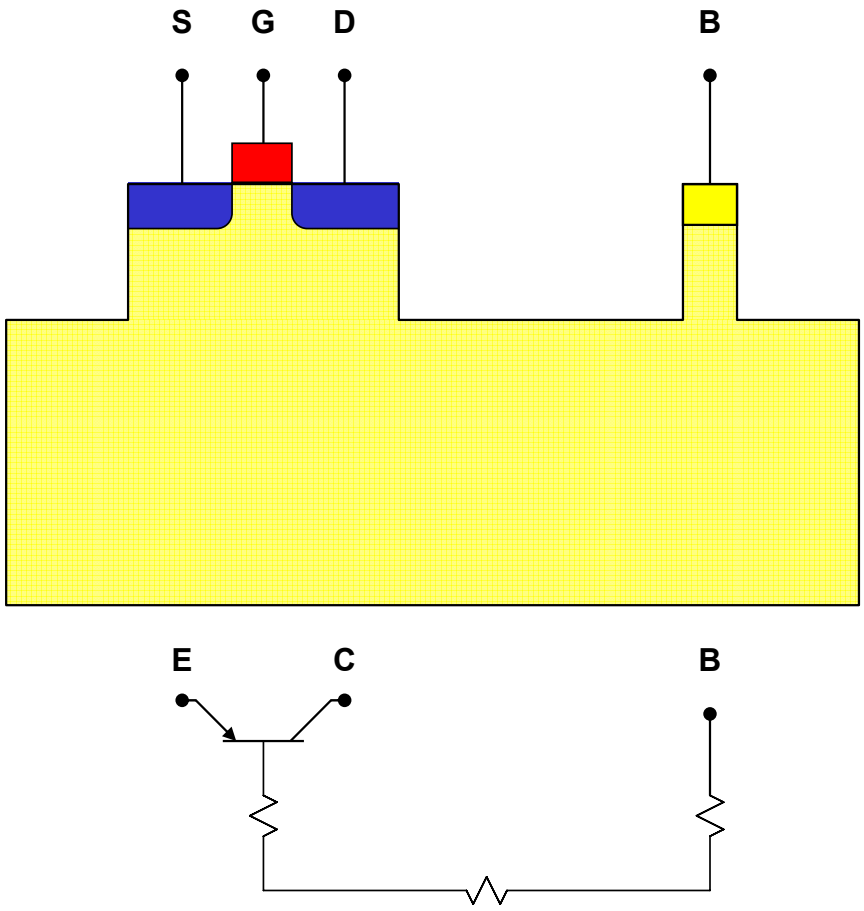



Figure 26. Sideview of pMOSFET layout in n-well with STI and BJT model.

the drain/body p-n junction of the MOSFET. This single event current modulates the base potential, thereby creating the forward bias in the source/body. In the well-collapse source-injection mechanism, the well/substrate p-n junction is the location of the charge collection. This single event current draw then displaces the body potential of the MOSFET. The second distinction is that PBE, by definition, can only affect MOSFETs in the OFF state. The well-collapse source-injection can and will be present on all MOSFETs where the source enters a forward bias. The well/substrate p-n junction is always in reverse bias, so this mechanism is possible under all conditions.

The other radiation effect response to be compared is dose-rate response. Messenger examined the conductivity modulation in diffused resistors under very high dose rate levels [Me79]. This work derived a dose-rate dependence within the resistor based on the single event current generation of excess carriers that alter the material conductivity. This work looked at conductivity modulation when the excess carrier densities were at or above the starting doping density. The resistor value was shown to be reduced at higher dose rates, by up to a factor of five. This trend would have continued as the dose rate increased. So, this is similar in concept to the resistivity modulation presented in this chapter, with the only difference being the source of the excess carriers. Massengill then examined the single event current generation in an SRAM cell as the basis for rail span collapse [Ma84]. In this analysis, it was observed that the well/substrate p-n junction was the largest source of single event current and contributed the most of the sag of the local $V_{DD}$ and $V_{SS}$ rails.

## Single Event Modeling Impact

There are a couple of impacts of the well-collapse source-injection mechanism with respect to single event modeling and simulation. The first relates to TCAD modeling. Assume that a single event charge track results in: (1) a current limiting condition on a well or substrate contact, and/or (2) the forward biasing of a source in a well. Then, the TCAD model should include all relevant current sources for the single event current. In the example presented in this chapter, two pMOSFETs were modeled in a large n-well. Since the well contact became current limited and both the pMOSFETs were forward biased, it is likely that excluding the modeling of the other pMOSFET

sources in the well leads to an inaccurate response. It is also noted that the path from the pMOSFET source to the well is resistive and affects the current supply to the charge collection. This means that the resistor geometry must represent the actual design as well. In the example presented in this chapter, the resistance was about 50% more than the actual case due to one source being shared with two drains. So, it is important to model all the sources of current for the well/substrate charge collection, and it is also important to accurately model the resistor from the implant depth to the top of the well.

The second impact of the well-collapse source-injection mechanism with respect to modeling is related to compact modeling. The model provided in Figure 17 is a model that could be made to fit a compact model. The main challenges with adapting that figure to a compact model are: (1) obtaining a relationship for the high injection case of the diode (i.e., providing the voltage drop and the carrier density) and (2) obtaining a relationship for the resistor with excess carriers. Messenger had already developed an equation for the modulation of the conductivity with respect to excess carriers, which likely can be modified for use in a compact model [Me79]. There are also closed-form equations for a diode at high injection that can be adapted. This chapter has shown a relationship between the magnitude of the forward bias current and the MOSFET response, so it is likely that a compact model could be developed for this mechanism.

# CHAPTER V

# STATIC RANDOM ACCESS MEMORY CELL

SRAM is one of two main types of volatile memory, the other type being dynamic random access memory (DRAM). SRAM typically is faster in operation, in terms of write and read speeds. DRAM, on the other hand, typically is the more dense memory, so single DRAM microcircuits contain more memory than those of SRAM in the same technology. In processing systems, SRAM is typically used for memory that is closest to the processor because it is accessed more frequently. So, SRAM is used for the cache memory on processing microcircuits. DRAM is then used farther away from the processor, where more memory is needed, but it is not accessed as often.

The other major characteristic of SRAM is that the memory should hold its state as long as it is powered. This is unlike DRAM, where the contents of the memory have to be refreshed from time to time.

## Schematic Diagram and Electrical Characteristics

A schematic diagram of a basic SRAM cell is shown in Figure 27. This cell consists of six MOSFETs, two pMOSFETs, and four nMOSFETs. The four internal transistors (MN0, MN1, MP0, and MP1) are used to hold the state of the SRAM. The other two (MN2, MN3) are access pass-gate transistors that are used to write and read the contents of the cell. MOSFETs MN0 and MP0 form one inverter and MOSFETs MN1 and MP1 form another. These two inverters are then cross coupled so that the held state is

reinforced by feedback; the memory cell can hold the state until it is overwritten or powered down. In the diagram, WL stands for word line and BL stands for bit line.

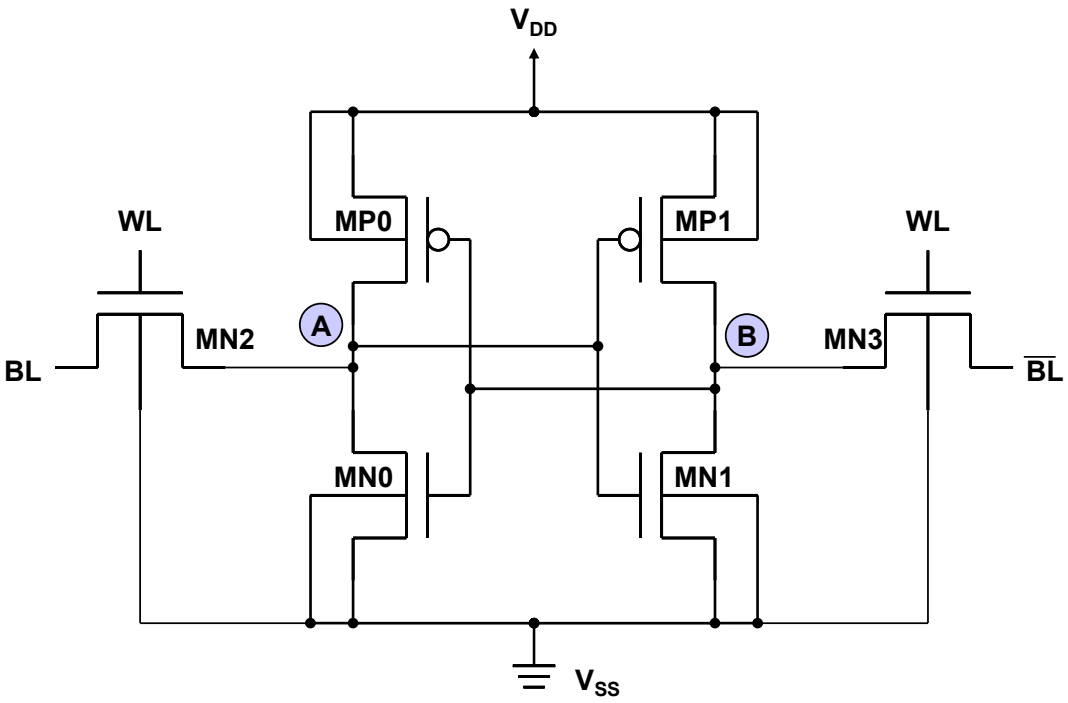



Figure 27. SRAM cell schematic diagram.

The cross-coupled inverter circuit has two stable states, one with node A being logic high and the other with node B being logic high. Note that in those two stable states, each node is the opposite of the other. If WL is logic low, the SRAM is not being accessed and is intended to hold its current state. When WL is logic high, the SRAM is connected to BL and its complement, $\overline{BL}$. In general, the bit lines are highly capacitive, so if BL and $\overline{BL}$ are at opposite logic values, that state will be written into the cell, overcoming its previous state. On the other hand, if BL and $\overline{BL}$ are at equal voltages, the SRAM cell will pull one bit line up slightly and pull one bit line down slightly. This

difference is then fed to a sense amplifier to read the given state of the cell. For most of the time, WL is low, and the cell is in a static hold mode, so that is the state of most concern for radiation effects.

The cross-coupled inverters also potentially have a meta-stable state. Consider an ideal cell where MN0 matches MN1, MP0 matches MP1, and MN2 matches MN3. During the power-up sequence, the SRAM cell nodes A and B will rise to some midpoint between the voltage at $V_{DD}$ and ground, but they will be identical. At some point, all the transistors will be ON, and a high current condition will exist in the SRAM cell. However, almost all actual SRAM cells will have a built-in preference for a power-up state and will enter it. Even if a cell is balanced and becomes meta-stable, this is not a long-lived state. A noise difference on nodes A versus B will drive the cell into one stable state or the other. While meta-stability does not factor into radiation effects, this condition does introduce the concept of SRAM cell imbalance.

It is noted here that there are some SRAM design variations beyond what is shown in Figure 27, many of them related to radiation effects mitigation. The first design variation is a change in the access pass-gate transistors from nMOSFET to pMOSFET. The nMOSFET access transistors are typically used since they provide greater drive at the minimum size than the pMOSFET alternative. If speed is not a driving factor in the SRAM cell design, then this alternative is fine. Also, with strain in the channel making pMOSFET drive strength on par with nMOSFET drive strength, the design choice of access transistors may only be by preference. Other design variations will add passive devices or additional transistors to mitigate the radiation effects. These types of

alternative designs will not be studied in this research, though the findings could be applied [Ro88, Li92, Ca96].

## Layout

There are a couple of different priorities in the layout of a SRAM cell. In a strict commercial sense, the primary driver for the layout is cell size. The smaller the cell size, the higher the density of memory that can be placed in a microcircuit. There is some consideration placed into the specific layout of the cell in terms of length and width, since metals lines containing $V_{DD}$, $V_{SS}$, WL, BL, and $\overline{BL}$ must be routed to each cell. Some of these are shared with adjacent cells, but there is still some restriction at the metal routing level. As a side note, the SRAM memory array layout is very regular, so typical design rules for metal spacings do not completely apply, and they can be relaxed for a denser cell layout.

The basic SRAM layout that was studied in this research is shown in Figure 28. This figure shows the node names on all the gates, drains, and sources of all the MOSFETs. This layout is based on the schematic diagram presented in Figure 27. The two nMOSFETs drawn above the n-well are MN0 and MN2 from left to right. In the n-well, pMOSFET MP0 is in the upper left and pMOSFET MP1 is in the bottom right. Finally, the two transistors on the bottom at MN4 and MN1 from left to right. A dashed box is drawn around the cell itself to provide a view of the SRAM layout that is duplicated in the array. The $V_{DD}$, $V_{SS}$, BL and $\overline{BL}$ connections are shared with adjacent cells to the left and right, so only half of the diffusion counts for the building block size.

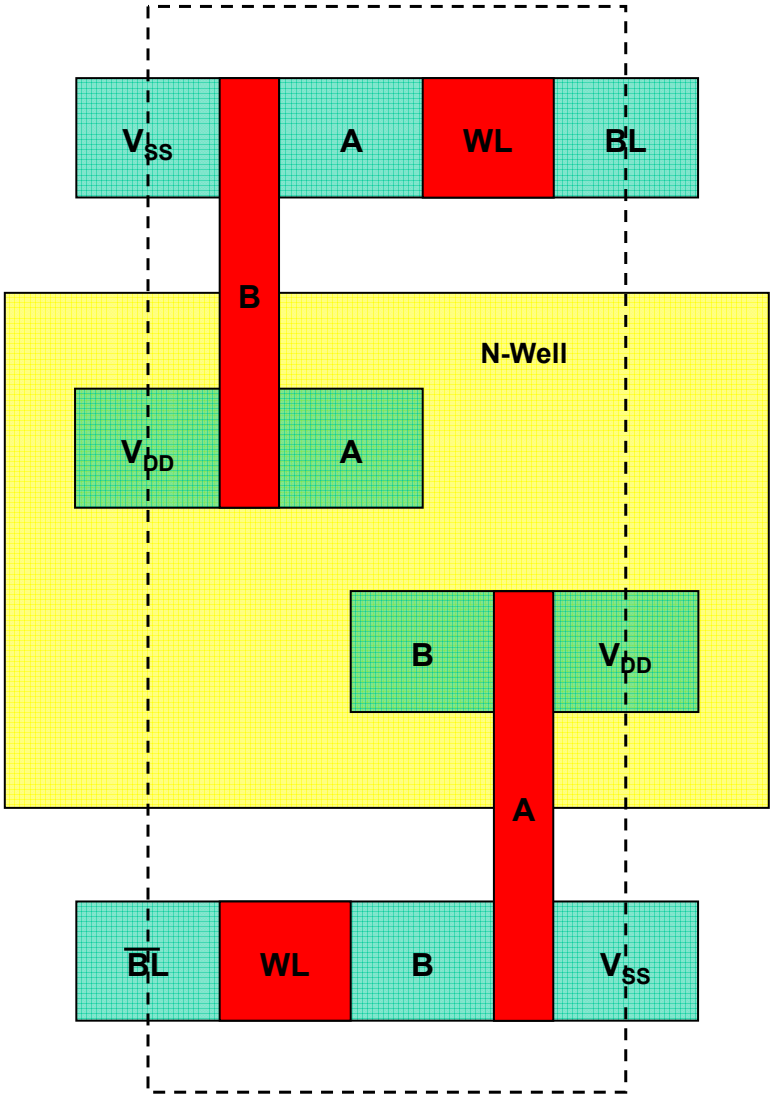



Figure 28. Example of a SRAM cell layout.

In the layout presented in Figure 28, the two pMOSFETs share the n-well, and the two sets of nMOSFETs are on opposite sides of the well. There are many potential design variations to the basic cell layout that can be made. In older technologies, designers would lay the transistors out in both directions to obtain a better density, making use of angling the polysilicon routing (shown in red). In the microelectronics processing generations presented in this document, the design rules prohibit this type of design.

Also, newly formed design rules force the orientation of transistors in one direction and do not allow them in both. So, this design is fairly indicative of most designs at these processing nodes. One potential design variation is to place all the nMOSFETs on the same side of the well. Another would place all the nMOSFETs between two n-wells and have one pMOSFET on top and one on bottom, as in the inverse of the layout shown in Figure 28. If pMOSFETs are ever going to be considered for the access transistors, this is the type of layout that might be considered.

## Single Event Upset Mechanisms

### Historical Basis

The study and analysis of SRAM SEU has been ongoing since the late 1970s [Ko79, Si79]. The schematic diagram for the SRAM cell is redrawn in Figure 29 with just the two cross coupled inverters. Diehl et al. identified strikes to the OFF nMOSFET drain and OFF pMOSFET drain as being the underlying events responsible for SRAM SEU and used circuit modeling to demonstrate the mechanism [Di82]. The schematic diagram in Figure 29 shows the NHIT and PHIT locations for the SRAM state when node A is logically high. A current source is used to model the single event at an OFF drain as shown in the figure. It was noted in this work that there was a difference in the amount of charge it took to upset the cell in either the NHIT or PHIT single event.

Dodd et al. expanded upon this basic theory of SRAM SEU mechanisms and described the modes of upset in terms of the underlying charge collection mechanisms. Figure 30 shows four different configuration for ion strikes that collect at one node; two

of the strikes are to ON transistor drains and the other two are to OFF transistor drains. In each case the source and direction of charge collection current are noted. In general, strikes to OFF transistor drains can cause upsets, and strikes to ON transistor drains will not cause upset. However, there was an ion shunt mechanism for a strike to an ON transistor in a well that could cause an upset (Figure 30d) [Do96].

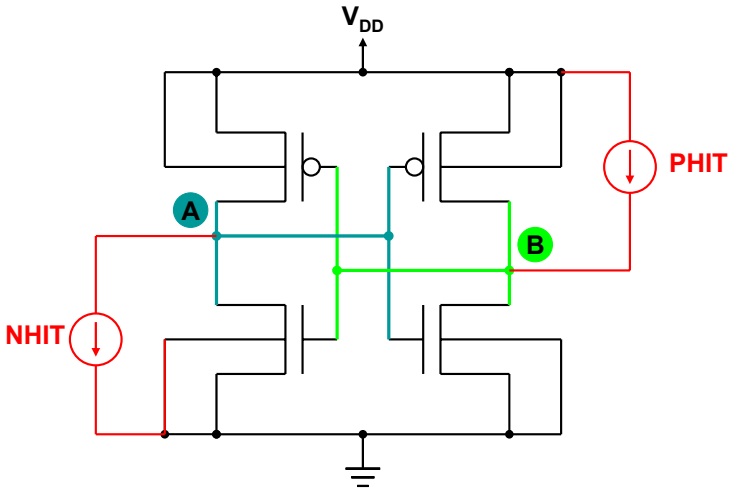



Figure 29. PHIT and NHIT SRAM upset mechanisms (after [Di82]).

Research Findings

This research extends the basic understanding of SRAM SEU with the well-collapse source-injection mechanism. At low charge depositions, the direct charge collection mechanisms dominate the conditions for upset on the cell. If the SRAM cell is struck in an OFF drain, drift and diffusion of the excess carriers will collect on the node, creating a single event current, and possibly inducing upset in the cell. If the SRAM cell is struck somewhere near an OFF drain, the minority carriers can diffuse to the node, collect, and create a single event current that induces upset in the cell. As the charge track

moves farther away from the OFF drain, it requires more charge deposition to induce an upset.

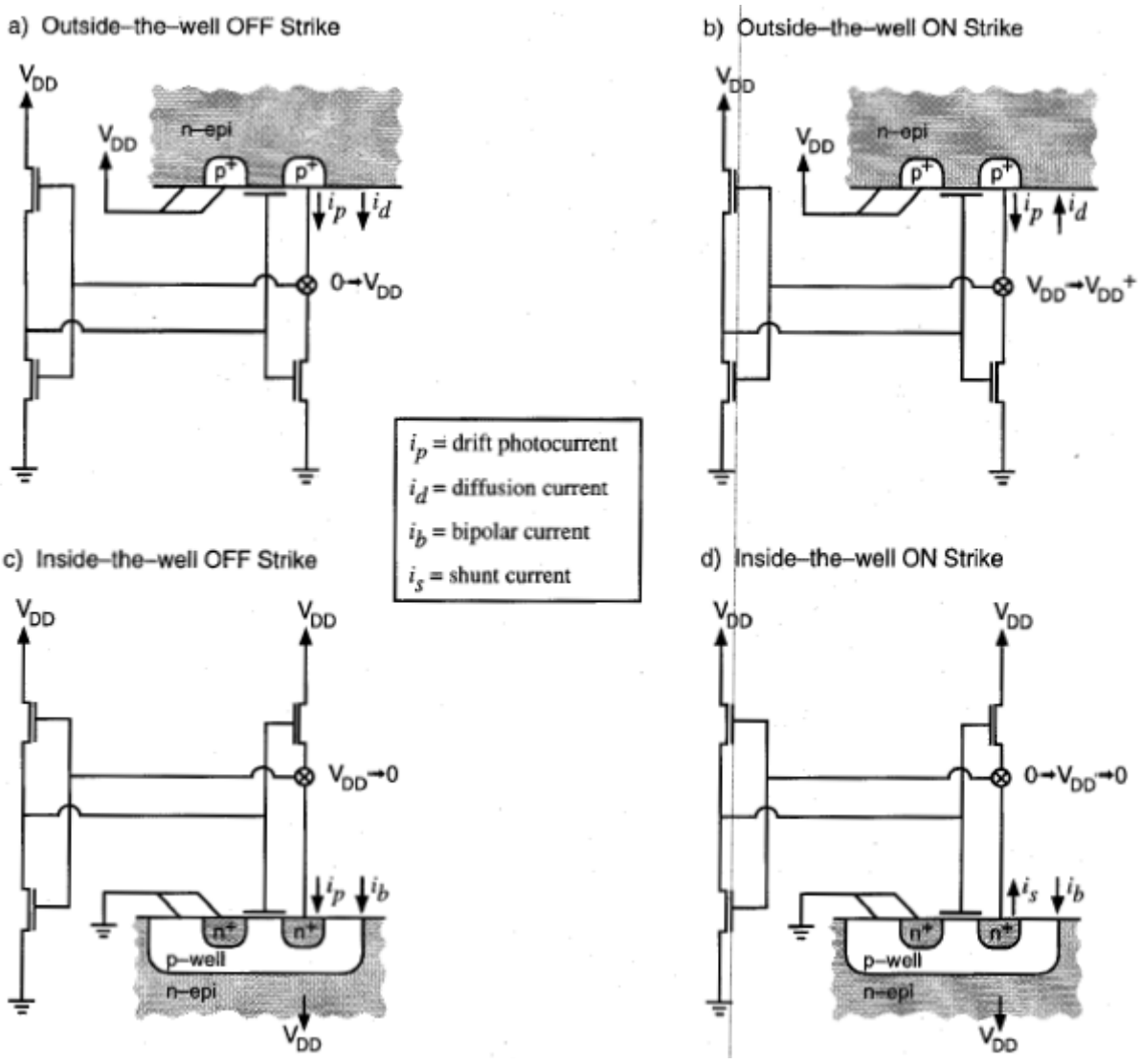



Figure 30. SRAM SEU mechanisms based upon charge collection at single node (after [Do96]).

At some point, the charge deposition becomes enough to induce the well-collapse source-injection mechanism. This can occur for any ion strike, inside or outside the well.

For this mechanism, the charge collection at all the transistors becomes important. To illustrate this transition, consider an ion strike in the center of the SRAM cell, normal to the surface, as shown in Figure 31. This particular TCAD simulation includes a single SRAM cell and two well contacts 5 μm on either side of the cell. At a charge deposition of 0.05 pC/μm (LET is approximately 5 MeV-cm$^2$/mg), the charge collection exhibits standard characteristics of direct collection via diffusion, as demonstrated in Figures 31 through 33. Figure 32 presents the currents that supply the charge collection. It is noted that both of the sources are forward biased, and the n-well contacts are current limited. However, this is all for a very short period of time (20-30 ps). Figure 33 shows the pMOSFET drain currents for the same strike. A negative drain current on MP0 shows charge collection due to diffusion and/or well-collapse source-injection, while the positive drain current on MP1 shows charge collection only due to diffusion. Well-collapse source-injection only has a negative current component. Diffusion charge collection at the ON drain, where there is a depletion region but no applied voltage, results in a reverse current due to a gradient of majority carriers in the source. The voltage plots of the two internal circuit nodes are given in Figure 34, showing that this particular charge deposition at this location does not induce upset or even come close to doing so.

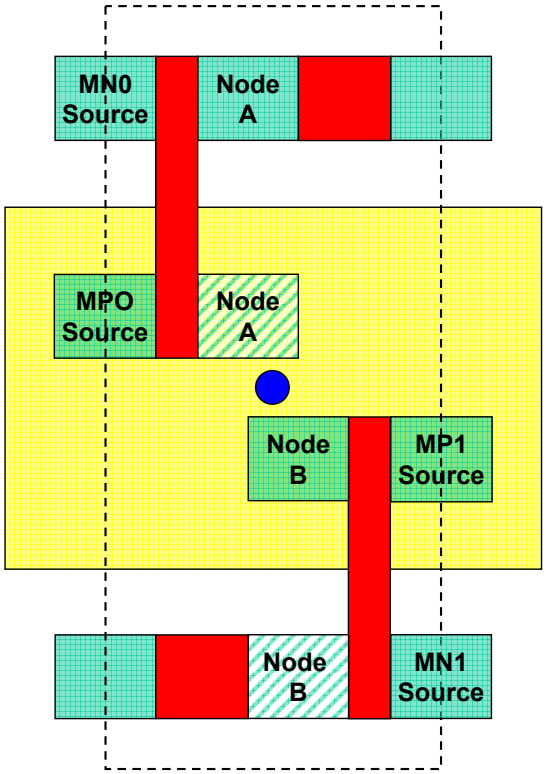



Figure 31. SRAM cell layout showing center ion strike location in blue.

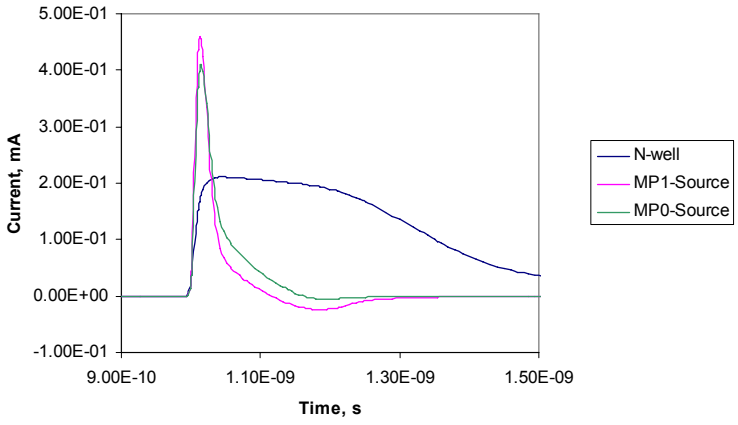



Figure 32. Single event current supply for center ion strike, 0.05 pC/μm.

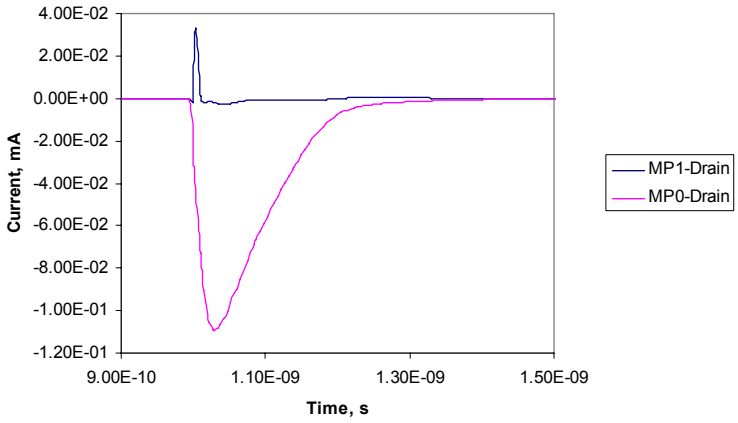



Figure 33. pMOSFET drain currents for center ion strike, 0.05 pC/μm.

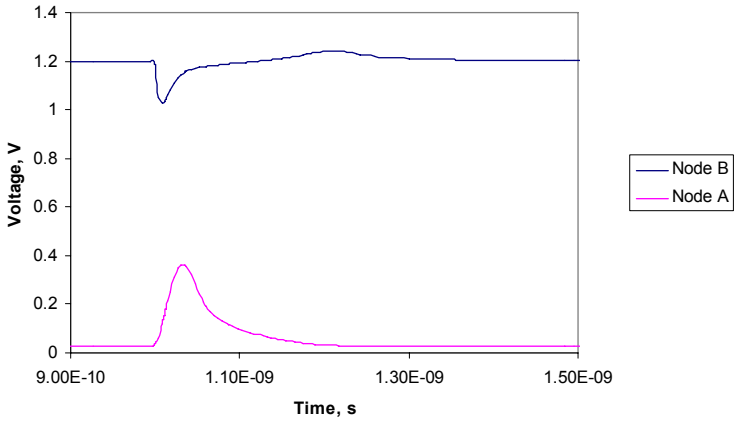



Figure 34. SRAM node voltages for center ion strike, 0.05 pC/μm.

Increasing the charge deposition from 0.05 pC/μm to 0.10 pC/μm (LET is approximately 10 MeV-cm$^2$/mg) changes the dominant mechanism from direct charge collection to well-collapse source-injection. The single event supply currents are shown in Figure 35. In this case, the p+-sources are in forward bias for much longer times and recover much more slowly. The large current drive of the sources lasts for about 80 ps, though the forward bias condition lasts for 200 ps. The pMOSFET drain currents are

given in Figure 36. The ON drain MP0 shows an initial positive current, and then reverts to a negative current, indicative of the well-collapse source-injection. This particular current also returns to zero at the 200 ps timeframe, again giving evidence to the length of time the source is in forward bias. The node voltages are plotted in Figure 37. This figure demonstrates the impact of well-collapse source-injection on the SRAM cell. Basically, both of the pMOSFET sources become forward biased, and the drain voltages follow as in the bipolar saturation condition. Both of the nMOSFETs turn ON and match the respective drain currents. This figure also indicates that the SRAM cell recovery begins at 200 ps after the strike, which coincides with the removal of the forward bias condition.

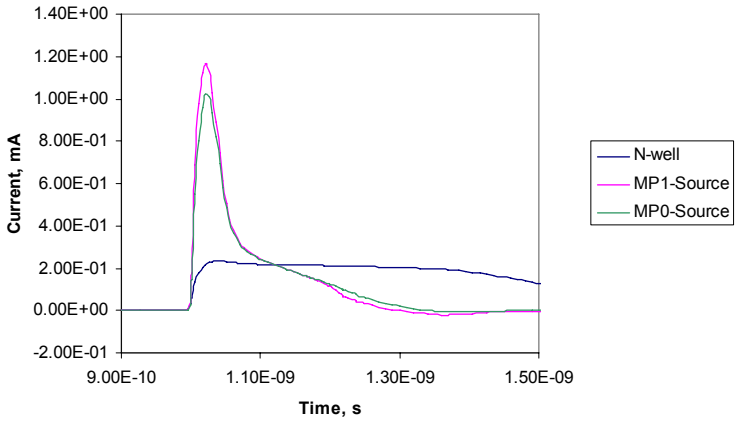



Figure 35. Single event current supply for center ion strike, 0.10 pC/μm.

To summarize the findings of this research with respect to individual SRAM cell SEU, a diagram showing the SRAM cell SEU mechanism as a function of deposited charge is given in Figure 38. At low deposited charge, there is not enough charge

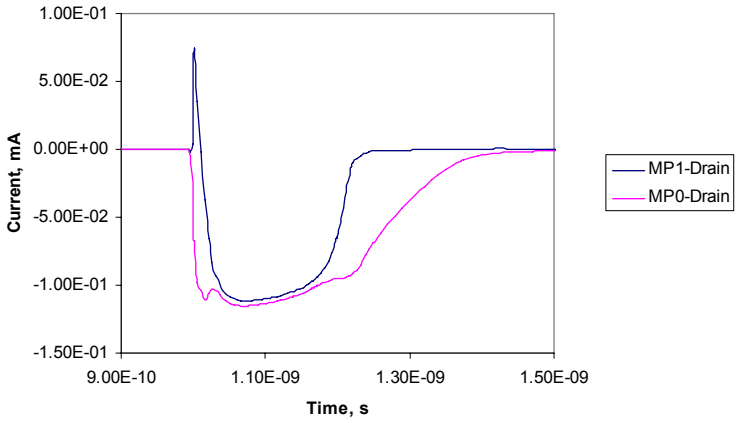



Figure 36. pMOSFET drain currents for center ion strike, 0.10 pC/µm.

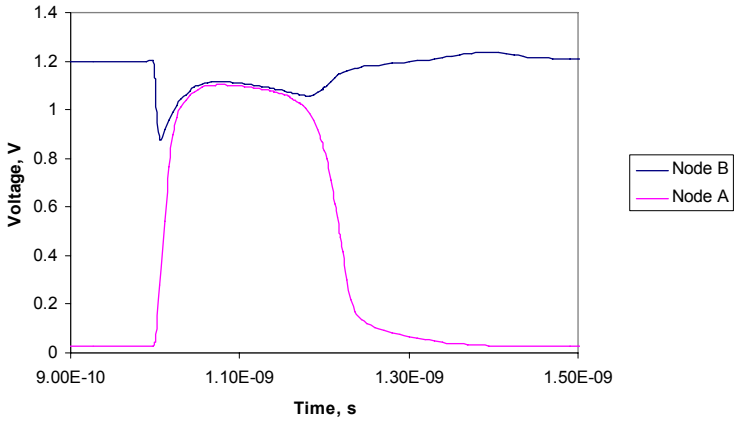



Figure 37. SRAM node voltages for center ion strike, 0.05 pC/µm.

collection to induce an upset on the cell. The charge strike may cause some variation in the node voltages, but the cell will return to the previous state. Onset is defined as the deposited charge that can cause upset through direct charge collection mechanisms. This occurs with an ion strike directly to an OFF drain. As the deposited charge increases, the mode changes from direct charge collection as the dominant mechanism to well-collapse

source-injection as the dominant mechanism. This is observed when both p+-sources forward bias in the SRAM and both pMOSFET drains have a negative current.

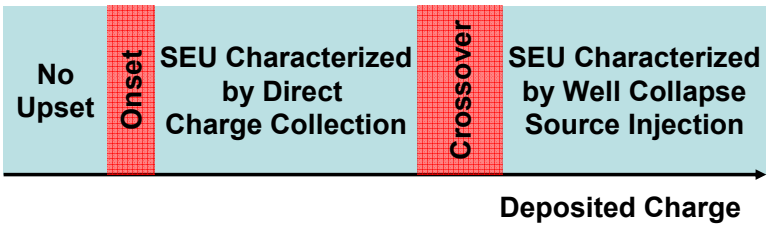



Figure 38. SRAM cell SEU modes as a function of deposited charge.

One more point should be noted with respect to SEU mechanisms relating to the ion shunt mechanism. There was no evidence in any of the simulations that demonstrated the ion shunt mechanism having a role in the upset for this cell at the 90-nm fabrication technology. The following figures compare two normal ion strikes of 0.15 pC/μm each, one to the ON pMOSFET drain and one near the ON pMOSFET drain, as shown in Figure 39. The node voltages for the ion strike directly to the ON pMOSFET drain are shown in Figure 40, and the node voltages for the ion strike near the ON pMOSFET drain are shown in Figure 41. The ON drain potential, Node B, does not collapse towards $V_{SS}$ any differently in either of these plots. Thus, there is no shunt created between the ON drain and the substrate.

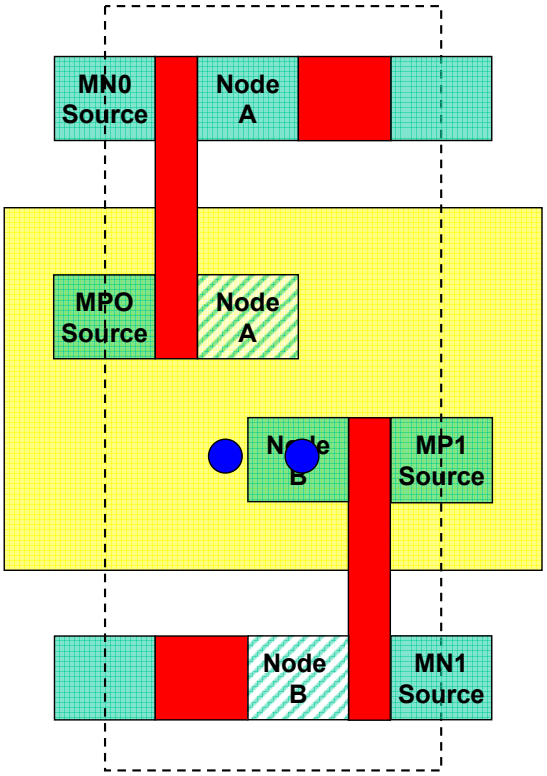



Figure 39. SRAM cell layout showing ion strike locations for ion shunt experiment.

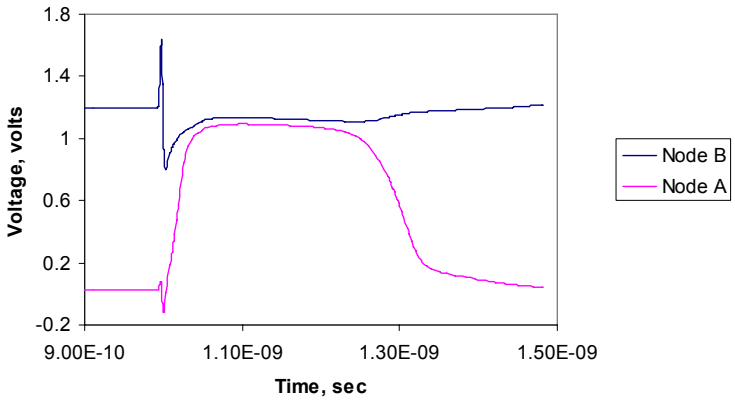



Figure 40. SRAM cell node voltage plot following ion strike to ON pMOSFET drain.

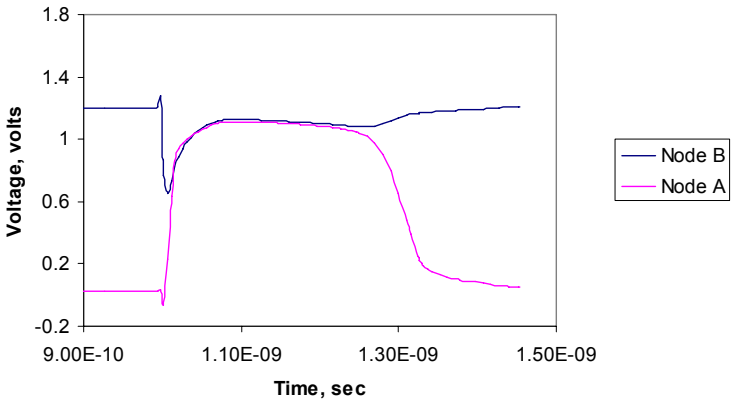



Figure 41. SRAM cell node voltage plot following ion strike near to ON pMOSFET drain.

## To Flip or Not to Flip, That is the Question

Examining the figures from the previous discussion, it could be argued that the well-collapse source-injection places the SRAM into a meta-stable state. The two pMOSFETs are in bipolar operation, and the two nMOSFETs are ON. So, this begs the question of what state will the SRAM cell produce once it recovers. The key issue is whether or not the post-strike state of the cell is flipped or not with respect to the pre-strike state. To answer the question, it has to be divided into different domains: (1) well-collapse – no nMOSFET direct charge collection, (2) well-collapse – OFF nMOSFET direct charge collection, and (3) well-collapse – ON nMOSFET direct charge collection.

### Well-Collapse – No nMOSFET Direct Charge Collection

The first domain is a strike inside the well that induces well-collapse source-injection, but does not diffuse significant charge to either nMOSFET device. Consider the following set of ion strikes, all normal to the surface, shown in Figure 42. The figure labels the locations I-VI and shows the locations of the p+-sources and the drains that

hold the node voltages. At first glance, locations I and VI are closer to the OFF pMOSFET drain (node A) than the ON pMOSFET drain (node B), and should flip the cell. Locations IV and V are closer to node B than node A and should hold the cell state. Finally, locations II and III are almost equidistant from each drain, though location II is closer to node A and location III is closer to node B, so ion strikes at location II should flip the cell, and ion strikes at location III should not. The following six figures show the pMOSFET source currents and the node voltages versus time for each of the locations. In each figure the two voltages, node A and node B, are referenced to the left axis, and the two currents, MP0-$I_S$ and MP1-$I_S$, are referenced to the right axis.

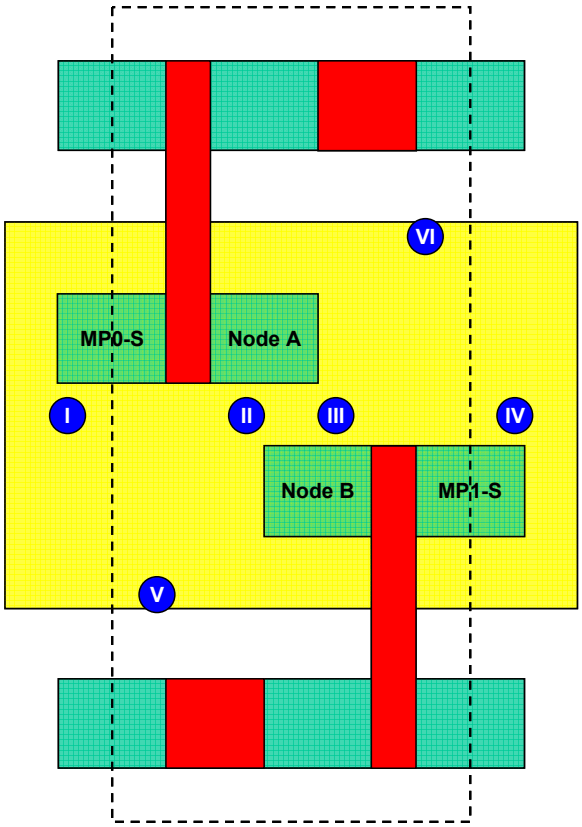



Figure 42. Ion strike locations for 0.10 pC/μm charge deposition to examine SRAM output state for well-collapse source-injection to pMOSFETs only.

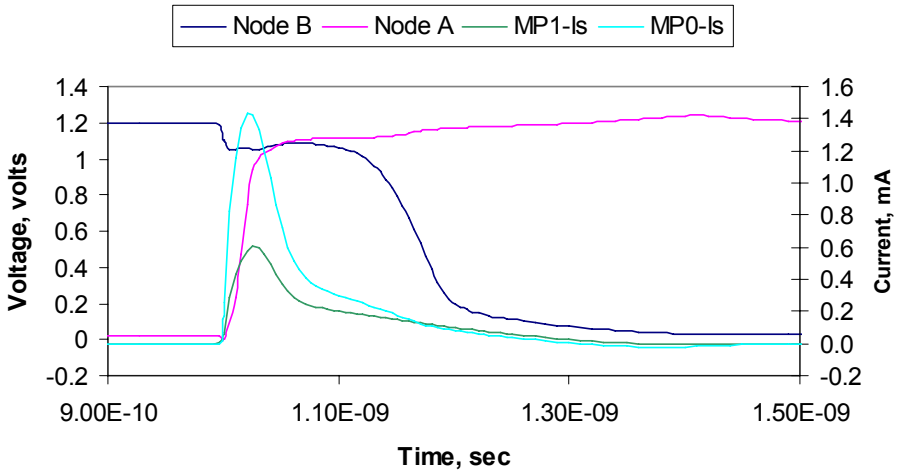



Figure 43. Node voltages and pMOSFET source currents versus time for ion strike location I as depicted in Figure 42.

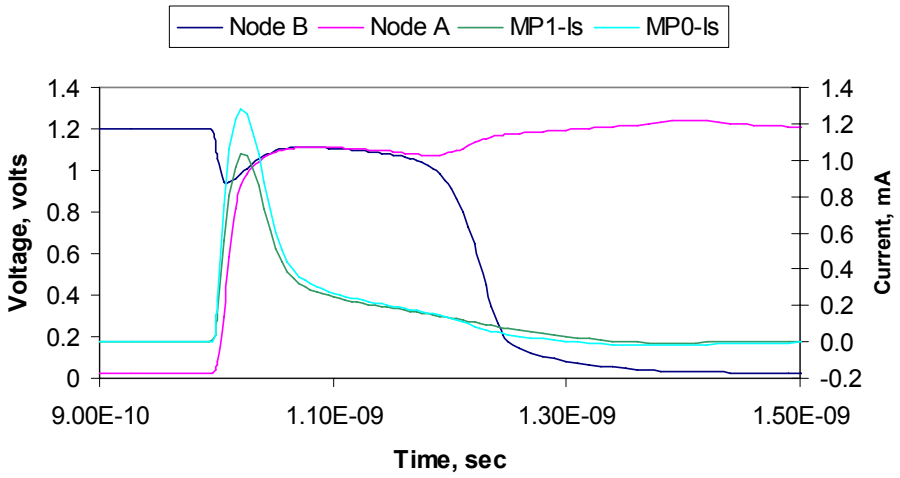



Figure 44. Node voltages and pMOSFET source currents versus time for ion strike location II as depicted in Figure 42.

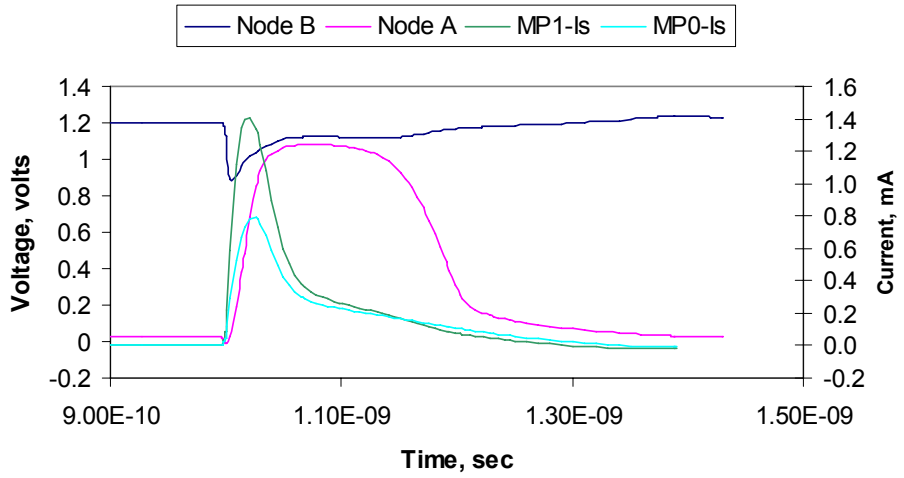



Figure 45. Node voltages and pMOSFET source currents versus time for ion strike location III as depicted in Figure 42.

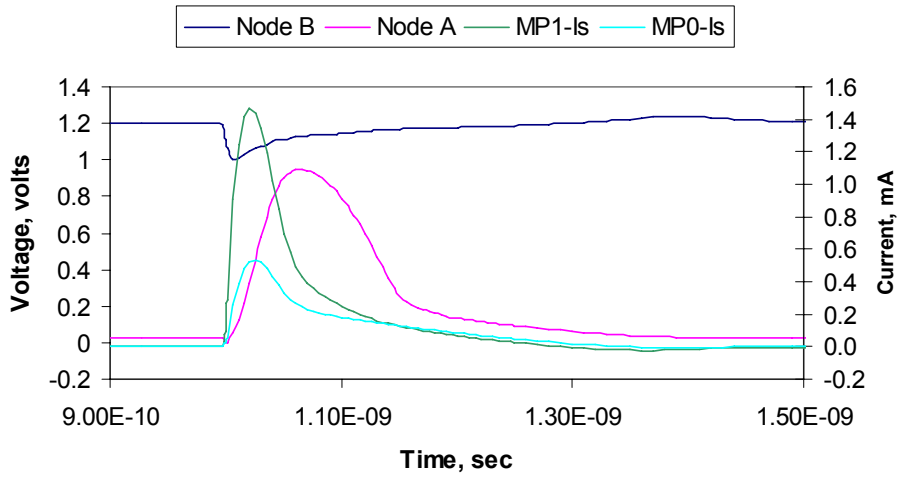



Figure 46. Node voltages and pMOSFET source vurrents versus time for ion strike location IV as depicted in Figure 42.

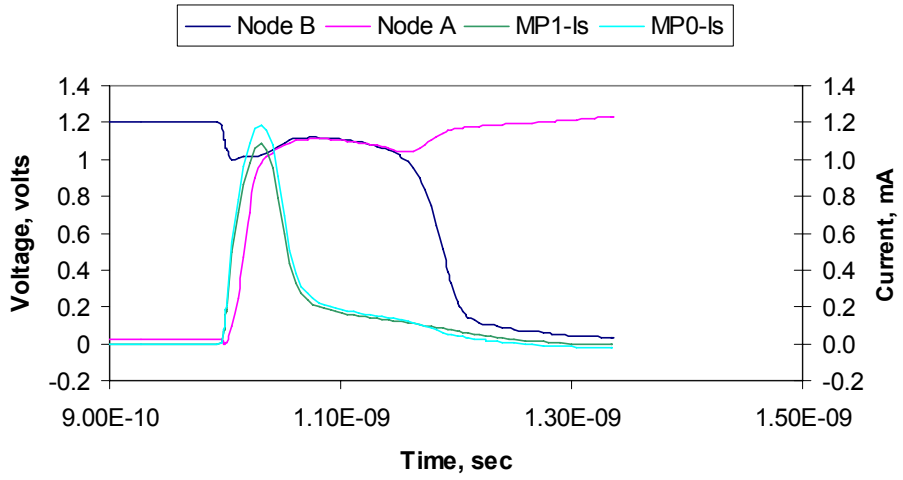



Figure 47. Node voltages and pMOSFET source vurrents versus time for ion strike location V as depicted in Figure 42.

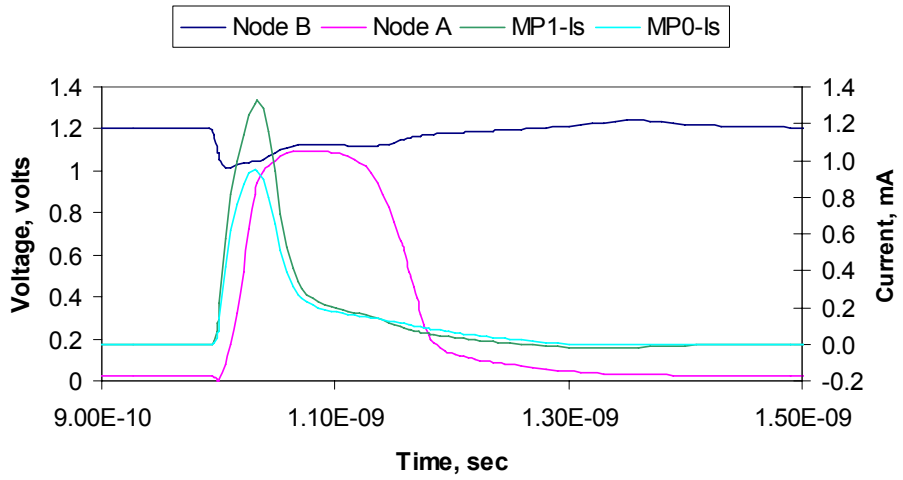



Figure 48. Node voltages and pMOSFET source currents versus time for ion strike location VI as depicted in Figure 42.

The results of these simulations followed the initial expectation for four of the six locations. Locations I, II, III, and IV responded as might be expected based upon distance to a respective drain. However, locations V and VI did not match this model. Although

location V is closer to the ON drain, a strike at that location did flip the cell. The strike at location VI did not flip the cell even though it was closer to the OFF drain.

Instead the output state of the SRAM cell at these strike locations is deterministic based upon well-collapse source-injection. Whichever p+-source in the SRAM provides more current dictates the final state of the SRAM cell. This is a key point which will be used later to perform MCU pattern identification. For the SRAM cell example, when MP0-$I_s$ is higher than MP1-$I_s$, Node A has a logic low output state, and when the currents are reversed, Node A has a logic high output state. Note that all the previous simulations were consistent with that model. The main factor that determines which source will provide the most current is dependent on the resistive path from the source to the location of the well-collapse.

The following example demonstrates that this difference is based upon the resistive path. It is assumed that the resistive path from the bottom of the source junction to the top of the well is identical for each source, given the design of the TCAD model. The resistance from the well-collapse point to the region where the source resistance meets the well is calculated by integrating the resistive path. To illustrate, consider the two resistive paths as shown in Figure 49. The resistive path to MP0 is wider, but longer than the resistive path to MP1. Note that this is a two dimensional rendering of the resistive path; in reality it is 3-D and much more complicated.

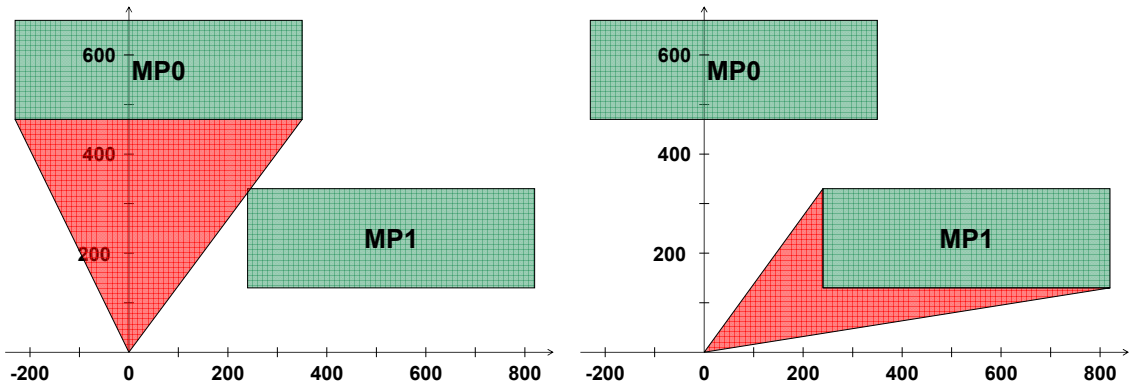



Figure 49. Image of resistive path to each p+-source (distances given in nm).

To calculate a comparative resistance value to each source, the following procedure is followed:

1. Calculate the angle formed at the ion strike location with respect to the path to the source, $\alpha$.
2. Divide the angular sweep into 10 equal intervals.
3. Calculate the distance from the ion strike location to where it reaches the source for each angle in the interval (11 total distances).
4. Average the distances for each interval. This provides the resistive length term, $l$ (10 average distances).
5. Calculate the arc path length near the source that is swept by the angular interval. This is calculated by the following equation.

$$w = 2\pi\alpha l \tag{15}$$

6. Calculate the resistance for each interval, assuming a nominal width at the ion strike (20 nm) and assuming a constant depth, $d$, in the third dimension. This calculation is based upon the following derivation using Figure 50.

$$R = \int_0^l \frac{\rho}{d\left[s + \frac{w-s}{l}x\right]} dx$$

$$R = \frac{\rho}{d}\int_0^l \frac{1}{\left[s + \frac{w-s}{l}x\right]} dx$$

$$Let\ u = s + \frac{w-s}{l}x$$

$$Then\ du = \frac{w-s}{l}dx$$

$$R = \frac{\rho}{d}\int_s^w \frac{1}{u}\frac{l}{w-s} du$$

$$R = \frac{\rho l}{d(w-s)}\int_s^w \frac{1}{u} du$$

$$R = \frac{\rho l}{d(w-s)}[\ln(w) - \ln(s)] \tag{16}$$

7. Calculate the combined resistance term by placing the 10 resistances in parallel.

Table 1 and Table 2 provide the results of applying this resistance calculation to each path shown in Figure 49. These tables start with the angle, α, and break it up into ten pieces. The second to seventh columns show the distances calculated as above, and are all provided in nanometer dimensions. The R-piece is calculated using equation 16, though no depth was used for either table; thus, the R-piece is a resistance per depth value. G-piece is the inverse of R-piece, and R-total is the inverse of the sum of the G-piece values. R-piece is provided for comparison between the two paths and is not an actual resistance value. From these calculations, it is noted that the path to MP0 is less than the

path to MP1, which is as expected. It is noted that this is a very simple calculation (i.e., a two dimensional representation of a 3-D problem), so it is important that the TCAD tool perform the simulation, as it can determine this resistive path automatically. This exercise demonstrates that the resistive path controls the p+-source current, which in turn determines the output state of the SRAM cell. As a result, an upset (flip) is observed on the cell if the OFF source is the less resistive path to the well-collapse charge collection region. Otherwise, the cell will revert to its original state following the well-collapse source-injection.

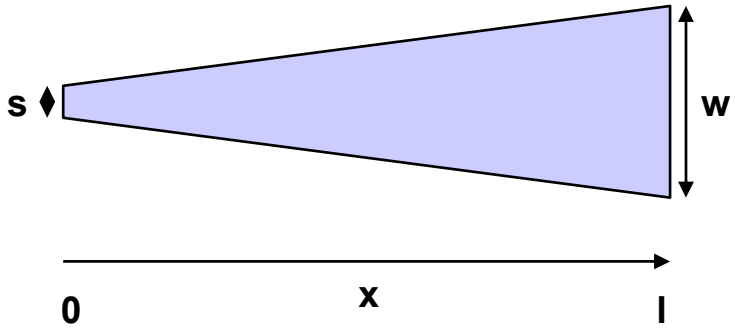



Figure 50. View of resistive path from small interval to large interval.

Well-Collapse – OFF nMOSFET Direct Charge Collection

The second domain is a strike inside or outside the well that induces well-collapse source-injection and has direct charge collection at the OFF nMOSFET. Consider the set of ion strikes, all normal to the surface, shown in Figure 51. The figure labels the location VII-X and shows the locations of the p+-sources and the drains that hold the node voltages. At a very similar charge deposition to the first domain, 0.12 pC/μm, the cell output state completely follows the well-collapse source-injection, as presented in the

Table 1. Quasi-resistance term calculation for path to MP0.

| | | |
|---|---|---|
| $\alpha$ | 1.0914 | radians |
| $\alpha/10$ | 0.1091 | radians |

| Interval | xdist, nm | ydist, nm | length, nm | l, nm | w, nm | s, nm | R-piece | G-piece | R-total |
|---|---|---|---|---|---|---|---|---|---|
| 0 | -0.2200 | 0.4700 | 0.5189 | | | | | | |
| 1 | -0.1603 | 0.4700 | 0.4966 | 0.5078 | 0.0554 | 0.0200 | 14.6110 | 0.0684 | |
| 2 | -0.1049 | 0.4700 | 0.4816 | 0.4891 | 0.0534 | 0.0200 | 14.3837 | 0.0695 | |
| 3 | -0.0521 | 0.4700 | 0.4729 | 0.4772 | 0.0521 | 0.0200 | 14.2361 | 0.0702 | |
| 4 | -0.0006 | 0.4700 | 0.4700 | 0.4714 | 0.0515 | 0.0200 | 14.1632 | 0.0706 | |
| 5 | 0.0509 | 0.4700 | 0.4728 | 0.4714 | 0.0514 | 0.0200 | 14.1624 | 0.0706 | |
| 6 | 0.1037 | 0.4700 | 0.4813 | 0.4770 | 0.0521 | 0.0200 | 14.2337 | 0.0703 | 1.4494 |
| 7 | 0.1590 | 0.4700 | 0.4962 | 0.4887 | 0.0533 | 0.0200 | 14.3796 | 0.0695 | |
| 8 | 0.2186 | 0.4700 | 0.5184 | 0.5073 | 0.0554 | 0.0200 | 14.6050 | 0.0685 | |
| 9 | 0.2846 | 0.4700 | 0.5495 | 0.5339 | 0.0583 | 0.0200 | 14.9183 | 0.0670 | |
| 10 | 0.3600 | 0.4700 | 0.5920 | 0.5707 | 0.0623 | 0.0200 | 15.3320 | 0.0652 | |

Table 2. Quasi-resistance term calculation for path to MP1.

| | | |
|---|---|---|
| $\alpha$ | 0.7848 | radians |
| $\alpha/10$ | 0.0785 | radians |

| Interval | xdist, nm | ydist, nm | length, nm | l, nm | w, nm | s, nm | R-piece | G-piece | R-total |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0.2400 | 0.3300 | 0.4080 | | | | | | |
| 1 | 0.2400 | 0.2808 | 0.3694 | 0.3887 | 0.0305 | 0.0200 | 15.6208 | 0.0640 | |
| 2 | 0.2400 | 0.2398 | 0.3393 | 0.3543 | 0.0278 | 0.0200 | 14.9573 | 0.0669 | |
| 3 | 0.2400 | 0.2049 | 0.3155 | 0.3274 | 0.0257 | 0.0200 | 14.4055 | 0.0694 | |
| 4 | 0.2400 | 0.1743 | 0.2966 | 0.3061 | 0.0240 | 0.0200 | 13.9451 | 0.0717 | |
| 5 | 0.2400 | 0.1470 | 0.2815 | 0.2890 | 0.0227 | 0.0200 | 13.5612 | 0.0737 | |
| 6 | 0.2552 | 0.1300 | 0.2864 | 0.2839 | 0.0223 | 0.0200 | 13.4433 | 0.0744 | 1.5083 |
| 7 | 0.3139 | 0.1300 | 0.3397 | 0.3131 | 0.0246 | 0.0200 | 14.0984 | 0.0709 | |
| 8 | 0.4001 | 0.1300 | 0.4207 | 0.3802 | 0.0298 | 0.0200 | 15.4606 | 0.0647 | |
| 9 | 0.5413 | 0.1300 | 0.5567 | 0.4887 | 0.0383 | 0.0200 | 17.3372 | 0.0577 | |
| 10 | 0.8200 | 0.1300 | 0.8302 | 0.6935 | 0.0544 | 0.0200 | 20.1670 | 0.0496 | |

preceding paragraph, with the exception of hit location VIII. The less resistive path to the p+-sources is as follows per hit location: VII – MP0, VIII, IX, and X – MP1. If the output

state model is based solely upon well-collapse source-injection, VII would flip states, and the rest would hold their states. The node voltages and source currents are plotted in Figure 52, Figure 53, Figure 54, and Figure 55. Normally, a higher source current at MP0 would indicate that Node A returns to logic low, but the ion strike at VIII flips under these conditions. It is noted that the two source currents are very close, so diffusion to the OFF nMOSFET is a factor in this particular location. This shows that a strike close to the OFF nMOSFET drain can enable direct charge collection to have an impact on the final state.

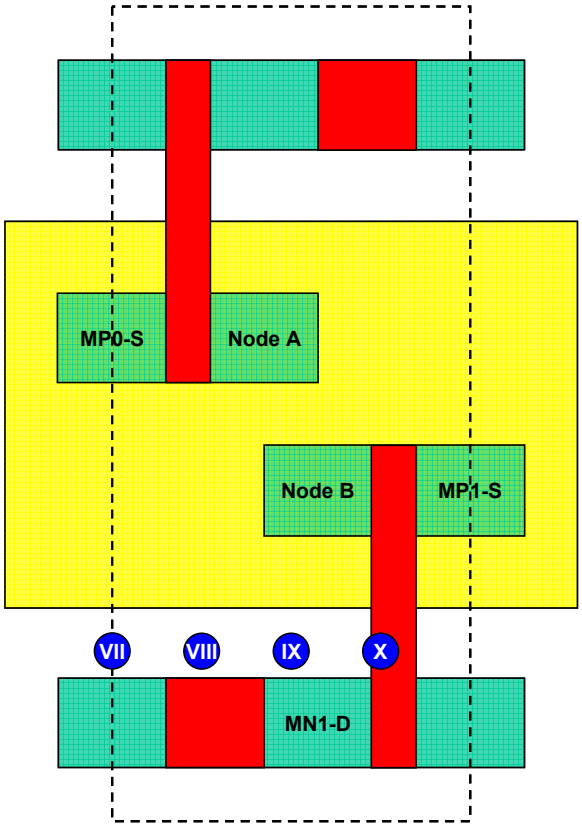



Figure 51. Ion strike locations for 0.12 pC/μm charge deposition to examine SRAM output state for well-collapse source-injection to pMOSFETs and direct charge collection for OFF nMOSFET.

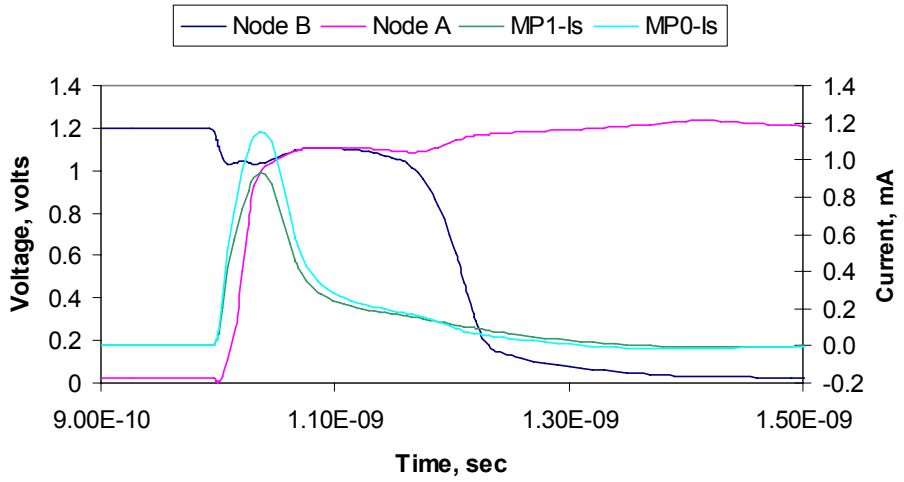



Figure 52. Node voltages and pMOSFET source currents versus time for ion strike location VII as depicted in Figure 51.

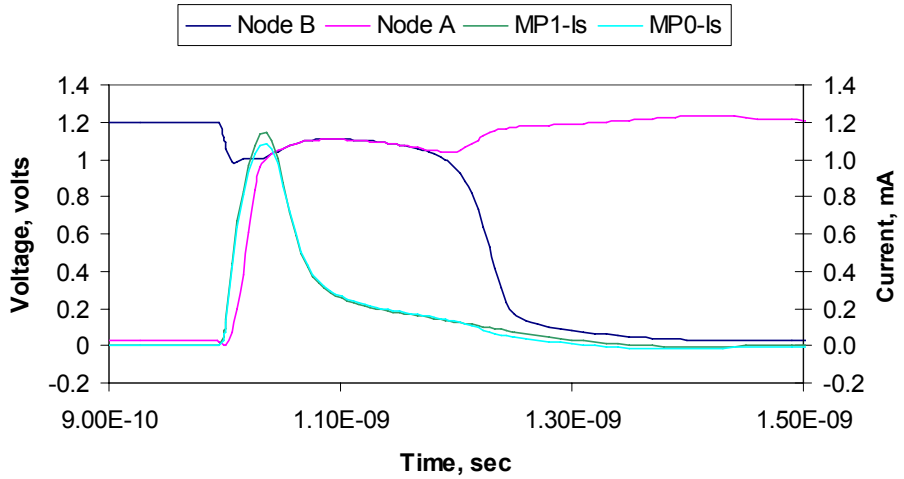



Figure 53. Node voltages and pMOSFET source currents versus time for ion strike location VIII as depicted in Figure 51.

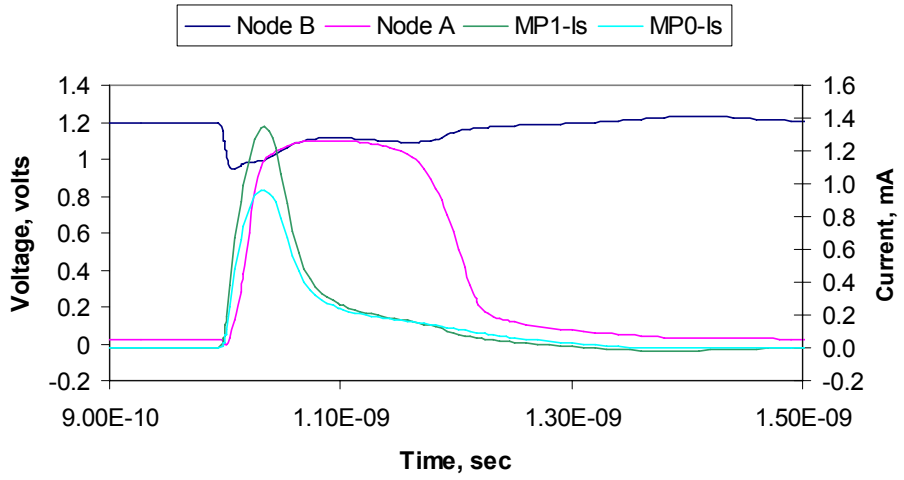



Figure 54. Node voltages and pMOSFET source currents versus time for ion strike location IX as depicted in Figure 51.

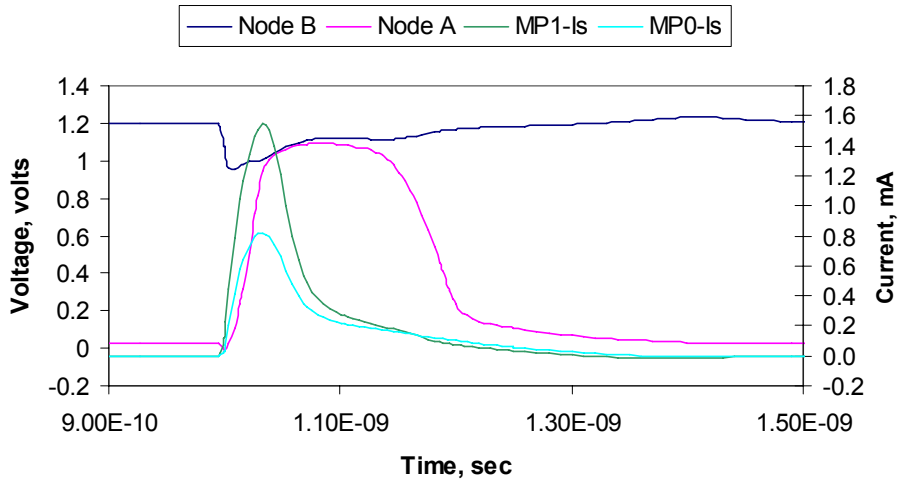



Figure 55. Node voltages and pMOSFET source currents versus time for ion strike location X as depicted in Figure 51.

A most interesting result of the well-collapse source-injection mechanism is now shown with a direct strike to the OFF nMOSFET drain. This particular ion strike should upset for any charge deposition greater than 0.005 pC/μm. This is generally the case. However at a charge deposition of 0.45 pC/μm, the SRAM flips its state due to the direct

charge collection, but then flips again due to the well-collapse source-injection mechanism. This is shown in Figure 56. It is noted that once the cell flips, MP0 becomes the OFF pMOSFET. Since it is the least resistive p+-source to the well-collapse region, the cell reverts back to its original state. This is the first time a direct strike to an OFF nMOSFET above the critical charge of the SRAM is demonstrated to upset twice (or result in no observable upset).

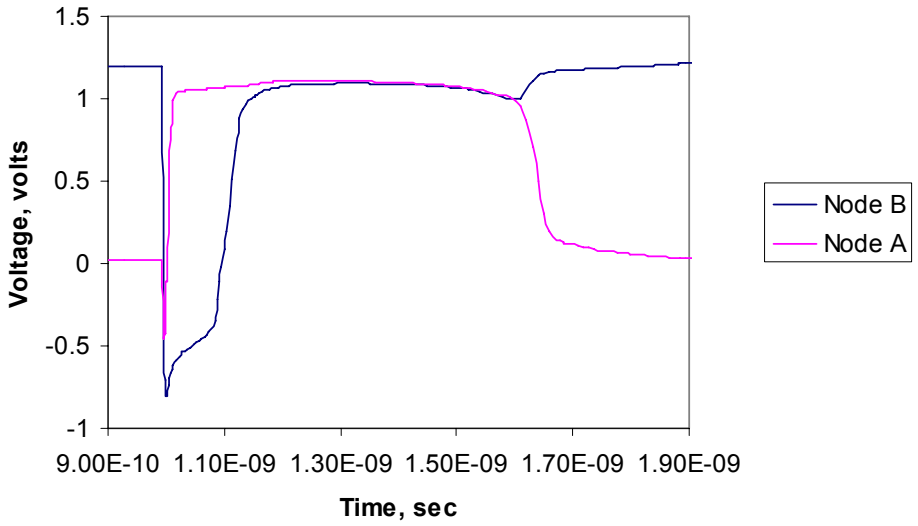



Figure 56. Ion strike, 0.45 pC/μm, to OFF nMOSFET drain showing double upset.

Well-Collapse – ON nMOSFET Direct Charge Collection

The last domain is a strike inside or outside the well that induces well-collapse source-injection and has direct charge collection at the ON nMOSFET. Consider the set of ion strikes, all normal to the surface, shown in Figure 57. The figure labels the location XI-XIV and shows the locations of the p+-sources and the drains that hold the node voltages. It takes a larger charge deposition than the first and second domains, 0.20

pC/μm, for the cell output state to somewhat follow the well-collapse source-injection mechanism. If that mechanism was dominant in all locations, XI, XII, and XIII would flip (resistance to MP0 is less than resistance to MP1) and XIV would not (resistance to MP0 is greater than resistance to MP1). In the data shown in Figure 58, Figure 59, Figure 60, and Figure 61, locations XII and XIII provide alternate results. This means that the direct charge collection by the ON nMOSFET drain is playing a role. However, it is noted that this is just a small region that does not exactly follow the mechanism; strikes to the left of XI will induce a cell upset and strikes to the right of XIV will not induce a cell upset.

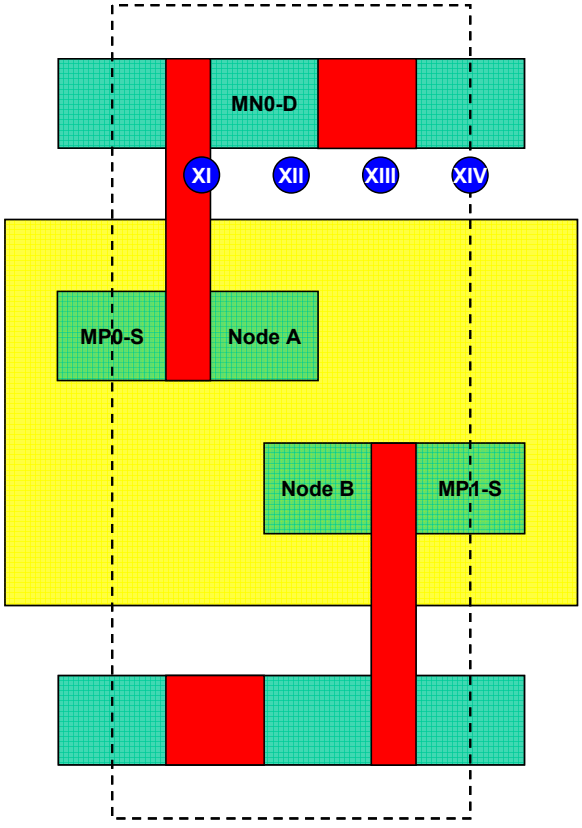



Figure 57. Ion strike locations for 0.20 pC/μm charge deposition to examine SRAM output state for well-collapse source-injection to pMOSFETs and direct charge collection for ON nMOSFET.

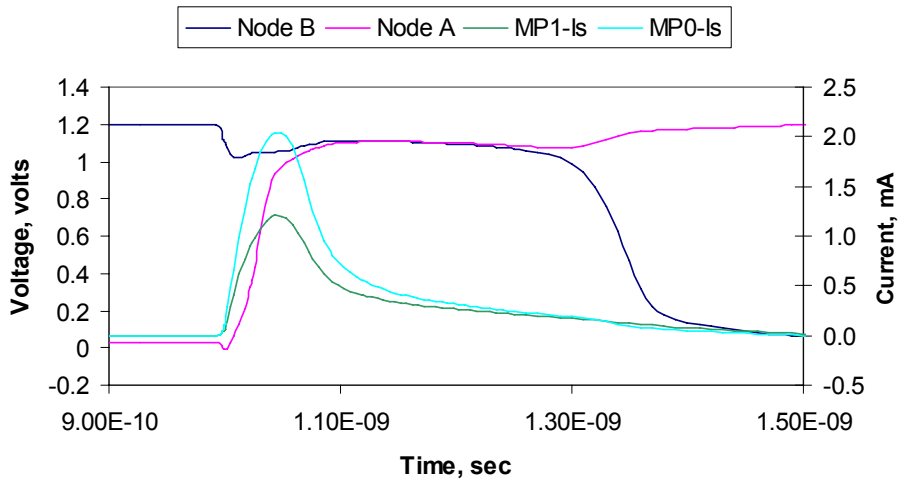



Figure 58. Node voltages and pMOSFET source currents versus time for ion strike location XI as depicted in Figure 57.

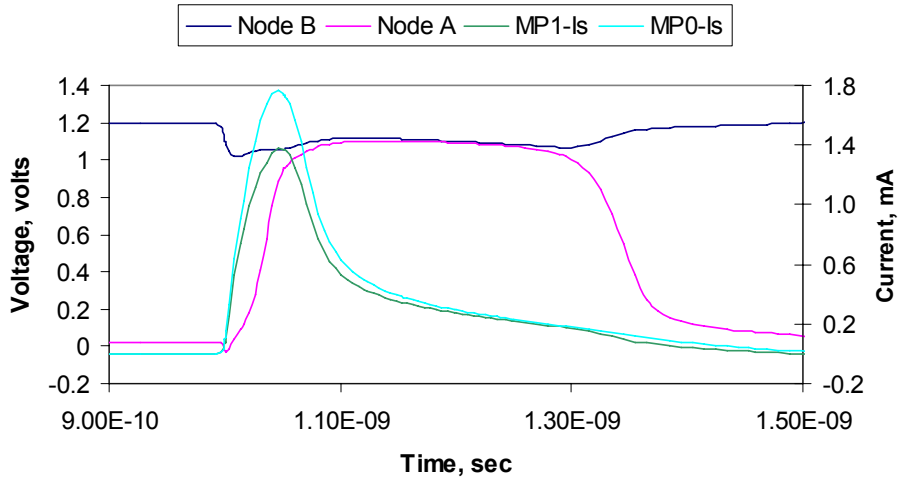



Figure 59. Node voltages and pMOSFET source currents versus time for ion strike location XII as depicted in Figure 57.

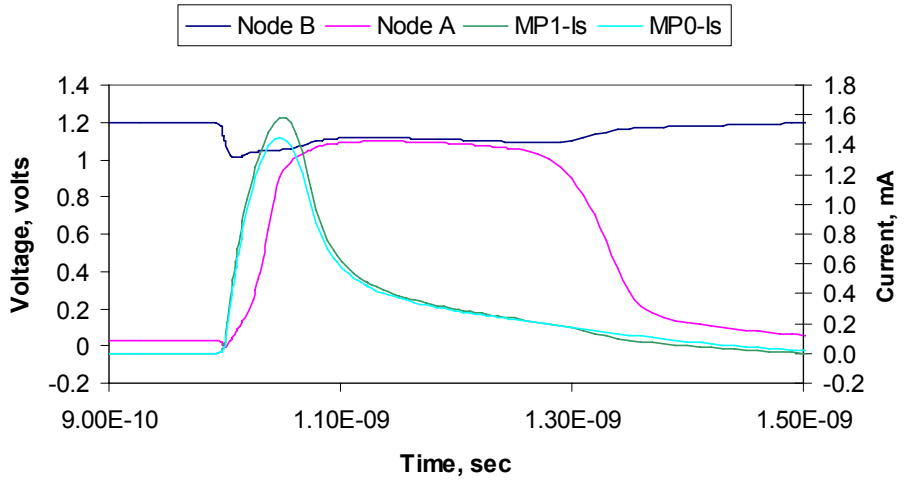



Figure 60. Node voltages and pMOSFET source currents versus time for ion strike location XIII as depicted in Figure 57.

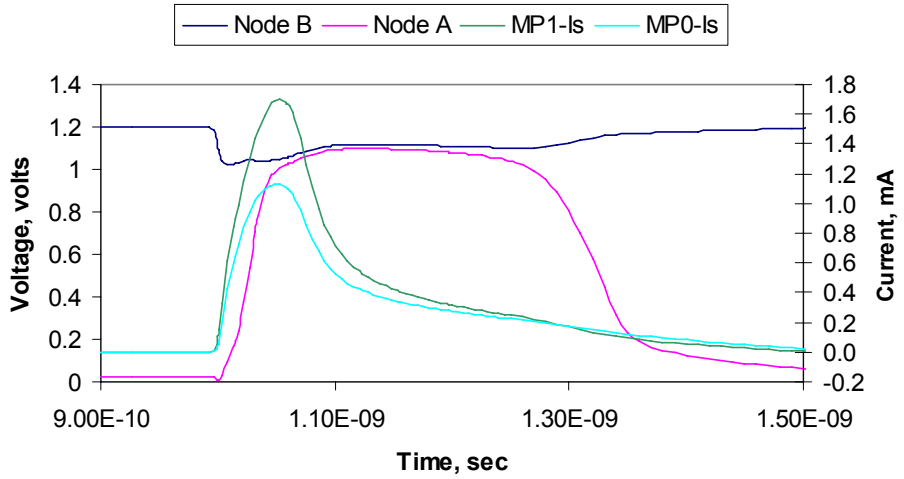



Figure 61. Node voltages and pMOSFET source currents versus time for ion strike location XIV as depicted in Figure 57.

## SRAM Cell Recovery

This subject has been touched upon briefly in this chapter, but this section describes the process by which the individual SRAM cell recovers. As the charge deposition increases, the amount of single event current generated at the well/substrate p-

n junction increases. This causes the p+-sources in the well to forward bias and inject more minority carriers into the well, in addition to the ones generated from the charge track. Once the single event current subsides, the well potential starts to restore, and the forward bias on the p+-sources reduces. When the forward bias declines to where the bipolar operation of the pMOSFETs is no longer dominant, the cell recovers to a stable state. So, it is the exit of the forward bias condition that determines when the cell recovers.

## Impact of Well-Collapse Source-Injection on SRAM Cell SEU

In the case of direct charge collection, when the SEU cross section approaches the area of the SRAM cell, the half of the cell nearest the OFF drains would be the expected regions of upset, while the other half would be the expected regions of no upset. With well-collapse source-injection, the half of the cell with the lowest resistive path to the OFF p+-source accounts for the expected region of upset, while the other half is for no upset. It amounts to a 50% region of upset in the first case and a 50% region of upset in the second case. While this mechanism does not alter the overall vulnerability within an SRAM cell, it does provide an improved understanding of SEU within a full SRAM array. This is discussed in the next chapter.

However, there is one note about the fabrication of SRAM cells and the fact that there are variations in the formation of the STI. As a result, the resistance for the p+-sources to the well will vary depending upon the area of the semiconductor region. If the variance is significant, the SRAM cell may have a preferred output state following the well-collapse source-injection event. This preference will not be produced 100% of the

time, but there may be some percentage difference in the output state instead of an even 50-50 split. In Chapter X, there will be additional discussion of this point.

# CHAPTER VI

# STATIC RANDOM ACCESS MEMORY ARRAY

In this chapter, the SRAM array is discussed with respect to single event effects. The main emphasis of the research is to determine the multiple cell upset (MCU) patterns so that SEU testing can be matched to mechanisms. In this chapter, the single SRAM cell SEU mechanisms will be projected to potential observed SRAM array MCU patterns. The following two chapters provide the TCAD modeling in support of the SRAM array MCUs and the correlation of SRAM array SEU test data. So, this chapter mainly serves to form the hypothesis that the next two chapters are testing.

## Characteristics

An SRAM circuit block or full SRAM chip is a very complex system. The SRAM cells are the bulk of the design, but there are many supporting circuits to write and read the contents of the cells. First, there are sense amplifiers, used to read small differential signals from the BL and $\overline{\text{BL}}$ wires. Second, there are other memory circuits, latches and flip-flops, which are used to store the row and column addresses as well as the data words. Finally, there is also a control circuit to distribute internal timing signals to the circuit block or full chip. Taking all these items together, the potential single event effects that could result are numerous. This research, however, only focuses on the SRAM cells in the array and their respective single event upset characteristics.

## Layout

Figure 62 shows a sample SRAM array composed of the basic SRAM cell layout provided in Figure 28. This has twelve rows and four columns. The metallization is not shown, just the n-well (yellow), n+ source/drains (light blue), p+ source/drains (light green), and polysilicon (red). There are a few items of note with respect to this layout. First, the wells are oriented in long strips, top to bottom in this figure. There are no well contacts shown. In commercial SRAM layouts, the well contacts are sparse, every 10-25 μm (10 μm is approximately the width of this layout in 90-nm microelectronics technology). In radiation hardened SRAM layouts, the well contacts are a little more regular to aid in mitigating single event latchup. Second, the n+-source/drains (light blue) that are to the left and the right of the n-well form a narrow continuous opening through the STI. This aspect of the array layout will impact MCU response due to direct charge collection. Third, the p+-source/drains each have one source and two drains with the exception of the top and bottom cells. That the source is shared with two adjacent SRAM cells is important for direct charge collection MCU. However, this also plays a role in the MCU patterns observed following well-collapse source-injection. Lastly, a column of SRAM cells alternately share BL and $\overline{BL}$ connections with the exception of the top and bottom cells. This vertically aligns both the true node and the complement node within the column. For purposes of this dissertation, it is always assumed that BL is always on the left of a column and $\overline{BL}$ is on the right. There are some instances where SRAM arrays alternate BL and $\overline{BL}$ orientation from column to column, but this topology is not discussed.

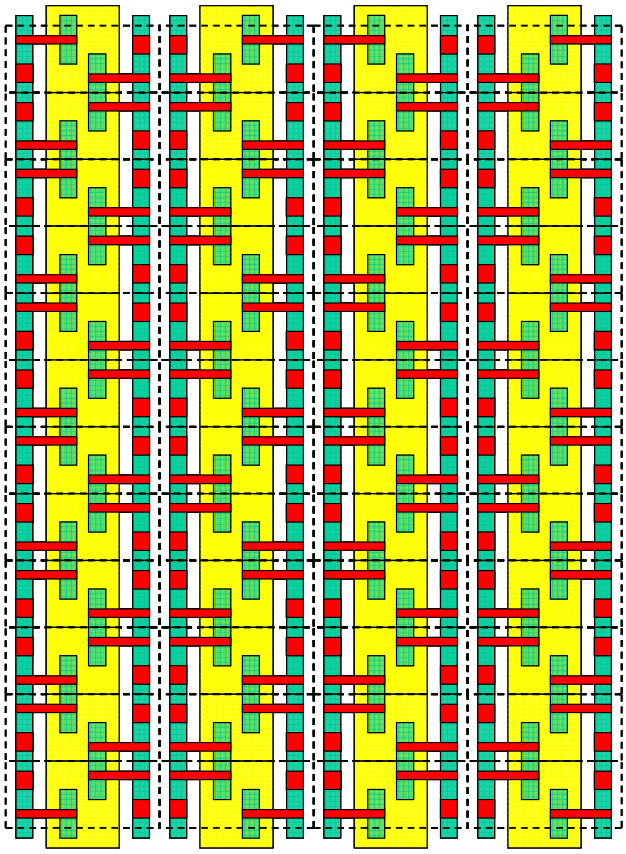


Figure 62. Sample layout of SRAM array (12 x 4).

## Single Event Upset Observations

### Historical Perspective

Over the years, as SRAM cells have scaled down in size, a new effect was observed: multiple cell upsets (MCU) from a single event [Ma87]. Dodd et al. used mixed-mode device/circuit modeling to demonstrate that the MCU mechanism is due to charge collection in adjacent SRAM cells [Do94]. Still, the primary mechanism for a single SRAM cell to flip was charge collection at an OFF transistor drain due to direct charge collection.

Characterizing SRAM SEU only by direct charge collection (drift and diffusion) restricts the range of possible MCU outcomes. Figure 63 shows the range of MCU outcomes from ion strikes normal to the surface. The strike marked A is on or near a shared p+-source with two p+-drains. Depending on the initial SRAM array configuration and the amount of charge collected on each drain, there can be zero, one, or two upsets. If both of the transistors in this region are ON, then there are no upsets from direct charge collection. If they are in opposite conditions, there can be one upset. However, both of the transistors have to be off for there to be two upsets. To encourage this mode for testing SRAM arrays, it is best to test with a constant pattern in each column, all zeros or all ones. In that manner, all the cells in the array are configured the same, so one half of the shared p+-source/drain regions will have two OFF MOSFETs and the other half will have two ON MOSFETs.

The ion strike marked as B is outside of the well and is centered about four adjacent nMOSFET drains which belong to different SRAM cells. Like the previous case, there are a number of deterministic outcomes based on the pre-existing storage states of the SRAM cell and the charge collection at each drain. A strike that is on or near this location can cause zero, one, two, three, or four upsets. As in the previous discussion, the best case for this is to load the memory with the same state in each column, but alternate logic high and logic low every other column. The nMOSFET drains between two wells will either all be ON or all be OFF.

Stepping beyond normal incident ions and considering all potential incoming angles, the number of affected cells can grow through direct charge collection, but it is possible to bound the range of outcomes depending on the direction and angle of

incidence. The major source of MCUs will be grazing angles along the well direction. In this direction, charge collection will be in only one of the transistors in each SRAM cell. Figure 64 shows a plot of the number of SRAM cells traversed for an ion traveling in this direction versus the ion strike angle. It is assumed that the ion starts in a drain of the first cell. It is also assumed that drains are spaced at 800 nm intervals. Two depths of ion penetration are plotted; 360 nm is for the bottom of the STI, and 1120 nm is for the bottom of the n-well. It is noted that both of these curves see sharp increases greater than $80^{o}$. At $60^{o}$, a typical limit for SEU testing, the cells traversed are one and three, respectively. At $75^{o}$, the cells traversed are two and six respectively. This shows how the ground-based testing can limit a realistic view of the MCUs, even just considering direct charge collection.

Well-Collapse Source-Injection Considerations

The potential MBU outcomes expand when the amount of charge deposition exceeds the crossover point; in this case, the SRAM SEU response is characterized by well-collapse source-injection. Figure 65 shows an example of an ion strike in the n-well, location C, in SRAM cell in row #6. Assuming the starting state of all the SRAM cells in this column is logic low (locations of OFF drain regions are displayed as a crossed pattern surrounded by thick lines) and assuming all the cells in the column are affected by the single event, the following list of results will occur.

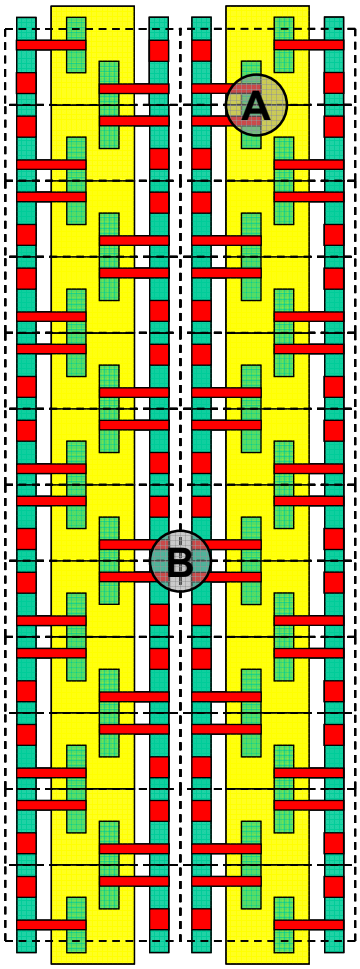



Figure 63. Top view of the sample SRAM array showing potential region of MBUs characterized by direct charge collection.

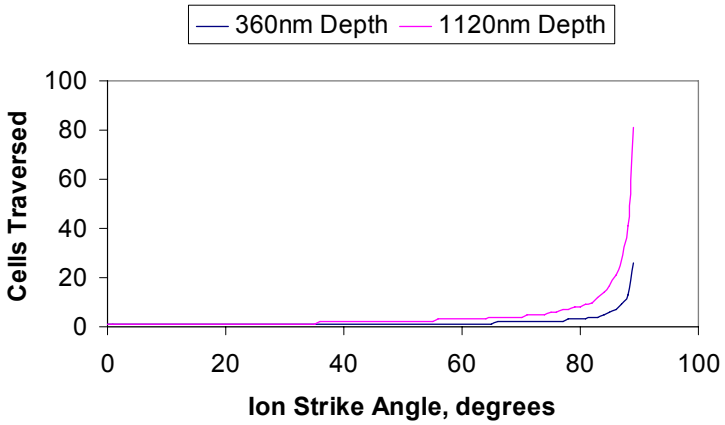



Figure 64. Number of SRAM cells traversed by an ion versus strike angle for two assumed depths.

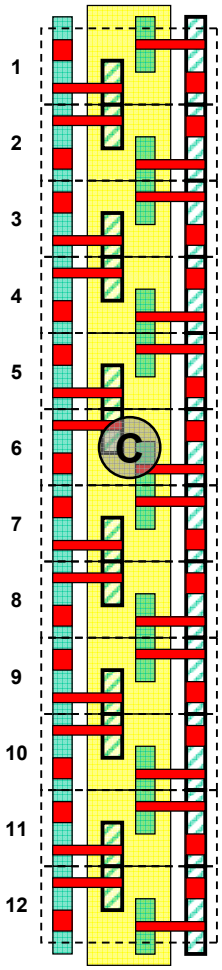



Figure 65. Top view of the sample SRAM array showing potential ion strike location inside the well for MBUs characterized by well-collapse source-injection.

1. SRAM cell in row #6 can upset depending on the specific well-collapse region and the resistive paths from its two p+-sources. This is as described in the previous chapter.
2. SRAM cells in rows #1 to #5 will output in a state dictated by which p+-source is on the bottom of the SRAM cell layout. This p+-source has the least resistive path to the well/substrate charge collection. As a result, these SRAM cells will recover with the lower pMOSFET being ON. Thus,

SRAM cells in rows #1, #3, and #5 will flip to logic high, and SRAM cells in rows #2 and #4 will recover to logic low.

3. SRAM cells in rows #7 to #12 will output a state dictated by which p+-source is on the top of the SRAM cell layout. SRAM cells in rows #8, #10, and #12 will flip to logic high, and SRAM cells in rows #7, #9, and #11 will recover to logic low.

The two possible observed error patterns are shown in Figure 66.

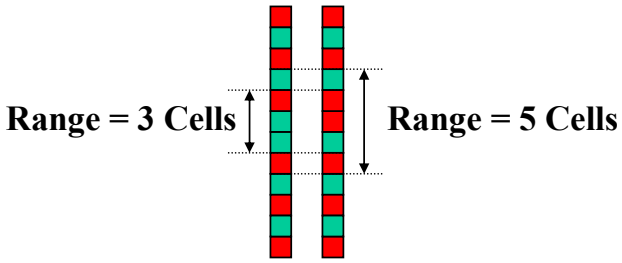



Figure 66. Possible observed error patterns for normal ion strike at location C in Figure 65 assuming all cells are affected by well-collapse source-injection mechanism. SRAM cells that do not upset are shown in green and SRAM cells that upset are shown in red.

The well-collapse source-injection mechanism will not always affect all the cells. So, a key parameter in predicting the specific MCU patterns is the range of effect. If the range of effect of the mechanism is one adjacent cell in the column in either direction, the potential MCU patterns are "■■■" and "■■■." If the range is two adjacent cells in either direction, then the MCU patterns are "■■■■■" and "■■■■■" (Figure 66). An input condition where all the SRAM cells hold the same state is not ideal to test the affected range from well-collapse source-injection. Ideally, all the SRAM cells above the struck location should be biased so that the top of each SRAM cell has the ON pMOSFET. Likewise, all the SRAM cells below the struck location should be biased so that the

bottom of each SRAM cell has the ON pMOSFET. Since it is generally impossible to know the strike location in single event tests outside of laser or microbeam, this type of SRAM cell state programming is impossible. So, the recommended starting SRAM cell state to determine the range of effect is alternating logic high and logic low going down the column. Returning to the example shown in Figure 65, loading the odd SRAM cells with logic low and the even SRAM cells with logic high will bias all the SRAM cells as shown in Figure 67. So, an ion strike at SRAM cell #6 would result in MCU patterns of "■■■■■■■■■■■■" or "■■■■■■■■■■■■," assuming every SRAM

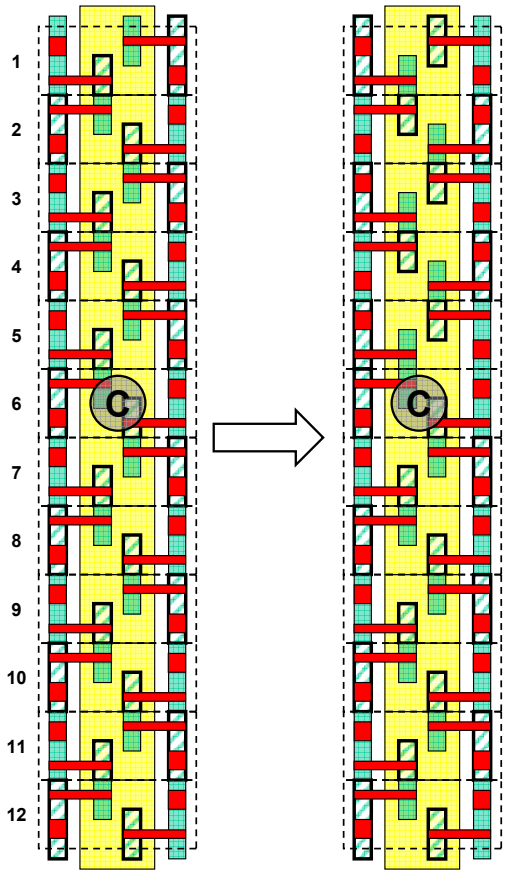



Figure 67. Top view of the sample SRAM array showing pre- and post-single event OFF MOSFETs for alternating data pattern assuming well-collapse source-injection.

cell in the column is affected. With this input condition, the resulting MCU pattern will indicate half of the range of the well-collapse source-injection mechanism.

The previous discussion centered on an ion strike location primarily in the well. The other possibilities for ion strikes normal to the surface are outside the well or between two wells as shown in Figure 68. In these cases, the resulting output MCU patterns are similar to the case inside the well, but are manifested in two columns. Examining the left column, the outcome will match the inside-the-well ion strike case with the exception of SRAM cells #6 and #7. Those cells will recover or flip depending on the respective starting SRAM cell states and the specific region of the well-collapse. In the exact case that is depicted in Figure 68, SRAM cells #6 and #7 will output with the pMOSFETs at the right of the cell ON, or logic high. With respect to the right column, the SRAM cells are just inverted. So, if the starting state in column #2 is the opposite of column #1 as depicted, then the MCU pattern in each row should be identical. To differentiate ion strikes to the well and between the wells, it is best to keep the same pattern in each column. For example, if the starting state in the two columns is

LL
HH
LL
HH
LL
HH
LL
HH
LL
HH
LL
HH

then an ion strike as shown in Figure 68 affecting all SRAM cells with well-collapse source-injection will result in

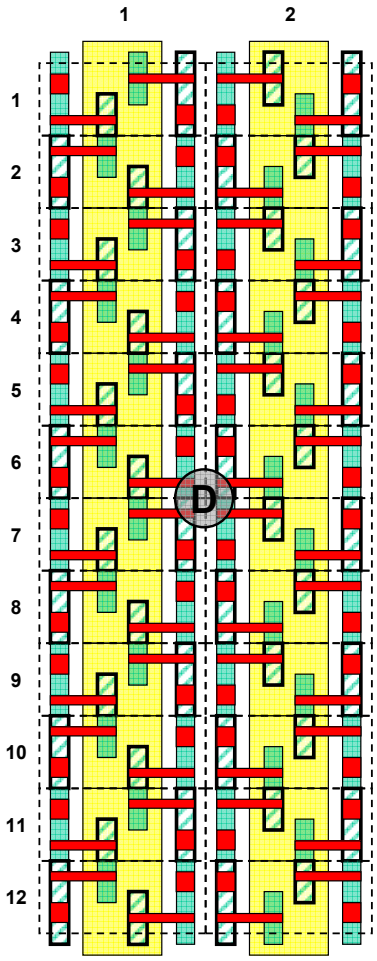



Figure 68 Top view of the sample SRAM array showing potential ion strike location outside the well for MBUs characterized by well-collapse source-injection.

HL
LH
HL
LH
HL
LH
LH
HL
LH
HL
LH
HL

or the MCU pattern

‘  ’

Thus, with this starting SRAM state, the range of the well-collapse source-injection can be determined in both directions. Also, the MCU results from ion strikes inside the well can be separated from those strikes outside the well.

Moving the discussion from normal incidence to other angles provides some interesting options for the well-collapse source-injection mechanism. The first angled scenario to consider is an ion strike down the direction of the well, either inside it or outside it. Near where the ion enters the top of the semiconductor, the SRAM cells will be affected either by direct charge collection or by well-collapse source-injection, depending on the amount of deposited charge. However, near the well/substrate p-n junction charge collection, the effect will be dominated by well-collapse source-injection. If the range of the well-collapse source-injection mechanism extends back to the cells where the ion entered, then the output state will be determined by this mechanism. Cells that may have been flipped due to direct charge collection may flip again in response to well-collapse source-injection. Also, cells that did not flip due to direct charge collection may now flip. So, the result of this type of angular ion strike will be a combination of well-collapse source-injection and direct charge collection.

The second angled scenario to consider is one that goes perpendicular to the well direction. In this case, the ion may travel through many wells, collapsing some to all of them. Once again, near the ion’s point of entry into the semiconductor, the nearby cells may be affected by direct charge collection and/or well-collapse source-injection. Direct charge collection will dominate in ion strikes near the surface of the semiconductor,

above the well, and when the ion distance through the well is small. The resulting MCU patterns of this type of ion strike can extend over many rows and columns. The number of columns affected is determined by the angle of the ion strike with respect to normal, and the cell width and the number of rows affected is determined by the range of well-collapse source-injection.

Most ion angles will not conform to these two scenarios, so the general MCU outcomes are some combination of the two scenarios described above. Angles that are close to the first scenario will generally match its pattern, while most angles will match the second scenario. However, modeling and testing with these two scenarios will give plenty of data to project the MCU possibilities at all angles.

## MCU Pattern Identification

A summary of the potential MCU patterns is provided in Table 3. The table is based on the discussions provided in this chapter. Both "best" test conditions are applied in all variations of angles, so that it is possible to distinguish one mechanism from another during testing. Chapter VII discusses TCAD modeling of the SRAM array to provide a basis for these observed MCUs. This chapter also discusses the models to determine the range of effect of both the direct and well-collapse source-injection mechanisms. Chapter VIII then presents data from SRAM SEU testing and relates the data back to these predictions for the MCU patterns.

Table 3. MCU patterns determined from primary charge collection mechanism, incident angle, direction, and input test condition.

| Charge Collection Mechanism | Incident Angle (degrees) | Direction | Input Test Condition | MCU Patterns | | | | |
|---|---|---|---|---|---|---|---|---|
| Direct | 0-30 | - | LLLL<br>LLLL |  |  |  |  |  |
| Direct | 0-30 | - | LLLL<br>HHHH |  | | | | |
| Direct | 30-90 | Parallel to the Well | LLLL<br>LLLL |  |  |  |  |  |
| Direct | 30-90 | Parallel to the Well | LLLL<br>HHHH |  |  | | | |
| Direct | 30-90 | Normal to the Well | LLLL<br>LLLL |  |  |  |  |  |
| Direct | 30-90 | Normal to the Well | LLLL<br>HHHH |  |  | | | |
| Well-collapse source-injection | 0-30 | - | LLLL<br>LLLL |  |  | | | |
| Well-collapse source-injection | 0-30 | - | LLLL<br>HHHH |  |  |  |  |  |
| Well-collapse source-injection | 30-90 | Parallel to the Well | LLLL<br>LLLL |  |  | | | |
| Well-collapse source-injection | 30-90 | Parallel to the Well | LLLL<br>HHHH |  |  |  |  |  |
| Well-collapse source-injection | 30-90 | Normal to the Well | LLLL<br>LLLL |  | | | | |
| Well-collapse source-injection | 30-90 | Normal to the Well | LLLL<br>HHHH |  | | | | |

# CHAPTER VII

## MODELING AND SIMULATION OF STATIC RANDOM ACCESS MEMORY

In device and circuit modeling, the SRAM cell is created to be ideally balanced, meaning that the device is perfectly symmetric between the two inverters both physically and electrically. An ideally balanced SRAM cell will most likely power up in a metastable state and will need some initial condition in order to drive the cell into one of the two stable states. However, SRAM cells are not ideally balanced in practice. There are a number of manufacturing variations, such as threshold voltage variation and metallization loading, which will unbalance the SRAM cell. In addition, there are some environmental variations, such as noise, which will also work to unbalance the SRAM cell. An unbalanced SRAM cell will power up into one of the two stable states [Fl87, Ax88].

In device modeling, the parameters related to well-collapse source-injection are also implemented ideally. The p+-source/n-body diodes are balanced, and the resistance parameters (resistivity, length, and area) are identical. As a result, the well-collapse source-injection mechanism will respond ideally in device models. However, doping variations in the n-well will affect the resistivity, and lithography variations will affect the length and area terms. Depending on these variations, the SRAM cell may have a preferred recovery state from the well-collapse source-injection mechanism.

This chapter of the dissertation presents the different TCAD models that were implemented to study the SEU response of the SRAM cell and array. Each section of the

chapter presents a TCAD model and discusses results from single event simulations. Models 1 through 4 were developed specifically to analyze the SRAM cell and array, while Models 5 and 6 examine special considerations of the well-collapse source-injection mechanism. All models are 3-D and were constructed using Synopsys Dessis.

## Model 1: SRAM Cell

The initial TCAD model used in this research was a six-transistor SRAM cell. This model was built by Dennis Ball of Vanderbilt University for BAE Systems to study SRAM cell hardening against single event effects. A top view of the cell is shown in Figure 69. An expanded view of the SRAM cell with node labels was provided in Figure 28. The SRAM cell is representative of an unhardened 90-nm SRAM cell produced on an epi-substrate. The TCAD design was ideally matched using symmetry in the doping definitions and meshing of the node points. This SRAM design was shown to upset in TCAD simulation with a charge deposition of 5 fC/μm (LET is approximately 0.5 MeV-cm$^2$/mg) due to an ion strike directly on the drain of the OFF nMOSFET (NHIT).

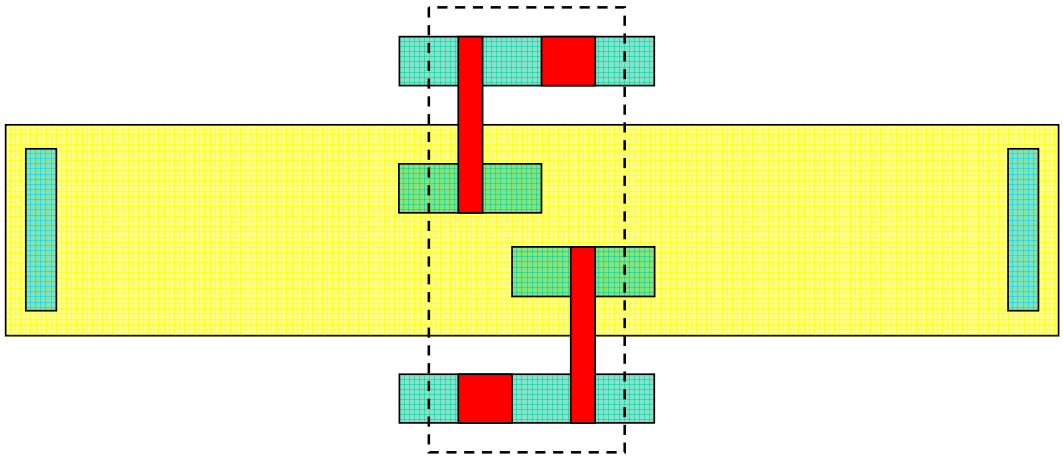


Figure 69. SRAM Cell Model.

All of the TCAD simulations presented in the preceding six chapters are results from this SRAM cell model. This particular model led to: (1) the identification of the well-collapse source-injection mechanism described in Chapter IV and (2) the response of the SRAM cell to this mechanism described in Chapter V. The models presented later in this chapter are all derived from the original SRAM cell model.

The original SRAM cell model is ideal for examining the onset of upset due to direct charge collection from ion strikes to the OFF drains, but it is inadequate to fully characterize SEU response with respect to diffusion and to the well-collapse source-injection mechanism in either the SRAM cell or array. As discussed in Chapter VI, SRAM cells placed in an array share bit lines, $V_{DD}$, and $V_{SS}$ contacts with adjacent cells. This alters the semiconductor region that exists above the bulk semiconductor. The nMOSFETs located above and below the n-well form long, continuous openings in the STI. Yet in the SRAM cell model, diffusing carriers in the nMOSFET regions above the bulk substrate have STI boundaries on the left and right that would not actually exist in a full SRAM cell array. Further, the area of the region containing the pMOSFETs within the n-well do not match the actual areas since there are two drains for each source. Thus, the resistance from the p+-source/n-body junctions to the n-well is modeled to be higher than the actual value. Finally, the SRAM cell model does not include all the p+-sources from the SRAM array that are contained in this n-well. Thus, all the sources of current for the well/substrate p-n junction charge collection are not modeled.

Model 2: N-Well with No P+ Implant Model

The first variation from the SRAM cell model is just a basic 3-D model of the n-well in the p-substrate with no transistors. The intent of this model is to examine the response when only the well contacts can supply current to the well/substrate charge collection. A top view of this TCAD model is shown in Figure 70. This is the exact n-well and n-well contacts found in the original SRAM TCAD model.

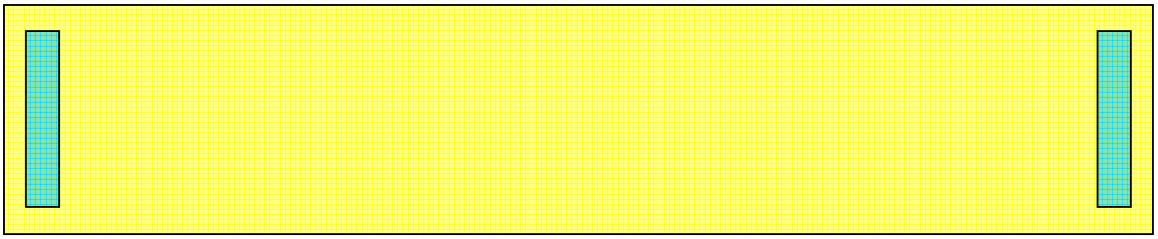


Figure 70. Top view of N-Well with No P+ Implant Model.

Model 2 demonstrates the issues that may be encountered when simulating ion strikes without sources in the well. In this case, the well/substrate p-n junction will become forward-biased; this does not happen when the p+-sources are included and biased at 1.2 V. The source/body p-n junctions will become forward-biased before the well/substrate p-n junction and aid in maintaining the well potential. Thus, Model 1 may provide unrealistic results for ion strikes located far outside of the cell. In this case, the well/substrate p-n junction may forward-bias due to the resistance from the p+-source to the ion strike location.

To demonstrate the charge collection response of this model, an ion strike is simulated in the center of the n-well with a charge deposition of 0.10 pC/μm. The potential of the n-well and p-substrate prior to the simulated ion strike is shown in Figure

71. This is a side view of the TCAD model using a cut line down the center of the n-well. The potential of the model just following the ion strike is shown in Figure 72. There is a 1.2 V drop from the well contacts to the ion strike location in the n-well at this point. Figure 73 shows the potential at 125 ps after the ion strike. This plot shows that the well/substrate p-n junction has forward-biased, indicated by the similar color of the potential in both the n-well at the ion strike and the substrate. The substrate potential does not exhibit much change. This is primarily due to the model being based on an epi-substrate, which is verified later in another TCAD model.

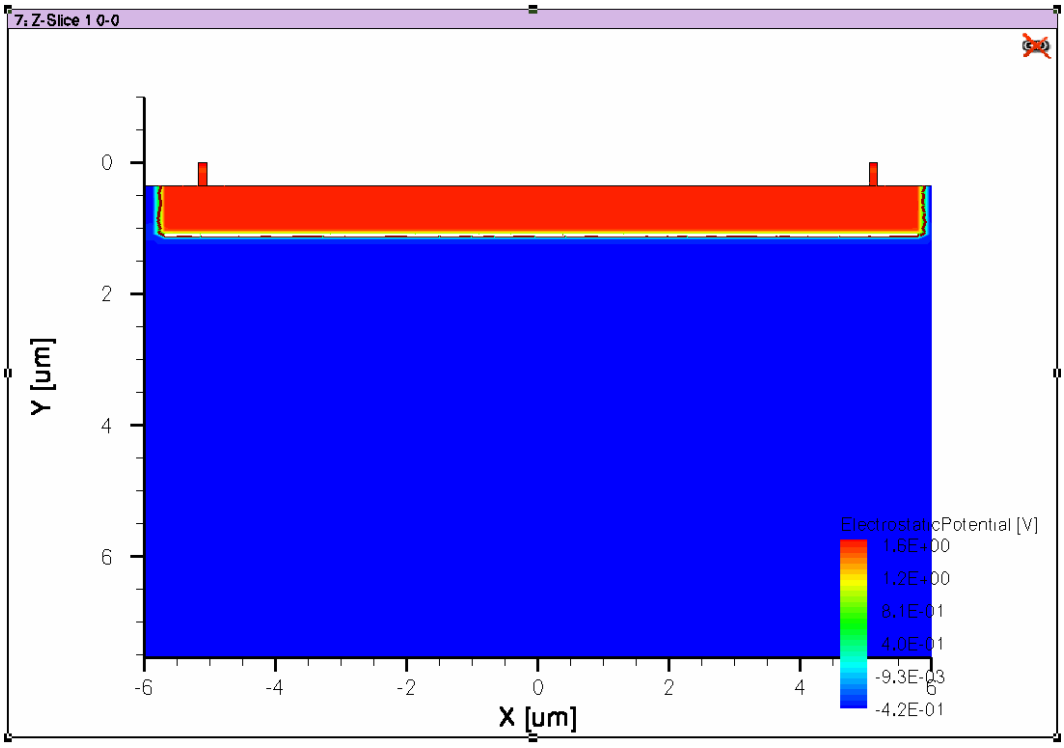



Figure 71. N-Well with No P+ Implant Model potential prior to ion strike.

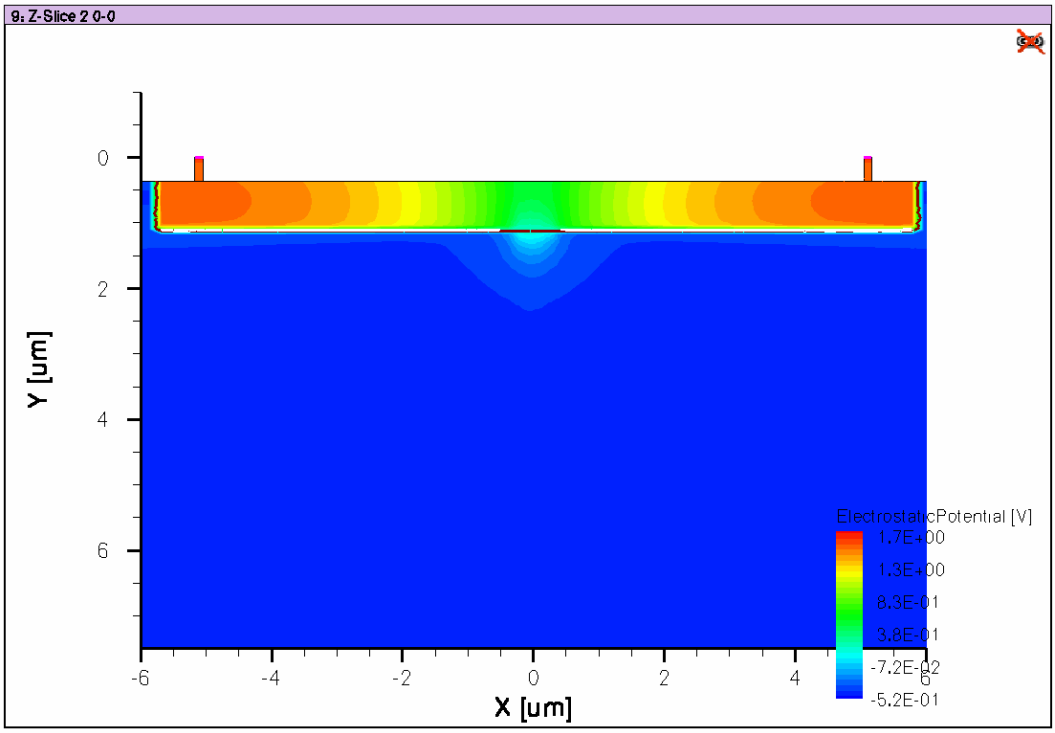



Figure 72. N-Well with No P+ Implant Model potential just after ion strike.

The hole density for this simulation is shown in Figure 74. This shows that minority carriers (holes) are being injected into the n-well under this condition. Lastly, Figure 75 compares Model 2 to the original SRAM TCAD model, showing the n-well currents that supply the single event current. Model 2 provides more current from the n-well contacts than the original SRAM model because a higher voltage drop occurs from the contact to the region of the well/substrate charge collection. However, the pulse width of the prompt charge collection is exactly the same. These simulations demonstrate that accurate modeling during single event current generation requires the sources to be included; the sources maintain the well potential and provide a source for the single event current.

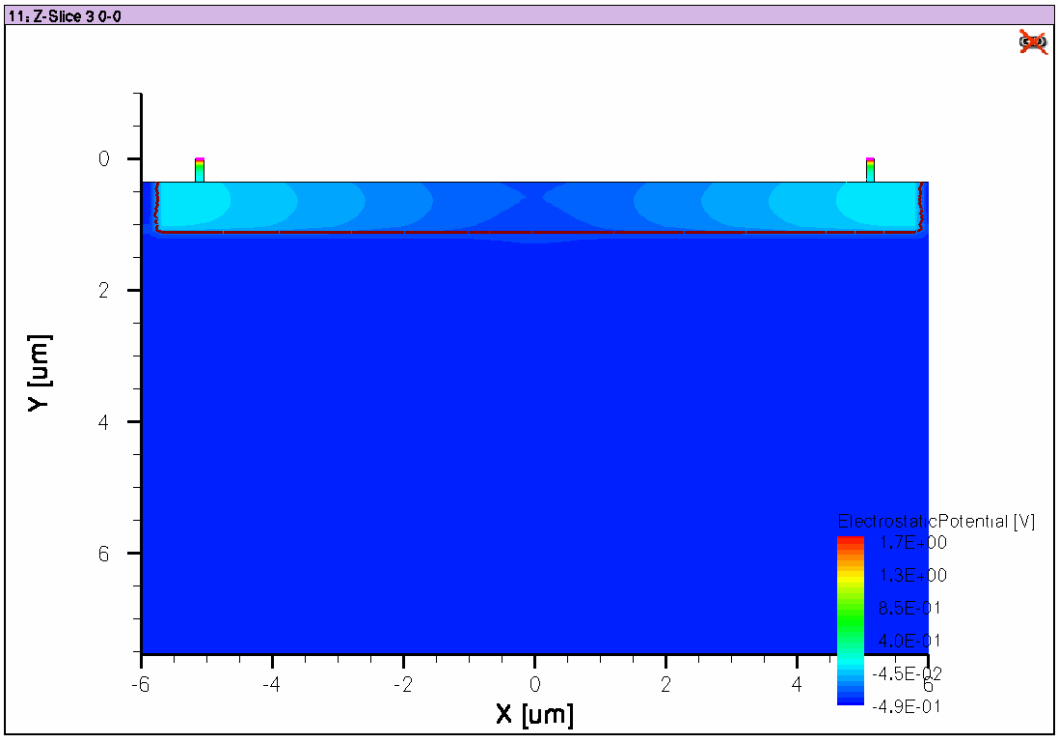



Figure 73. N-Well with No P+ Implant Model potential at 125 ps after ion strike.

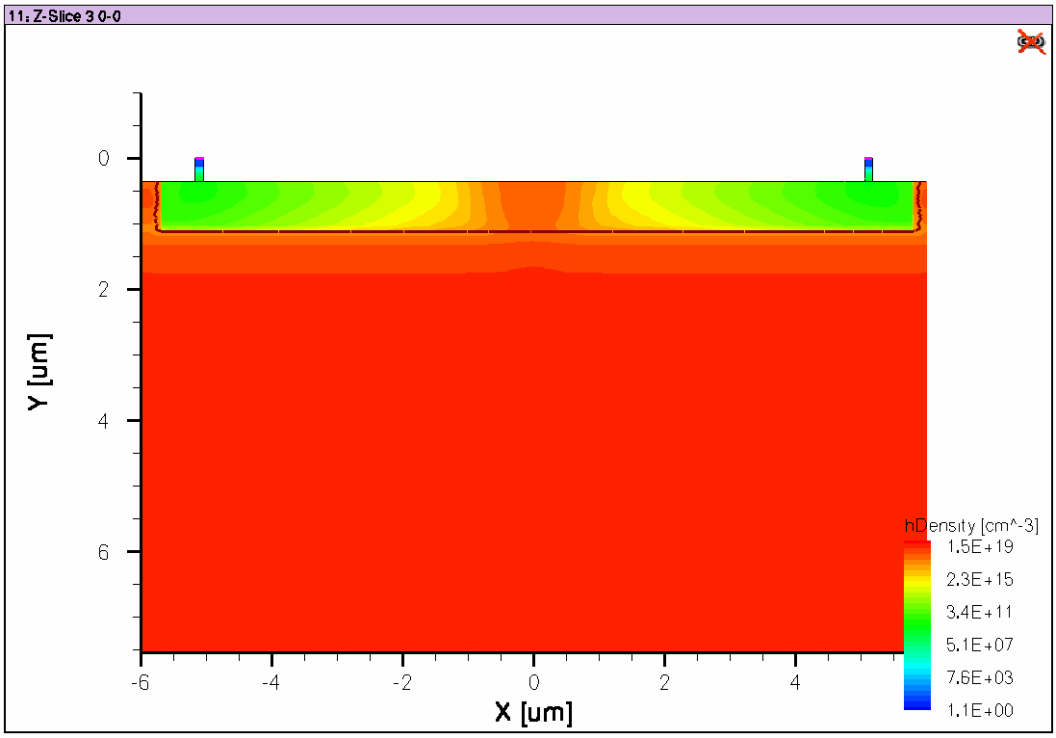



Figure 74. N-Well with No P+ Implant Model hole density at 125 ps after ion strike.

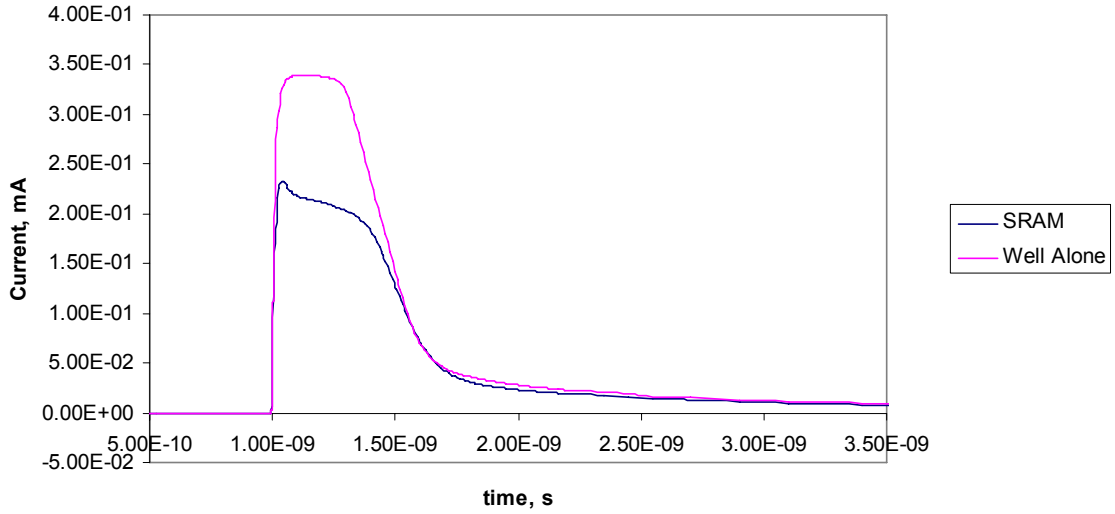



Figure 75. N-well current versus time for N-Well with No P+ Implant Model and SRAM Cell Model.

## Model 3: N-Well with P+-Sources Model

In Chapter IV, it was theorized that single event current for charge collection at the well/substrate p-n junction was supplied by well contacts and p+-sources in the n-well. The previous section further assumes that the p+-sources help to maintain the well potential, which limits the single event current supply from the well contacts. To examine these hypotheses, a TCAD model was produced of an n-well with p+-sources in the same positions as the pMOSFET source/drains from the original SRAM model. The purpose of Model 3 is to compare the single event response to the previous models to ensure that the p+-sources were responsible for maintaining the well potential. Also, Model 3 can verify whether the p+-sources were the first p-n junctions to forward-bias.

Figure 76 presents a side view of a pMOSFET in the n-well from the original SRAM model, showing the complex doping profile implemented in the model. The drain

is on the left in this figure and the source is on the right. Figure 77 shows how Model 3 differs. This model uses a flat doping profile so that it can easily be meshed in the TCAD tool. Since the pMOSFET has a more complex doping profile, it requires many more mesh points to model. So, the implementation of the flat doping profile will allow for more p+-sources to be implemented in a single TCAD model.

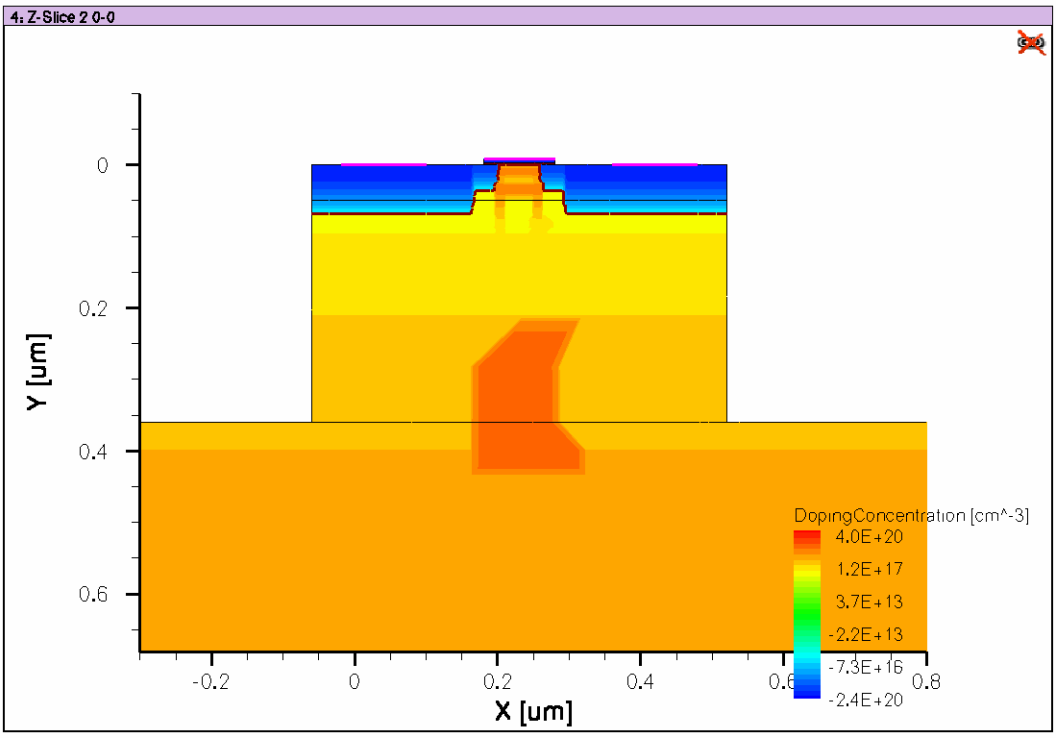



Figure 76. SRAM Cell Model pMOSFET side view showing drain (left) and source (right) in the n-well.

The top view of Model 3 is shown in Figure 78. The two p+ implants in the center apply the flat doping profile shown in Figure 77. The first step in the simulation was to calibrate the diode characteristics. The area for the p+-sources in this model exactly matches the area of the pMOSFETs in the original SRAM model, so the resistances from the junctions to the top of the well are identically modeled. The p+-source current during

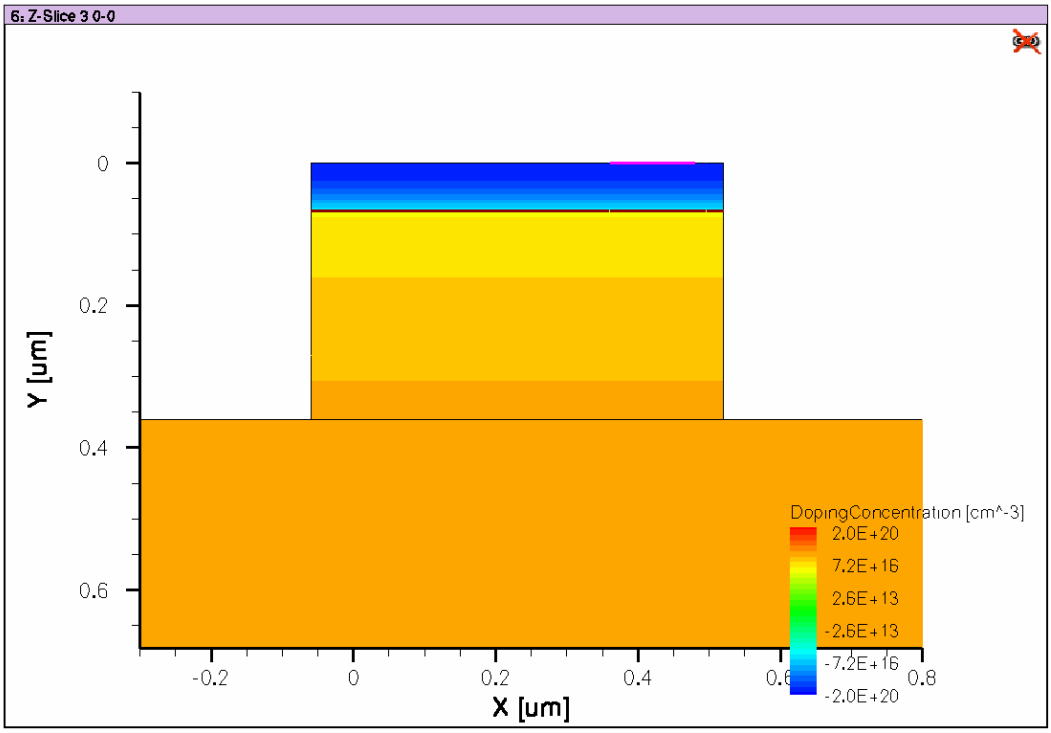



Figure 77. N-well with p+-source side view.

the single event current generation depends on the p+-n diode current density, the diode area, and the resistance. By using the same doping profile and resistance, the only parameter that differs between the original SRAM model and Model 3 is the diode area. The p+-source takes up about half of the area in the SRAM model, whereas the p+-source in the model in Figure 78 takes up the whole area. Thus, it was expected that the p+-source current could be off by a factor of two during the initial simulations.

Model 3 was calibrated by executing 20 single event simulations. The choices of the ion strike locations and charge deposition were matched to the original SRAM model data sets. A subset of those results is given in the next few figures using a charge deposition of 0.1 pC/μm. The first two sets of results are for normal ion strikes at Points A and B in Figure 78. A side-by-side comparison of the single event current sources for

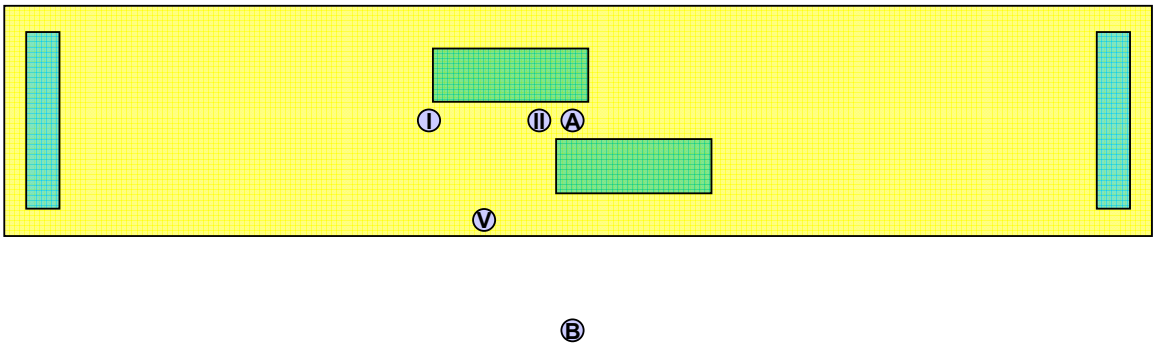



Figure 78. Top view of N-Well with P+-Sources Model showing sample ion strike locations.

Point A is shown in Figure 79. The n-well current is in good agreement, but the two sources show a difference in the current profile. In the case of modeling just the p+-sources, the two source currents are the same due to location of the ion strike. This is not the case for the original SRAM model, where the initial MOSFET operation of the transistors affects the current profile. However, the currents do not differ by a factor of two as expected; instead, there is approximately 25% difference in the currents for the MP1-source.

The side-by-side comparison for Point B is shown in Figure 80. This ion strike location corresponds to the OFF nMOSFET drain in the original SRAM model. As a result, there are some differences in the currents. In the SRAM model (left), the p+-source currents show a small perturbation and then enter forward-bias due to the direct charge collection. However, once the SRAM has exhibited the well-collapse source-injection mechanism, the overall current profiles appear similar. However, the initial perturbation in the original SRAM model causes differences at the maxima and in the timing between the two models. Since Model 3 includes a source/body diode with more than twice the area as the original SRAM model, it was anticipated that there might be factor of two difference between the source currents observed in the simulations.

However, the resistance from the source/body junction to the top of the well appears to be the dominant characteristic that determines the source current. The differences observed in these simulations are mainly due to the MOSFET operation in the SRAM model, which is not included in Model 3.

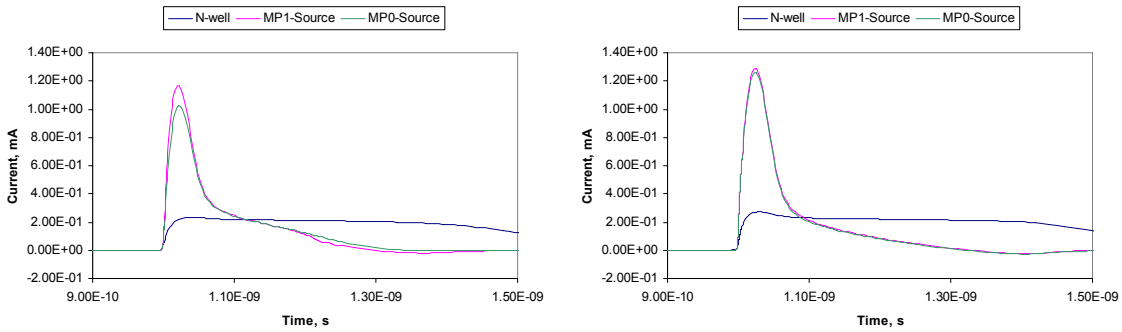



Figure 79. Side-by-side comparison of single event current sources during ion strike at center of SRAM Cell Model (left) and N-Well with P+-Sources Model (right) – point A in Figure 78.

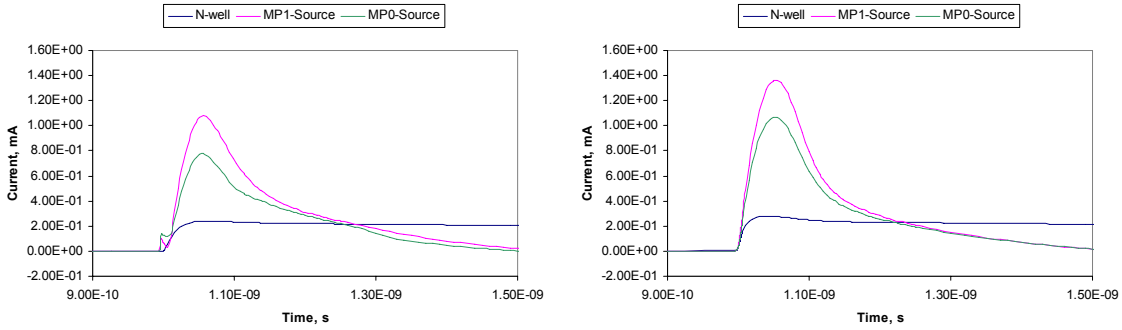



Figure 80. Side-by-side comparison of single event current sources during ion strike outside of the n-well for the SRAM Cell Model (left) and N-Well with P+-Sources Model (right) – point B in Figure 78.

Figure 81, Figure 82, and Figure 83 show current profiles for simulated ion strikes at Points I, II, and V, respectively, from Figure 78. These locations correspond to the same ion strikes provided in Figure 42. For all these cases, the current profiles match

very well between Model 3 and the original SRAM model. This is because the well-collapse source-injection mechanism dominates early in time. These plots verify that the diode area does not determine the forward-bias current during the prompt charge collection. Instead, the resistance between the p+-source and the top of the well is the determining characteristic. Following the prompt pulse of current, the curves differ, so diode area is important. Since SRAM upset is primarily based on prompt charge collection current overcoming the cell's restoring current, the model should match best in the prompt region. Thus, Model 3 is an accurate model for studying the well-collapse source-injection mechanism as long as the resistance from the p+-source to the well is modeled correctly. However, this model is not a great match when other mechanisms are significantly involved.

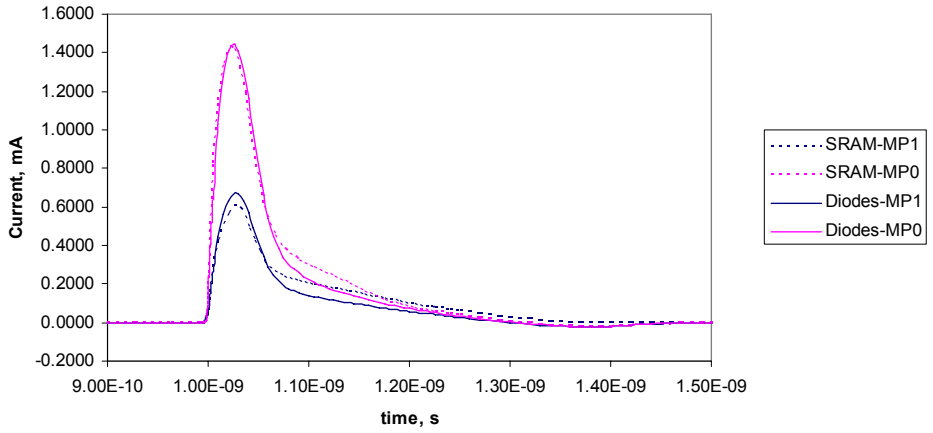



Figure 81. Comparison of single event current sources during ion strike at point I in Figure 78 for the SRAM Cell Model and N-Well with P+-Sources Model (diodes).

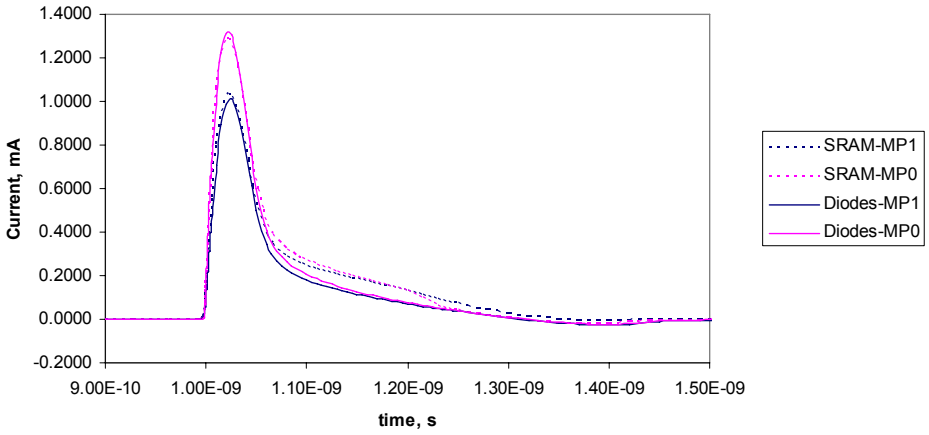



Figure 82. Comparison of single event current sources during ion strike at point II in Figure 78 for the SRAM Cell Model and N-Well with P+-Sources Model (diodes).

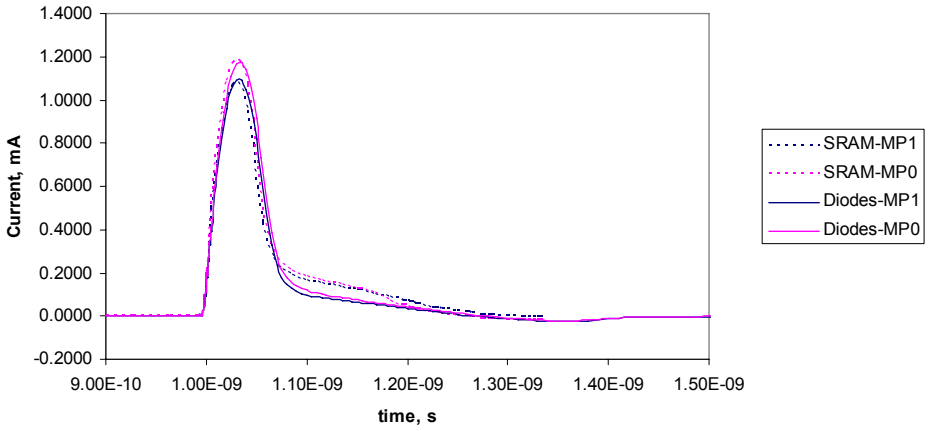



Figure 83. Comparison of single event current sources during ion strike at point V in Figure 78 for the SRAM Cell Model and N-Well with P+-Sources Model (diodes).

## Model 4: SRAM Array Model

### Model Description

The SRAM Array Model was proposed earlier in the discussion of the well-collapse source-injection mechanism. It is shown again in Figure 84. The previous

section demonstrated that the well-collapse source-injection mechanism can be simulated using p+-sources with a flat doping profile in the place of pMOSFET source/drains; therefore, this method was used to construct Model 4 in TCAD. This model contains the largest number of 3-D mesh points of any model used in the study, but all the p+-sources were modeled in the n-well. Replicating the original SRAM model is infeasible because it contains almost as many mesh points as required by Model 4. This new model enables the study of the well-collapse source-injection mechanism for an array of SRAM cells. Figure 85 shows the top view of Model 4 as implemented in TCAD. Several ion strike locations (Points A through E) were chosen to examine the response variation due to: (1) the distance to the well contacts and (2) the variation in strike angle.

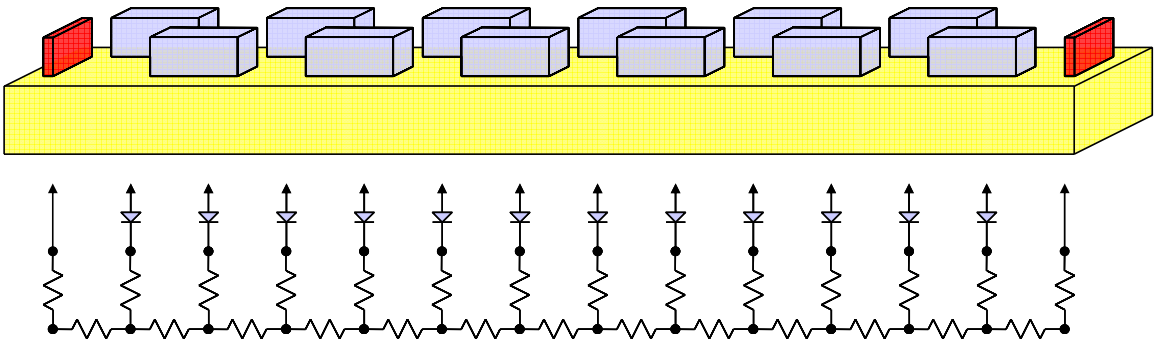


Figure 84. SRAM Array Model for eell-collapse source-injection mechanism study.

Upset Threshold Based on Forward-Bias Current

Since the original SRAM array model only provides the source currents as outputs, a threshold current value must be used to denote a cell upset. This value is used to observe the range of the well-collapse source-injection. Using the original SRAM model, a set of simulations was performed with normal ion strikes to the left of the

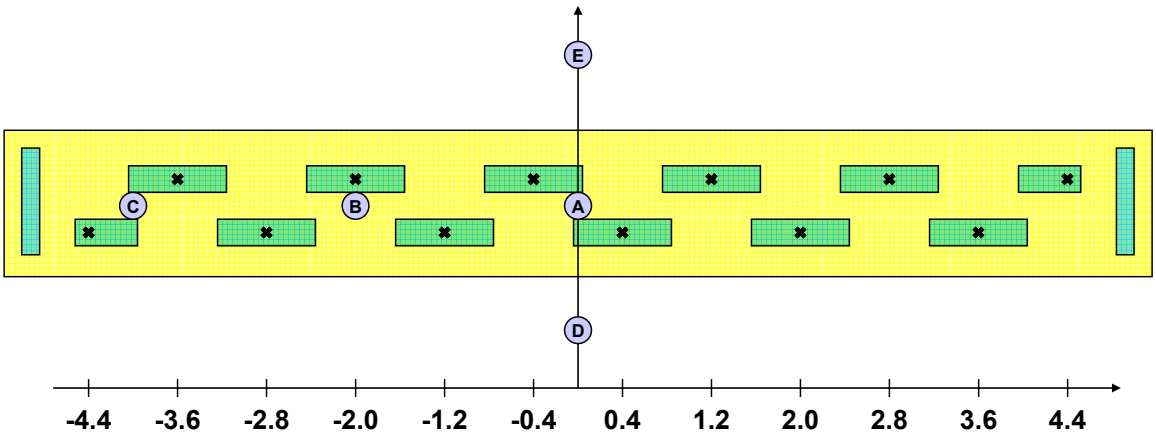



Figure 85. Top view of SRAM Array Model showing simulated ion strike locations. P+-source locations are marked with Xs and with hashes on the x-axis. The x-axis is in units of μm and referenced to the center of the model.

SRAM cell. The current for the OFF pMOSFET source was examined at the onset of cell upset. For an ion strike 1 μm to the left of the SRAM cell center, a charge deposition of approximately 0.066 pC/μm caused an upset. Figure 86 shows a plot of the node voltages and pMOSFET source currents for this case. From this simulation, the peak current for the OFF pMOSFET source (MP1-$I_s$) is slightly greater than 0.6 mA.

The charge deposition required to cause an upset at a distance of 2 μm to the left of the center of the SRAM cell is approximately 0.08 pC/μm. The plot of the SRAM node voltages and pMOSFET source currents is given in Figure 87. In this case, the peak current for the OFF pMOSFET source is just less than 0.6 mA. The current profile has a longer duration than shown in Figure 86. It was previously stated that simulations far away from the p+-source may not give accurate results due to the well-collapse enhancements. However, since the magnitude of the OFF pMOSFET source currents were both near 0.6 mA for upset, this will be considered the threshold for upset in the SRAM array model. This approximation is used because SRAM upset is primarily based

on the magnitude of the prompt charge collection to the OFF drain, which is related to the magnitude of the forward-bias current at the OFF source.

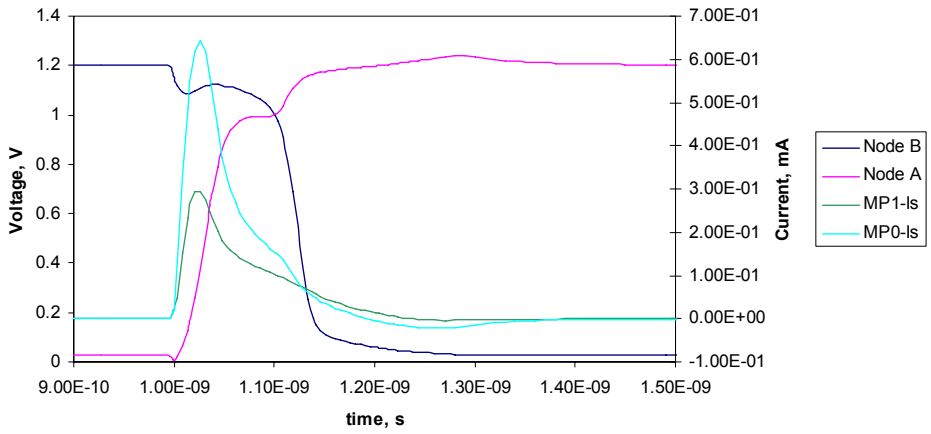



Figure 86. SRAM Cell Model node voltages and pMOSFET source currents for an ion strike 1 μm to the left of the center of the SRAM cell (0.066 pC/μm).

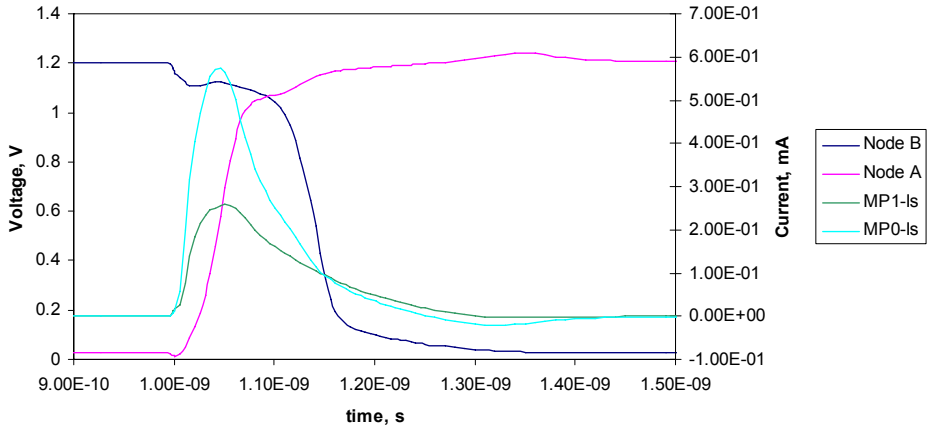



Figure 87. SRAM Cell Model node voltages and pMOSFET source currents for an ion strike 2 μm to the left of the center of the SRAM cell (0.08 pC/μm).

Simulation Results from Normal Ion Strikes

Figure 88 plots three different charge depositions at Point A from Figure 85. The data from the SRAM array model is presented by plotting the pMOSFET source currents versus their respective location in the well for each ion strike (i.e., a plot of the peak source current observed in the simulation). For a normal strike, a significant amount of charge deposition is required to cause more than the two center pMOSFETs to exceed the threshold condition. Figure 89 shows the simulation results for Point B, which is very close to a single pMOSFET source instead of being centered between two sources. This exhibits nearly the same shape as in the first case, except that three pMOSFETs exceed the threshold for the highest charge deposition simulated. The ion strike location nearest the well contact, Point C, showed some difference in the simulation (Figure 90). This location is similar to Point A in that it is exactly between two pMOSFET sources. However, since this location is near the well contact and near the well boundary, it has higher currents at the two closest pMOSFET sources. So, the charge deposition required to induce this mechanism would be slightly less at this point than in the center of the well. Also, the 0.05 pC/μm case never exceeded the threshold for these ion strikes. This is consistent with the SRAM cell model simulations.

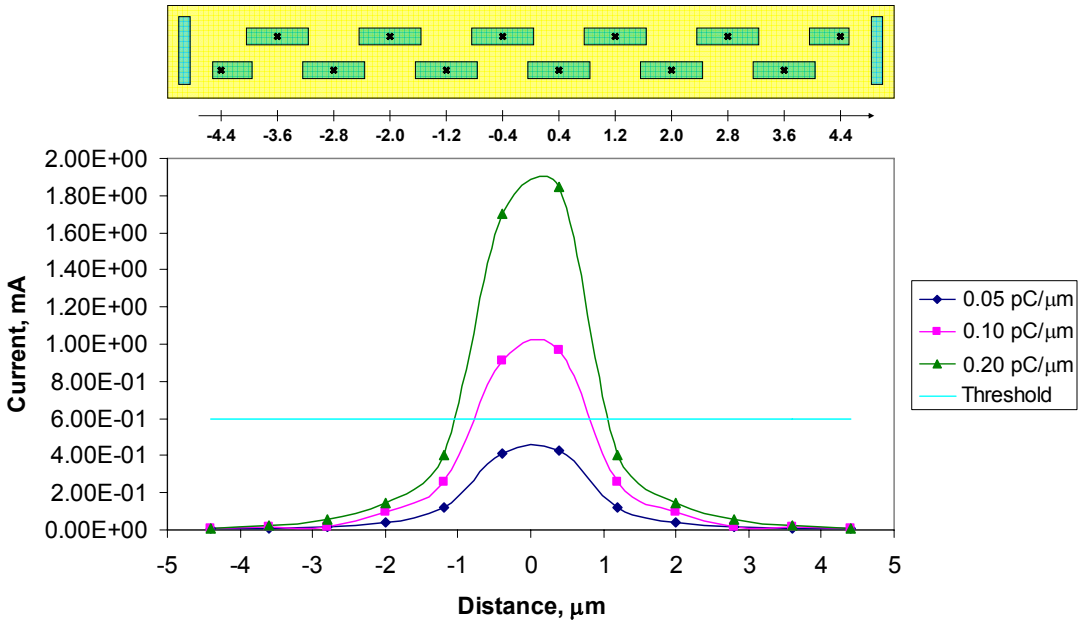



Figure 88. pMOSFET source currents for ion strike location A from Figure 85.

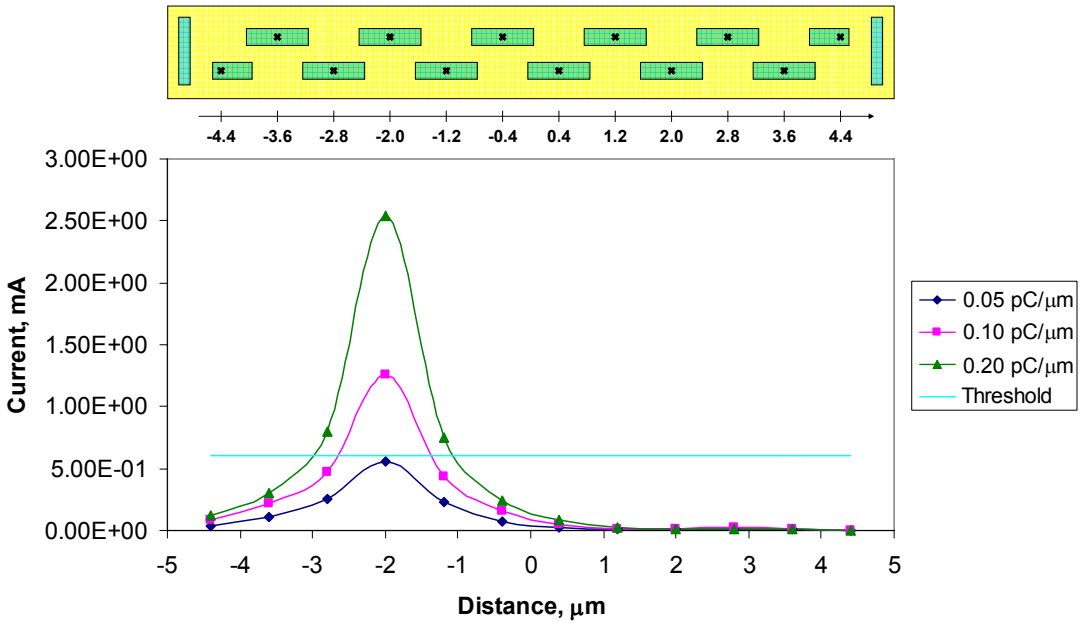



Figure 89. pMOSFET source currents for ion strike location B from Figure 85.

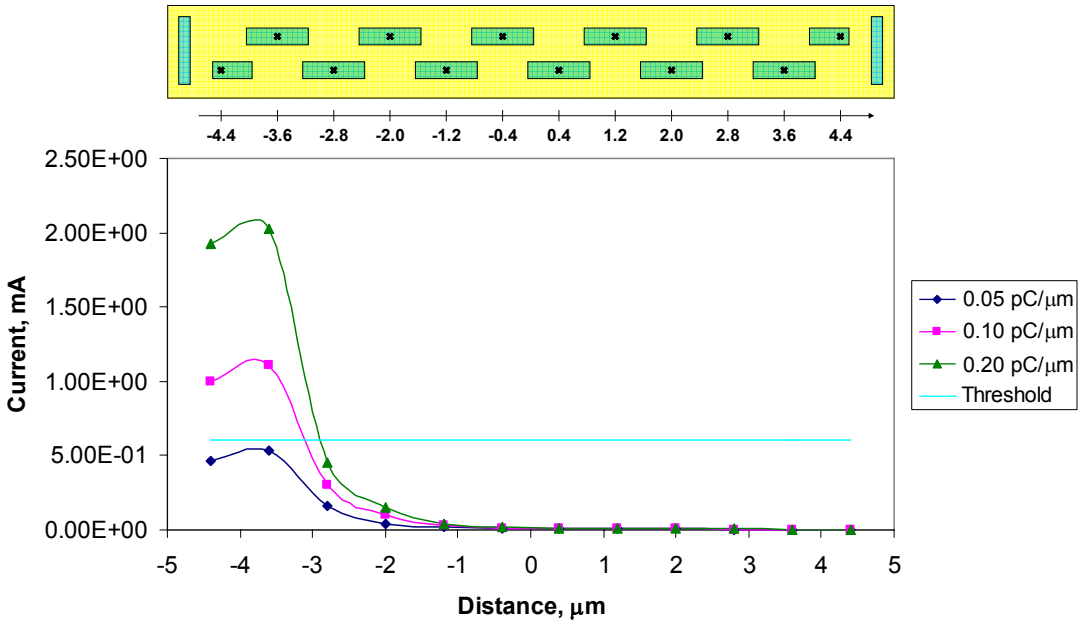



Figure 90. pMOSFET source currents for ion strike location C from Figure 85.

Simulation results from Model 4 are shown for an ion strike location outside the n-well (Figure 91). In this case, the resistance for the pMOSFET sources nearest that side of the well is less, at least for the sources in the center of the well. So, the data curve looks slightly different, though it exhibits some of the same basic qualities. There is still a falloff from the closer high current sources to the neighboring sources, and the width of the effect seems to track. This shows that normal ion strikes outside of the n-well, but near it, can induce well-collapse source-injection.

The main difference in the charge collection inside the well versus outside the well is the amount of surface area of the well/substrate p-n junction collecting the charge. For ion strikes inside the well, the holes generated inside the well can move to three nearby surfaces of the junction (bottom or the well and the two sides), while the electrons

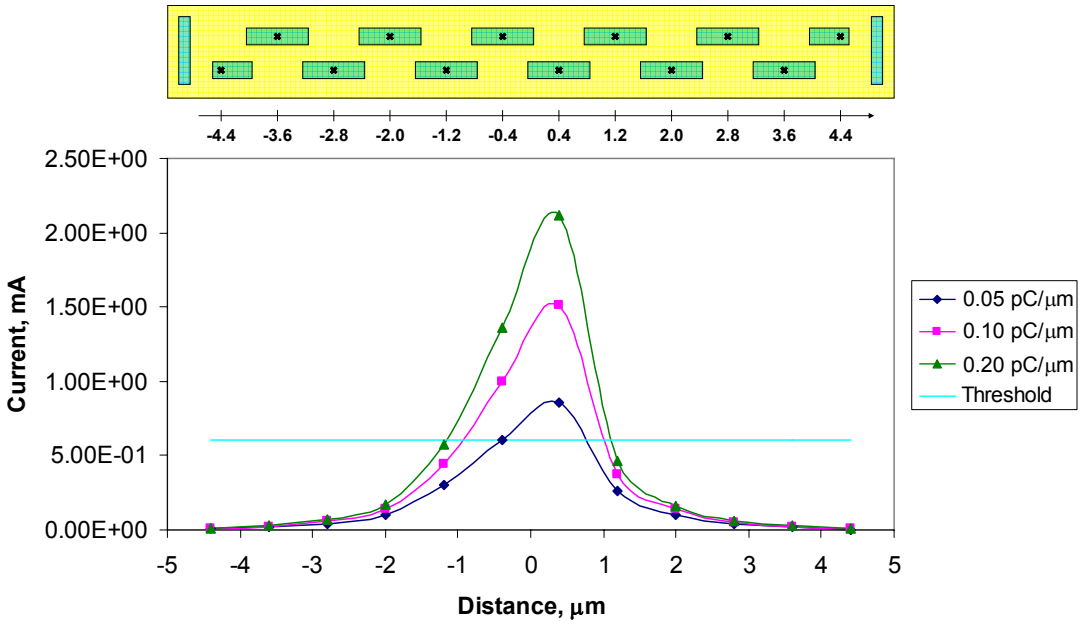



Figure 91. pMOSFET source currents for ion strike location D from Figure 85.

generated outside the well can move generally to one surface of the junction (bottom of the well). On the other hand, for ion strikes outside of the well, only the electrons generated outside the well contribute to the charge collection, though two surfaces may collect (the side nearest the ion strike and the bottom of the well). For the simulations at Point A and Point D, there is an approximate 75% difference in the charge collection when considering the well-collapse source-injection mechanism.

Simulation Results from Angled Ion Strikes

The next set of simulations examine the effect of angular ion strikes to induce the well-collapse source-injection mechanism. It is expected that ion strikes angled in the direction of the well will follow effective LET theory [Ko84]. So, ion strikes at a $60^{o}$ angle will deposit twice as many holes inside the well and twice as many electrons

outside of the well for charge collection at the well/substrate p-n junction. Ion strikes angled perpendicular to the well should not follow this trend. The well is narrow in this dimension, and ion strikes that exit the well are going to be moving away rapidly from the well/substrate p-n junction. The holes generated within the well should match the path length of the ion through the well, but the electrons collected at the junction will depend upon where the charge track leaves the well.

Figure 92 and Figure 93 show simulation results for angled ion strikes at Point A and Point D respectively (Figure 85). The points represent where the ion enters at the top of the well. The ion path forms an angle of $60^{o}$ from normal to the surface in a negative X direction (i.e., to the left). These strikes show a significant increase in the range of the well-collapse source-injection mechanism. At this angle, the number of pMOSFET sources that exceed the threshold is much higher. This is observed for the both the angled ion strike inside the well and outside of it. The main difference in these simulations is that for angled ion strike outside the well, the location of the peak pMOSFET source current stays the same. For the angled ion strikes inside the well, the peak shifted from the point of well exit for the smallest charge deposition to the point of well entry for the highest charge deposition.

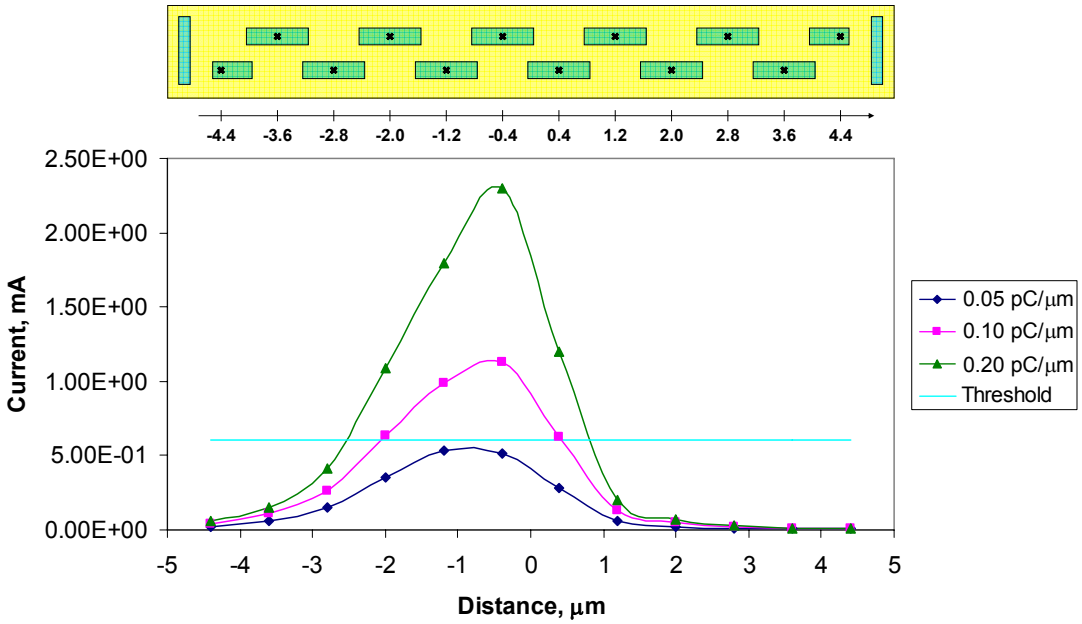



Figure 92. pMOSFET source currents for ion strike location A from Figure 85 at an incident angle 60° from normal to the surface traveling in a negative x direction.

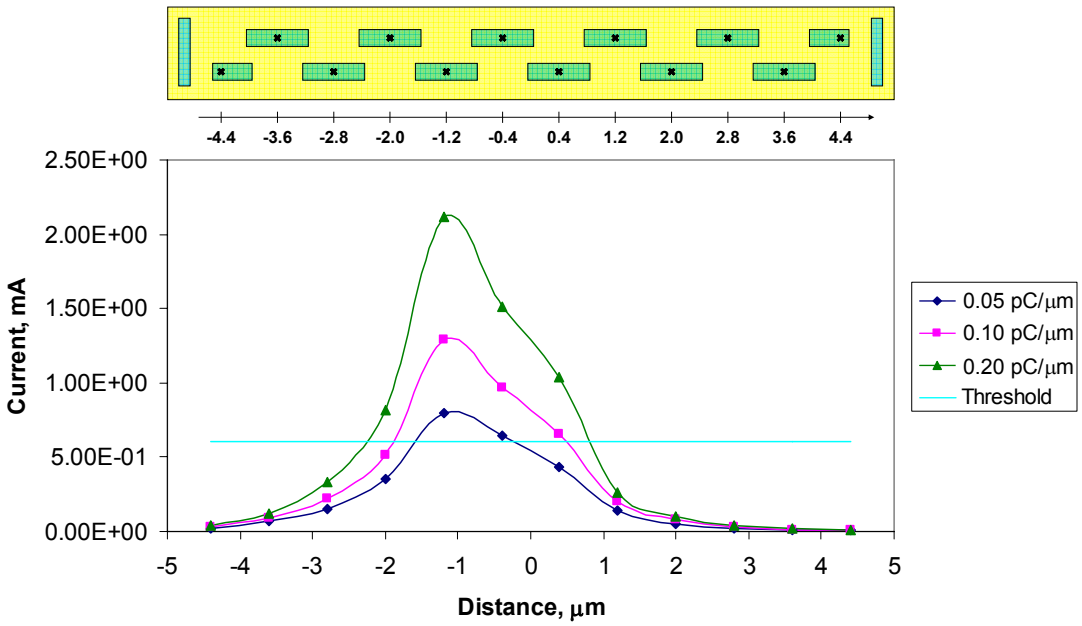



Figure 93. pMOSFET source currents for ion strike location D from Figure 85 at an incident angle 60° from normal to the surface traveling in a negative x direction.

Simulations of angled ion strikes with a direction perpendicular to the well (negative Y direction on Figure 85) were performed at Points A and E. At an angle of incidence of $60^{o}$ to normal, the path length of the ion through the well is approximately 0.52 μm for Point A and approximately 1.03 μm for Point E. The path length in the well for normal ion strikes is 0.76 μm. The angled simulations from Point A should have less forward-bias current than the normal ion strike at Point A, which in turn, should be less than the forward-bias current for the angled ion strike at Point E. The simulation results for the angled ion strikes in the negative Y direction are given in Figure 94 for Point A and Figure 95 for Point E. The results for Point A are not as expected. The forward-bias currents at the two center p+-sources are higher than the normal ion strike at Point A. However, the forward-bias currents are lower for the rest of the p+-sources. This occurs because the charge collection of the well-substrate p-n junction is located at the side of the n-well rather than at the bottom. The resistive path for the two center sources is less for the charge collection at the side of the n-well than at the bottom. On the other hand, the simulation results for Point E follow the path length argument. The path of this particular ion exits the n-well near its bottom, so the resistance to the well/substrate charge collection is similar to the normal ion strike location.

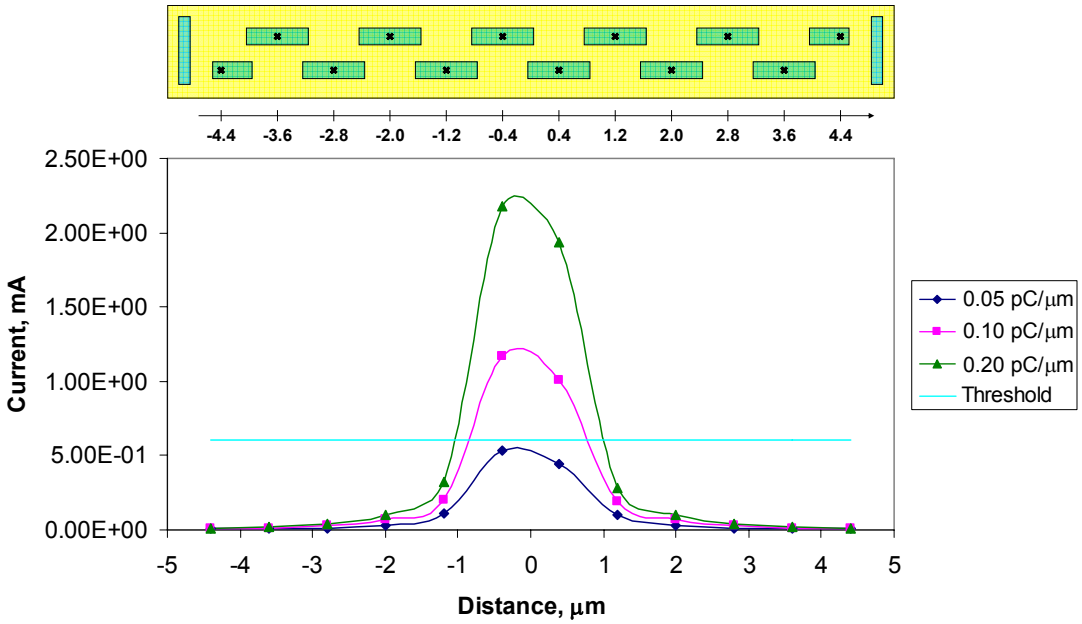



Figure 94. pMOSFET source currents for ion strike location A from Figure 85 at an incident angle 60° from normal to the surface traveling in a negative y direction.

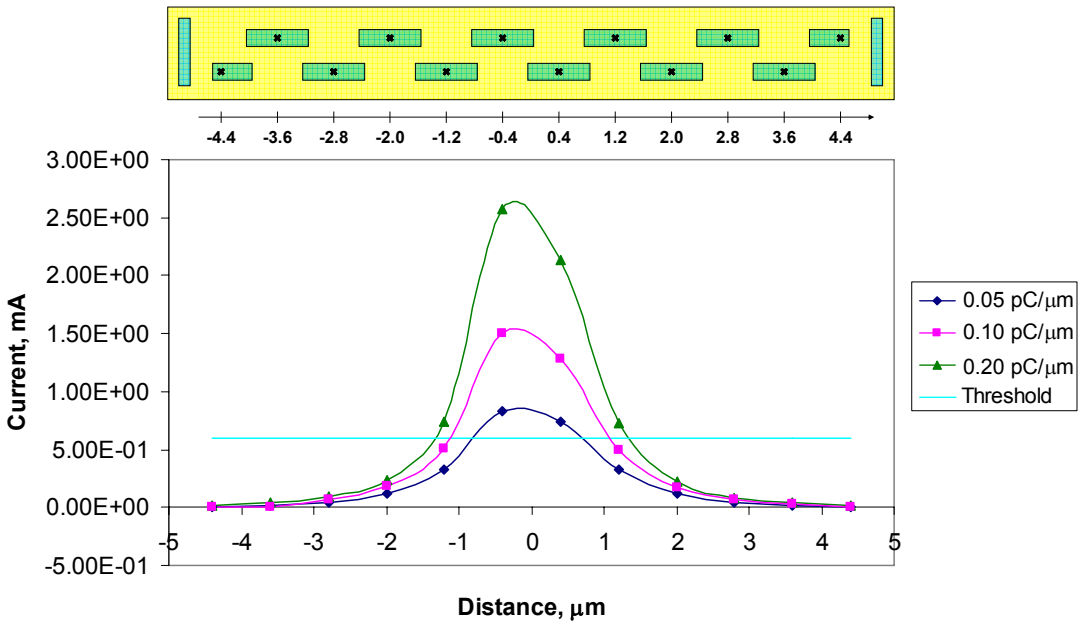



Figure 95. pMOSFET source currents for ion strike location E from Figure 85 at an incident angle 60° from normal to the surface traveling in a negative y direction.

Well Potential and Minority Carrier Density

Beyond observing the range of the well-collapse source-injection mechanism, the SRAM array model also provide an interesting look at the potentials and the minority carriers in the n-well. The next three figures show TCAD simulation plots for a normal ion strike at Point A with a charge deposition of 0.05 pC/µm. Figure 96 shows the top view, and Figure 97 shows the side view for the potential in the TCAD model. There is some voltage drop from Point A to the well contacts. However, all of the p+-sources are forward-biased and aid in holding the well potential so that the well/substrate p-n junction does not forward-bias. Figure 98 shows the side view of the hole density. This shows that holes are being injected from each p+-source, though the p+-sources in the middle are providing the most. This is the indicator of the well-collapse source-injection mechanism.

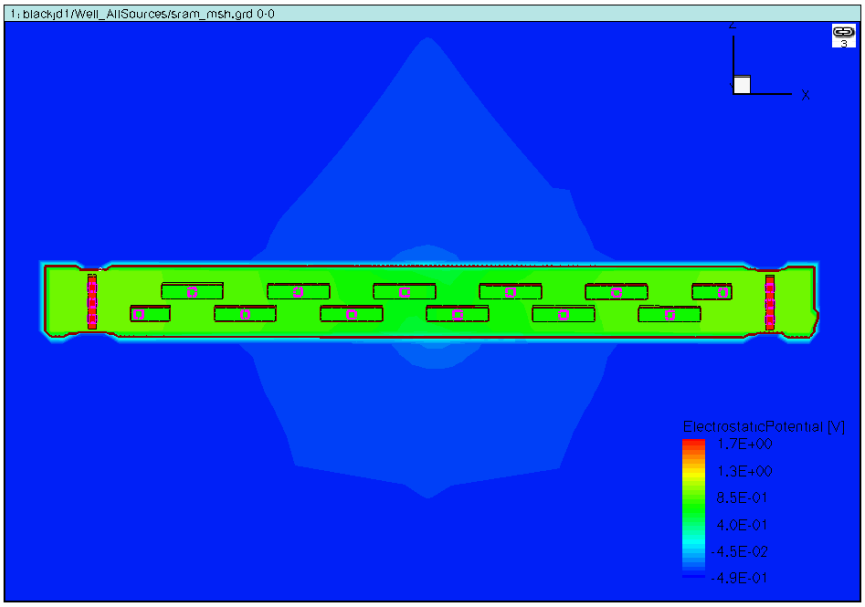



Figure 96. Top view of SRAM Array Model showing potential 50 ps following a normal ion strike at location A with a charge deposition of 0.05 pC/µm.

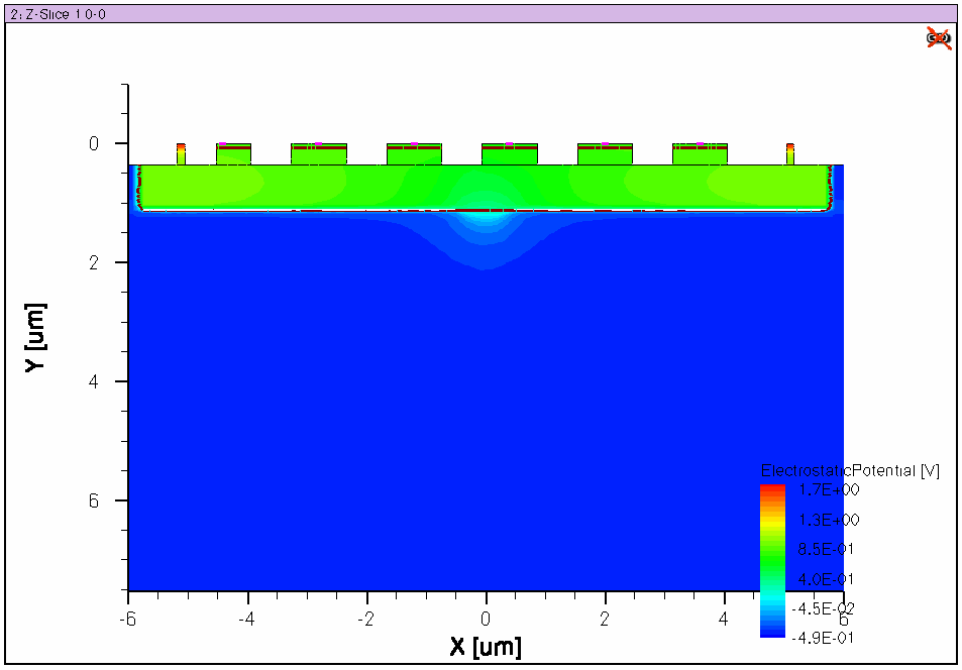



Figure 97. Side view of SRAM Array Model showing potential 50 ps following a normal ion strike at location A with a charge deposition of 0.05 pC/µm.

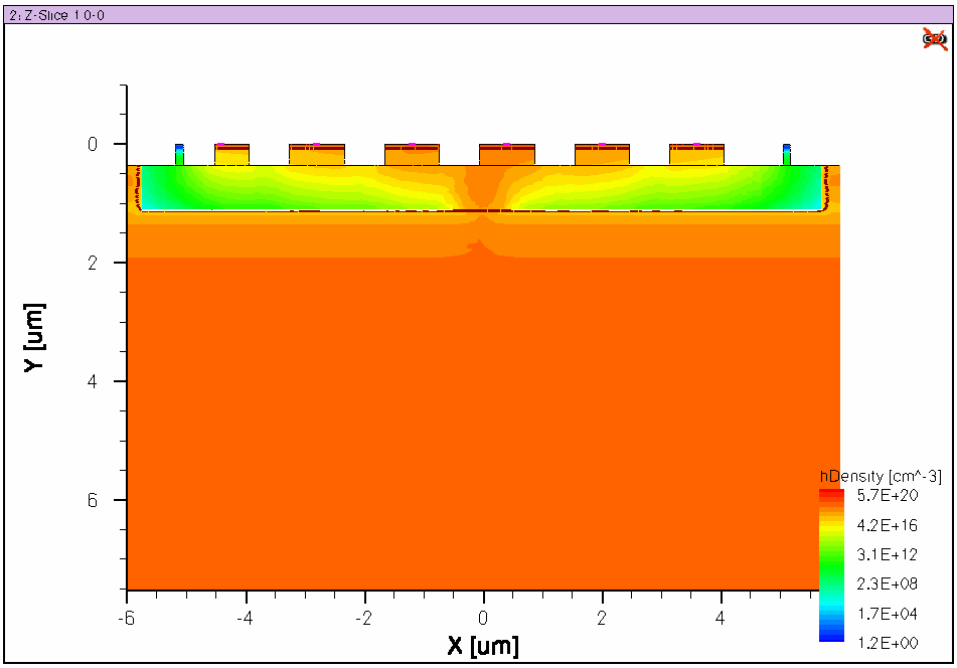



Figure 98. Side view of SRAM Array Model showing hole density 50 ps following a normal ion strike at location A with a charge deposition of 0.05 pC/µm.

## Model 5: Electron Diffusion TCAD Model

Models 1 to 4 represent the focus of the research in this dissertation with Model 4 representing the culmination of all the other models. The last two models were developed to answer questions that came up in the study. Model 5 examines the diffusion of carriers following an ion strike. The purpose of the model is to compare the charge collection mechanisms of PBE and well-collapse source-injection. This model also provided insight into which deposited carriers contribute to prompt charge collection. Finally, Model 4 examines the characteristics of charge transport for the long/thin semiconductor areas above the substrate containing the nMOSFETs shown in the SRAM array layout (Figure 62).

One component of direct charge collection that has not been included in the previous models is the diffusion of the minority carriers. Diffusion of carriers is a well-known process, but the diffusion following an ion strike is a very complex process involving very high diffusion gradients, ambipolar diffusion, and complex 3-D structures with boundary conditions. To briefly study the diffusion of minority carriers, a TCAD model was constructed with no p-n junctions. Figure 99 depicts the TCAD model used to study the electron diffusion. The areas above the substrate are where the nMOSFETs would be located in the SRAM array for two adjacent rows. The height of this region is normally 360 nm with a number of p-n junctions 260 nm above the substrate. Since there are no p-n junctions implemented in the model, the height was raised to 10 μm to allow the carriers to move as though they were swept across the junction electric field. It is noted that this is not an ideal TCAD simulation, but it will provide insight into the carrier motion and range of diffusion.

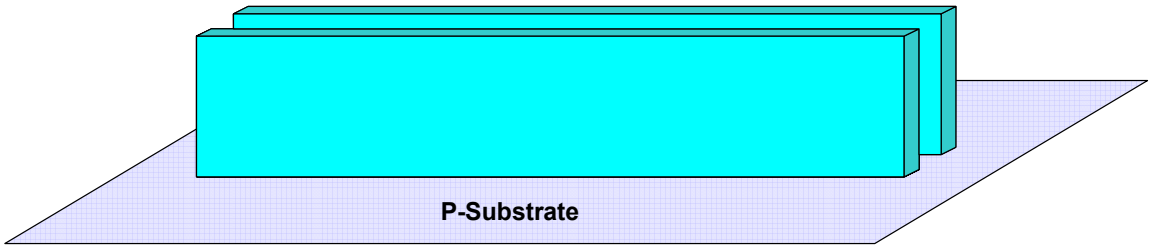



Figure 99. Electron Diffusion TCAD Model.

Model 5 was used with normal ion strikes in the substrate between the two raised semiconductor areas. Figure 100 shows a plot of the electron density just after an ion strike with charge deposition of 0.05 pC/μm. This plot is a cut line in the substrate between the two raised areas, and only shows the carriers in the substrate itself. Figure 101 shows the same plot 50 ps later in time. It is observed that the electrons have spread out slightly, but most of the electrons are still very close to the ion strike. The electron density falls off one order of magnitude at a radius of 0.6 μm and two orders of magnitude at a radius of 0.8 μm. This means that 90% of the excess electrons are within 0.6 μm of the charge track, and 99% of them are within 0.8 μm of the charge track for the prompt charge collection. So, this provides an indication of how close generated carriers must be to p-n junctions to contribute to prompt single event current. Since all the p+-sources in Model 4 are forward-biased, some of which are located more than 8 μm from the ion strike, it is not realistic to consider this to be the result of PBE. Instead, the well-collapse source-injection mechanism is the best explanation for the charge collection at those locations.

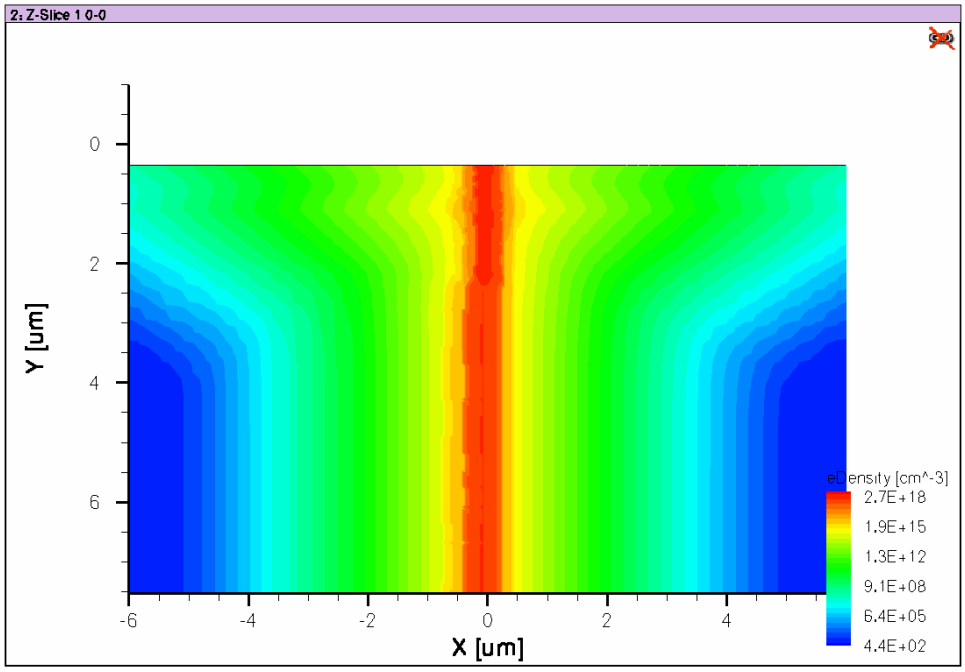



Figure 100. Electron density immediately after ion strike to substrate centered between the two raised semiconductor areas (0.05 pC/μm).

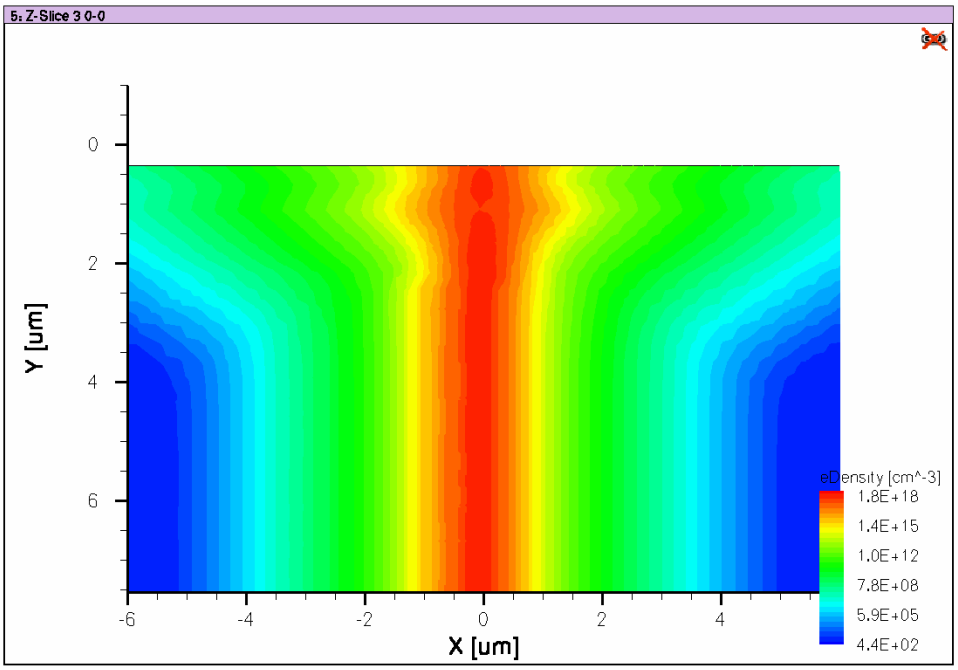



Figure 101. Electron density 50 ps following ion strike to substrate centered between the two raised semiconductor areas (0.05 pC/μm).

Another aspect of this simulation is the propagation of the electrons to the p-type semiconductor regions above the substrate. Figure 102 shows the electron density for a cut line that includes one of the two narrow regions. This shows how the boundary conditions participate in the motion of the electrons. The direction into the paper is the narrow direction. Since the carriers are reflected at this boundary, the density lines form generally in the vertical direction. This also shows that 10 μm of height of the semiconductor above the substrate may not be enough to reduce the effect of a non-physical boundary in that dimension.

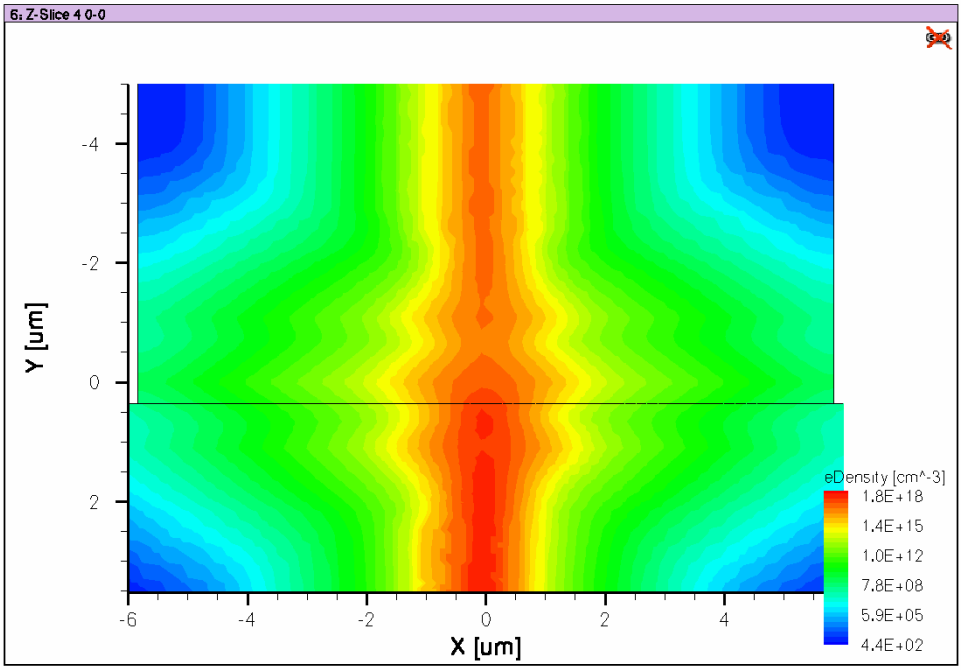



Figure 102. Electron density 50 ps following ion strike to substrate centered between the two raised semiconductor areas (0.05 pC/μm). Cut line now includes one of the raised semiconductor areas.

Other sets of simulations were performed using the model for strikes in a raised semiconductor region to look at angular ion strikes. Figure 103 shows an electron density

plot using the same cut line as Figure 102 for an ion strike in that region at an incident angle of 60°. The charge track is drawn in this figure to show the starting point and the direction. The starting point is the physical location of the top of the semiconductor. This shows the same general characteristics as the previous examples. All of the simulation results provided from this model are as expected, and they provide insight as to the range of carriers that can contribute to prompt charge collection.

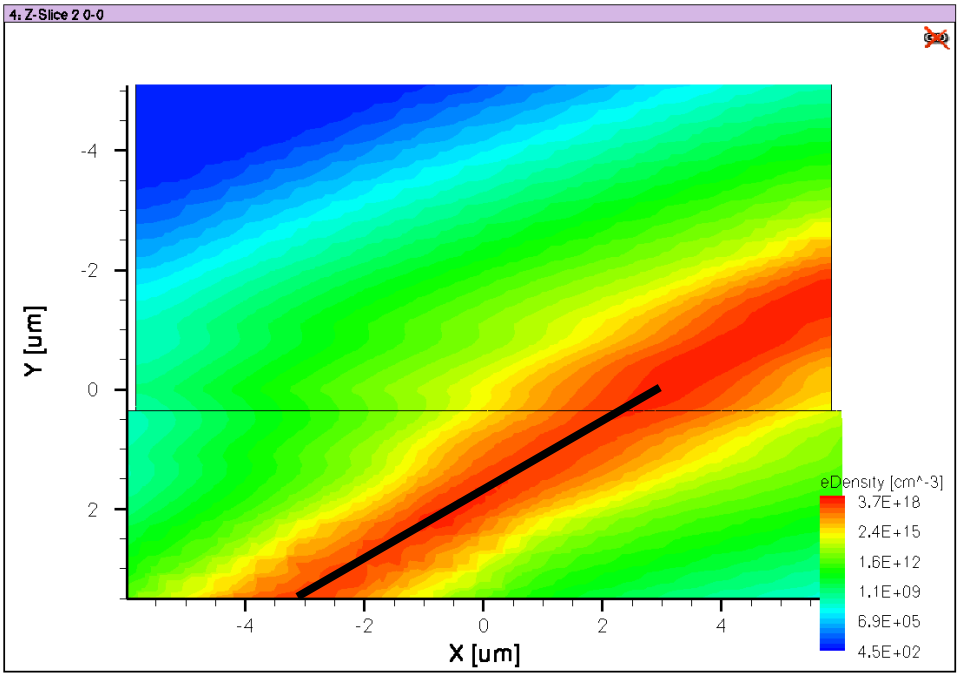



Figure 103. Electron density 50 ps following angled ion strike to substrate In one of the raised semiconductor areas (0.05 pC/µm). Cut line includes one of the raised semiconductor areas.

## Model 6: No Epi-Substrate Models

An issue that occurred when reviewing the test data presented in the next chapter was that the SRAM evaluated was not manufactured on an epi-substrate. A few models were developed to analyze the difference in the SRAM cell and array response due to a different substrate material. Model 2 was updated to examine this response. With the epi-

substrate, the substrate potential was not affected much with the simulation of an ion strike. After replacing the substrate with lower doped material, removing the large substrate contact at the bottom of the model, and adding substrate contacts similar to the well contacts, it was determined that the substrate potential near the ion strike did change significantly. Since the well-collapse source-injection mechanism is based upon the well-collapse, the fact that the substrate potential raises will obviously impact the mechanism.

To gauge how much effect the application of a lower doped substrate might have, Model 4 was rebuilt. Since this model does not contain n+-sources in the p-substrate, there is nothing to control the substrate potential. However, the SRAM array model with the epi-substrate is the extreme case where the substrate potential cannot change much, and the SRAM array model without the epi-substrate and with no n+-sources is the other extreme case where the substrate potential can change the most. So, the actual result will be somewhere in the middle. The reason n+-sources were not implemented is that the model was already the maximum size possible.

Simulation results for the updated SRAM array model without an epi-substrate are shown in Figure 104. This demonstrates that the p+-sources still forward-bias, just that the forward-bias current is lower. The difference between the two SRAM array models is more than a factor of ten. This difference means that the crossover point between direct charge collection and well-collapse source-injection may occur at a higher charge deposition for the lower doped substrate than for the epi-substrate. But, the well-collapse source-injection mechanism will still be observed.

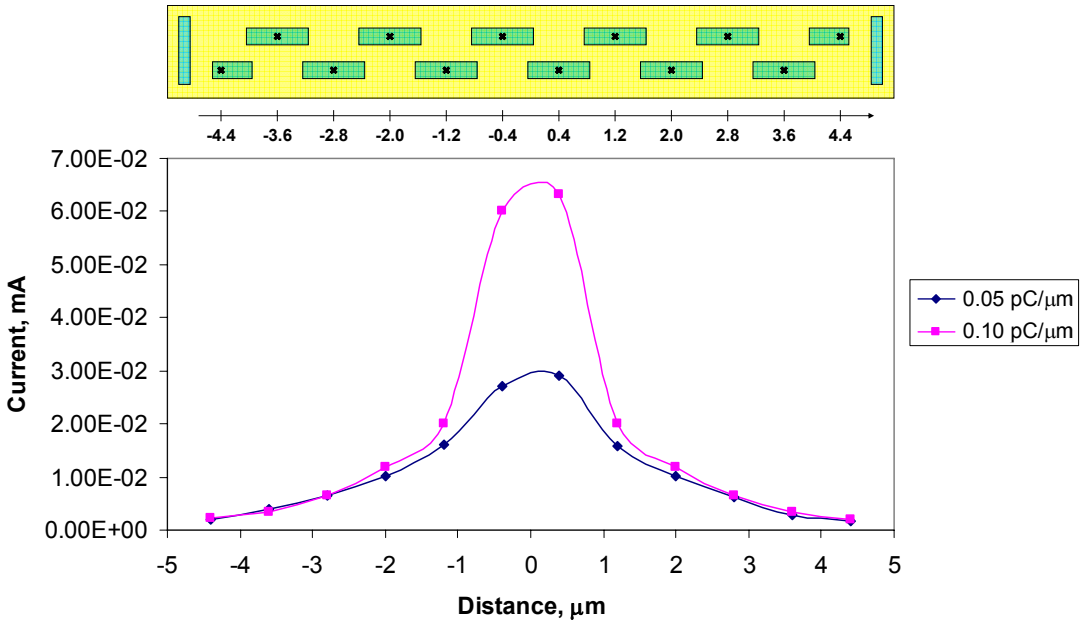



Figure 104. pMOSFET source currents for ion strike location A from Figure 85 with a low doped p-substrate.

# CHAPTER VIII

# EXPERIMENTAL RESULTS OF SINGLE EVENT EFFECTS IN STATIC RANDOM ACCESS MEMORY

The previous chapter detailed the modeling of the well-collapse source-injection mechanism and centered around a 90-nm SRAM cell design on an epi-substrate. However, all of the analysis is applicable to the general class of SRAM SEU analysis when the SRAM is implemented on an STI process with various substrates. Certainly, the mechanism will be easier to observe on designs that use an epi-substrate with the smallest available feature sizes. The best available SRAM to compare to the well-collapse source-injection mechanism was a small test array of 65-nm SRAM cells designed by Texas Instruments (TI). This represents the smallest feature size available for study where the mapping of the cells (i.e., data bits) is known by row and column address.

## SRAM Test Chip Overview

This section will present a few details of the TI SRAM cell and array design in order to interpret the set of data. It is not a complete description of the SRAM cell, SRAM array, or processing technology, as those items are proprietary. For the purposes of this dissertation, it is enough to know that the 65-nm SRAM cell layout is similar to the 90-nm SRAM cell layout (Figure 28) that was investigated. The similarity lies in the locations of the MOSFETs with respect to the n-well, with the two nMOSFETs being on

either side of the n-well. As a result, the MCU patterns that were developed in Chapter VI should apply to this test chip.

The topology of the TI SRAM test chip is shown in Figure 105. The rows addressed by the row address bits are numbered in consecutive order from bottom to top. The 16 data bits form the major division in the other dimension. Figure 106 shows the division of the data bits into 32 columns. This also shows the orientation of BL and $\overline{BL}$ with respect to adjoining columns. Finally, this figure shows the orientation of the n-wells with respect to row and column addressing. It is also noted that the rows and columns are not continuous. There are well and substrate contacts at specific intervals of rows. The data bits are also divided into a left and right memory bank.

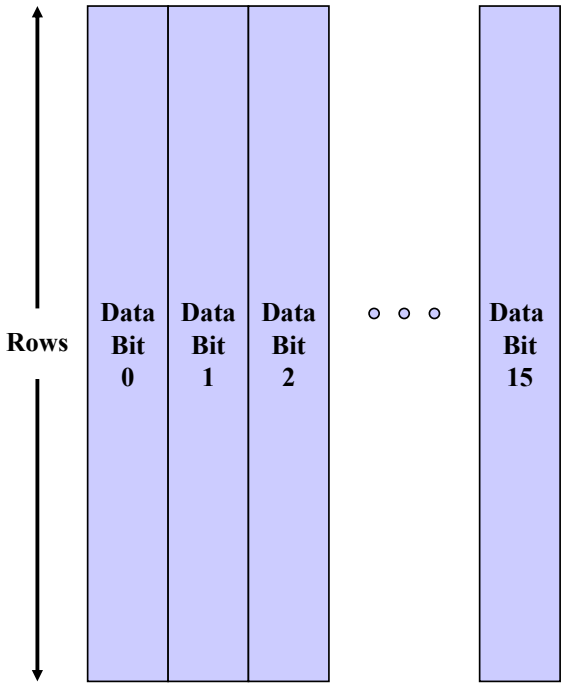



Figure 105. TI SRAM test chip topology – top level.

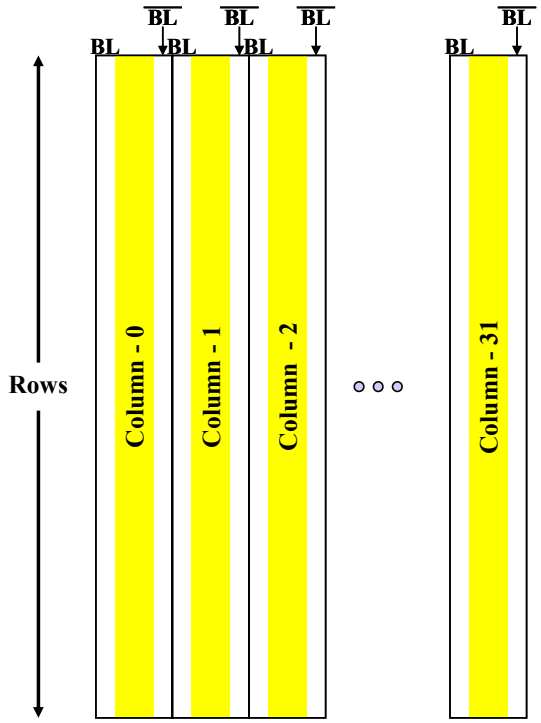



Figure 106. TI SRAM test chip topology – second level.

Two important items need to be considered concerning test patterns written into the TI SRAM array. First, if the same 16-bit word is written into all the row and column address locations, some effects may not be observable. Consider the nMOSFETs between columns 0 and 1 in Figure 106. If the data written in all these SRAM cells are the same, then the tops of each cell will hold the ON (OFF) nMOSFET and the bottom of the cell will hold the OFF (ON) nMOSFET. Thus, there is no way for two adjacent columns to have the adjoining nMOSFETs both OFF. The only difference will be in the transition from one data bit to the next in the topology. If opposite states are written into successive data bits, then the end columns will either have two OFF nMOSFETs or two ON nMOSFETS. The second important item to consider is the writing of alternating patterns

down the well as proposed in Chapter VI. This requires that the data bits be alternated every other row.

There is one other characteristic of the TI SRAM array that is important. The test design allows independent voltage supply to the n-well contacts and to the $V_{DD}$ connected to the p+-sources. This option was included to minimize standby current in the array by enabling the pMOSFETs to have a negative gate voltage with respect to the body. As a result, SEU or MCU variation can be observed by changing the well bias with respect to $V_{DD}$.

## Heavy Ion Tests

The TI SRAM test chip has been evaluated for heavy ion single event effects in cyclotrons at both Texas Agricultural and Mechanical University (TAMU) and Lawrence Berkeley National Laboratories (LBNL). The TAMU testing was conducted by personnel from the National Aeronautics and Space Administration Goddard Space Flight Center (NASA-GSFC) and their contractors. The LBNL testing was conducted by Vanderbilt University. Jeffrey Black and Alan Tipton led the testing, and Dr. Robert Reed and Estevan Bunker provided testing support.

Both sets of tests used the same hardware/software to control the testing, though difference devices were used for each test. The hardware used to control the testing was the NASA-GSFC Spartan-3 Field Programmable Gate Array (FPGA) Low Cost Tester [Ho06] board with a daughter card containing the SRAM device under test. The SRAM is programmed and read via the FPGA that is controlled through a computer serial port. The serial data stream defines when the SRAM is written and/or read as well as returns the

locations of incorrect (upset) data bits. The FPGA firmware and the Labview control software were both developed by NASA-GSFC. Due to the nature of the test hardware, all the row and column addresses were written with the same data pattern. The primary data pattern used and analyzed alternated between logic high and logic low in the data bits.

The procedures were similar for the TAMU and LBNL tests. The list that follows is the procedure that was followed at LBNL.

1. Select ion and particle flux and calibrate the dosimeters. Repeat this step a few times to observe the dosimetry uncertainty. The flux was selected to obtain a minimal 30 seconds of ion beam exposure to reach the total particle fluence. It was noted that the flux was kept low for the cyclotron and that the dosimetry uncertainty was on the order of a factor of two.
2. Select incidence angle and direction for the exposure. Center the SRAM device in the particle beam.
3. Select the $V_{DD}$ and N-Well bias for the exposure.
4. Perform a pre-irradiation write and read of the SRAM and track the bad bits. Since this SRAM is a test chip, there are a number of bad bits per device. The number of bits that were bad varied as a function of the n-well bias. At a low bias (0.7 V), there were approximately 15 bad bits in the SRAM array. At a normal bias (1.2 V), there were approximately 50 bad bits in the SRAM array. Finally, at the low standby power bias (1.8 V), there were approximately 70 bad bits. The number of bad bits did not affect the testing as there were over four million SRAM bits evaluated.

5. Expose the device to a set fluence. The goal of the exposure was to have about 1000 SEUs in the SRAM. More upsets would push the limit of the FPGA controlling the test and would increase the probability for co-incidence ion strike locations.
6. Read the SRAM array contents, remove the pre-irradiation bad bit addresses, and record the location of SEUs.

There is one final note about the testing. The TI SRAM array has shown susceptibility to single event latchup (SEL). Since the devices are bonded to a daughter card, it is not a trivial cost to prepare devices for test. So, ions, angles, and $V_{DD}$ were generally restricted to avoid SEL. In addition, the current to the device was limited and monitored during the testing. There were no unexpected increases in device current observed during the testing, so it is assumed that SEL was not encountered.

## TAMU Test Results

The test log of the TAMU SEU testing on the TI SRAM array is provided in Table 4. There were three ions used in the testing: Ne, Ar, and Kr. The tests also covered normal angle of incidence and two other angles in directions both parallel and perpendicular to the n-well. All the tests were performed with the same biases. The rows highlighted in red are the test runs that will be the focus of the analysis for this research. Based upon the TCAD modeling results, it was evident that the well-collapse source-injection mechanism is more easily observed at high angles of incidence.

Table 4. TAMU SEU test log.

| Run # | Ion | LET MeV-cm$^2$/mg | Eff. Fluence particles/cm$^2$ | Incident Angle degrees | Direction | $V_{DD}$ volts | N-Well Bias volts |
|---|---|---|---|---|---|---|---|
| 5-9 | $^{20}$Ne | 2.8 | 2.5x10$^5$ | 0 | - | 1.2 | 0.7 |
| 10-14 | $^{20}$Ne | 2.8 | 2.5x10$^5$ | 45 | Parallel | 1.2 | 0.7 |
| 15-20 | $^{20}$Ne | 2.8 | 1.0x10$^5$ | 78.5 | Parallel | 1.2 | 0.7 |
| 21-26 | $^{40}$Ar | 8.6 | 3.5x10$^4$ | 78.5 | Parallel | 1.2 | 0.7 |
| 27-34 | $^{40}$Ar | 8.6 | 1.1x10$^5$ | 45 | Parallel | 1.2 | 0.7 |
| 35-39 | $^{40}$Ar | 8.6 | 1.5x10$^5$ | 0 | - | 1.2 | 0.7 |
| 40-45 | $^{84}$Kr | 28.9 | 7.1x10$^4$ | 0 | - | 1.2 | 0.7 |
| 46-50 | $^{84}$Kr | 28.9 | 3.7x10$^4$ | 45 | Parallel | 1.2 | 0.7 |
| 51-60 | $^{84}$Kr | 28.9 | 1.4x10$^4$ | 78.5 | Parallel | 1.2 | 0.7 |
| 61-62 | $^{84}$Kr | 28.9 | 2.0x10$^4$ | 0 | - | 1.2 | 0.7 |
| 63.67 | $^{84}$Kr | 28.9 | 4x10$^4$ | 45 | Perpendicular | 1.2 | 0.7 |
| 68-77 | $^{84}$Kr | 28.9 | 1.0x10$^4$ | 78.5 | Perpendicular | 1.2 | 0.7 |
| 78-82 | $^{40}$Ar | 8.6 | 3.1x10$^4$ | 78.5 | Perpendicular | 1.2 | 0.7 |
| 83-87 | $^{40}$Ar | 8.6 | 1.0x10$^5$ | 45 | Perpendicular | 1.2 | 0.7 |
| 88-89 | $^{40}$Ar | 8.6 | 1.0x10$^5$ | 0 | - | 1.2 | 0.7 |
| 90-92 | $^{20}$Ne | 2.8 | 1.0x10$^5$ | 0 | - | 1.2 | 0.7 |
| 93-97 | $^{20}$Ne | 2.8 | 2.5x10$^5$ | 45 | Perpendicular | 1.2 | 0.7 |
| 98-103 | $^{20}$Ne | 2.8 | 1.1x10$^5$ | 78.5 | Perpendicular | 1.2 | 0.7 |

All of the highlighted test runs were analyzed by hand to examine the upset patterns. It is challenging to extract the patterns automatically since the SRAM cells themselves are not ideal in layout. So, the upset patterns do not completely conform to the predicted patterns listed in Table 3. To present an overview of the data set, each of the data sets was split into MCU groups. The groups were then analyzed and categorized by the type of MCU pattern observed. If the MCU pattern was consistent with direct charge collection, then it was categorized as “direct.” On the other hand, if the MCU pattern indicated well-collapse source-injection, it was categorized as “well-collapse.” If the MCU pattern contained elements of both, it was still categorized as “well-collapse.” In general, MCU patterns categorized as well-collapse fit the later condition.

For the data sets that were parallel to the long n-well direction, each set had some of the MCU observations fit the well-collapse source-injection mechanism. For Ne (LET = 2.8 MeV-cm$^2$/mg), there were a total of 540 MCUs observed with 30 of those exhibiting well-collapse source-injection (5.6%). Some of the MCU patterns observed are shown in Figure 107, with the most prevalent patterns being A and B. For Ar (LET = 8.6 MeV-cm$^2$/mg), there were a total of 415 MCUs observed with 75 exhibiting well-collapse source-injection (18.1%). A selection of observed MCU patterns is shown in Figure 108. Patterns A through F occur most frequently. All of these patterns, excluding Pattern A, are a long chain of direct charge collection upsets with a well-collapse source-injection tail. This is likely near where the ion exits the n-well. When the LET of the incident ion is increased to 28.9 MeV-cm$^2$/mg, most of the observed MCU indicate the well-collapse source-injection mechanism. It was very difficult to decipher the patterns as they were large and of numerous shapes. Also, since the average MCU was between 20 and 30 SEUs, it did not take many ion strikes to arrive at 1000 upsets. In the data set, there were 212 MCUs observed with 183 clearly exhibiting the well-collapse source-injection mechanism. The remaining 29 observations (13.7%) spread out over multiple columns. It is possible that the well-collapse source-injection mechanism was involved, but the patterns were inconclusive in these cases. A few sample MCU patterns for this ion are shown in Figure 109. These are some of the shorter patterns observed, but give a good indication of the complexity of the patterns.

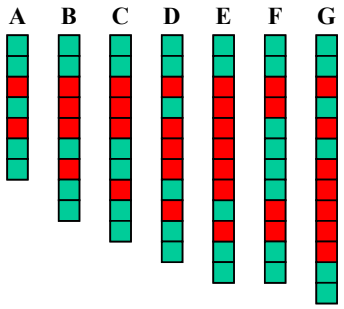



Figure 107. Examples of observed MCU patterns for TAMU SEU test (LET = 2.8 MeV-cm$^2$/mg, incident angle = 78.5$^o$, parallel to the n-well).

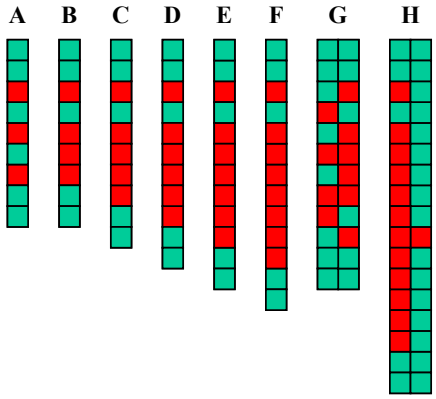



Figure 108. Examples of observed MCU patterns for TAMU SEU test (LET = 8.6 MeV-cm$^2$/mg, incident angle = 78.5$^o$, parallel to the n-well).

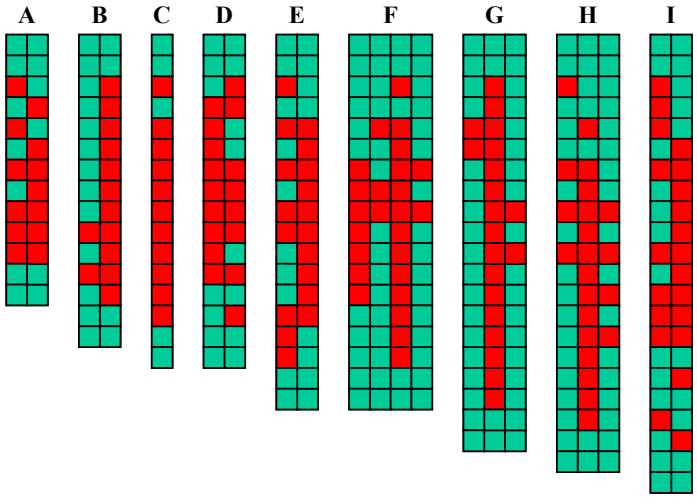



Figure 109. Examples of observed MCU patterns for TAMU SEU test (LET = 28.9 MeV-cm$^2$/mg, incident angle = 78.5$^o$, parallel to the n-well).

When the ion strikes are angled perpendicular to the n-well direction, there are no observed well-collapse source-injection MCU patterns for Ne or Ar. This agrees with the angled TCAD simulations from Chapter VII. However, with the Kr ions, most of the MCU patterns indicate the well-collapse source-injection mechanism; 134 of the 170 MCU patterns or 78.8% fit that category. These patterns are spread out over multiple columns as seen in Figure 110.

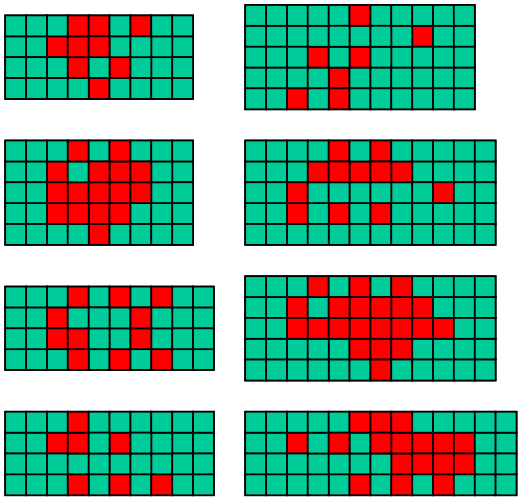


Figure 110. Examples of observed MCU patterns for TAMU SEU test (LET = 28.9 MeV-cm$^2$/mg, incident angle = 78.5$^o$, perpendicular to the n-well).

The results of the SEU testing of the TI SRAM at TAMU support the well-collapse source-injection mechanism concepts. It is easier to observe the mechanism with highly incident angles down the well rather than perpendicular to the well. However, at the highest LET tested, both directions exhibit the characteristics of the well-collapse source-injection mechanism, which is also as predicted.

## LBNL Test Results

Since the TAMU SEU tests of the TI SRAM produced MCU patterns consistent with the well-collapse source-injection mechanism, the LBNL tests focused on voltage variations. The TI SRAM has the ability to independently control the $V_{DD}$ connected to the p+-sources and the n-well bias. All of the TAMU data were taken with the same $V_{DD}$ and n-well bias, 1.2 V and 0.7 V, respectively.

Varying the n-well bias controls the body bias of the pMOSFETs in the SRAM. Increasing the n-well bias with respect to $V_{DD}$ effectively increases the magnitude of the threshold voltage of the pMOSFETs. As a result, the OFF pMOSFET will have less leakage current, and the overall SRAM array standby current will be less. However, the increase in the body potential will also increase the reverse bias for the drain/body and source/body p-n junctions. The depletion regions for these junctions will be larger as will the electric fields in the depletion regions. With respect to SEU, the increase in the well bias is expected to harden the cell due to the increased noise margin in the cell. This hardening should manifest itself when charge deposition is near the onset of SEU. However, it is not expected to have an effect when charge deposition is much greater than required to upset the cell. Thus, variations in the n-well bias should have no significant effect on the SEU cross section of the TI SRAM for most of the heavy ions tested.

On the other hand, increasing the $V_{DD}$ of the SRAM is expected to affect the SEU or MCU response of the TI SRAM array. $V_{DD}$ is connected to the p+-sources and sets the potential at that terminal of the p-n source/body junction diodes. This is very important for the well-collapse source-injection mechanism, as the well potential does not have to reduce as much to forward-bias the source/body diodes. So, increasing $V_{DD}$ is expected to

increase the effect of the well-collapse source-injection mechanism. Conversely, SEU response from direct charge collection should decrease with an increased $V_{DD}$. Increasing $V_{DD}$ will: (a) increase the depletion region and electric field in the OFF nMOSFET, (b) decrease or maintain the depletion region and electric field in the pMOSFETs, and (c) increase the noise margin of the SRAM cell. All but (a) will act to harden the cell to direct charge collection. The change in the nMOSFET depletion region and electric field should have no effect when the charge deposition is much greater than required to upset the SRAM cell. In summary, increasing the SRAM cell $V_{DD}$ should increase the SEUs due to the well-collapse source-injection mechanism, while not increasing SEUs due to direct charge collection.

A summary of the LBNL SEU testing on the TI SRAM array is given in Table 5. These are a subset of the testing that was performed showing only the experiments related to voltage variations. In general, the test results were as expected. The variation in the well bias did not affect the observed SEU cross section. The only difference is seen in the first two columns for the B ion. It is possible there is a higher cross section for the higher well bias, but there is no way to conclude that. The B ion beam was very unstable in flux, so it is quite possible that the difference is the result of a testing error.

The test results for the $V_{DD}$ variation also followed expectation. Increasing $V_{DD}$ from 1.2 to 1.4 V, while maintaining the well bias at 1.8 V, showed a significant increase in the number of SEUs observed for both directions. For the direction that was parallel to the n-well, the data for $V_{DD}$ = 1.2 V showed a small percentage of double column MCUs. Due to the nature of the SRAM array topology, the generally constant pattern made it difficult to attain double column MCUs with direct charge collection (there were very

few cases where OFF nMOSFET drains from two columns were adjacent). However, the data for $V_{DD}$ = 1.4 V showed mostly double column MCU patterns. The double column MCU patterns are the result of the well-collapse source-injection mechanism. For the direction that was perpendicular to the n-well, the data shows a similar result. For $V_{DD}$ = 1.2 V, there are few double column MCUs; while most of the MCUs for $V_{DD}$ = 1.4 V cross two columns. Thus, the increase in the number of upsets for $V_{DD}$ = 1.4 V is a direct result of increasing the susceptibility to the well-collapse source-injection mechanism.

Table 5. LBNL SEU test results.

| Ion | LET MeV-cm$^2$/mg | Incident Angle Degrees | Direction | $V_{DD}$ volts | Well Bias volts | Fluence particles/cm$^2$ | Eff. Fluence particles/cm$^2$ | SEUs | Cross Section cm$^2$ |
|---|---|---|---|---|---|---|---|---|---|
| B | 0.89 | 0 | - | 1.2 | 1.8 | $4.0x10^{5}$ | $4.0x10^{5}$ | 776 | $1.94x10^{-3}$ |
| B | 0.89 | 0 | - | 1.2 | 0.7 | $8.0x10^{5}$ | $8.0x10^{5}$ | 1360 | $1.70x10^{-3}$ |
| Cu | 21.17 | 45 | Perpendicular | 1.2 | 0.7 | $4.0x10^{4}$ | $2.8x10^{4}$ | 1884 | $6.66x10^{-2}$ |
| Cu | 21.17 | 60 | Parallel | 1.2 | 0.7 | $4.0x10^{4}$ | $4.0x10^{4}$ | 1717 | $8.59x10^{-2}$ |
| Cu | 21.17 | 60 | Parallel | 1.2 | 1.8 | $6.0x10^{4}$ | $3.0x10^{4}$ | 2714 | $9.05x10^{-2}$ |
| Cu | 21.17 | 45 | Perpendicular | 1.2 | 1.8 | $4.0x10^{4}$ | $2.8x10^{4}$ | 1900 | $6.72x10^{-2}$ |
| Kr | 30.86 | 45 | Parallel | 1.2 | 0.7 | $5.0x10^{4}$ | $3.5x10^{4}$ | 1843 | $5.21x10^{-2}$ |
| Kr | 30.86 | 45 | Parallel | 1.2 | 1.8 | $6.0x10^{4}$ | $4.2x10^{4}$ | 2165 | $5.10x10^{-2}$ |
| Kr | 30.86 | 45 | Parallel | 1.4 | 1.8 | $6.0x10^{4}$ | $4.2x10^{4}$ | 3608 | $8.50x10^{-2}$ |
| Kr | 30.86 | 45 | Perpendicular | 1.2 | 0.7 | $6.0x10^{4}$ | $4.2x10^{4}$ | 2543 | $5.99x10^{-2}$ |
| Kr | 30.86 | 45 | Perpendicular | 1.2 | 1.8 | $6.0x10^{4}$ | $4.2x10^{4}$ | 2474 | $5.83x10^{-2}$ |
| Kr | 30.86 | 45 | Perpendicular | 1.4 | 1.8 | $6.0x10^{4}$ | $4.2x10^{4}$ | 4763 | $1.12x10^{-1}$ |

# CHAPTER IX

# IMPLICATIONS OF WELL-COLLAPSE SOURCE-INJECTION MECHANISM

## Multiple Node Charge Collection

In highly scaled geometries (< 250 nm), the effect of a single ion track has been observed on multiple circuit nodes. For multiple transistors in a common well, the charge collection may be the direct result of drift or diffusion. Alternatively, the collapse of the well potential by a single ion strike can induce the well-collapse source-injection mechanism in some or all of the transistors. Previous work by Black et al. examined two pMOSFETs in an n-well and the charge collection on each drain [Bl05]. Figure 111 shows the results of a device simulation of two transistors. In the top cross section, the transistors have a well contact between the drains, and in the lower cross section, there is no well contact. An ion strike was simulated on the drain on the right. Without the well contact, the well-collapse extended to the channel of the device on the left. As a result, this device collected charge, even though it was not directly struck. Figure 112 shows the two cases of drain current for the left device. Note the significant increase when the well contact did not exist.

One implication the well-collapse source-injection mechanism is the knowledge that a p+-source diode placed in the center of these two pMOSFETs instead of the n-well contact would have provided better isolation. The well contact can only supply so much single event current, where the p+-source diode can supply much more and aid in maintaining the well potential.

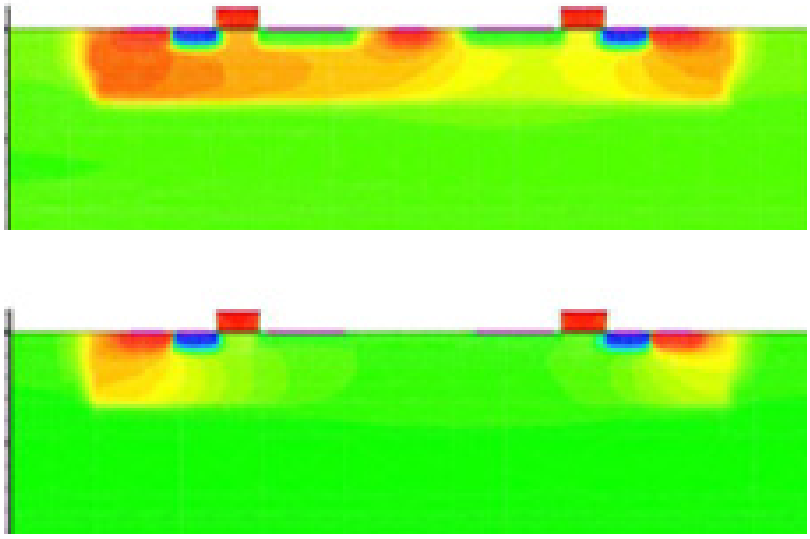


Figure 111. Two transistor simulation showing well-collapse (after [Bl05]).

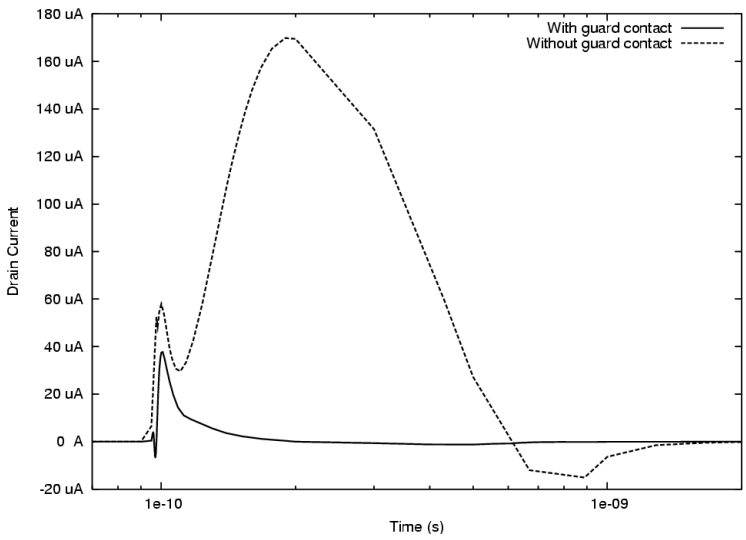



Figure 112. Simulated current on device in same well as ion strike (after [Bl05]).

Another implication of understanding the well-collapse source-injection mechanism is examining multiple node charge collection between: (1) pMOSFETs inside the n-well and (2) nMOSFETs near the n-well. SRAM cell TCAD simulations showed

that charge collection outside the well can collapse its potential very much like ion strikes inside the well. Thus, a single ion strike can cause charge collection via drift and diffusion on nMOSFETs near the well and cause charge collection via well-collapse source-injection to pMOSFETs inside the well.

The multiple node charge collection discussed in the preceding paragraphs spawned various studies in deep submicron charge collection. Amusan et al. examined charge collection and charge sharing in 130-nm technology [Am06]. This study resulted in an assessment of the parasitic bipolar enhancement on the secondary node charge collection. Figure 113 shows one result of this study where the diffused charge to the secondary node was demonstrated to have parasitic bipolar enhancement for pMOSFETs. This also shows that diffusion is more pronounced between nMOSFETs, but the bipolar enhancement makes the pMOSFET to pMOSFET charge sharing the worst case at higher charge depositions. It is more likely that the passive pMOSFET with source charge collection is the result of the well-collapse source-injection than parasitic bipolar enhancement, though the mechanisms are similar.

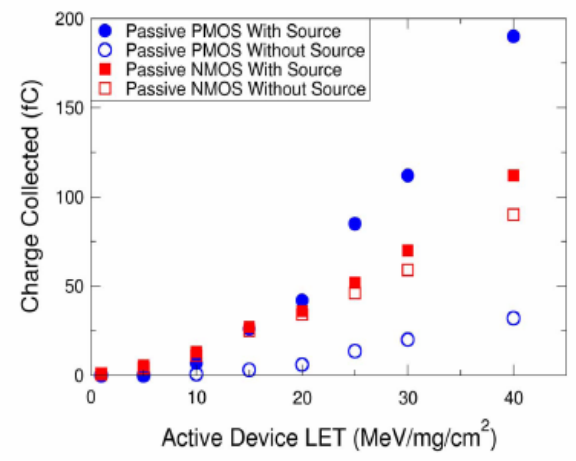



Figure 113. Parasitic bipolar enhancement study of secondary node collection showing significant effect in pMOSFET devices in 130-nm technology. (after [Am06]).

## Single Event Transient Generation

Another implication of the well-collapse source-injection mechanism is seen in the generation of single event transients (SETs) in combinational logic. Narasimham et al. examined the generation of single event transients in modern scaled silicon technology. While single event transients may not be important to the understanding of SRAM, this work highlighted the importance of proper modeling of the collection region and the well and substrate contacts. It has been shown that changing the location of ion strike, while keeping the charge deposition constant, changes the amount of charge collected on a node. This work demonstrated the proximity of the well and substrate contacts in varying the observed width of the single event transients; this directly relates to collected charge and is shown in Figure 114 [Na07]. The closer the well contact is to the ion strike, the better the contact can supply single event current; the well contact has a less resistive path. So, it is consistent that the SET pulse width would decrease when the ion strike is closer to the well contact.

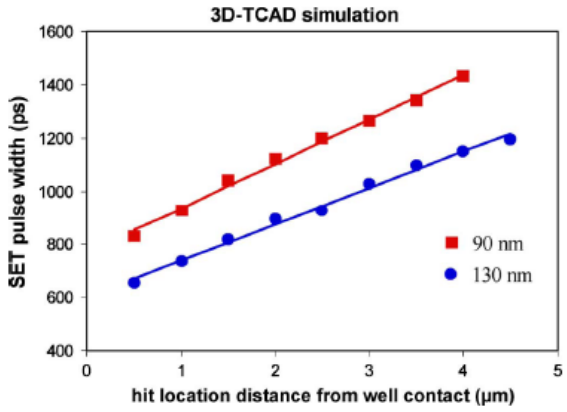



Figure 114. Single event transient pulse width as a function of ion strike distance to well contact in two scaled technology nodes showing large variation (after [Na07]).

Beyond the location of the well contacts are the locations of the p+-sources in the n-well. P+-sources that are close to the ion strike location will affect the pulse width. They can supply single event current and can enable the n-well to recover faster. The TCAD modeling in this research showed that the current pulses are shorter when all the p+-sources were included in the model, so it is reasonable that the SETs will be affected by the proximity of sources to the ion strike location. Further, the well-collapse source-injection mechanism affected all the sources in the SRAM array model, even those many micrometers away from the ion strike. Depending on the input/output mapping of the combinational logic, a variety of SET responses may be observed. The SET pulse may be lengthened, shortened, or blocked from propagation depending on the state of the input and outputs. As a result, the potential SETs generated in a logic block may have a very wide distribution.

## Low Voltage Operation

The LBNL test results showed a MCU dependence on the power supply, $V_{DD}$. The increase in $V_{DD}$ led to an increase in susceptibility to the well-collapse source-injection mechanism. There are circuit design concepts to reduce $V_{DD}$ to a very small level to operate the MOSFETs in the subthreshold region. Certainly circuits designed for such a small power supply will be more susceptible to direct charge collection, as the noise margins have been significantly reduced. The values of the critical charge for these circuits should be much lower than for circuits using the normal MOSFET operation. However, it is not clear whether or not low voltage operation will completely reduce the susceptibility of the well-collapse source-injection mechanism. The single event current generation will be the same, and that current will still need to be supplied. The well contacts will be further limited by the reduced power supply, so the p+-sources in the n-well and n+-sources outside of the n-well will have to supply the single event current. This likely will result in the well/substrate p-n junction forward-biasing. So, susceptibility to the well-collapse source-injection mechanism may actually increase with lower $V_{DD}$ as well. This is an area of further research.

## Resistive Hardening

The other interesting implication of the well-collapse source-injection mechanism and the crossover point is that it bounds the hardness that can be achieved by adding resistance to the feedback path of the SRAM cell. If the basic layout of the SRAM cell is not modified, but feedback resistors are added through other means (e.g., within the metallization layers), then the crossover to well-collapse source-injection defines a

maximum achievable point for the onset of upset of the hardened SRAM cell. Figure 115 shows the node voltages and source currents for the SRAM cell with no resistive hardening. Figure 116 shows the resulting node voltages and source currents when the SRAM cell is implemented with 10 kΩ feedback resistors and struck with the same 0.10 pC/μm single event. These simulations are virtually the same. So, once the upset mechanism is dominated by well-collapse source-injection, feedback resistors do not provide any hardening. This type of upset is dependent on the source/body diode resistance to the well and is not dependent on the feedback resistance.

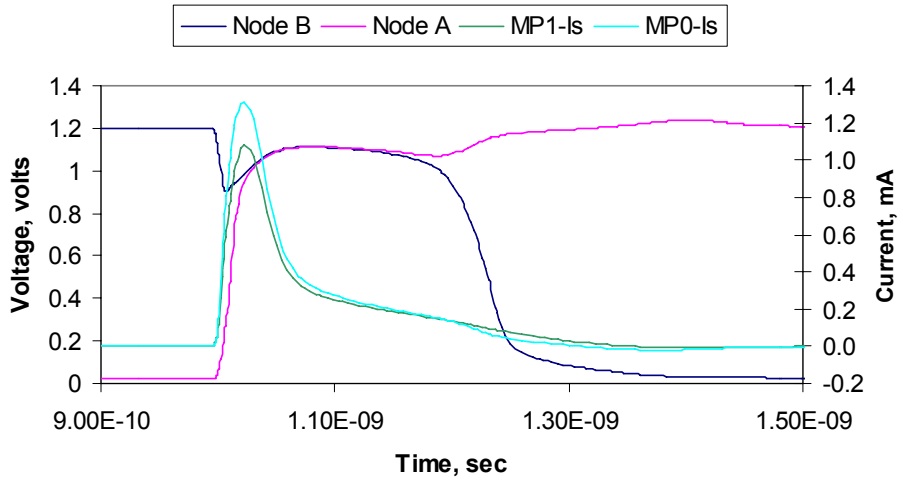



Figure 115. Node voltages and source currents for SRAM cell with no resistive feedback.

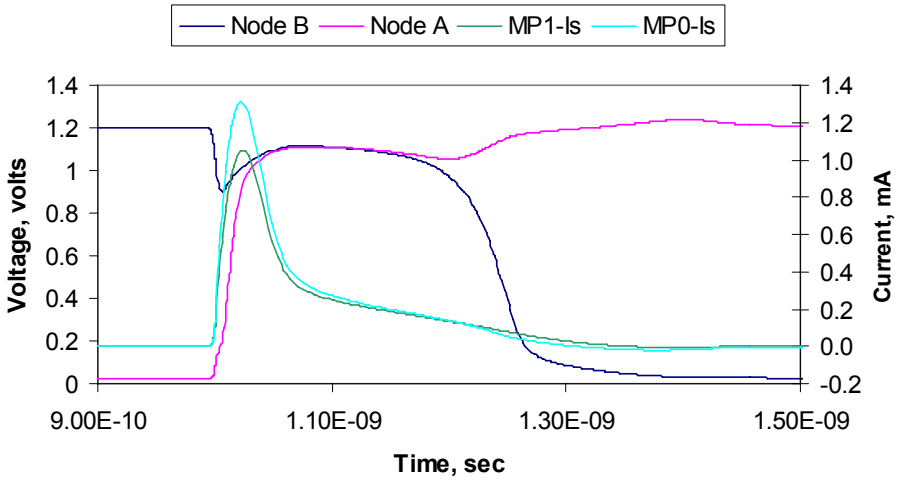



Figure 116. Node voltages and source currents for SRAM cell with 10kΩ resistive feedback.

# CHAPTER X

# WELL-COLLAPSE MITIGATION APPROACHES

The chapter briefly discusses a few approaches to mitigate the well-collapse source-injection mechanism. It is not a thorough review of mitigation techniques. Instead, it is an introduction to areas of further study.

## Improving Well Contact Single Event Current Supply

One conclusion that can be reached from the epi-substrate versus non-epi-substrate simulations is that a low resistive contact (epi-substrate) can keep the substrate potential pinned. It is the highly resistive well contact that enables the well potential to collapse. When the resistance to the well and substrate is equalized, the well potential decreases and the substrate potential increases, as in the non-epi-substrate simulations. From this, there are two methods to mitigate the well-collapse source-injection mechanism.

The first method is to reduce the well contact resistance to all regions of the well. The bulk of the contact resistance was in the region where the well contact was implanted above the well. A layout option to reduce this resistance is to increase the well contact area, but that has some limitations. Increases in well contact area will reduce semiconductor layout area available for design elements, so it is not desirable to make well contacts too large. A processing option to reduce this resistance is to change the well contact design. It would be better to make the well contact virtually on top of the well, as

was the case with LOCOS isolation. Replacing the well contact with either a longer, highly doped region down into the well or with some kind of metal plug would serve this purpose. If the contact resistance down to the well can be significantly reduced, then the resistance through the well becomes the limiting factor. The highly doped substrate region provides low resistivity to all areas of the substrate. A highly doped region within the bottom part of the well could aid in reducing the well resistance per unit length. If the well contact resistance can be significantly reduced, then the well contact can supply most to all of the well/substrate p-n junction single event current.

The second method is to follow the lightly doped substrate concept and make the contact resistance equivalent for the well and for the substrate. This can reduce the forward-bias current that is observed at the p+-sources, but may enable forward-bias current in the n+-sources outside the well. Nonetheless, the application of a lower doped substrate with a reduction in the operating voltage likely reduces the ability for the source/body junctions to forward-bias. The radiation challenge that this option adds is the potential for SEL. Allowing the well and substrate local voltages to modulate creates a sufficient condition for latchup. So, this would not be a desirable option for most radiation hardened designs.

### Using P+-Sources to Pin the N-Well Voltage

A design hardening concept that was initially thought to be very effective against well-collapse source-injection was increasing the voltage connection on one of the p+-sources in the n-well. In the SRAM array model, there were 12 p+-sources in the n-well, all biased at 1.2 V. If one of them is biased at 1.5 V, while the rest remain at 1.2 V along

with the well bias, then this one p+-source is much closer to forward-biasing than the rest. It was theorized that, during an ion strike that causes well-collapse, this source/body p-n junction would forward-bias earliest and pin the well potential, keeping the other p+-sources from forward biasing. This had the advantage of overcoming the p+-source resistance to the well; however, it could not overcome the resistance down the well. A summary plot of the forward-bias currents for three different ion strikes normal to the semiconductor surface is shown in Figure 117. These data were for a charge deposition of 0.20 pC/μm. The plot in Figure 118 is the same ion strikes given the case that the p+-sources at -0.4 μm bias was altered to 1.5 V. The results for these simulations show that the increased source bias aids in restricting the region of the well-collapse source-injection. The curves for ion strike at -4.0 and -2.0 μm shows less forward-bias current on the right side of the figure. The change in current is only a factor of two to three in this case, so this hardening approach does not seem too effective. However, this was not a complete analysis of the mitigation approach and there may other ways to “steer” the single event current away from critical circuit areas to designed single event current sources.

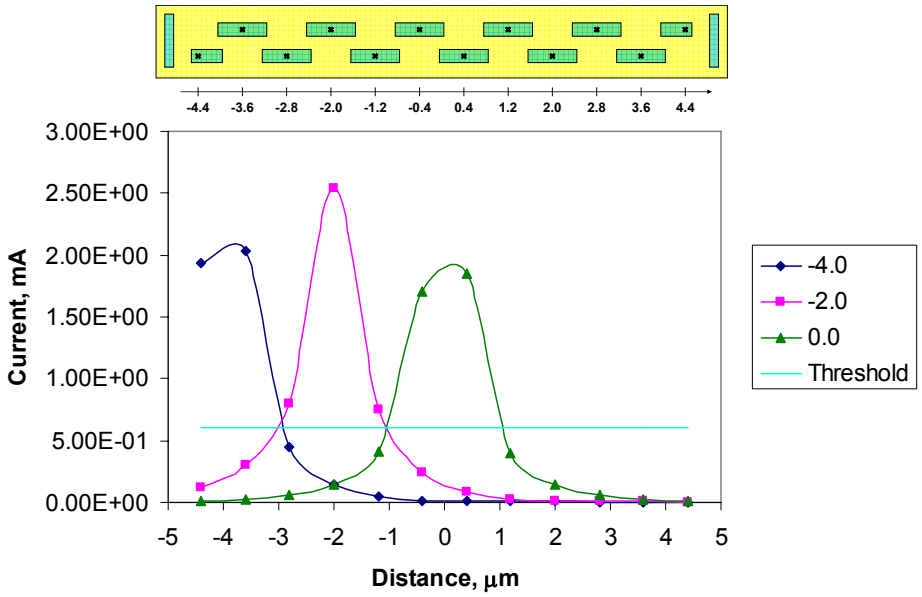



Figure 117. SRAM array forward-vias currents for three different ion strikes with all p+-sources at 1.2 V.

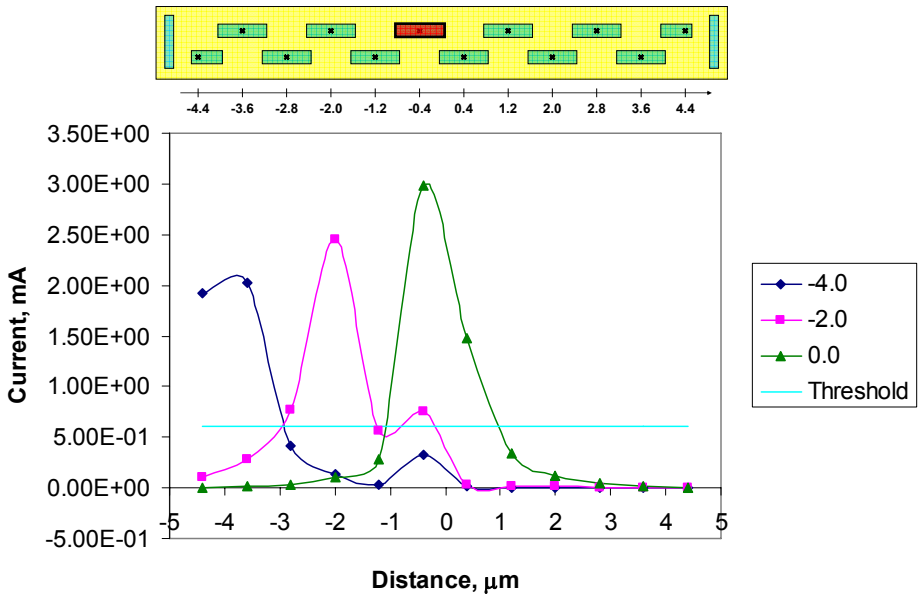



Figure 118. SRAM array forward-bias currents for three different ion strikes with p+-source at -0.4 µm biased at 1.5 V and the rest biased at 1.2 V.

## Defining a SRAM Preferred Recovery State

Since the recovery from the well-collapse source-injection mechanism is based upon the lowest resistance path to a p+-source, it is possible to design the SRAM cell to prefer one state over the other when subjected to this mechanism. The best way to do this is to increase the size of one pMOSFET with respect to the other. A significant size increase is not required since most of the resistance is from the bottom of the source to the top of the well. The SRAM cell will still flip due to direct charge collection, so the post-single event state of the SRAM cell may not always be the preferred state. However, if the dominant mechanism for MCUs is well-collapse source-injection, then the cells will recover to a preferred state.

There are a couple of applications for a preferred recovery state. The first application is the case when error detection and correction is employed in the SRAM array. If one error type, for example, logic high to logic low, is much more likely, then error correcting codes can be defined to take advantage of that fact. This would have the potential of restricting the overhead associated with encoded bits or improve the error correcting ability of the SRAM array. The second application is the case when the need for SRAM storage is mostly one of the two states. If the SRAM is storing an image that is typically of a dark background, most of the SRAM storage may be logic low. For this situation, it would be best to have a preferred recovery state of logic low to reduce to overall error rate of the SRAM for this application.

# CHAPTER XI

## SUMMARY

The study of SRAM SEU mechanisms in this research project led to the identification of the well-collapse source-injection mechanism. This mechanism was encountered when charge collection in the well/substrate p-n junction exceeds what can be supplied by the well and/or substrate contacts. When this occurs, the single event current was supplied by p+-source/n-body junction diodes in the well or by n+-source/p-body diodes in the substrate. The forward-bias condition injects minority carriers near the MOSFET drain that induces drain current. The SRAM cell recovery from well-collapse source-injection was defined by which p+-source had the lowest resistive path to the well/substrate charge collection.

This research project developed many TCAD models to study the well-collapse source-injection mechanism. Early on it was determined that to examine MCU properties, it was important to model as many devices as possible. The concept of replacing the MOSFETs in the model with diodes enabled many more devices to be simulated in one model. It was this breakthrough that enabled the MCU properties of the well-collapse source-injection mechanism to be understood.

Two SEU data sets for a 65-nm SRAM were analyzed for the well-collapse source-injection mechanism. TCAD modeling had indicated that ion strikes at high incident angles would demonstrate the mechanism better than low incident ion strikes. The TI data set from TAMU verified this result as well as provided many examples of

MCU patterns from the well-collapse source-injection mechanism. The patterns were complex, which meant that the patterns had to be hand analyzed. The second set of data was based upon SRAM bias voltage variations. It was shown that well bias voltage variations do not affect the upset cross section. However, increasing the SRAM $V_{DD}$ did significantly affect the observed upset cross section. The increase in the number of upsets was shown to be due to the well-collapse source-injection mechanism.

There are many implications of the well-collapse source-injection mechanism. The primary implication is being able to identify and categorize MCU patterns in an SRAM array. This research has shown how this identification and categorization can be achieved. Beyond SRAM, the mechanism has implications in multiple node charge collection, SET pulse width generation, and low-voltage circuit operation. Within SRAM, the well-collapse source-injection mechanism can identify the bound for resistive hardening. The mechanism was shown not to depend upon the feedback resistance.

As a final note, this research points out the importance of including all relevant structures in TCAD modeling. The SRAM cell model by itself is one of the largest TCAD models that can be simulated today. However, it was shown to be inadequate by itself to study the well-collapse source-injection mechanism or even study upsets due to diffusion charge collection. It is common practice in single event TCAD modeling to validate the meshing density and simulation time step. This research adds that models may need to include nearby sources to accurately model the supply of the single event current. Thus, TCAD modeling should validate whether nearby sources are necessary in the model to capture the observed behavior in actual devices.

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