ANALYSIS OF SINGLE EVENT TRANSIENTS IN DYNAMIC LOGIC CIRCUITRY

By

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CHAPTER I

INTRODUCTION

State-of-the-art high-speed integrated circuits frequently utilize dynamic logic circuitry to realize faster and smaller designs than corresponding static CMOS logic circuits. The use of these circuits in space is desirable, but not much work has been performed in assessing their vulnerability to ionizing particles present in the space environment. These particles pose a threat to the operation of digital CMOS logic circuitry when incident on an IC by creating electron-hole pairs that result in a voltage perturbation called a single event transient (SET). As these particles pass through a semiconductor material, they lose energy via Rutherford scattering with the nuclei of the lattice [1]. This energy is then transferred from the particle to bound electrons that are ionized into the conduction band, leaving a dense plasma track of electron-hole pairs [1]. The rate of energy loss to electron-hole creation is expressed as the linear energy transfer (LET). Along an incremental length *dx*, the electron-hole pairs created by the ion, with standard units MeV/gm/cm^2, are given by

$$dQ = (LET(x) \cdot \rho/G)dx$$

where dQ is the electron-hole pairs created in length dx

G is the energy for electron-hole pair creation

LET(x) is the particle LET as a function of distance

and ρ is the density of the target material

If the charge generated occurred in the bulk of the semiconductor device, then it may simply recombine or diffuse out. If the hit occurs at or near a p-n junction, then the charged particles are swept away via the associated electric fields at the junction. The current thus created by the drift and diffusion processes is then able to interact with the circuit and possibly cause incorrect circuit operation. The magnitude and direction of the current is determined by the structure of the hit device and bias conditions at the terminals of the device. Ion hits that occur on the drains of devices that are "off" may cause an upset. A hit on an "on" device will actually reinforce the logic level associated with the hit drain. Fig. 1 depicts the direction of current flow.

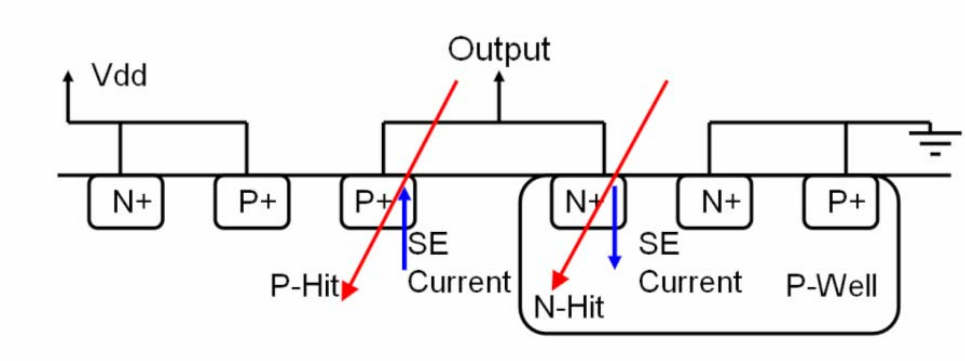

Fig. 1. Direction of transient current flow caused by a P-hit (strike on a PMOS device) and an N-hit (strike on an NMOS device) in an inverter using a bulk CMOS process. [1]

The voltage disturbance caused by this photocurrent is known as a single event transient (SET). An incorrect voltage that is latched and stored becomes a single event upset (SEU), otherwise known as a "bit flip".

Dynamic logic shares a few of the vulnerabilities that static logic exhibits. A transient error may result in a circuit fault depending on the current operation of the

circuit. Because the vulnerability depends on the logic state, circuit nodes become vulnerable at different times [3]. Fig. 2a show a combinational logic block with inputs "1101". For this set of inputs, the circuit has six nodes that could upset and create an error if latched. If the input vector then changed to "0000" (Fig. 2b), only one node would be vulnerable to an SET.

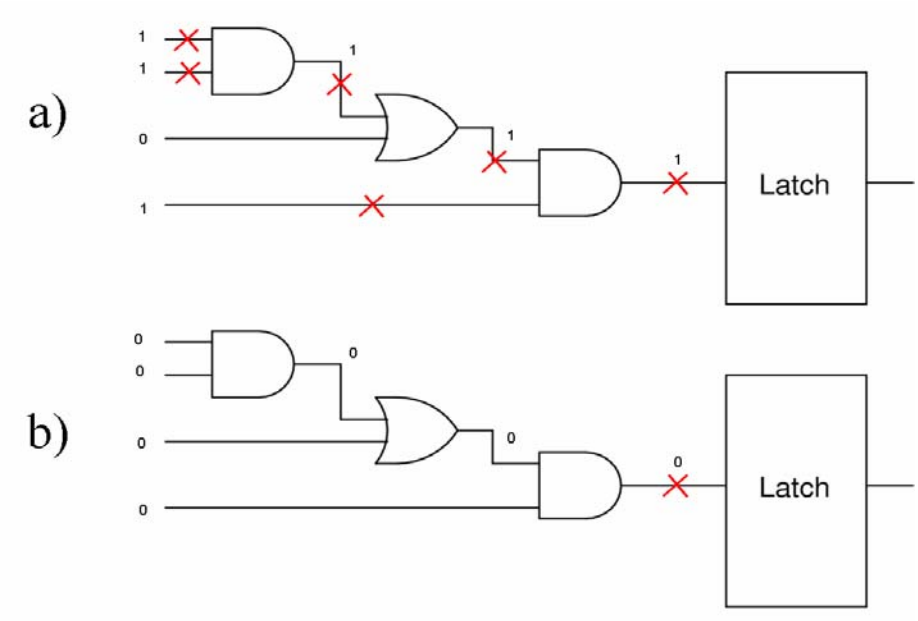

Fig. 2. a) Input vector creates multiple vulnerable nodes. b) Input vector produces only a single vulnerable node

Only vulnerable nodes that collect enough charge will cause an SEU. The charge required to upset a node is dependent on the nodal capacitance as well as the available current drive of the node [13].

Previous studies involving SETs in static logic circuits have shown that advances in technology and increased operating frequency result in an increase in the circuit

vulnerability to SET induced upsets (Fig. 3) [2]. This increase in vulnerability is due to the setup-and-hold requirements of static latches. During the setup-and-hold time of a static latch, the inputs to the combinational circuit feeding the latch are not allowed to change to ensure that the correct state is latched. An SET that reaches a latch input node during the setup-and-hold time will cause an error to be latched. Therefore, the setup-and-hold time can also be taken as the window of latch vulnerability. The setup-and-hold time is frequency independent, so as the frequency is increased, the ratio of the window-of-vulnerability to the clock period increases, assuming constant set-up-and-hold time requirements. This causes an overall linear increase in the number of errors that occur in the combinational blocks of static logic circuitry with increasing frequency.

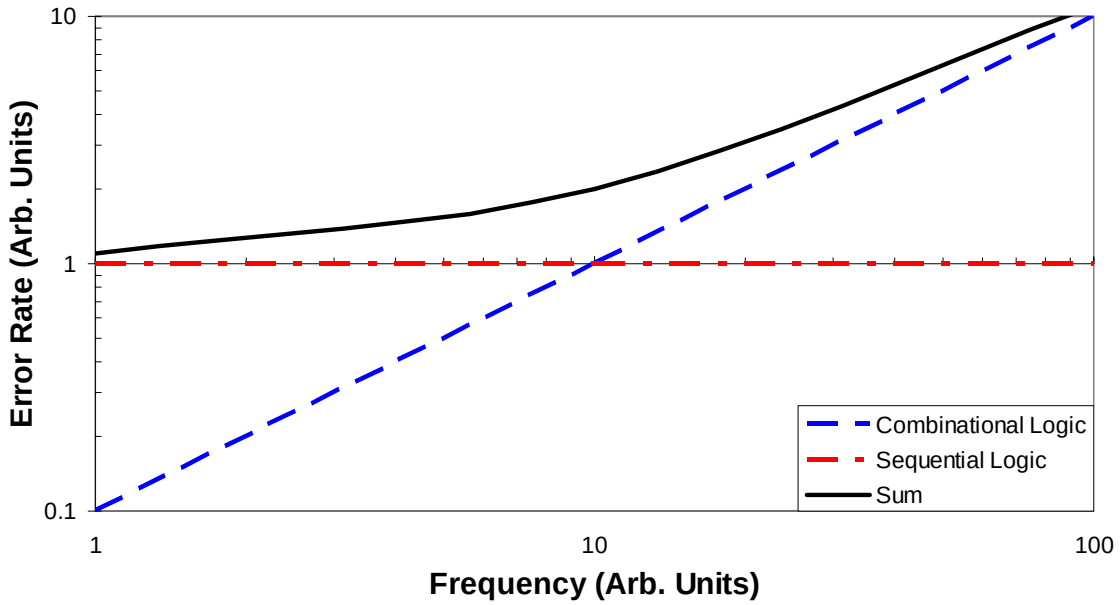

Fig. 3. Static error rate Vs frequency in both the combinational and sequential logic[5]

Static sequential logic error rate does not depend on circuit frequency. The only factor that determines a sequential node upset is the collected charge on the hit node. If the collected charge exceeds the critical charge then the bit will flip and an upset will occur [2].

This thesis examines the effects of SETs in combinational dynamic logic circuits. Simulations were performed using Spice-based simulations in both 130 nm and 90 nm technologies to examine dynamic logic vulnerability.

CHAPTER II

DYNAMIC LOGIC OVERVIEW

Dynamic logic circuits are appealing to use in circuit design because they are generally smaller and faster than static circuits [4]. A dynamic logic gate replaces the PMOS block of static gates with a single PMOS transistor and an extra NMOS "foot". Removing the PMOS block reduces the capacitance on the output node as well as reducing the loading of inputs. This allows the circuit to operate at higher clock frequencies.

TABLE 1. DYNAMIC LOGIC COMPARED TO STATIC LOGIC [11]

Area	**Speed**	**Power**	**Noise**
Smaller	Faster	Increased usage	Increased sensitivity

A dynamic NAND gate is shown in Fig. 4(a).

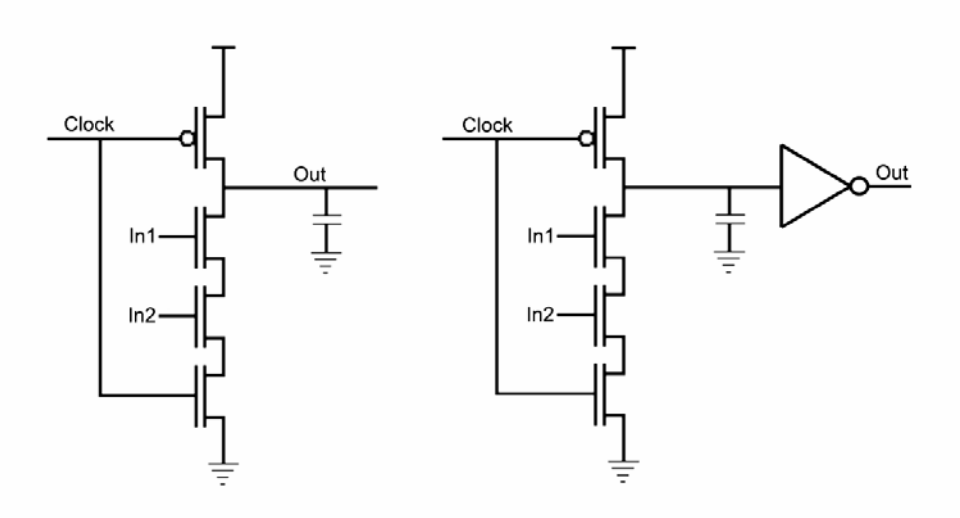

Fig. 4. Example of (a) dynamic NAND, (b) domino AND

When the clock is logically LOW, the gate is in the *precharge* mode of operation and the capacitance associated with the output node is charged to Vdd. As the clock goes to a logic level HIGH, the gate transitions to the *evaluate* mode of operation where the output may then float HIGH or conditionally discharge. Floating nodes are more vulnerable to noise because they cannot easily recover once charge has been lost. Dynamic circuit inputs must satisfy the monotonicity constraint. An input cannot start HIGH and fall LOW during *evaluate* because charge may be lost on a floating node before the device turns off. A standard domino gate solves the monotonicty problem by adding an inverter to the output as in Fig. 1(b). As the input of the inverter is charged HIGH during *precharge*, the output will only stay LOW or transition from LOW to HIGH during the evaluate phase[4].

CHAPTER III

PRECHARGE PHASE UPSET MECHANISMS

During *precharge*, an ion hit on the drain of an NMOS device will give rise to a transient current that could discharge the node. Because the node is still connected to Vdd through the PMOS device, it will start charging back up. If the charging does not complete before the *evaluation* phase begins, then an upset may occur. The node will be unable to recover until the next precharge phase (Fig. 5).

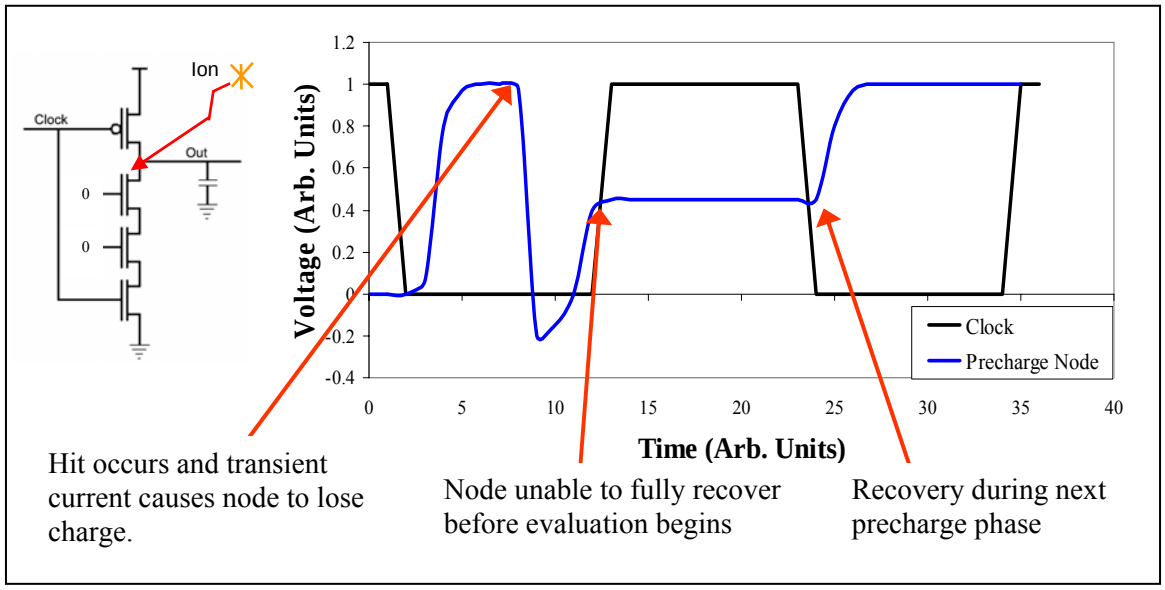

Fig. 5. The dynamic precharge transient

A simulated example can be seen in Fig. 6 using a 130 nm technology and a transient with total deposited charge of 21.1 fC. The latch output should remain LOW (the pulses

are normal for dynamic operation). A hit occurred near the end of a precharge phase that caused an upset in the next clock cycle and can be seen with the rise in the latch output voltage. The voltage overshoot is due to clock feedthrough. During the clock transition, the precharge device's gate-to-drain parasitic capacitance couples with the gates output allowing the voltage to rise above the rail. A window of vulnerability for the precharge upset mechanism therefore exists at the end of the precharge phase. This window of vulnerability is the time required for the circuit to precharge up to a logic level "1". Any hit occurring during this time will be unable to recover before evaluation. The window could also be considered as the minimum allowable time required for the circuit to precharge. This time will also change with inputs. For dynamic circuits, the worst-case precharge time is the time necessary to charge up the node with all other NMOS devices "on" (expect the foot NMOS device). This is the time required for all internal nodes to be precharged HIGH.

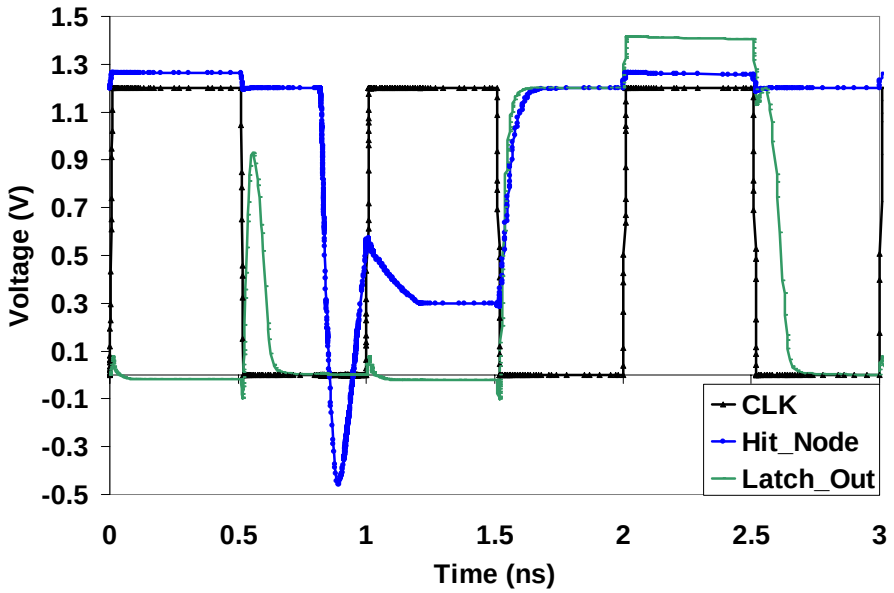

Fig. 6. Simulated Dynamic Precharge Upset

CHAPTER IV

EVALUATION PHASE UPSET MECHANISMS

Two mechanisms exist that could cause an upset in the evaluation phase of dynamic logic as a function of frequency. The first mechanism works by an N-hit causing a floating node to lose charge (Fig. 7). When the node loses charge, the voltage transient then begins propagating towards latching elements. If the transient is unable to reach a latch before the precharge phase, then an upset will not occur. Because a floating node has no active path back to Vdd, it cannot recover from charge loss until the next precharge phase. A window of invulnerability therefore exists at the end of the evaluation phase and is equal to the time needed for a transient to propagate to a latch.

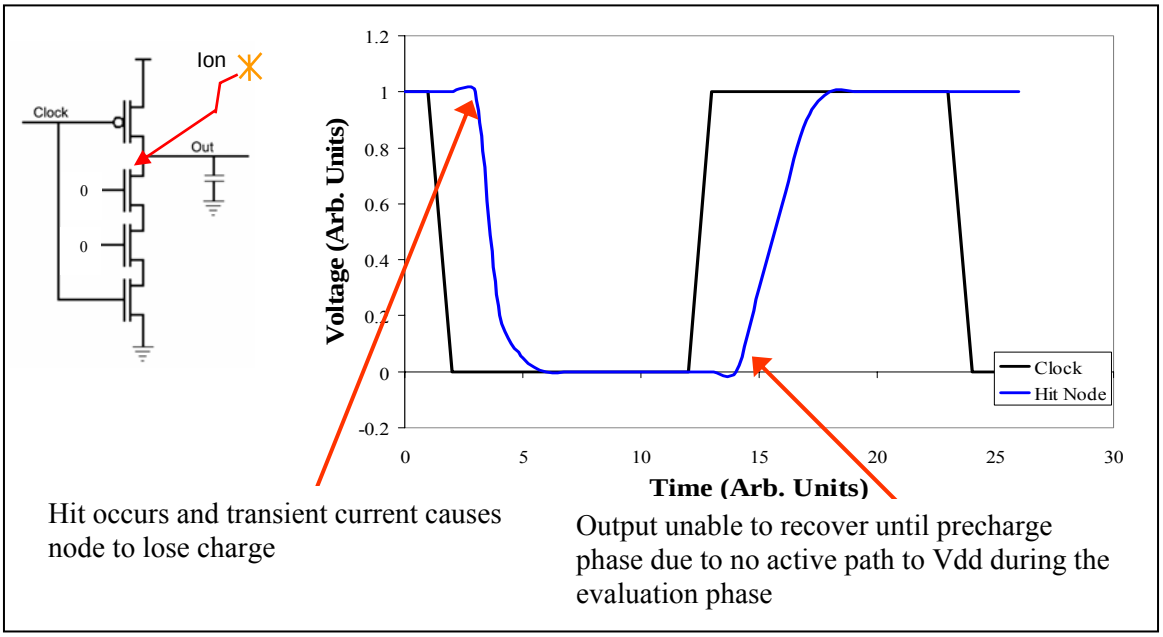

Fig. 7. Dynamic Evaluation Transient

A simulated example can be seen in Fig. 8 using the same transient previously defined.

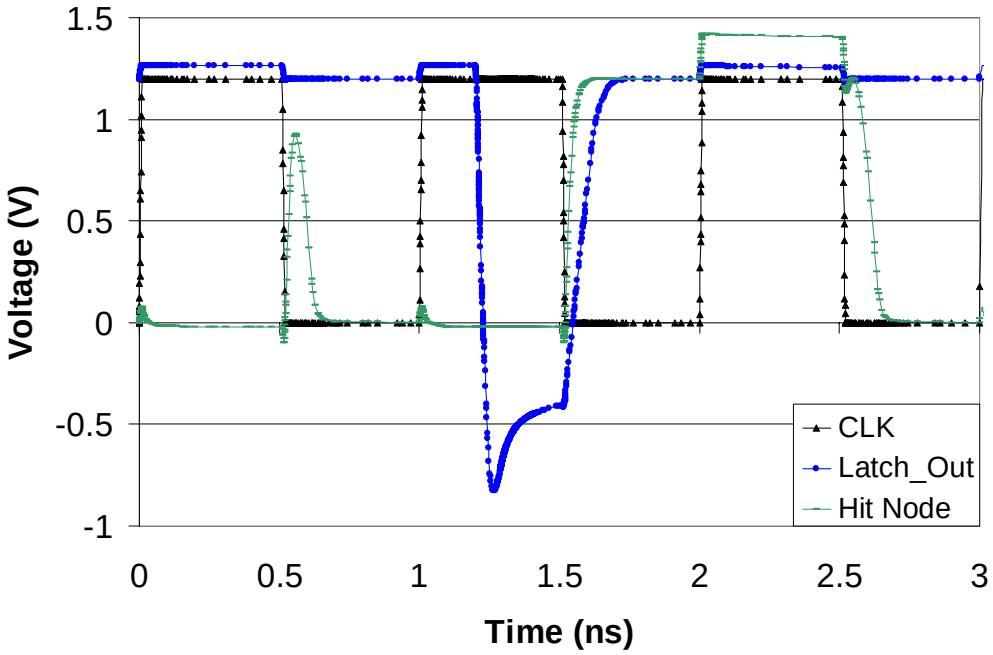

Fig. 8. Simulated Dynamic Evaluate Upset

The second upset mechanism is caused by a P-hit adding charge to a node (Fig. 9) and thereby increasing the voltage on the node. (In this thesis, the term "charge gain" is used to describe this event.) Nodes that should conditionally discharge during evaluation are susceptible to this upset mechanism. A hit on the clocked PMOS device will keep a node charged for some time even if it should conditionally discharge. At higher frequencies, this delay in evaluation is long enough to cause an upset. A window of vulnerability here exists at the beginning of the evaluation phase. The window of vulnerability is equal to the time needed to discharge the hit node. Because using multiple dynamic gates requires that domino logic is used, once a node has discharged

the dominos will “begin to fall”. After the dominos have started falling, it does not matter if the node gains charge. This is due to the fact that the gates have already completed their evaluation.

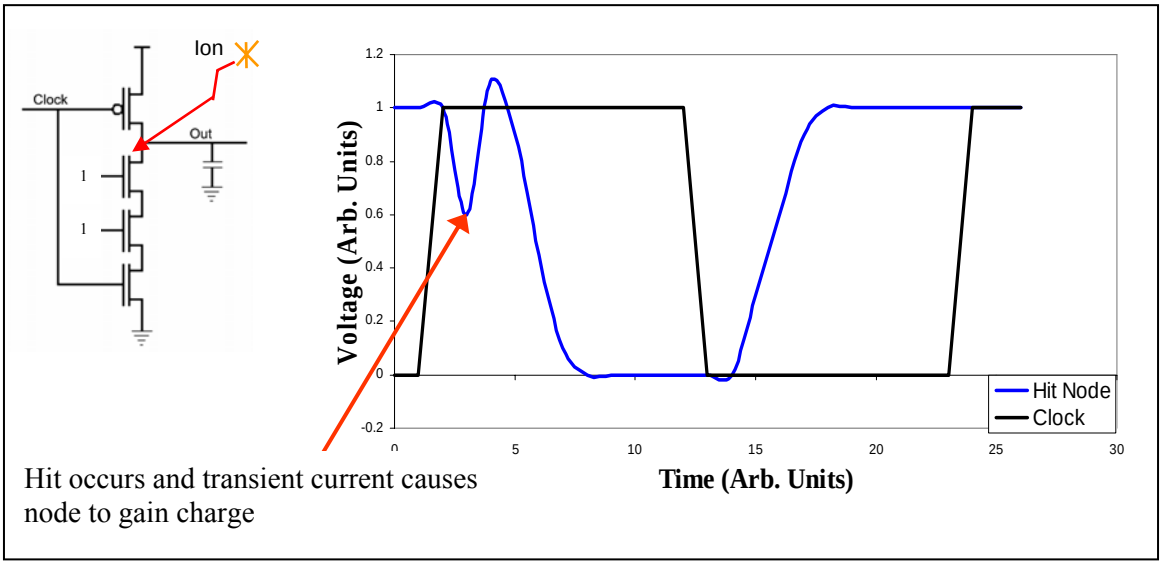

Fig. 9. Dynamic Charge Gain Transient

A simulated example can be seen in Fig. 10 using the same transient defined above.

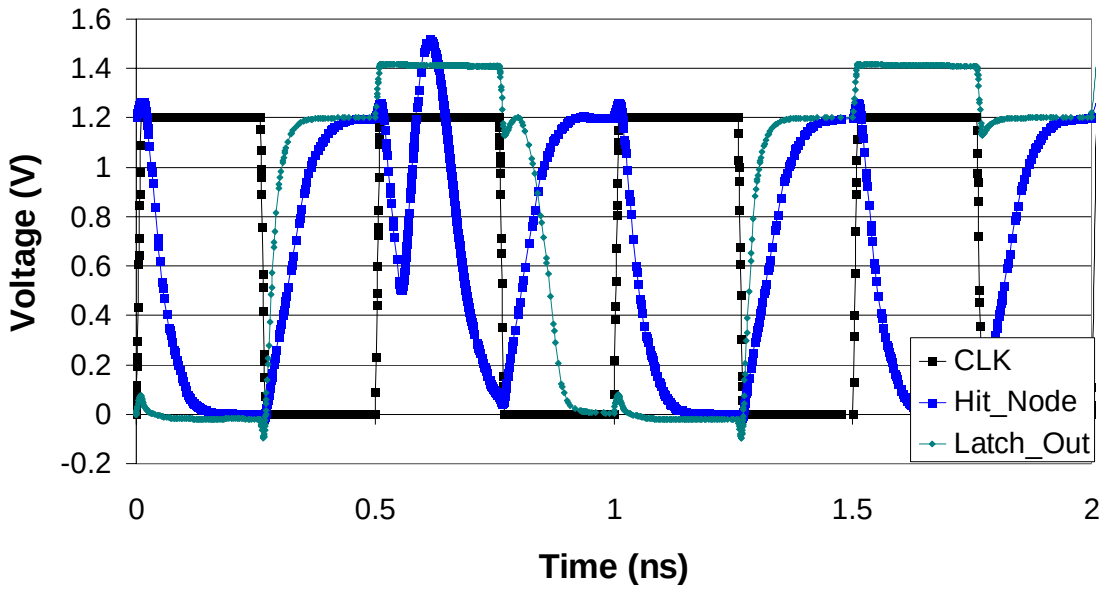

Fig. 10. Simulated Dynamic Charge Gain Upset

The circuit configuration will determine which evaluation upset mechanism will dominate. AND-like gates (gates with parallel NMOS devices) will be most vulnerable to the first evaluation upset mechanism while OR-like gates (gates with series NMOS devices) will be most vulnerable to the second evaluation mechanism. This is because when random inputs are used, an AND-like gate is less likely to discharge to ground than an OR-like gate. For the series AND gates circuits used, the first evaluation upset mechanism was three times more likely than the second evaluation upset mechanism.

CHAPTER V

PRECHARGE AND EVALUATE SIMULATON RESULTS

Two test circuits were used in this study (Fig. 11). Both were designed using IBM MOSIS 130 nm and 90 nm model definitions in static and dynamic logic. The static AND gates consisted of a static NAND coupled with a static inverter. The dynamic circuits were built using standard domino logic involving a dynamic NAND coupled with a static inverter at each output. To increase the evaluation time of the dynamic circuits, the PMOS device in the inverter was scaled eight times bigger than the NMOS device. The circuits consist of three stages (Fig. 11a) of AND gates in series and six stages (Fig. 11b) of AND gates in series. The static circuits used static latches and the dynamic circuits used dynamic latches (Fig. 12).

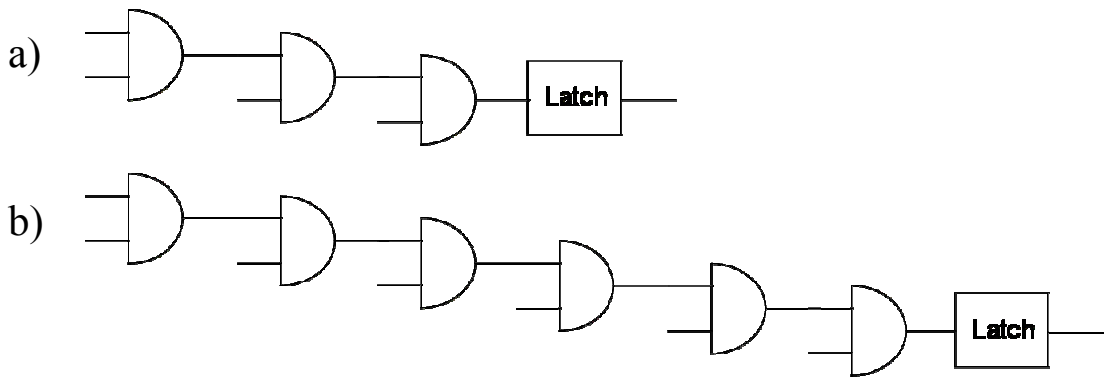

Fig. 11: Series AND Circuits Used

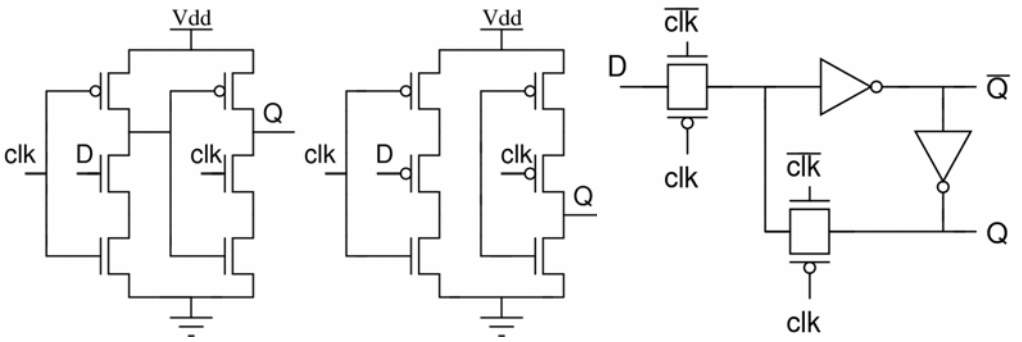

Fig. 12: Dynamic NMOS Latch, Dynamic PMOS Latch, and Static Latch Used

A transient current profile was used to simulate the photocurrent created when an ion hits a drain. The profile used was generated via 3D mixed-mode simulations on devices that were calibrated to the IBM process. Table 2 gives the characteristics of the SET current.

TABLE 2. SET CURRENT STATISTICS

LET	Peak Current	Rise Time	Fall Time	Collected Charge
5 MeVcm^2/mg	2.18 mA	7.33 ps	26.9 ps	47 fC

The node feeding the inverter was hit at multiple times in the clock cycle with a 2 ps resolution. The output of the latch was used to determine if an error occurred by comparing the expected latch output with the actual latch output. Hits that occurred

during clock transitions were ignored due to the fact that the transition time is very short compared to the non-transition time. All circuits used a 50% duty cycle for clocking.

Precharge simulation results for the three-stage circuit are presented in Fig. 13. The upset probability here is defined as:

$$\text{Upset Probability} = \frac{\text{Vulnerable Time}}{\text{Time Spend in Precharge}}$$

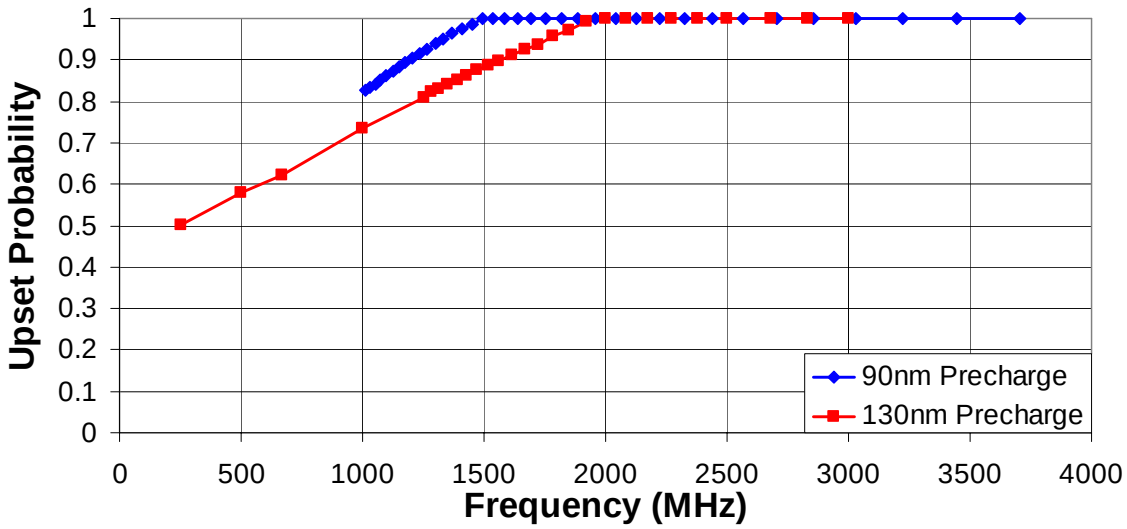

Fig. 13. Precharge Upset Probability versus Frequency

The precharge upset probability increases linearly with frequency to a point and then saturates. This is due to the fact that as frequency increases, the circuit has less time to precharge. Hits at higher frequencies are therefore more likely to cause an upset. Precharge upset probability saturates around 2 GHz for 130 nm and around 1.5 GHz in

the 90 nm circuit. The window of vulnerability at this point is equal to the total precharge time, and the circuit is unable to recover from any hit.

Evaluation phase simulation results for both evaluation upset mechanisms in the three stage circuit are presented in Fig. 14.

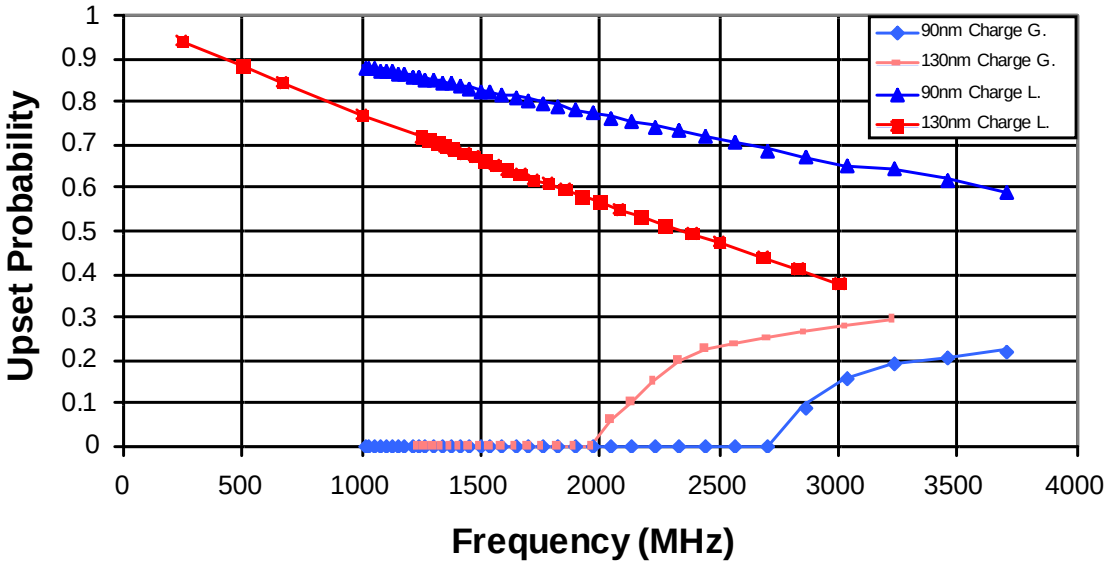

Fig. 14. Evaluation Upset Probability versus Frequency

For the charge loss upset mechanism, the upset probability decreases with increasing frequency. At higher frequencies, the transient has less time to propagate to a latch and cause an upset. Therefore, the upset probability decreases with increasing frequency. Other studies have shown that circuits with floating nodes tend to have a decrease in upsets as frequency increases [6]. With a charge gain upset, the upset probability increases with increasing frequency as expected. The delay in evaluation caused by the P-hit is only significant at higher frequencies. At lower frequencies, the delay is not long

enough to cause an upset as the circuit has plenty of time to evaluate, even with a transient induced delay.

Stage Length Dependency

Because the upset mechanisms are strongly dependent on a transient being able to propagate to a latch, a 6-stage circuit was simulated to complement the 3-stage study. Precharge simulation results can be seen in Fig. 15.

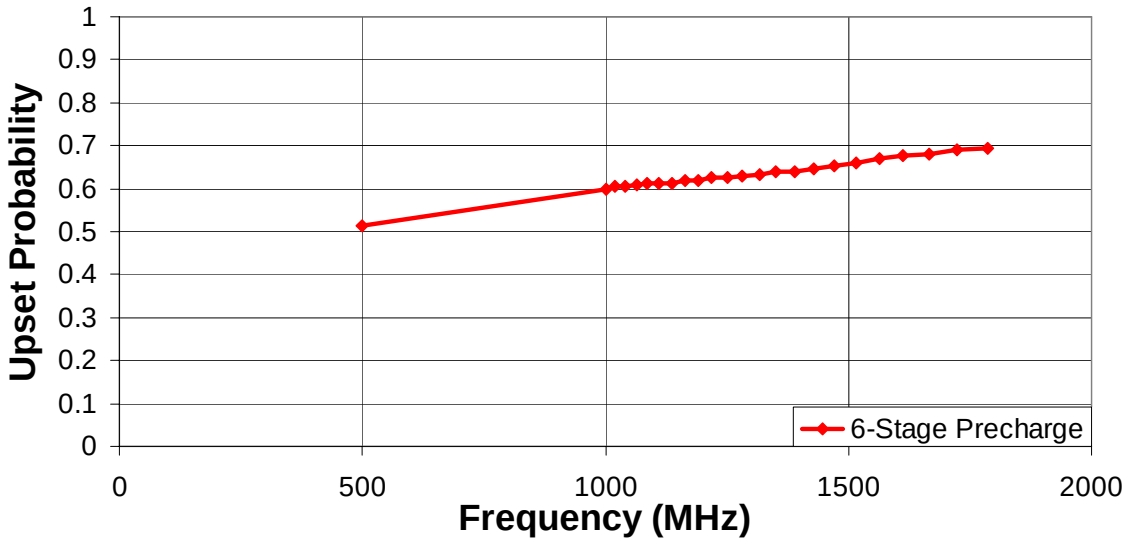

Fig. 15. 6-Stage Precharge Upset Probability versus Frequency

As expected, the upset probability increases with increasing frequency due to an affected node having less time to recover. The 6-stage circuit is unable to operate as fast as the 3-stage circuit, so the upset probability never reaches saturation.

The evaluation charge loss mechanism is strongly dependent on stage length. Having more stages increases the path length to a latch so it becomes harder for a transient to propagate and be latched before the next precharge phase. The effect is to increase the magnitude of the slope, causing fewer upsets at higher frequencies (Fig. 16).

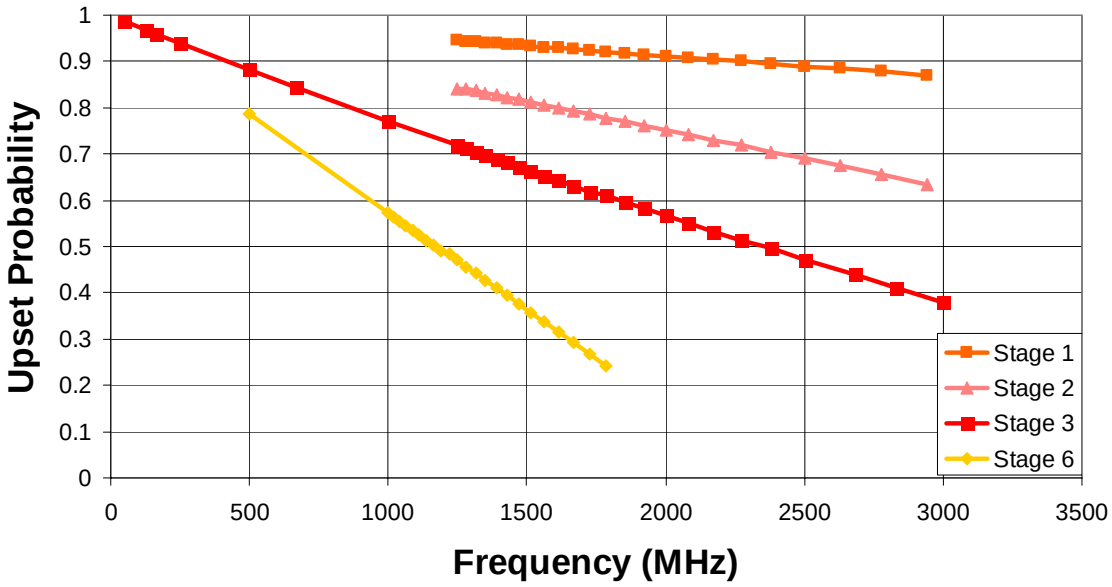

Fig. 16. Multiple Stage Evaluation Upset Probability versus Frequency

For the 6-stage circuit, the charge gain upset probability increases with increasing frequency (Fig. 17). As with the 3-stage circuit, the delay in evaluation caused by the P-hit is only significant at higher frequencies.

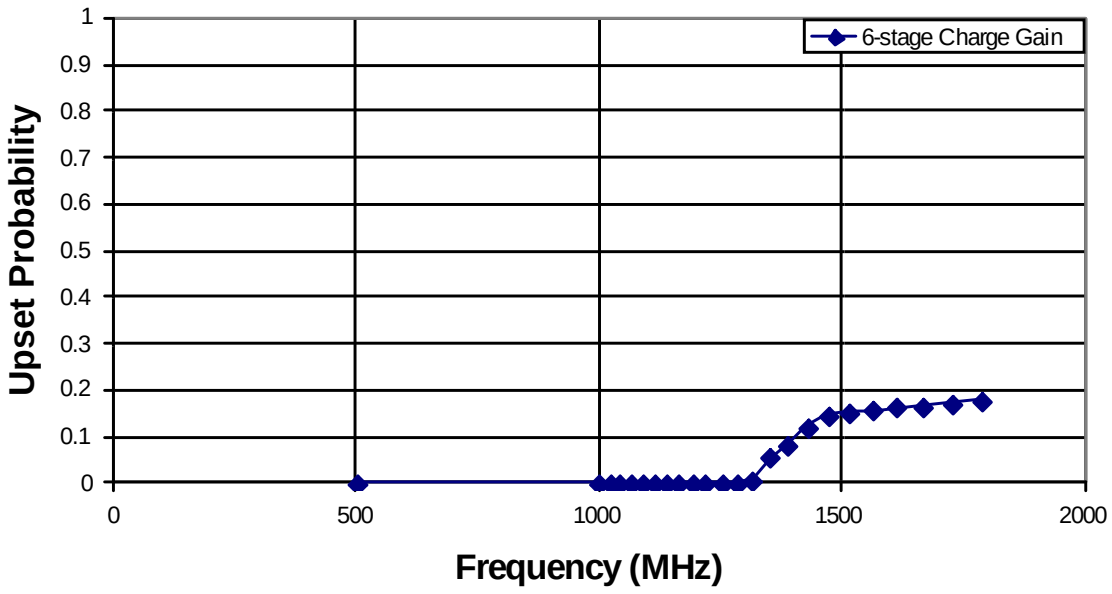

Fig. 17. 6-Stage Charge Gain Upset Probability versus Frequency

Keeper Device Effects

One technique to help mitigate upsets is to add a dynamic keeper device (Fig. 18). A keeper device is a static-like feedback device that helps maintain the floating node voltage. This device is usually minimally sized in order to reduce parasitic capacitance and keep circuit area small. If a hit occurs on the keeper node, the keeper's feedback will attempt to fight the loss in charge until the keeper device turns off. Adding a small keeper device decreases the upset probability and moves the saturation point to a higher frequency for the precharge phase. The keeper device works with the precharge device to provide more current drive to the node, which in turn reduces the time needed to recover from an SET.

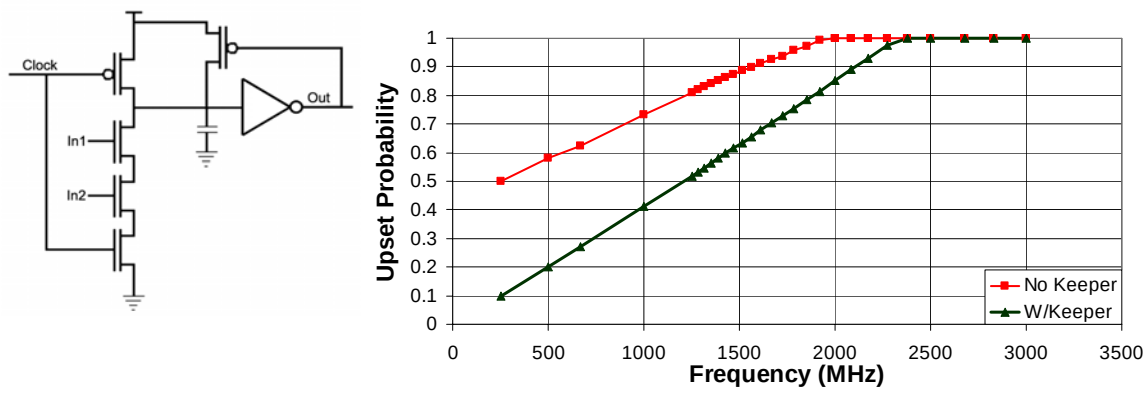

Fig. 18. 130 nm Precharge Upset Probability Keeper Effects

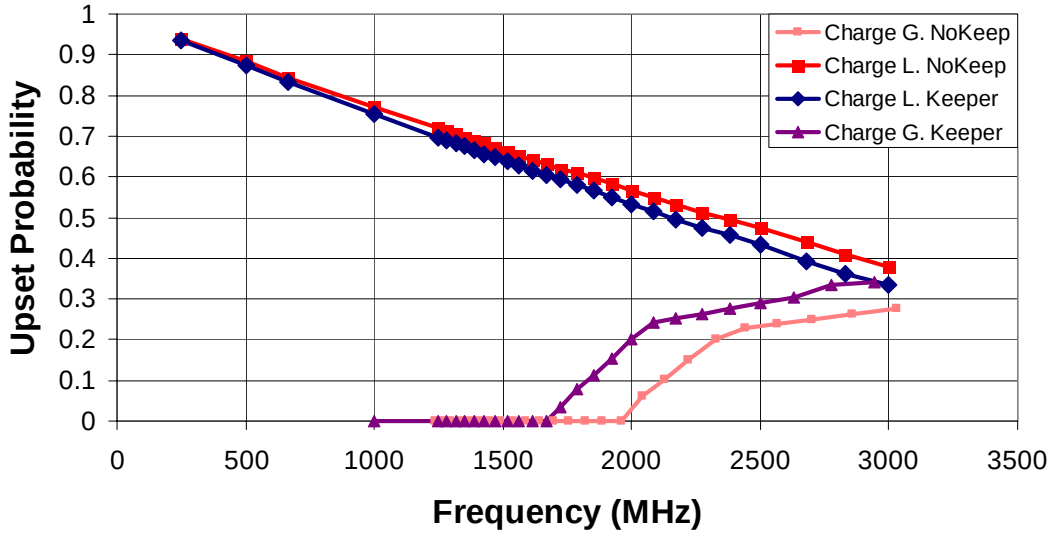

Fig. 19. 130 nm Evaluate Upset Probability keeper effects

The keeper device is unfortunately not as effective in decreasing upsets in the evaluation phase (Fig. 19). The keeper has little effect on the charge loss upset. There is no active path back to Vdd on a floating node. Once the charge is lost, there is no way to recover until precharge. The keeper is therefore quickly turned off as the inverter switches state. For the charge gain upset, the keeper actually increases the upset

probability. Adding a keeper increases the contention current when the node evaluates LOW. This current slows down the conditional discharge. Once the node evaluates LOW, it is no longer vulnerable to upsets by this mechanism as stated in the evaluation upset section (Chapter IV). Because the vulnerable time increases, the upset probability also increases.

LET Effects

The effects of a change in LET were also simulated using 90 nm technology definitions. First, a static circuit was simulated to form a base to compare with the dynamic logic circuit (Fig. 20). SETs with LETs of 5 and 1 were both simulated across frequency. Results match previous studies [2] and show a reduction in upset probability with lower LET. Smaller amounts of charge generated at lower LETs allow the circuit to recover faster.

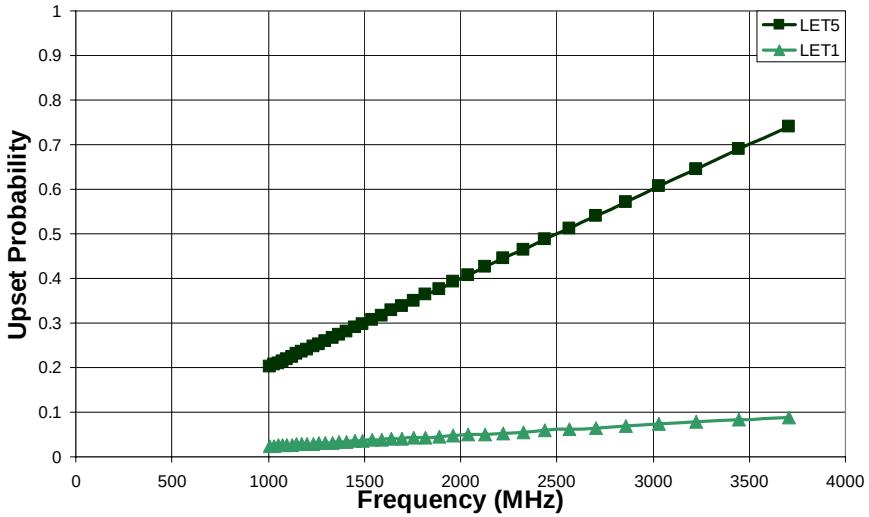

Fig. 20. 90 nm Static LET effects

For dynamic logic, the precharge phase upset probability shows a large dependence on LET (Fig. 21). During precharge, the node is connected to Vdd through the precharge device. The circuit is essentially in a static-like state and behaves the same way as the static circuit in response to a change in LET. At lower LETs, there is a greater chance that the precharge PMOS device can pull the node back to Vdd before evaluation begins.

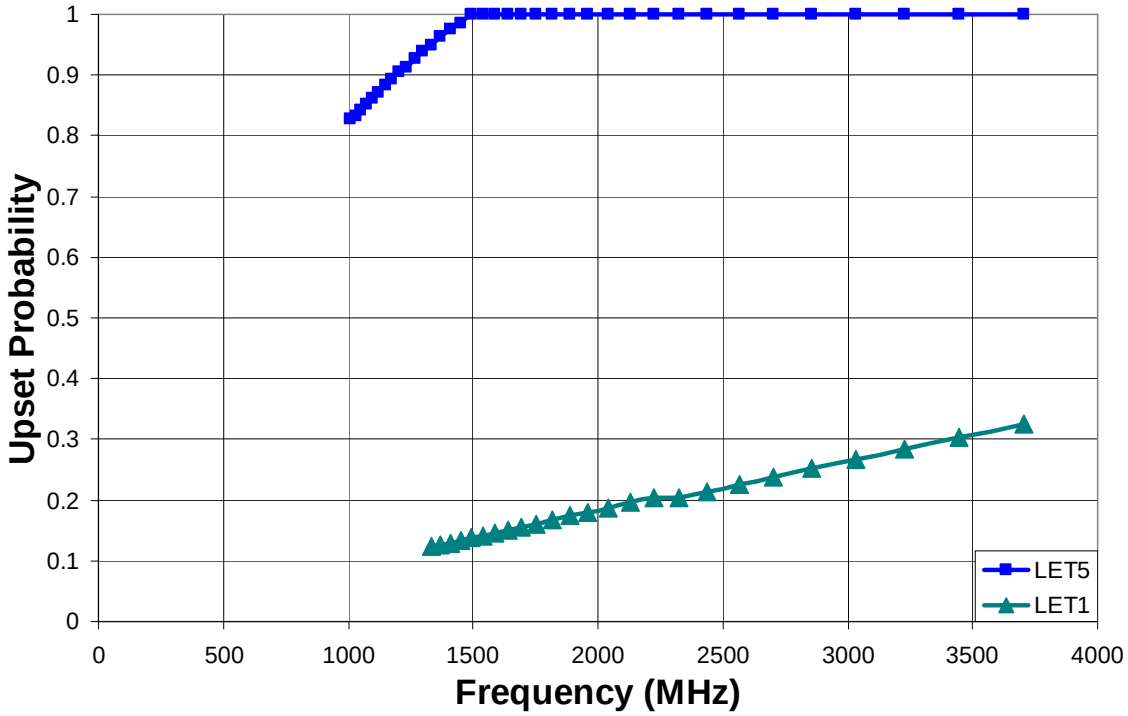

Fig. 21. 90 nm Precharge LET effects

The evaluation phase does not show a strong dependence on the LET (Fig. 22). This result has a similar explanation as to why a keeper does little to harden this phase. Once the charge is lost on the node, it will not recover until the precharge phase. The

LET simply needs to be large enough to deposit enough charge and reduce the voltage to a logic ‘0’.

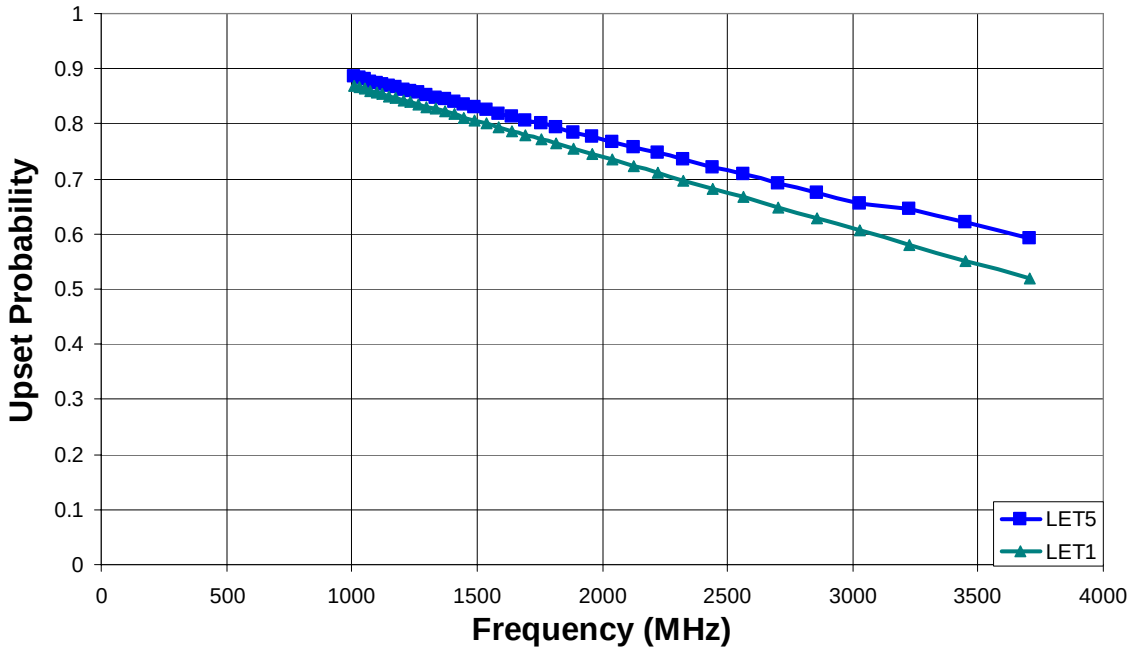

Fig. 22. 90 nm Evaluate LET effects

Static And Dynamic Comparisons

The total upset probability of the static circuit is plotted with the dynamic circuit in Fig. 23 for both 130 nm and 90 nm technologies. The static upset probability increases linearly with frequency as expected due to setup-and-hold time requirements. The dynamic upset probability increases slowly up to a point, and then decreases slightly. The positive slope section is due to the fact that precharge upset probability is increasing faster than the evaluation upset probability is decreasing. The decrease at the end is due to the fact that around 2 GHz, the precharge upset probability saturates. The evaluation

upset probability continues to decrease since the evaluate charge loss mechanism is three times more likely to occur than the charge gain upset mechanism for this circuit. If the charge gain mechanism had dominated, then the upset probability would have slightly increased and then saturated. However, this increase would still be less than the static increase. Hardening techniques for dynamic logic could improve the upset probability at the expense of the area, speed, or power. For example, increasing the precharge PFET would reduce the large vulnerable time in the precharge phase by providing a stronger current pull-up. Disadvantages would include a larger total circuit area, more power, and a larger vulnerable area.

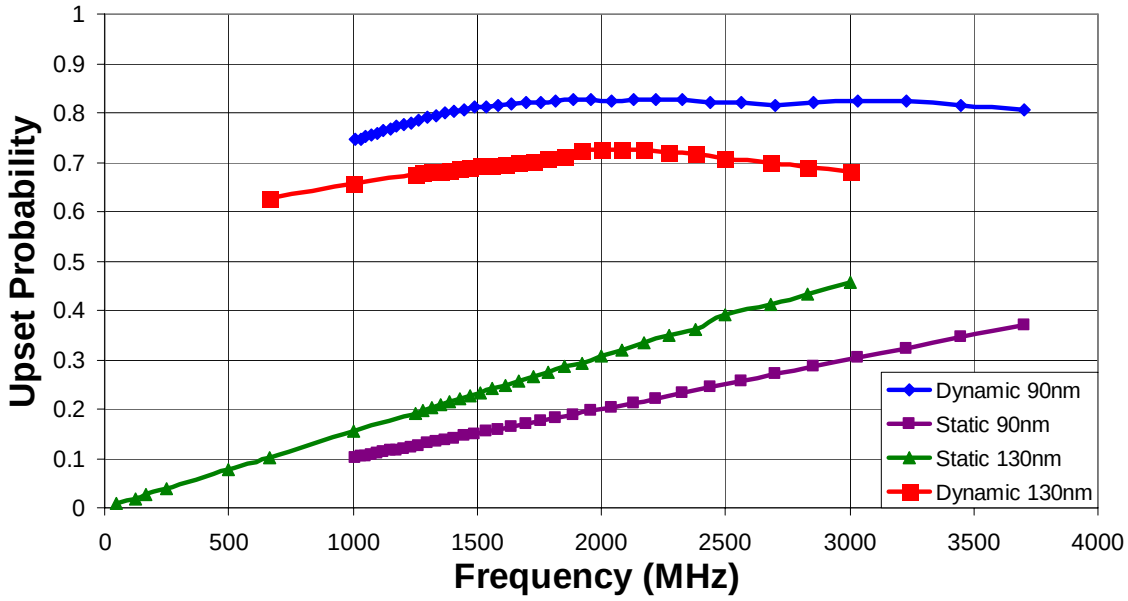

Fig. 23. Total upset probability of the hit node in static and dynamic 3-stage AND gates

CHAPTER VI

DYNAMIC AND STATIC NODAL ANALYSIS

A nodal analysis was performed using dynamic full adder circuit in Fig. 24 and the static full adder circuit in Fig. 25. The dynamic full adder was derived from the dynamic circuitry used in the Itanium-2 Microprocessor [16]. The circuit uses "footless" dual-rail domino logic with an inverter PFET-to-NFET size ratio of 5:1. The maximum delay on this circuit was found by simulation to be 161 ps including a 15% margin. The circuit contains 16 total nodes that could be affected by an SET. The static circuit used standard CMOS NAND gates. Maximum delay for this circuit was found to be 454 ps with a 15% margin. The static circuit consists of a total of 18 nodes. Each node was hit with a transient current derived from a mixed-mode analysis of an N-hit having a total charge of 24 fC at 10 ps intervals across the clock period.

Each circuit was also laid out in Virtuoso to determine the vulnerable area. The vulnerable area is defined as the drain area of each transistor connected to a vulnerable node. For the dynamic and static adders, the vulnerable area was found to be 3.65 μm^2 and 2.16 μm^2 respectively.

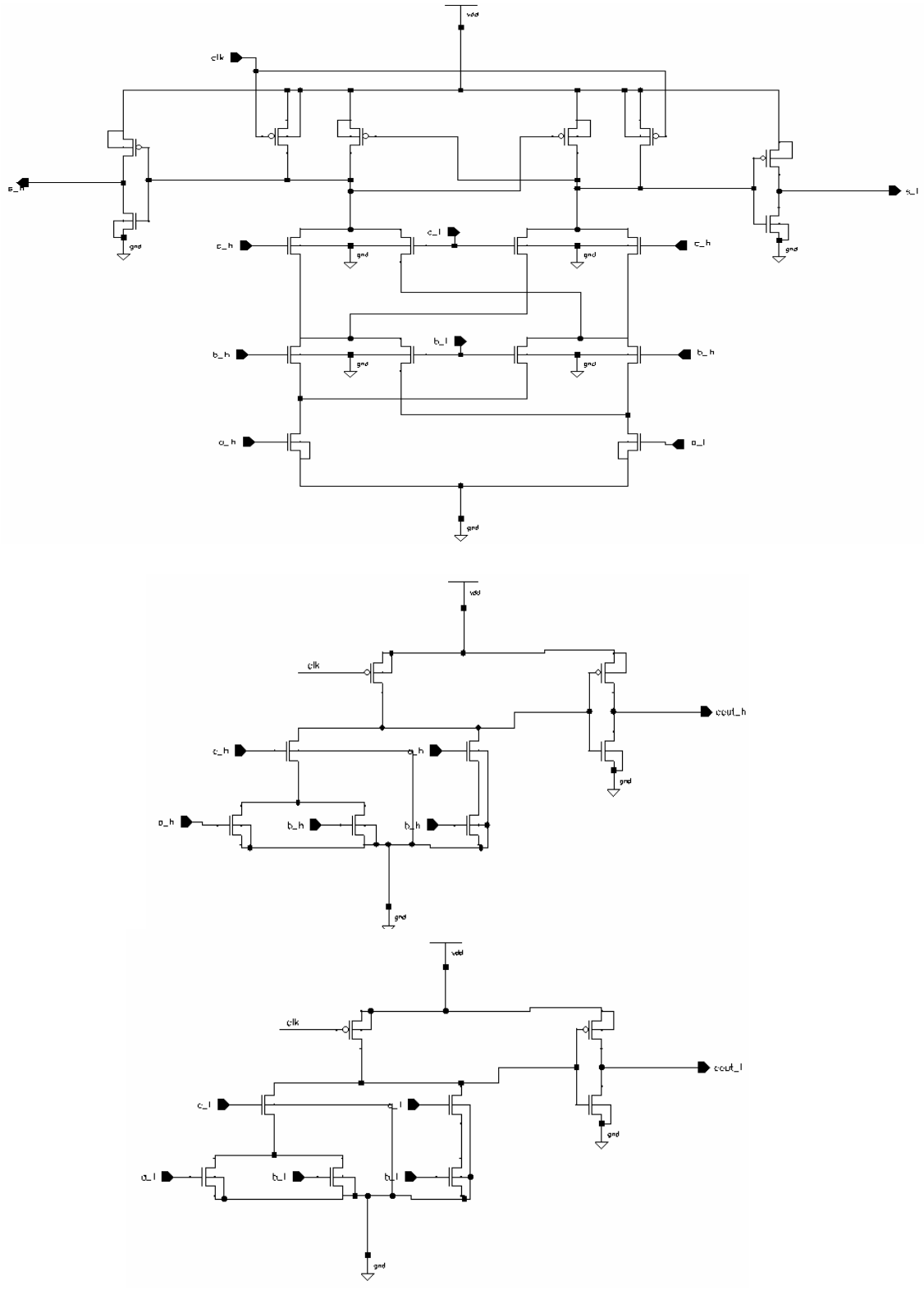

Fig. 24. Dynamic Full Adder Circuit

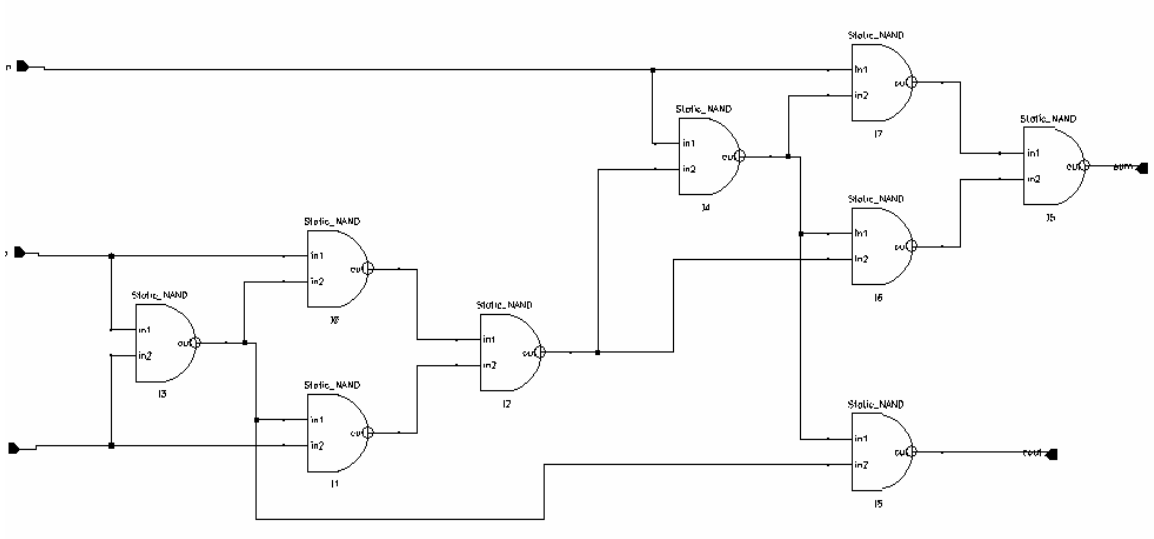

Fig. 25. Static Full Adder Circuit

Each node's upset probabilities were added together to establish a final "vulnerability number" for the circuit. The number was determined as follows:

$$\sum_{All\ Nodes} (\text{VulnerableTime}_{node} * \text{Area}_{node})$$

where the *VulnerableTime* was obtained by simulation for each node, while the *Area* of each node was determined by layout. Vulnerability results were plotted against multiple frequencies and can be seen in Fig. 26.

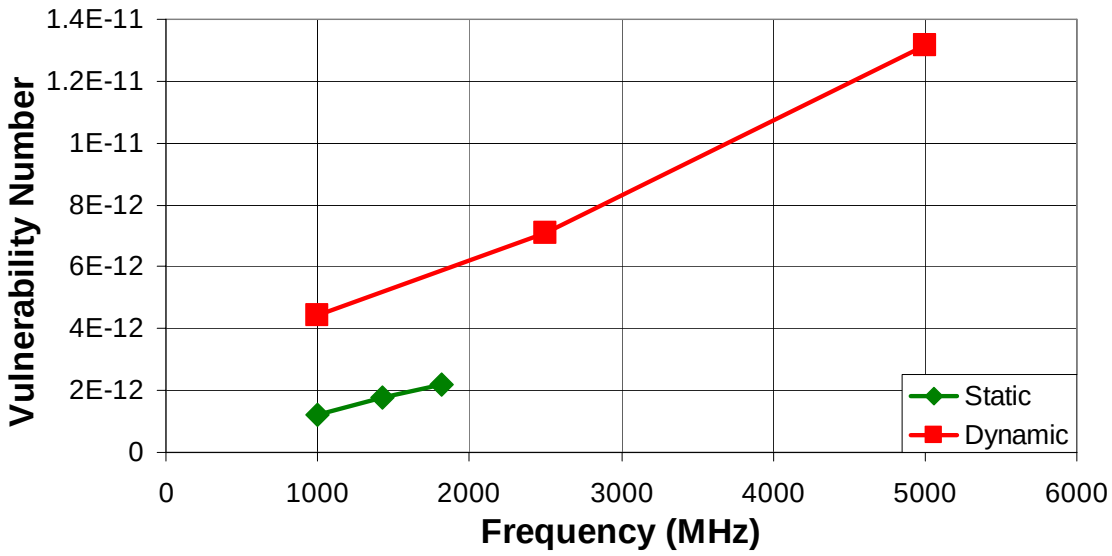

Fig. 26. Static and Dynamic Nodal Vulnerabilities

The previous chapter discussed why the dynamic logic circuit is more vulnerable than the static logic circuit. At 1000 MHz, the dynamic circuit is 3.72 times more vulnerable than the static circuit. The overall trend of increasing vulnerability with increasing frequency continues. While it is true that during the evaluate phase, the dynamic nodes generally decrease in upset probability with increasing frequency; there are only four dynamic nodes in the adder circuit out of a total of 16. As a result, the vulnerability continues to increase with frequency as the additional nodes exhibit static-like response. Because the dynamic circuits have a smaller critical charge required to upset, the upset probabilities are higher than the static circuits.

CHAPTER VII

CONCLUSION

This thesis has analyzed the effects of SETs in dynamic logic circuitry. Simulations in 130 nm and 90 nm technologies were performed for both static and dynamic logic circuits. Dynamic precharge upset probability was found to increase with frequency due to dynamic circuits operating in a static-like state for a significant portion of the clock cycle. Two types of upsets were found in the evaluation phase. The charge loss upset decreases the upset probability, since an upset must be latched before the next precharge phase. At higher frequencies, the precharge phase occurs more often. The charge gain upset increases the upset probability by delaying the node's discharge. At higher frequencies, this delay is long enough to cause an upset. The number of stages present in the circuit has little effect on the upset probability for both static logic and the precharge phase of dynamic logic (assuming hits occur at random times). During the evaluate phase, the further the hit is from a latch, the less likely it will propagate and become latched causing an upset. A keeper device can be used to help mitigate upsets in the precharge phase by providing static-like feedback onto the dynamic node. As with static logic, larger LETs in dynamic logic lead to a greater vulnerability in the precharge phase. The evaluation phase does not show as large a sensitivity to LET because the floating node has a relatively small critical charge. As long as the critical charge is reached, a similar upset response will occur. A full nodal analysis was preformed to determine overall circuit vulnerability. This analysis took both upset probability and

circuit area into account. The dynamic circuit was found to be approximately 3.72 times more vulnerable than the static equivalent circuit. Based on the 130 nm and 90 nm simulation results, this trend is expected to continue for the near future.

Historically, dynamic logic has not been considered well-suited for applications in radiation environments. As this research has shown, this conclusion is valid down to the 90 nm process node, and should remain valid for the foreseeable future. While tradeoffs exist, in general the single-event vulnerability of dynamic logic gates will remain much greater than the vulnerability of equivalent static logic gates.

APPENDIX

Spice Circuit Schematics

The following are schematics with device sizes used in simulations. Simulations were performed using the Cadence Spectre spice simulator.

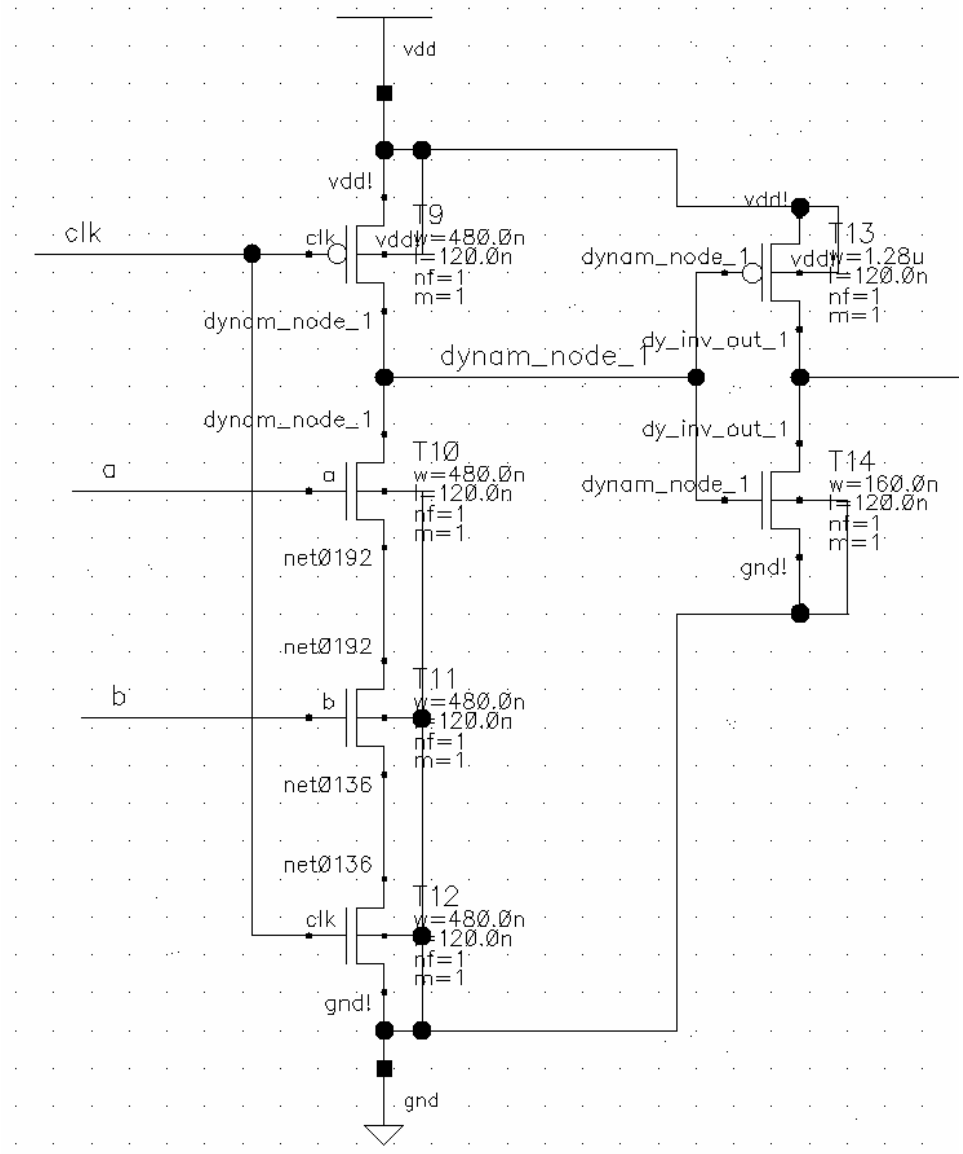

Fig. 27. 130nm Dynamic AND Gate Used

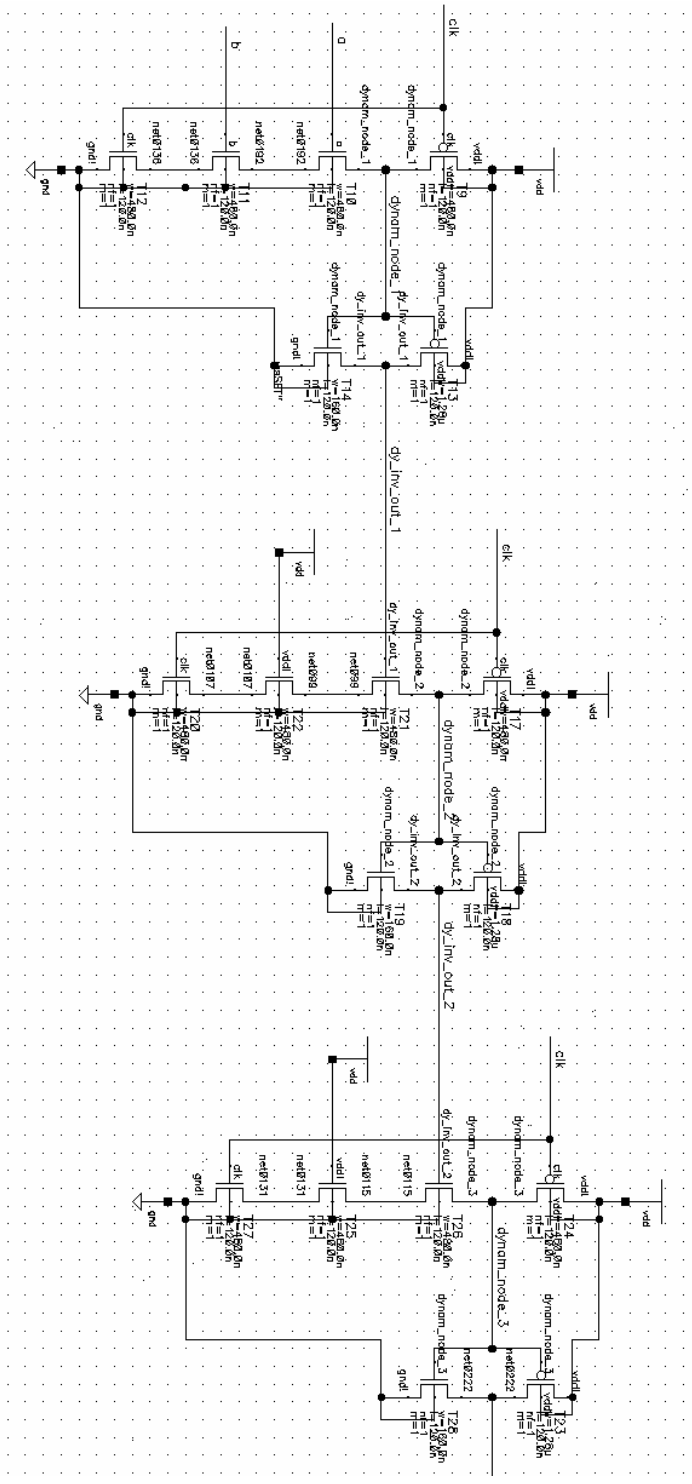

Fig. 28. 130nm Dynamic AND Gates In Series

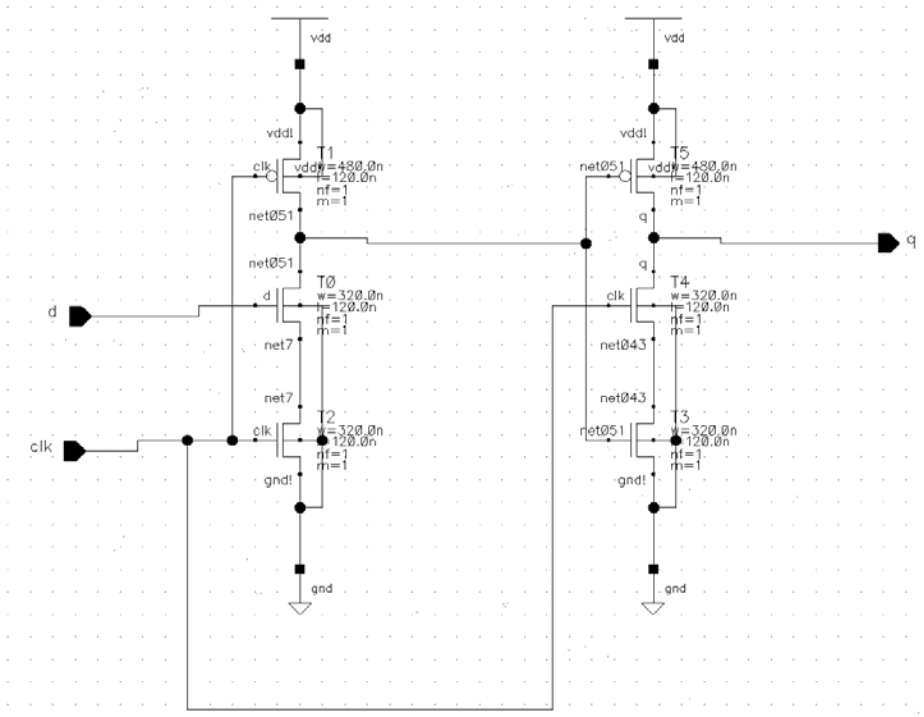

Fig. 29. 130nm Dynamic NMOS Latch Used

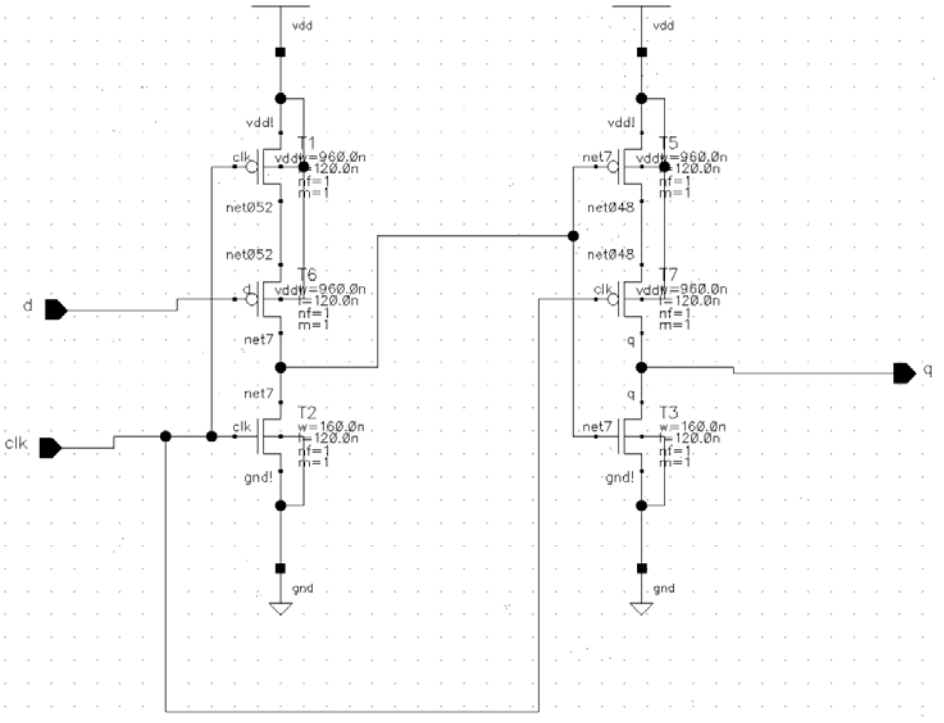

Fig. 30. 130nm Dynamic PMOS Latch Used

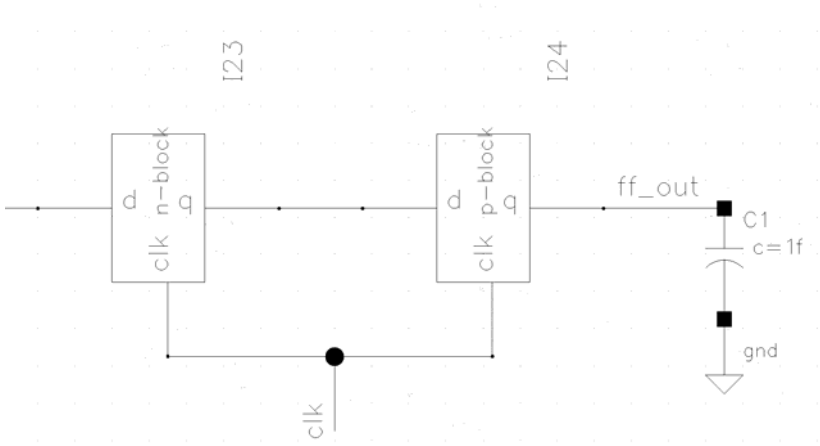

Fig. 31. Dynamic Flip-flop Connections

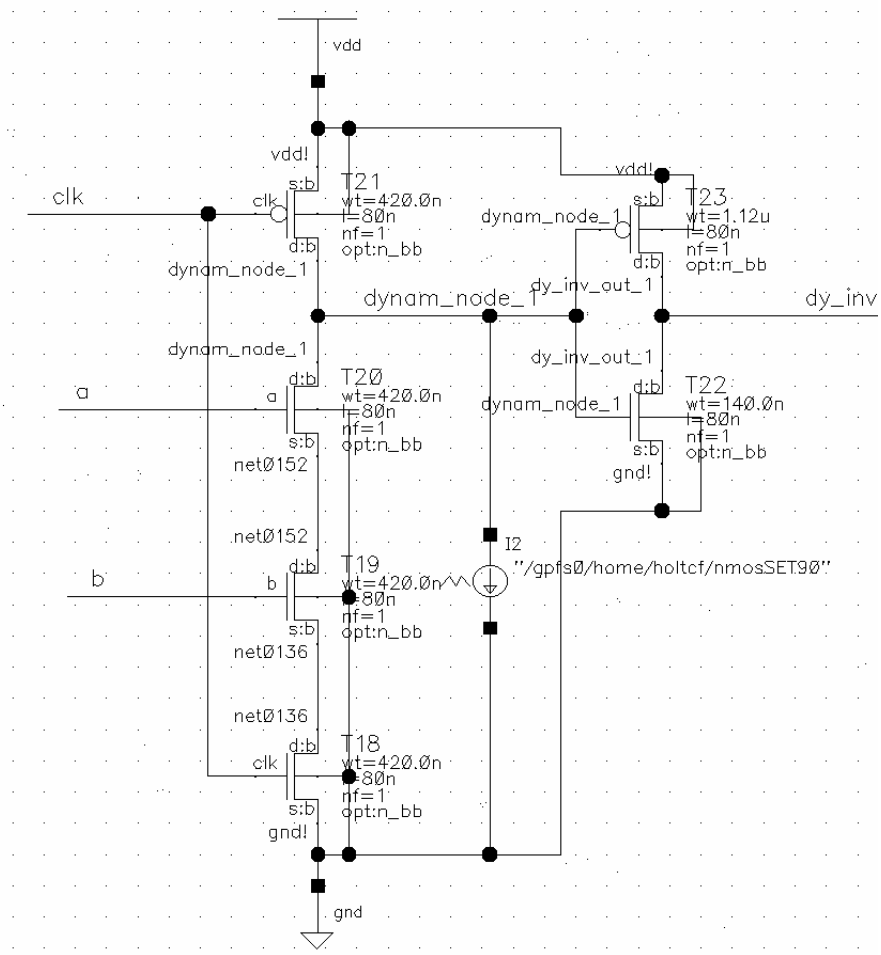

Fig. 32. 90nm Dynamic AND Gate

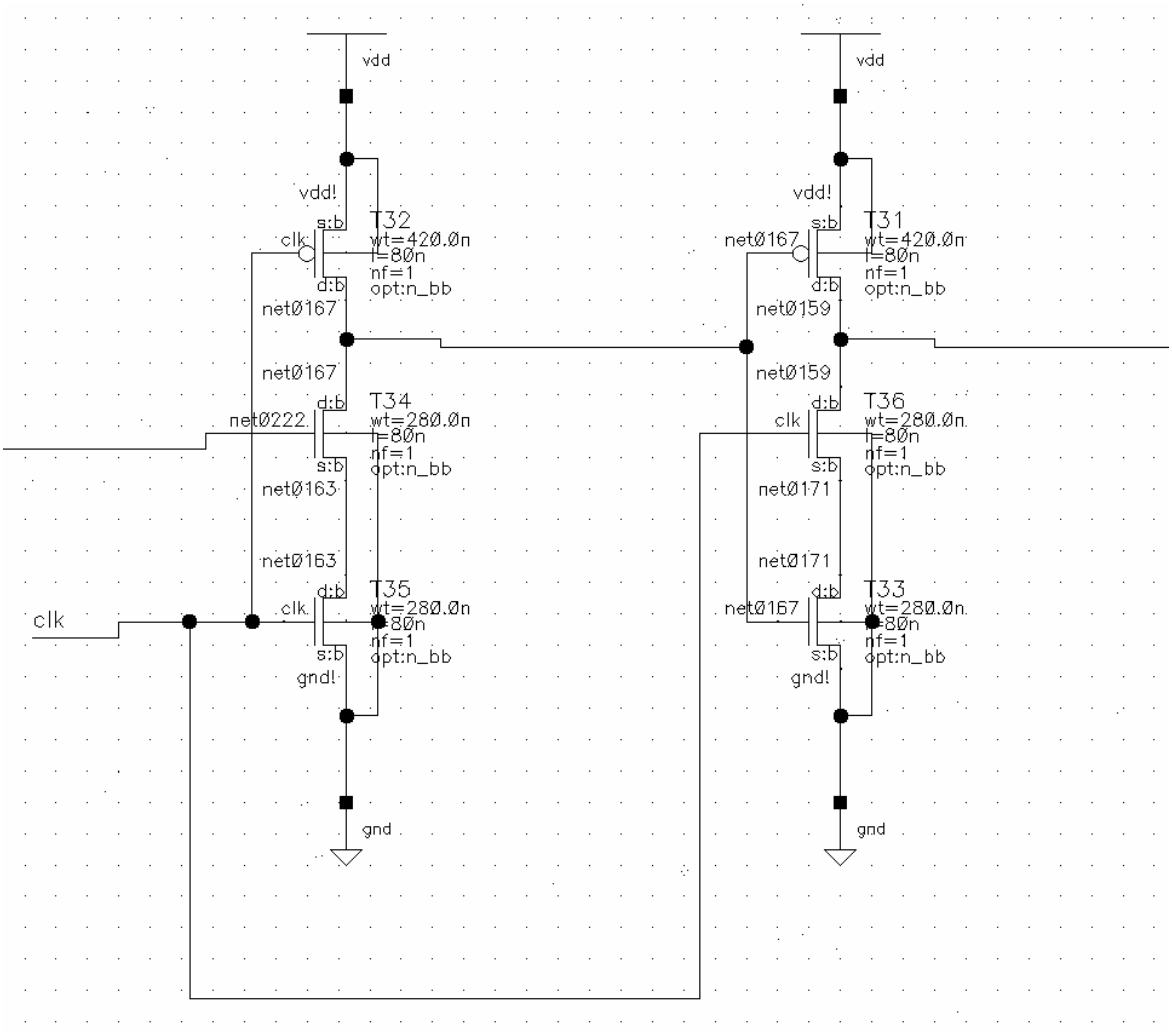

Fig. 33. 90nm Dynamic NMOS Latch

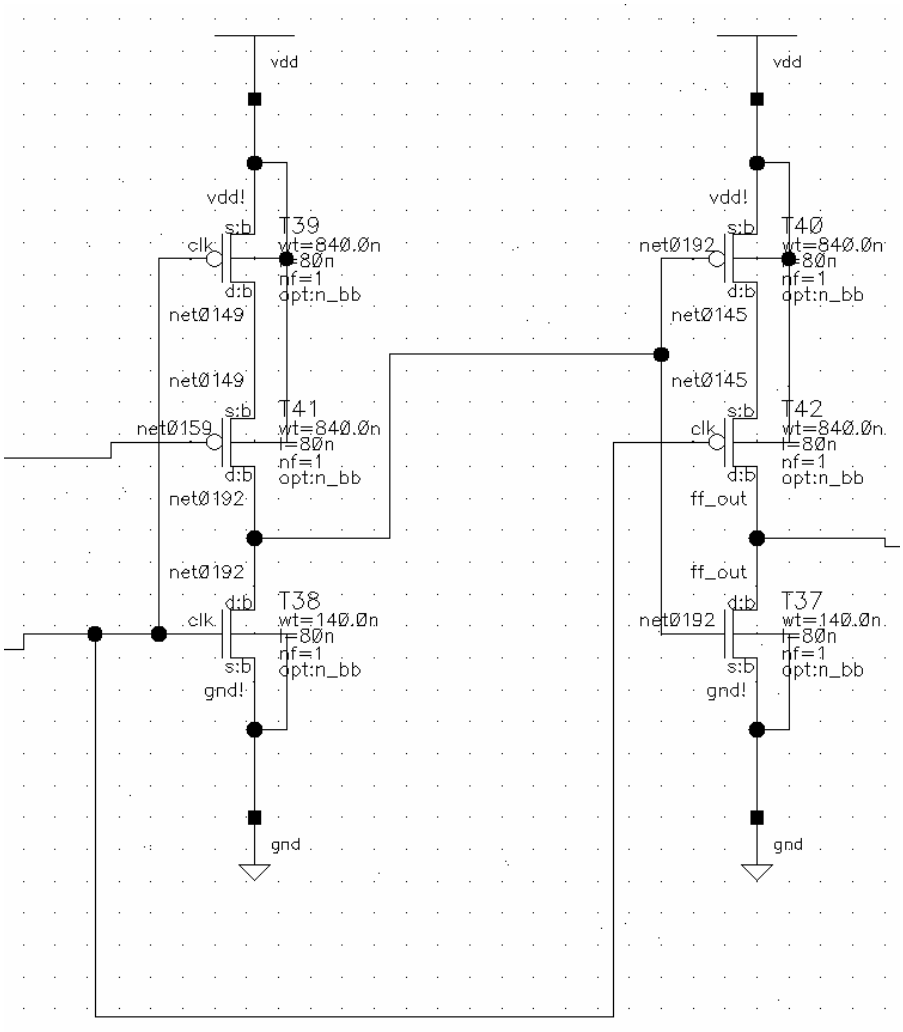

Fig. 34. 90nm Dynamic PMOS Latch

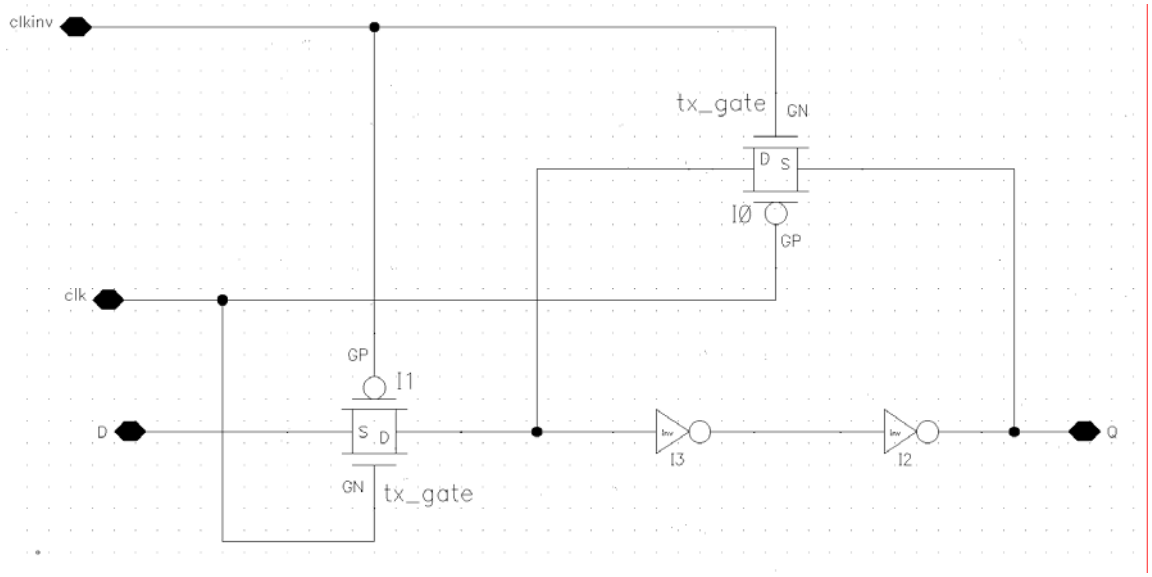

Fig. 35. Static Latch Used

Bash Script Used To Run Spectre Simulations

This file contains an example of a bash script used to run all of the spectre simulations. The example here is a dynamic 90nm PHIT during the evaluation phase. The script consists of two "for" loops that loop across each clock period and for incrementing frequencies. Each simulation produces and output file with the voltage level of the flip-flop which is used to determine if an upset occurs.

```
#!/bin/bash
#PBS -M christopher.f.holt@vanderbilt.edu
#PBS -m bae
#PBS -l nodes=4:ppn=2:x86
#PBS -l walltime=0:10:00
#PBS -l cput=0:40:00
#PBS -o test_job_submit.out
#PBS -j oe
CLKWIDTH=270
CLKHALF=135
CLKTHING=270
WORD1="Clk-"
```

```
WORD2="p__SET-"
for ((CLKWIDTH=270; CLKWIDTH<=1000; CLKWIDTH+=20))
do
let "CLKHALF=(CLKWIDTH/2)"
let "CLKTHING=(CLKWIDTH/10)"
let "PULSETIME= (CLKWIDTH)"
let "PULSESTART = PULSETIME"
for ((PULSETIME=PULSETIME; PULSETIME<=(PULSESTART + CLKHALF);
PULSETIME+=2))
do
echo "// Generated for: spectre
// Generated on: Jul  3 11:47:48 2006
// Design library name: Chris_lib
// Design cell name: SET_TESTING_DYNAMIC_90nm
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
\"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/f
ixed_corner.scs\"
include
\"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/d
esign.scs\"
include
\"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/p
rocess.scs\"

// Library name: Chris_lib
// Cell name: DY_LATCH_PBLOCK_90nm
// View name: schematic
subckt DY_LATCH_PBLOCK_90nm clk d q
    T0 (q net7 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f as=33.6f \
        pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T2 (net7 clk 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f as=33.6f \
        pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n \
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T4 (net052 clk vdd! vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f \
        as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T6 (net048 net7 vdd! vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f
\
        as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T1 (net7 d net052 vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f \
        as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
```

```
    T5 (q clk net048 vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f \
        as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends DY_LATCH_PBLOCK_90nm
// End of subcircuit definition.

// Library name: Chris_lib
// Cell name: DY_LATCH_NBLOCK_90nm
// View name: schematic
subckt DY_LATCH_NBLOCK_90nm clk d q
    T7 (q net051 vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T1 (net051 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T6 (net043 net051 0 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f
as=67.2f \
        pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T3 (net051 d net7 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f
as=67.2f \
        pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T2 (net7 clk 0 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f as=67.2f \
        pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (q clk net043 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f as=67.2f
\
        pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends DY_LATCH_NBLOCK_90nm
// End of subcircuit definition.

// Library name: Chris_lib
// Cell name: SET_TESTING_DYNAMIC_90nm
// View name: schematic
I74 (clk net64 ff_out) DY_LATCH_PBLOCK_90nm
I73 (clk net0222 net64) DY_LATCH_NBLOCK_90nm
T0 (net0222 dynam_node_3 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1
ad=268.8f \
        as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
```

```
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T7 (dy_inv_out_2 dynam_node_2 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1 \
        ad=268.8f as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T17 (dynam_node_2 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1
ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T21 (dynam_node_1 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1
ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T23 (dy_inv_out_1 dynam_node_1 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1
\
        ad=268.8f as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T5 (dynam_node_3 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f
\
        as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T1 (net0222 dynam_node_3 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f \
        as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T8 (net0107 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
\
        pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T15 (net099 vdd! net0107 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T16 (dynam_node_2 dy_inv_out_1 net099 0) nfet w=420.0n l=80n par=1 m=1
\
        ad=100.8f as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 \
        rgatemod=0 sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
\
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T6 (dy_inv_out_2 dynam_node_2 0 0) nfet w=140.0n l=80n par=1 m=1
ad=33.6f \
        as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
```

```
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T22 (dy_inv_out_1 dynam_node_1 0 0) nfet w=140.0n l=80n par=1 m=1
ad=33.6f \
        as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T3 (net0115 vdd! net0131 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T18 (net0136 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
\
        pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T20 (dynam_node_1 a net0152 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f
\
        as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T4 (dynam_node_3 dy_inv_out_2 net0115 0) nfet w=420.0n l=80n par=1 m=1
\
        ad=100.8f as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 \
        rgatemod=0 sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
\
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T2 (net0131 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
\
        pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
\
        sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T19 (net0152 b net0136 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f \
        as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
\
        sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p \
        panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
V1 (clk 0) vsource type=pulse val0=0.0 val1=1.2 period=${CLKWIDTH}p
delay=0 \
        rise=10p fall=10p width=${CLKHALF}p
I2 (vdd! dynam_node_1) isource
file=\"/gpfs0/home/holtcf/nmosSET90let1\" type=pwl \
        delay=${PULSETIME}p
C1 (ff_out 0) capacitor c=500.0a
V11 (a 0) vsource dc=1.2 type=dc
V10 (b 0) vsource dc=1.2 type=dc
V0 (vdd! 0) vsource dc=1.2 type=dc
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27
\
    tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
```

```
    sensfile=\"../psf/sens.output\"
tran tran stop=${CLKWIDTH}*4p write=\"spectre.ic\"
writefinal=\"spectre.fc\" \
    annotate=status maxiters=5
Settings options rawfmt=psfascii
save ff_out clk dynam_node_1
saveOptions options save=selected
">stuff10.scs
spectre stuff10.scs
cp /home/holtcf/stuff10.raw/tran.tran /home/holtcf/stuff10.raw/test.dat
awk '/ff_out/{print $2}' /home/holtcf/stuff10.raw/tran.tran >
/home/holtcf/stuff10.raw/ff_out.dat
awk '/time/{print $2}' /home/holtcf/stuff10.raw/tran.tran >
/home/holtcf/stuff10.raw/time.dat
awk '/clk/{print $2}' /home/holtcf/stuff10.raw/tran.tran >
/home/holtcf/stuff10.raw/clk.dat
awk '/dynam_node_1/{print $2}' /home/holtcf/stuff10.raw/tran.tran >
/home/holtcf/stuff10.raw/dynam_node_1.dat
sed -e '1,2d' /home/holtcf/stuff10.raw/time.dat >
/home/holtcf/stuff10.raw/timefixed.dat
sed -e '1d' /home/holtcf/stuff10.raw/ff_out.dat >
/home/holtcf/stuff10.raw/ff_outfixed.dat
sed -e '1d' /home/holtcf/stuff10.raw/clk.dat >
/home/holtcf/stuff10.raw/clkfixed.dat
sed -e '1d' /home/holtcf/stuff10.raw/dynam_node_1.dat >
/home/holtcf/stuff10.raw/dynam_node_1fixed.dat
paste /home/holtcf/stuff10.raw/timefixed.dat
/home/holtcf/stuff10.raw/ff_outfixed.dat
/home/holtcf/stuff10.raw/clkfixed.dat
/home/holtcf/stuff10.raw/dynam_node_1fixed.dat >
/home/holtcf/stuff10.raw/$WORD1$CLKWIDTH$WORD2$PULSETIME.dat
done
                                    done
```

The file that is generated from the above and then run using spectre is as follows.

```
// Generated for: spectre
// Generated on: Jul  3 11:47:48 2006
// Design library name: Chris_lib
// Design cell name: SET_TESTING_DYNAMIC_90nm
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/fi
xed_corner.scs"
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/de
sign.scs"
```

```
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmos9sf/V2.0.0.1IBM/Spectre/models/pr
ocess.scs"

// Library name: Chris_lib
// Cell name: DY_LATCH_PBLOCK_90nm
// View name: schematic
subckt DY_LATCH_PBLOCK_90nm clk d q
    T0 (q net7 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f as=33.6f
pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T2 (net7 clk 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f as=33.6f
pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T4 (net052 clk vdd! vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f
as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T6 (net048 net7 vdd! vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f
as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T1 (net7 d net052 vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f
as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T5 (q clk net048 vdd!) pfet w=840.0n l=80n par=1 m=1 ad=201.6f
as=201.6f pd=2.16u ps=2.16u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends DY_LATCH_PBLOCK_90nm
// End of subcircuit definition.

// Library name: Chris_lib
// Cell name: DY_LATCH_NBLOCK_90nm
// View name: schematic
subckt DY_LATCH_NBLOCK_90nm clk d q
    T7 (q net051 vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T1 (net051 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T6 (net043 net051 0 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f
as=67.2f         pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n         sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p         panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T3 (net051 d net7 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f
as=67.2f         pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n         sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p         panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T2 (net7 clk 0 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f as=67.2f
pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
```

```
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
    T0 (q clk net043 0) nfet w=280.0n l=80n par=1 m=1 ad=67.2f as=67.2f
pd=1.04u ps=1.04u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
ends DY_LATCH_NBLOCK_90nm
// End of subcircuit definition.

// Library name: Chris_lib
// Cell name: SET_TESTING_DYNAMIC_90nm
// View name: schematic
I74 (clk net64 ff_out) DY_LATCH_PBLOCK_90nm
I73 (clk net0222 net64) DY_LATCH_NBLOCK_90nm
T0 (net0222 dynam_node_3 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1
ad=268.8f         as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n         sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p         panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T7 (dy_inv_out_2 dynam_node_2 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1
ad=268.8f as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T17 (dynam_node_2 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1
ad=100.8f         as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n         sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p         panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T21 (dynam_node_1 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1
ad=100.8f         as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n         sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p         panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T23 (dy_inv_out_1 dynam_node_1 vdd! vdd!) pfet w=1.12u l=80n par=1 m=1
ad=268.8f as=268.8f pd=2.72u ps=2.72u nf=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T5 (dynam_node_3 clk vdd! vdd!) pfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T1 (net0222 dynam_node_3 0 0) nfet w=140.0n l=80n par=1 m=1 ad=33.6f
as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T8 (net0107 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T15 (net099 vdd! net0107 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T16 (dynam_node_2 dy_inv_out_1 net099 0) nfet w=420.0n l=80n par=1 m=1
ad=100.8f as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0
rgatemod=0 sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T6 (dy_inv_out_2 dynam_node_2 0 0) nfet w=140.0n l=80n par=1 m=1
ad=33.6f         as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0
```

```
rgatemod=0         sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
panw4=0p         panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T22 (dy_inv_out_1 dynam_node_1 0 0) nfet w=140.0n l=80n par=1 m=1
ad=33.6f         as=33.6f pd=760.0n ps=760.0n nf=1 ptwell=1 dtemp=0.0
rgatemod=0         sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
panw4=0p         panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T3 (net0115 vdd! net0131 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T18 (net0136 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T20 (dynam_node_1 a net0152 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T4 (dynam_node_3 dy_inv_out_2 net0115 0) nfet w=420.0n l=80n par=1 m=1
ad=100.8f as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0
rgatemod=0 sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p
panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T2 (net0131 clk 0 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f as=100.8f
pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0 sa=240.0n
sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p
panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
T19 (net0152 b net0136 0) nfet w=420.0n l=80n par=1 m=1 ad=100.8f
as=100.8f pd=1.32u ps=1.32u nf=1 ptwell=1 dtemp=0.0 rgatemod=0
sa=240.0n sb=240.0n sd=0 panw1=0p panw2=0p panw3=0p panw4=0p
panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p
V1 (clk 0) vsource type=pulse val0=0.0 val1=1.2 period=670p delay=0
rise=10p fall=10p width=335p
I2 (vdd! dynam_node_1) isource file="/gpfs0/home/holtcf/nmosSET90let1"
type=pwl         delay=800p
C1 (ff_out 0) capacitor c=500.0a
V11 (a 0) vsource dc=1.2 type=dc
V10 (b 0) vsource dc=1.2 type=dc
V0 (vdd! 0) vsource dc=1.2 type=dc
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27
tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5
digits=5 cols=80 pivrel=1e-3 ckptclock=1800
sensfile="../psf/sens.output"
tran tran stop=670*4p write="spectre.ic" writefinal="spectre.fc"
annotate=status maxiters=5
Settings options rawfmt=psfascii
save ff_out clk dynam_node_1
saveOptions options save=selected
```

Desis File Used For 3D mixed-mode 3-Stage AND Gate Transient Current Extraction

This file contains the netlist for the mixed-mode simulation used in Desis. The transient current obtained from this simulation was used in the previous Spectre simulations.

```
######################################################################
### MIXED-MODE 130nm 3 Dynamic AND GATES NHIT During EVALUATE######
######################################################################


DEVICE NMOS_480n{
File  {
        Grid    = "NMOS_480n_msh.grd"
        Doping  = "NMOS_480n_msh.dat"
        Param   = "dessis.par"
        }

Electrode {
        { Name="Drain"         Voltage=1.2  }
      { Name="Gate"          Voltage=0.0  }
        { Name="Source"        Voltage=0.0  }
      { Name="Pwell"          Voltage=0.0  }
        { Name="Substrate"      Voltage=0.0  }
      }


Physics {
        Recombination(SRH Auger) #TPA_gen
        Mobility(Phumob HighFieldsat Enormal)
        EffectiveIntrinsicDensity( OldSlotboom )
      Fermi
      HeavyIon(
      time=3.81e-10
      length=5
      wt_hi=0.05
      location=(0.25,0,0)
      direction=(0,0,1)
      LET_f=0.05
      Gaussian
      Picocoulomb )
      }



Plot  {
        Potential Electricfield
```

```
        eDensity hDensity
        eCurrent/Vector hCurrent/Vector
        TotalCurrent/Vector
        SRH Auger Avalanche
        eMobility hMobility
        eQuasiFermi hQuasiFermi
        eGradQuasiFermi hGradQuasiFermi
        eEparallel hEparallel
        eMobility hMobility
        eVelocity hVelocity
        DonorConcentration Acceptorconcentration
        Doping SpaceCharge
        ConductionBand ValenceBand
        BandGap Affinity
        xMoleFraction
        eTemperature hTemperature
        HeavyIonChargeDensity
      }
}

Math  {
      WallClock
      Extrapolate
      Derivatives
      RelErrControl
      Iterations=15
      notdamped=100
      Newdiscretization
      Method=ILS
      RecBoxIntegr
      number_of_threads=2
      }

File  {
      Output = "WORKING_NHIT_EVAL_130_log.out"
      SPICEPath = "." ###path where your spice models are ###
      Plot    = "WORKING_NHIT_EVAL_130_plot.dat"
      Current = "WORKING_NHIT_EVAL_130_current.plt"
        }

System      {

      Vsource_pset      VDD   (vdd 0)     {dc = 1.2}  ###voltage source
(HIGH 0) are node names###
      Vsource_pset      clock (clk 0)     {pulse = (0 1.2 0 1e-11 1e-11
1.8e-10 3.6e-10)}  ###voltage source (clk 0) are node names###


######## mosfet (drain gate source bulk)  ####################
###This is the TCAD device,I am referencing the device above, and
connecting the electrodes to spice nodes###
      NMOS_480n   device1     ("Drain" = dynam_node_1
                        "Gate"       = 0
                   "Source"   = net0192
                   "Substrate"      = 0
                   "Pwell"    = 0)
```

```
###These are spice transistors, NMOS13 & PMOS13 are the names from the
spice model file####

      PMOS13      MP50  (net0229 clk vdd vdd)
                  {w = 960e-9       l = 0.12e-6
                  pd = 2.885e-6     ps = 2.885e-6
                  ad = 4.83e-13     as = 4.83e-13}

      PMOS13      MP7   (ff_out clk net0221 vdd)
                  {w = 960e-9       l = 0.12e-6
                  pd = 2.885e-6     ps = 2.885e-6
                  ad = 4.83e-13     as = 4.83e-13}

      PMOS13      MP49  (net0221 net0266 vdd vdd)
                  {w = 960e-9       l = 0.12e-6
                  pd = 2.885e-6     ps = 2.885e-6
                  ad = 4.83e-13     as = 4.83e-13}

      PMOS13      MP6   (net0266 net64 net0229 vdd)
                  {w = 960e-9       l = 0.12e-6
                  pd = 2.885e-6     ps = 2.885e-6
                  ad = 4.83e-13     as = 4.83e-13}

      PMOS13      MP1   (net0114 clk vdd vdd)
                  {w = 480e-9       l = 0.12e-6
                  pd = 1.925e-6     ps = 1.925e-6
                  ad = 2.29e-13     as = 2.29e-13}

      PMOS13      MP5   (net64 net0114 vdd vdd)
                  {w = 480e-9       l = 0.12e-6
                  pd = 1.925e-6     ps = 1.925e-6
                  ad = 2.29e-13     as = 2.29e-13}

      PMOS13      MP17  (dynam_node_2 clk vdd vdd)
                  {w = 480e-9       l = 0.12e-6
                  pd = 1.925e-6     ps = 1.925e-6
                  ad = 2.29e-13     as = 2.29e-13}

      PMOS13      MP9   (dynam_node_1 clk vdd vdd)
                  {w = 480e-9       l = 0.12e-6
                  pd = 1.925e-6     ps = 1.925e-6
                  ad = 2.29e-13     as = 2.29e-13}

      PMOS13      MP18  (dy_inv_out_2 dynam_node_2 vdd vdd)
                  {w = 1280e-9      l = 0.12e-6
                  pd = 3.525e-6     ps = 3.525e-6
                  ad = 6.51e-13     as = 6.51e-13}

      PMOS13      MP13  (dy_inv_out_1 dynam_node_1 vdd vdd)
                  {w = 1280e-9      l = 0.12e-6
                  pd = 3.525e-6     ps = 3.525e-6
                  ad = 6.51e-13     as = 6.51e-13}

      PMOS13      MP23  (dy_inv_out_3 dynam_node_3 vdd vdd)
                  {w = 1280e-9      l = 0.12e-6
                  pd = 3.525e-6     ps = 3.525e-6
                  ad = 6.51e-13     as = 6.51e-13}
```

```
PMOS13      MP24  (dynam_node_3 clk vdd vdd)
            {w = 480e-9       l = 0.12e-6
            pd = 1.925e-6     ps = 1.925e-6
            ad = 2.29e-13     as = 2.29e-13}

NMOS13      MN48  (net0266 clk 0 0)
            {w = 160e-9       l = 0.12e-6
            pd = 1.42e-6      ps = 1.42e-6
            ad = 8.8e-14      as = 8.8e-14}

NMOS13      MN47  (ff_out net0266 0 0)
            {w = 160e-9       l = 0.12e-6
            pd = 1.42e-6      ps = 1.42e-6
            ad = 8.8e-14      as = 8.8e-14}

NMOS13      MN0   (net0114 dy_inv_out_3 net0118 0)
            {w = 320e-9       l = 0.12e-6
            pd = 1.605e-6     ps = 1.605e-6
            ad = 1.45e-13     as = 1.45e-13}

NMOS13      MN2   (net0118 clk 0 0)
            {w = 320e-9       l = 0.12e-6
            pd = 1.605e-6     ps = 1.605e-6
            ad = 1.45e-13     as = 1.45e-13}

NMOS13      MN4   (net64 clk net0126 0)
            {w = 320e-9       l = 0.12e-6
            pd = 1.605e-6     ps = 1.605e-6
            ad = 1.45e-13     as = 1.45e-13}

NMOS13      MN3   (net0126 net0114 0 0)
            {w = 320e-9       l = 0.12e-6
            pd = 1.605e-6     ps = 1.605e-6
            ad = 1.45e-13     as = 1.45e-13}

NMOS13      MN21  (dynam_node_2 dy_inv_out_1 net099 0)
            {w = 480e-9       l = 0.12e-6
            pd = 1.925e-6     ps = 1.925e-6
            ad = 2.29e-13     as = 2.29e-13}

NMOS13      MN22  (net099 vdd net0107 0)
            {w = 480e-9       l = 0.12e-6
            pd = 1.925e-6     ps = 1.925e-6
            ad = 2.29e-13     as = 2.29e-13}

NMOS13      MN19  (dy_inv_out_2 dynam_node_2 0 0)
            {w = 160e-9       l = 0.12e-6
            pd = 1.42e-6      ps = 1.42e-6
            ad = 8.8e-14      as = 8.8e-14}

NMOS13      MN20  (net0107 clk 0 0)
            {w = 480e-9       l = 0.12e-6
            pd = 1.925e-6     ps = 1.925e-6
            ad = 2.29e-13     as = 2.29e-13}

NMOS13      MN14  (dy_inv_out_1 dynam_node_1 0 0)
```

```
                {w = 160e-9       l = 0.12e-6
                pd = 1.42e-6      ps = 1.42e-6
                ad = 8.8e-14      as = 8.8e-14}

      NMOS13    MN25  (net0115 vdd net0131 0)
                {w = 480e-9       l = 0.12e-6
                pd = 1.925e-6     ps = 1.925e-6
                ad = 2.29e-13     as = 2.29e-13}

      NMOS13    MN12  (net0136 clk 0 0)
                {w = 480e-9       l = 0.12e-6
                pd = 1.925e-6     ps = 1.925e-6
                ad = 2.29e-13     as = 2.29e-13}

#######THIS IS THE HIT DEVICE ########################################
####  NMOS13    MN10  (dynam_node_1 0 net0192 0)
###             {w = 480e-9       l = 0.12e-6
###             pd = 1.925e-6     ps = 1.925e-6
####            ad = 2.29e-13     as = 2.29e-13}
#####################################################################

      NMOS13    MN26  (dynam_node_3 dy_inv_out_2 net0115 0)
                {w = 480e-9       l = 0.12e-6
                pd = 1.925e-6     ps = 1.925e-6
                ad = 2.29e-13     as = 2.29e-13}

      NMOS13    MN27  (net0131 clk 0 0)
                {w = 480e-9       l = 0.12e-6
                pd = 1.925e-6     ps = 1.925e-6
                ad = 2.29e-13     as = 2.29e-13}

      NMOS13    MN28  (dy_inv_out_3 dynam_node_3 0 0)
                {w = 160e-9       l = 0.12e-6
                pd = 1.42e-6      ps = 1.42e-6
                ad = 8.8e-14      as = 8.8e-14}

      NMOS13    MN11  (net0192 vdd net0136 0)
                {w = 480e-9       l = 0.12e-6
                pd = 1.925e-6     ps = 1.925e-6
                ad = 2.29e-13     as = 2.29e-13}

        Capacitor_pset C1 (ff_out 0) {capacitance = 1e-15}


####this is initializes the node outright to 0 volts, look at the
manual for more information###
Initialize (dynam_node_1 = 1.2)
Initialize (net0192 = 0)
Initialize (net0136 = 0)
Initialize (dy_inv_out_1 = 0)
Initialize (dynam_node_2 = 1.2)
Initialize (net099 = 0)
Initialize (net0107 = 0)
Initialize (dy_inv_out_2 = 0)
Initialize (dynam_node_3 = 1.2)
Initialize (net0115 = 0)
```

```
Initialize (net0131 = 0)
Initialize (dy_inv_out_3 = 0)
Initialize (net0114 = 1.2)
Initialize (net0118 = 0)
Initialize (net0126 = 0)
Initialize (net64 = 0)
Initialize (net0229 = 1.2)
Initialize (net0226 = 1.2)
Initialize (net0221 = 0)
Initialize (ff_out = 0)


###this is for the spice .plt file###
      Plot "WORKING_NHIT_EVAL_130" (time() v(clk) v(ff_out)
v(dy_inv_out_3) v(dy_inv_out_2) v(dy_inv_out_1)
         v(dynam_node_3) v(dynam_node_2) v(dynam_node_1))
       }

Solve{
    Coupled (iterations=100) {Circuit}
    Coupled (iterations=100) {Poisson}
    Coupled (iterations=100) {Poisson Circuit}
    Coupled (iterations=100) {Poisson Circuit Contact}
#    Coupled (iterations=100) {Poisson Hole Contact Circuit}
    Coupled (iterations=100) {Poisson Electron Hole Contact Circuit}

NewCurrentFile="transient_"

Transient (
      InitialTime=0
      FinalTime=3.7e-10
      InitialStep=1e-14
      MaxStep=3e-12
      Increment=1.2)
       {
            coupled {device1.poisson device1.electron device1.hole
device1.contact circuit}
       }

Transient (
      InitialTime=3.7e-10
      FinalTime=5.2e-10
      InitialStep=0.1e-14
      MaxStep=0.2e-12
      Increment=1.2 )
        {
            coupled{device1.poisson device1.electron device1.hole
device1.contact circuit}
            Plot ( FilePrefix="imA" Time=(3.9e-9;4e-9;4.1e-9;4.15e-
9;4.2e-9;4.3e-9;4.5e-9) NoOverwrite)
        }

Transient (
      InitialTime=5.2e-10
      FinalTime=1e-9
      InitialStep=1e-12
      MaxStep=3e-12
```

```
      Increment=1.2 )
        {
           coupled{device1.poisson device1.electron device1.hole
device1.contact circuit}
           Plot (FilePrefix="laterA" Time=(5e-9;6e-9;7e-9;8e-9)
NoOverwrite)
}
}
```

Devise File For The 130nm Struck NMOS Device

Doping, device dimensions, and doping profiles are contained within this file.

```
Controls {
}

Definitions {
      Constant "Profile.Npolysi.Bor" {
            Species = "ArsenicActiveConcentration"
            Value   = 1e+20
      }
      Constant "Profile.Silconst.Bor" {
            Species = "BoronActiveConcentration"
            Value   = 1e+16
      }
      AnalyticalProfile "Profile.DeepPWell.Bor.1" {
      Species = "BoronActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 1e+18, ValueAtDepth =
1e+16, Depth = 0.4)
      LateralFunction = Gauss(Factor = 0.0001)
      }
      AnalyticalProfile "Profile.PWell.Bor.2" {
      Species = "BoronActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 8e+17, ValueAtDepth =
1e+17, Depth = 0.35)
      LateralFunction = Gauss(Factor = 0.01)
      }
      AnalyticalProfile "Profile.PWellCon.Bor.3A" {
      Species = "BoronActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 9e+19, ValueAtDepth =
3e+17, Depth = 0.08)
      LateralFunction = Gauss(Factor = 0.01)
      }
      Constant "Profile.ImplantB" {
            Species = "BoronActiveConcentration"
            Value   = 5e+19
      }
      AnalyticalProfile "drain.ProfileB" {
      Species = "ArsenicActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 2e+20, ValueAtDepth =
1e+17, Depth = 0.08)
      LateralFunction = Gauss(Factor = 0.1)
```

```
      }
      AnalyticalProfile "source.ProfileB" {
      Species = "ArsenicActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 2e+20, ValueAtDepth =
1e+17, Depth = 0.08)
      LateralFunction = Gauss(Factor = 0.1)
      }
      AnalyticalProfile "drainldd.ProfileB" {
      Species = "ArsenicActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 2.15e+18, ValueAtDepth =
1e+17, Depth = 0.03)
      LateralFunction = Gauss(Factor = 0.1)
      }
      AnalyticalProfile "sourceldd.ProfileB" {
      Species = "ArsenicActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 2.15e+18, ValueAtDepth =
1e+17, Depth = 0.03)
      LateralFunction = Gauss(Factor = 0.1)
      }
      AnalyticalProfile "implant.ProfileB" {
      Species = "BoronActiveConcentration"
      Function = Gauss(PeakPos = 0, PeakVal = 6e+18, ValueAtDepth =
1e+17, Depth = 0.0165)
      LateralFunction = Gauss(Factor = 0.0001)
      }
      Refinement "size.whole2" {
            MaxElementSize = ( 0.3 0.5 0.3 )
            MinElementSize = ( 0.1 0.1 0.05 )
      }
      Refinement "size.dopingmeshb" {
            MaxElementSize = ( 0.1 0.1 0.05 )
            MinElementSize = ( 0.05 0.05 0.05 )
            RefineFunction = MaxTransDiff(Variable =
"DopingConcentration",Value = 1)
      }
      Refinement "size.dopingmesh1b" {
            MaxElementSize = ( 0.1 0.1 0.05 )
            MinElementSize = ( 0.025 0.025 0.025 )
            RefineFunction = MaxTransDiff(Variable =
"DopingConcentration",Value = 1)
      }
      Refinement "size.dopingmesh2b" {
            MaxElementSize = ( 0.05 0.1 0.05 )
            MinElementSize = ( 0.01 0.01 0.005 )
            RefineFunction = MaxTransDiff(Variable =
"DopingConcentration",Value = 1)
      }
}

Placements {
      Constant "Place.Npolysi1.Bor" {
            Reference = "Profile.Npolysi.Bor"
            EvaluateWindow {
                  Element = Cuboid [( -0.06 -0.24 -0.0025 ) , ( 0.06
0.24 -0.1425 )]
            }
      }
```

```
      Constant "Place.Npolysi2.Bor" {
            Reference = "Profile.Npolysi.Bor"
            EvaluateWindow {
                  Element = Cuboid [( -0.06 -0.24 -0.025 ) , ( 0.06 -
0.47 -0.1425 )]
            }
      }
      Constant "Place.Npolysi3.Bor" {
            Reference = "Profile.Npolysi.Bor"
            EvaluateWindow {
                  Element = Cuboid [( -0.06 0.24 -0.025 ) , ( 0.06 0.47
-0.1425 )]
            }
      }
      Constant "Place.Silconst.Bor" {
            Reference = "Profile.Silconst.Bor"
            EvaluateWindow {
                  Element = Cuboid [( -5 5 0 ) , ( 5 -5 5 )]
            }
      }
      AnalyticalProfile "Place.DeepPWell.Bor.1" {
            Reference = "Profile.DeepPWell.Bor.1"
            ReferenceElement {
                  Element = Rectangle [( -5 5 1.25 ) , ( 5 -5 1.25 )]
            }
      }
      AnalyticalProfile "Place.PWell.Bor.2" {
            Reference = "Profile.PWell.Bor.2"
            ReferenceElement {
                  Element = Rectangle [( -5 -5 0.45 ) , ( 5 5 0.45 )]
            }
      }
      AnalyticalProfile "Place.PWellCon.Bor.3A" {
            Reference = "Profile.PWellCon.Bor.3A"
            ReferenceElement {
                  Element = Rectangle [( -5 -0.64 0 ) , ( 5 -0.92 0 )]
            }
      }
      Constant "Place.Implant.FrontPA" {
            Reference = "Profile.ImplantB"
            EvaluateWindow {
                  Element = Cuboid [( -0.06 -0.24 0 ) , ( 0.06 -0.485
0.36 )]
            }
      }
      Constant "Place.Implant.BackPA" {
            Reference = "Profile.ImplantB"
            EvaluateWindow {
                  Element = Cuboid [( -0.06 0.24 0 ) , ( 0.06 0.485
0.36 )]
            }
      }
      AnalyticalProfile "drain.Profile.PlaceB" {
            Reference = "drain.ProfileB"
            ReferenceElement {
                  Element = Rectangle [( 0.089 -0.24 0 ) , ( 0.46 0.24
0 )]
```

```
            }
      }
      AnalyticalProfile "source.Profile.PlaceB" {
            Reference = "source.ProfileB"
            ReferenceElement {
                  Element = Rectangle [( -0.089 -0.24 0 ) , ( -0.46
0.24 0 )]
            }
      }
      AnalyticalProfile "drainldd.Profile.PlaceB" {
            Reference = "drainldd.ProfileB"
            ReferenceElement {
                  Element = Rectangle [( 0.039 -0.24 0 ) , ( 0.46 0.24
0 )]
            }
      }
      AnalyticalProfile "sourceldd.Profile.PlaceB" {
            Reference = "sourceldd.ProfileB"
            ReferenceElement {
                  Element = Rectangle [( -0.039 -0.24 0 ) , ( -0.46
0.24 0 )]
            }
      }
      AnalyticalProfile "implant.Profile.PlaceB" {
            Reference = "implant.ProfileB"
            ReferenceElement {
                  Element = Rectangle [( -0.03 -0.24 0.0165 ) , ( 0.03
0.24 0.0165 )]
            }
      }
      Refinement "placement.whole2" {
            Reference = "size.whole2"
            RefineWindow = Cuboid [( -5 5 0 ) , ( 5 -5 5 )]
      }
      Refinement "placement.dopingmeshb" {
            Reference = "size.dopingmeshb"
            RefineWindow = Cuboid [( -5 -0.64 0 ) , ( 5 -0.92 0.1 )]
      }
      Refinement "placement.dopingmesh1b" {
            Reference = "size.dopingmesh1b"
            RefineWindow = Cuboid [( -0.46 -0.5 0 ) , ( 0.46 0.5 0.1 )]
      }
      Refinement "placement.dopingmesh2b" {
            Reference = "size.dopingmesh2b"
            RefineWindow = Cuboid [( -0.07 -0.5 0 ) , ( 0.07 0.5 0.1 )]
      }
}
```

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