TRENDS IN SINGLE EVENT PULSE WIDTHS AND PULSE SHAPES IN DEEP SUBMICRON CMOS

By

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TABLE OF CONTENTS

Page

ACKNOWLEDGMENTS ii

LIST OF FIGURES v

LIST OF TABLES viii

Chapter

I. INTRODUCTION 1

1.1 Overview 1

1.2 Overview of Previous Work 1

1.3 Overview of thesis 2

II. CALIBRATION OF DEVICE MODELS 5

2.1 Variants in a commercial 90nm node 5

2.2 IBM 90nm Device Cross Sections 6

2.3 Results of Electrical Calibration 9

2.4 Compact modeling 11

III. BASIC SINGLE EVENT SIMULATIONS AND PULSE WIDTHS 15

3.1 Collection Depths in 90nm CMOS 16

3.2 Pulse Shapes 19

IV. CONTACT LAYOUT AND PARASITIC BIPOLAR AMPLIFICATION 24

4.1 N-Well Contact Area 25

4.2 N-Well Contact Location 25

V. POTENTIAL MODULATION IN THE SUBSTRATE AND PULSE WIDTHS 27

5.1. Formation of the plateau 29

5.2. Contact placement and the potential pushout 32

5.3. Summary of the mechanism of the plateau 34

5.4 Conclusion 35

VI. THE RECOVERY MECHANISM..........36
6.1. Sanity Checks..........37
6.2. Justifying the presence of hole current 39
6.3. The Recovery Mechanism 44

VII. SUBSTRATE ENGINEERING- EFFECT ON PULSE WIDTHS..........46
7.1. First pass, different substrate profiles, charge collection…..........47
7.2. Diffusion collection 53
7.3. Proper Combination of Substrate Profile and Contact Scheme 54
7.4. Substrate engineering and the longer DSETs 56
7.5. Effect of buried n-type layer 56
7.6. Future Work 63
7.7. Summary 63
CONCLUSION..........65
REFERENCES 66
APPENDIX..........68

LIST OF FIGURES

Figure Page

1. Doping Profiles for Regular Vt High Performance NMOS 7

2. Calibration curves for a 90nm Low Power CMOS...9

3. Calibration curves for a 90nm High Performance CMOS 10

4. Comparison between compact models of Regular Vt High Performance CMOS.........12

5. Comparison between a TCAD and a mixed mode ring oscillator 13

6. Schematic of inverter chain used in mixed mode modeling 15

7. Collection depth estimation for 4 devices...17

8. Distinctly different pulse shapes for an LET of 1 MeV/mg/ cm^2 and one of 20 $MeV/mg/cm^2$..19

9. Current pulse profiles for High Performance NMOS, collected charge, potential pulse profiles at hit node and at circuit terminal 20

10. Current pulse profiles for Low Power NMOS, collected charge, potential pulse profiles at hit node and at circuit terminal 20

11. Current pulse profiles for High Performance PMOS, collected charge, potential pulse profiles at hit node and at circuit terminal 21

12. Current pulse profiles for Low Power PMOS, collected charge, potential pulse profiles at hit node and at circuit terminal 22

13. Summary SEE pulse widths for Low Power and High Performance variants............23

14. CMOS cross section, showing parasitic elements 25

15. FWHM voltage pulse widths for a) varying n-well contact location and b) varying n-well contact area 26

16. Effect of node capacitance and restoring PMOS drive current on pulse width...........28

17. Current SETs for Low Power and High Performance variants for an LET of 20 MeV/mg/cm^2..........28

18. A 2-d slice at the center of device drain (NMOS). First cutline is at the drain, second one is at the well contact..........29

19. A 2-d slice at the center of device drain (NMOS), 10ps into the strike. First cutline is at the drain, second one is at the well contact..........30

20. Diagram of the mechanism of potential collapse and 1D plots of potentials under the drain and well contact for LET=1 and 10 MeV/mg/cm^2..........31

21. Setup for simulation with variation in well contact doping..........32

22. 1-d potential contour plots for highly and lightly doped substrate profiles..........34

23. Current profiles at different terminals of the struck device and potential profile at drain..........37

24. Electron, Hole Concentration and potential plot right underneath the drain contact, as a function of depth..........38

25. Difference between the internal current stimulus and the circuit current stimulus, Kirchoff's law needs to be satisfied..........39

26. Possible sinking of Single Event current through loading capacitance..........40

27. Formation of hole current. Step 1:.......... 42

28. Formation of hole current. Step 2:.......... 42

29. Formation of hole current. Step 3:.......... 43

30. Actual rate at which carriers leave hit volume, for different LETs..........45

31. Substrate engineering, first pass..........47

32. Substrate engineering, first pass- not a significant difference in any of the short-term collections, but significant differences in the long-term collection performance..........48

33.Long and short-term collections for different strike locations and angles..........49

34. Alignment of fields for the epi on p+ substrate..........49

35. 1-d doping gradients for a) no substrate engineering, b) epi on p+ 50

36. Concentration profiles at a plane at the center of the drain 25ns from the strike 51

37. Field magnitudes at a plane at the center of the drain 25ns from the strike 52

38. Transient comparison: epi on p+ with backside contact vs usual doping and topside contact 55

39. 4 structures studied for the effectiveness of the buried n-layer a) Some bias, some confinement, b) No bias, no confinement, c) Good bias, high confinement d) Reasonable bias, low confinement 57

40. Potential transients for 4 structures studied for the effectiveness of the buried n-layer……………………………………………………………………………58

41. Buried layer almost abstracts all the electrons from the deep substrate. Strike is 8 microns deep 59

42. Buried n-layer to mitigate well collapse and parasitic bipolar in PMOS 60

43. Pulse width and integrated conduction charge for different LETs- no substrate engineering and n+ buried layer 61

44. 3-d view of buried n-layer structure to mitigate well collapse and parasitic bipolar turn-on in PMOS. Potential and current transients are short compared to Low Power transients for an ordinary substrate 62

45. Buried n-layer defined locally underneath n-well of the PMOS. Mitigation of well collapse without degrading the NMOS performance..63

LIST OF TABLES

Table I: Dependence of plateau voltage on substrate doping and contact depth...............34

Table II: Diffusion Charge collection for different strike locations 54

Table III: Comparison of FWHM pulse widths for no substrate engineering and buried n-layer...62

CHAPTER I

INTRODUCTION

1.1 Overview

In this thesis, some of the basic mechanisms dictating single event pulse shapes and pulse widths in deep submicron CMOS as suggested by 3-D TCAD simulations are discussed. The utility of substrate engineering techniques in mitigating single-event sensitivity is demonstrated and a specific technique to mitigate some of the widest single-event pulses in deep submicron CMOS is proposed.

1.2. Overview of Previous Work

Single Events, caused by incident ions on a semiconductor device, are typically described by charge collection models based on drift and diffusion across the affected junction [1-5]. All these models involve drift across the drain body junction, and more or less assume a constant built-in potential for the junction during the entire duration of the single event voltage transient. Models developed by Hu [1], Messenger [2] or Oldham and McLean [3] belong to this category and hold good for older technologies, where the minimum dimensions are on the order of microns. Such a model provided sufficient accuracy for investigating the Single Event (SE) effects on CMOS devices and circuits using compact models and circuit-level simulators (such as SPICE) in micron scale technologies. However, for the current generation of deep-sub-micron processes (90, 130 and 180nm), the redistribution of electric fields resulting from an ion strike, spans several nodes and contacts. This causes a distinct change in the single event pulse shape from earlier observed technologies. The experimental observations of [6-8] introduce some estimations of the magnitude of typical FWHM (Full Width Half Max) pulse lengths in deep sub micron CMOS and its trends with technology scaling. The actual shape of the transient is difficult to ascertain because of its short duration, and more importantly due to the difficulty of irradiating an ultra small target device at an intended location. Even

the measurements by Ferlet-Cavrois et. al. on SOI and bulk CMOS devices [17] irradiated with pulsed laser or heavy ion microbeam were performed with 20 micron wide devices, which is very different from the devices used in a conventional digital design (close to minimum size), both in terms of area or restoring current drives, which are two extremely important parameters in the single event response of a circuit.

Characterization of SETs through Technology Computer Aided Design (TCAD) simulations indicates a distinct change in the transient waveform from the familiar double exponential shape. The first departure from the double exponential form was shown explicitly in TCAD simulations by Dodd et. al. [4, 14] on 180 nm bulk CMOS and SOI processes. This was also shown by Amusan et. al. for 130 nm CMOS and Turowski et. al. in [9] and [13] for 90nm CMOS. All these observations point to a change in the sequence (or important regions) of drift and diffusion events contributing to the overall charge collection, as we scale down from micron to deep sub-micron dimensions.

1.3 Overview of thesis

Mixed-mode simulations combining TCAD device simulation and compact model simulation can reveal the fine structure of a single-event current pulse with properly accounted device loading and complementary device restoring currents. This research deals with identification of the most important features in the complex shape of the Digital Single-Event Transients (DSETs) in deep sub-micron CMOS, and explaining the mechanism behind them. A mitigation technique for some of the longest DSETs through substrate engineering is also discussed.

This thesis organized into seven topics:

1) The characterization of device variants in a commercial deep sub micron process and electrical calibration of 3-D TCAD and compact models of different devices:

Electrical calibration of TCAD models giving close agreement with electrical characteristics of devices modeled in a commercial process design kit lends credibility to simulation results. A deep sub-micron process such as 90 nm CMOS has a large number of application specific device variants, mostly based on power dissipation and speed. Many of these variants are major candidates for radiation hard applications. For example, the Low Power variant is an interesting option because of its low power dissipation,

which is a desired characteristic for high-density space applications such as SRAMs. The characterization of Device Variants in a commercial deep sub-micron process and Electrical Calibration of 3D TCAD and Compact Models of different devices are summarized in this section.

2) Basic Single-Event simulations and relating the pulse widths to a salient feature (namely, a “plateau”) in the DSET:

The DSET shape in a modern deep-sub micron digital circuit is complicated, and each salient feature depends on a different circuit or substrate parameter, and the level of the charge injection. However, not all these are equally important in deciding the width of the pulse, which propagates through the circuit. A “plateau” in the current pulse is the feature that strongly decides the circuit FWHM pulse width, and it becomes necessary to characterize the plateau in terms of circuit parameters.

3) Identification of the mechanism behind the “plateau” (in point 2):

A close investigation of the carrier concentration and potential modulation in the substrate following the Single Event strike gives an idea of the mechanism behind the “plateau” shape.

4) Verification of the theory behind the plateau mechanism by investigation of different substrate profiles and contact doping schemes:

Based on the observations, it was hypothesized that in addition to circuit parameters the plateau features are a strong function of the substrate profile and well contact layout scheme. It is fairly easy to verify that hypothesis against a few variations in the substrate and well contact doping.

6) Truncation of pulse widths using substrate-engineering techniques:

The last section is fundamentally different from all the mechanisms and modeling tasks mentioned earlier. The aim is to achieve some mitigation of DSETs and error rates using substrate-engineering techniques. A few points have been discussed about some techniques (primarily involving the compatibility between a substrate profile and a well contact layout scheme in mitigating SETs) that have been effective in mitigating DSETs only in certain specific cases.

7) Mitigation of longest pulse widths through the implementation of a buried n+ layer:

The bulk of this work has been to propose the utilization of a novel buried layer scheme to reduce charge collection due to parasitic bipolar conduction. Parasitic bipolar conduction due to n-well collapse caused by an influx of minority carriers from the deposited charge in the substrate has been shown to be a prime contributor to Single Event vulnerability, and its mitigation would have a major effect on error rates and circuit/ system level hardening. The study is rounded off by proposing a substrate engineering technique that is effective in mitigating parasitic bipolar conduction, giving significant improvements in single-event pulse widths.

Thus, broadly speaking-

a) In the first part, one mechanism that plays a major role in deciding the pulse widths and pulse shapes in deep sub micron CMOS is discussed.

b) In the second part, some mitigation techniques for the longest DSETs are proposed, which work by eliminating the well collapse and parasitic bipolar turn-on.

CHAPTER II

CALIBRATION OF DEVICE MODELS

In this section, the first primary task of modeling is discussed, which is to develop calibrated 3-D TCAD electrical models for the devices in a commercial deep sub-micron technology. As we will find out later, the Single-Event behavior of a circuit turns out to be a fairly sensitive function of a number of device properties such as its drive strength, drain engineering and threshold voltage levels. Therefore, it is necessary to replicate the device properties with sufficient accuracy in order to lend credibility to the mechanisms described later in this thesis. The required input for the calibration task is the geometry and doping profiles of two commercial 90nm technologies, one for a high performance and the other one for a low power application. Most of the information used to model the device comes from two sources. For basic well doping profiles and isolation geometry, a third-party report on the digital base for a commercial analog and RF process in the 130 nm [12] was used. The actual doping profiles were determined using the commercial PDK and the corresponding documentation, through a trial-and-error method. Published literature on other 90 nm technologies such as the ITRS roadmap was also consulted. In this task, the earlier work done in calibration performed at the 130nm node by O. A. Amusan et al. [16] helped greatly to get a close initial guess. The TCAD simulations for the 3-D electrical models and single events were performed with version 10.0.6 of the Synopsis (formerly ISE) TCAD tool suite, primarily with Devise (to define the device geometry and dopings) and Dessis. For the mixed-mode TCAD simulations, Synopsis' ISExtract was used for extraction of SPICE models.

2.1 Variants in a commercial 90nm node

The 90 nm technology has a number of application-specific technology variants. While the 130 nm node had a normal low voltage device (1.2 V) and a high voltage (3.3 V) device for I/ O devices, the 90 nm node has many more variants of the low voltage

device- depending on an emphasis on power or speed. Two of these variants, which may be widely utilized in radiation hardened circuit design, are:

1) **High Performance:** This is the, conventional medium-power, medium-speed device.
2) **Low Power:** It is a low-power device. It is characterized by low drive strength and leakage current about an order of magnitude lower than High Performance. In circuits where the off-state power dissipation is on the order of the on-state dissipation, as in SRAMs, it is an attractive option. On the other hand, the reduced drive adversely affects the speed. As we will see later, it also gives an added Single-Event vulnerability.

The major point of structural difference between High Performance and Low Power is a much thicker gate oxide (about 2.8nm) for Low Power. Other factors are higher gate lengths (100 nm as opposed to 80 nm in High Performance), proportionally high channel lengths, lighter channel and LDD dopings. The minimum allowed gate dimension is also smaller in the Low Power technology. The gate capacitances of either variety are comparable. In addition to these broad variants, each of the High Performance and Low Power PDKs has regular and low threshold voltage variants (Regular Vt and Low Vt respectively). We were able to calibrate all these variants using minor variations in the channel implant profile.

2.2 IBM 90nm Device Cross Sections

The device geometry and doping profiles are described in this section. The well and substrate doping profiles are a key factor in the Single-Event response. Most of the dimensions and profiles for the well and substrate were retained from the ones used in 130 nm CMOS described in [12].

For the NMOS, the doping in the P-well is Gaussian with the peak around 0.65 μm down from the surface. There is also a P+ deep implant with the peak of the Gaussian at about 1.25 μm. This is primarily a low resistance path introduced for latchup protection. The shallow trench isolation is about 0.43 μm deep, and is present where source, drain, or well contact diffusions are not defined. The transition between the deep p+ implant and the well plays a role in charge collection, as will be seen later.

An accurate estimate of the gate oxide thickness is necessary to achieve proper calibration. Compact models used in the PDK indicated that this thickness would be physically 1.7 nm. However, since gate leakage due to tunneling was not modeled (as this introduced unreasonable computational requirements), the leakage equivalent thickness of 1.4 nm was used, and good agreement with the PDK device characteristics were obtained. The polysilicon gate was taken to be 140 nm thick, which was the same value, used for 130 nm devices.

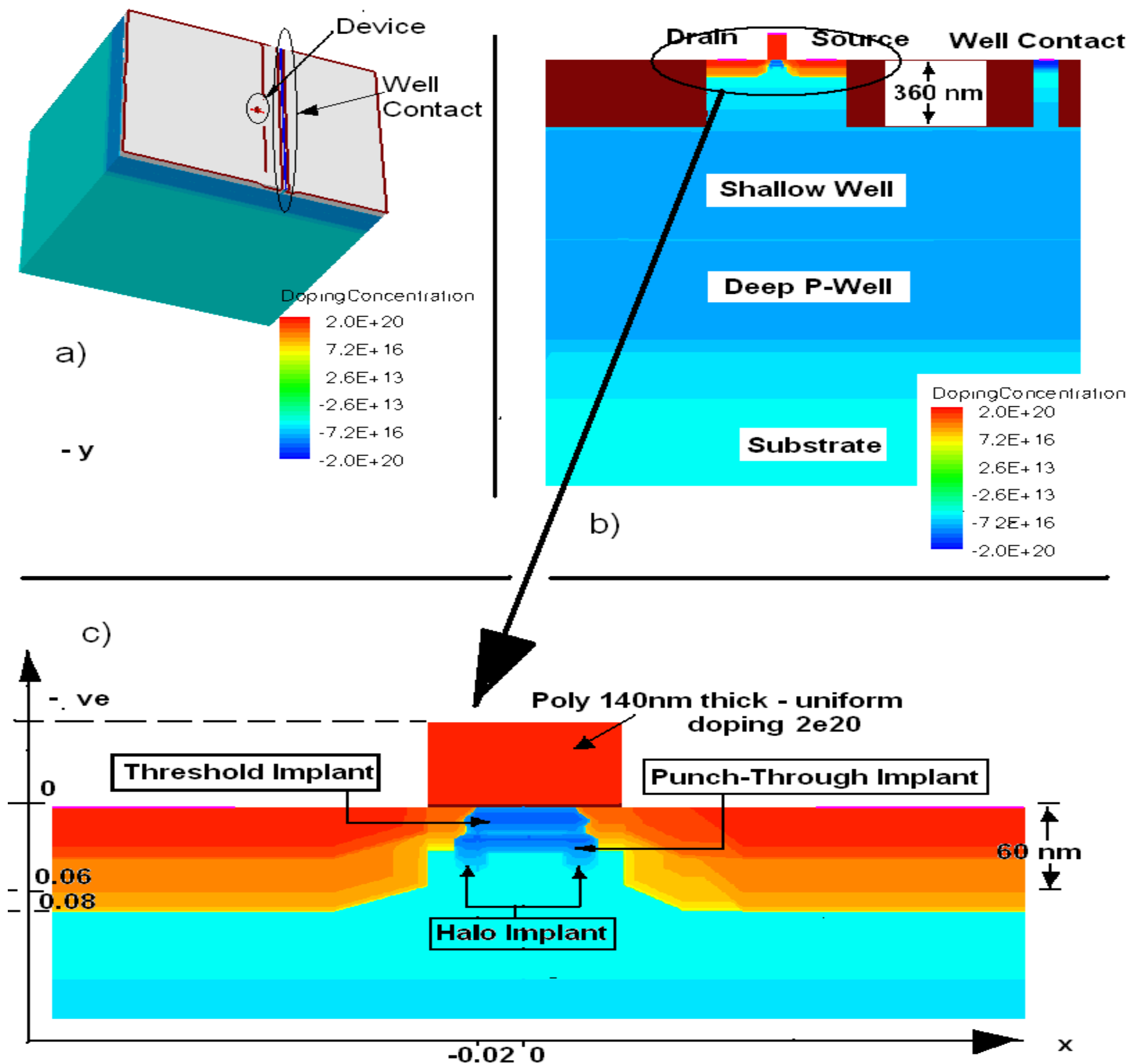


Fig 1. a) 3-d device (tiny red dot), b) a vertical cutline along center of drain showing well and substrate doping profiles, and c) a magnified view of the source, drain and channel implants (this is a High Performance Regular Vt NMOS).

Coming to the actual device, the doping profiles in the channel were ascertained largely through iterative methods during the dc calibration process. The channel implant structure consisted of a threshold implant right at the surface, which was the main "knob" for adjusting the device threshold voltage (Vt). Flanking the lightly-doped shallow drain (LDD) extensions on both the source and drain sides are two small regions of doping known as "halo doping". Electrically, the halo is a deterrent for short channel effects and DIBL (Drain Induced Barrier Lowering) without introducing unwontedly high capacitances. From a calibration perspective, it provides a knob for adjusting the sub-threshold slope without changing the threshold voltage too much. There is also a separate subsurface punch-through implant. For the lightly-doped drain extensions (LDD), dimensions and doping levels decide the series resistance of the device, which has a significant effect on the peak drive strength of the device. Once these factors were determined through a prolonged iterative comparison of the device characteristics with the ones in the PDK, the effective channel length came to be about 50 nm. Also, at the gate-STI crossover region, using a heavy sidewall implant becomes imperative in this technology- particularly for low gate widths. For a cursory idea of the doping profiles, Fig. 1 with the doping contours along a cutline at the center of the drain is used. A detailed numerical description and 1-d profiles are given later in appendix.

2.3 Results of Electrical Calibration

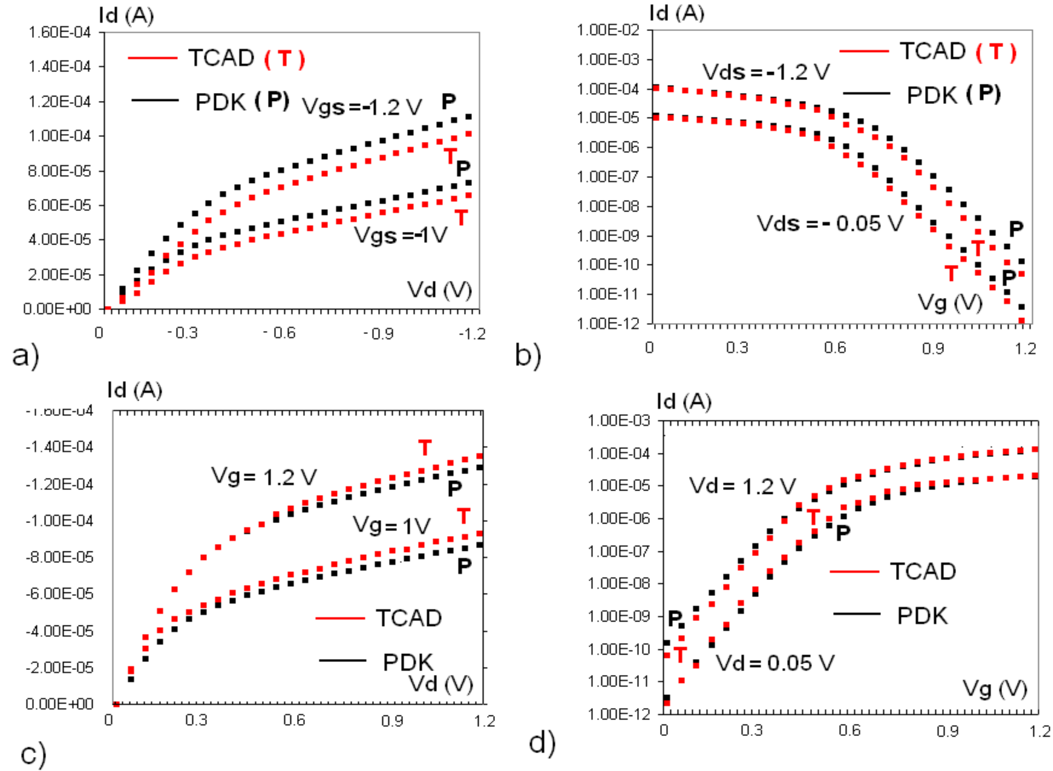


Fig. 2. Calibration curves for a 90nm Low Power PMOS (a and b) with Gate Length (L) = 100nm and Gate Width (W) = 480 nm, and a 90nm Low Power NMOS (c and d) with Gate Length (L) = 100nm and Gate Width W (W) = 200 nm. The red curves are for the TCAD and the black ones are for the PDK values.

Three-dimensional TCAD models were constructed for the different variants of NMOS and PMOS devices. The placement of well contacts can have a significant influence on the charge collected in single-event strikes and it is possible to model this only in 3-D simulations. The 3-D simulation is based on actual layout practice and design rule spacings, which are impossible to represent in the 2-D geometry. The 3-D models are also necessary to accurately predict the charge collected from a single-event strike, which is non-uniform in the third dimension. The 3-D structures were calibrated to the 90 nm

High Performance and Low Power process design kits (PDKs) by biasing the devices and sweeping the terminal voltages.

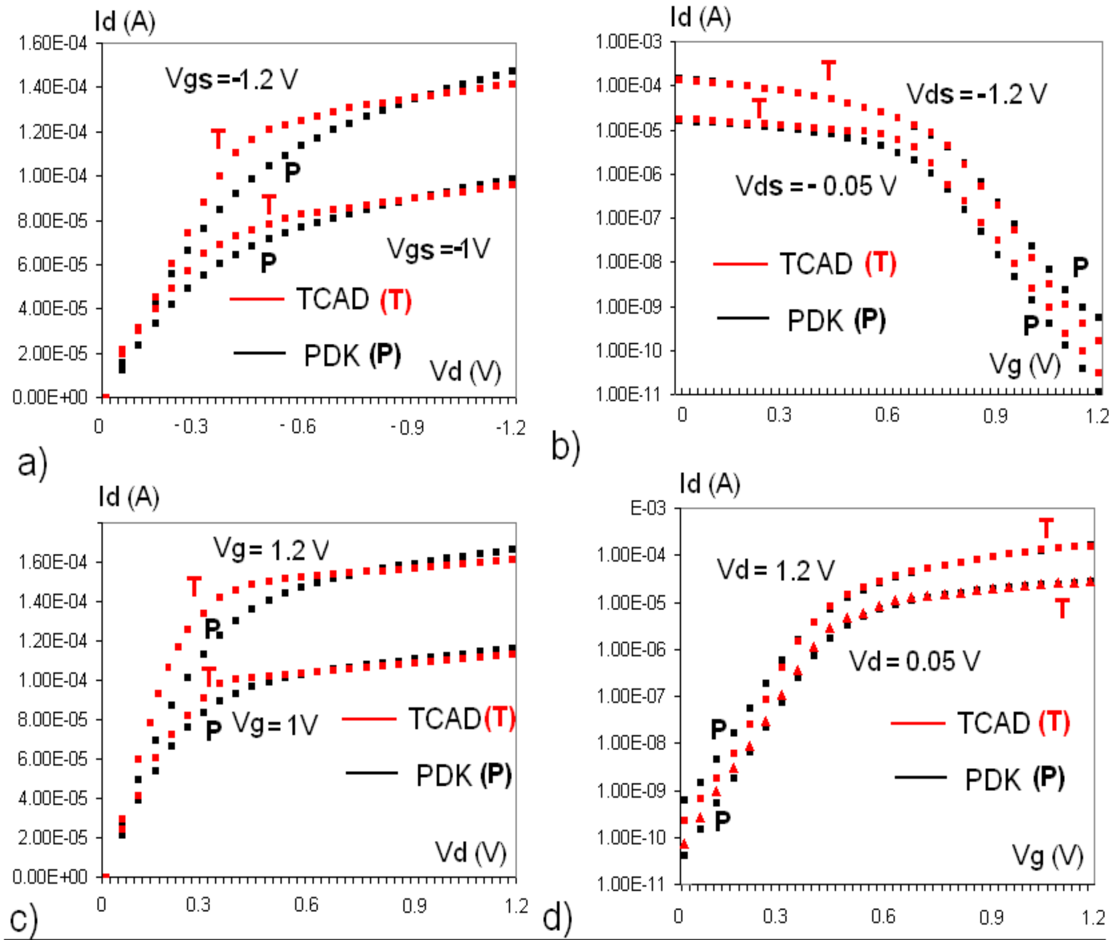


Fig. 3. Calibration curves for a 90nm High Performance PMOS (a and b) with Gate Length (L) = 80nm and Gate Width (W) = 480 nm, and a 90nm High Performance NMOS (c and d) with Gate Length (L) = 80nm and Gate Width W (W) = 200 nm. The red curves are for the TCAD and the black ones are for the PDK values.

The Low Power calibration is shown above for two devices for which experimental data might be available later. An important feature of the 90 nm node is that, leakage currents do not exactly scale in proportion to gate width. For a small change in the width, simple scaling holds good, but for a factor of, say 2, a full recalibration might be necessary. Matching characteristics of the High Performance variant is

considerably tougher than for the Low Power variant, especially in the transition or "kneeing" region. This is because, the small channel length and the low series resistance associated with it makes it difficult to compensate for mobility enhancing factors such as channel strain with doping.

2.4 Compact modeling

2.4a. DC modeling

Compact modeling for mixed-mode TCAD (where one or a few devices are simulated in TCAD and the rest as SPICE level compact models) has typically not been a problem. This is because in the earlier technology generations, the device currents have scaled almost linearly with dimensions. Also Dessis device solver in the Synopsis TCAD tool suite supports BSIM3 and only certain specific versions of BSIM4 models. The compact models in the IBM PDK are of a version (4.3.1) that is not currently supported by Dessis. For the previous versions of compact models, such as BSIM3 or BSIM4.1, it was usually sufficient to use the values of the SPICE compatible parameters provided by the PDK. However, with the later versions of BSIM4, a single model file approach usually does not work. Each device in BSIM4.3 has a number of "subcircuit wrappers", which are usually parasitic diodes and capacitances introduced during the fabrication process. These cause the parameter values of 4.3.1, when put into a version 4.1 solver to yeild characteristics that are extremely inaccurate. Thus, having used device libraries based on BSIM4.3.1, the earlier approach of using the PDK model parameters for compact model parameters in TCAD had to be abandoned. Synopsis' ISExtract, which is a compact model extractor program, was used. The inputs to ISExtract programs are a comprehensive set of device characteristic sweeps:

1)Id-Vd sweeps (4 different Vg between 0 and Vdd, with body bias at 0 and -Vdd)

2)Id-Vg sweeps (high and low Vd- with 5 different body biases between 0 and -Vdd.)

While these sweeps are normally experimentally measured curves, in our case the sweeps are performed on the compact models in the PDK to be emulated. Parameter fits to these characteristic curves for a given compact model version can be obtained by adjusting tolerance limits for drain current and drain voltage. The result of this exercise was

extremely accurate compact models for the given size. DC characteristics were matched with an average error of less than 2 %.

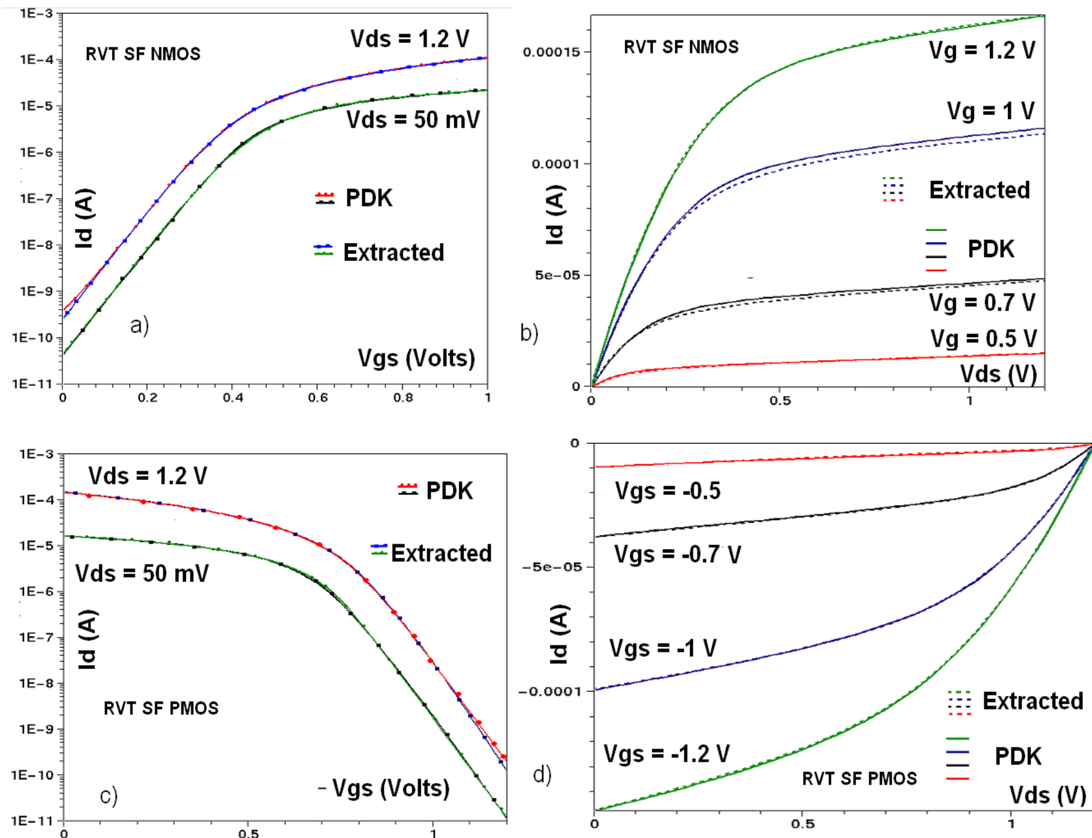


Fig. 4. Comparison between compact models of an Regular Vt High Performance NMOS transistor (80 x 200) (a and b) and an Regular Vt High Performance PMOS transistor (80 x 480) (c and d). The dotted lines are the extracted models. Visibility is difficult due to extreme close match.

2.4b. AC Calibration and Modeling

A detailed ac calibration of a compact model is very difficult and time consuming. However, since a correct estimate of the propagation delay is the most important issue from a Single Event standpoint, a comparison was made between a mixed-mode TCAD ring oscillator and the same ring oscillator simulated in Spectre.

The ring oscillator had 11 inverter stages. The 6th stage inverter had the NMOS in TCAD. Comparison between the mixed mode oscillator (with the extracted compact models and one NMOS in TCAD) and the Spectre equivalent is shown in Fig. 5:

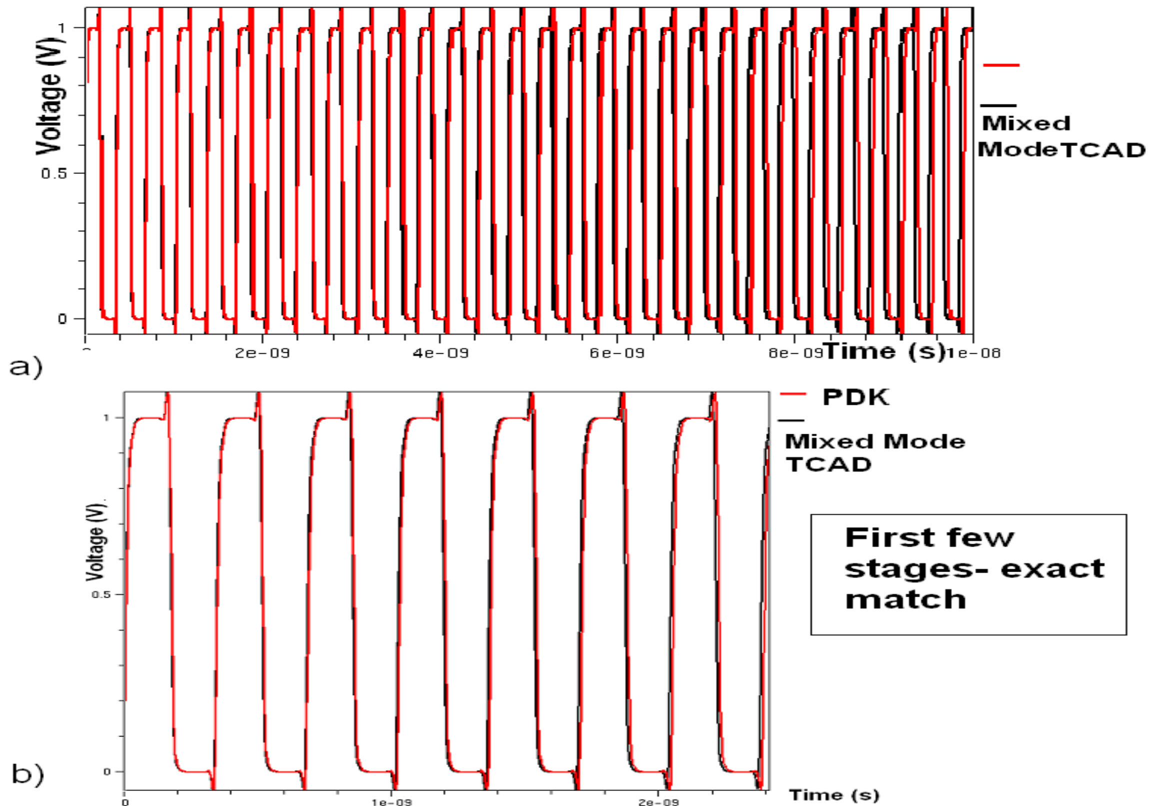


Fig. 5. Comparison between a TCAD and a mixed mode ring oscillator for a period of 10ns (a) and for the first 7 cycles (b).

As the comparison shows, the timings match almost exactly. More importantly, a close match in the overshoot region is a clear indication that the parasitic resistance and capacitances match the PDK values to a high degree of accuracy.

In conclusion, reliable models for our Single-Event simulations have been obtained, matching the dc characteristics and individual gate delays to a high degree of resemblance. The TCAD models have matched drive currents within 5 % accuracy and sub-threshold currents matched within a factor of 2. This ensures that our modeling of the

channel and active areas of the device is accurate within reasonable limits. Another important aspect of this modeling exercise has been the extraction of accurate compact models. As we will show later on, pull-up drive current strength is probably the single most important parameter influencing DSET widths. Another study of interest is the modification of a DSET as it passes through a large number of gate delays. High accuracy in DC and AC properties of compact models ensures accuracy in observations about DSET widths, which are discussed in the next chapter.

CHAPTER III

BASIC SINGLE EVENT SIMULATIONS AND PULSE WIDTHS

Having satisfied the primary requirement of having reliable TCAD and compact models for the devices, a set of mixed-mode single-event simulations were performed. These were mostly done to address the following issues:

1) Accurate single-event pulse shapes and magnitude of pulse widths for combinational logic circuits at the 90 nm node.

2) Effect of having different variants within the same technology generation. Relative Single Event vulnerabilities of the variants.

3) Impact of layout techniques and contact placement on pulse shapes and pulse widths.

To answer the first 2 questions, a set of Single Event simulations on a 5-inverter chain circuit was performed with the middle inverter having a device (PMOS or NMOS) in TCAD.

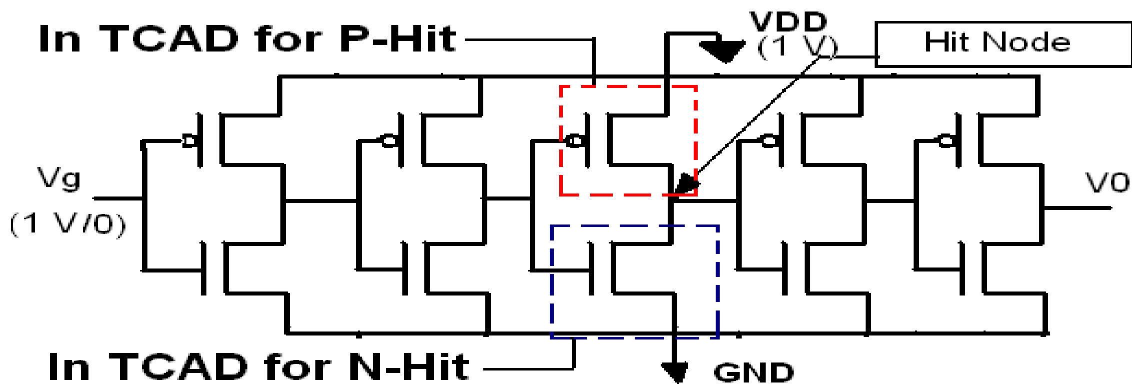


Fig. 6. The schematic for the circuit used in mixed-mode modeling. The NMOS is 200 x 80 and the PMOS is 480 x 80.

In most of these simulations, the strikes were in the center of the drain. The strike radius (characteristic length of the spatial charge deposition profile) has been a debatable issue, and the value used in this study is 30 nm. Varying this value to 50 nm did not significantly affect the observations. The time profile of the charge deposition is an error function with a characteristic time of about 2 ps.

3.1. Collection Depths in 90nm CMOS- Implication on Substrate Block Sizing

TCAD simulations almost always suggest that for an ion strike several microns deep, not all the deposited charge is collected. Beyond a certain depth, the charge collection saturates. This stems from the fact that the fields in the vicinity of the drain become ineffective in collecting charge that is generated beyond a certain distance from the source and the drain and that some charge recombines or exits through other contacts. For determining the collection depth, the strike depth was varied in small steps and the incremental changes in collected charge on the drain were observed. The depth at which the collected charge saturates is taken to be the collection depth (Refer Fig. 7).

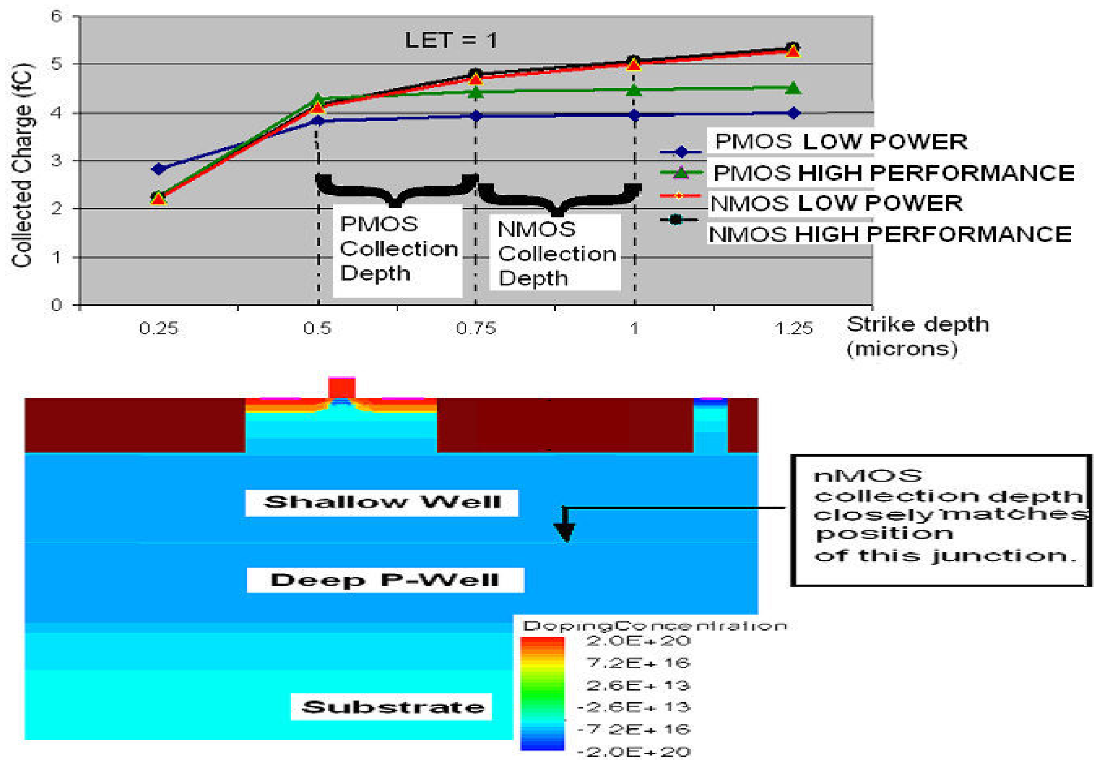


Fig. 7. Collection depth estimation for 4 devices. Mostly, collection depths correspond to well-substrate junction depth.

The simulations for ascertaining collection depth shown here were performed at a relatively low LET (1 MeV/mg/cm^2) to eliminate any extra charge collection due to parasitic conduction. Later, simulations performed at higher LETs yielded almost the same results. There is no variation in collection depth between technology variants, because the well and substrate doping profiles are presumably the same for both. For the PMOS, the collection depth is sharply defined, as collected charge rapidly saturates between 0.5 to 0.75 micron. This corresponds nicely to the junction between the substrate latchup profile and the n-well implant. For NMOS, this change is much more gradual, because there is no real junction between the latchup profile and p-well. Nevertheless, the high-low junction plays a significant role in determining collection depth (Fig. 14).

The collection depth has an important implication for the simulation setup. Ideally,

the simulation should be performed in a chunk of silicon- each of whose dimensions are equal to a diffusion length for the substrate doping levels, but that is not practical given the large diffusion lengths and tight meshing requirements. The two effects associated with truncating the silicon block are:

i) Reflection from the lateral boundaries, and

ii) Vertical truncation of the charge deposition track (specially for high energy ions).

For case i), the optimal sizing of the silicon chunk has been estimated at about 10 micron x 10 micron. This size gives a significant amount of reflection from the edges, but it makes a difference only for collection at fairly high time durations after the strike, and does not make any significant difference to the Full-Width-Half-Max (FWHM) pulse width. The collection depth estimation ensures that going with a substrate depth that is somewhat shorter than strike depths of some of the higher energy ions, does not imply that the collection depth is being truncated, so that we can expect a reliable response. In practice, ending the strike about 1-2 microns above the bottom of the substrate works well.

Another factor in the simulation setup that is open to a lot of speculation is the meshing, which decides the spatial points at which discretized forms of Poisson's and continuity equations are formed. A number of different meshing schemes were used- and the collection volume (roughly a block 1 micron on a side) around the struck device and well contact doping were identified as the areas that needed to be tightly meshed. In a single-event simulation where one of the devices are not a part of the pull-up circuitry, we have repeatedly observed the simulation results to be independent over large limits on the meshing of the source, drain or the channel. With only 5 mesh points along the length of the channel and 6 points along the lateral extent of the source and drain, it is possible to get results which vary only negligibly from a simulation with a very tightly meshed channel and active region. This mostly has to do with the destruction of carrier gradients due to the high charge injection from a single event strike. However, devices were never meshed so loosely so as to keep the models suitable for simulations with multiple devices in the same body, where the electrical performance of a device away from the strike might affect the single-event response of the circuit. Details of this are included in the

Appendix.

3.2 Hit Current Pulse Shapes for different Technology Variants at 90 nm

The single event hit current pulse profile for low energy ions (LET of less than 5 MeV/mg/cm^2) is characterized by the classical double exponential shape, mostly. For higher LETs, the pulse shows a sharp peak of about 10-15 ps followed by a region of nearly flat response. The duration of this "plateau" can be taken as the pulse width for all practical purposes, because the recovery of the pulse is usually pretty fast for matched transistors designs. For this reason, identification of the mechanism of the plateau and formulation of a simple electrostatics based model may be useful in attempts to quantify pulse widths in a predictive way.

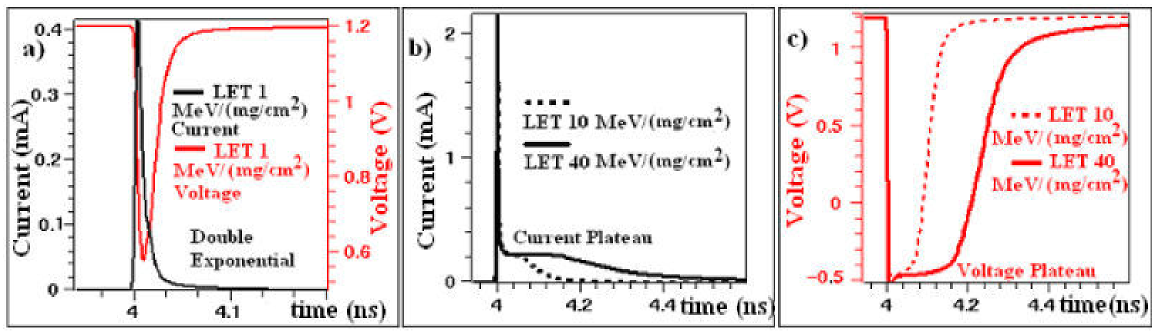


Fig. 8. Distinctly different hit current pulse shapes for a) an LET of 1 MeV/mg/cm^2 (double exponential) and b), c) one of 10 MeV/mg/cm^2 or above (exponential plus plateau).

The first observation that was fairly useful (Fig. 16 in Chapter 5) was that, the capacitance of the next stage inverter was of minimal consequence in determining the pulse width (for capacitances corresponding to reasonable sizing for digital logic). The drive strength of the pull up transistor was the only circuit parameter playing a major role in the pulse width. Let us take a look at the general pulse shapes, pulse widths and collected charges for a number of different LET strikes.

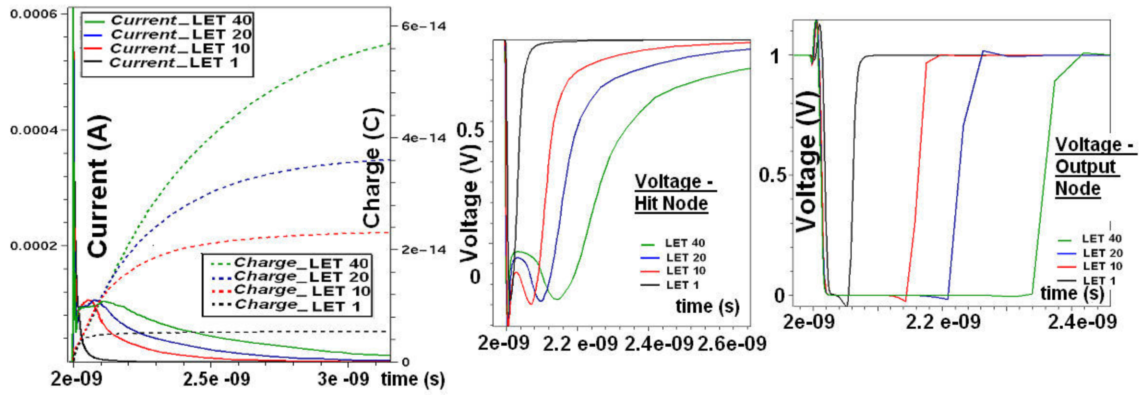


Fig. 9. Hit current pulse profiles for High Performance NMOS, collected charge, potential pulse profiles at hit node and at circuit terminal.

The major point of importance in this is that, the slowly varying (or almost flat region in the initial portion of the strike is the deciding factor for the FWHM pulse width (refer Fig. 8). The long recovery tail is of fairly low importance to the voltage pulse shape.

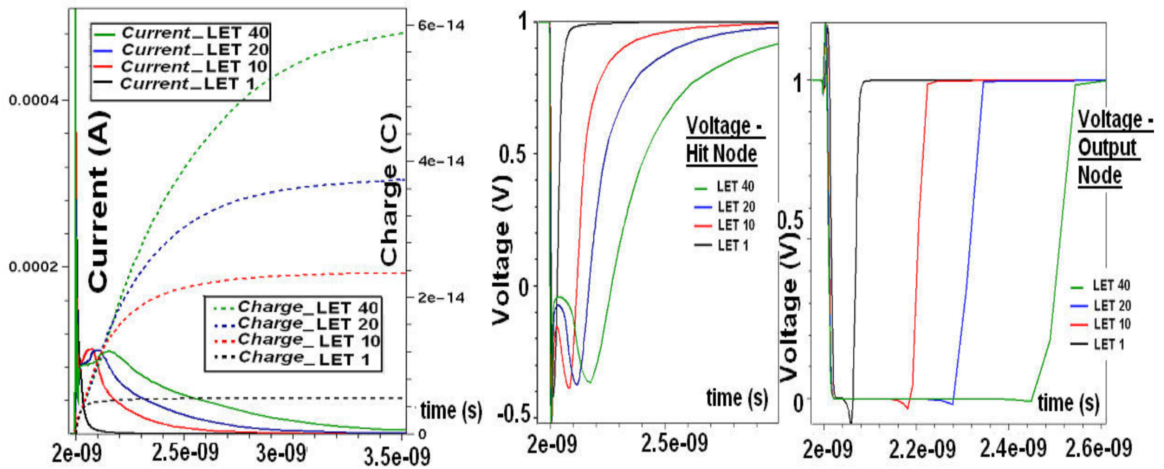


Fig. 10. Hit current pulse profiles for Low Power NMOS, collected charge, potential pulse profiles at hit node and at circuit terminal.

Low Power characteristics are not very different from High Performance. Only the current pulse "plateaus" at somewhat lower levels and the voltage pulse widths are marginally on the higher side. This comparison will be shown more explicitly in subsequent discussions.

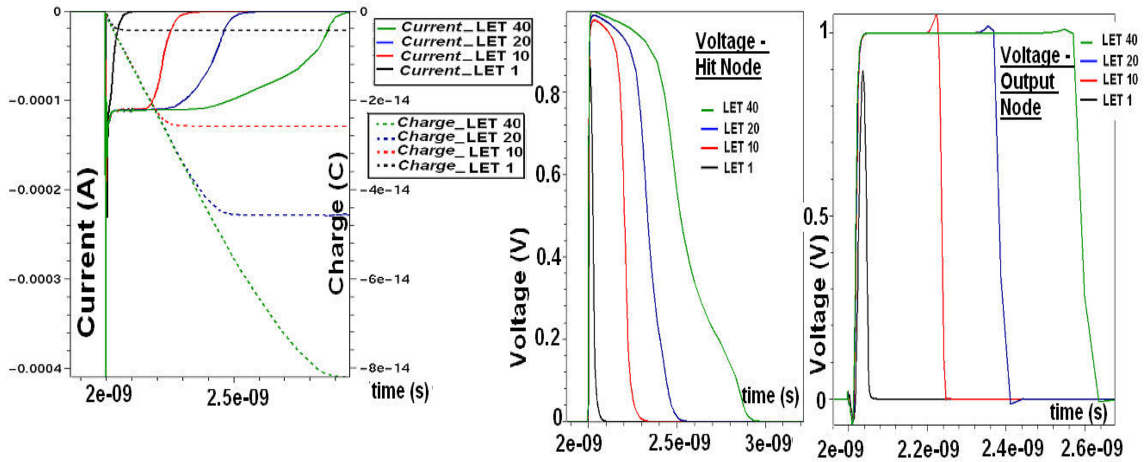


Fig. 11. Hit current pulse profiles for High Performance PMOS, collected charge, potential pulse profiles at hit node and at circuit terminal.

The situation is considerably more interesting for PMOS pulse widths. As we have seen in earlier deep sub micron processes, parasitic bipolar amplification has traditionally been a dominant factor in the PMOS Single-Event response. It results in considerably wider pulses, and a much larger sensitive cross-section associated with the n-well. Also, the flat "plateau response" is much more pronounced in this case.

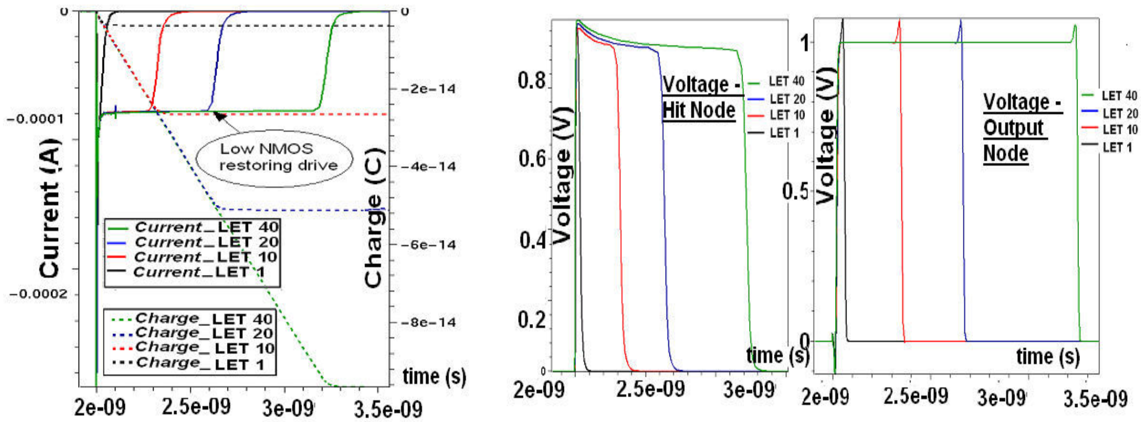


Fig. 12. Hit current pulse profiles for Low Power PMOS, collected charge, potential pulse profiles at hit node and at circuit terminal.

One thing that is noticeable here is that, the relation of pulse width with LET is monotonic, almost linear in certain areas. This may not necessarily be true in a real circuit, where charge confinement and charge sharing effects due to device layout might lead to pulse width truncation or elongation after a certain amount of initial deposited charge. This estimation is mainly useful for an analysis of the basic charge collection mechanism. There can be several secondary inter related mechanisms that might complicate the response. Parasitic bipolar amplification is probably the most important of all these and will be discussed in the next section. To summarize the effect of technology variants on pulse widths, a final chart is presented listing FWHM (Full Width Half Max) pulse widths in Fig. 13:

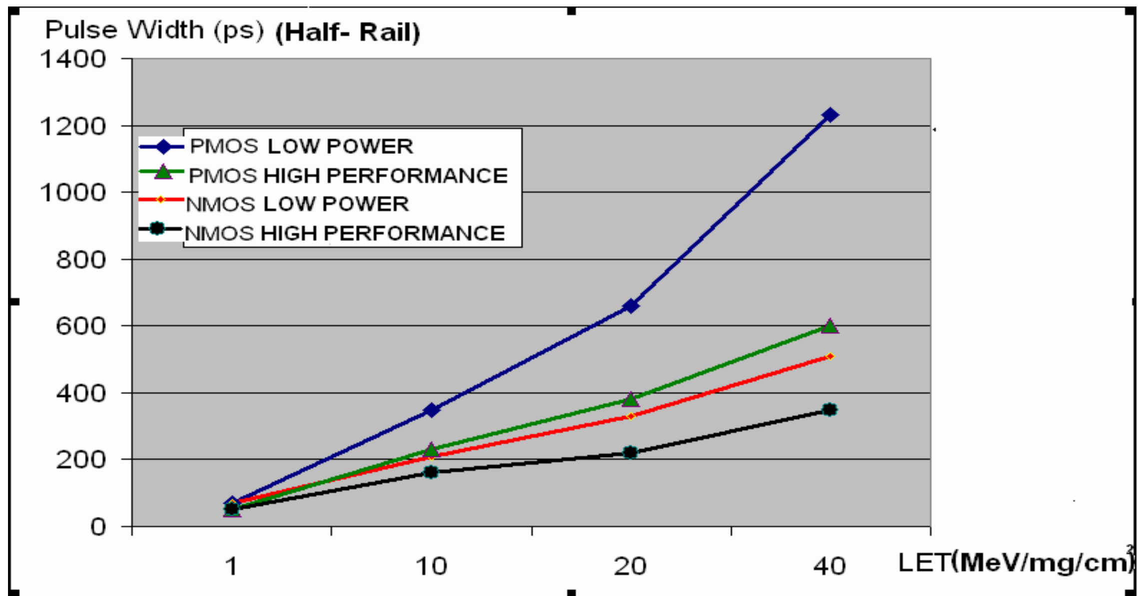


Fig. 13. Summary SEE pulse widths for Low Power and High Performance variants. Low Power shows considerably more SEE vulnerability.

Having observed the basic Single-Event characteristics of a variety of devices under irradiation at different energies, the basic mechanism for Single Events in a deep sub micron technology is examined next. But first, some more details of interest to RHBD circuit designers are summarized.

CHAPTER IV

CONTACT LAYOUT AND PARASITIC BIPOLAR AMPLIFICATION

Enhanced charge collection due to parasitic bipolar turn-on has been an observed problem in earlier deep sub micron technologies, and is expected to get worse with device scaling. The parasitic device structures are shown in Fig. 14. In the aftermath of the strike, the high carrier concentrations causes collapse in well potentials, causing the parasitic device to turn on. The concentration of minority carriers (for the hit device) is not very high for the p-well (NMOS). However, the strong junction (a high built-in potential of about 0.7 V) at the well-substrate boundary causes a high enough electron concentration to give pronounced bipolar activity in PMOS. As is evident from the figure, the base resistance is a strong factor controlling the well potential in the PMOS. This well resistance is guided by:

1) N-Well Contact area

2) Distance of N-Well Contact from device drain.

Nominally, to eliminate parasitic effects, all simulations performed so far were with the well-contact structure as shown in figure (a minimum width stripe running all along the device blocks). We studied the parasitic bipolar effect in 90 nm CMOS by varying the 2 factors controlling the base resistance, and hence the well potential.

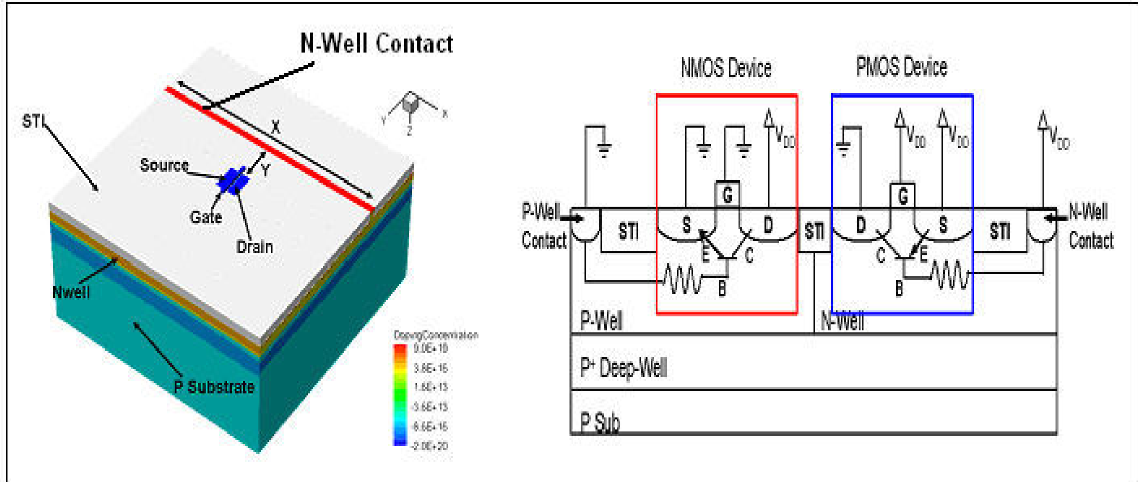


Fig. 14. CMOS cross section, showing parasitic elements. The PMOS device has a lateral parasitic pnp bipolar transistor, effect is more due to confinement of carriers by n-well. Structure of well contact is shown.

4.1 N-Well Contact Area

To study the effects of the n-well contact area (i.e. contact resistance) on the generated pulse width, simulations were conducted for contact sizes ranging from 200 nm x 200 nm to 200 nm x 10 µm. The well contact was located 500 nm away from the PMOS device and was kept at that constant distance from the device for all simulations. The simulations results shown in Fig. 15(b) illustrate the dependence of the pulse width on the n-well contact area. The reduction in the pulse width is due to the increased contact area creating a larger collection area for the electrons generated from the ion strike, resulting in the reduced pulse width.

4.2 N-Well Contact Location

To study the effects of the distance between n-well contact and the PMOS device, the distance was varied from 500 nm to 4 µm (Fig. 15). The n-well contact size was fixed at 200 nm x 10 µm for all simulations. The simulation results in Fig. 15(a) show the effect of the contact location on the generated pulse width. The reduction in the generated pulse width with increased contact proximity is due to the reduced n-well resistance. The reduced potential drop associated with a proximally located and small well contact resistance helps reduce the bias at the base of the parasitic bipolar device resulting in

lesser parasitic charge generation. A combination of n-well area and contact location can be used to mitigate the longer pulse widths generated in the PMOS devices.

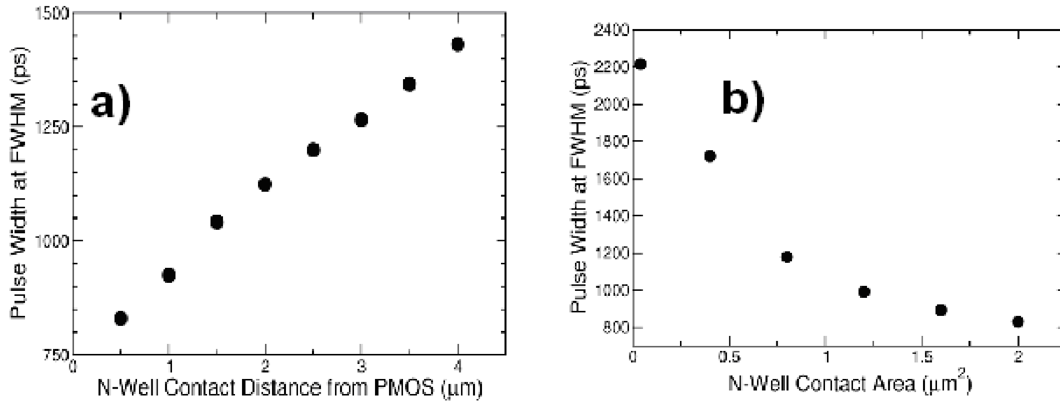


Fig. 15. FWHM voltage pulse widths for a) varying n-well contact location from 500 nm to 4 um and b) varying n-well contact area from 200 nm x 200 nm to 200 nm x 10 um. For all these studies the PMOS was part of a five inverter chain, size of contact was 1micron x 80nm.

Please note the magnitude of the pulse widths presented in the two graphs. Even with reasonably close spacing, or fairly generous contact sizing, these pulse widths definitely exceed the longer pulse widths for N-Hits by quite some margin. Theoretically, we can make the well-contact sizes as large or the placements as close to the device as the design rules allow, but that is an undesired way of mitigating Single-Event vulnerability, because of the large area penalty involved, which somewhat defeats the purpose of scaling in the first place. At the same time, the well collapse adds to the sensitive cross section associated with a device in case of the P-Hits. Consequently, based on our simulations, in conventional digital circuits such as combinational logic or digital memory, the PMOS can be expected to be the main contributor to the error rate. The long pulses from single events indicate that requirement for system-level mitigation techniques such as EDAC might be more demanding due to the exacerbation of the parasitic bipolar with every single generation of technology scaling, unless a physical or circuit level mitigation technique is introduced which addresses the issue of the well collapse and parasitic device turn-on.

CHAPTER V

POTENTIAL MODULATION IN THE SUBSTRATE AND PULSE WIDTHS

The single-event descriptors in different situations and devices have been discussed. Fig. 8 reveals an important observation pertaining to the pulse width. The diffusion tail of the SET pulses is long, and extends over more than a nanosecond, but its role in determining the FWHM pulse width is negligible. This pulse width matches very closely, the width of the flat or "plateau" portion of the pulse. It suggests that there might be a way to avoid modeling the entire complex shape of the SET, and develop a considerably simple circuit-level representation of the current pulse, without losing accuracy in the circuit response. The focus of this section will be to justify the shape of the "plateau" portion of the hit current, and characterize it as a function of loading conditions, substrate profiles and contact layout. To do that, the pulse shape needs to be justified and the physical mechanisms responsible for the shape need to be validated.

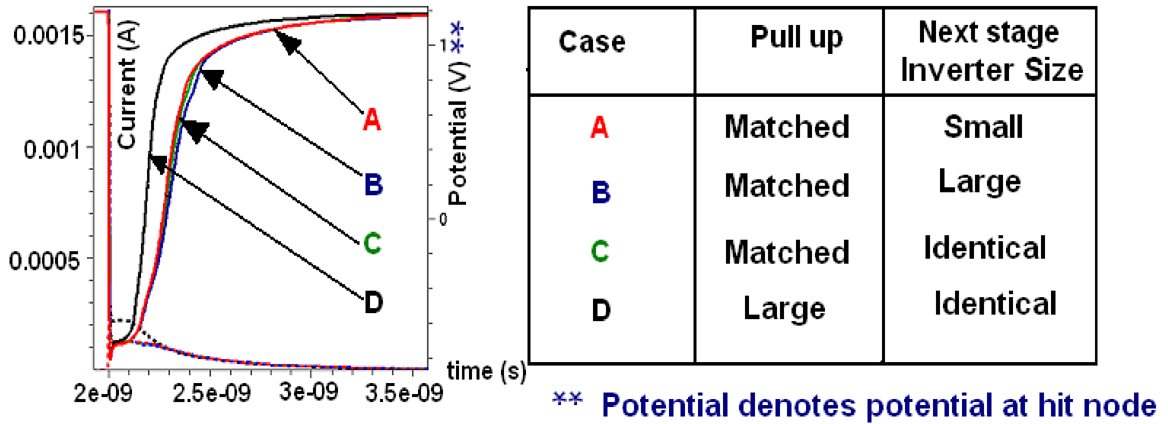
Before going into deducing the mechanism behind the plateau, some factors affecting the "plateau" current have to be discussed.

1) The plateau current corresponds to the drive of the restoring (pull-up or pull-down) device, at the drain bias level of the struck device during the plateau interval.

2) The plateau level does not depend on the device current of the next stage loading capacitance. Given that the rate of voltage change is small in the plateau region, this is expected, because capacitive current is given by C x dV/dt. With C getting smaller at every new technology and bias voltages shrinking, the smallness of C x dV/dt causes the loading capacitance to play a diminishing role in the Single-Event response.

We demonstrate this claim through a simple set of simulations: Using the same inverter string in TCAD mixed-mode simulations, four different simulations were performed. In two of the simulations, the inverter undergoing the radiation event remains the same, but the downstream inverter loading the irradiated inverter is simulated in one run with a small inverter and in the other run with a large inverter, increasing the

capacitive load on the struck node. In the next two simulations, the size of the restoring PMOS in the struck inverter is small in one run and large in the other, testing the effect of the restoring drive current on the current pulse. As seen here, the only place where the capacitive load makes a difference is in the recovery after the plateau, but that is not a major contributor to the pulse width.



Case	Pull up	Next stage Inverter Size
A	Matched	Small
B	Matched	Large
C	Matched	Identical
D	Large	Identical

Fig. 16. The effect of node capacitance and restoring PMOS drive current on pulse width of struck node from a two-inverter simulation with struck NMOS in TCAD. Configuration A- Hit Node: NMOS- 240 x 120, PMOS 600 x 120. Loading inverter stage: 240 x 120, PMOS 240 x 120. Configuration B- Hit Node: NMOS- 240 x 120, PMOS 600 x 120. Loading inverter stage: 400 x 120, PMOS 1000 x 120. Configuration C- Hit Node: NMOS- 240 x 120, PMOS 600 x 120. Loading inverter stage: 240 x 120, PMOS 600 x 120. Configuration D- Hit Node: NMOS- 240 x 120, PMOS 1000 x 120. Loading inverter stage: 240 x 120, PMOS 600 x 120.

In another simulation, hits for the same LET are compared for a high restoring drive (High Performance) and a low restoring drive (Low Power) in pull down.

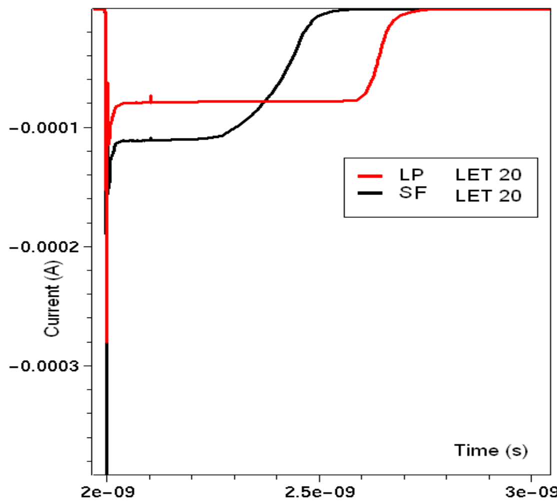


Fig. 17. Current SETs for High Performance and Low Power variants for an LET OF 20 MeV/mg/cm^2. Note that LP “plateaus” lower, due to low pull-up drive.

These simulation results strongly suggest that if the plateau of the pulse is modeled with sufficient accuracy, the circuit response will be accurate too. This is a useful simplification considering that the generally complicated shape of the pulse can be done away with. But before doing that, the plateau in the potential and current profiles need to be justified from a circuit / device standpoint.

5.1. Formation of the plateau

Let us look at the internal state of the device before and after the strike. In the pre-strike scenario, a large potential across the drain body junction is observed. The well contact high-low junction is a weak one and supports only a few hundred millivolts in the equilibrium state.

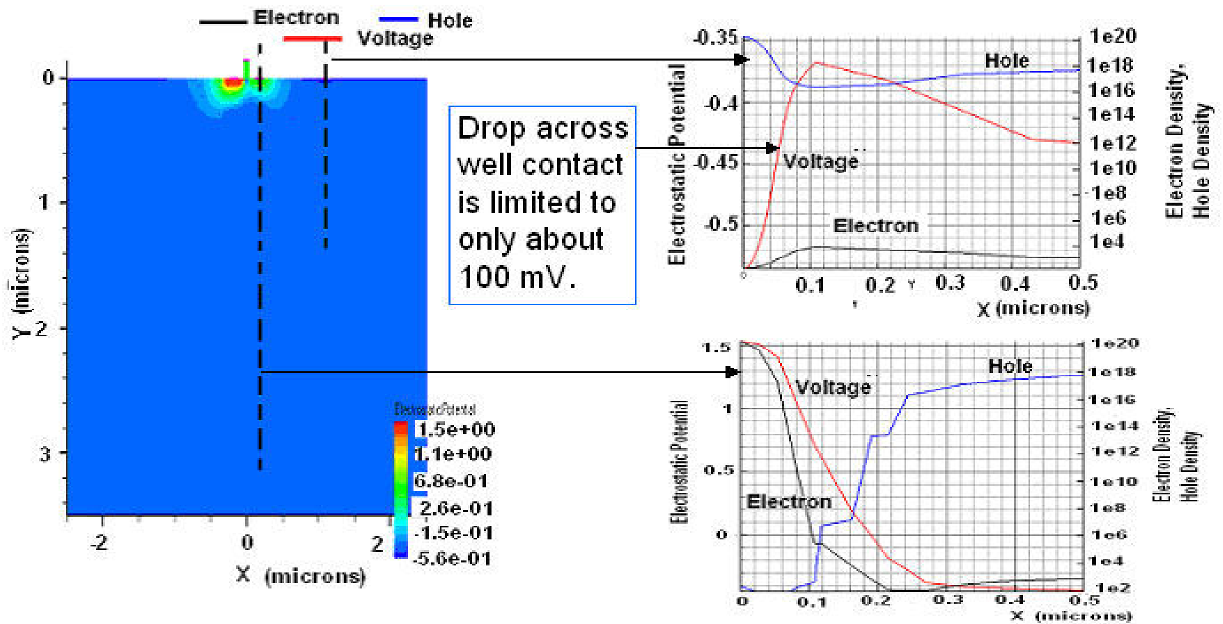


Fig. 18. A 2-d slice at the center of device drain (NMOS). First cutline is at the drain, second one is at the well contact. For potential reference level, see caption of Fig. 22.

The situation changes drastically within 10 ps of the strike. There is a major change in the potential distribution in the well. The huge number of carriers generated from the SE strike lead to the charge in the drain body depletion layer being neutralized (Refer Fig.

19). As a result of this, the potential across the drain body junction is lost, and the junction gets “pushed out”. How far the junction gets pushed out depends on the well contact placement and distance. The reason for this is: Since the well contact is very highly doped, when the potential pushout happens, the well contact doping is too high to “neutralize”. As a result, the collapse of the well potential gets “arrested” and the junction potential drop increases across the high-low contact junction, creating a high field in the well-contact region.

For the potential to vary rapidly at the drain terminal, there has to be a region in the well across which the potential can be dropped. With the drain body junction not there, the only option is the “high-low” contact junction, and only a small potential can be dropped across it. For this reason, the potential in the well near the device becomes uniform within a few picoseconds. The drain is the only node in the circuit whose potential is not pinned. With saturation of potential modulation in the substrate, the drain potential also becomes fairly constant, which implies that the SET current “plateaus” out.

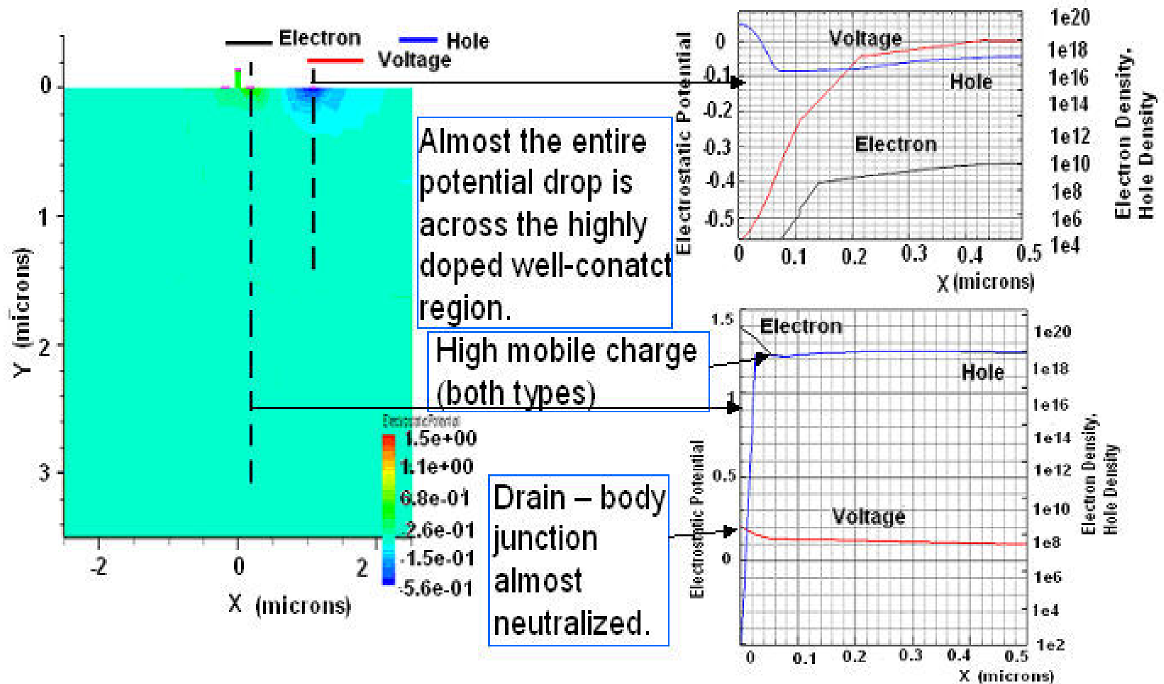


Fig. 19 A 2-d slice at the center of device drain (NMOS), 10ps into the strike. First cutline is at the drain, second one is at the well contact. Potential redistribution and increased gradient near well contact is shown. For potential reference level, see caption of Fig. 22.

In the case of deep-submicron CMOS, since the 1-D cut in Fig. 19 (potential curve) shows the potential to be nearly constant underneath the drain for a high LET case, the potential in a region of the well close to the source-substrate junction translates to the potential at the drain terminal. In the NMOS device the path for the shift of potential is from the N+ source, through the P- well, to the P+ well contact. The drop of potential at the well contact affects the potential of the source-substrate junction. If a potential of V_d is present across the equilibrium source- substrate junction, then an increase in the P+ contact potential of magnitude V_w reduces the built-in potential of the source- substrate junction to V_d - V_w, because both the well contact and the source are pinned to ground, so the total potential drop in this path must be zero. Therefore, the drain terminal of the irradiated transistor, which now has very little drop of its own, is pulled down to V_d - V_w below the ground, as shown in Fig. 20(c). Consequently, if the NMOSFET drain voltage is pinned during the plateau, and the gate voltage of the restoring PMOSFET is fixed at ground during the event, then the gate-to-source and drain-to-source voltages of the PMOSFET are constant. Thus, the PMOSFET current is constant throughout this interval, resulting in the observed plateau in the current waveform.

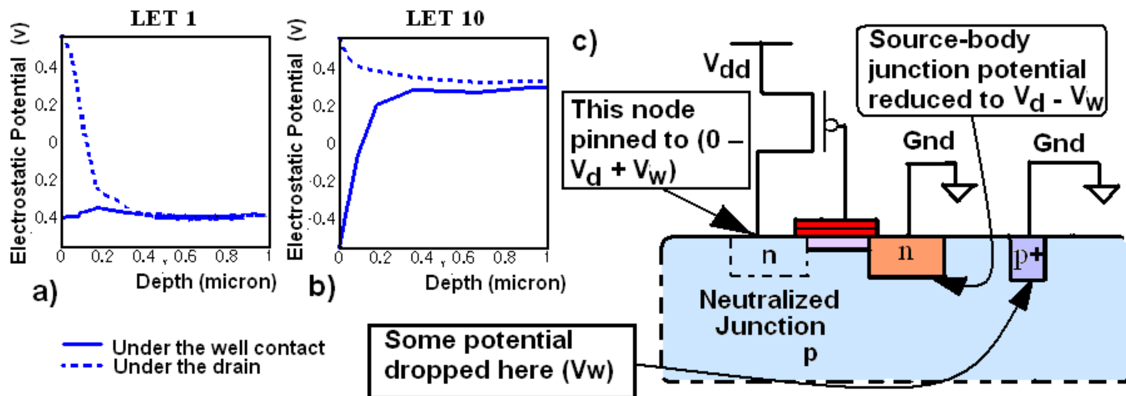


Fig. 20. Diagram of the mechanism of potential collapse and 1D plots of potentials under the drain and well contact for LET=1 and 10 MeV/(mg/cm^2) (25 ps after strike). Cartoon (circuit explanation) potentials referenced to Fermi level in metal ($V(x) = E_{fm}/q - \phi_s(x)$)). In 1-d plots, potentials referenced to E_i. ($V(x) = \phi_s(x) - E_i/q$) As we go from LET 1 (a) to 10 (b), region of high potential drop can be seen to shift from drain to well contact. Drop at the well contact affects the drain terminal voltage (c).

The mechanism of the potential modulation and saturation of the potential push out against a very heavily doped well contact is similar to the field-funneling model developed by Hu and Hsieh [1]. Validity of Hu's model requires a lightly doped substrate on the side of the funnel extension into the substrate. The situation described here can be visualized as a funnel reaching a hard boundary due to the highly doped contact, and all the strong fields accumulating at the funnel boundary.

5.2. Contact and substrate doping and potential pushout

To test the hypothesis regarding the relation of the "plateau" potential to the potential drop at the well contact (as demonstrated in Fig. 20c), we consider the results from a set of simulations in which we vary the background substrate doping, which is the uniform doping of the die before the well dopings are implemented. This primarily changes the doping immediately underneath the source, drain or well contact diffusions. This is

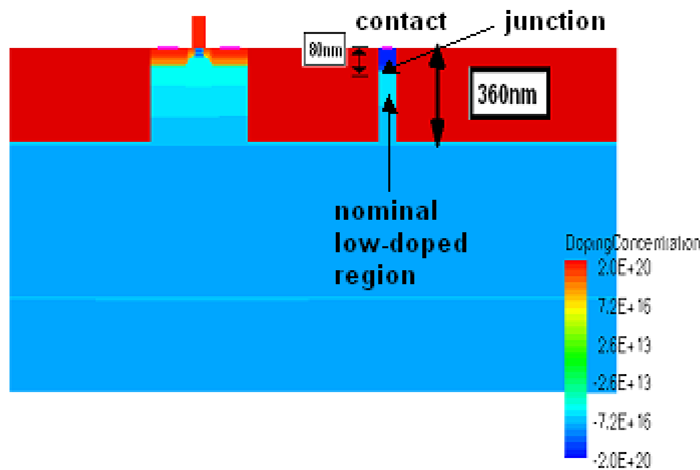


Fig. 21. Nominally the depth of the well contact junction is about 80nm. This depth is changed to 450, 350 and 280 nm. Setup for simulation with variation in well contact doping.

because the well doping is a fairly steep Gaussian profile that falls off to be lightly doped right below the diffusions (Fig. 5), and the doping level in those regions only is given primarily by the background substrate doping. We also consider the case in which the background doping remains constant but the depth of the heavily doped well contact varies. The results reinforce our earlier hypothesis described at the end of Section 5.1, illustrated in (Fig. 20c). As shown in Fig. 22a, for a highly doped substrate (background doping of 5×10^{17} cm^{-3}), resulting in a weak high-low junction at the well contact, there

is hardly any drop at the well contact (well-contact cut line of Fig. 22), and the source-well junction has a potential as high as 0.8 V (source cut line of Fig. 22).

Consequently, the "plateau" potential drops 0.75 V below the ground (shown in Table I). On the other hand, for a lightly doped substrate (nominal background doping of 10^{16} cm^{-3}), a stronger high-low junction at the well-contact supports a much higher potential gradient from the push out (well contact cut line in Fig. 22b), resulting in a smaller potential drop across the source-well junction, and a much smaller excursion of about 0.4 V below the rail (Table I). Very similar trends are seen due to an increase in the depth of the heavily doped well contact (Table I).

Table I: Dependence of plateau voltage on substrate doping levels and contact doping depth.

Substrate Doping Concentration (cm^{-3})	Plateau Voltage (V)	Well Contact Doping Depth (nm)	Plateau Voltage (V)
10^{14}	-0.03 V	80 nm	-0.41 V
10^{15}	-0.18 V	250 nm	-0.53 V
10^{16}	-0.41 V	350 nm	-0.61 V
5×10^{17}	-0.75 V	450 nm	-0.71 V

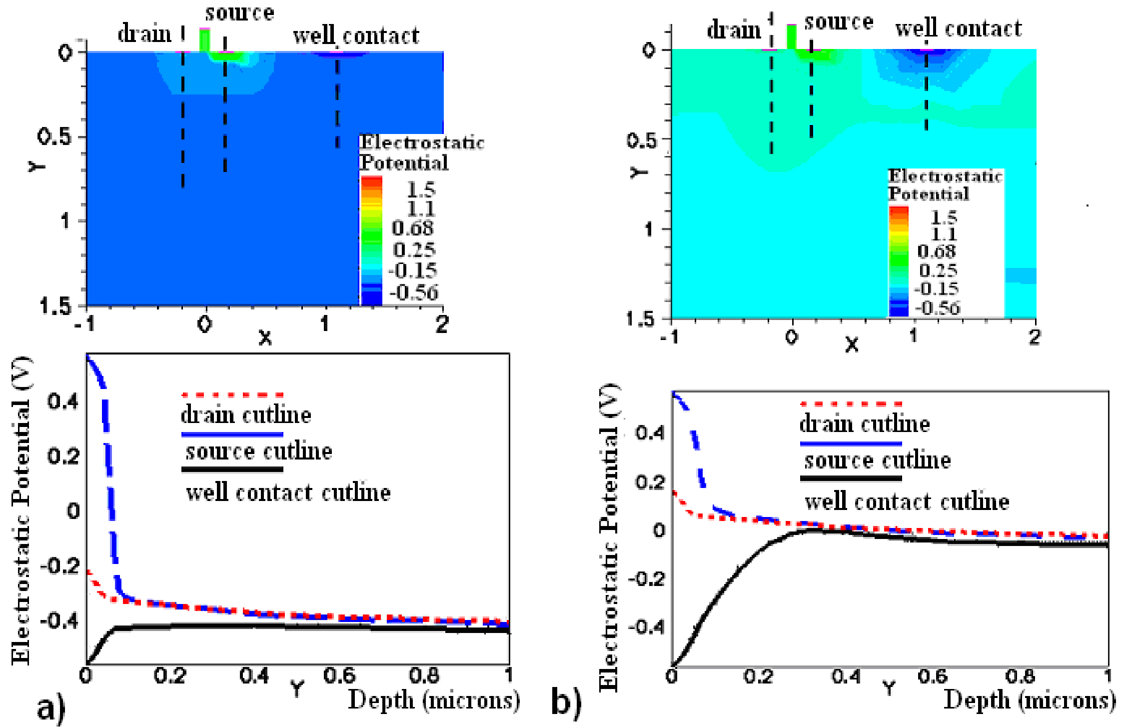


Fig. 22. Contour plot of potential (top) and 1-D profile of potential (bottom) underneath the drain, source and well contact for a a) highly doped (5×10^{17} cm^{-3}) and b) lightly doped (10^{16} cm^{-3}) substrate. Significant potential drop at the well contact leads to low source-substrate junction potential, which translates to a small excursion of the drain voltage below the rail (Table II). The depth of the heavily doped well contact in this case is 80 nm. Cutlines have been obtained 25 ps after a strike of LET 10 MeV/(mg/cm^2). Potentials are referenced to Ei, i.e., $V(x) = \Phi_s(x) - E_i/q$.

5.3. Summary of the mechanism of the plateau

1) Within a few picoseconds of the heavy ion induced charge generation, the mobile charge cloud spreads across the entire well**,** neutralizing the drain body junction and pushing the location of the drain potential gradient outwards from the metallurgical junction.

2) The neutralization of space charge goes on until a region of extremely high doping (the well contact) is reached. This arrests the potential because the space charge is too high to be neutralized by the deposited charge.

3) The drop in the high-low junction next to the well contact does not change much until the number of carriers is low enough for the drain body junction to recover, and return the well back to its normal potential. This fairly constant potential drop near the contact

during the plateau causes the excursion of the drain potential below the rail, since there is no other region in the high conductivity well to create a potential drop across.

4) The gate and source voltage of the pull-up PMOS are pinned. The drain potential during the plateau is fairly constant, and it reduces the possibility of capacitive currents to the next stage (Fig. 15). The entire SE current passes through the pull-up PMOS.

For low LETs, the classical double exponential charge collection pattern is still valid.

5.4. Conclusion

This concludes this section, where a detailed study of the charge collection mechanism (as shown by TCAD simulations) has been performed; a hypothesis has been formulated and tested against different cases of substrate doping and well contact depths.

CHAPTER VI

THE RECOVERY MECHANISM

An observation about the single event transients in deep sub micron CMOS is that, the recovery is extremely fast in the aftermath of the plateau (Fig. 8 – 12). While one might think that the recovery would be fairly gradual, depending on the rate at which minority carriers are removed and the drain body junction is restored, the reality is somewhat different. Even for a high LET of 40 MeV/mg/cm^2, the time from the end of the plateau to half rail on the voltage pulse takes place within about 50 ps. If the reversal of the SET were simply due to enough charges being removed for the drain body junction to recover, then the topside contact sizing would have changed pulse widths (since this is the only outlet for minority carriers in the NMOS). But repeated simulations have proved otherwise, within large limits.

In addition to this, there are quite a few characteristics of the current SET which require a better explanation than simply charge collection and removal through the different contacts.

1) As can be seen from the charge collection curves, the fraction of charge collected to charge deposited inside the collection volume is low (about 1:6 to 1:10) and the collected to deposited charge ratio keeps getting lower as we move higher up in LET.

2) Very surprisingly, the SET current is not a single carrier current. It is actually composed of almost equal counterbalancing components of electrons and holes. These component currents have a strong dependence on LET, and have nearly double exponential profiles in time.

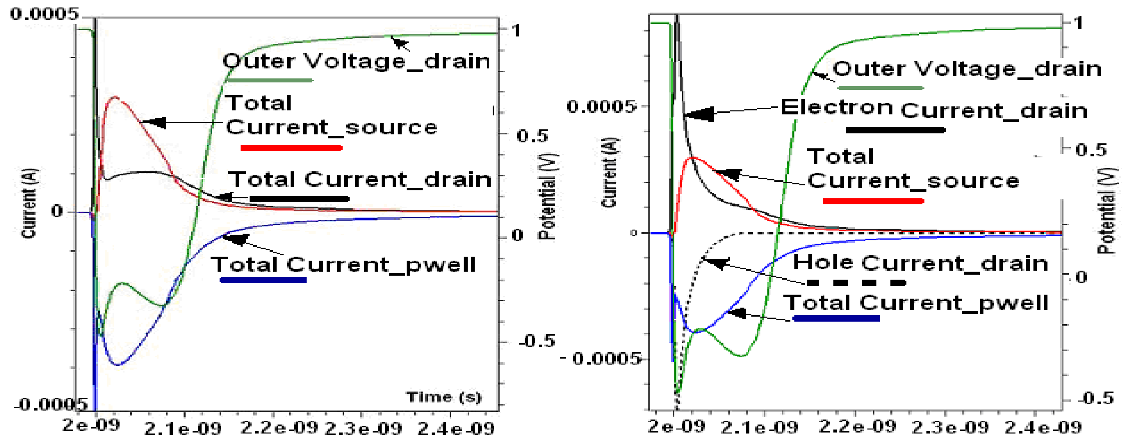


Fig. 23. Current profiles at different terminals of the struck device and potential profile at drain. Figure on the right shows the total drain current and one on the left shows the breakup of the drain current into electron and hole current components.

The above result is unexpected because of the very high n-type doping of the source/drain diffusion regions. Note that the drain is the only terminal, which gets an ambipolar current. This is not the case for the source or p-well, which are pinned. The simulation was repeated with a small resistance (only about 10 Ohms) as the only load, and this time, the Single Event current was almost like the electron current plot, with no hole current at all.

A particular correlation between the hole current and the potential transient was repeatedly observed. Wherever the hole current hits 0, the voltage SET recovers. The rate of the recovery is usually fast, and varies with the substrate profile, but the simultaneity of the transient reversal and the hole current disappearance is something that has been observed for almost all devices, for all pull-ups and LET range. While the first instinct might be to reject the hole current as a simulation artifact, it is necessary to make a careful analysis of the hole current before we accept or reject its relevance.

6.1. Sanity Checks on Simulation Currents

1) **Drift: $J = n.q.\mu.E$**

The 20 ps. time slice after the strike (Fig. 25) is studied. The current SET graph (Fig. 24) shows the electron current roughly at 500 microamps. The voltage drop is roughly 100

mV over the first 60 nm, as the 1-d cuts show (Fig. 25). This is the only stimulus the electrons have. Their gradient is not very large, and the field is negligible over the first micrometer from the surface. This puts **ε** roughly at 1.67e+4 V/cm. A mobility probe close to the contact put the mobility at roughly 20 cm^2 / (V-s) (pretty reasonable considering the high background doping of 2e20/ $(cm)^3$. Charge of an electron is q = 1.6 $\times 10^{-19}$ C. For 500 microamps, and a source contact 120 nm on a side, J = 0.347e+7 A/cm^2. Plugging these values into the drift equation, $n = 6.4 \times 10^{+19} / (cm)^3$. Now, for an LET of 10 with a strike radius of 30 nm, this is perfectly reasonable. The density of charge inside the track is $2.2 \times 10^{+20} / (cm)^3$, assuming a uniform spread (which is not the case, it is Gaussian). So, there is no reason to suppose that this is an artifact of solving Poisson' equations in a situation with abrupt steps in charge densities.

2) Diffusion (holes): J = q.Dp.dp/dx.

Hole gradient dp/dx is known from the 1-d cuts. It is $(10^{+19})/30 \times 10^{-7}/(cm)^4$.

The value of Dp is not known. So, the hole current density about the contact ($0.185 \times 10^{+7}$) is taken and Dp is back calculated from it. Dp stands at roughly 3.4 cm^2/s . That is smaller then the lightly doped 300 K value of 13 cm^2/s, but given the high hole density, that too is reasonable.

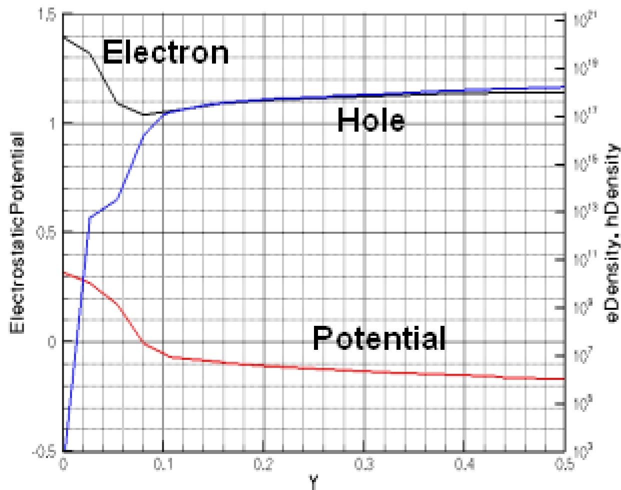


Fig. 24. Electron, Hole Cocentration and potential plot right underneath the drain contact, as a function of depth

So, we can see here that there are no discrepancies between terminal currents and carrier distributions. The huge hole gradient within such a small depth near the surface still needs to be justified, but if that gradient can be justified, the hole current can be accepted as a "real" observation.

6.2. Justifying the presence of the hole current

Consider the following statement: The electron drift current due to the residual field at the NMOS drain contact is controlled by:

1) The source/drain diffusion gradients (field) and
2) The ion LET (carrier density). Please note that increasing the LET almost proportionally increases electron drift current, because the residual field is not touched over wide limits of deposited charge.

The restoring current in the pull-up PMOS is controlled by:

1) Potential drop at well contact
2) Size of the PMOS transistor.
3) Vgs of PMOS transistor- fixed at Vdd for static logic circuits.

Needless to say, if 2 quantities are controlled by completely unrelated factors, it is perfectly possible that these 2 could be grossly mismatched. This fact plays an important role in the recovery mechanism. We need the two drain currents to be matched, because of Kirchoff's law and because very little current is observed going to the gate of the loading device, but all the possibilities of achieving that condition need to be investigated.

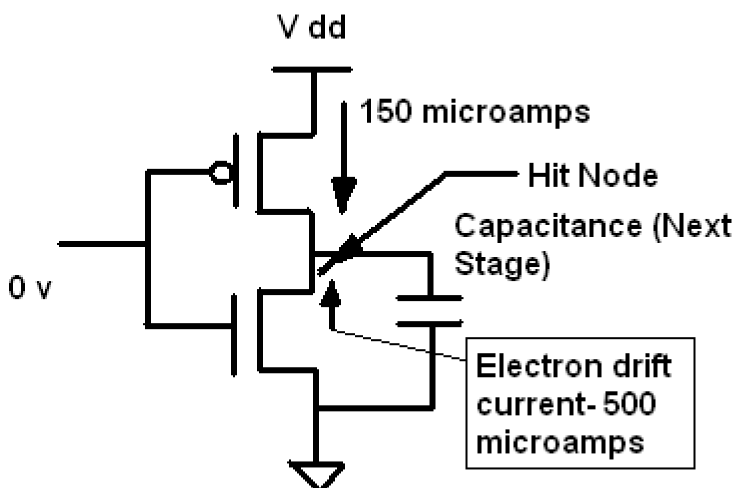


Fig. 25. Difference between the internal current stimulus and the circuit current stimulus, Kirchoff's law needs to be satisfied.

To restate the problem: Electron drift supplies way more current than the PMOS current at that voltage- but Kirchoff's law needs to hold good at that node. The first reaction to this could be that- the capacitance is the dominant load current component as it used to be in older technologies and the capacitance current could be the balancing component.

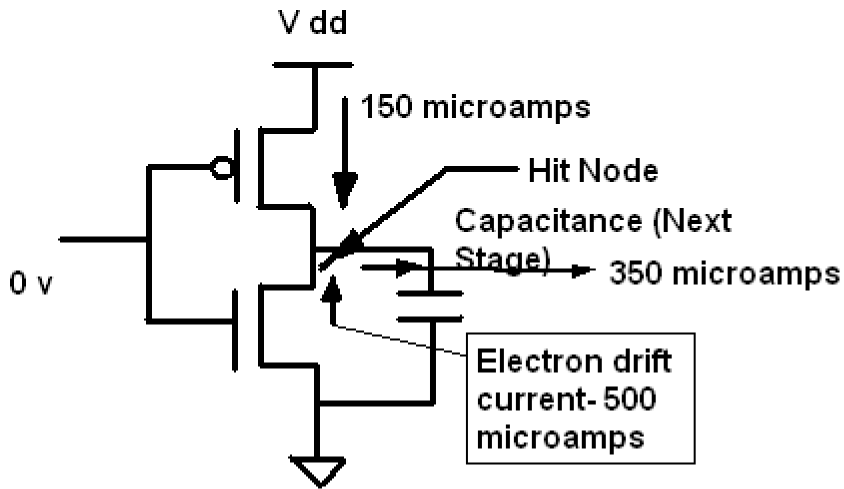


Fig. 26. Possible sinking of Single Event current through loading capacitance.

Let us consider what it means to send 350 microamps through the next stage capacitive load (roughly 5 Ff).

3) Q = C x V.

3a) I = C x dV/dt.

This would mean a voltage drop at 7e10 V/s. It implies that within 100 ps, we should see a 7 V drop. Needless to say, that is impossible. In the "plateau" portion of the SET, voltage cannot change all that fast- because the drain-body junction space charge is already neutralized due to too much charge injection. For a slowly changing potential, the only perceptible current is present through the next stage inverter gates only in the initial spiked region of the SET, after that, it's the PMOS that gets more than 95 % of the NMOS SET current. So, there's only one option left, if we have to satisfy Kirchoff's law. The counterbalancing hole current in the same direction as the electron has to be real to

maintain continuity. The electron drift is way too high for the PMOS to handle (and there's no reason why it cannot be that way), and we need a hole current to maintain continuity.

A reason that may be offered in favor of the hole current being a convergence artifact is: The hole concentration at the contact is really small. It has to be much larger to give a large hole current. The concentration need not be large. The hole current is diffusion current. As long as the hole gradient is high enough, there need not even be a non-zero concentration at the contact for a current. All that is needed is q.Dp.dp/dx to beat n.q.μ_p.ε. It does that comfortably. Please note that this current is actually opposite to the direction of the field. At the same time, within the first 20 nm underneath the struck drain, where the hole gradient exists (refer Fig. 25), potential is only about 25 mV (less than 26)- so it does not really qualify as a barrier.

However, the origin of the steep gradient of holes close to the contact has still not been adequately explained. The need for it to exist can probably be understood, but the electrostatics behind it has still not been formulated. The steady state situation is broken up into 3 different non-equilibrium steps to explain the steep hole gradient. It is not implied that the simulator actually does it this way. It is just a way of understanding a situation by breaking it into hypothetical stages. Instead of analyzing the component currents all at once, we shall introduce one current component at a time and analyze the electrostatic forces on the carriers in absence of one or more of the components.

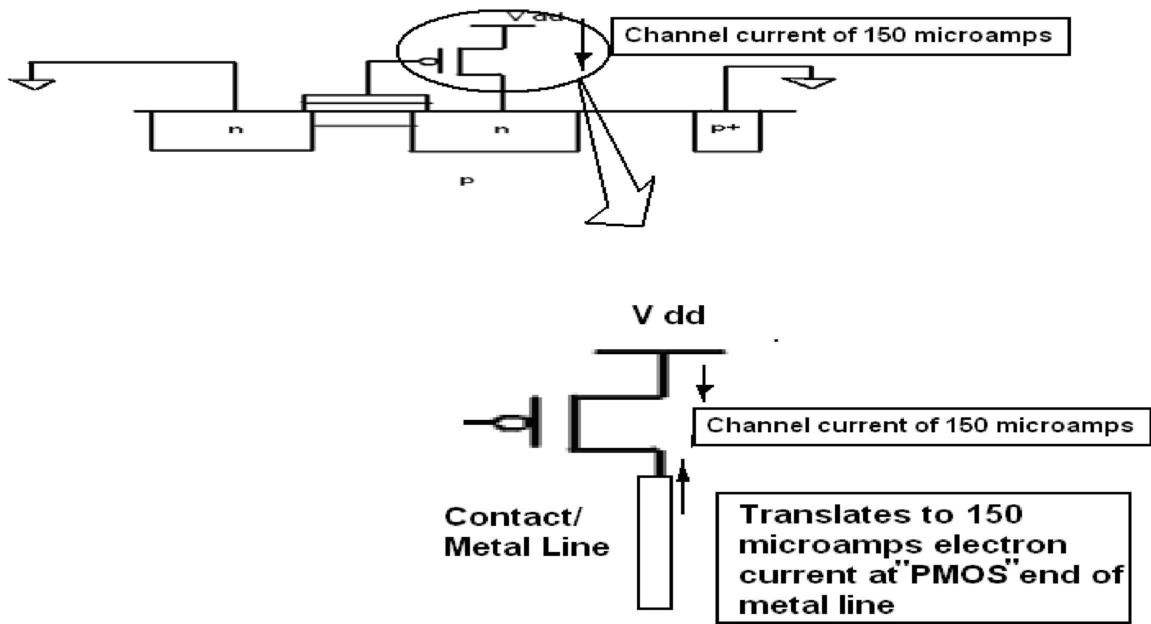


Fig 27. Formation of hole current. Step 1: Setting up the current at the PMOS end of the interconnect.

In the first step, we excite the drain end of the PMOS channel with the "plateau" current of roughly 150 microamps.

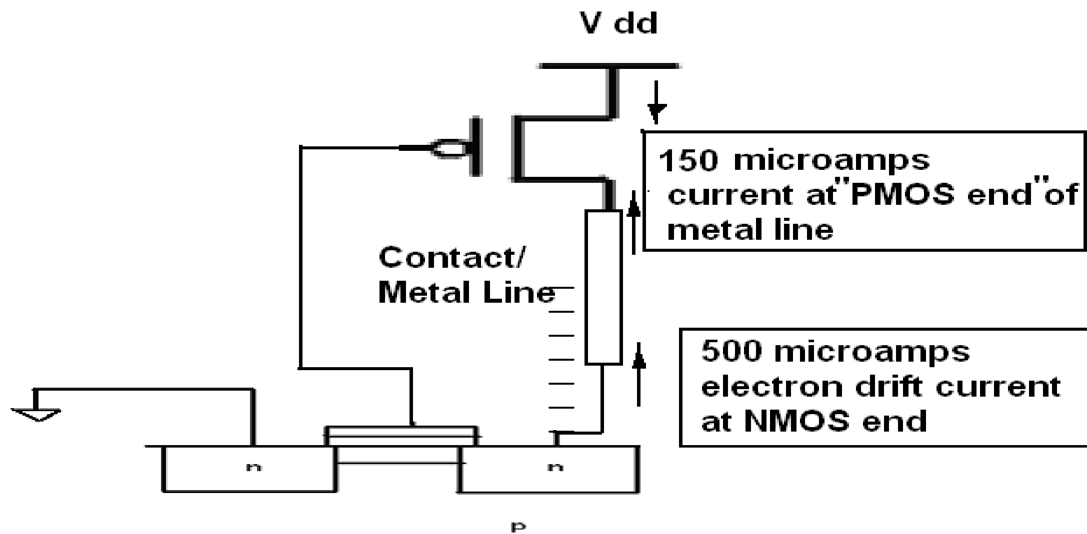


Fig 28. Formation of hole current. Step 2: Mismatch between pull-up current and electron drift current.

In the next stage, the other end of the NMOS to PMOS interconnect is excited with the terminal drift current from the NMOS. Let us for the time being, consider a quasi-equilibrium step at this stage. In this situation what is the state of the metal line? It has a charge imbalance near the NMOS end by the unbalanced component of the electron current. Please note here that the "charging the metal line" should not be compared to the charging of the nodal capacitance. This is not a proper "charging" step involving a time constant. It just describes the imbalance of charge, and the force on free carriers as a result of that imbalance. Once the line has the charge imbalance, the "imbalanced end will pull holes towards it from the drain, which has a plentiful supply of holes in the aftermath of the strike. This constitutes the hole current.

It cannot be claimed that this is a proof of existence of the hole current. We have taken a look at the convergence of the drift diffusion equations, and looked at the values of physical quantities like potential, field, mobility and carrier concentration, which lead to those solutions of the basic electrostatic and continuity equations. Since the physical quantities under observation assume values that are not unexpected, given the device geometry and charge injection, it is entirely possible that the solution is a real one.

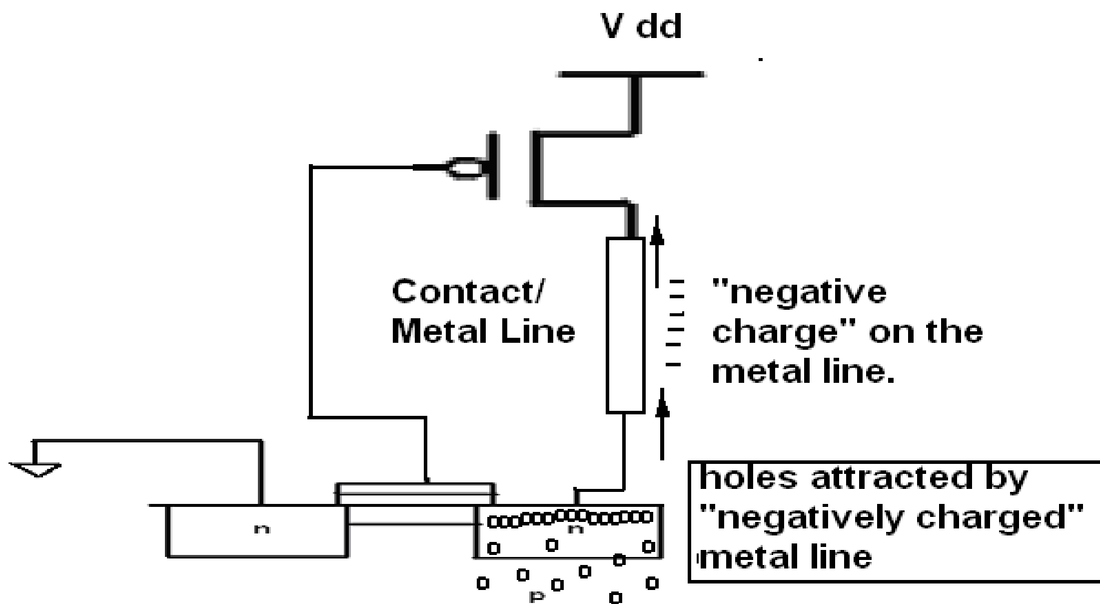


Fig 29. Formation of hole current. Step 3: Steady state achieved by introduction of the hole current.

6.3. The Recovery Mechanism

Now that the hole current has been justified- what does that tell us about the mechanism? The recovery mechanism that fits well into the observation of the simultaneous disappearance of the hole current and the reversal of the potential SET can be summed up as follows:

1) Collapse and pushout of the drain-body metallurgical junction- as long as we have injected minority carriers in the source/drain diffusions, the quasi-Fermi levels will not come back to where they were before the strike.
2) The neutralization of the space charge stops some distance from the source/drain contact- because of a very high doping concentration. The field in this portion of the source/drain diffusion (where the injected charge is much lower than the background charge) coupled with the high injection charge gives a high electron current, much higher than what the PMOS can pass.
3) To satisfy current continuity, a large hole current is set up in the same direction.
4) If the holes have to flow to the contact supplying the balancing current, how can they turn back and clear out the hit drain diffusion area? They cannot and they don't. As long as the electron concentration is not low enough, so that the drift current is weak enough for the PMOS to pass it through without a counterbalancing hole current, the holes push up close to the contact. The high concentration of holes makes it impossible for the NMOS drain-body junction to recover. This is why, we see the recovery of the SET only and immediately after the hole current hits 0, because that is when the minority carrier concentration gets low enough to allow the junction recovery.

Thus we finally can justify the huge concentration gradient of holes at the contact as a consequence of the electrostatics of the contact. This observation is also helpful in explaining the low ratio of collected to deposited charge. For every bit of collected charge that we see as the terminal current, there's a lot of current we do not see, which constitutes a simultaneous outflow of electrons and holes annihilating them on the contact, which is an infinite recombination reservoir. If this were not true, we would indeed have the DSET pulse widths becoming much longer with the progress of technology scaling, because the drive current is a factor, which does decrease every

generation. The drive current is just an indicator of the SET recovery point. Strictly speaking, the term "collected charge" should not be applied to an integrated SET current curve in a loaded device, because it is really not a measure of how many carriers flow out of the struck volume.

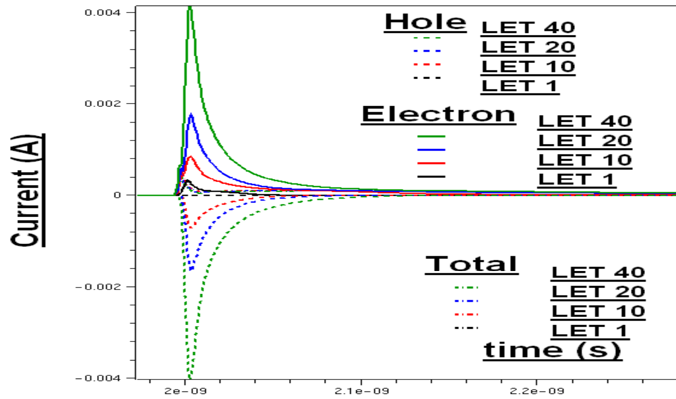


Fig 30. Actual rate at which carriers leave hit volume, for different LETs. The net current curves almost disappear on this scale. For a clearer view, refer Fig. 24, showing the breakup of current for strike at a given LET.

CHAPTER VII

SUBSTRATE ENGINEERING - EFFECT ON PULSE WIDTHS**

So far, some of the parameters affecting the pulse widths, namely the contact structure and layout and circuit parameters such as threshold voltage or pull-up current, have been studied. While these methods are effective in varying degrees in shortening pulse lengths, each one has a significant area, power or performance penalty associated with it. Since the potential modulation in the substrate has been proved to play such a significant role in determining pulse widths in deep sub-micron processes, the substrate profile might play a key role in determining pulse widths in deep sub-micron CMOS. Mitigation through substrate engineering is an attractive option, because:

a) It is relatively simple compared to a layout modification or a redundancy scheme.

b) It can provide an alternative scheme of hardening in which relatively high performance circuits can operate with acceptably small error rates, and low penalties.

The feasibility of the substrate modification is different for different substrate engineering schemes. It is interesting to start off with some options, which suggest only minor changes to existing popular substrate profiles, mostly by changing doping levels or gradients by an order of magnitude. These are expected to create fields close to the collection depth, which would affect the total collected charge.

** The work in this section was motivated by Dr. M. L. Alles of EECE department, Vanderbilt University.

7.1. First pass, different substrate profiles, short and long-term charge collections

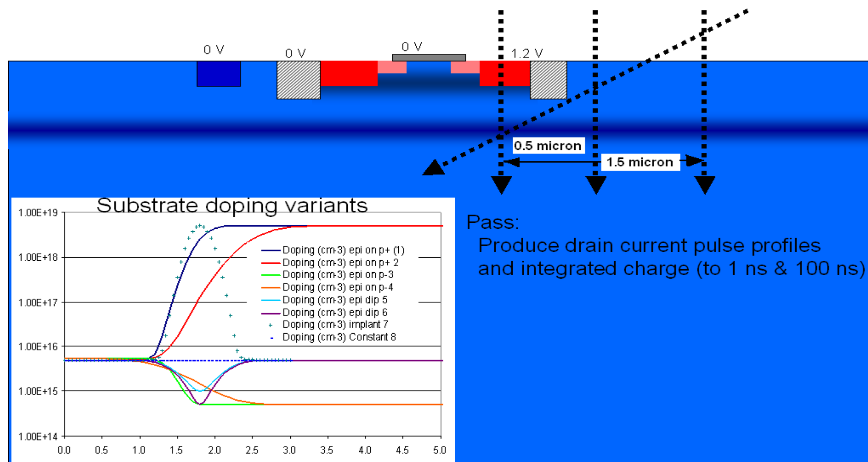


Fig 31. Substrate engineering, first pass- small variations of deep p+ buried implant layer, epi on p+ substrate compared against the base case of no substrate engineering. A few structures with epi dip were also tried.

In the first pass of this study, we tried to find out the relative effectiveness of different popular substrate profiles, in terms of long and short term collection. The profiles used were:

i) Buried p+ layer on a lightly doped substrate.

ii) epi on p+ substrate, which is a popularly used choice because of its resistance to latchup.

iii) A slightly thicker epi on p+.

iv) No substrate engineering, just the first well, as per the layout. This was the base case.

v), vi) A buried p- layer in a lightly doped substrate. (epi dip)

vii), vii) epi on a substrate which is lightly doped. (epi on p+)All these substrate profiles were tested with only front side well contacts and no backside ones, as is the popular practice in several deep submicron processes. Here is a chart showing the results for short (2ns) and long (100ns) term charge collection for different substrates. All the results are for strikes with an LET of 20 MeV/mg/cm^2, in the center of the drain of the device. The circuit was the same five-inverter chain used in earlier studies.

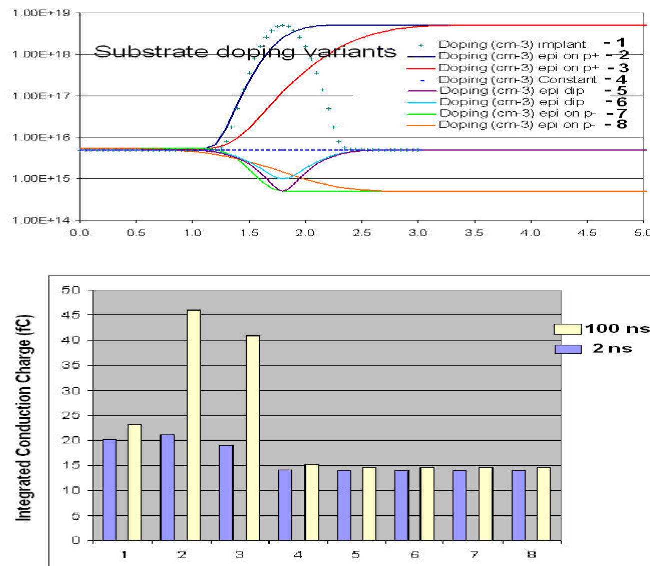


Fig 32. Substrate engineering, first pass- not a significant difference in any of the short-term collections, but significant differences in the long-term collection performance. Surprisingly, no substrate engineering seems to be the best option. P+ on epi seems to be the worst option. The difference in pulse widths was minimal not exceeding 6ps anywhere.

As has been indicated by Fig. 32, a couple of other cases were also tried to ascertain if the substrate profiles made a big difference to pulse widths from strikes that were oriented in a particular way with respect to the region having the highest gradient. Two normal strikes were tried, one half micrometer and one 1.5 micrometer away from the center of the drain (both through the STI). The 3rd case was an angled strike at 60 degrees to the normal, passing the region of high doping gradient right underneath the drain. All the cases gave the same trends in long-term charge collection, and none of the angled or off-center strikes showed actual upsets.

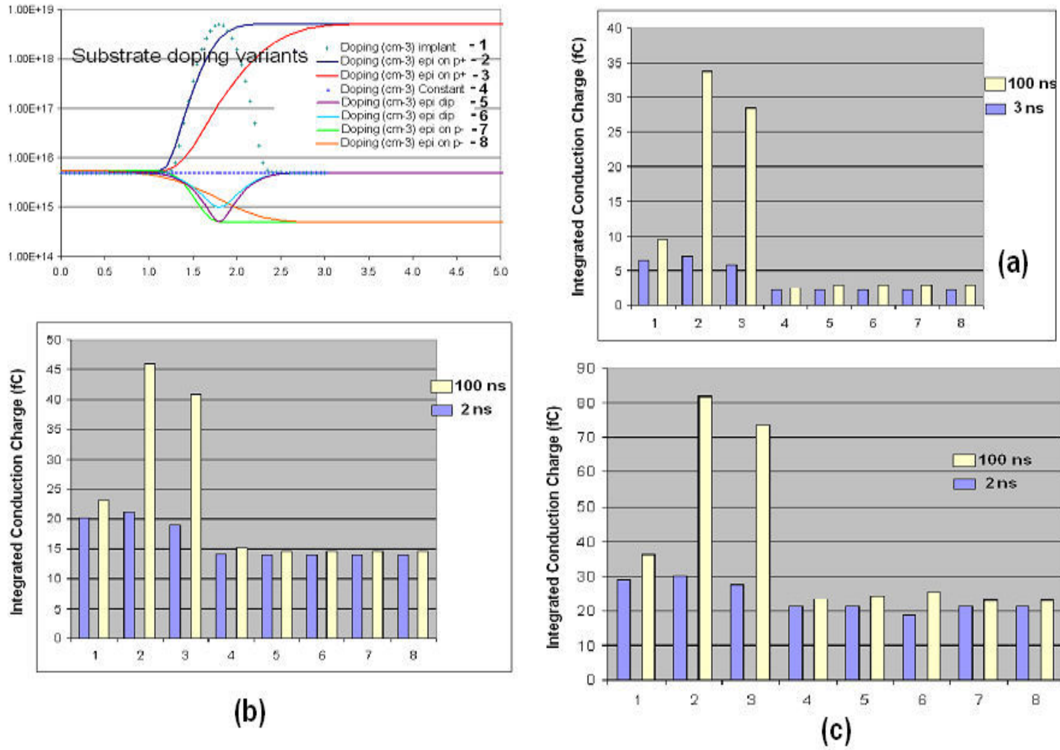


Fig 33.Long and short-term collections a) vertical strike 0.5 microns from the drain center, b) 1.5 micron form drain center, c) angled strike at 60 degrees passing under the drain at the p+/p junction (refer Fig. 32). In all cases, no substrate engineering seems to be the best option. P+ on epi seems to be the worst option.

Although any significant mitigation was not achieved through this exercise, some important insights were obtained as to what the desired features of a substrate doping profile should be, in order to improve resistance to Single Events. If the reason behind the higher collection in the epi on p+ substrates is sought, an analysis of the direction of fields setup by a given doping gradient has to be made. Please note that no doping profile or junction acts as a “barrier” to both type of carriers- if it repels one type, it will attract the other type.

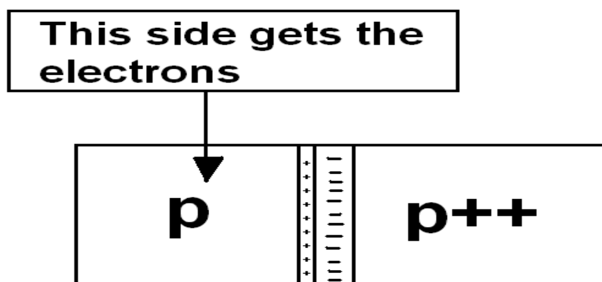


Fig 34. Alignment of fields for the epi on p+ substrate. After the recovery of the weak junction p+/p junction, the side closer to the device (lightly doped epi) gets more electrons.

Consider the case of the epi on p+ substrate against the no substrate engineering case. The positive field points towards the epi side, or the side of the shallow well, in which the device is present. This field direction attracts electrons from the deep substrate. In the aftermath of the strike, with very high charge densities having destroyed the gradient at the p+-epi confluence, this field will not play a significant role. However, after an appreciable period of time (say 25 ns), when all the gradients have gone back close to their equilibrium state in terms of charge density, this "wrongly" directed field rolls back majority carriers (electrons) for the device to collect.

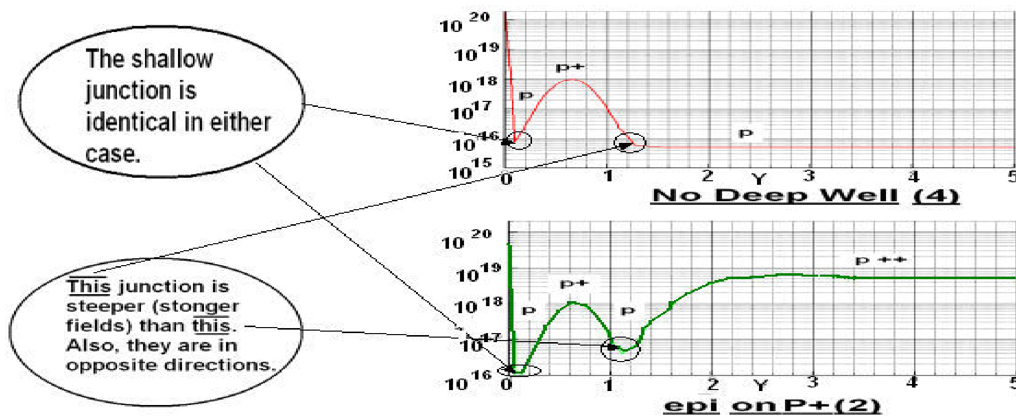


Fig. 35. 1-d doping gradients for a) no substrate engineering, b) epi on p+.

Notice, the main points of difference, as pointed out in Fig. 36, between the epi on p+ and the base case is the gradient at the junction of the main or first well and the deep substrate. In one case, the p++ points to the deep substrate, and the p is towards the device, while in the other, the higher doping is the first or main well. So, the p+/p direction has been reversed, and so has the direction of the field. But there is one more high-low junction to consider here- the one between the first-well and the lightly doped epi, i.e. the side of the well hump opposite to the well-drain junction. This junction should be rolling back electrons into the doping "trough" between the well and the deep substrate p+. So why is the collected charge so great for the epi on p+ ? To answer that

question, the magnitude of the field and potentials due to these 2 high-low junctions need to be looked at and compared.

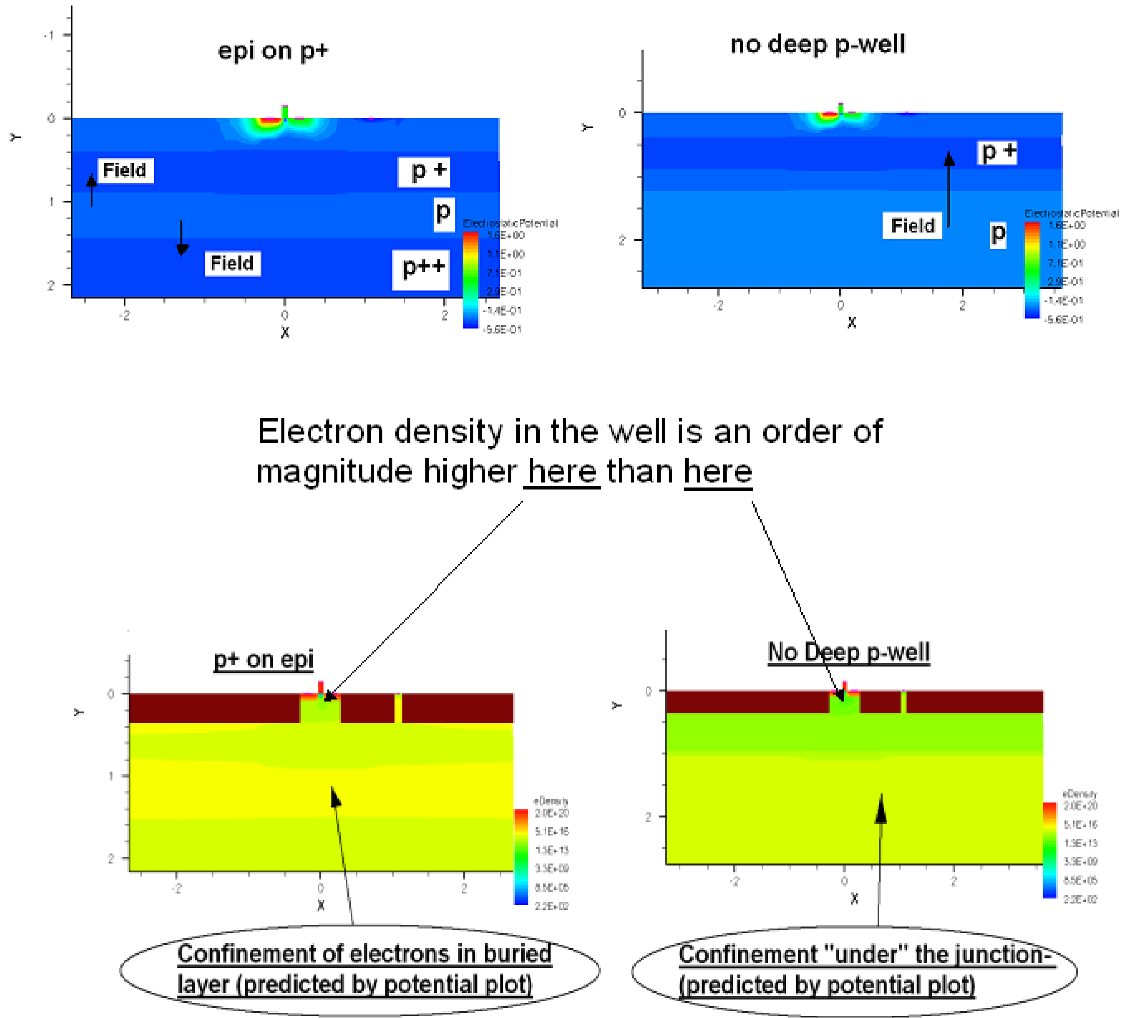


Fig. 36. Concentration profiles at a plane at the center of the drain 25ns from the strike. The direction of the field due to the in-built potential has been marked on the potential contour plot. Electron density as a consequence of these fields shows the predicted trends.

As is demonstrated by Fig. 33, the in built fields point away from the lightly doped regions. This implies that electrons (which will be repelled by the field lines), will be pushed towards the "trough" in the epi on p+ case. Where there is no deep well, the entire

substrate below the well will get the electrons. So effectively, in the first structure, electrons are being collected in a thin layer, and in the second one, they are being pushed into the substrate underneath the well. This is clearly demonstrated in Fig. 38, where the deep yellow patch of high electron concentration can be seen in the trough layer. Needless to say, a thin layer is much less effective in confining the electrons than a deep substrate chunk, which is why, a lot more holes spill past the "trough" onto the device side.

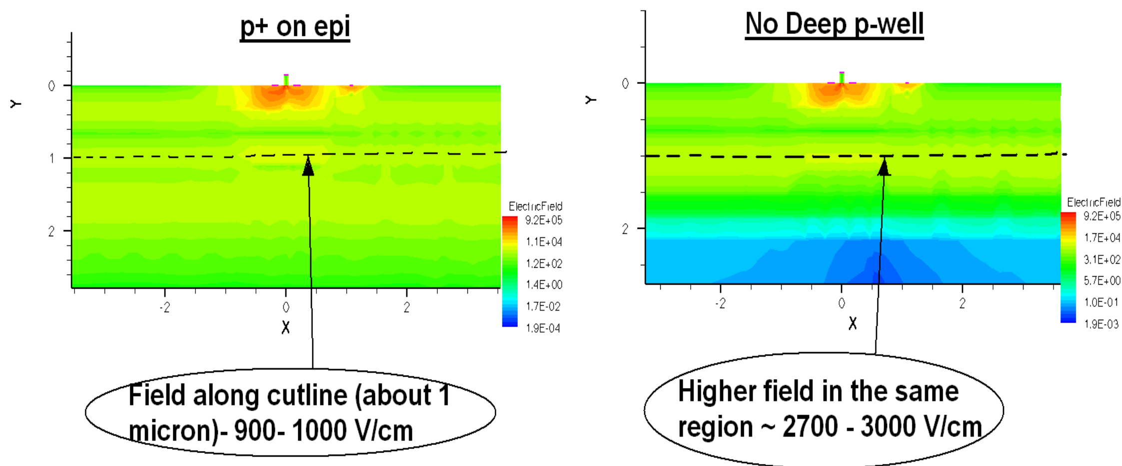


Fig. 37. Field magnitudes at a plane at the center of the drain 25ns from the strike. The relative magnitudes at 1 micron depth (roughly where the "trough" is centered) have been highlighted.

Also, if the fields at the high-low junction (roughly 1 micrometer) in either case are compared, an important detail is noticed- the somewhat abrupt nature of the high-low junction in the profile with no deep well gives a field that is about 3 times stronger than in the epi on p+ case, which again explains the very significant difference between the long term collection in the two cases. More importantly, it provides a concrete reason for the significant differences between the epi on p+ (2 or 3) and the deep p+ implant (1) cases.

So, in spite of the fact that no significant improvement in mitigation has been achieved with any of the techniques used, a few important things about charge collection have

been concluded, namely- the effects that matter are the orientation of fields in the deep substrate, and the effect of confinement of charge in a given region on the in-built fields in that region.

7.2. Diffusion collection

The reason behind the negligible effect of substrate engineering on the FWHM pulse widths can be intuitively understood. The argument about in built fields holds good only in situations very close to equilibrium. Close to the strike instant, the high charge concentrations involve a lot of modifications to these fields- in most cases weakening of the fields. In case of strikes at the center of the drain, where the charge density inside the collection volume is extremely high, the effect of a minor modification of the substrate field is negligible. However, if a significant amount of the deposited charge has to diffuse across the weak high-low junction in built potential gradients, then we could probably see a greater contribution of the in built fields in shortening pulse widths. The table below will show a comparison between pulse widths for strikes at different distances from the center of the drain for the three major cases (epi on p+ , no substrate engineering and deep p+ implant) indicated by the previous sections.

Table II: Diffusion Charge collection for different strike locations. 3 main substrate profiles studied.

Substrate	Location	Edge of drain	50 nm from drain	100 nm from drain	150 nm from drain
Epi on p +		160 ps	145 ps	90ps	80 ps
Lightly doped substrate with p+ buried layer		160 ps	140 ps	80ps	70 ps
No substrate engineering, only a shallow well.		150 ps	135 ps	65 ps	50 ps

As has been predicted, the relative improvement in pulse width mitigation does increase with the distance from the center of the drain. From just about 5 percent at the edge of the drain, it increases to about 30 % for a strike 150 nm from the drain. The problem however, is that, this happens only in a range where pulse widths are sufficiently small, so that the absolute improvement is not too good. In the next 50 nm distance, a full upset is not observed any more. So, there will probably be some improvement in error cross-section, but not a very large one.

7.3. Proper Combination of Substrate Profile and Contact Scheme

All our simulations, as mentioned were with no backside substrate contacts. There are reasons to believe that the presence or absence of a backside substrate contact would make a significant difference to the pulse width. As we saw earlier, in chapter 5, a backside contact gives a distinctly higher "plateau" voltage (more negative for NMOS), which implies a much higher pull-up drive current. Secondly, the recovery following the "plateau", which we have not discussed in detail, could be slow, depending on the surrounding concentration of holes. The backside contact will affect the rate of outflow of holes, so for a slowly recovering SET, the presence of a backside contact might make a significant difference.

The contribution of the recovery tail to the FWHM pulse widths was increased by using a very small pull-up. The reason behind low pull-up transistors giving a gentle recovery slope can be traced back to chapter 6, where the recovery mechanism is described. For low pull-ups, the excess carrier concentration close to the struck drain at the point of recovery (end of the plateau) is pretty low. The continuity requirement induced by the contact electrostatics pulls back the holes towards the device junction, and there is a lack of continuity in hole concentration between the metallurgical junction location and the deep substrate. Equalizing this discontinuity through diffusion of holes back into the substrate is relatively time consuming, and the pulse widths get longer. Of course, in this case the reverse argument of the electron collection from the deep substrate works. Since it is the hole collection that is being discussed, the p+ side of the deep well has the requisite field direction to attract the free holes. With a backside contact on, the rate of removal of holes will be faster, and the epi on p+ will have the correct

direction for removal of holes and having a steeper recovery slope. The next simulation clearly demonstrates this. Instead of using matched inverters, we use pull ups of equal size as the struck device. One had a p+ on epi implant with a backside contact; the other one was the usual deep p+ buried implant substrate with only front side contacts.

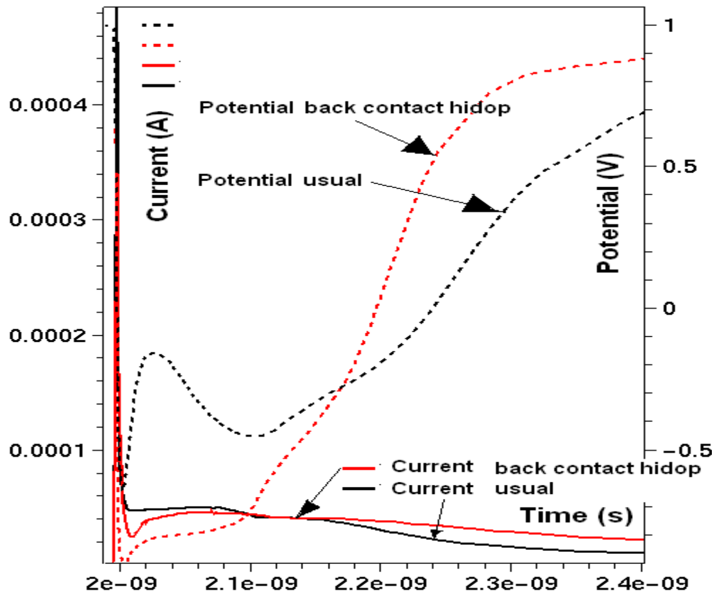


Fig. 38. Single Event current and potential profiles for an LET of 20 MeV/mg/cm^2, for a strike in the center of the drain for an inverter chain with similar sized NMOS and PMOS. The structure with a epi on p+ and a backside contact has a significantly shorter pulse (about 35 %).

It can clearly be seen here that taking use of the slow recovery in the SET tail, and accelerating the outflow of holes from the hit device, the pulse widths have been reduced by about 35 %.

So, at the end of all these studies, the following conclusions are drawn:

1) The orientation of fields in the substrate affects mostly long term charge collection, but does not have significant effect on the pulse width.

2) When choosing a substrate, the correct combination of the substrate and contact scheme is necessary- otherwise, a substrate engineering scheme could worsen charge collection significantly.

3) Substrate engineering has significant effects for low pull-up current conditions. For adequate pull up currents, this effect is nearly not as significant.

7.4. Substrate engineering and the longer DSETs

So far, the methods that have been discussed might be case specific answers to some of the problems of circuits in a heavy radiation environment. Radiation hardening of circuits is done by the consideration of event cross sections. In case of chips that have requirements for extremely low upset probabilities, the hardening has to be carried out against the worst-case situation, i.e. the longest pulse widths in the circuit. Mitigation by layout has its disadvantages, as demonstrated in Chapter 3. Both of these considerations lead us to introduce some measures that would address the issue of the PMOS well collapse and the parasitic bipolar turn on. The physical cross section of the p-well (having the NMOS) might be large (because it covers most of the chip), but not all that cross section is sensitive, as our simulations in Table 1 have shown. There is a much larger problem with the p-well because well collapse and parasitic device turn-ons can give upsets for strikes at very large distances (close to a micrometer) from the vulnerable node, and because the resultant upsets tend to last longer than NMOS strikes. Thus, if the issue of the bipolar effect can be addressed through substrate engineering, a huge gain will be achieved in terms of error cross-sections as well as maximum pulse widths.

7.5. Effect of buried n-type layer

The final substrate modification that will be agreed upon was reached as a result of simulations, which were performed using a buried n layer instead of a buried p layer. The idea was to shorten n-hits by creating a strong junction that would take away all the majority carriers for the device. A number of variations of this structure were tried. The different structures mostly aimed at studying the effect of bias on the buried layer against confinement of charges inside the main well. In all the cases (except one), the buried n-layer was contacted through a highly doped vertical n-type layer through the p-well. As of yet, PDKs do not allow for this type of contacting. It is not impossible to achieve this type of contacting though, either by implantation or by back-filling oxide-lined deep trenches with very heavily doped poly [15]. The variations tried involved a buried layer with no contact (floating), a buried layer with a long contact extending along the entire length of the p-well, like a 1 sided triple well, a buried layer with two long contacts extending along the entire length of the p-well (2 sided triple well), and a structure

similar to the third structure with truncated well contacts. The 4th structure is to study the effect of relaxing the confinement of carriers in the p-well. All these structures had a backside contact, as would be necessary to avoid a floating substrate below the n layer.

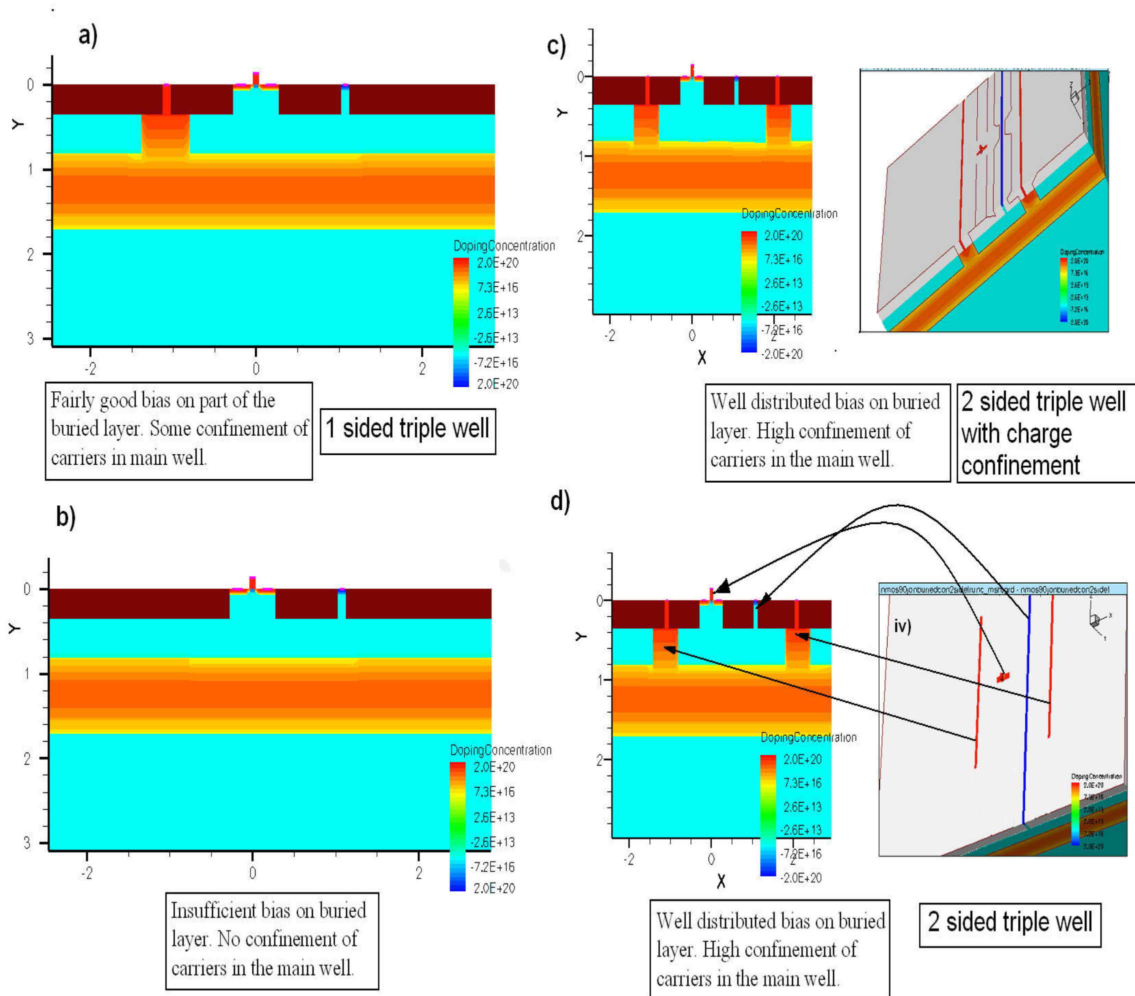


Fig. 39. 4 structures studied for the effectiveness of the buried n-layer a) Some bias, some confinement, b) No bias, no confinement, c) Good bias, high confinement d) Reasonable bias, low confinement.

The results that were obtained turned this into more of a well parasitic bipolar study. Considerable parasitic bipolar amplification was observed and pulse widths observed for

an LET of 20 MeV/mg/cm^2 were definitely higher than the pulse widths obtained in case a regularly sized NMOS in a single well.

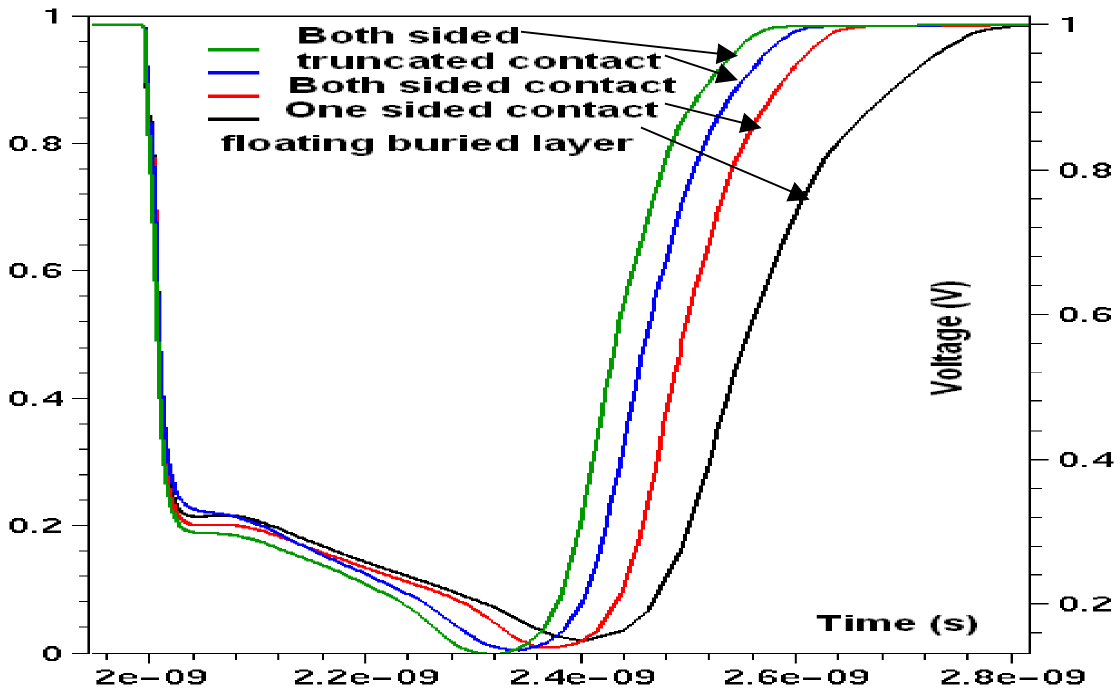
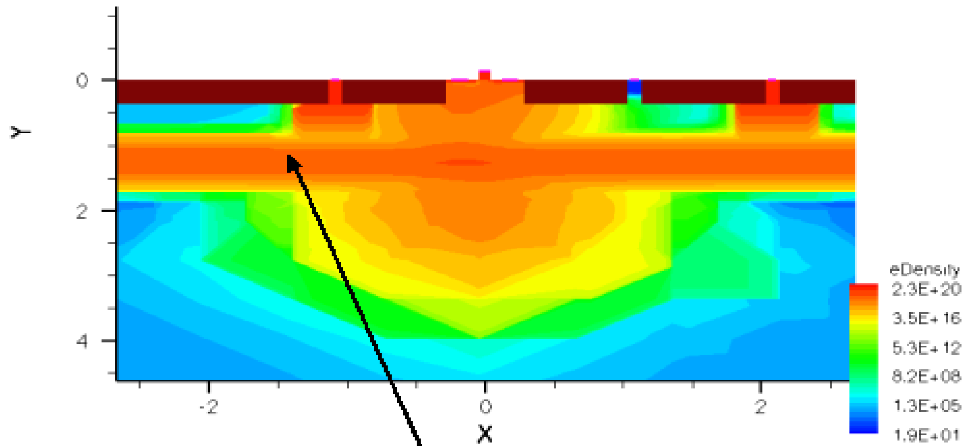


Fig. 40. Potential transients for 4 structures studied for the effectiveness of the buried n-layer. Pulse widths vary from 560 ps to 420 ps.

As the potential profiles show, a well distributed bias is necessary for the buried layer to remove charges. This can be seen in the longer pulses of the floating buried layer and the one sided triple well. A comparison between a 2 sided triple well and a truncated two sided triple well however suggests that beyond a certain point, the confinement in the well has a much higher effect on the parasitic bipolar turn on than the proper contacting of the buried layer. This might be kept in mind; because contacting the buried layer in this way is something that has to be done with our final structures as well. The internal state of the device however, gives an interesting detail.

Figure 42 very clearly demonstrates the effectiveness of a strong buried layer in abstracting almost all the majority carriers (electron in this case) from the strike. Only 50 ps from the strike, the bottom 4 microns of the strike are almost entirely cleaned out. The

excess concentration of carriers has caused a local depletion region neutralization (similar to the mechanism described in Chapter 3), which pushes out all the way up to the source and drain, neutralizing them both. The lowering of the barriers at the junctions of the source and drain with the substrate constitutes the parasitic device "turn-on".



Most electrons from the deep substrate are pulled into this layer. The polarization of charge is quick.

Fig. 41. Buried layer almost abstracts all the electrons from the deep substrate. Strike is 8 microns deep.

In all the structures we discussed so far, the buried layer has been instrumental in removal of majority carriers only. Parasitic bipolar and well collapse are caused by minority carriers for the device or majority carriers for the well (holes in this case). So, if the n-type buried layer is implemented, it might make a big improvement for the PMOS, which is the cause for the longer pulse widths and the larger contributor to the error cross section.

The structure tried out here was a buried n-layer about a micron deep, centered roughly at 2.25 microns, running all the way through the die. The contacting of this layer can be a critical issue, and there are 2 options. In the first case, it can be contacted

through the main n-well. This may be less difficult fabrication wise, but it would not be as effective, because the buried contact active will leak back electrons into the main n-well. The second option would be to contact it with a heavily doped n-type diffusion layer through the p-well. Currently, the PDK does not allow this facility, but its implementation is definitely possible. The contacting could be achieved through implantation of the n-type active layer. While this is an easier option fabrication wise, the lateral diffusion could have an effect on the device mobility and characteristics. A more complicated but better way of achieving these contacts would be etching deep trenches in the silicon all the way down to the buried layer, deposit oxide on the vertical walls to prevent lateral diffusion, and filling the trench with high-doped polysilicon.

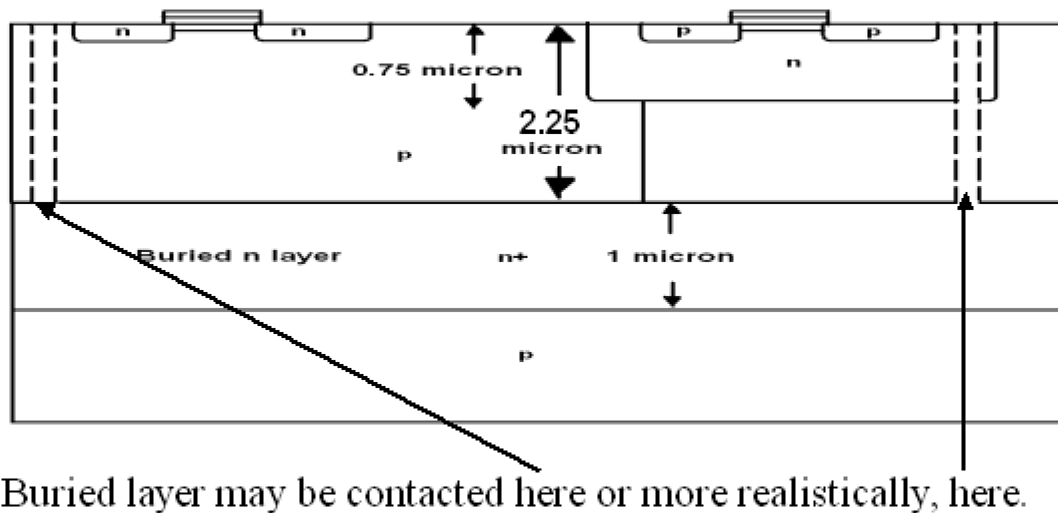


Fig. 42. Buried n-layer to mitigate well collapse and parasitic bipolar turn-on in PMOS.

The mitigation of the parasitic bipolar in the PMOS was achieved with drastic effect. Even at LETs as high as 50 MeV/mg/cm^2, there was considerable evidence of no parasitic bipolar turn on- some of the longest pulse widths were truncated by almost a nanosecond and single device charge collection was considerably improved, too. All these were achieved for contact (to the buried n-layer) placements at a fairly large

distance from the device, which indicates the area penalty due to a contact scheme that adequately mitigates the bipolar will be fairly small.

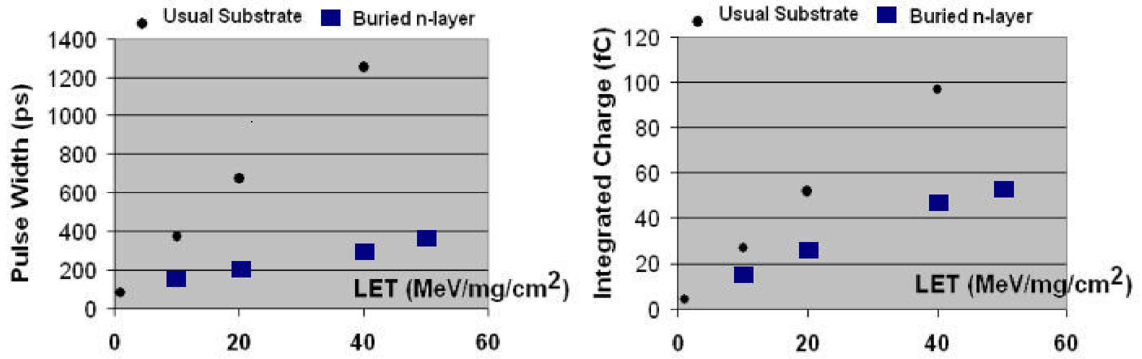


Fig. 43. Pulse width and integrated conduction charge for different LETs- no substrate engineering and n+ buried layer.

Admittedly the buried layer introduces some bipolar turn-on for the NMOS, though not as severe as the PMOS for the large depth of the strong n/p junction (2 microns).

Table III: Comparison of FWHM pulse widths for no substrate engineering and buried n-layer.

Substrate type	N/P	PMOS FWHM Pulse Width	NMOS FWHM Pulse Width	Average FWHM Pulse Width
No Substrate Engineering		1250 ps	500 ps	875 ps
Buried n-layer		290 ps	610 ps	450 ps

We still have about 50 % improvement in the average worst-case pulse width for an LET of 40 MeV/mg/cm^2 although the bipolar in the n-device decreases the reduction in sensitive cross-section. One of our next tasks will be to find the optimal depth of the

buried n-layer that would give the best possible tradeoff in terms of pulse widths, with both the NMOS and the PMOS.

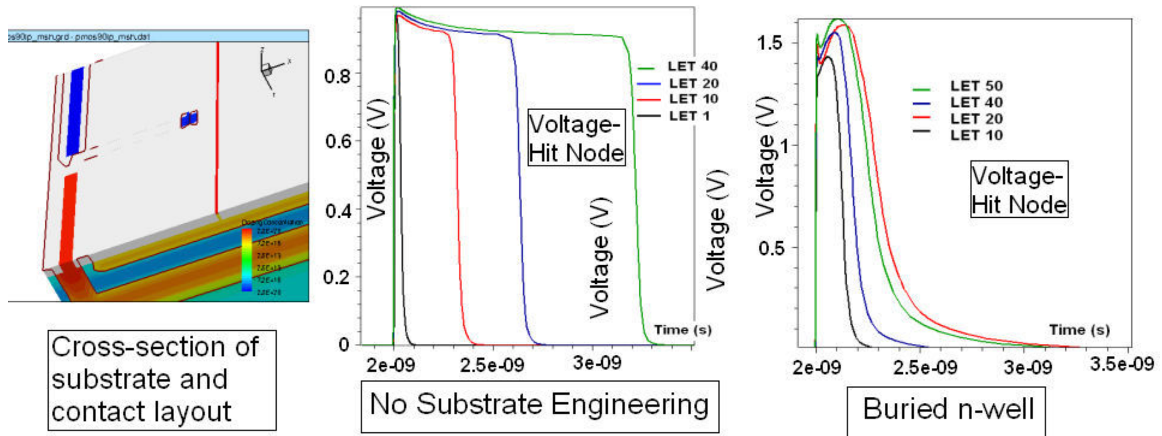


Fig. 44. 3-d view of buried n-layer structure to mitigate well collapse and parasitic bipolar turn-on in PMOS. Potential and current transients are short compared to Low Power transients for an ordinary substrate.

However, given our current capabilities fabrication wise, a lot more can be improved on this. Defining the buried layer with a patterned implant only underneath the p-channel device can eliminate the degradation in the NMOS. It is perfectly possible to define the buried well locally underneath the n-well through ion implantation, as in case of the 3rd well of a triple well process, and then contact it through the p-well. This will give the big improvement for the PMOS, and at the same time, not degrade the NMOS performance at all. For the LET 40 MeV/mg/cm^2 case, the average pulse length for the Low Power inverter will be reduced to only about 400ps. More importantly though, the well collapse will be avoided almost completely for either one of the devices, and significant improvement in sensitive cross section is expected.

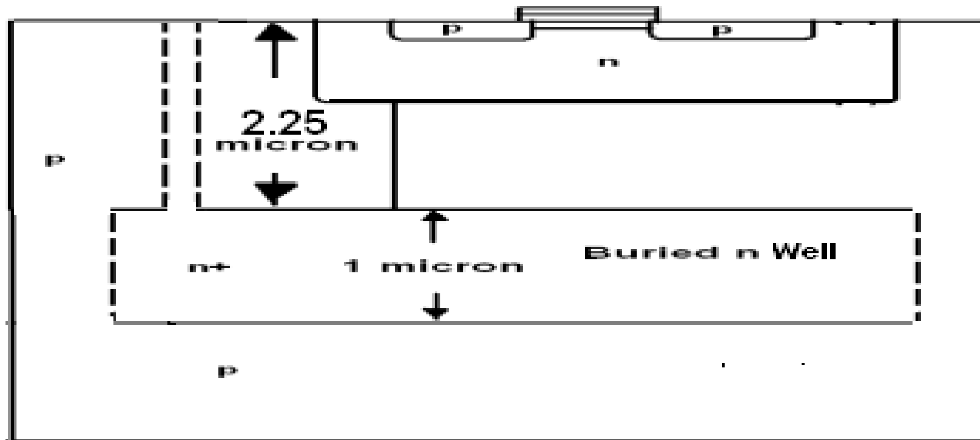


Fig. 45. Buried n-layer defined locally underneath n-well of the PMOS. Mitigation of well collapse without degrading the NMOS performance.

Let us finish with a quick word about the area penalty for this process. A topside contact on the buried layer, to be effective, is expected to have certain minimum dimension and spacing requirements. From the simulation setup shown in Fig. 43, this requirement is not very stringent, because the contact has an area equivalent to a square of 1 micrometer on a side. In addition to this, it is as much as 5.5 micrmeters away, so which indicates that spacing requirements will not be too strict, either.

7.6. Future work

The buried well option not withstanding, a buried layer going all the way through the die would be easier fabrication wise. Determining the optimal depth of the layer will be helpful in this case. Also, for sake of the ease of contacting, the option of a lightly doped n-substrate and a backside contact has to be considered and analyzed.

7.7. Summary

We have looked at a number of substrate engineering techniques, ranging from minor changes to popular profiles, their respective effectiveness when employed with a given contact scheme, to major changes involving steps outside the existing process flow. Accordingly, the improvement in Single Event response has ranged

between improvements in the long-term collection to major improvements in the longest pulse widths and sensitive cross sections. The main findings have been:

1) For topside contacts, no substrate engineering (constant doping beneath the normal shallow wells) gives the best long-term charge collection.

2) When utilizing an in-built field due to a doping gradient to screen out carriers, the direction of the fields and its effects on the majority carriers for the device must be kept in mind.

3) For low pull-up strength, a backside contact with an epi on p+ substrate can give substantial improvement in pulse widths.

4) The PMOS contributes much more to the longer pulses and sensitive cross section than the NMOS. Preventing the well-collapse by providing a separate layer to remove the minority carriers can cause a big improvement in pulse widths and error rates.

5) There are a number of trade-offs between ease of fabrication and mitigation efficiency for the n-type buried layer. All of them will show considerable improvement in the average FWHM pulse widths. However, all of them may not translate to a proportional improvement in error rates.

CONCLUSION

We studied a number of technology variants within the 90nm node and extensively characterized them. We calibrated 3-d TCAD device models and compact models to give a pretty good match to PDK characteristics. An extensive Single Event characterization was done on these models and conclusions were made regarding performance and SEE hardness tradeoffs. The additional vulnerability (longer pulse widths) of the low power (LP) technology due to its low drive strength was identified. Traditional vulnerabilities such as parasitic bipolar amplification were studied, and mitigation techniques proposed.

In the next stage, the mechanisms responsible for deciding pulse widths and pulse shapes in deep sub micron CMOS were analyzed, and a simple electrostatic model was proposed, based on the potential modulation in the substrate. The hypothesis was tested against different contact setups. A fairly extensive sanity check was done to support the observations, and the recovery mechanism was identified.

In the final chapter, we addressed mitigation of the longest pulse widths observed at these technologies through substrate engineering. An extensive analysis was conducted of the effect of different doping gradients on the pulse width and charge collection patterns for an NMOS. The compatibility of a given substrate profile with a given contact scheme has been presented and some case specific mitigation schemes have been presented. Finally, we have proposed a scheme of reducing SEE vulnerability by eliminating well-collapse and parasitic bipolar turn on. A buried n-layer, separated from the main n-well was demonstrated to shorten pulse widths very significantly, and effectively mitigate the well collapse and parasitic bipolar turn on. A large improvement in error rates is likely as a consequence of this.

In the final analysis, this thesis has outlined a central mechanism and pulse modeling technique in deep sub micron CMOS, and proposed a highly efficient SEE vulnerability mitigation technique using substrate engineering.

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APPENDIX

I. Doping profiles of Devices:

The doping profiles of the different device models were reached by iterative calibration to match the device characteristics with PDK characteristics. The substrate and well doping profiles were obtained from [Chip Report], which was a report on 130 nm devices. It was assumed that similar well and substrate profiles were used for the 90 nm devices. Same well and substrate doping profiles were used for both Low Power and High Performance device variants.

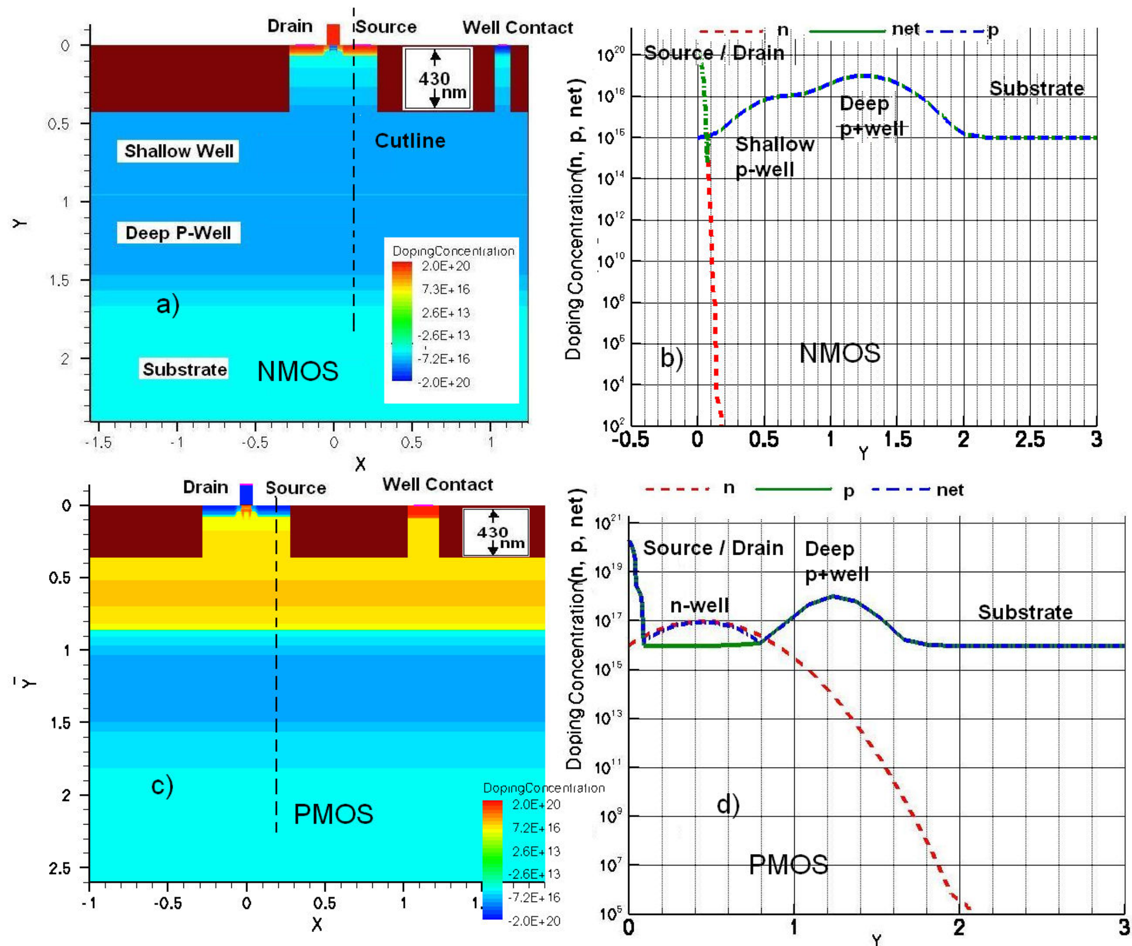

Fig. A1.1-d doping cuts showing the well and substrate profiles for the PMOS and NMOS devices. a) and b) show 2-d cross sections, and doping concentrations as a function of depth for the NMOS, c) and d) do the same for PMOS.

For the fine structure of the channel and LDD doping profiles, we choose a number of cutlines in different locations. Chapter 1 has described the main components of the channel doping profiles- These Cutlines will show some representative numbers for a High Performance PMOS device.

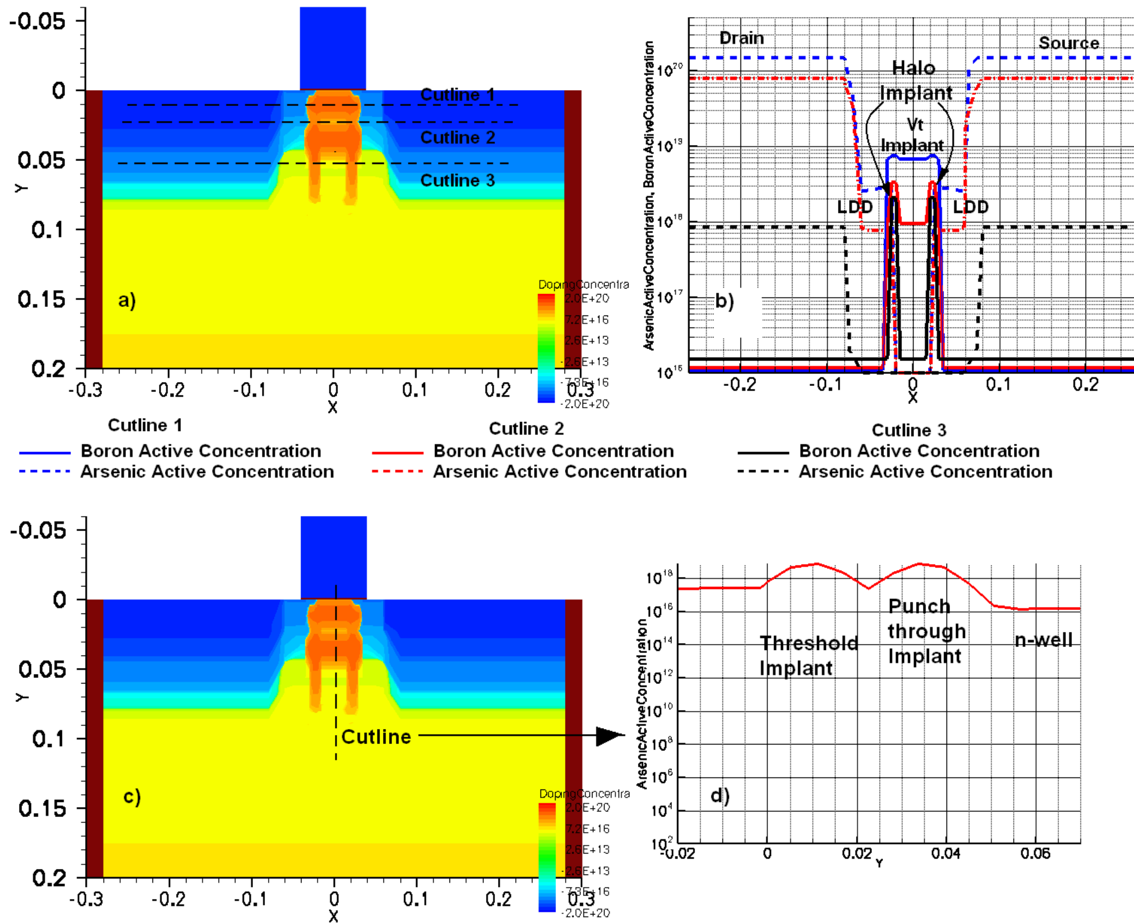

Fig. A2. 1-d doping cuts showing channel and LDD doping fine structure of a High Performance PMOS device. a) shows a 2-d cross sections with 3 cut lines at different depths. Cut line 1- goes through close to the surface. Cut line 2- goes between the threshold and punch through implant regions. Cutline 3 goes below the punch through implant, and shows only the halo implant spikes.

Ia) Doping Profiles common to all Devices:

1. Substrate: Constant p-type 1e16.

2. Deep p+ Implant: p-type, peak 5e18, 1.25 micron from surface, straggle 0.45 micron, value at depth 1e16 (throughout the die). Gaussian with y roll-off.

Ib) Similar Doping Profiles for N and PMOS devices:

1. Polysilicon Gate: 140 nm thickness, on top of gate oxide. Constant 2e20 n-type for NMOS, p-type for PMOS.
2. STI (Sidewall Implant): 430 nm (same as STI thickness) vertical sheet, with uniform doping of 5e19 on either edge of gate. Thickness of STI implant sheet is 10nm, from STI inwards under the gate.
Gaussian with vertical roll-off:
2. Shallow (main) well implant for NMOS: p-type, peak 1e18, 0.65 micron from surface, straggle 0.65 micron, value at depth 1e17 (defined by layout).
3. Shallow (main) well implant for PMOS: n-type, peak 1e17, 0.45 micron from surface, straggle 0.45 micron, value at depth 2e16 (defined by layout).
4. Source/ Drain: p+/ n+ type (for PMOS/ NMOS), peak 1e20, peak at surface, depth 60 nm, value at depth 1e17, length same as gate width, gate width 240 nm from High Performance, 260 nm for Low Power.

Ic) Channel and LDD Doping Profiles for N and PMOS devices:

1. Threshold implant:

i) For NMOS High Performance:
Peak 8e18, 10nm from surface, straggle 10nm, value at depth 3.5e17, Gaussian with vertical roll-off centered under gate- lateral spread 60 nm (effective channel length).

ii) For PMOS High Performance:
Peak 8e18, 10nm from surface, straggle 10nm, value at depth 6e17, Gaussian with vertical roll-off centered under gate- lateral spread 60 nm (effective channel length).

iii) For NMOS Low Power:
Peak 3.6e18, 10nm from surface, straggle 10nm, value at depth 1.5e17, Gaussian with vertical roll-off centered under gate- lateral spread 70 nm (effective channel length).

iv) For PMOS Low Power:

Peak 3.5e18, 10nm from surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off centered under gate- lateral spread 70 nm (effective channel length).

2. Punch through implant:

i) For NMOS High Performance:

Peak 7e18, 35nm from surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off centered under gate- lateral spread 60 nm (effective channel length).

ii) For PMOS High Performance:

Peak 5e18, 35nm from surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off centered under gate- lateral spread 60 nm (effective channel length).

iii) For NMOS Low Power:

Peak 7e18, 35nm from surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off centered under gate- lateral spread 70 nm (effective channel length).

iv) For PMOS Low Power:

Peak 5e18, 35nm from surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off centered under gate- lateral spread 70 nm (effective channel length).

3. Halo Implant:

i) For NMOS High Performance:

Peak 1e18, 25nm from surface, straggle 35nm, value at depth 1e17, Gaussian with vertical roll-off - lateral spread 5nm (on each side- source or drain, from channel edge to 5nm).

ii) For PMOS High Performance:

Peak 5e18, 25nm from surface, straggle 35nm, value at depth 4e17, Gaussian with vertical roll-off - lateral spread 5nm (on each side- source or drain, from channel edge to 5nm).

i) For NMOS Low Power:

Peak 2e18, 25nm from surface, straggle 35nm, value at depth 5e16, Gaussian with vertical roll-off - lateral spread 5nm (on each side- source or drain, from channel edge to 5nm).

ii) For PMOS Low Power:

Peak 2e18, 25nm from surface, straggle 35nm, value at depth 5e16, Gaussian with vertical roll-off - lateral spread 5nm (on each side- source or drain, from channel edge to 5nm).

4. LDD implant:

i) For NMOS High Performance:

Peak 1e19, peak at surface, straggle 30nm, value at depth 1e17, Gaussian with vertical roll-off - lateral spread 43 nm (regular drain to channel edge).

ii) For PMOS High Performance:

Peak 5e18, peak at surface, straggle 30nm, value at depth 1e17, Gaussian with vertical roll-off - lateral spread 47 nm (regular drain to channel edge).

iii) For NMOS Low Power:

Peak 8e18, peak at surface, straggle 30nm, value at depth 1e17, Gaussian with vertical roll-off - lateral spread 43 nm (regular drain to channel edge).

iv) For PMOS Low Power:

Peak 5e18, peak at surface, straggle 10nm, value at depth 2e17, Gaussian with vertical roll-off - lateral spread 47 nm (regular drain to channel edge).

Id) Other device model parameters:

Oxide thickness: 1.4 nm for High Performance and 2.8 nm for Low Power.

STI Depth: 430 nm

II. Meshing strategy and choice of substrate block size:

The meshing scheme and substrate block size are two important areas were simulation artifacts may be introduced for TCAD simulations. The mesh vertices in TCAD represent points at which Poisson's and continuity equations are discretized and solved. A mesh that is too widely spaced might cause significant errors in calculating the time evolution of the charge densities. An infinitely tight mesh is the ideal situation, but that is not possible due to memory and time constraints. An optimally tight mesh would give the shortest possible simulation time without compromising the accuracy of the simulation. The size of the substrate block is another important variable in the accuracy of the simulation. Too small a substrate block can cause the charge, (which in a real substrate block would diffuse away from the device) to get reflected off the substrate block edges and increase the charge density close to the device, giving enhanced charge collection.

The usual way to test the accuracy of the mesh is to make it tighter until no further change is seen in the simulation results. We found through a lot of simulations, some important strategies of meshing a device for a Single Event simulation. By and large the meshing in the source, drain and channel have very negligible effects on the voltage and current transients, because Single Event simulations are usually on off-state devices, and the channel is not a major deciding factor for the Single Event current. The important regions to mesh are the well contacts. A mesh with a spacing of about 100 nm is a good option for a volume around the device whose depth is same as the collection depth and whose area is covers the device and the nearest well contacts.

Increasing the size of the substrate block can resolve the substrate block issue. Ideally, the lateral dimensions should be on the order of a diffusion length, so as to prevent the issue of reflection. For substrate dopings on the order of 1e16, this dimension is about 200 microns, which is a large block to simulate. It is also very difficult to mesh this block without exceeding memory limits of the simulator. With a moderately loose substrate mesh profile, the increased substrate block size seems to make pulses slightly longer. However, on tightly meshing a 10 x 10 x 10 micron block around the device, we got back almost exactly similar results to the simulation with the 10 x 10 x 10 micron block.

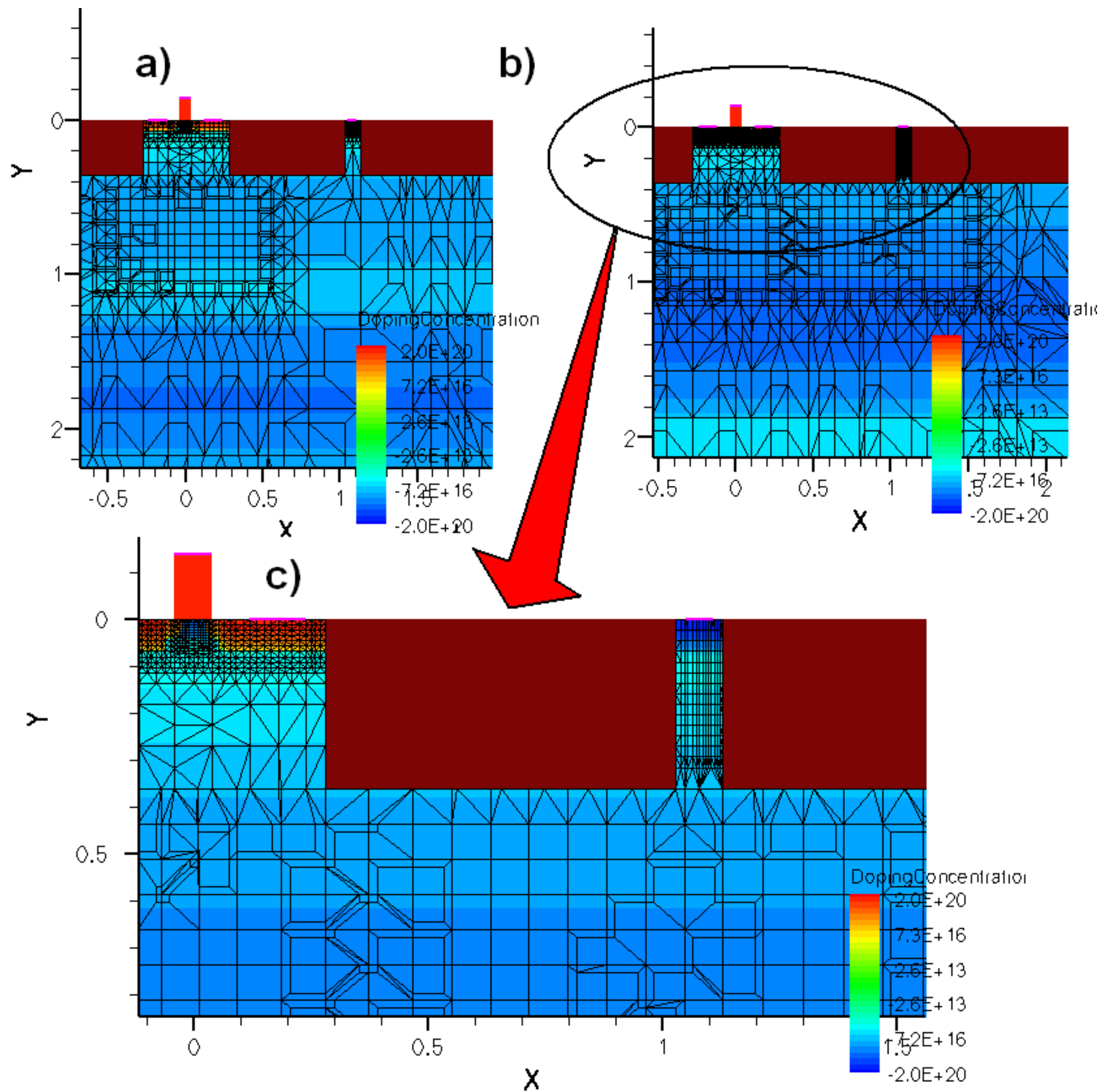

Fig. A2. Two different meshing schemes, a) with light meshing in the source drain and channel having about 85000 mesh elements and b) a very tight mesh in the same region with about 14500 mesh elements. Zoomed in view in the active device area and well contacts is shown. There is almost no difference in the transients, as Fig. A3 will show.

We show some results justifying our choice of the meshing scheme and the substrate block- mesh with 145000 elements and 85000 elements shown as b) and a) in Fig. A2. Two more simulations, one with a huge substrate block of 200 x 200 x 40 microns and a relatively light mesh in the upper collection volume, and the other with a 200 x 200 x 40 micron block, and a tight mesh in the top 10 x 10 x 10 portion. What we have been using in most simulations is a 10 x 10 x 10 block and a meshing scheme somewhere in between b) and a).

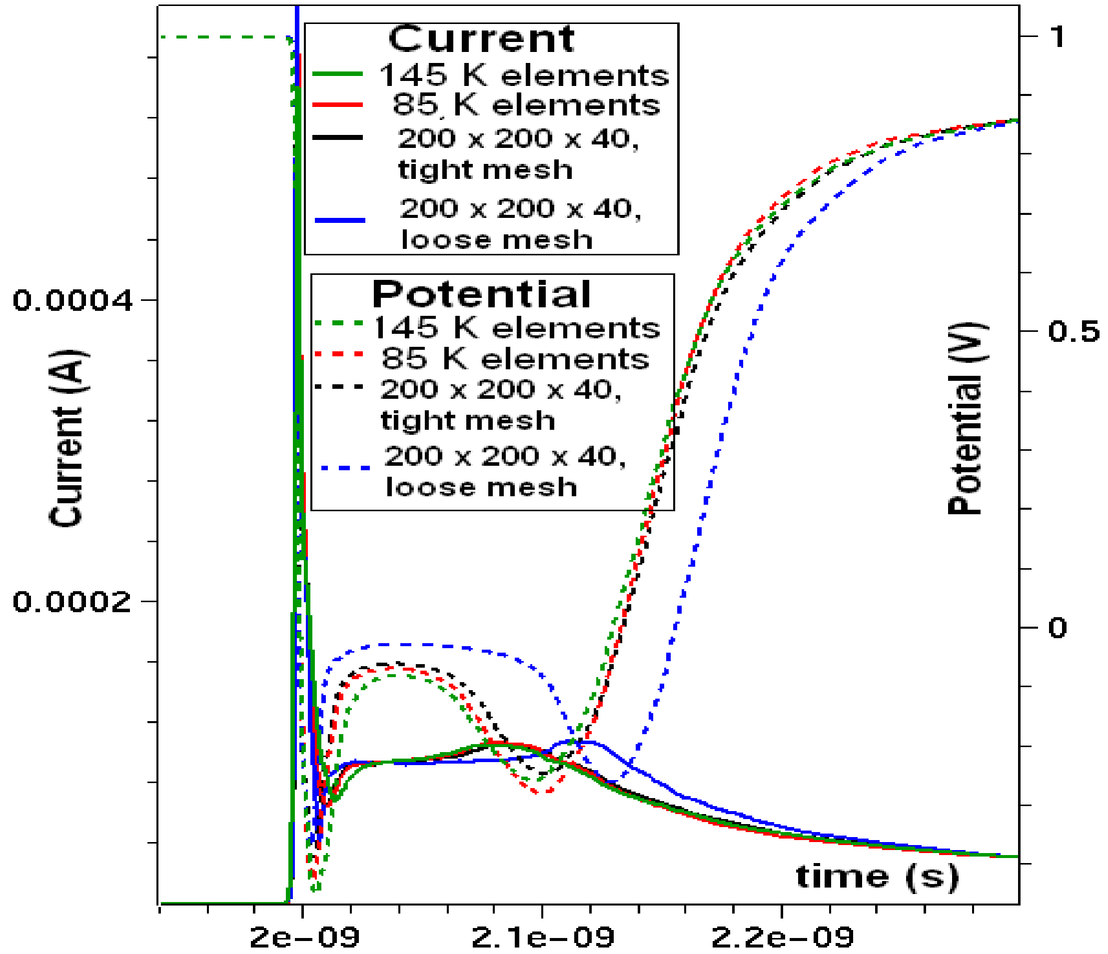

Fig. A3. Potential and current transients for 145000 and 85000 mesh elements. Two more simulations have been done with a substrate block of 200 x 200 x 40 microns, one with a tight and the other with a loose mesh. There is a very minimal difference between all these cases.

III. BSIM3 models for the devices:

NMOS High Performance:

nmos = 1

vth0 = 5.918017e-01

k1 = 2.742905e-01

k2 = -6.669476e-03

k3 = 0

k3b = 0

w0 = 0

nlx = 0

vbm = -2

dvt0 = 0

dvt1 = 0

dvt2 = -3.200000e-02

dvt0w = 0

dvt1w = 0

dvt2w = 0

u0 = 6.392374e+02

ua = -6.804152e-08

ub = -3.043522e-17

uc = 6.821090e-10

vsat = 160000

a0 = 1.000034e-01

ags = 2.947022e-01

b0 = 0

b1 = 0

keta = -4.309541e-02

a1 = -2.718153e-01

a2 = 1

rdsw = 4.472253e+02

prwb = 5.208531e-02

prwg = -5.947393e-01

wr = 1

wint = 0

lint = 0

dwg = 0

dwb = 0

voff = -1.960581e-01

nfactor = 2.929098e+00

eta0 = 1.480800e-02

etab = -5.329846e-03

dsub = 0

cit = 0

cdsc = 0

cdscb = -2.576440e-04

cdscd = -1.420956e-04

pclm = 2.386136e+01

pdiblc1 = 0

pdiblc2 = 8.787967e-20

pdiblcb = 0

drout = 0

pscbe1 = 4.166928e+08

pscbe2 = 5.399489e-09

pvag = 9.850056e-02

delta = 5.438155e-02

ngate = 0

alpha0 = 1.000000e-10

alpha1 = 0

beta0 = 1.094181e+01

rsh = 0

jsw = 0

js = 1.000000e-04

ijth = 1.000000e-01

wl = 0

wln = 1

ww = 0

wwn = 1

wwl = 0

ll = 0

lln = 1

lw = 0

lwn = 1

```
lwl     = 0
tnom    = 27
ute     = -1.500000e+00
kt1     = -3.000000e-01
kt1l    = 0
kt2     = -3.000000e-02
ua1     = 4.310000e-09
ub1     = 7.610000e-18
uc1     = -2.378000e-10
at      = 33000
prt     = 0
nj      = 1
xti     = 3
tox     = 2.000000e-09
xj      = 5.350000e-09
nch     = 7.800000e+17
mobmod  = 1
dlc     = 2.140000e-08
llc     = 0
lwc     = 0
lwlc    = 0
dwc     = 1.000000e-08
wlc     = 0
wwc     = 0
wwlc    = 0
noff    = 2.100000e+00
voffcv  = -3.000000e-02
acde    = 1.200000e+00
moin    = 10
clc     = 1.000000e-07
cle     = 6.000000e-01
```

xpart = 0

cj = 8.500000e-04

cjsw = 3.500000e-11

cjswg = 5.000000e-10

mj = 3.480000e-01

mjsw = 5.810000e-01

mjswg = 3.300000e-01

pb = 7.600000e-01

pbsw = 8.500000e-01

pbswg = 1.080000e+00

cf = 0

cgdo = 2.550000e-10

cgso = 2.550000e-10

cgbo = 0

cgdl = 5.000000e-11

cgsl = 5.000000e-11

ckappa = 8.460000e-01

tcj = 0

tcjsw = 0

tcjswg = 0

tpb = 0

tpbsw = 0

tpbswg = 0

capmod = 3

vfbcv = -1

PMOS High Performance:

pmos = 1

vth0 = -4.089577e-01

k1 = 3.435707e-01

k2 = -2.994037e-02

k3 = 0

k3b = 0

w0 = 0

nlx = 0

vbm = -2

dvt0 = 0

dvt1 = 0

dvt2 = -3.200000e-02

dvt0w = 0

dvt1w = 0

dvt2w = 0

u0 = 8.573328e+01

ua = -1.290068e-09

ub = 2.091850e-18

uc = -1.550747e-10

vsat = 160000

a0 = 7.687697e+00

ags = 1

b0 = 0

b1 = 0

keta = -7.472363e-02

a1 = -6.851165e-01

a2 = 1

rdsw = 6.771157e+02

prwb = -5.424275e-01

prwg = -7.181422e-01

wr = 1

wint = 0

lint = 0

dwg = 0

dwb = 0

voff = -1.000047e-01

nfactor = 3.201106e+00

eta0 = 2.348288e-02

etab = -8.441516e-04

dsub = 0

cit = 0

cdsc = 0

cdscb = -2.823795e-04

cdscd = -4.967410e-04

pclm = 2.094227e+00

pdiblc1 = 0

pdiblc2 = 3.805447e-03

pdiblcb = -2.047924e+00

drout = 0

pscbe1 = 4.376660e+08

pscbe2 = -1.312901e-28

pvag = -1.782638e+00

delta = 7.584024e-02

ngate = 0

alpha0 = 1.000000e-10

alpha1 = 0

beta0 = 1.098993e+01

rsh = 0

jsw = 0

js = 1.000000e-04

ijth = 1.000000e-01

wl = 0

wln = 1

ww = 0

wwn = 1

wwl = 0

ll = 0

lln = 1

lw = 0

lwn = 1
lwl = 0
tnom = 27
ute = -1.500000e+00
kt1 = -3.000000e-01
kt1l = 0
kt2 = -3.000000e-02
ua1 = 4.310000e-09
ub1 = 7.610000e-18
uc1 = -2.378000e-10
at = 33000
prt = 0
nj = 1
xti = 3
tox = 2.000000e-09
xj = 3.000000e-09
nch = 7.800000e+17
mobmod = 1
dlc = 1.950000e-08
llc = 0
lwc = 0
lwlc = 0
dwc = 1.000000e-08
wlc = 0
wwc = 0
wwlc = 0
noff = 2.380000e+00
voffcv = -8.000000e-02
acde = 6.100000e-01
moin = 14
clc = 1.000000e-07

cle = 6.000000e-01

xpart = 0

cj = 9.200000e-04

cjsw = 5.000000e-11

cjswg = 3.500000e-10

mj = 3.640000e-01

mjsw = 7.967000e-02

mjswg = 6.900000e-01

pb = 6.620000e-01

pbsw = 2.077000e-01

pbswg = 1.050000e+00

cf = 0

cgdo = 1.670000e-10

cgso = 1.670000e-10

cgbo = 0

cgdl = 1.300000e-10

cgsl = 1.300000e-10

ckappa = 1.900000e+00

tcj = 0

tcjsw = 0

tcjswg = 0

tpb = 0

tpbsw = 0

tpbswg = 0

capmod = 3

vfbcv = -1

NMOS Low Power:

nmos = 1

vth0 = 6.946453e-01

k1 = 2.588840e-01

k2 = -6.518990e-02

k3 = 0

k3b = 0

w0 = 0

nlx = 0

vbm = -2

dvt0 = 0

dvt1 = 0

dvt2 = -3.200000e-02

dvt0w = 0

dvt1w = 0

dvt2w = 0

u0 = 1000

ua = -6.848360e-08

ub = -1.042650e-17

uc = 4.410992e-09

vsat = 160000

a0 = 4.519476e+00

ags = 2.006332e-01

b0 = 0

b1 = 0

keta = -5.994306e-02

a1 = 7.149372e-02

a2 = 1

rdsw = 3.388469e+02

prwb = 1.734479e-01

prwg = -4.777294e-01

wr = 1

wint = 0

lint = 0

dwg = 0

dwb = 0

voff = -1.783939e-01

nfactor = 5

eta0 = 3.796969e-02

etab = -4.253997e-03

dsub = 0

cit = 0

cdsc = 0

cdscb = -1.669953e-03

cdscd = -1.401147e-03

pclm = 4.267361e+00

pdiblc1 = 0

pdiblc2 = 1.688315e-02

pdiblcb = 9.210287e-01

drout = 0

pscbe1 = 4.165965e+08

pscbe2 = 1.033603e-09

pvag = 4.776750e+00

delta = 1.327501e-01

ngate = 0

alpha0 = 1.000000e-10

alpha1 = 0

beta0 = 1.092925e+01

rsh = 0

jsw = 0

js = 1.000000e-04

ijth = 1.000000e-01

wl = 0

wln = 1

ww = 0

wwn = 1

wwl = 0

ll = 0

lln = 1

lw = 0

lwn = 1

lwl = 0

tnom = 27

ute = -1.500000e+00

kt1 = -3.000000e-01

kt1l = 0

kt2 = -3.000000e-02

ua1 = 4.310000e-09

ub1 = 7.610000e-18

uc1 = -2.378000e-10

at = 33000

prt = 0

nj = 1

xti = 3

tox = 2.800000e-09

xj = 6.360000e-08

nch = 2.490000e+17

mobmod = 1

dlc = 2.930000e-08

llc = 0

lwc = 0

lwlc = 0

dwc = 0

wlc = 0

wwc = 0

wwlc = 0

noff = 3

voffcv = -1.500000e-01

acde = 1

moin = 24

clc = 0

cle = 6.000000e-01

xpart = 0

cj = 9.500000e-04

cjsw = 4.490000e-11

cjswg = 1.860000e-10

mj = 3.230000e-01

mjsw = 1.000000e-03

mjswg = 3

pb = 4.317000e-01

pbsw = 3

pbswg = 9.237000e-01

cf = 0

cgdo = 1.800000e-10

cgso = 1.800000e-10

cgbo = 0

cgdl = 9.000000e-11

cgsl = 9.000000e-11

ckappa = 6.000000e-01

tcj = 9.000000e-04

tcjsw = 7.000000e-04

tcjswg = 6.000000e-04

tpb = 1.500000e-03

tpbsw = 2.000000e-03

tpbswg = 1.200000e-03

capmod = 3

vfbcv = -1

PMOS Low Power:

pmos = 1

vth0 = -4.448059e-01

k1 = 5.763476e-01

k2 = -1.143436e-01

k3 = 0

k3b = 0

w0 = 0

nlx = 0

vbm = -2

dvt0 = 0

dvt1 = 0

dvt2 = -3.200000e-02

dvt0w = 0

dvt1w = 0

dvt2w = 0

u0 = 3.241884e+02

ua = 1.292132e-08

ub = -1.254877e-17

uc = 2.912881e-09

vsat = 160000

a0 = 3.760218e+00

ags = 7.344106e-01

b0 = 0

b1 = 0

keta = 5.030666e-01

a1 = 1.685331e-03

a2 = 1

rdsw = 2.204726e+02

prwb = 8.167979e+00

prwg = 3.280445e-01

wr = 1

wint = 0

lint = 0

dwg = 0

dwb = 0

voff = -8.685920e-02

nfactor = 4.008504e+00

eta0 = 3.375992e-02

etab = -2.028398e-03

dsub = 0

cit = 0

cdsc = 0

cdscb = -1.016349e-03

cdscb = -1.016349e-03

cdscd = 8.774370e-05

pclm = 3.341063e+01

pdiblc1 = 0

pdiblc2 = 3.184844e-19

pdiblcb = 0

drout = 0

pscbe1 = 4.660921e+08

pscbe2 = -2.297577e-28

pvag = -5.081450e-03

delta = 5.027565e-02

ngate = 0

alpha0 = 1.000000e-10

alpha1 = 0

beta0 = 1.099141e+01

rsh = 0

jsw = 0

```
js      =  1.000000e-04
ijth    =  1.000000e-01
wl      =  0
wln     =  1
ww      =  0
wwn     =  1
wwl     =  0
ll      =  0
lln     =  1
lw      =  0
lwn     =  1
lwl     =  0
tnom    =  27
ute     = -1.500000e+00
kt1     = -3.000000e-01
kt1l    =  0
kt2     = -3.000000e-02
ua1     =  4.310000e-09
ub1     =  7.610000e-18
uc1     = -2.378000e-10
at      =  33000
prt     =  0
nj      =  1
xti     =  3
tox     =  2.800000e-09
xj      =  1.000000e-08
nch     =  2.490000e+17
mobmod  =  1
dlc     =  3.160000e-08
llc     =  0
lwc     =  0
```

lwlc = 0

dwc = 1.000000e-08

wlc = 0

wwc = 0

wwlc = 0

noff = 4

voffcv = -1.500000e-01

acde = 6.000000e-01

moin = 12

clc = 0

cle = 6.000000e-01

xpart = 0

cj = 8.500000e-04

cjsw = 6.300000e-11

cjswg = 2.100000e-10

mj = 3.090000e-01

mjsw = 3.300000e-02

mjswg = 3

pb = 6.810000e-01

pbsw = 1.340000e-01

pbswg = 6.170000e-01

cf = 0

cgdo = 1.800000e-10

cgso = 1.800000e-10

cgbo = 0

cgdl = 1.000000e-10

cgsl = 1.000000e-10

ckappa = 5.000000e-01

tcj = 1.060000e-03

tcjsw = 8.140000e-04

tcjswg = 1.920000e-03

```
tpb      =  1.760000e-03
tpbsw    = -2.700000e-04
tpbswg   = -3.660000e-03
capmod   =  3
vfbcv    =  -1
```

IV. Sample Scheme Script for Devise: NMOS High Performance:

```
; Setting parameters

; - lateral
(define Ltot 3.5)   ; [um] Lateral extend total
(define Lg 0.08)   ; [um] Gate length
(define subzmin -4.88); [um] Max. frontside extension in the z-direction
(define subzmax 5.12); [um] Max. backside extension in the z-direction
(define subxmin -5.42); [um] Max. leftside extension in the x-direction
(define subxmax 5.253); [um] Max. rightside extension in the x-direction
(define wn 1); [um] width of the nmos device

; Layers
(define Ysub 10)   ; [um] Substrate thickness
(define Tox 14e-4) ; [um] Gate oxide thickness
(define Ypol -0.14)  ; [um] Poly gate thickness

; Substrate doping level
(define Dop 1e16) ; [1/cm3]

; Derived quantities
(define Xmax (/ Ltot 2.0))
(define Xg   (/ Lg   2.0))
(define Ygox (* Tox -1.0))
```

```
;-----------------------------------------------------------------------------------------------
; Overlap resolution: New replaces Old
(isegeo:set-default-boolean "ABA")
;-----------------------------------------------------------------------------------------------
; CREATE REGIONS

; SUBSTRATE REGION
(isegeo:create-cuboid (position subxmin 0 subzmin) (position subxmax Ysub subzmax)
"Silicon" "region_1" )

; GATE OXIDE REGION - Main
(isegeo:create-cuboid (position (* Xg -1.0) 0 0) (position Xg Ygox wn) "SiO2"
"region_2")

; GATE OXIDE REGION - Front Extension
;(isegeo:create-cuboid (position (* Xg -1.0) 0 subzmin) (position Xg Ygox 0) "SiO2"
"region_22")

; GATE OXIDE REGION - Back Extension
;(isegeo:create-cuboid (position (* Xg -1.0) 0 wn) (position Xg Ygox subzmax) "SiO2"
"region_222")

; PolySi GATE - Main
(isegeo:create-cuboid (position (* Xg -1.0) Ygox 0) (position Xg Ypol wn) "PolySi"
"region_3")

; STI REGION - I ("behind" S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 wn) (position 0.28 0.43 subzmax) "Oxide"
"STI1" )
; STI REGION - I ("behind" S/D, till the left edge of the gate extension)
```

```
(isegeo:create-cuboid (position subxmin 0 wn) (position 0.28 0.43 subzmax) "Oxide"
"STI1" )

; STI REGION - II ("behind" S/D, from the right edge of the gate extension to edge of
S/D)
;(isegeo:create-cuboid (position Xg 0 wn) (position 0.62408 0.43 subzmax) "Oxide"
"STI2" )

; STI REGION - III ("to the right" of S/D)
(isegeo:create-cuboid (position 0.28 0 subzmin) (position 1.03 0.43 subzmax) "Oxide"
"STI3" )

; STI REGION - IV ("in front of" of S/D, till the left edge of the gate extension)
(isegeo:create-cuboid (position subxmin 0 0) (position 0.28 0.43 subzmin) "Oxide"
"STI4" )

; STI REGION - V ("in front of" of S/D, from the right edge of the gate extension to the
edge of S/D)
;(isegeo:create-cuboid (position Xg 0 0) (position 0.62408 0.43 subzmin) "Oxide" "STI5"
)

; STI REGION - VI ("to the left of" of S/D)
(isegeo:create-cuboid (position subxmin 0 0) (position -0.28 0.43 wn) "Oxide" "STI6" )

; STI REGION - VII ("to the right of p-well contact" of S/D)
(isegeo:create-cuboid (position 1.13 0 subzmin) (position subxmax 0.43 subzmax)
"Oxide" "STI7" )

;---------------------------------------------------------------------------------------------
; DEFINING AND PLACING CONTACTS
```

```
; SUBSTRATE CONTACT
;(isegeo:define-contact-set "substrate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
;(isegeo:define-3d-contact (find-face-id (position 0 Ysub 0)) "substrate")

; GATE CONTACT
(isegeo:define-contact-set "gate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0 Ypol 0.5)) "gate")

; DRAIN CONTACT
(isegeo:create-cuboid (position -0.12 0 0.25) (position -0.24 -0.2 0.75) "Metal"
"Drainmetal")
(isegeo:define-contact-set "drain_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position -0.2 0 0.5)) "drain_nmos")
(isegeo:delete-region (find-body-id (position -0.2 -0.1 0.5)))

; SOURCE CONTACT
(isegeo:create-cuboid (position 0.12 0 0.25) (position 0.24 -0.2 0.75) "Metal"
"Sourcemetal")
(isegeo:define-contact-set "source_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 0.2 0 0.5)) "source_nmos")
(isegeo:delete-region (find-body-id (position 0.2 -0.1 0.5)))

; p-WELL CONTACT (this would be connected to ground, along with the source)
(isegeo:create-cuboid (position 1.05 0 (+ subzmin 0.02)) (position 1.11 -0.2 (- subzmax
0.02)) "Metal" "pwell")
(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-3d-contact (find-face-id (position 1.1 0 0.12)) "pwell")
(isegeo:delete-region (find-body-id (position 1.1 -0.1 0.12)))

;-------------------------------------------------------------------------------------------
; Saving BND file
```

```
;(define SOI (part:entities (filter:type "solid?"))) (iseio:save-dfise-bnd SOI "nmos90jon.bnd")

;-------------------------------------------------------------------------------------------
; SET DOPING REGIONS AND PROFILES

; CONSTANT DOPING PROFILES

; SUBSTRATE REGION AND PROFILE
(isedr:define-constant-profile "region_1" "BoronActiveConcentration" Dop )
(isedr:define-constant-profile-region  "region_1" "region_1" "region_1" )

; PolySi GATE REGION AND PROFILE - Main
(isedr:define-constant-profile "region_3" "ArsenicActiveConcentration" 1e20)
(isedr:define-constant-profile-region "region_3" "region_3" "region_3")

; PolySi GATE REGION AND PROFILE - Front Extension
;(isedr:define-constant-profile "region_33" "ArsenicActiveConcentration" 1e20)
;(isedr:define-constant-profile-region "region_33" "region_33" "region_33")

; PolySi GATE REGION AND PROFILE - Back Extesnion
;(isedr:define-constant-profile "region_333" "ArsenicActiveConcentration" 1e20)
;(isedr:define-constant-profile-region "region_333" "region_333" "region_333")

;-------------------------------------------------------------------------------------------
; ANALYTICAL DOPING PROFILES

; SUBSTRATE (LATCHUP) PROFILE (IN BETWEEN THE p-WELL AND THE SUBSTRATE)
(isedr:define-refinement-window "Latchup.Profile.Region" "Rectangle" (position subxmin 1.25 subzmin) (position subxmax 1.25 subzmax))
```

```
(isedr:define-gaussian-profile "Latchup.Profile" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.4 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Latchup.Profile.Place" "Latchup.Profile"
"Latchup.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL PROFILE OF THE NMOS DEVICE
(isedr:define-refinement-window "pwell.Profile.Region" "Rectangle" (position subxmin
0.65 subzmin) (position subxmax 0.65 subzmax))
(isedr:define-gaussian-profile "pwell.Profile" "BoronActiveConcentration" "PeakPos" 0
"PeakVal" 1e18 "ValueAtDepth" 1e17 "Depth" 0.35 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwell.Profile.Place" "pwell.Profile"
"pwell.Profile.Region" "Symm" "NoReplace" "Eval")

; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT)
(isedr:define-refinement-window "pwelltap.Profile.Region" "Rectangle" (position 1.03 0
subzmin) (position 1.13 0 subzmax))
(isedr:define-gaussian-profile "pwelltap.Profile" "BoronActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap.Profile.Place" "pwelltap.Profile"
"pwelltap.Profile.Region" "Symm" "NoReplace" "Eval")

; SOURCE
(isedr:define-refinement-window "source.Profile.Region" "Rectangle" (position 0.068 0
0) (position 0.28 0 wn))
(isedr:define-gaussian-profile "source.Profile" "ArsenicActiveConcentration" "PeakPos"
0 "PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.Place" "source.Profile"
"source.Profile.Region" "Symm" "NoReplace" "Eval")
; SOURCE HALO
(isedr:define-refinement-window "HSimplant.Profile.Region" "Rectangle" (position 0.02
0.03 0) (position 0.025 0.03 wn))
```

```
(isedr:define-gaussian-profile "HSimplant.Profile" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "HSimplant.Profile.Place" "HSimplant.Profile"
"HSimplant.Profile.Region" "Symm" "NoReplace" "Eval")

; DRAIN
(isedr:define-refinement-window "drain.Profile.Region" "Rectangle" (position -0.068 0
0) (position -0.28 0 wn))
(isedr:define-gaussian-profile "drain.Profile" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" 2e20 "ValueAtDepth" 1e17 "Depth" 0.06 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.Place" "drain.Profile"
"drain.Profile.Region" "Symm" "NoReplace" "Eval")

; DRAIN HALO
(isedr:define-refinement-window "HDimplant.Profile.Region" "Rectangle" (position -
0.02 0.03 0) (position -0.025 0.03 wn))
(isedr:define-gaussian-profile "HDimplant.Profile" "BoronActiveConcentration"
"PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth" 1e16 "Depth" 0.025 "Gauss" "Factor"
0.0001)
(isedr:define-analytical-profile-placement "HDimplant.Profile.Place"
"HDimplant.Profile" "HDimplant.Profile.Region" "Symm" "NoReplace" "Eval")

; LDD - SOURCE
(isedr:define-refinement-window "sourceldd.Profile.Region" "Rectangle" (position 0.025
0.0 0) (position 0.068 0 wn))
(isedr:define-gaussian-profile "sourceldd.Profile" "ArsenicActiveConcentration"
"PeakPos" 0 "PeakVal" 1e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.Place" "sourceldd.Profile"
"sourceldd.Profile.Region" "Symm" "NoReplace" "Eval")
```

```
; LDD - DRAIN
(isedr:define-refinement-window "drainldd.Profile.Region" "Rectangle" (position -0.025 0.0 0) (position -0.068 0 wn))
(isedr:define-gaussian-profile "drainldd.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 1e19 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drainldd.Profile.Place" "drainldd.Profile" "drainldd.Profile.Region" "Symm" "NoReplace" "Eval")

; Vt IMPLANT
(isedr:define-refinement-window "implant.Profile.Region" "Rectangle" (position -0.025 0.01 0) (position 0.025 0.01 wn))
(isedr:define-gaussian-profile "implant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e18 "ValueAtDepth" 3.5e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.Place" "implant.Profile" "implant.Profile.Region" "Symm" "NoReplace" "Eval")

; IMPLANT TO MITIGATE LEAKAGE (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.Region" "Rectangle" (position -0.025 0.03 0) (position 0.025 0.03 wn))
(isedr:define-gaussian-profile "limplant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 7e18 "ValueAtDepth" 2e17 "Depth" 0.005 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.Place" "limplant.Profile" "limplant.Profile.Region" "Symm" "NoReplace" "Eval")

; STI Implant - Front & Back Extensions
(isedr:define-refinement-window "Window.FrontB" "Rectangle" (position -0.04 0 0) (position 0.04 0.36 0))
(isedr:define-refinement-window "Window.BackB" "Rectangle" (position -0.04 0 wn) (position 0.04 0.36 wn))
(isedr:define-constant-profile "Profile.ImplantB" "BoronActiveConcentration" 5e19)
```

```
(isedr:define-constant-profile-placement "Place.Implant.FrontB" "Profile.ImplantB"
"Window.FrontB")
(isedr:define-constant-profile-placement "Place.Implant.BackB" "Profile.ImplantB"
"Window.BackB")
;-----------------------------------------------------------------------------------------------------------
---------------------------------
; DEFINE MESHING REGIONS AND MAX-MIN MESH SPACINGS

; UPPER SUBSTRATE REGION
(isedr:define-refinement-size "region_1" 0.5 0.5 0.5 0.2  0.2 0.2)
(isedr:define-refinement-window "region_1" "Cuboid" (position subxmin 0.1 subzmin)
(position subxmax 2 subzmax))
(isedr:define-refinement-function "region_1" "DopingConcentration" "MaxTransDiff"
0.1)
(isedr:define-refinement-placement "region_1" "region_1" "region_1" )
; STI IMPLANT
(isedr:define-refinement-size "sti" 0.01 0.025 0.001 0.005 0.005 0.0005)
(isedr:define-refinement-window "sti" "Cuboid" (position -0.04 0 0) (position 0.04 0.36
0.002))
(isedr:define-refinement-function "sti" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sti" "sti" "sti" )

; STI IMPLANT-I
(isedr:define-refinement-size "sti1" 0.01 0.025 0.001 0.005 0.005 0.0005)
(isedr:define-refinement-window "sti1" "Cuboid" (position -0.04 0 0.998) (position 0.04
0.36 1))
(isedr:define-refinement-function "sti1" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sti1" "sti1" "sti1" )

; LOWER SUBSTRATE REGION
(isedr:define-refinement-size "region_12" 0.75 0.75 0.75 0.5 0.5 0.5)
```

```
(isedr:define-refinement-window "region_12" "Cuboid" (position subxmin 2 subzmin) (position subxmax Ysub subzmax))
(isedr:define-refinement-function "region_12" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "region_12" "region_12" "region_12" )

; CHANNEL REGION
(isedr:define-refinement-size "R.Channel" 0.01 0.01 0.1 0.002 0.002 0.1)
(isedr:define-refinement-window "R.Channel" "Cuboid" (position (* Xg -1.0) 0 0) (position Xg 0.05 wn))
(isedr:define-refinement-function "R.Channel" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "R.Channel" "R.Channel" "R.Channel" )

; SOURCE/DRAIN REGION
(isedr:define-refinement-size "sourcedrain" 0.02 0.02 0.1 0.02 0.02 0.1)
(isedr:define-refinement-window "sourcedrain" "Cuboid" (position -0.28 0 0) (position 0.28 0.1 wn))
(isedr:define-refinement-function "sourcedrain" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sourcedrain" "sourcedrain" "sourcedrain")

; Vt & LEAKAGE IMPLANT REGIONS
(isedr:define-refinement-size "implant" 0.01 0.01 0.1 0.002 0.002 0.1)
(isedr:define-refinement-window "implant" "Cuboid" (position -0.04 0 0) (position 0.04 0.07 wn))
(isedr:define-refinement-function "implant" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "implant" "implant" "implant" )
; p-WELL CONTACT REGION
(isedr:define-refinement-size "ptap" 0.1 0.1 0.2 0.05 0.05 0.2)
```

```
(isedr:define-refinement-window "ptap" "Cuboid" (position 1.03 0 subzmin) (position
1.13 0.1 subzmax))
(isedr:define-refinement-function "ptap" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap" "ptap" "ptap" )

; p-WELL CONTACT REGION-I
(isedr:define-refinement-size "ptap1" 0.02 0.02 0.1 0.005 0.005 0.05)
(isedr:define-refinement-window "ptap1" "Cuboid" (position 1.03 0 0) (position 1.13 0.1
wn))
(isedr:define-refinement-function "ptap1" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "ptap1" "ptap1" "ptap1" )
; ION  TRACK
(isedr:define-refinement-size "itrack" 0.01 0.5 0.01 0.005 0.5 0.005)
(isedr:define-refinement-window "itrack" "Cuboid" (position -0.15 0 0.04) (position -0.21
Ysub 0.1))
(isedr:define-refinement-function "itrack" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "itrack" "itrack" "itrack" )
(isedr:write-cmd-file "nmos90jon.cmd")
(ise:save-model "nmos90jon")
```

V. Sample Scheme Script: Dessis file: NMOS High Performance, LET 10 MeV/mg/cm^2:

```
Device NMOS {

Electrode {
  { Name="source_nmos" Voltage=0 }
  { Name="drain_nmos" Voltage=0 }
     { Name="gate" Voltage=0}
      { Name="pwell" Voltage=0 }
}
```

```
File {
# input files:
      Grid   = "nmos90jon_msh.grd"
      Doping  = "nmos90jon_msh.dat"
      Param   = "dessis.par"

}

Physics {
 Mobility( PhuMob ( Arsenic ) HighFieldsat Enormal )
 Fermi
 EffectiveIntrinsicDensity( OldSlotboom )
 Recombination ( SRH Auger )
 HeavyIon (
      PicoCoulomb
      Direction=(0,1,0)
      Location=(-0.18,0,0.1)
      Length=9.95
      Time=2e-9
      LET_f=0.1
      wt_hi=0.03
      Gaussian
      )
}
}

File {
 Plot="nmoslet10mm.dat"
 Current="nmoslet10mm.plt"
 SPICEPath = "."
```

```
}

System {
NMOS nmos ("source_nmos"=0 "pwell"=0 "gate"=n1 "drain_nmos"=n2 )

    rvt_pfet          MP1    (n2 n1 n3 n3)
        {w = 0.480e-6   l = 0.08e-6
            pd = 1.440e-6   ps =1.440e-6
            ad = 11.52e-14  as = 11.52e-14
           nrd = 0.01      nrs =0.01
              }


    rvt_nfet          MN1    (n4 n2 0 0)
        {w = 0.200e-6   l = 0.08e-6
            pd = 0.880e-6   ps =0.880e-6
            ad = 4.8e-14    as = 4.8e-14
           nrd = 0.01      nrs =0.01
              }

    rvt_pfet      MP2    (n4 n2 n3 n3)
        {w = 0.480e-6   l = 0.08e-6
            pd = 1.44e-6    ps = 1.44e-6
            ad = 11.52e-14  as = 11.52e-14
            nrd = 0.01      nrs = 0.01}



    rvt_nfet          MN2    (n5 n4 0 0)
        {w = 0.200e-6   l = 0.08e-6
```

```
                pd = 0.880e-6   ps =0.880e-6
                ad = 4.8e-14    as = 4.8e-14
               nrd = 0.01      nrs =0.01}


 rvt_pfet        MP3     (n5 n4 n3 n3)
         {w = 0.48e-6    l = 0.08e-6
                pd = 1.44e-6    ps = 1.44e-6
                ad = 11.52e-14  as = 11.52e-14
                nrd = 0.01      nrs = 0.01}


 rvt_nfet                MN3     (n1 n6 0 0)
         {w = 0.200e-6   l = 0.08e-6
                pd = 0.880e-6   ps =0.880e-6
                ad = 4.8e-14    as = 4.8e-14
               nrd = 0.01      nrs =0.01}

rvt_pfet        MP4     (n1 n6 n3 n3)
         {w = 0.48e-6    l = 0.08e-6
                pd = 1.44e-6    ps = 1.44e-6
                ad = 11.52e-14  as = 11.52e-14
                nrd = 0.01      nrs = 0.01}


 rvt_nfet                MN4     (n6 n7 0 0)
         {w = 0.200e-6   l = 0.08e-6
                pd = 0.880e-6   ps =0.880e-6
                ad = 4.8e-14    as = 4.8e-14
               nrd = 0.01      nrs =0.01}
```

```
    rvt_pfet       MP5     (n6 n7 n3 n3)
          {w = 0.48e-6    l = 0.08e-6
               pd = 1.44e-6    ps = 1.44e-6
               ad = 11.52e-14  as = 11.52e-14
               nrd = 0.01      nrs = 0.01}

Vsource_pset v1 (n3 0) {dc = 1.0}
Vsource_pset v2 (n7 0) {dc = 0}

Initialize (n6 = 1.0)
Initialize (n1 = 0)
Initialize (n2 = 1.0)
Initialize (n4 = 0)
Initialize (n5 = 1.0)
Plot "nmos90constdmm10.plt" (time() n1 n2 n4 n5 n6 i(MP1 n2 ) i(MN2 n5) i(MP3 n5))
}


Plot {
  eDensity  hDensity  eCurrent  hCurrent
  Potential  SpaceCharge  ElectricField
  eMobility  hMobility  eVelocity  hVelocity
  Doping  DonorConcentration   AcceptorConcentration
  ConductionBandEnergy ValenceBandEnergy
  AugerRecombination
  HeavyIonChargeDensity
}

Math {
   NoAutomaticCircuitContact
```

```
  WallClock
  Extrapolate
  Derivatives
  Newdiscretization
  RecBoxIntegr
  Method=ILS
  RelErrControl
  Spice_gmin=1e-15
  Iterations=20
  notdamped=100
}

# Initial Solution build-up

Solve {

Coupled (Iterations=100) {Poisson}
Coupled (Iterations=100) {Poisson Circuit}
Coupled (Iterations=100) {Poisson Contact Circuit}
Coupled (Iterations=100) {Poisson Hole Contact Circuit}
Coupled (Iterations=100) {Poisson Hole Electron Contact Circuit}

NewCurrentFile="transientconstdmm10"

Transient (
 InitialTime=0 FinalTime=1.99e-9 InitialStep=1e-12 MaxStep=1e-10
 Increment=1.3)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }

}
```

```
Transient (
 InitialTime=1.99e-9 FinalTime=2.1e-9 InitialStep=1e-13 MaxStep=1e-12
 Increment=1.3)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }
Plot  (FilePrefix="invconstdmm10"  Time=(2.0e-9;  2.01e-9;  2.02e-9;  2.035e-9;  2.05e-9;
2.07e-9; 2.09e-9) NoOverwrite)
}

Transient (
 InitialTime=2.1e-9 FinalTime=10e-9 InitialStep=1e-12 MaxStep=1e-10
 Increment=1.3)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }
Plot (FilePrefix="invconstdmm10_1" Time=(2.11e-9; 2.13e-9; 2.25e-9) NoOverwrite)
}
}
```

---X---