LOW FREQUENCY NOISE AND CHARGE TRAPPING IN MOSFETS

By

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CHAPTER I

INTRODUCTION

Spontaneous fluctuations (noise) underlie the most amazing and ubiquitous phenomena in both the physical and biological worlds. The observed random time record of noise can carry a large amount of information about a system and its interaction with the surrounding environment. Noise can limit the speed of information transfer and data manipulation; however, noise also can contain a treasure-chest of information about a particular system. Today's noise research covers the most important fields including biology, biomedicine, materials, magnetism, devices, reliability, circuits, optics, nonlinear systems, nanotechnology, classical and quantum information, quantum computing, communications, wireless, economic fluctuations, etc. In this work, we study the low frequency noise and fluctuation phenomena in semiconductor devices, and more specifically, the metal oxide semiconductor field effect transistor (MOSFET), which is the building block of modern ultralarge scale integration (ULSI) electronic circuits.

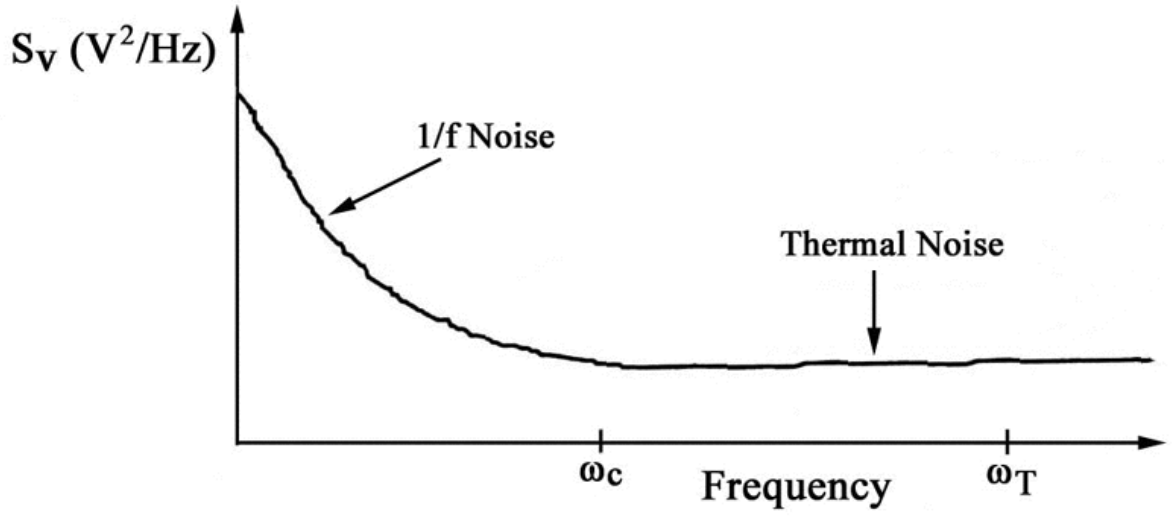

Figure 1: Schematic variation of S_V with frequency, showing the key characteristics of 1/f noise at low frequencies, and thermal noise at high frequencies.

If a constant voltage is applied to a semiconductor device, a resistor or vacuum tube, the current will exhibit fluctuations. The spectral density will show a constant value at high frequencies, due to thermal and shot noise components. However, at low frequency, f, usually below approximately a few kilohertz, the noise typically is found to be proportional to $1/f^{\alpha}$ (with α in the range 0.8-1.4). This kind of noise is frequently called low frequency noise, flicker noise, pink noise, or $1/f$ noise. Figure 1 shows a typical noise spectrum in a MOS transistor, in which the power spectral density S_V of the drain voltage is plotted as a function of frequency, emphasizing the dominance of $1/f$ noise at low frequencies and thermal (white) noise at higher frequencies. Low-frequency noise or flicker noise has been found in an astonishing variety of systems. The study of fluctuations and low frequency noise, especially in metals and semiconductor devices, has been an active area of research for decades [1]-[7]. The motivations behind the study of low-frequency noise in semiconductor devices are four-fold: (1) Low frequency noise is an important parameter for analog and RF applications. For example, low frequency noise in MOS devices can be up-converted to oscillator phase noise, degrading system performance [8], [9]. It gains increasing importance in view of, e.g., system-on-chip applications, especially for highly scaled mixed signal and analog applications. A comprehensive knowledge of all dominant noise-generating sources in the device is thus crucial to achieving an optimized noise performance of analog/RF circuits. (2) Despite decades of theoretical and experimental research work, the microscopic origins of $1/f$ noise are not well understood in most systems. (3) Extensive $1/f$ noise measurements have been done on MOS devices. Researchers have found that the variation of the $1/f$ noise of unirradiated transistors in the linear operation regime can correlate strongly with post-irradiation threshold voltage shifts due to oxide trap charge [10]-[14]. No direct link is found with interface traps at room temperature and frequencies below ~ 10

kHz [15]. In comparative studies with radiation effects, it has been shown that the 1/*f* noise of MOS transistors correlates strongly with the density of oxygen vacancies in SiO_2 [10]-[14]. The 1/*f* noise of nMOS devices generally increases with increasing oxide-trap charge during irradiation and decreases with decreasing oxide-trap charge during postirradiation annealing. These observations have made 1/*f* noise a promising tool as a nondestructive test of MOS failure in a radiation environment where oxide trap charge buildup is the dominant failure mode. Thus, 1/*f* noise can be used to help screen out devices that may not survive a radiation environment due to high oxide trap densities. This correlation also implies that the methods developed to reduce the amount of radiation-induced-charge trapping in MOS oxides could be applied to reduce the 1/*f* noise of MOS devices, which can otherwise limit the performance of some analog circuits and low frequency amplifiers. (4) Low frequency noise measurements can be used as a characterization tool for the quality or long-term reliability of MOS devices [16]-[18]. It is well documented in the literature that increased 1/*f* noise in MOSFETs can be associated with some major oxide degradation and reliability mechanisms, including dielectric leakage, gate oxide breakdown, hot-carrier effects and bias temperature instabilities [19]-[38].

A microelectronics technology of emerging commercial interest is silicon-on-insulator (SOI). SOI structures consist of a film of single crystalline Si separated by a layer of SiO_2 from the bulk substrate [39]-[41], thus electrically isolating the devices from the underlying silicon substrate and from each other. Historically, there have been three reasons for developing and using SOI. In earlier years, transient radiation hardness of SOI circuits was the main motivation for choosing these new substrates. Thin active Si films and the presence of the buried oxide greatly reduce the volume from which charges generated by ionizing radiation can be collected and minimize the impact of soft errors. Currently, performance enhancement motivates many

integrated circuit companies to use SOI wafers. The source and drain junction capacitance is almost entirely eliminated in SOI MOSFETs, while the capacitance through the thick buried oxide layer to the substrate is very small, so for the same supply voltage, digital logic circuits run faster in SOI than in bulk Si. Another advantage of SOI technology is the reduction or elimination of short channel effects [42], [43], especially for fully depleted SOI.

SOI devices are susceptible to total ionizing dose-induced charges that can be trapped in the buried oxide layer (BOX). Trapped positive charges may invert the back channel and create a leakage path at the island/BOX interface that severely degrades performance [44]. Hence, it is important and necessary to understand the charge trapping effects and radiation response of SOI buried oxides. One purpose of this work is to study the charge trapping effects and radiation response of SOI buried oxides using sub-threshold current-voltage, back-gate constant voltage stressing, and low frequency noise measurements. The majority of work in the literature on low frequency noise is on traditional bulk MOSFETs and/or the top gates of SOI devices, with only a limited number of studies reported on SOI buried oxides [45]-[48]. Hence, in this work we investigate these SOI-specific noise mechanisms, for example, back-channel noise and $1/f$ noise in the double-gate (both top and back gate turned on) modes of operation.

Many materials systems are currently being considered as potential replacements for SiO_2 as the gate dielectric material for sub-0.1 μm bulk and SOI CMOS technologies. Optimizing high-κ dielectrics for future generations of deep-submicrometer CMOS transistors remains a challenging field. Issues that remain to be solved are the stability of the threshold voltage and the significantly lower mobility compared with thermal SiO_2 gate devices. These are related closely to the high density of traps that are often found in the bulk or at the interface of a high-κ dielectric gate stack. The charging and discharging of these traps can greatly affect the operation

of the transistors. The effects of radiation in high-κ devices are only beginning to be understood [49]-[50]. Also, only a few reports are available in the literature on the low frequency noise of transistors with a high-κ gate dielectric stack [51]. So, in this case study, we also have investigated the low frequency noise and radiation response of MOS transistors with Al_2O_3/SiOxNy/Si(100) gate dielectrics.

This thesis is organized as follows. Chapter II introduces the basic mathematical background related to low frequency noise, the derivation of the Lorentzian spectrum for generation and recombination (GR) noise, and how $1/f$ noise can be constructed by the superposition of GR noise. Chapter III gives a brief overview of total dose radiation effects in microelectronic devices, followed by a description of the relationship between radiation effects and $1/f$ noise in MOSFETs. Increases in low frequency noise associated with long-term reliability degradation in previous studies are also discussed and compared to effects in irradiated devices. Chapter IV describes the experimental details for this project. Chapter V shows results on low frequency noise and radiation response of MOS transistors with Al_2O_3/SiOxNy/Si(100) gate dielectrics. Charge trapping effects and radiation effects in SOI buried oxides that have received silicon implantation are investigated in chapter VI. The charge trapping, radiation response, and bias instabilities of SOI MOSFET buried oxides are studied through low frequency noise and *DC* current voltage measurements. Also, the noise of fully-depleted SOI MOSFETs in double-gate mode operation and the back gate noise are investigated. Chapter VII provides the summary and conclusions of this work.

CHAPTER II

LOW FREQUENCY NOISE THEORY

This chapter contains background information about low frequency noise. A variety of models have been used to explain the $1/f$ noise in MOSFET devices. It has been generally accepted that the $1/f$ noise in the conduction channel of the device is associated with capture and emission of charge carriers from traps in the oxide, very near to the Si/SiO_2 interface. Before we discuss the details of the noise in microelectronics, we first discuss some general properties of low-frequency noise.

Mathematical Background

A continuous valued random variable X is completely specified by its probability density function (PDF)

$$f_X(x) \geq 0, \quad \int_{-\infty}^{\infty} f_X(x)dx = 1. \tag{2.1}$$

From the PDF one can calculate all the moments of the random variable. Among them the most important two for noise analysis are the mean

$$\overline{X} = \int_{-\infty}^{\infty} xf(x)dx, \tag{2.2}$$

and the mean square

$$\overline{X^2} = \int_{-\infty}^{\infty} x^2 f(x)dx. \tag{2.3}$$

The mean square is often interpreted as the average power of a signal X. The square root of this power (denoted as RMS) represents an equivalent constant signal with power equal to the average power of X. From the mean and mean square, we can calculate the variance of X

$$\sigma^2{}_X = \overline{X^2} - (\overline{X})^2, \tag{2.4}$$

which is interpreted as the square distance of X from its mean. When X has zero mean, its variance is equal to the mean square. Variance is often used to estimate the noise power.

A random process $X(t),\ -\infty \le t \le \infty$ is used to model a noise waveform. It is an infinite collection of random variables (noise samples) indexed by time t. For times $t_1, t_2 ....., t_n$, the samples $X(t_1), X(t_2), ..., X(t_n)$ are random variables. In noise analysis, it is often important to know the process mean $\overline{X}(t)$ and the autocorrelation function $R_X(t+\tau) = \overline{X(t+\tau)X(t)}$. Many important noise processes are modeled as stationary random processes, *i.e.*, processes with time invariant statistics. If both mean and autocorrelation function are time invariant, *i.e.*, $\overline{X}(t) = \mu$ and $R_X(t+\tau, t) = R_X(\tau)$, then $X(t)$ is a wide-sense stationary (WSS) process and its autocorrelation function has the following properties

- $R_X(0) = \overline{X^2(t)}$, which has the interpretation of average process power.
- $R_X(\tau)$ is an even function, which means $R_X(\tau) = R_X(-\tau)$.

In the time range $0 \le t \le T$, the Fourier Transform of $X(t)$ is

$$X(t) = \sum_{-\infty}^{\infty} \alpha_n \exp(j\omega_n t). \tag{2.5}$$

where $\alpha_n = \frac{1}{T}\int_0^T X(t)\exp(-j\omega_n t)dt$. The power spectral density of $X(t)$ is defined as

$$S_X(f) = \lim_{T\to\infty} \overline{2T\alpha_n \alpha_n^*}. \tag{2.6}$$

According to the Wiener-Khintchine theorem, the autocorrelation function and power spectral density function of a random variable $X(t)$ has the following relationship

$$S_X(f) = 2\int_{-\infty}^{\infty} R_X(\tau)\exp(-j2\pi f\tau)d\tau \tag{2.7}$$

$$R_X(\tau) = \int_0^{\infty} S_X(f)\cos 2\pi f\tau df \ . \tag{2.8}$$

When $\tau = 0$ in Eq. (2.8), we have

$$\overline{X^2(t)} = \int_0^{\infty} S_X(f)df. \tag{2.9}$$

The physical meaning of the power spectral density is the mean square of the random variable in the unit frequency bandwidth.

In noise analysis it is often required to estimate the mean and the autocorrelation function of a stationary noise process. There are two approaches to estimate them: the ensemble average and the time average. In the ensemble average approach, a large number of identical systems are constructed. They are measured simultaneously to extract the statistics in which we are interested. Although very powerful in theoretical noise analysis, this approach is not well suited for noise measurements. This is simply because a large number of identical systems are not available in practical experiments. Instead, the time average approach is often used to analyze experimental noise data, as long as the noise process is stationary. More detailed analysis can be found in [52]-[54].

Generation and Recombination Noise

In semiconductor materials or devices, generation-recombination (GR) noise is due to fluctuations in the number of free carriers inside of a two terminal semiconductor device sample associated with random transitions of charge carriers between states in different energy bands

[54], [55]. Typical examples of transitions are between conduction band and localized levels in the energy gap, conduction and valence bands, etc. Therefore, GR noise is inherently due to fluctuations of carrier number, usually keeping charge neutrality of the total sample.

As a simple model, assume there are N carriers in the device, with a generation rate $g(N)$ and recombination rate $r(N)$. The fluctuations in the numbers of carriers is described by a differential equation of the form

$$\frac{dN}{dt} = g(N) - r(N) + \Delta g(t) - \Delta r(t). \tag{2.10}$$

Here $N = N_0 + \Delta N$, where N_0 is equilibrium number of carriers. We now expand $g(N)$ and $r(N)$ in a Taylor series and neglect the higher order terms:

$$g(N) = g(N_0 + \Delta N) = g(N_0) + \frac{\partial g}{\partial N}\Big|_{N_0} \Delta N \tag{2.11}$$

$$r(N) = r(N_0 + \Delta N) = r(N_0) + \frac{\partial r}{\partial N}\Big|_{N_0} \Delta N. \tag{2.12}$$

Substituting these two equations into Eq. (2.10), we can simplify it into

$$\frac{d\Delta N}{dt} = -\frac{\Delta N(t)}{\tau} + H(t)\ , \tag{2.13}$$

with $g(N_0) = r(N_0)$. Here $H(t)$ is a random noise term and $H(t) = \Delta g(t) - \Delta r(t)$, and τ is defined as the lifetime of the carriers,

$$\frac{1}{\tau} = (\frac{dr}{dN} - \frac{dg}{dN})\Big|_{N_0}. \tag{2.14}$$

For $0 \le t \le T$ we can expand $H(t)$ and $\Delta N(t)$ in a Fourier series

$$H(t) = \sum_{n=-\infty}^{\infty} \alpha_n \exp(j\omega_n t) \tag{2.15}$$

$$\Delta N(t) = \sum_{n=-\infty}^{\infty} \beta_n \exp(j\omega_n t) \tag{2.16}$$

where $\omega_n = 2\pi m/T$ and n is an integer. Substituting Eq. (2.15) and (2.16) into Eq. (2.13) one finds

$$\beta_n = \frac{\alpha_n \tau}{1 + j\omega_n \tau} \ . \tag{2.17}$$

The power spectral density of $H(t)$ and $\Delta N(t)$ can be defined as

$$S_H(f) = \lim_{T\to\infty} \overline{2T\alpha_n \alpha_n^*} \tag{2.18}$$

$$S_{\Delta N}(f) = \lim_{T\to\infty} \overline{2T\beta_n \beta_n^*} \ . \tag{2.19}$$

Also since $H(t)$ is a white noise source, $S_H(f) = S_H(0)$. So from (2.17) to (2.19) we find

$$S_N(f) = \frac{S_H(0)\tau}{1 + \tau^2\omega^2} . \tag{2.20}$$

$$\overline{\Delta N^2} = \int_0^\infty S_N(f) df = \frac{S_H(0)\tau}{4} \tag{2.21}$$

Substituting (2.21) into (2.20), we can obtain the widely used expression for GR noise

$$S_N(f) = \overline{4\Delta N^2} \frac{\tau}{1 + \tau^2\omega^2} \tag{2.22}$$

The spectrum of the fluctuations in Eq. (2.22) is of a Lorentzian type with two parameters; that is, the variance of number fluctuations and the characteristic time of charge carriers. Figure 2 shows a typical noise curve of the current in a small device as a result of carrier interactions with a single trap center, which is of the Debye-Lorentzian spectrum shape. Figure 3 shows a discrete modulation of current level through a submicron MOSFET in the time domain [4]. This type of spectrum is called random-telegraph-signal (RTS) noise or popcorn noise. When the device is big enough, there usually are a large number of trapping centers with a distribution of characteristic times $g(\tau)$. Any spectrum may be generated by postulating an appropriate distribution of the characteristic times within the sample.

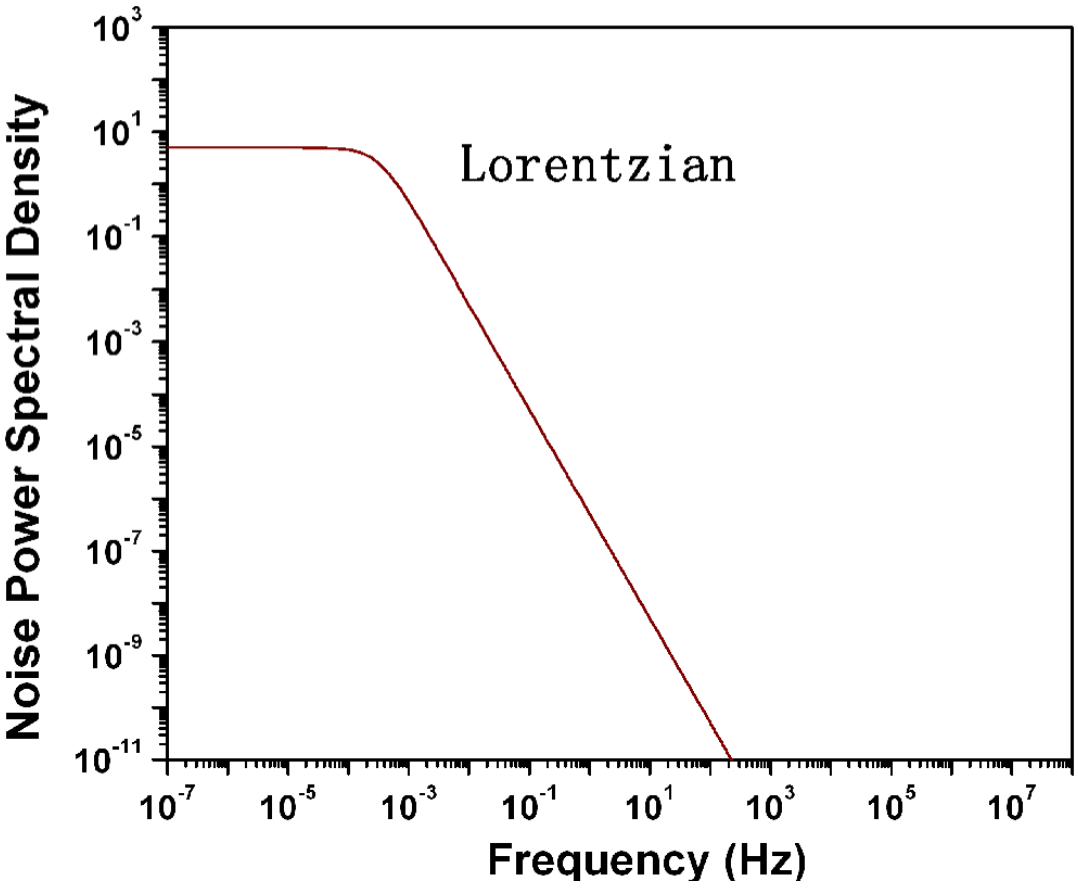

Figure 2: A typical Debye-Lorentzian spectrum

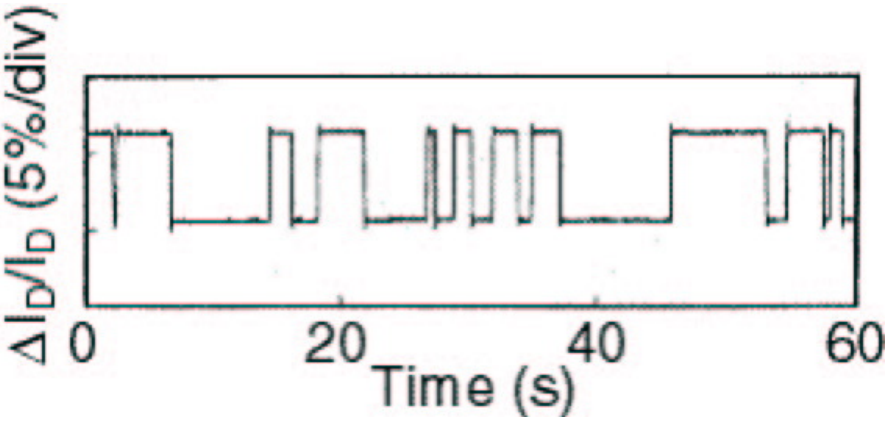

Figure 3: Typical RTS noise, showing discrete levels of channel current modulation due to the trapping and release of a single carrier [4].

Low Frequency Noise in MOSFETs

A superposition of a large number of Lorentzian spectra might result in a 1/*f* spectrum [54], [55]. To investigate this problem we rewrite instead of Eq. (2.22)

$$S_N(f) = \overline{4\Delta N^2} \int_0^\infty \frac{\tau g(\tau) d\tau}{1 + \tau^2 \omega^2} \tag{2.23}$$

where the probability $g(\tau)d\tau$ is normalized by requiring

$$\int_0^\infty g(\tau) d\tau = 1. \tag{2.24}$$

In the particular case that

$$g(\tau)d\tau = \frac{d\tau/\tau}{\ln(\tau_1/\tau_0)} \text{ for } \tau_0 \le \tau \le \tau_1 \tag{2.25}$$

and $g(\tau)d\tau = 0$ otherwise, so that $g(\tau)$ is normalized, one obtains

$$S_N(f) = \frac{2\overline{\Delta N^2}}{\pi f \ln(\tau_1/\tau_0)} [\tan^{-1}(\omega\tau_1) - \tan^{-1}(\omega\tau_0)], \tag{2.26}$$

which corresponds to

$$S_N(f) = \frac{4\overline{\Delta N^2}\tau_1}{\ln(\tau_1/\tau_0)} \quad \text{for} \quad \omega << \frac{1}{\tau_1} \tag{2.27a}$$

$$S_N(f) = \frac{\overline{\Delta N^2}}{f \ln(\tau_1/\tau_0)} \quad \text{for} \quad \frac{1}{\tau_1} << \omega << \frac{1}{\tau_0} \tag{2.27b}$$

$$S_N(f) = \frac{\overline{\Delta N^2}/\tau_0}{\pi^2 f^2 \ln(\tau_1/\tau_0)} \quad \text{for} \quad \omega >> \frac{1}{\tau_0}. \tag{2.27c}$$

We thus see that the spectrum is white at very low frequencies, goes as $1/f^2$ at very high frequencies, and varies as 1/*f* over a wide intermediate frequency range. A graphic representation of the discussion above is shown in Figure 4. In this figure, 11 Lorentzian spectra have been added, each with a time constant 10 times higher than the previous one. The resultant summation of the spectra gives a 1/*f* type spectrum.

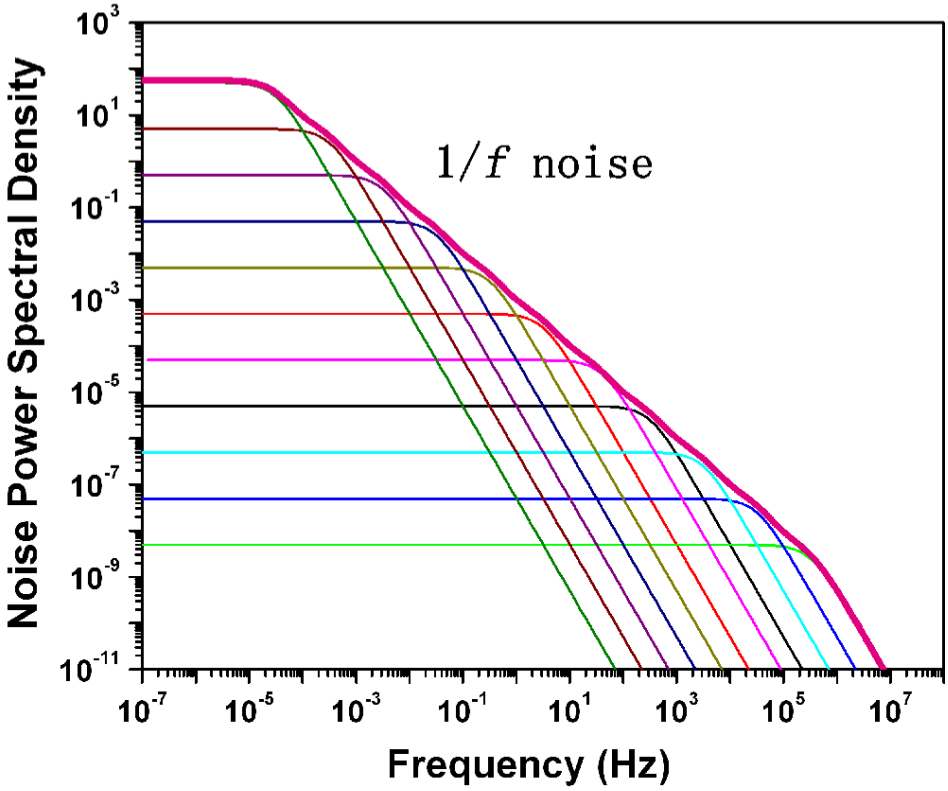

Figure 4: 1/f noise power spectral density can be obtained as a weighted summation of Lorentzians. Here ten Lorentzian spectra have been added, each with a characteristic time constant ten times higher than the previous one.

A variety of models have been proposed to explain 1/*f* noise in MOSFETs [56]-[65]. After much controversy, it is now widely accepted that the noise of MOSFETs is associated with capture and emission of charge carriers in the conducting channel from traps in the oxide, very near to the Si/SiO_2 interface. Fluctuations in oxide-trap charge couple to the channel, both directly through fluctuations in the numbers of inversion layer charges, and indirectly through fluctuations in scattering associated with changes in trap occupancy. Data from narrow-channel MOSFETs confirm that both effects can be important [4]. In general, noise studies on n-channel MOSFETs tend to follow a number fluctuation model, at least to first order. In p-channel devices, noise is often attributed to both number and mobility fluctuations [10].

In experiments we measure the noise power spectral density of the drain-source voltage. The n-type MOSFET device is usually operated in the linear region in strong inversion, and the number fluctuation model gives [10]:

$$S_{V_d}(f) = \frac{K}{f^{\gamma}} \frac{{V_d}^2}{(V_g - V_t)^2} \tag{2.28}$$

where K is a device-dependent noise level:

$$K = \frac{q^2 kTD_{bt} t_{ox}^2}{LW\varepsilon_{ox}^2 \ln(t_{\max}/t_{\min})} \tag{2.29}$$

CHAPTER III

LOW FREQUENCY NOISE, RADIATION EFFECTS, AND RELIABILITY

Total Dose Radiation Effects

Ionizing radiation is known to produce MOS component degradation and radiation damage in solid-state devices; this has been a major concern of space and military experts since the launch of the first Telstar satellite in the early 1960s. Radiation in the form of x-rays, energetic electrons, protons, and heavy ionized particles can significantly affect MOS devices. The sequence of events leading to ionizing radiation-induced damage is illustrated schematically in Figure 5 [66]. The primary effect directly related to the ionizing radiation is the generation of electron-hole pairs throughout the oxide. A percentage of the generated electrons and holes recombine immediately. The electric field in the oxide can separate the surviving carriers, accelerating electrons and holes in opposite directions. Electrons, which have a relatively high mobility in SiO_2, drift to the gate and are swept out of the oxide in a picosecond or less for irradiations at typical device operating conditions. Holes, on the other hand, transport much more slowly through SiO_2. Over a period of time the holes can migrate to the Si/SiO_2 interface under positive bias, where they either recombine with the electrons injected from the silicon, or fall into relatively deep trap states, forming a positive oxide-trap charge. Large concentrations of oxide-trap charge can shift the threshold voltage of MOS devices and increase the leakage current of an integrated circuit. Hydrogen ions can be released as holes travel through the oxide or when they are trapped near the Si/SiO_2 interface. The hydrogen ions can react with Si-H bonds at the Si/SiO_2 interface to form interface traps. These effects tend to change the threshold

voltage of the transistor, decrease the mobility, or even cause the complete failure of the IC. More detailed descriptions of the total dose irradiation process can be found in [66]-[68].

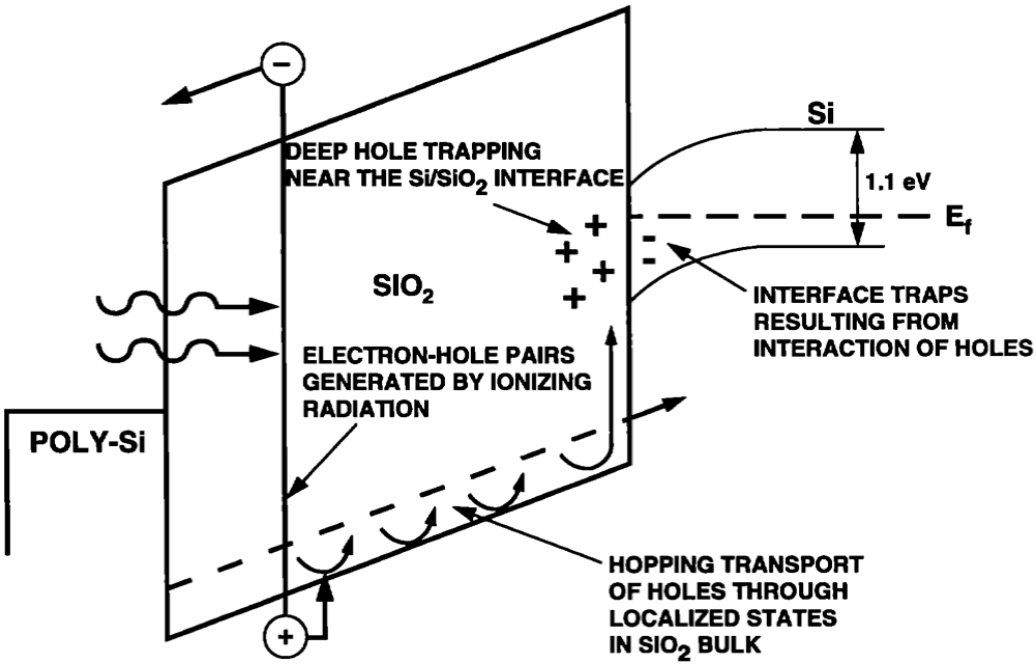

Figure 5: Band diagram of an nMOS device with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation. After [66].

We are particularly interested in the oxide trapped charge due to its close relationship with low frequency noise. A popular model of hole trapping and annealing was developed by Lelis *et al.*, through a dipole model [69]-[71], as illustrated in Figure 6 [72]. Basically, a weak Si-Si bond (oxygen vacancy) in Figure 6(a) captures a positive charge (hole), the Si-Si bond is broken and the lattice relaxes into a planar configuration and a tetrahedral configuration [73], as seen in Figure 6(b). Lenahan and Dressendorfer first established the correlation of E′ centers, and oxygen vacancies, with radiation-induced trapped holes [74]. Oxide trapped charge can undergo a long-term annealing process as a function of time, temperature, and applied electric field through either tunneling or thermally activated processes. The transition process between Figure

6(b) and 6(c) describes the switched bias annealing first reported by Schwank *et al.* [75], which involves a compensation process instead of true annealing. The true annealing is observed as the transition from Figure 6(c) to 6(a) when the positive and negative structures bond again.

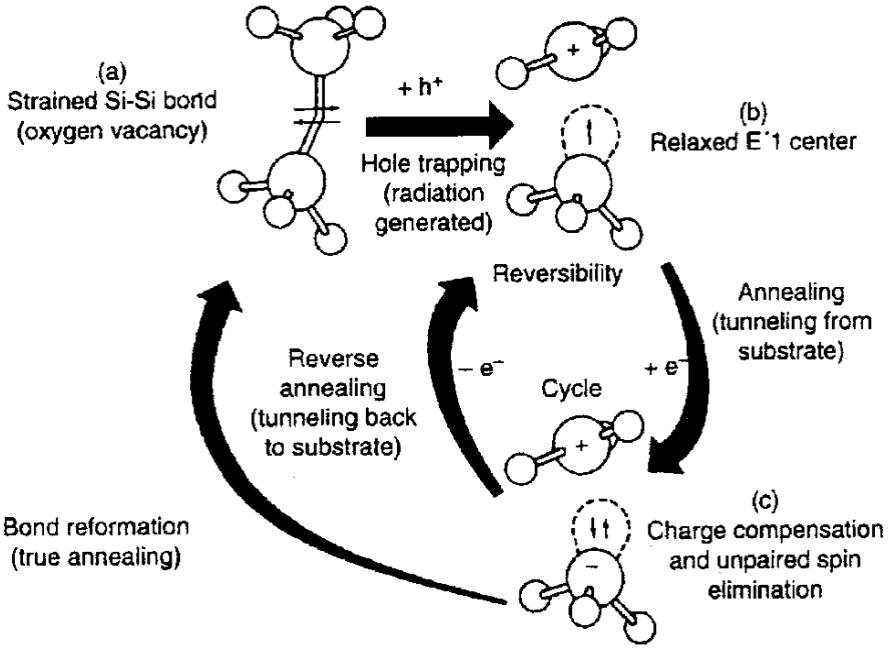

Figure 6: Model of hole trapping, permanent annealing, and compensation processes. After[72].

Radiation Effects and Low Frequency Noise

After irradiation, MOS device structures typically exhibit both an increase in the fixed charge density within the oxide and an increase in the interface trap concentration, resulting in a reduction of the transconductance and a change in the threshold voltage. Additionally, the low frequency noise generally increases [10]-[14], [76]-[78]. It has been found that the 1/*f* noise magnitude of unirradiated MOS transistors correlates with the radiation-induced-hole trapping efficiency of the oxide, suggesting the defect responsible for 1/*f* noise is linked to the E' center, or a direct precursor [15]. It was also found that 1/*f* noise has a strong correlation with oxide

trapped charge, but not usually with interface trap charge [10] [11], as shown in Figure 7, leading to the conclusion that oxide traps within a few nm of the Si-SiO_2 interface, defined as border traps, are responsible for 1/*f* noise in MOS devices [14]. Here $K = S_{V_d} f (V_g - V_{th})^2 V_d^{-2}$ is defined as the normalized excess 1/*f* noise. This normalization presumes that the 1/*f* noise is due primarily to carrier number fluctuations due to charge trapping and emission, a good assumption in this case, and most other noise experiments involving (especially n-channel) MOSFETs in the literature [10].

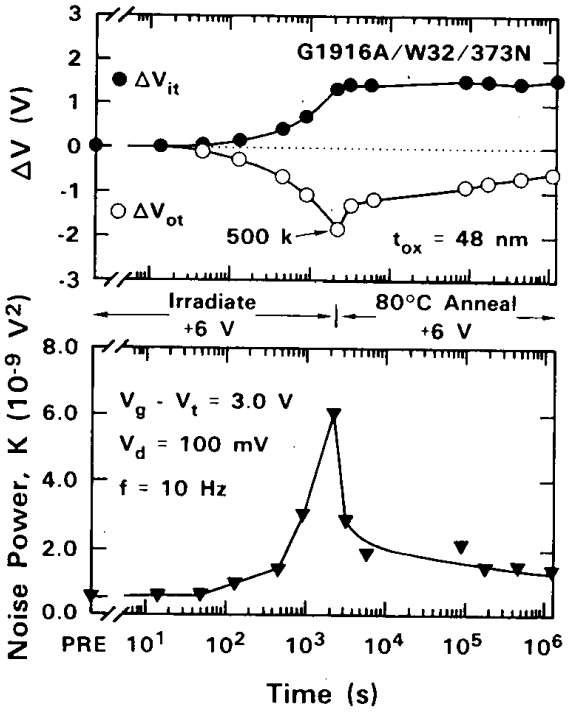

Figure 7: Top: threshold voltage shifts due to interface-trap charge (ΔVit) and oxide-trap charge (ΔVot) as functions of irradiation and annealing time for 3 μm long, 16 μm wide n-channel MOS transistors with ~ 50 nm oxides. Bottom: normalized noise power through the same irradiation and annealing. After [11].

Evidence from density-functional theory and 1/*f* noise measurements as a function of temperature and irradiation has suggested that the 1/*f* noise of n-channel MOS devices is caused

by the capture and emission of electrons at oxygen vacancy defects near the Si/SiO_2 interface [78], [79]. These processes likely are accompanied by significant SiO_2 network relaxation, and share a lot of similarities with the processes described in the dipole model discussed earlier in the chapter, involving a simple oxygen vacancy-related defect in SiO_2 that is either initially charged positively or neutral. In order for the trap centers to become a 1/*f* noise source, there should be a large number of traps available at suitable energy levels and/or locations. Border traps, located at suitable positions and energy levels, may lead to thermally activated trapping kinetics and account for the 1/*f* noise results [78], .

Dutta-Horn Model and Energy Distribution

The low frequency noise behavior of at least some n-channel MOS devices can be described quantitatively by the model of Dutta and Horn [1] [78], showing that 1/*f* noise of these devices is due to a random thermally-activated process having a broad distribution of energies relative to *kT*. The frequency and temperature dependence of the noise are related via

$$\alpha(\omega,T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S(\omega,T)}{\partial \ln T} - 1\right). \tag{3.1}$$

Here the frequency exponent is defined as $\alpha = -\frac{\partial \ln S}{\partial \ln f}$. The conditions for which Eq. (3.1) is valid [1] are:

1. The noise is due to random processes with thermally activated characteristic times.
2. The distribution of activation energies $D(E_0)$ varies slowly over any interval, $\Delta E \cong kT$.
3. The attempt frequency $f_0 = 1/\tau_0$ is much larger than the frequency at which the noise is measured.

4. The total noise magnitude $\overline{\delta V^2} \equiv \int_0^\infty S_V(f)df$ is independent of temperature.

It is also presumed that no new defects are created or existing defects annealed during the noise measurements. If Eq. (3.1) is satisfied for the noise of a particular system, this indicates that the noise is due to a thermally activated process with a distribution of activation energies, as opposed to an alternative process – e.g., tunneling [1]-[3]. This success of this model in describing the correlated temperature and frequency dependence of the noise in some MOS devices allows the energy distributions of the defects in these devices to be estimated from noise measurements as a function of temperature via

$$D(E_0) \propto \frac{\omega}{k_B T} S(\omega, T) \tag{3.2}$$

before and after irradiation, and after postirradiation annealing [78], as shown in Figure 8. The defect energy is related to the temperature and frequency through the simple expression $E_0 \approx -k_B T \ln(\omega\tau_0)$. In Figure 8, $S_V f / T$ at f = 1 Hz is plotted as a function of T (lower x-axis) and E_0 (upper x-axis). It is found that irradiating an nMOS transistor increases its 1/f noise and annealing decreases it. After annealing, the energy distribution of the defects changes from preirradiation values. Also we can infer the distribution of activation energies $D(E_0)$ from the temperature dependence of the noise magnitude. From Eq. (3.2) it is clear that the defect-energy distribution is proportional to $S_V f / T$, and that the defect energy can be parameterized as a function of temperature through the expression $E_0 \approx -k_B T \ln(\omega\tau_0)$ [1] [2] [79]. Before irradiation, there are peaks in the energy distribution at ~0.3 eV and ~ 0.6 eV. After irradiation, there is instead a peak at ~0.45 eV and a dip near 0.55 eV. After annealing, there are peaks at ~ 0.28 eV (although not as large as before irradiation), ~ 0.45 eV, and ~ 0.70 eV.

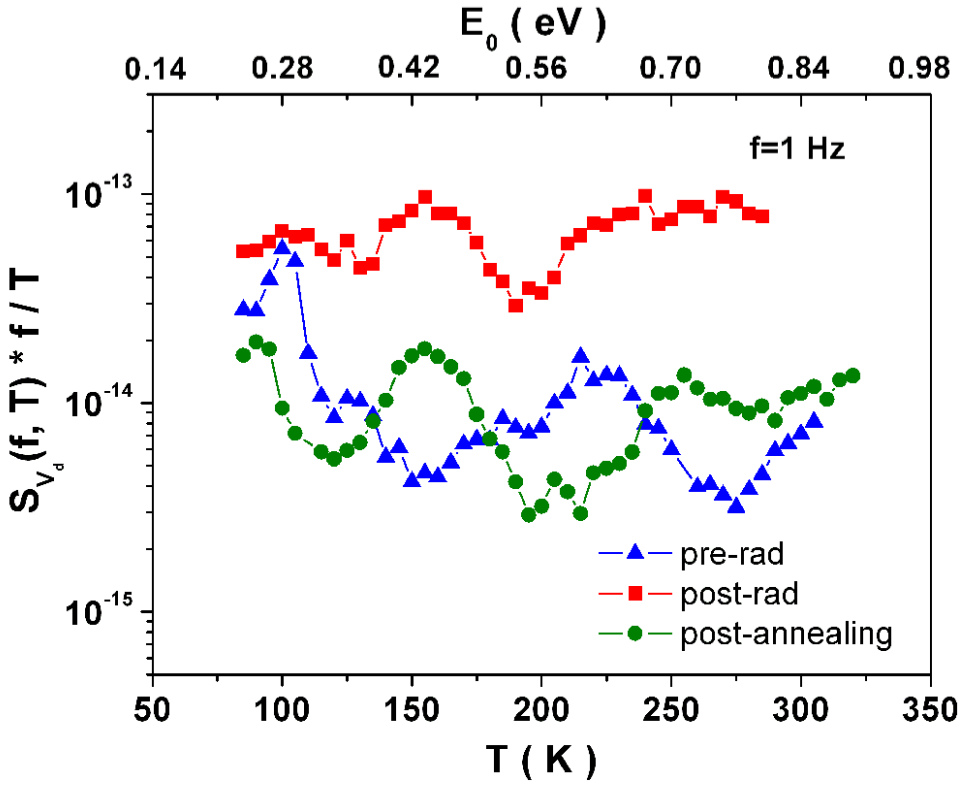

Figure 8: $S_V f / T$ as a function of T and E_0 for a 3 × 16 μm nMOS transistor with 32-nm oxides before irradiation, after 500-krad (SiO2) irradiation at 6-V bias, and after 24 h of 0-V annealing at 473 K. The energy scale inferred from the Dutta-Horn model is on the upper x-axis. After[78].

Low Frequency Noise in Long-term Reliability Studies

Not only has low-frequency noise been studied in the context of radiation effects, it also has been used extensively in the reliability study in MOSFETs for decades [16]-[18], mostly by studying the DC and noise characteristics degradation under high voltage stressing on the gate and/or drain. Stress-induced damage under channel hot-electron stress or Fowler-Nordheim stress can have similar effects to radiation-induced damage. The stress can cause an increase in the oxide-trap charge and an increase in the interface trap concentration. In most cases, a much stronger increase has been observed for low frequency noise compared with *DC* characteristics during device degradation. In this section, we will briefly discuss noise due to hot carrier

degradation, Fowler-Nordheim stressing, and thin gate oxide leakage and breakdown. The floating body-related noise overshoot is also covered for SOI devices. The sources of noise are also important for MOS device operation for long times in a radiation environment, and in some cases, may dominate over radiation-induced increases in noise.

Hot-carrier Effects/Fowler-Nordheim Stress

Hot-carrier effects (HCEs) and their consequences for transistor operation have been known and examined since the late 1970s [80]. HCEs lead to a gradual change in the drive current and threshold voltages, causing potential circuit failure. Extensive studies of the degradation of 1/*f* noise under various kinds of hot-carrier stresses [19]-[32] have been made and show that

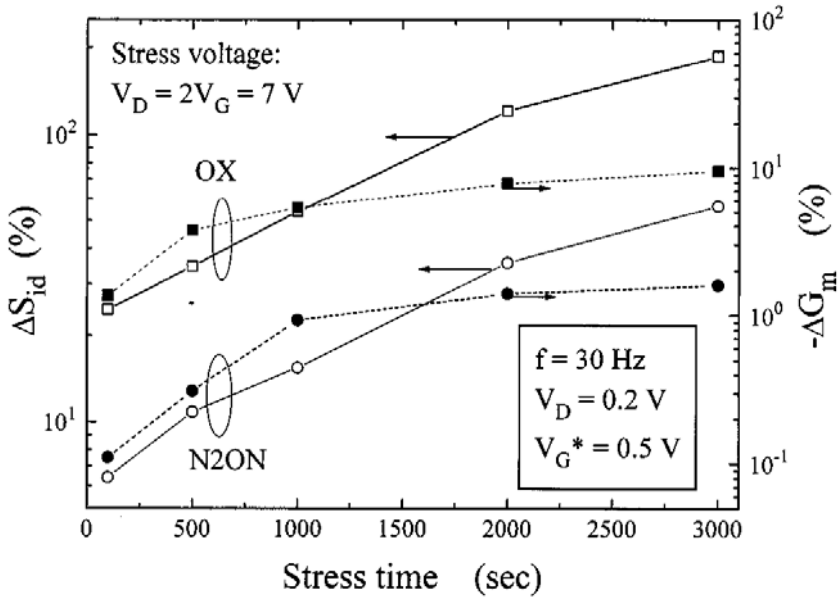

Figure 9: Degradation of drain-current noise power and peak linear transconductance under I_{Bmax} stress (V_D = $2V_G$=7 V) as a function of stress time on n-channel MOSFET. After [29].

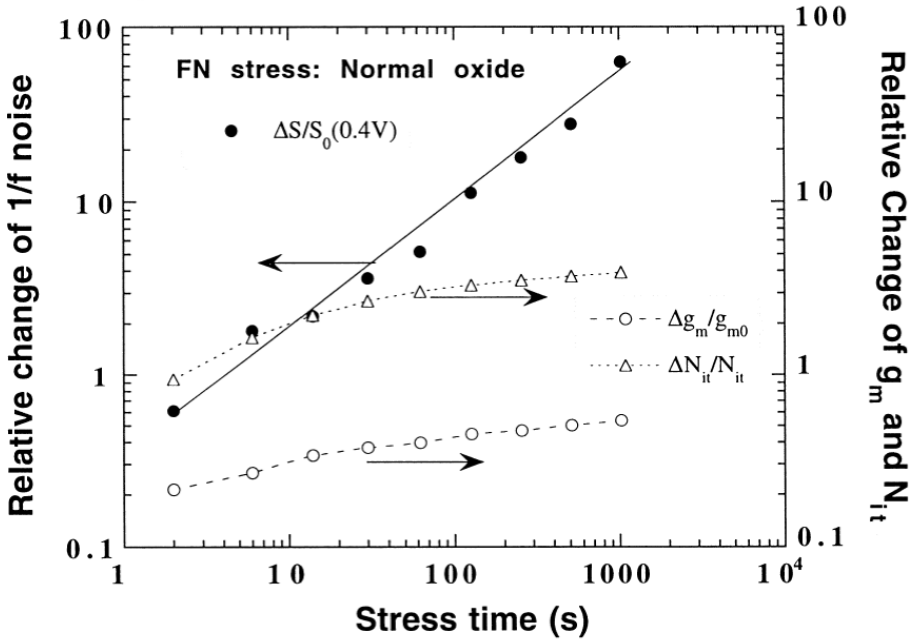

Figure 10: Time-Dependent degradation behavior of a n-type MOSFET upon FN stress. After [28].

a much stronger increase has typically been observed for the noise compared with the threshold voltage or transconductance degradation. As shown in Figure 9, the peak linear transconductance of the regular oxide sample has a 10% change while the drain current noise change is one to two orders of magnitude larger [29]. This emphasizes the higher sensitivity of 1/*f* noise to oxide traps/degradation induced by hot-carrier stressing.

A similar tendency was also found after Fowler-Nordheim stress [21] [28] [31] [32]. An example of relative 1/*f* noise and transconductance changes is shown in Figure 10 [28]. These are associated with oxide and interface traps created by the high-field stress in the oxide.

Dielectric Leakage and Gate Breakdown

Stress-induced leakage current (SILC), soft breakdown (SBD) and hard breakdown (HBD) are highly challenging reliability issues in thin gate oxide MOSFETs, especially when the

gate oxide thickness in submicron CMOS is below 5 nm. Noise in the quasi- or SBD regime of ultrathin oxides has drawn considerable attention [33]-[36]. Chen. *et al.* have characterized the low-frequency noise of 3.3-nm gate oxide nMOSFETs when the devices were subjected to a stress voltage of 5.5 V and encountered in the time evolution of SILC, SBD, and HBD [36], as presented in Figure 11. Figure 11 (a) depicts the gate current during stressing, showing the spontaneous changes at three critical points: the time to first SBD, the time to secondary SBD, and the time to HBD. Along with the sudden increase in gate current, it is found that the drain current noise power spectrum S_{id} (fresh) < S_{id} (SILC) < S_{id} (SBD) < S_{id} (HBD), as seen in Figure 11 (b). The SILC-induced noise increase is due to the increase in number of traps with the stress, until a critical number triggering soft breakdown occurs when the traps constitute a percolation path. The S_{id}(SBD) originates from current fluctuations in the SBD percolation paths, as demonstrated by the gate current fluctuation following each SBD event and the Lorentzian spectrum for S_{id}(SBD) manifested by the noise curve in Figure 11 (b). After HBD, the noise spectrum does not change much and is insensitive to subsequent stressing, indicating a complete conductive path.

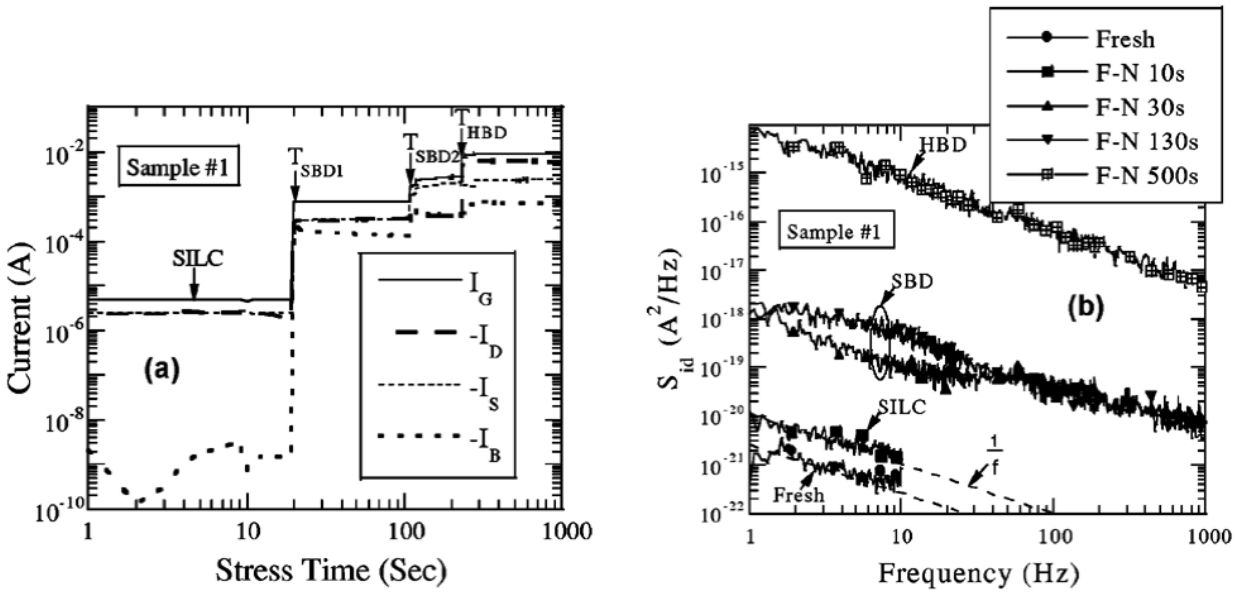

Figure 11: (a) Measured terminal currents versus stress time under constant voltage stressing. The constant voltage of V_G = 5.5 V is for Fowler-Nordheim (F-N) tunneling stress; (b) Measured drain current noise spectra (Sid) with V_D = 0.1 V and V_G = 1 V for several stress times. After [36].

Floating Body Related Noise Overshoot

In partially depleted SOI nMOSFETs, when the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs, due to impact ionization. The generated electrons move rapidly into the channel and the drain, while the holes, which are majority carriers, move to the floating body, increasing the body potential and forward biasing the drain-body diode. The body potential increase manifests itself in an increase of the drain current; this is called "kink effect", which is particularly important for partially depleted nMOSFET operated in saturation. It is well known that, along with the current-voltage kink, there is a strong increase in the low frequency noise [81]-[91], whereby the noise spectrum changes typically from 1/*f* noise to a Lorentzian shape.

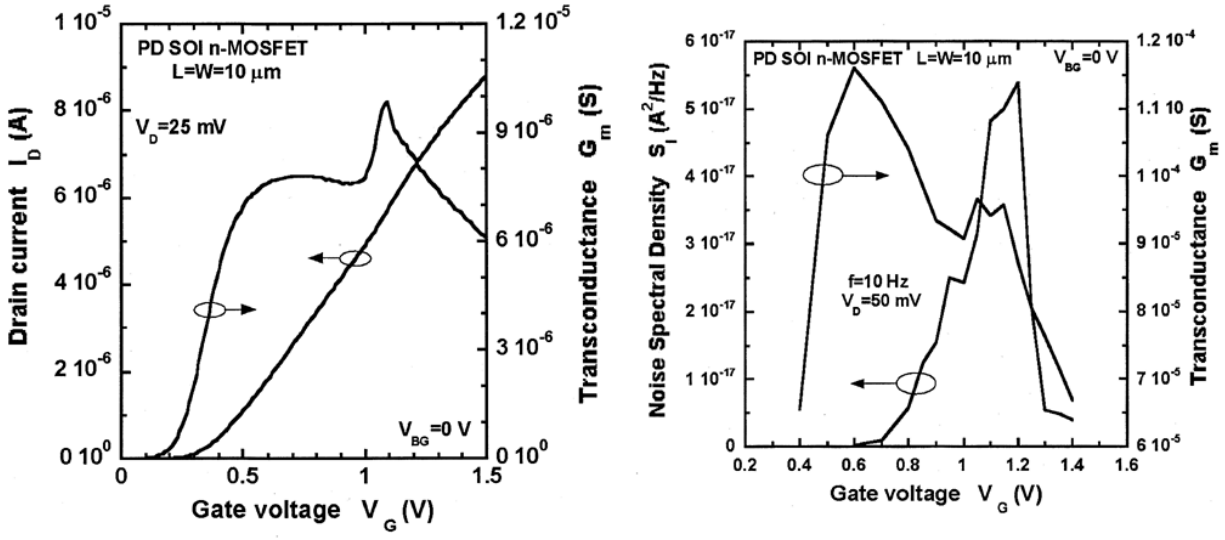

Figure 12: Linear kink effect (LKE) (a) and LKE related noise contribution to the drain current noise power spectral density (b) observed in partially (at V_{BG} = 0 V) depleted SOI n-MOSFETs. After [94].

In recent years, it has become clear that the use of an ultrathin gate dielectric in SOI MOSFETs gives rise to so-called gate-leakage induced floating body effects [93], which is a new class of floating body effects, which have a similar influence on device and analog/RF circuit operation as the classical impact-ionization related kink effect. It is found in partially depleted, fully depleted SOI devices with the back-gate biased into accumulation, and bulk MOSFETs at cryogenic temperatures [93]-[96]. Figure 12 shows that both the drain current and drain current noise show a strong increase at sufficiently large front-gate voltage. The main difference is that, for ultrathin gate oxides, electron valence-band (EVB) tunneling [93], [94], occurring for a sufficiently large front gate voltage, supplies the necessary majority carriers to forward bias the source-body junction and to induce a kink in the drain current. The main mechanism observed in this case can be simply interpreted as in the traditional kink-effect noise overshoot by considering the electrical field is vertical and the hole generation mechanism is related to valence band electron tunneling.

The results discussed in this chapter show that radiation exposure, high field stress, or other types of degradation mechanisms can increase MOS 1/*f* noise. Moreover, SOI devices can show responses that differ qualitatively from bulk MOSFETs. We now discuss work we have done to investigate the noise of advanced MOS structures – first for bulk devices with high-κ gate dielectrics in which large amounts of 1/*f* noise are associated with high defect levels, and then for SOI devices where back-gate noise and the noise of devices operated in double-gate mode are investigated.

CHAPTER IV

EXPERIMENTAL DETAILS

System Setup and Measurement Techniques

Excess noise measurements were performed on n-channel MOSFET transistors in strong inversion in the linear region using the apparatus diagrammed in Figure 13. Both the gate and drain were D.C. biased using a HP model 4140B constant voltage source/picoammeter. The substrate and the source terminals were grounded during the noise measurements. An 80 kΩ resistor was used in series with the transistor channel to limit the current and control the bias point. The drain to source voltage noise was amplified by a Stanford Research SR560 low noise preamplifier in the 1 Hz to 1 kHz frequency range. The preamplifier gain was set at 1000 since $\overline{v_{ds}}$ can be as low as 10 nV and the fluctuation of the drain-source voltage is sometimes too small to measure directly, so we use a low-noise preamplifier to amplify the noise signal before feeding it into the signal analyzer and oscilloscope. The low-pass filtering frequency of the preamplifier was set to 0.3 Hz. For a measurement bandwidth of 1 kHz, the high-pass filtering frequency of the preamplifier was set to around 10 kHz. The output of the preamplifier was connected to an oscilloscope and to a HP 3562A dynamic signal analyzer. The oscilloscope was used so that the noise could be observed in real time; the spectral analyzer can convert the time domain signal to power spectral density spectrum in the frequency domain, as described in more detail in [78], [97].

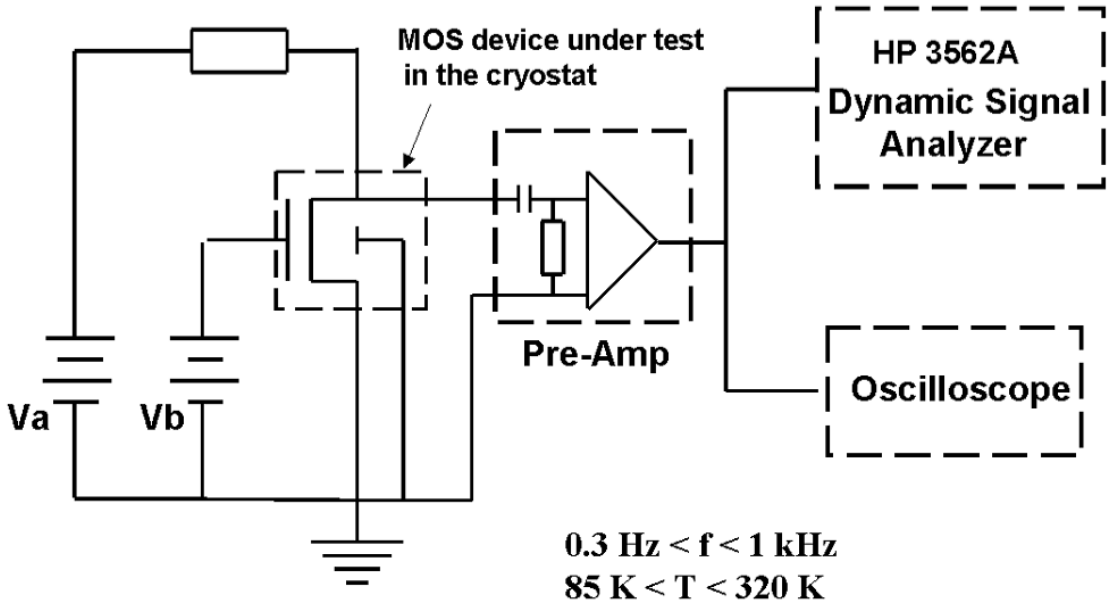

Figure 13: 1/f noise measuring circuit diagram

Aside from the noise contribution from the device under measurements, there are other noise sources from the equipment and its surroundings, such as the preamplifier, the voltage sources and the interference from the cables and the environment. In order to get an accurate measurement of 1/*f* noise from the MOSFET devices, we need to optimize the measurement circuit and suppress other noise sources in the system. We improved our noise measurement system in the following ways:

1. Noise spikes can be introduced by the power supply, and are located at the frequency of 60 Hz and its multiples. The 60 Hz pickup and its harmonics are hard to eliminate, but their effects can be reduced by operating some equipment such as the preamplifer in the battery mode. The spikes in the noise curves are ignored (via digital filtering) during the data analysis.
2. Grounding is one of the primary ways of minimizing unwanted noise and pick-up. First of all, safety considerations require the chassis of electric equipment to be grounded;

otherwise, the chassis may charge up due to stray impedances or insulation breakdown. Secondly, signal grounds, which may or may not be at Earth potential and are normally defined as equipotential points that serve as a reference potential for a circuit or system, should be connected together in order to prevent interference and intercoupling (i.e., ground loops). Examples of signal grounds in our measurement circuit are the source of the MOSFET device and the guards of all the BNC cables.

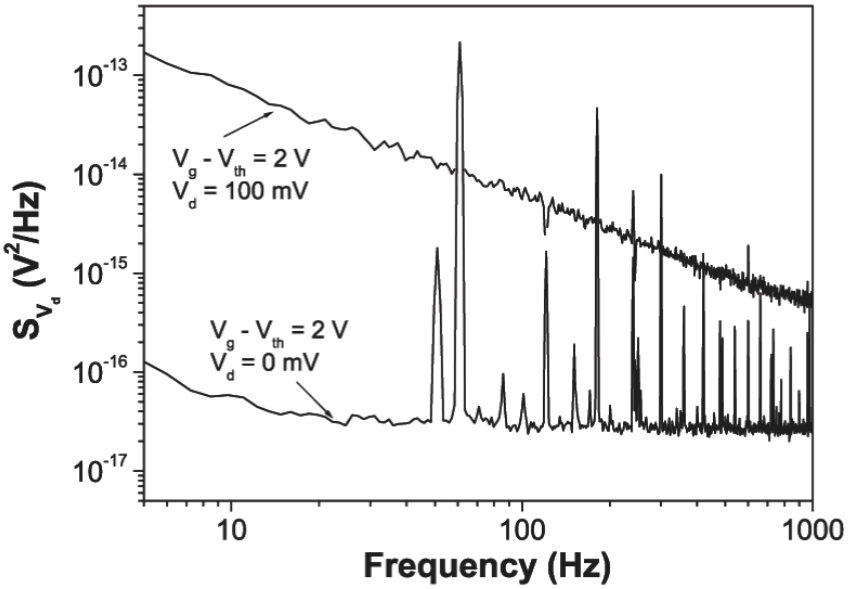

Figure 14: 1/f noise power spectral density for an unirradiated n-channel transistor with dimensions t_{OX} = 48 nm, L = 3.5 μm and W = 2.3 μm; the second trace is the background noise.

Figure 14 shows a plot of a typical 1/*f* noise spectrum for an unirradiated bulk n-channel transistor. The figure shows two separated traces with the drain to source bias at 0 V, which is the background noise, and 100 mV. These two traces show raw data. The background noise was subtracted from the curves before data analysis to calculate the noise parameters. The large "spikes" at 60 Hz and its multiples are caused by the power line fundamental and higher

harmonics, and noise data at these frequencies were excluded from noise curve fitting and subsequent analysis. All the noise measurements in this work were performed while operating the samples in the linear regime in strong inversion; i.e., the channel current varies linearly with the drain bias. In this regime, electrical and device properties, such as electrical field, channel carrier density, and depletion length, are roughly constant along the channel. Background noise measurements were made at each gate bias with zero channel current. The background noise is mostly composed of preamplifier noise and thermal noise. All the low frequency noise data in the thesis show noise spectra after background noise subtraction if not otherwise pointed out.

Irradiations were performed using an ARACOR Model 4100 10-keV X-ray irradiator. The choices of specific dose rate during irradiation did not significantly affect the results below.

Bias instability measurements were carried out using an HP 4156B semiconductor parameter analyzer for applying the bias stress and measuring the I-V characteristics. The cycle of the bias stressing and I-V measurements was automated so that the intervals between the stress and I-V measurements could be minimized. Charge detrapping is minimized as a result. The contribution of interface traps to the threshold voltage shifts is generally negligible since the subthreshold I-V characteristics show very little additional stretchout after stress [98], [99].

Current-voltage and low frequency noise measurements are automated in order to achieve higher efficiency and accuracy. There are a couple of reasons to computerize the measurements. First, the HP 3562A dynamic signal analyzer does not support data saving and printing, which prevents one from storing and further analyzing the data. Second, computerizing the systems, which involves programming instruments, enables remote-controlled measurements and automation in data acquisition, analysis, and visualization. Thirdly, during the stressing and current-voltage measurements, manual measurements cause long intervals between the stress and

subsequent *I-V* measurements and introduce inaccuracy. An example of the automation scripts is shown in the Appendix.

Devices

We investigated the total dose radiation response and low frequency noise of polycrystalline Si gate nMOS transistors with dielectric stacks consisting of an Al_2O_3 layer deposited on an interfacial oxynitride. These transistors were fabricated by IBM on n-type Si(100) wafers with a doping concentration of ~ 3×10^{17} cm^{-3}. The interfacial oxynitride films were thermally grown on HF-last Si(100) resulting in ~ 10-15% of N incorporation. The physical thickness of the Al_2O_3 was 20 nm, and the oxynitride layer was ~ 0.7 nm. After deposition, the Al_2O_3 was given a high temperature anneal at 1000^0C, resulting in κ ~ 11 [100]. The relative dielectric constant of the oxynitride used here is ~ 5. The equivalent oxide thickness (EOT) of the stacked dielectric of these films is ~ 8 nm.

We also studied three types of fully-depleted (FD), n-channel SOI devices that were processed in the same lot at Sandia National Laboratories, but with different types of buried oxide processing for the starting wafers. The cross-section of a typical device is plotted in Figure 15. The devices have 12 nm thick gate oxides, 110 nm thick Si film, 170 nm thick buried oxides, and have length L = 0.6 μm and width W = 2.3 μm. Below we will show irradiation and noise results from wafers A, B and C from this lot; wafer A did not receive any Si implantation during processing, while wafers B and C received special process treatments (two different types of Si implantation at an energy of 130 keV to high fluence levels [101]) to introduce electron traps into the buried insulator. The implant conditions used for wafer C were expected to result in more electron traps than for wafer B. For this implant energy, the Si implant peaks in the buried

oxide and creates electron traps deep within the oxide and near the Si channel/buried oxide interface. These transistors were made in a full, standard IC process that includes numerous high temperature oxidations and anneals.

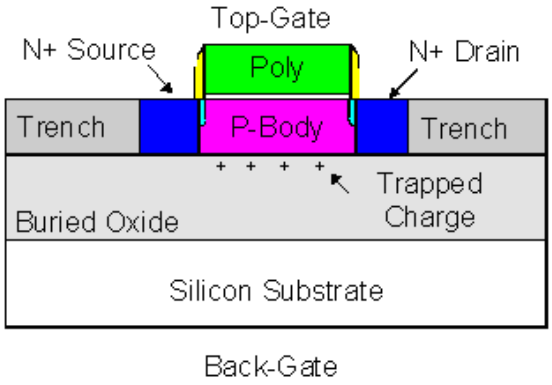

Figure 15: Cross-section of a n-channel SOI MOSFET illustrating a poly-Si top gate, thin gate oxide, Si body, buried oxide and Si substrate as back gate.

CHAPTER V

LOW FREQUENCY NOISE AND RADIATION EFFECTS IN MOS TRANSISTORS WITH $Al_2O_3/SiO_xN_y/Si(100)$ GATE DIELECTRICS

High gate (tunneling) leakage current and dielectric reliability issues may not permit the use of conventional SiO_2 for complementary metal-oxide-semiconductor (CMOS) devices below ~ 1 nm physical thickness [102]. Among alternative (high-κ) dielectrics under consideration as possible replacements for SiO_2, alumina (Al_2O_3) is a strong candidate for a relatively short-term solution to this dilemma [103]-[105]. Hence, the performance and reliability of devices having Al_2O_3 gate dielectrics is of extreme interest. Moreover, the radiation response of devices is also a concern for electronics that will be used in space electronics systems.

A key parameter that can affect the performance of analog and radio-frequency MOS devices is low-frequency excess noise [106], [107]. Moreover, low frequency noise measurements have also been used to characterize near-interfacial oxide (border) traps in transistors with thermal SiO_2 [10], [108], [109], oxynitrides [110], [111], and some kinds of high-κ dielectrics [51]. We now describe the total dose radiation response and low frequency noise of polycrystalline Si gate nMOS transistors with dielectric stacks consisting of an Al_2O_3 layer deposited on an interfacial oxynitride.

The transistors were characterized using subthreshold current-voltage (I-V) and low frequency noise measurements. The irradiations were performed at a dose rate of ~ 1000 rad(SiO_2)/s using an ARACOR 10-keV x-ray source. The transistors were irradiated incrementally to a total dose of 3.03 Mrad(SiO_2). The bias on the gate during the irradiation was 2 V, i.e., a positive static electric field of approximately 1.0 MV/cm, with all other pins

grounded. After irradiation, the devices were annealed at 200˚C with all pins grounded. All irradiations, and all I-V and noise measurements were performed at room temperature.

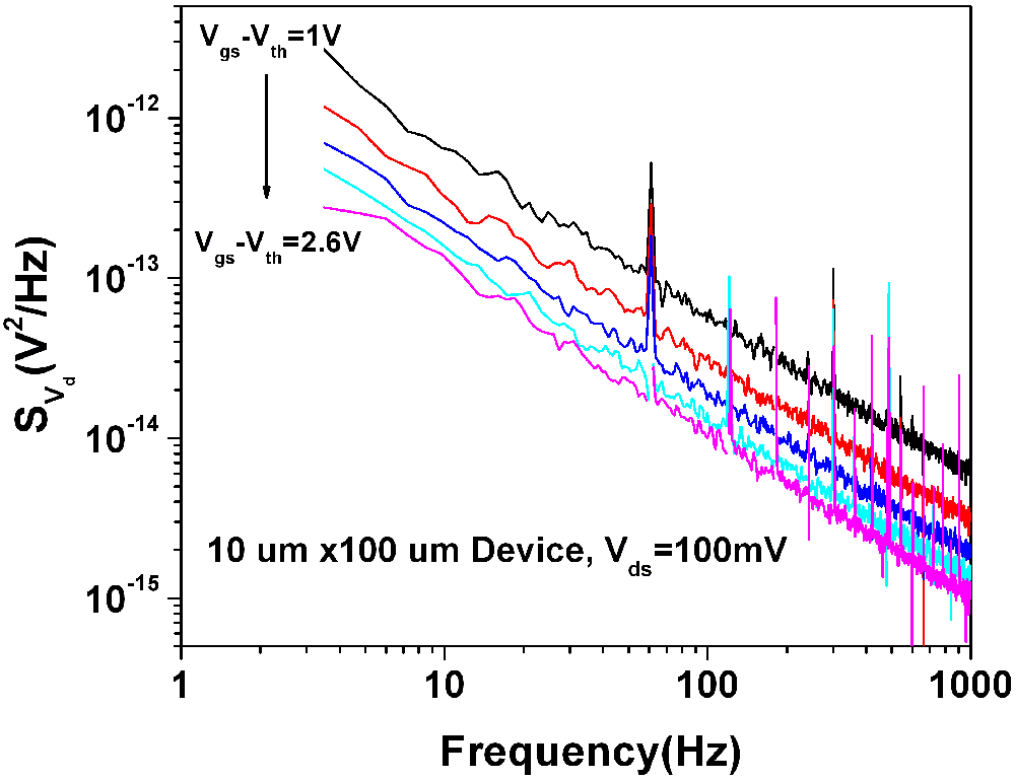

Figure 16: Pre-irradiation noise power spectral density for an unirradiated 10 μm x 100 μm transistor for V_{gs}-V_{th}=1, 1.4, 1.8, 2.2 and 2.6 V, while V_{ds} is maintained at a constant 100 mV.

The drain voltage-noise power spectral density was measured as a function of V_{ds} and V_{gs} in the linear region of transistor operation. Figure 16 shows a plot of S_{V_d} versus frequency for varying V_{gs} with a constant V_{ds} of 100 mV. The noise decreases with increasing V_{gs}. In Figure 17 the noise power S_{V_d} is plotted as a function of $V_{ds}^2/(V_{gs}-V_{th})^2$. The data can be described well by Eq. (2.28), as expected for noise due to number fluctuations [10].

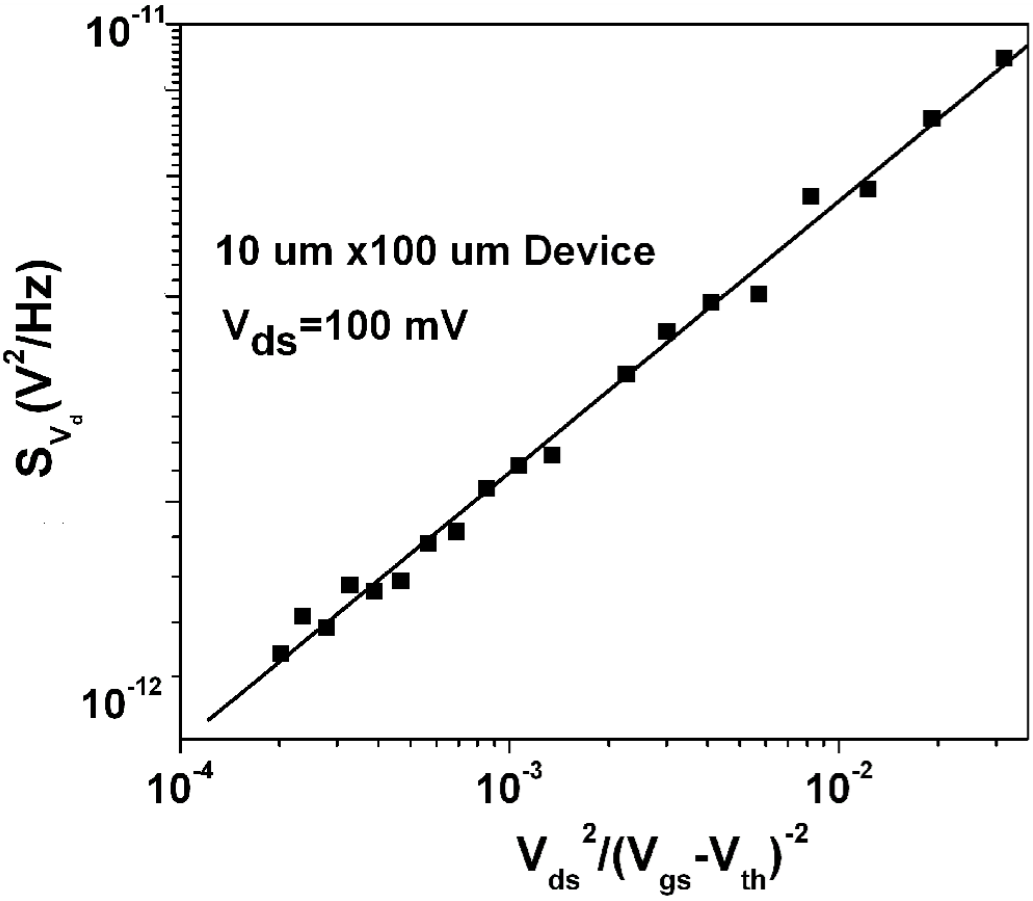

Figure 17: log-log plot of the noise power spectral density versus $V_{ds}^2/(V_{gs}-V_{th})^2$.

In all cases, the frequency exponent α was 1.0 ± 0.1. The normalized 1/*f* noise power, *K*, can be found from the slope of a linear fit to the data in Figure 17.

A semi-empirical expression has been developed to describe the correlation between the normalized noise power *K* and the density of border traps D_{bt}, as we rewrite Eq. (2.29) here: $K = \frac{q^2 kTD_{bt}t_{ox}^2}{LW\varepsilon_{ox}^2 \ln(t_{\max}/t_{\min})}$. This is only a rough estimate of the effective trap density owing to the large number of approximations made in common trapping models of the noise [14], [15], but it is useful for comparing the noise of different devices. Here $-q$ is the electronic charge; *k* is the

Boltzmann constant; T is the absolute temperature; t_{ox} is the oxide thickness; L is the channel length; W is the channel width; ε_{ox} is the dielectric constant of SiO_2; and $t_{\max}$ and $t_{\min}$ are the presumed "cutoff" times for the noise process [1], [2]. This expression was derived assuming that (1) defects with similar average, effective capture cross sections σ_t are responsible for both $1/f$ noise and radiation-induced-hole trapping, (2) the preirradiation noise S_V is proportional to the density of oxide traps, which is in turn proportional to f_{ot}/σ_t, (3) oxide traps near the Si/SiO_2 interface are distributed approximately uniformly in space and energy, and (4) carrier number fluctuations are the dominant cause of the noise.

Rearranging Eq. (2.29) we have

$$D_{bt} = (\frac{A}{q^2 kT}) \ln(\frac{\tau_1}{\tau_2})(\frac{\varepsilon_{OX}}{t_{OX}})^2 K . \tag{5.1}$$

It is possible to extract the density of border traps D_{bt} through low frequency noise measurements and compare the data from different devices. The device in Figure 17 has a normalized noise level K value of 3.4×10^{-11} V^2, corresponding to a border trap density of 2.8×10^{12} cm^{-2} eV^{-1}. It is interesting to note that the border trap density in the high-κ devices is more than an order of magnitude higher than is commonly seen in high quality thermal SiO_2, but not surprising as there is a lot of efforts now to improve the fabrication and manufacturing of the high-κ devices.

Figure 18 is a plot of the I-V characteristics of the device in Figure 16 as a function of irradiation dose and annealing. The I-V curves shift to the left with increasing dose, indicating a monotonic increase of net-positive oxide-trap charge in the gate insulator [98], [99]. Little change in I-V stretchout is observed, indicating that there is little increase in interface-trap density for these devices and irradiation conditions [49], [98], [99]. The curves shift back to the right after annealing, showing a decrease of net-positive oxide-trap charge. The increase in

leakage current with irradiation is associated with net positive oxide-trap charge buildup in the parasitic field oxide, and is not large enough to affect the noise measurements performed on these devices.

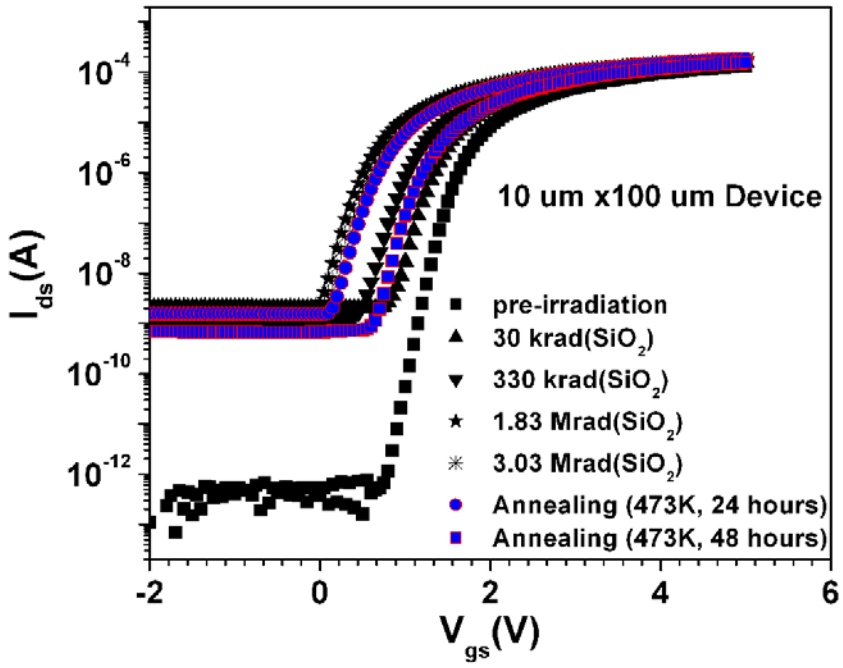

Figure 18: Drain current at 5 V drain bias as a function of gate voltage for the device of Figure 16 before and after X-ray irradiation up to 3 Mrad (SiO_2), and subsequent annealing at an electric field of 1 MV/cm. The enhanced leakage current after irradiation is likely due to radiation-induced trapped charge in the field isolation oxide.

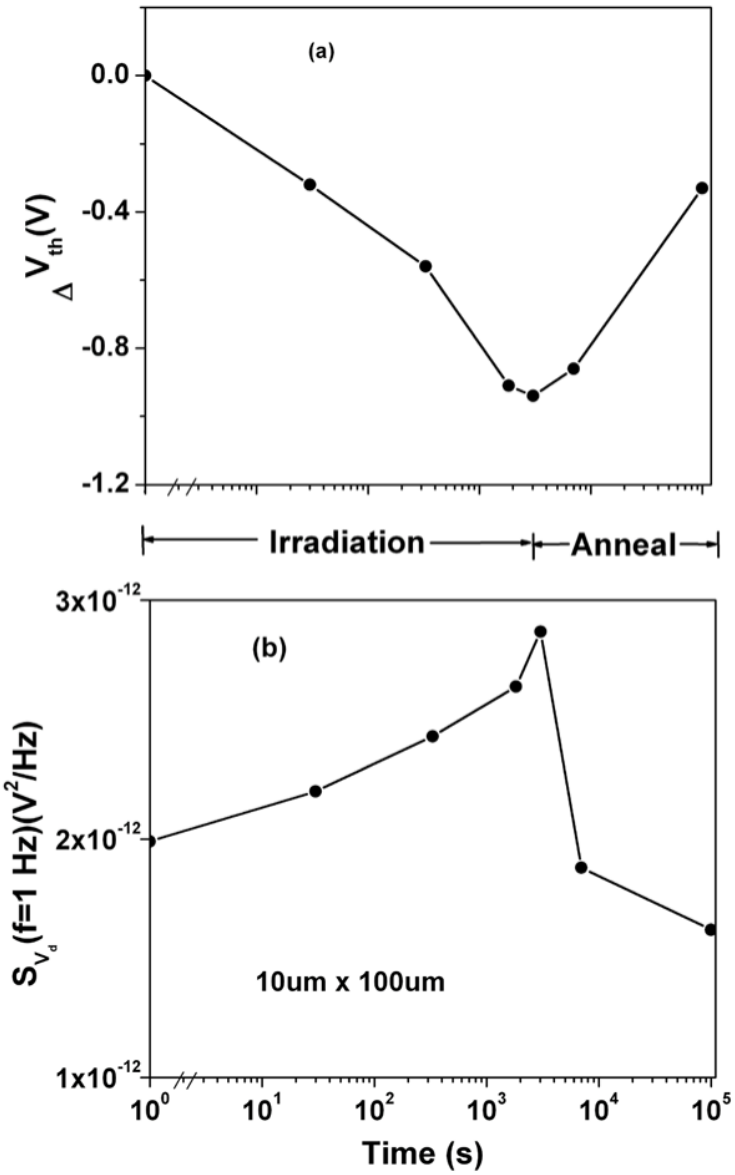

Figure 19: Top: threshold-voltage shifts as functions of irradiation and annealing time for a 10 μm x 100 μm n-channel MOS transistor. Bottom: Noise power spectral density at f = 1 Hz through the same irradiation and annealing sequence. V_{gs}-V_{th}=2 V, and V_{ds}=100 mV during the noise measurements. The radiation doses and annealing times are those used in Figure 18.

Figure 19 is a summary of the radiation-induced changes in V_{th} and the low-frequency noise during and after irradiation. Values of V_{gs} were adjusted as a function of irradiation conditions to ensure that V_{gs}-V_{th} remained constant at 2 V for all noise measurements. In order to better compare the trapped charge in Al_2O_3 films with SiO_2, we normalized the results of the

radiation response by estimating the effective charge-trapping efficiency of the oxide, f_{ot}, which is defined as the ratio of the net positive oxide-trap charge to the number of the electron-hole pairs (EHPs) created by ionizing radiation [10], [15], [49]:

$$f_{ot} = -\frac{\Delta V_{mg}\varepsilon_{OX}}{q\kappa_g f_y t_{eq} t_{phys} D}. \tag{5.2}$$

Here ΔV_{mg} is the midgap voltage shift, ε_{OX} is the dielectric constant of SiO_2, κ_g is the number of electron-hole pairs (EHPs) generated per unit dose, f_y is the charge yield, and D is the dose. Some assumptions about Al_2O_3 charge trapping properties are necessary to obtain first-order estimates of the effective hole trapping efficiency, which is a measure of the inherent defect density of the layer that is independent of thickness, bias, etc. For charge yield (f_y) we use 0.45, which is similar to the value for SiO_2 at the same electrical field [112], [113]. The κ_g used here is ~ 1.2 x 10^{13} $cm^{-3}rad^{-1}$ (SiO_2). This value is inferred from the known value of SiO_2 [15] scaled by the ratio of the band gap of SiO_2 to the band gap of Al_2O_3(~ 6 eV [114]). For a total dose of 330 krad(SiO_2), and with these assumptions, we estimate an effective trapping efficiency of ~ 40% for these devices and irradiation conditions, which is considerably higher than the net oxide charge-trapping efficiencies for radiation-hardened SiO_2 reported in the literature [74], [49], [115]. However, this value is comparable to the trapping efficiency of Hf silicate films measured by Felix et al. [49].

In SiO_2, a large hole trapping efficiency typically correlates strongly with large, preirradiation low-frequency noise. The response of these high-κ devices certainly is consistent with this trend. This suggests that low-frequency noise measurements may provide a sensitive, nondestructive probe of the radiation response of high-κ dielectrics. However, additional work on a broad range of materials will be required to establish whether this is true in general, or only

for some types of high-κ dielectrics. In any case, decreases in defect densities are required before high-κ dielectrics can be used effectively in MOS manufacturing. In the future, noise studies may help to identify processing conditions that minimize these defect densities.

CHAPTER VI

CHARGE TRAPPING AND LOW FREQUENCY NOISE IN SOI BURIED OXIDES

SOI structures impose an interesting challenge in terms of their low frequency noise. Besides the natural noise sources situated at the front Si/SiO_2 interface, other sources can also play an important role, including back-gate and sidewall insulators. A limited number of studies have been reported on the back-channel low frequency noise of SOI MOSFETs [45]-[48]. We measured the back-channel noise of devices from three types of wafers and estimated border trap density in the buried oxides using the normalized noise power values.

We also investigate the temperature dependence of the back-gate noise. We find strong evidence of thermally-activated charge exchange between the Si channel and defects in the near-interfacial buried oxide. In this study, the Dutta-Horn noise model does not always describe SOI back gate noise as well as it describes gate-oxide noise in many bulk MOS devices.

Silicon-on-Insulator (SOI) technologies have been developed for radiation-hardened applications and offer hardness advantages such as reduced transient radiation response and freedom from latch-up [44]. However, the thick buried oxide (BOX) imposes challenges for its use in total dose radiation environments due to the potential for radiation-induced charge trapping in the BOX [116], [117]. A method that has been proposed to reduce the net positive radiation-induced trapped charge in the BOX is ion implantation of SOI buried oxides with silicon [101], [118]-[121]. It has been reported that implantation of Al or Si at high dose into the buried oxide, and subsequent high temperature annealing, can create electron traps with a very large capture cross section which, when filled, compensate the trapped positive charge [118],

[119]. For example, Nicklaw *et al.* demonstrated the formation of Si nanocrystals in a buried oxide implanted with Si to a dose of $5 \times 10^{17}/cm^2$ and annealed at 1000°C [121]. In more recent work, Mrstik *et al.* showed the formation of Si clusters at the peak of the implant [120]. It has also been found that near-interface shallow electron traps are created by ion implantation, leading to large bias instabilities at the interface between the Si and the buried oxide [101]. Hence, the properties of buried oxides implanted with Si are of significant interest.

Comparative studies of low frequency 1/*f* noise and radiation effects can provide great insight into the characteristics and impact of defects in the gate oxide [10]-[14]. In this work, we also examine charge trapping effects in buried oxides by performing subthreshold current-voltage measurements and low frequency noise measurements on the back gates of irradiated and bias-stressed SOI devices. We find that SOI buried oxides implanted with Si ions show higher noise levels. Devices without Si implantation are found to exhibit greater increases in 1/*f* noise after irradiation than devices with Si implantation. Temperature dependence measurements show back-gate bias instabilities are caused by trapping and detrapping of electrons through a field-induced tunneling process.

An important aspect related to a fully depleted SOI MOSFET is the coupling effect between the front and the back gate, which makes the parameters of the front channel a function of the back-gate bias V_{BG}. Low frequency noise is also investigated in the double-gate mode of device operation in this work. It is found that operating the SOI devices in double-gate mode can help to reduce the low frequency noise.

Back Channel Noise

Back channel noise measurements were performed before and after irradiation. The excess drain voltage noise power spectral density (PSD) was measured with the devices operated in strong inversion in the linear regime. At this bias condition, the voltage PSD is described well by:

$$S_{V_d} = \frac{K}{f^{\alpha}} \frac{V_d^{\,2}}{(V_{bg} - V_{th(bg)})^2}, \tag{5.1}$$

assuming that the dominant cause of the 1/*f* noise is fluctuation in the number of channel carriers [78], [97]. In all cases, the frequency exponent α was 1.0 ± 0.2. The normalized 1/*f* noise power, *K*, can be found from the slope of a linear fit to the noise spectrum. This is used as a figure of merit to compare noise magnitudes for devices measured under different bias conditions.

Figure 20 shows typical 1/*f* noise spectra as a function of back gate bias for an unirradiated device from wafer B while the top gate is grounded together with the body and source. The figure shows seven separate traces with $(V_{bg} - V_{th(bg)})$ varying from 4 V to 22 V at intervals of 3 V. The background noise, which is the noise contribution from the measurement system and thermal noise of the device, also was measured by keeping the same $(V_{bg} - V_{th(bg)})$ and grounding all other pins, and subtracted from measurements at non-zero drain bias to calculate the excess (1/*f*) noise, S_{V_d}. As expected, the noise magnitude decreased with increasing back gate bias.

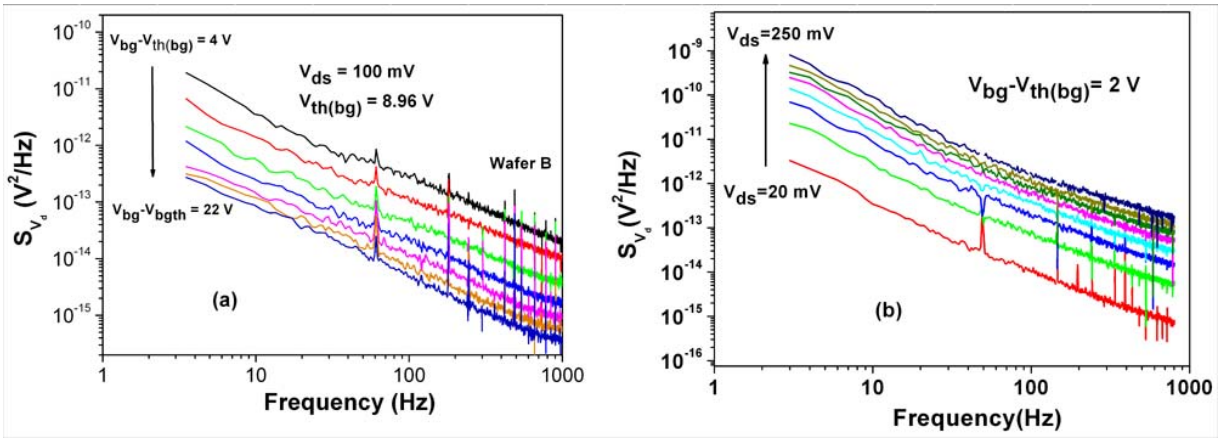

Figure 20: 1/f noise spectra, S_{V_d}, for an unirradiated n-channel SOI transistor from wafer B, with dimensions t_{OX} (gate oxide thickenss) = 12 nm, t_{BOX} (buried oxide thickness) = 170 nm, L =0.6 μm, W = 2.3 μm, (a) as a function of back gate bias while the drain bias is constant. Values of $V_{bg} - V_{th(bg)}$ are 4, 7, 10, 13, 16, 19, and 22 V, respectively; (b) as a function of drain bias while the back gate bias is constant. Values of V_{ds} are 20, 50, 80, 110, 140, 170, 200, 250 mV, respectively. The spikes are the result of 60-Hz pickup and are ignored in the fitting and analysis of the data.

The noise magnitude as a function of the drain bias was also tested while the back gate bias was kept constant; as expected, the noise increases as $V_{ds}^{\ 2}$. In Figure 21, the noise magnitude at $f = 1Hz$ is plotted as a function of $V_{ds}^{\ 2}/(V_{bg} - V_{th(bg)})^{-2}$. The linear response (to within experimental error) agrees well with one's expectations from Eq. (5.1), consistent with a simple number fluctuation model [12], [78], [122]. It also demonstrates we have strong enough coupling to the back channel to permit reliable noise measurements to be performed on these fully depleted devices.

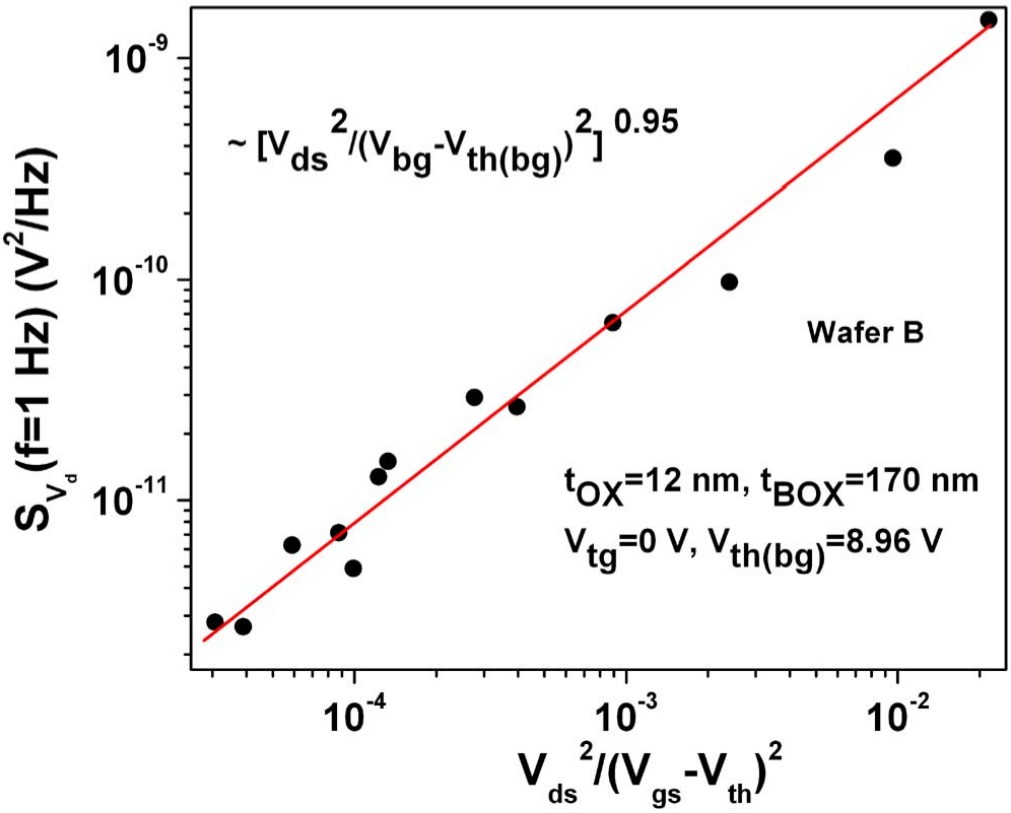

Figure 21: 1/f noise power spectral density S_{V_d} *of the device in Figure 20 at* $f = 1Hz$ *as a function of* $V_{ds}^{\ 2}/(V_{bg} - V_{bg-th})^{-2}$. *The device has dimensions* t_{OX} *(gate oxide thickenss) = 12 nm,* t_{BOX} *(buried oxide thickness) = 170 nm, L =0.6* μ*m, W = 2.3* μ*m.*

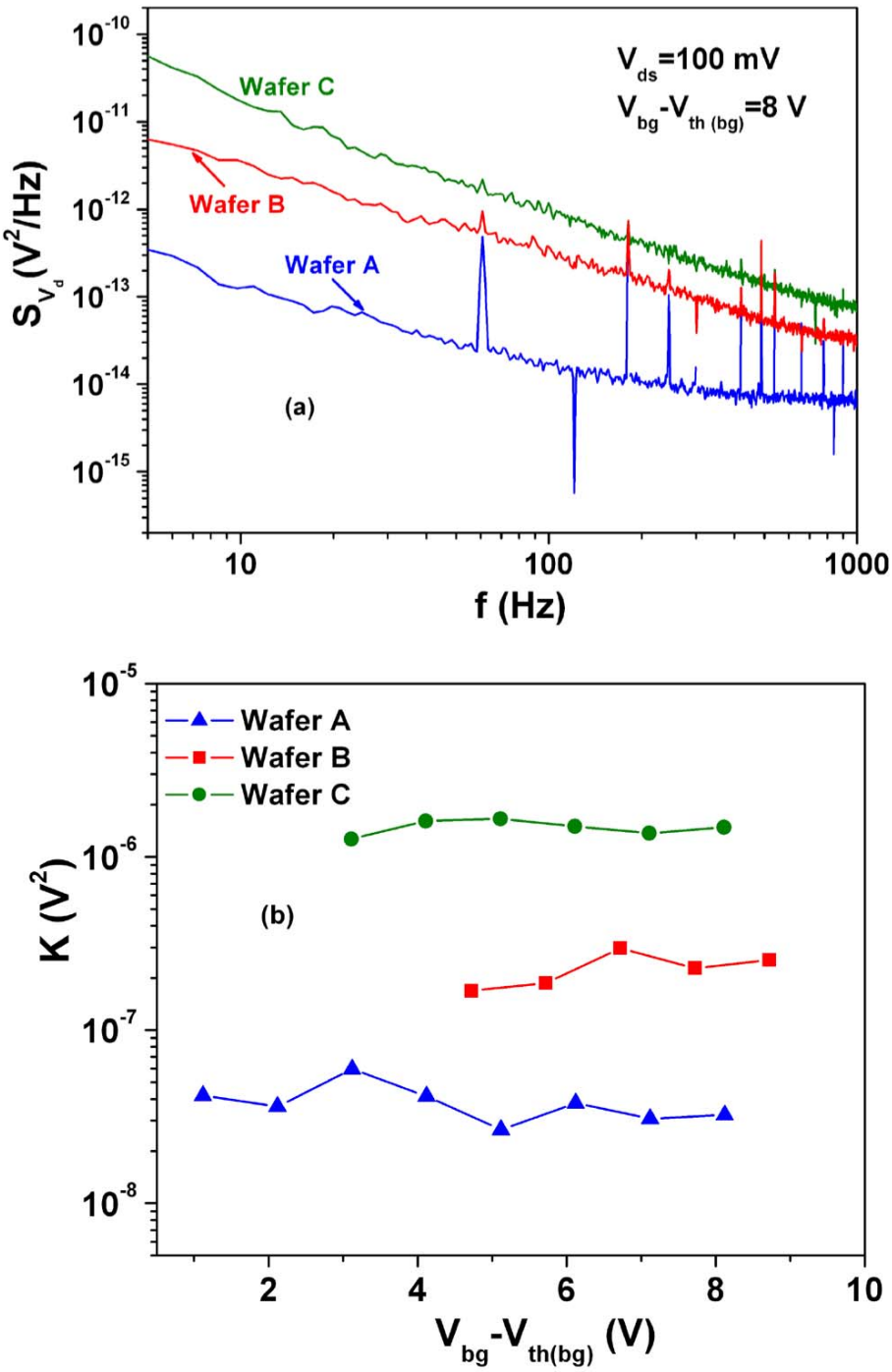

Figure 22: (a) Back-gate noise spectra of SOI devices from wafers A, B, and C in the linear regimes in strong inversion with V_{ds}=100 mV and V_{bg}-$V_{th(bg)}$ = 8 V. The front gate was grounded during the back gate noise measurement. (b) Variation of normalized drain voltage noise power K versus $(V_{bg}-V_{th(bg)})^2$ for devices from wafer A, B, and C. The devices have dimensions t_{OX} (gate oxide thickenss) = 12 nm, t_{BOX} (buried oxide thickness) = 170 nm, L =0.6 μm, W = 2.3 μm.

Figure 22(a) shows the drain voltage noise PSD comparison for a set of devices from wafers A, B, and C as a function of frequency at the same drain bias and effective back-gate bias $V_{bg} - V_{th(bg)}$ = 8 V. For each noise spectrum, the normalized noise power K was acquired by linearly fitting the measured spectrum between 10 and 200 Hz, after correcting for background and zero current noise. Figure 22(b) shows the pre-irradiation back-gate normalized noise power for devices from wafers A, B, and C at V_{ds} = 100 mV. The device from wafer A has the lowest back-gate noise magnitude, while the one from wafer C has the largest back-gate noise. This increase in back-gate noise likely is associated with O vacancy-related defects, as often found for MOS noise [79], [123]-[125]. It is not surprising that Si implantation would increase the density of these kinds of defects.

Front channels and back channel low frequency noise measurements were performed on devices from wafer A, B, and C and were used to calculate border trap density using Eq. (5.1). The front channel noise levels for devices from three different wafers are comparable to each other, indicating that the density of border traps at the front gate oxide is independent of the buried oxide processing conditions. From data obtained by other analytical techniques, like charge pumping or the subthreshold slope method, one expects the back-interface to be more defective, and therefore to be more noisy [128], [129]. However, this is not always observed [47], [48]. The border trap density of the front gate oxide and buried oxide for the control device from wafer A in this study also shows comparable values, as seen in Table 1.

Table 1 also shows that the border trap density in the buried oxide of wafer C is ~ 1.7×10^{12} cm^{-2} eV^{-1}, much larger than is commonly seen in gate SiO_2, while wafer A buried oxide border trap density is estimated at ~1.67×10^{10} cm^{-2} eV^{-1}, indicating that silicon implantation causes a higher oxygen vacancy density.

Table 1: Summary of room-temperature noise data for different devices along with estimated border trap density data. Shown are equivalent oxide thickness (EOT), gate length (L) and width (W), normalized noise level (K), and estimated border trap density (D_{bt}).

Device	EOT (nm)	L x W $(\mu m)^2$	K (V^2)	D_{bt} $(cm^{-2}\ eV^{-1})$
SOI Wafer A Back Gate	170	0.6 x2.3	7×10^{-8}	1.67×10^{10}
SOI Wafer B Back Gate	170	0.6 x2.3	3×10^{-7}	7.2×10^{10}
SOI Wafer C Back Gate	170	0.6 x2.3	7×10^{-6}	1.7×10^{12}
SOI device Front Gate	12	0.6 x2.3	4×10^{-10}	1.9×10^{10}

Low Frequency Noise in Double-gate Mode

SOI devices can also be operated in double-gate (DG) mode, in which the front and back gates of a FD transistor are simultaneously biased to form front and back inversion channels [130]-[132]. Figure 23 shows the noise PSD as a function of frequency at different back gate biases ranging from –10 V to +20 V. The front inversion channel was formed at V_{fg} = 4 V and V_{th} (front gate) = 1.1 V. The front-gate bias and the drain bias were kept constant during the noise measurements. The noise level decreases with increasing back-gate bias from –10 V to +20 V, suggesting lower 1/*f* noise in the DG mode of operation. Qualitatively similar trends are also seen in UNIBOND SOI devices with thinner silicon films, as shown in Figure 24, as well as in short-channel SOI devices with thin silicon films [133].

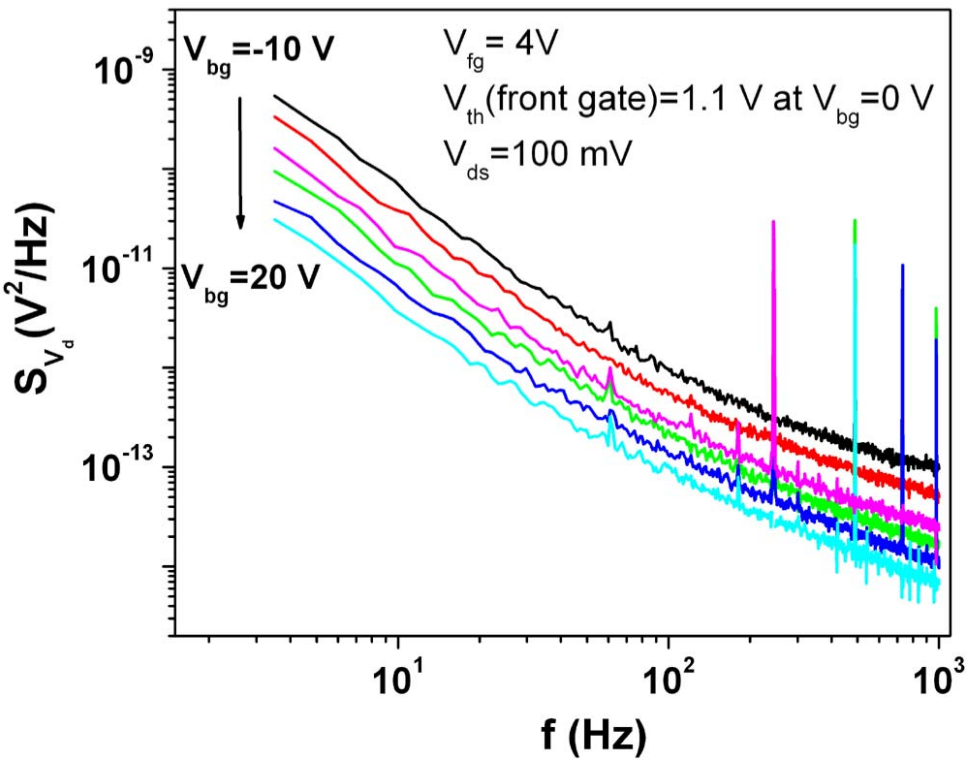

Figure 23: Log-log plots of the low frequency noise PSD of a wafer C device as a function of back-gate bias (V_{bg}= –10, 0, 5, 10, 15, 20 V respectively), while the front-gate bias and drain biases were kept constant (V_{fg}= 4 V and V_{ds}= 100 mV). The device has dimensions t_{OX} (gate oxide thickenss) = 12 nm, t_{BOX} (buried oxide thickness) = 170 nm, L =0.6 μm, W = 2.3 μm.

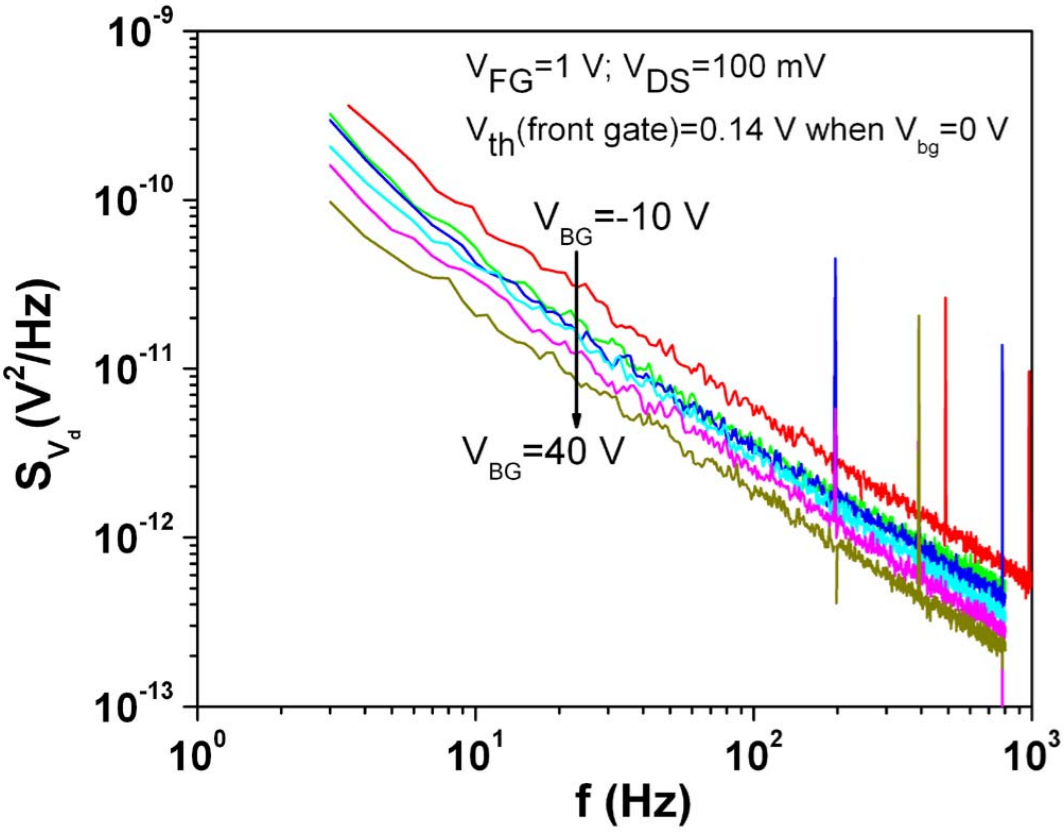

Figure 24: Log-log plots of the low frequency noise PSD of a UNIBOND device as a function of back-gate bias (V_{bg}= –10, 0, 10, 20, 30, 40 V respectively), while the front-gate bias and drain biases were kept constant (V_{fg}= 1 V and V_{ds}= 100 mV). The device has dimensions t_{OX} (gate oxide thickenss) = 4.5 nm, t_{BOX} (buried oxide thickness) = 400 nm, L =0.8 μm, W = 40 μm.

It is worth noting that the transistors in this study have relatively *thick* silicon films and two well-defined channels form when the positive bias on each gate is sufficiently large [135]. As the back-gate bias changes from –10 V to 20 V, the front-gate threshold voltage is reduced, as expected [136]. The increase of ($V_{fg} - V_{th(fg)}$) causes the noise to decrease, consistent with the results on bulk MOSFETs [12]. In the DG mode of operation of SOI devices with ultrathin Si films (a few nanometers), the minority carriers flow in the middle of the film and experience less surface scattering. Hence the mobility, transconductance, and drive current are considerably improved [130]-[132]. Because noise is caused by the interaction between the channel carriers and near-interface oxide traps, it might be expected that the 1/*f* noise should also be improved in

ultrathin SOI devices. In any event, the 1/*f* noise in double-gate SOI MOSFETs is improved compared with their single-gate counterparts, regardless of the Si film thickness. This may help mitigate the increased noise associated with electron traps in the BOX in advanced FD SOI technologies.

Radiation Effects

As is the case with gate and field oxides, the radiation response of buried oxides has been found to be highly dependent on the fabrication process [138], [139]. Two common methods for fabrication SOI substrates are separation by implanted oxygen (SIMOX) and wafer bonding. Both wafer technologies requires high temperature anneals. It is well known that high temperature anneals cause oxygen to out-diffuse from the buried oxide, leaving behind numerous oxide defects [115], [134]. These defects can lead to enhanced radiation-induced charge trapping. On the other hand, one technique has been proposed to reduce the amount of net radiation-induced positive trapped charge in the buried oxides by implanting the BOX with silicon [118]-[120]. Devices from three different wafers were irradiated to 1 Mrad(SiO_2) at a dose rate of 32 krad(SiO_2)/min. Figure 25 shows the I-V characteristics for back-gate transistors from wafer A, B, and C irradiated to 1 Mrad(SiO_2). During the back gate I-V measurements, the front gate was grounded. The transistors were irradiated with X-rays with all the pins grounded. As shown in Figure 25, positive charge buildup in the buried oxides causes large negative shifts in the back-gate transistor I-V curves. As the radiation dose increases, the trapped charge in the buried oxides becomes large enough to cause an increase in the leakage current at zero back-gate bias. This leakage current can prevent the top-gate from being completely turned off. If it is large enough, it can cause parametric (and potentially functional) failure in integrated circuits. The

leakage currents at zero back-gate bias of the three devices from wafers A, B, and C after 1 Mrad (SiO_2) irradiation are ~20 μA, ~0.2 μA and ~0.1 nA, respectively. It is clear that silicon implantation is very effective to reduce the leakage current caused by the radiation-induced positive charge buildup in the buried oxides. Also for both SIMOX and UNIBOND substrates, very little interface trap buildup has been observed for standard bias conditions and radiation levels. As can also been seen in the I-V curves in Figure 25, there is only very small stretchout due to interface traps in these devices from three wafers.

Figure 26 shows back gate threshold voltage shifts as a function of irradiation dose for SOI devices with and without Si implantation. The back-gate threshold voltage shifts of the three devices from wafers A, B, and C after 1 Mrad (SiO_2) irradiation are –8.5 V, –7.2 V, and –6.9 V, respectively. Devices from wafers B and C have relatively smaller shifts in the back gate threshold voltage, confirming the expected reduction in net positive oxide-trap charge in the BOX.

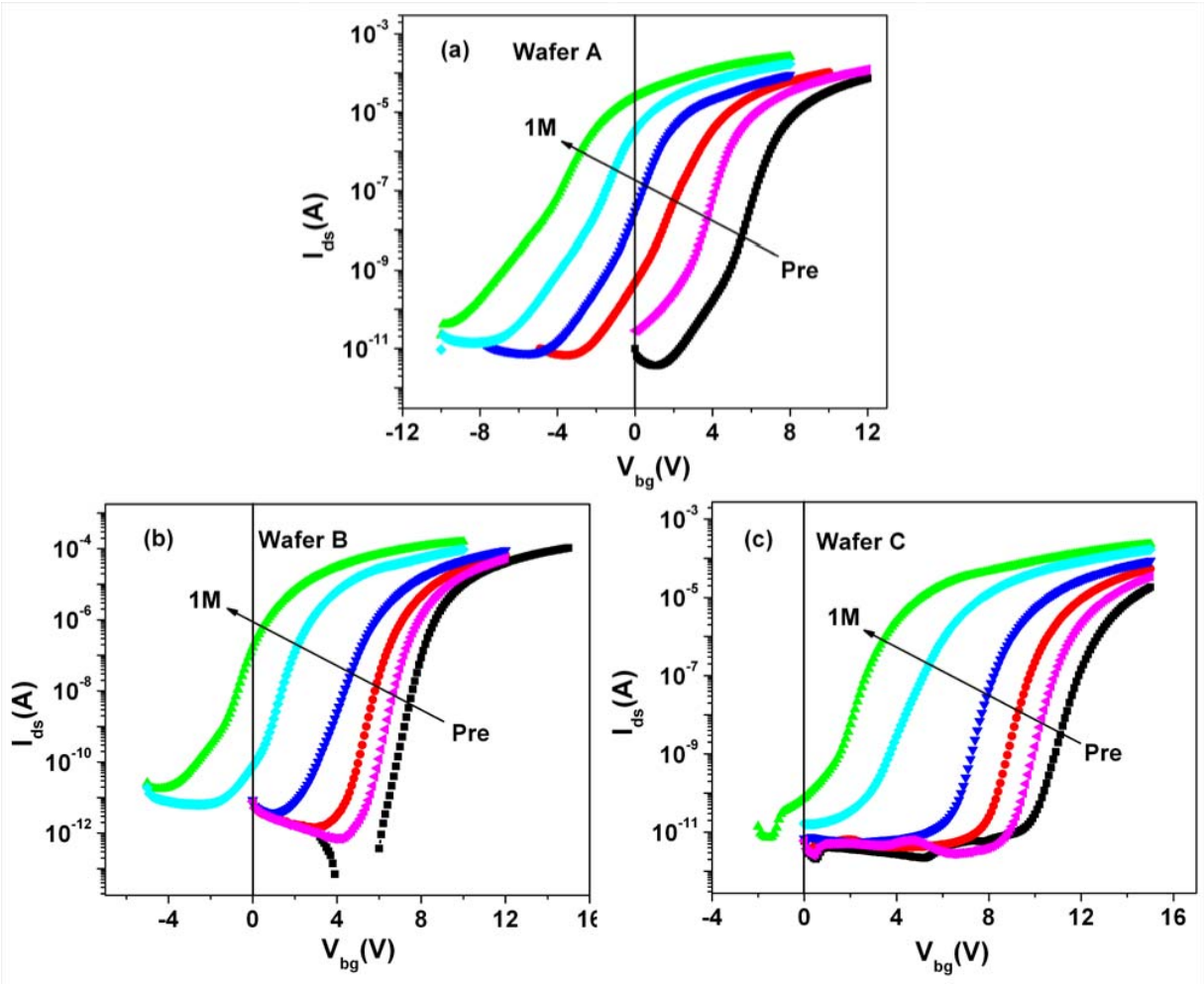

Figure 25: I-V characteristics for back-gate transistors from wafer A, B, and C irradiated to 1 Mrad(SiO_2). The top gates were grounded during the back-gate I-V measurements. The transistors were irradiated with all the pins grounded. The intermediate irradiation doses are 50 krad, 100 krad, 200 krad, 500 krad, and 1 Mrad(SiO_2). Wafer A received no Si implant in the buried oxide; Wafers B and C were implanted with Si to different doses at an energy of 130 keV.

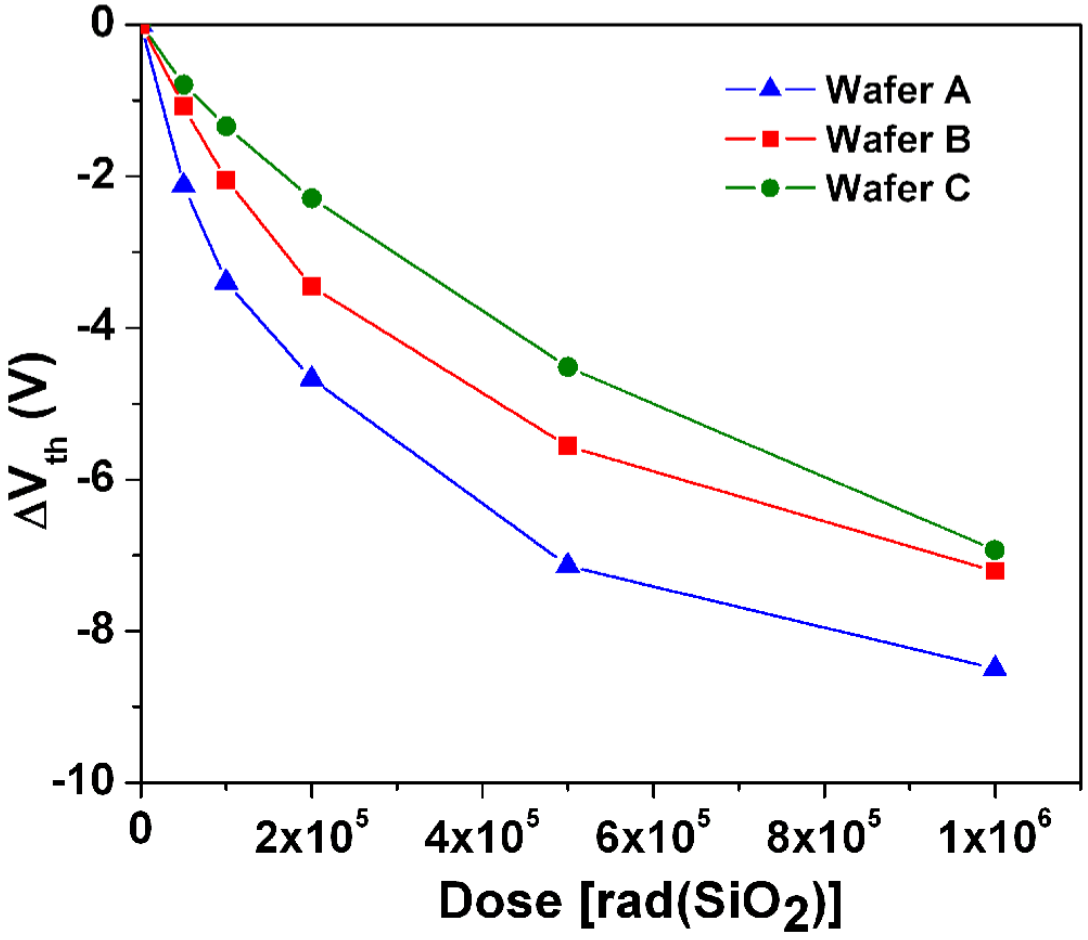

Figure 26: Back-gate threshold voltage shifts measured for transistors fabricated using wafers A, B, C. The transistors were irradiated with all pins grounded. Wafer A received no Si implant in the buried oxide; Wafers B and C were implanted with Si to different doses at an energy of 130 keV.

A plot of the noise power spectral density of a wafer C device at room temperature as a function of total dose is presented in Figure 27. Here the drain bias was held at 100 mV and $(V_{bg} - V_{th(bg)})$ at 4 V. As expected from previous work on the gate oxides of bulk MOS devices [10]-[11], [13], S_{V_d} increases with increasing total dose, and power-law frequency dependences are consistently observed for these devices. Compared to the results on the gate oxide of bulk MOS devices under positive gate bias [10]-[11], [13], the noise power does not increase as much with irradiation in this case. This likely is due to the fairly high defect density in these devices

due to the Si implantation before irradiation [101], making them less sensitive to changes with radiation-induced charge.

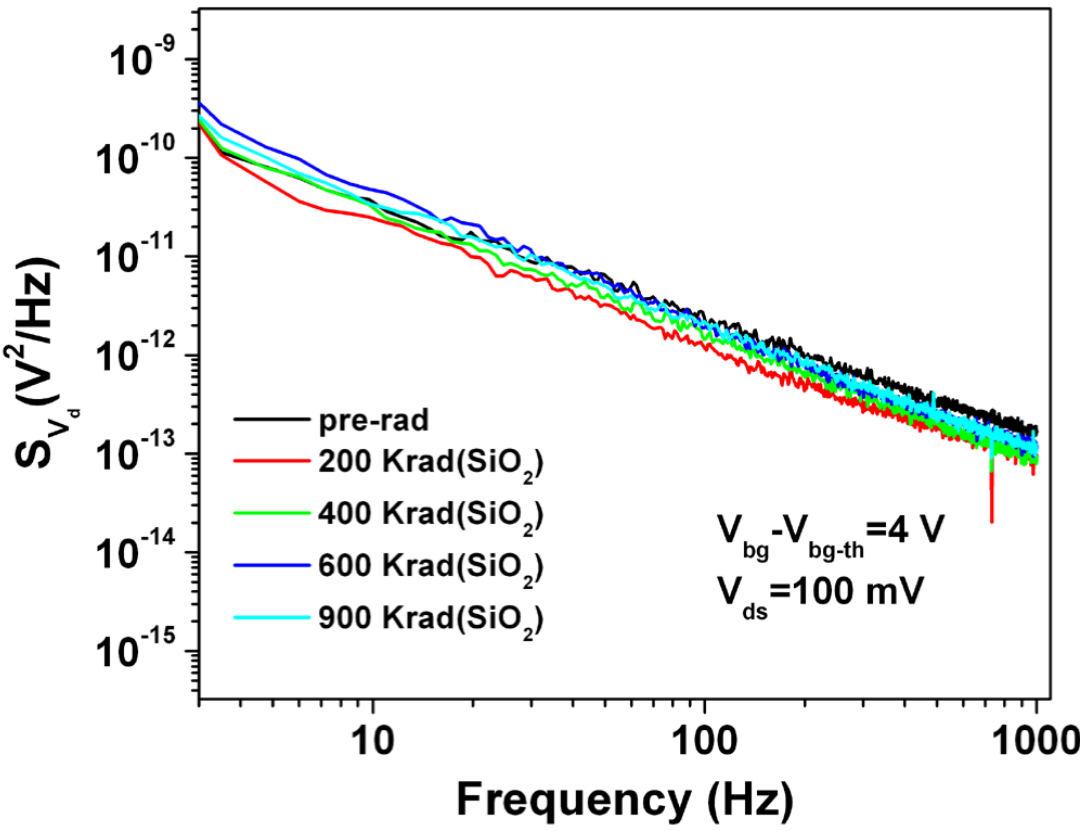

Figure 27: 1/f noise power S_{V_d} *for a wafer C device as a function of total irradiation dose.*

Figure 28 also shows the effects of radiation exposure on the back-gate 1/*f* noise of the SOI transistors from three wafers. The wafer A transistors have the lowest noise before irradiation, but their noise increases the most after irradiation. Wafer C transistors have the highest pre-irradiation noise, but their noise level shows little change after irradiation [97]. Hence, the differences in noise levels among the devices with and without Si implantation of the BOX become less significant after irradiation. Again, this is probably due to the high defect

density caused by Si implantation, which makes the noise less sensitive to the radiation-induced trapped charge.

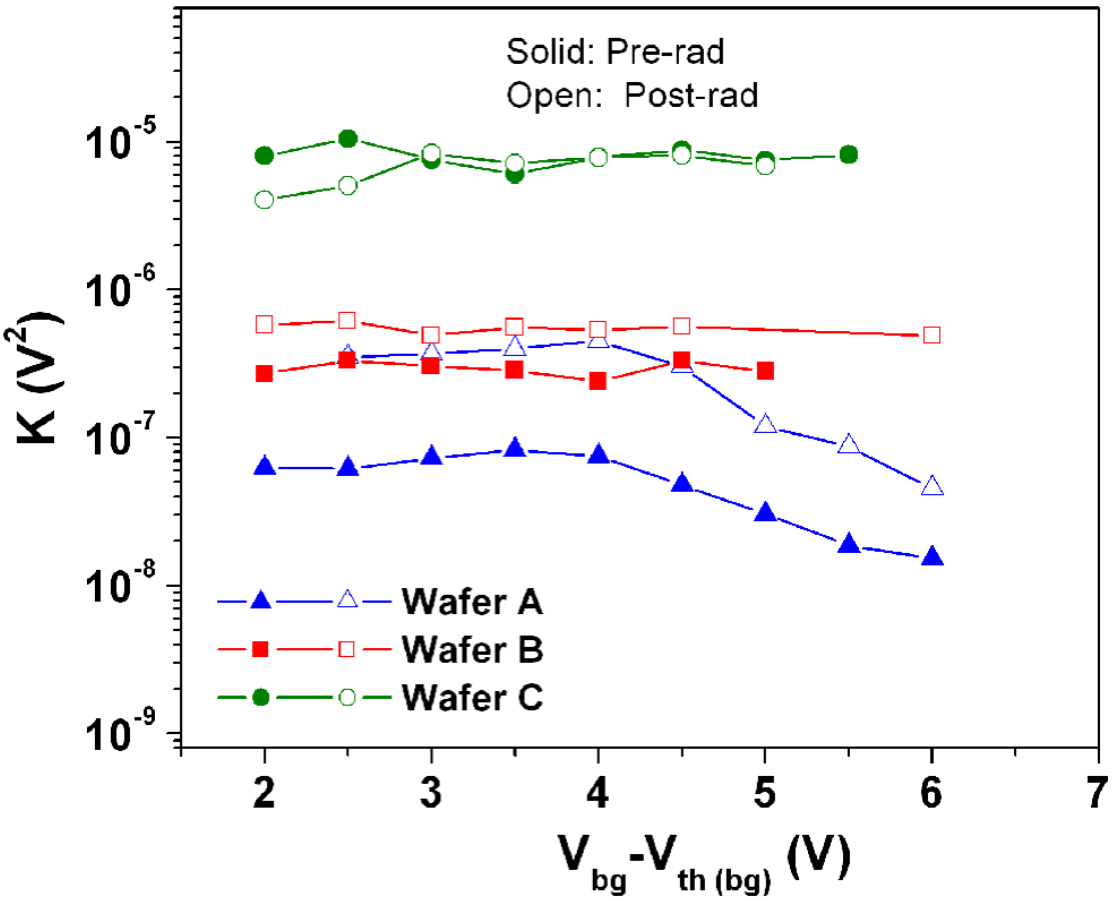

Figure 28: Normalized drain voltage noise power K for the back-gate channels of the SOI transistors from wafers A, B, and C before and after 1 Mrad(SiO_2) irradiation.

Test of Dutta-Horn Model

Back gate threshold voltages were measured as a function of temperature before noise measurement. We measured the drain current in the linear region as a function of applied back gate voltage with $V_{ds} = 0.1V$, and extrapolated or interpolated the threshold voltages from the I-V curve at each temperature before and after irradiation to ensure that $(V_{bg} - V_{bgth})$ was held constant

during all noise versus temperature measurements to facilitate noise comparisons. The threshold voltage decreased with increasing temperature by ~ 4.4 mV/K over this temperature range, which is a somewhat stronger temperature dependence than that observed for bulk MOS devices [78].

Voltage noise power spectral densities were measured at intervals of 5 K between 85 K and 320 K with the drain biased at $V_d = 100mV$. At each temperature, the noise was measured with gate bias $(V_{bg} - V_{bg-th}) = 4V$. Figure 29 shows typical noise versus frequency curves at different temperatures. At all temperatures at which we checked, S_{V_d} could be described well by Eq. (5.1).

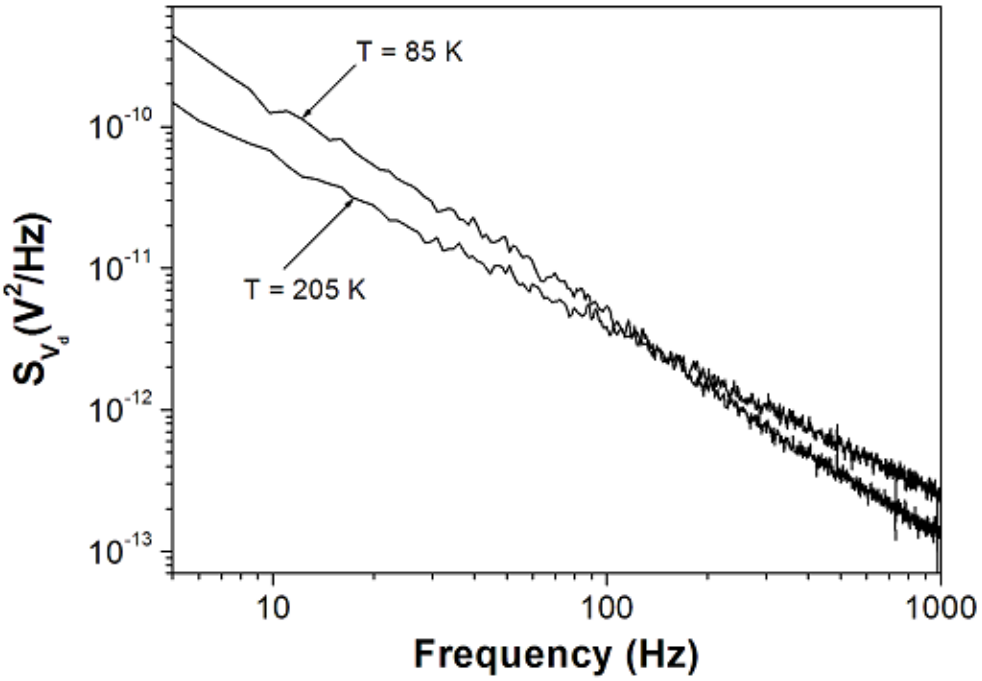

Figure 29: Log-log plots of the excess drain-voltage noise power spectral density S_V, after correction for thermal and background noise, at T=85 K and T= 205 K after 2.08 Mrad(SiO_2) irradiation.

For data like those in Figure 29, we fit each excess noise curve in the frequency range 5 Hz to 500 Hz to determine the frequency exponent α at each temperature for use in later

analysis. In Figure 29, at 85 K after 2.08 Mrad(SiO_2) irradiation, $S_V(1Hz) = 5.82 \times 10^{-9} V^2/Hz$ and α = 1.55. The value of $S_V(1Hz) = 9.31 \times 10^{-10} V^2/Hz$ and α = 1.19 at 205 K. This illustrates the range of variation in noise magnitude and frequency dependence observed as functions of temperature for these back-channel SOI devices. The spectral slope at low temperature is higher than typically observed for top-gate noise in SOI MOSFETs and bulk MOS noise [10]-[15], [78], as we will discuss further below. However, the results were consistent and repeatable for these devices, as we now demonstrate.

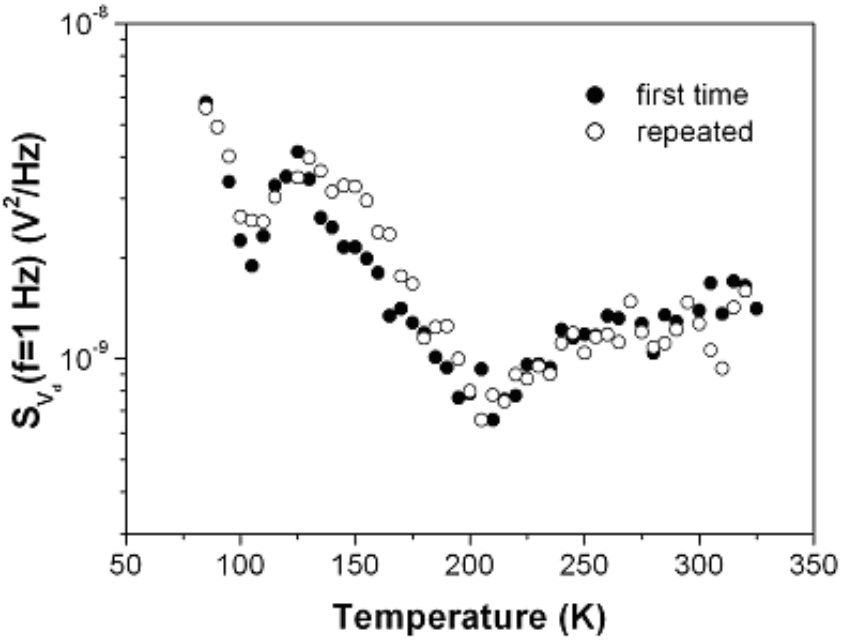

Figure 30: The noise magnitude at 1 Hz versus temperature for a wafer C device after 10-keV X-ray irradiation to 2.08 Mrad (SiO_2).

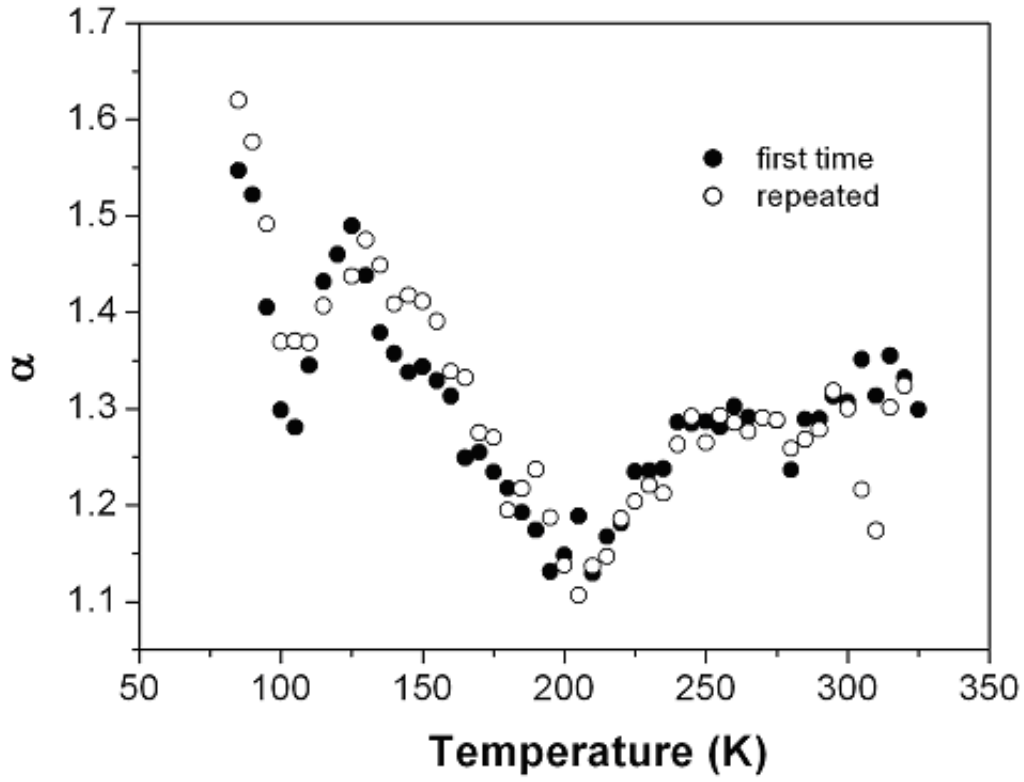

Figure 31: Frequency dependence of the noise versus temperature for the device of Figure 30 after 10 keV X-ray irradiation to 2.8 Mrad(SiO_2).

In Figure 30, the voltage-noise power-spectral density at $f = 1Hz$ (the choice of specific frequency is not critical to the results) is plotted as a function of measurement temperature. The second trace is a repeated measurement for the same device and measuring conditions. As can be seen, the device response is unchanged by temperature cycling, to within experimental uncertainty. Also, there was no obvious annealing during noise measurement up to 320 K (47ºC); but at higher temperatures, annealing of radiation damage would of course be expected [11], [13], [137]. Figure 31 shows the frequency dependence of the noise as a function of temperature for the same device as Figure 30. The frequency exponent α is in the range of 1.1-1.64, with the higher values occurring at the lowest temperatures.

Figure 30 and Figure 31 clearly demonstrate a strong and qualitatively correlated temperature dependence of the noise. To determine whether the noise of the devices can be described quantitatively by the Dutta-Horn model, we applied Eq. (3.1) to try to predict $\alpha(T)$ from the noise magnitude data, and compared the predictions with the measured noise. The results of the comparison are shown in Figure 32 for low frequency noise of the wafer C device after 2.08 Mrad(SiO_2) irradiation. A value of $\tau_0 \cong 1.8x10^{-15}\,s$ was used in this comparison, which corresponds to a typical inverse-phonon frequency in the near-interfacial SiO_2 [79], [140], [141]. The particular value assumed for the attempt to escape time did not strongly affect the analysis, because it appears in a logarithm in Eq. (3.1). It is found that a significant offset exists between measured and calculated $\alpha(T)$, as shown in Figure 32, and consistent with prior work on carbon resistors [142]. The largest difference between the prediction and experiment is observed at low temperature. The peak at ~ 125 K for the measured noise is similar in shape to the peak in predicted noise at a comparable temperature. However, such an offset is not observed for bulk Si MOS devices [78], nor as we now show, is it always observed for SOI back gate noise.

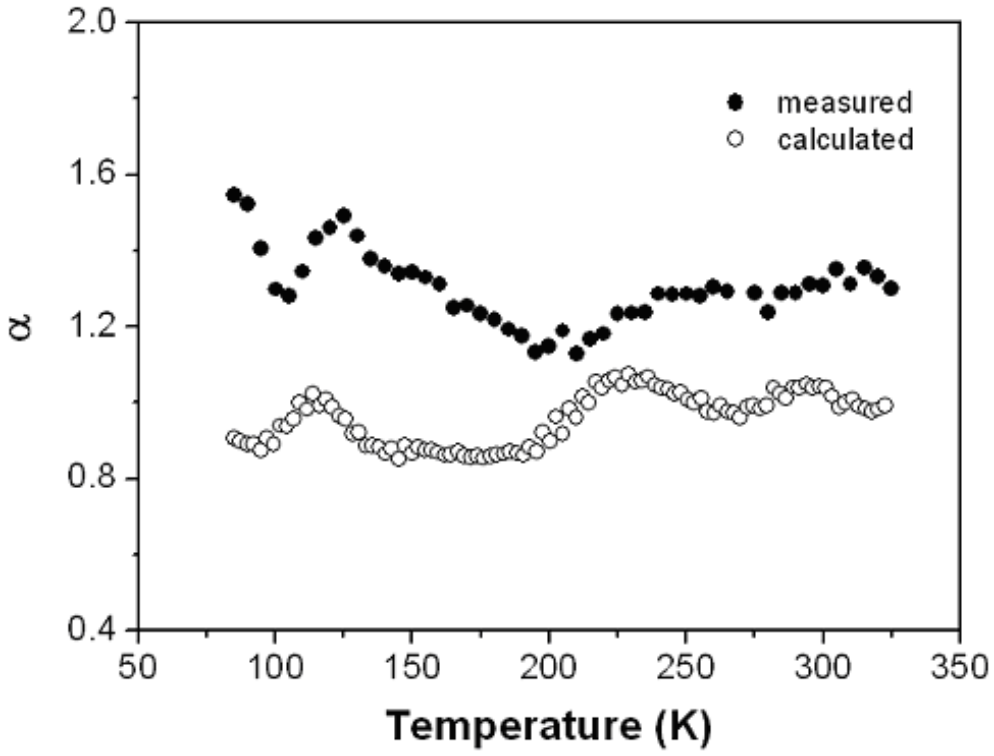

Figure 32: α as a function of T for a wafer C device after irradiation. [solid symbols for measured data, open symbols calculated from data shown in Figure 30 through Eq. (3.1)].

For an SOI nMOS device with the same feature size from wafer B, we performed noise measurements as a function of temperature before and after 1.04 Mrad(SiO_2) unbiased irradiation. Figure 33 and Figure 34 show the temperature dependence of the noise magnitude and frequency exponent of these devices, having differently processed buried oxides. A strong temperature dependence of the noise is observed, with the noise magnitude showing a comparable level before and after irradiation. The prediction of the Dutta-Horn model is compared with the measured $\alpha(T)$ for the post-irradiation condition in Figure 35. The overall shape and magnitude of $\alpha(T)$ are generally reproduced very well by the Dutta-Horn model, consistent with what we have recently reported for bulk MOS devices both before and after irradiation [78]. These results show that sometimes one gets good quantitative agreement with

the Dutta-Horn model for SOI back-gate noise, and sometimes one does not, depending on specific device processing and experimental conditions. Both of these types of response have been observed for more than one device, and are repeatable for individual devices.

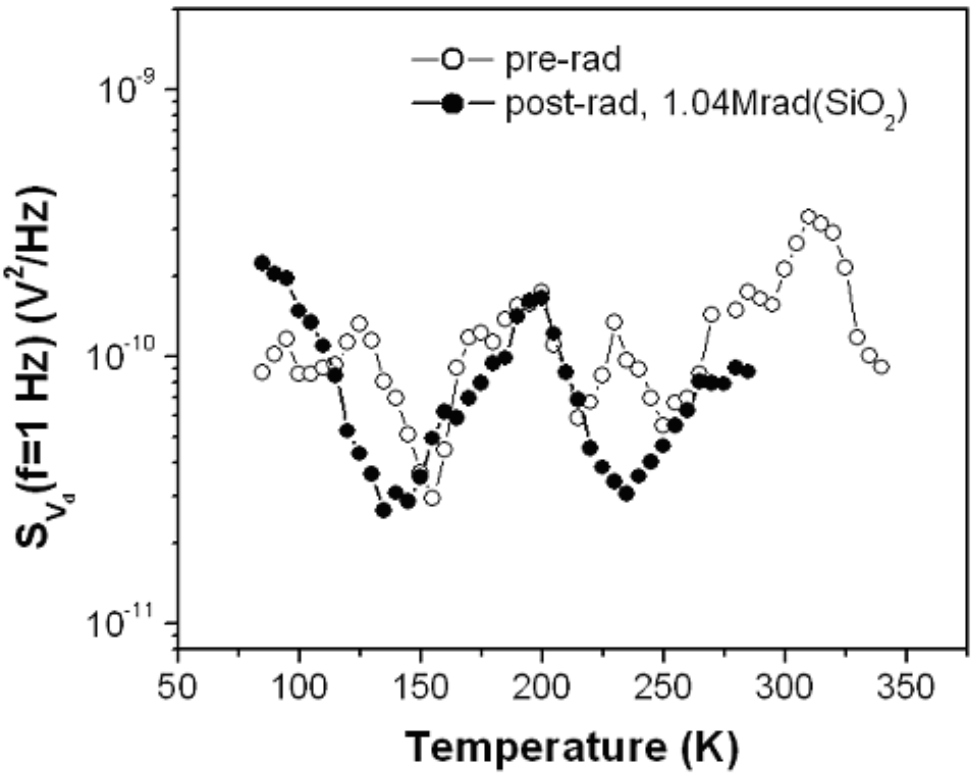

Figure 33: The noise magnitude at 1 Hz versus temperature for wafer B SOI nMOS devices before and after 10-keV X-ray irradiation to 1.04 Mrad (SiO2). $(V_{bg} - V_{bg-th}) = 4V$ *and* $V_{ds} = 100mV$.

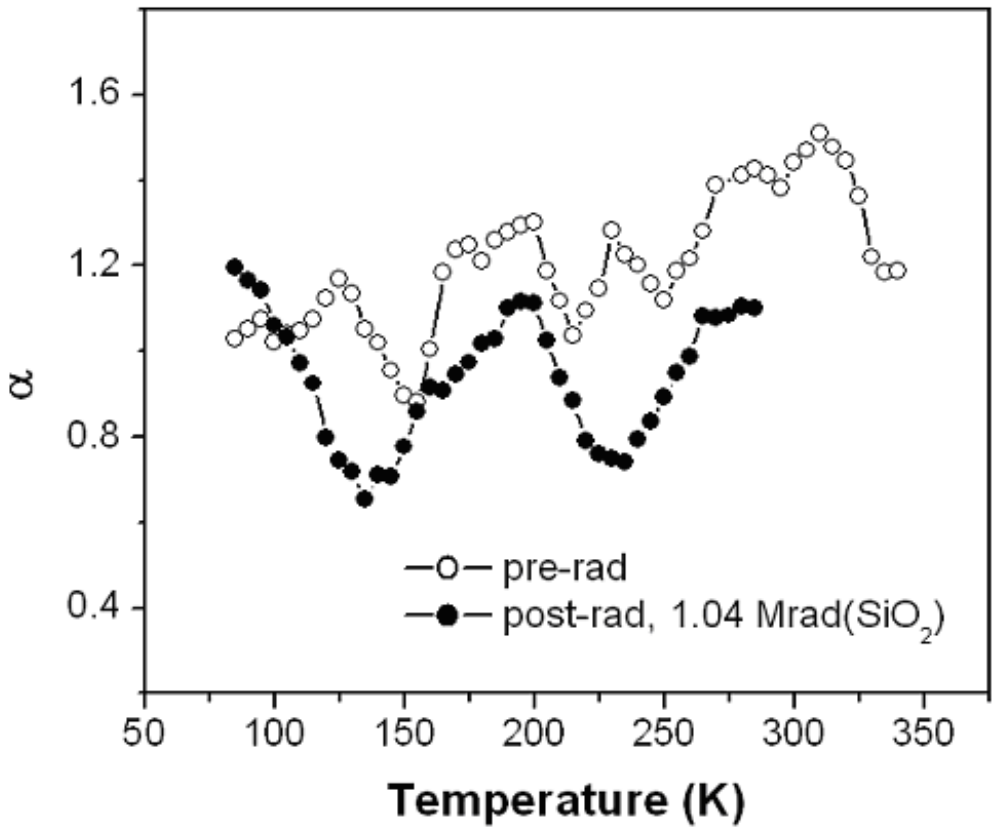

Figure 34: The frequency exponent α *versus temperature for wafer B devices before and after 10-keV X-ray irradiation to 1.04 Mrad (SiO2).* $(V_{bg} - V_{bg-th}) = 4V$ *and* $V_{ds} = 100mV$.

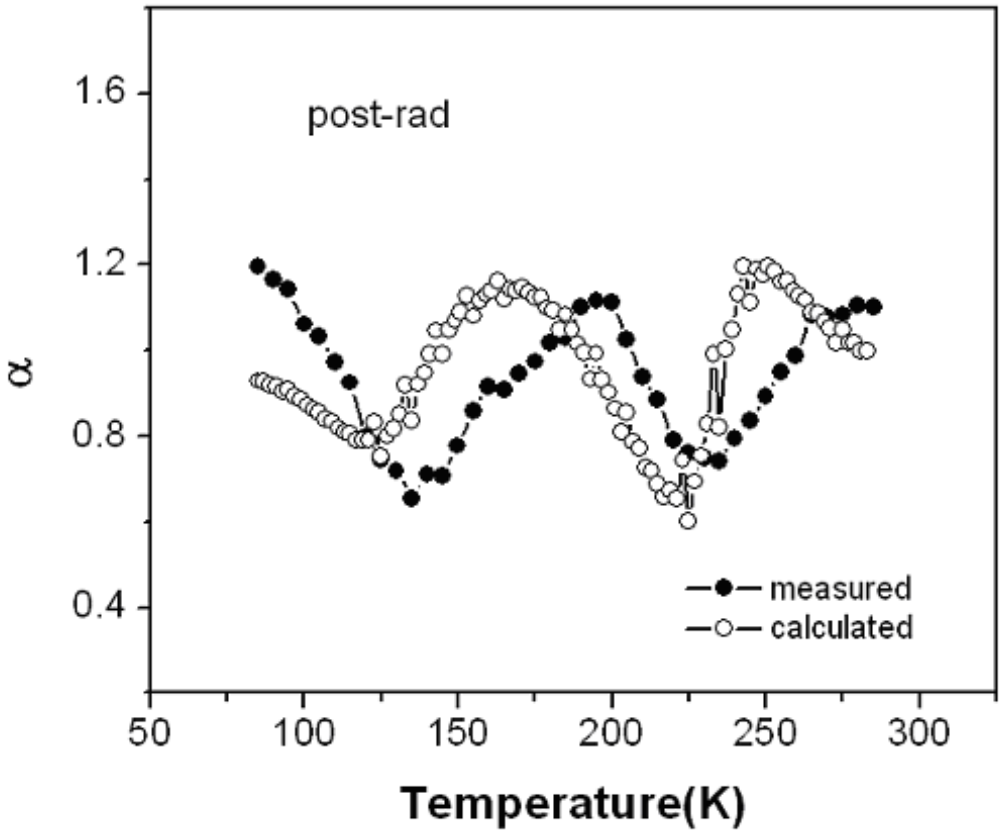

Figure 35: α as a function of T for the wafer B SOI nMOS device after irradiation [solid symbols for measured data, open symbols calculated from data shown in Figure 33 through Eq. (3.1)].

The differences in the responses of devices from wafers B and C are quite interesting and may indicate a mixture of noise sources in the wafer C devices that do not follow simple Dutta-Horn defect kinetics. At present we do not know the reason for these differences. One noise mechanism that leads to a frequency exponent $\alpha \sim 1.5$ in some types of device geometries that could be consistent with the results we see is diffusion of a hydrogen-related species. For example, Scofield *et al.* have observed this type of noise in Nb films [143], [144] and Zimmerman et al. have studied it in detail in Pd and $Pd_{0.8}Si_{0.2}$ films [145], [146]. Material types and sample geometries differ in those studies from ours. However, it is interesting to note that

mobile protons are often observed in SOI buried oxides [147], [148], and the mobility of these protons can be affected by applied bias and radiation exposure [149], [150]. Indeed, some protons are sufficiently mobile that it has been suggested for different kinds of device structures that they might be suitable for use as nonvolatile memory devices [43], [44]. So it is possible that the wafer C devices include a much stronger diffusion noise component than the wafer B devices. However, this is presently speculation, and more work is required to determine whether this or another mechanism is responsible for the observed differences in results.

Stress Instabilities

For fully-depleted transistors the top and back gates are electrically coupled together and charge in the BOX will directly affect the top-gate transistor threshold voltage. Also, by varying the bias on either the top-gate transistor or the bottom of the wafer, electrons can tunnel in and out of the metastable electron traps changing the amount of trapped charge in the BOX pre-irradiation. Figure 36 is a plot of pre-irradiation back-gate transistor I-V curves for process C taken with a) a +40 to –40 V back-gate transistor sweep, b) after applying a +50 V bias to the back-gate transistor for 5 minutes and sweeping the back-gate transistor from +40 to –40 V, and c) after applying a -50 V bias for 5 minutes to the back-gate transistor and sweeping the back-gate transistor from -40 to +40 V. The direction of the shift is inconsistent with hole, proton, mobile ion, or electron transport through the buried oxide. It is consistent with electron tunneling from the silicon into metastable electron traps in the buried oxide. With a positive bias applied to the substrate (red curve), electrons in the channel region can tunnel into the electron traps making the oxide more negatively charged. This will increase the back-gate transistor threshold voltage. Conversely, with a negative bias applied to the substrate (green curve), holes in the

channel region can tunnel into the neutral traps making the oxide more positively charged. This will decrease the back-gate transistor threshold voltage (towards depletion). Thus, the creation of the electron traps by the hardening implant has produced a large bias-induced hysteresis in the I-V curves.

Figure 37 shows threshold voltage shifts as a function of back-gate bias and stressing time for transistors from wafers A, B, and C. Here the devices were stressed with V_{bg} = 50 V for 2000 s, then at V_{bg} = –50 V for 4900 s, and another stress cycle with different stress time [117], [118]. I-V curves were collected during stressing interruptions to extract threshold voltages. The back-gate was swept from +35 V to –35 V to collect the I-V curves after positive bias stressing, and from –35 V to 35 V after negative bias stressing. The effects of bias stressing are very different for these transistors. Wafer A device back-gate threshold voltages do not show any noticeable change. Wafer C device back-gate threshold voltages change as much as ± 10 V at these bias conditions.

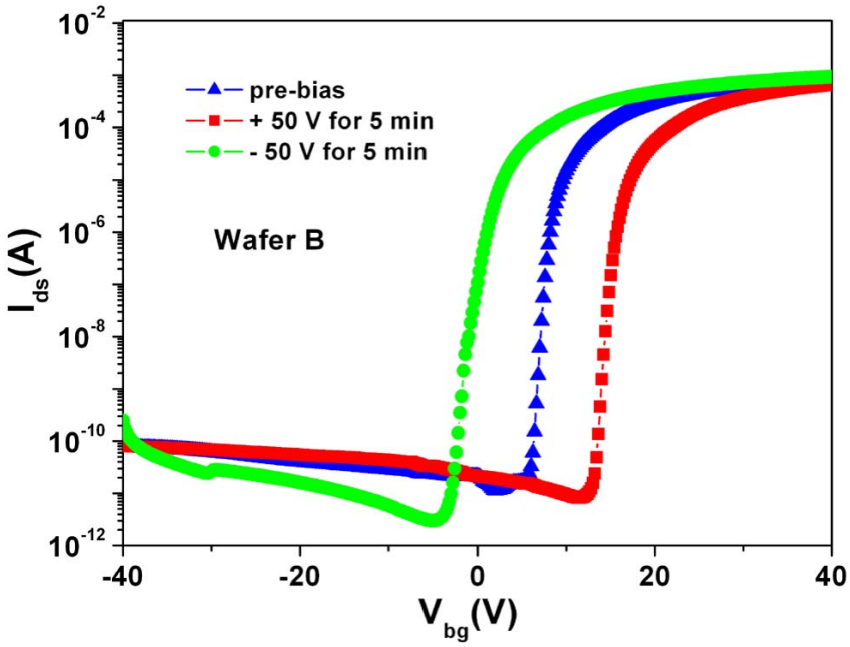

Figure 36: Back-gate transistor I-V curves on a hardened, standard-geometry transistor fabricated using process B with a) a +40 to –40 V back-gate sweep, b) after applying a +50 V bias to the back gate for 5 min and sweeping the back gate from +40 to –40 V, and c) after applying a –50 V bias for 5 min to the back gate and sweeping the back gate from –40 to +40 V.

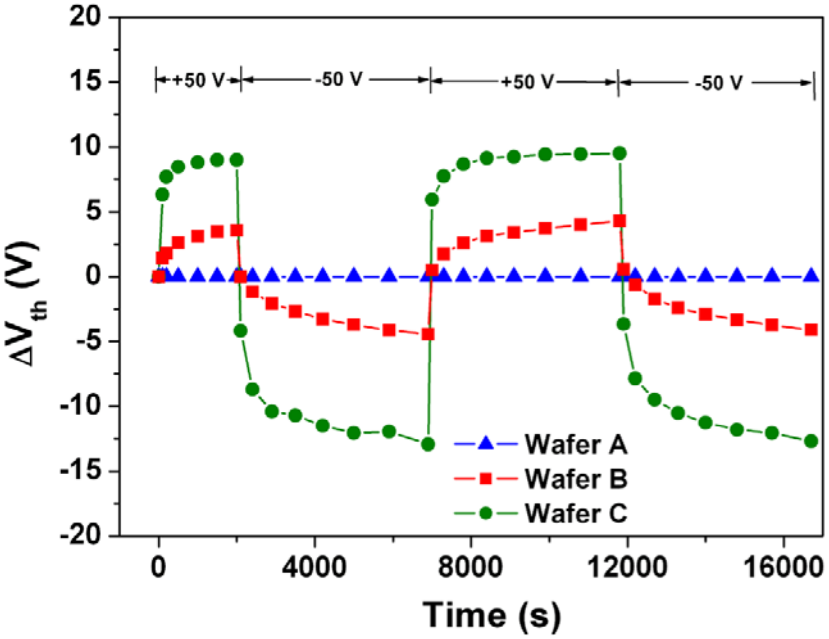

Figure 37: Back-gate threshold voltage shifts of devices from wafers A, B, and C as a function of time and bias, at room temperature.

The threshold voltage shifts in Figure 37 are consistent with electron trapping and detrapping from shallow traps. Under positive back-gate stress bias, electrons in the back channel move into the buried oxide and are captured by the electron traps, making the BOX more negatively charged, hence a higher back-gate threshold voltage is observed. Under negative bias, electrons are detrapped and the BOX is more positively charged. This behavior is consistent with the type of charge compensation that is often exhibited by electron traps associated with trapped holes in SiO_2 [10], [69]-[71], [75], [125].

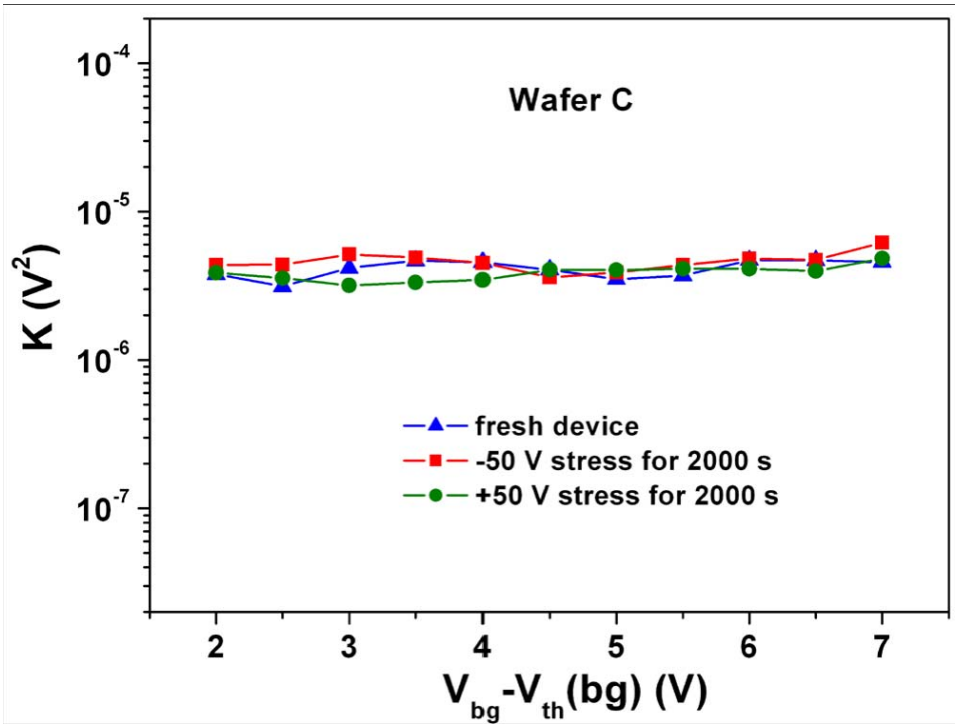

Figure 38: Normalized drain voltage noise power K for back-gate SOI transistors from wafer C before stressing, after –50 V stress for 2000 s, and after +50 V stress on the back gate for 2000 s. All stresses and noise measurements are performed at room temperature.

Figure 38 shows the comparison of normalized back-gate noise levels in a wafer C device before stress, after +50 V stressing on the back-gate for 2000 s, and after –50 V stressing for

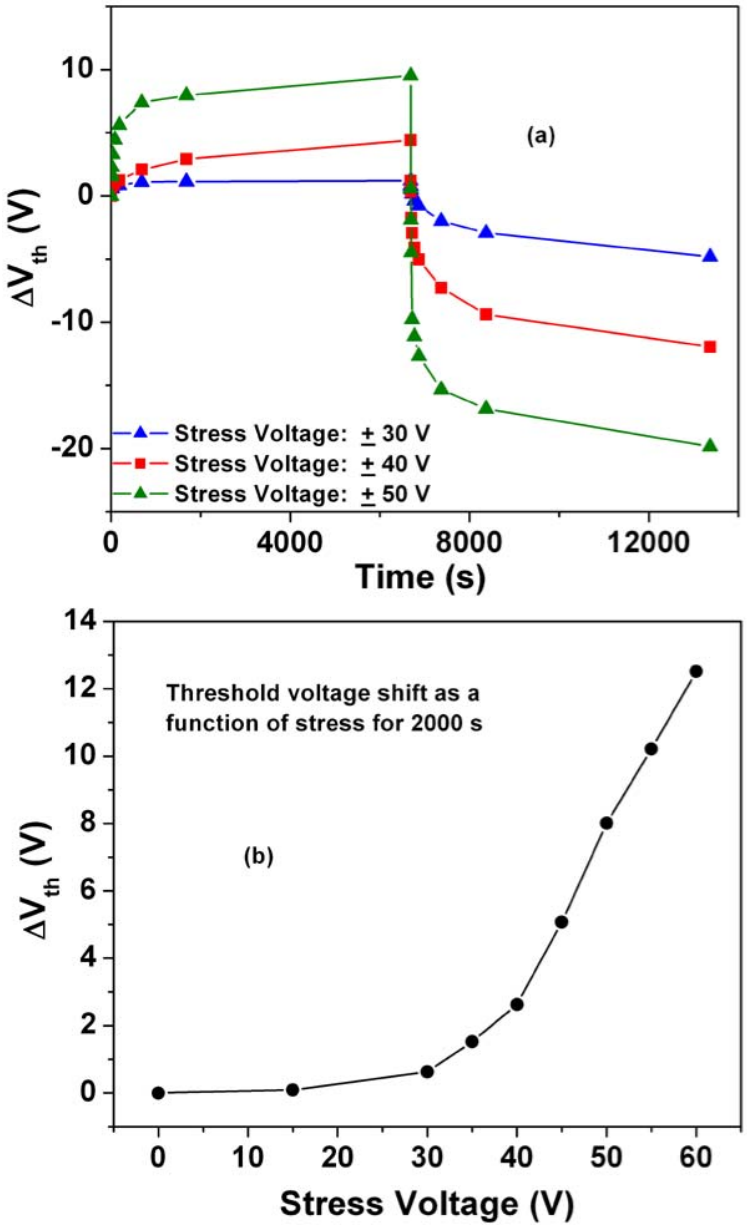

Figure 39: (a) Back-gate threshold voltage shifts of a wafer C device as a function of stress time with different stress bias at ±30 V, ±40 V and ±50 V; (b) back-gate threshold voltage shifts as a function of stress voltage after 2000 s stressing at each voltage. The starting threshold voltage is kept the same.

another 2000 s. The noise levels show little change after stressing, although the threshold voltage shifts can be as large as ± 8 V. This shows that changes in the charge states (filled or empty) of

the defects responsible for the back-gate threshold-voltage instabilities do not strongly affect the carrier interactions with the shallow defects very near the interface that lead to the noise. Hence, the defects causing the bias instabilities apparently are deeper in energy and/or further from the interface than the particular defects that cause the noise. However, their microstructures may be similar [79], [125].

Bias instabilities of a wafer C device were also tested as a function of stress magnitude. Figure 39(a) shows the threshold voltage shifts as a function of both back-gate bias and stress time for a wafer C device; Figure 39(b) shows the threshold voltage shifts as a function of the back-gate bias after 2000 s stressing at each voltage. The bias-induced threshold voltage shift is less than 2 V after 2000 s stressing at +35 V, while biasing at +60 V for 2000 s introduces a threshold voltage shift of more than 12 V.

In Figure 40, the same stress cycling is repeated three times at ± 50 V before irradiation to 1 Mrad(SiO_2) at 0 V. The threshold voltage shifts are strikingly repeatable, indicating the reversibility of the charge trapping/detrapping under stressing at different polarity. After irradiation, positive charge is trapped in the BOX, shifting the threshold voltage curve in Figure 40 negatively. However, the radiation-induced trapped holes are stable under the electrical field during bias stressing. This likely is because the radiation-induced trapped holes are distributed through the buried oxide during the 0 V irradiation [44]-[120], so they do not interact strongly with the shallow electron traps near the interface that cause the bias instabilities. Hence, the bias instabilities observed here would continue to be observed after the device is irradiated.

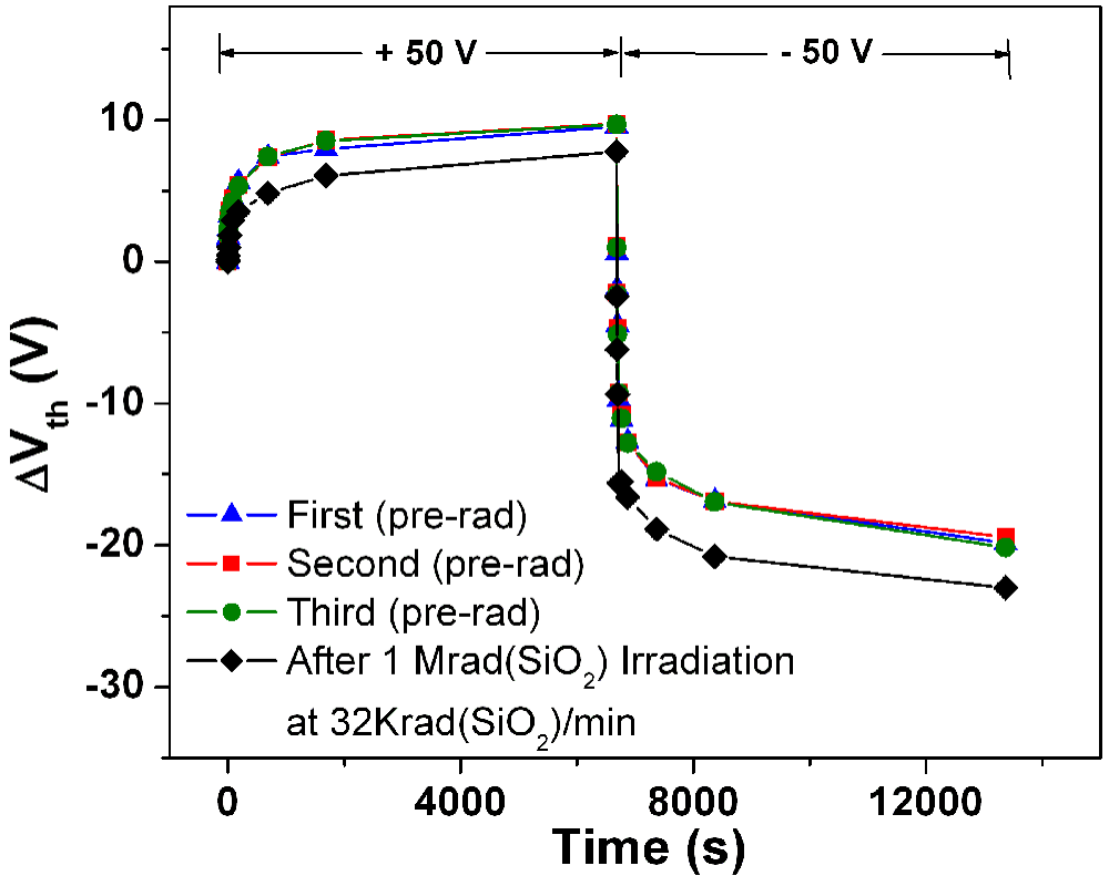

Figure 40: Back-gate threshold voltage shifts of a wafer C device with the stress voltage at ±50 V. The cycling was repeated three times and once more after 1 Mrad (SiO_2) irradiation at 0 V bias. The starting threshold voltage is kept the same.

Figure 41 shows the effect of stress cycling on wafer C device back-gate threshold voltage shifts at different temperatures as a function of applied voltage stress. The shifts are essentially independent of temperature, suggesting that the charge exchange between the Si channel and the shallow electron traps responsible for the voltage instabilities occurs primarily due to tunneling [124], [125].

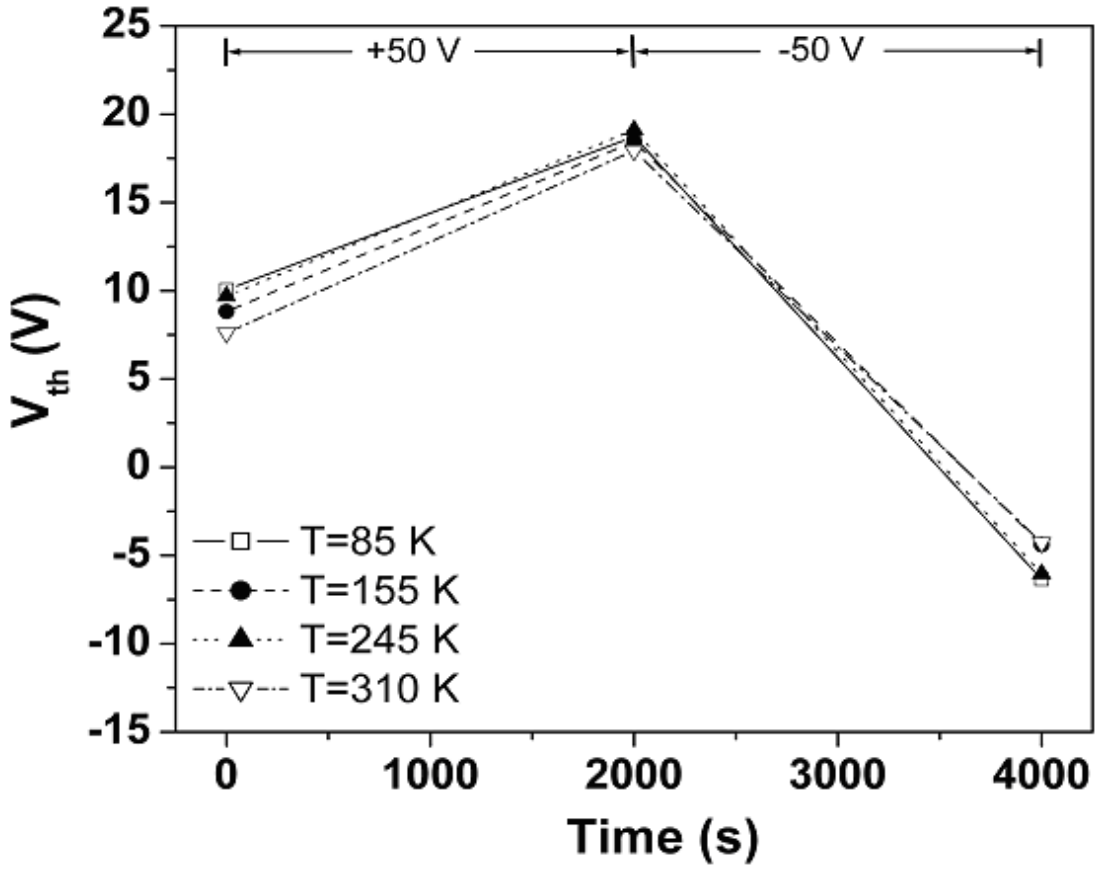

Figure 41: Effect of temperature on the back-gate threshold voltage shifts of wafer C transistor under bias stressing.

CHAPTER VII

CONCLUSION

In summary, we have measured the low-frequency noise and radiation response of MOS transistors with Al_2O_3/SiOxNy/Si(100) gate dielectrics. We find that both the radiation-induced threshold-voltage shifts and the low-frequency noise are significantly larger than are typically observed for high-quality thermal SiO_2 thin films of comparable thicknesses. The low-frequency noise of these high-κ devices can be described well with a number fluctuation model.

Low frequency noise measurements were performed on the fully depleted SOI MOSFET buried oxides, and used to estimate the density of border traps in the buried oxides. It was shown that silicon implantation in the buried oxide increases the back-channel low frequency noise. Our measurements show that noise is improved in the double-gate mode of operation, which may benefit the performance of FD SOI devices in a radiation environment.

We have shown that the back-gate $1/f$ noise of SOI MOS transistors is strongly temperature-activated, consistent with previous work on bulk MOSFETs. Noise measurements are consistent and repeatable for each type of device. The Dutta-Horn model describes the noise well for some devices we have measured, but not for all devices under all experimental conditions. Future work exploring the reasons for these differences should provide significant insight into the defects that cause back-gate $1/f$ noise in MOS devices.

Si ion implantation of the BOX of SOI transistors decreases the net oxide trap charge created during irradiation in the buried oxide. The noise in these wafers changes little compared to the control wafer without Si ion implantation after irradiation. Differences in the noise levels

of the implanted and unimplanted devices are reduced during irradiation exposure. Si implantation also creates shallow electron traps near the Si/SiO_2 interface that can exchange charge with the back channel easily. The charge exchange responsible for bias instabilities in the implanted BOX is shown to be primarily due to tunneling.

APPENDIX

A. Thermal Noise Measurement

Thermal noise comes from the random thermal movements of the carriers in solids. It exists universally in all kinds of electronic devices. The magnitude of thermal noise is only dependent on the resistance and temperature, even without current or voltage applied. Nyquist's theorem for the thermal noise of a resistance R at a temperature T leads to the following expression for the thermal noise power spectral density:

$$S_V = 4KTR. \tag{A.1}$$

For a 1 MΩ resistor at room temperature, the power spectral density equals $1.66 \times 10^{-14} (V^2/Hz)$.

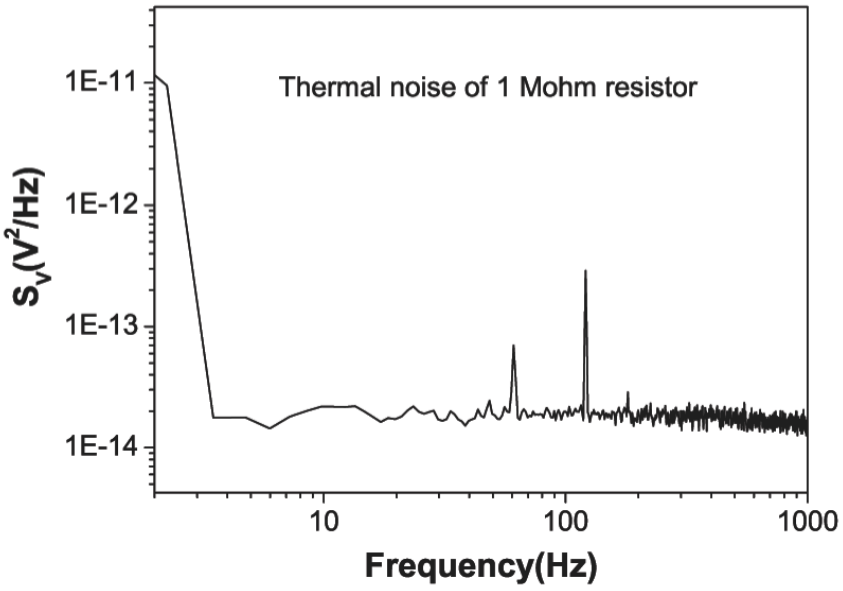

Figure 42: 1 MΩ resistor's thermal noise from 0.3 Hz to 1 kHz

We have used this as a self-test and calibration of our noise measurement systems. We measured the thermal noise of the resistor in the frequency range of 1 Hz to 1000 Hz. The spectrum is shown in Figure 42. The thermal noise has the same level as what Eq. (A.1) expects. The big increase at low frequency is due to amplifier noise, which is ignored in the analysis.

B. Control Source Code Examples

BASH is the shell, or command language interpreter that will appear in the GNU operating systems like Linux. It is also a fairly powerful programming language. A shell program, called a script, is an easy-to-use tool for building applications by "gluing" together systems calls, tools, utilities, and complied binaries. We use BASH shell to write scripts to control the measurement flow. Below is the example code written in BASH for the entire noise measurement flow.

```
#!/bin/sh
dir=/home/noise/measurement/SOI/W1-61/noise          # Directory to store data
device=W3-85-T1N4                                    # Device under test
vth=7.68                                             # Threshold voltage value
for Vdrain in 0.1
do
echo "Device: $device" >>$dir/current
echo "Vth=$vth, Vgs-Vth=2V, R=80.3Kohm,designed drain voltage=$Vdrain " >>$dir/current
./voltb `echo "$vth+2" | bc`                         # Apply bias on the back gate
./volta 1                                            # Apply bias on the drain
sleep 3
VDS=`./multimeter1`                  # Obtain the drain DC bias from the multimeter
VA=`./voltage-convert 1 $VDS $Vdrain`  # Calculate proper bias for  the designed bias point
./volta $VA                          #  Apply proper bias
sleep 3
A=`./multimeter1`
echo "Va=$VA, Vdrain= $A" >>$dir/current        # Record the bias values
echo "      " >>$dir/current

echo "Finishing applying bias, beginning counting 150:"
#measure the noise

#echo "Press return when the overloading light is off"
#read a

sleep 10
./3562init 150 1000                  # Signal analyzer start measuring
./read >log                          # Measurement done, save the data to computer
cat log >$dir/$device-TG-$Vdrain-fg.dat
echo "Finishing Fg noise measurement."
#measure the background
```

```
./volta 0                          # Keep the bias on the gate but ground the drain
sleep 10
./3562init 80 1000                 # Do the background measurement.
./read >log                        # Save the background noise data
cat log >$dir/$device-TG-$Vdrain-bg.dat
echo "Finish the Bg noise measurement."
#Lines below are used to do the data analysis and plot the noise curve using gnuplot
cat $dir/$device-TG-$Vdrain-fg.dat | tail -802 >tmp/tmpdata-fg
cat $dir/$device-TG-$Vdrain-bg.dat | tail -802 >tmp/tmpdata-bg
./convert.pl >$dir/$device-TG-$Vdrain
done
cat >tmp/cmd << EOF
set data style linespoints
set logscale
plot '$dir/$device-TG-$Vdrain' using 1:2
EOF
gnuplot -persist tmp/cmd
rm tmp/tmpdata-fg
rm tmp/tmpdata-bg
rm tmp/cmd
```

GPIB instruments are the most popular, worldwide standard for test and measurement systems. The National Instruments GPIB-ENET/100 Ethernet-to-GPIB controller and NI-488.2 take advantage of the network connectivity in instrument control applications. Using the GPIB-ENET/100 box, networked computers can communicate with and control IEEE 488.2 enabled equipment from anywhere on an Ethernet-based TCP/IP network. Codes were written in C language to send commands to each equipment item through GPIB-ENET controller. Most equipment in the system is connected to the GPIB controller, including HP 3562A dynamic signal analyzer, HP 4140 voltage source, HP 3478A digital multimeter, and the temperature controller. It turns out the codes share a lot of similarities, so only the commands specific to each instrument need be modified to suit our demands. The following script written in C is used to control the HP 3562A dynamic signal analyzer and is used as an example here to show how to send commands over GPIB bus.

```
#include"ugpib.h"                          # User GPIB include file
#include<stdio.h>
#include<stdlib.h>
#include<string.h>
#include<unistd.h>
#define PAD 22              # Define the GPIB primary address of the equipment under control
#define SAD 0               # Define the GPIB secondary address of the equipment
void wait(int ud)
{
   int stat;
   int status;

   stat=0;
   while((char)stat!='1')
   {
      send(ud,"smsd\n");
         ibrd(ud,&stat,3);
         sleep(1);
   }

}

int send(int ud,char *command)          # Subroutine, used to send command or instruction
                                        # to the equipment
{
   ibwrt(ud,command,strlen(command));
}

int main(int argc, int *argv)
{
   int id,rd,handle,ud;
   short lnf;
   char readbuf[100000],rsp;
   char trace[100];
   char avgstr[100],frsstr[100];
   int i,avg;
   handle=ibfind("gpib0");              # Find the GPIB controller
   ibpad(handle,0);
   ibrsc(handle,1);
   ibsic(handle);
   ibsre(handle,1);
   ud=ibdev(0, PAD, SAD, 13, 1, 0);     # Find the equipment with the specified primary address
   send(ud,"RST\n");                    # Reset the dynamic signal analyzer
   strcpy(avgstr,"navg ");
```

```
   strcat(avgstr,argv[1]);
   strcat(avgstr,"\n");

   strcpy(frsstr,"frs ");
   strcat(frsstr,argv[2]);
   strcat(frsstr," Hz\n");

//   printf("beginning measurement...\n");
   send(ud,"rst;lnrs\n");                  # Set the analyzer in linear mode
   send(ud,"clen 1000pts\n");             # Clear the buffer
   send(ud,"pspc\n");
   send(ud,"ch1\n");                      # Select Channel 1
   send(ud,frsstr);                       # Set the frequency range
   send(ud,avgstr);                       # Set the average number
   send(ud,"stbl\n");
   send(ud,"yasc\n");
   send(ud,"ism 4\n");
   send(ud,"strt\n");                     # Start the measurement
   wait(ud);
}
```

REFERENCES

[1] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: 1/*f* noise," *Rev. Mod. Phys.*, vol. 53, pp. 497-516, 1981.

[2] M. B. Weissman, "1/*f* noise and other slow, nonexponential kinetics in condensed matter," *Rev. Mod. Phys.,* vol. 60, pp. 537-571, 1988.

[3] A. L. McWhorter, "1/*f* noise and germanium surface properties," in *Semiconductor Surface Physics*. Philadelphia: Univ. Pennsylvania Press, 1957, pp. 207-228.

[4] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures - a new perspective on individual defects, interface states and low-frequency (1/*f*) noise," *Adv. Phys.*, vol. 38, pp. 367-468, 1989.

[5] F. N. Hooge, T. G. Kleinpenning, and L. K. J. Vandamme, "Experimental studies on 1/*f* noise," *Rep. Prog. Phys.*, vol. 44, pp. 481-532, 1981.

[6] A. van der Ziel, "Unified presentation of 1/*f* noise in electronic devices: fundamental 1/*f* noise sources", *Proc. IEEE*, vol.76, pp. 233-258, 1988.

[7] Special issue of *IEEE Trans. Electron Devices* vol. 41, Nov. 1994.

[8] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, 1996.

[9] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *IEEE J. Solid-State Circuits*, vol. 35, pp. 326-336, 2000.

[10] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, "1/*f* noise and radiation effects in MOS devices," *IEEE Trans. Electron Dev.,* vol. 41, pp. 1953-1964, 1994.

[11] T. L. Meisenheimer and D. M. Fleetwood, "Effect of radiation-induced charge on 1/*f* noise in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 37, pp. 1696-1702, 1990.

[12] J. H. Scofield, T. P. Doerr, and D. M. Fleetwood, "Correlation between preirradiation 1/*f* noise and postirradiation oxide-trapped charge in MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 1946-1953, 1989.

[13] T. L. Meisenheimer, D. M. Fleetwood, M. R. Shaneyfelt, and L. C. Riewe, "1/*f* noise in n-channel and p-channel MOS devices through irradiation and annealing," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1297-1303, 1991.

[14] D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, L. C. Riewe, "Effects of oxide traps, interface traps, and border traps on metal-oxide-semiconductor devices," *J. Appl. Phys.,* vol. 73, pp. 5058-5074, 1993.

[15] D. M. Fleetwood and J. H. Scofield, "Evidence that similar defects cause 1/*f* noise and radiation-induced-hole trapping in metal-oxide-semiconductor transistors," *Phys. Rev. Lett.*, vol.64, pp. 579-582, Jan. 1990.

[16] B. K. Jones, "Electrical noise as a measure of quality and reliability in electronic devices," *Adv. Electron. Electron Phys.*, vol. 87, pp. 201-257, 1993.

[17] L. K. J. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Trans. Electron Devices*, vol. 41, pp. 2176-2187, 1994.

[18] C. Claeys and E. Simoen, "Noise as a diagnostic tool for semiconductor material and device characterization," *J. Electrochem. Soc.*, vol. 145, pp. 2058-2067, 1998.

[19] Z. H. Fang, S. Christoloveanu, and A. Chovet, "Analysis of hot-carrier-induced aging from *1/f* noise in short-channel MOSFET's," *IEEE Electron Device Lett.*, vol. 7, pp. 371-373, 1986.

[20] C. H. Cheng and C. Surya, "The effect of hot-electron injection on the properties of flicker noise in n-channel MOSFET's," *Solid State Electron.*, vol. 36, pp. 475-479, 1993.

[21] P. K. Hurley, E. Sheehan, S. Moran, and A. Mathewson, "The impact of oxide degradation on the low-frequency (*1/f*) noise behavior of p-channel MOSFET," *Microelectron. Reliab.*, vol 36, pp. 1679-1682, 1996.

[22] J. M. Pimbley and G. Gildenblat, "Effect of hot-carrier stress on low frequency MOSFET noise," *IEEE Electron Device Lett.*, vol. 5, pp. 345-347, 1984.

[23] M. Aoki and M. Kato, "Hole-induced *1/f* noise increase in MOS transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 118-120, 1996.

[24] J. P. Xu, P. T. Lai, and Y. C. Cheng, "Dynamic-stress-induced enhanced degradation of *1/f* noise in n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 47, pp. 109-112, 2000.

[25] E. Simoen and C. Claeys, "Reliability aspects of the low-frequency noise behaviour of submicron CMOS technologies," *Semicond. Sci. Technol.*, vol. 14, pp. 61-71, 1999.

[26] E. Simoen, P. Vasina, J. Sikula, and C. Claeys, "Empirical model for the low-frequency noise of hot-carrier degraded submicron LDD MOSFETs," *IEEE Electron Device Lett.*, vol. 18, pp. 480-482, 1997.

[27] L. Ren, S. Okhonin, and M. Ilegems, in "Proceedings of the 14th Int. Conf. On Noise in Physical Systems and *1/f* Fluctuations," (C. Claeys and E. Simoen, Eds.) p. 253. World Scientific, Singapore, 1997.

[28] L. Ren, S. Okhonin, M. Ilegems, "Low frequency noise in electrically stressed n-MOSFETs," *Solid State Electron.*, vol. 43, pp. 849-856, 1999.

[29] J. P. Xu, P. T. Lai, and Y. C. Cheng, "*1/f* noise in n-channel metal-oxide-semiconductor field-effect transistors under different hot-carrier stresses," *J. Appl. Phys.,* vol. 86, pp. 5203-5206, 1999.

[30] R. Brederlow, W. Weber, D. Schmitt-Landsiedel, and R. Thewes, "Hot-carrier degradation of the low-frequency noise in MOS transistors under analog and RF operating conditions," *IEEE Trans. Electron Devices*, vol. 49, pp. 1588-1596, 2002.

[31] F. Dieudonne, S. Haendler, J. Jomaah, and F. Balestra, "Low frequency noise and hot-carrier reliability in advanced SOI MOSFETs," *Solid State Electron.*, vol. 48, pp. 985-997, 2004.

[32] Y. J. Song, J. W. Lim, B. Mheen, S. H. Kim, H. C. Bae, J. Y. Kang, J. H. Kim, J. I. Song, K. W, Park, K. H. Shim, "*1/f* noise in $Si_{0.8}Ge_{0.2}$ pMOSFETs under Fowler-Nordheim stress," *IEEE Trans. Electron Dev.*, vol. 50, pp. 1152-1156, 2003.

[33] G. B. Alers, K. S. Krisch, D. Monroe, B. E. Weir, and A. M. Chang, "Tunneling current noise in thin gate oxides," *Appl. Phys. Lett,* vol. 69, pp. 2885-2887, 1996.

[34] M. Depas, T. Nigam, and M. M. Heyns, "Soft breakdown of ultra-thin gate oxide layers," *IEEE Trans. Electron Dev.*, vol. 43, pp. 1499-1504, 1996.

[35] N. Vandewalle, M. Ausloos, M. Houssa, P. W. Mertens, and M. M. Heyns, "Non-Gaussian behavior and anticorrelations in ultrathin gate oxides after soft breakdown," *Appl. Phys. Lett,* vol. 74, pp. 1579-1581, 1999.

[36] M. J. Chen, T. K. Kang, Y. H. Lee, C. H. Liu, Y. J. Chang, and K. Y. Fu, "Low-frequency noise in n-channel metal-oxide-semiconductor field-effect transistors undergoing soft breakdown," *J. Appl. Phys.,* vol. 89, pp. 648-653, 2001.

[37] D. K. Schroder and J. A. Babcock, "Negative bias temperature instabilities: road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.,* vol. 94, pp. 1-18, 2003.

[38] H. S. Momose, T. Ohguro, K. Kojima, S. I. Nakamura, and Y. Toyoshima, "1.5-nm gate oxide CMOS on (110) surface-oriented Si substrate," *IEEE Trans. Electron Dev.*, vol. 50, pp. 1001-1008, 2003.

[39] S. Cristoloveanu and S. S. Li, *Electrical Characterization of Silicon On Insulator Materials and Devices.* Boston: Kluwer, 1995.

[40] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI, 2nd ed.* Boston: Kluwer, 1997.

[41] G. K. Celler, *Silicon-on-Insulator Structures: Fabrication, The Encyclopedia of Advanced Materials.* New York: Pergamon, 1994.

[42] A. Vandooren, D. Jovanovic, S. Egley, M. Sadd, B.-Y. Nguyen, B. White, M. Orlowski, and J. Mogab, "Scaling assessment of fully-depleted SOI technology at the 30 nm gate length generation," *IEEE International SOI Conference, Williamsburg,* pp. 25-26, 2002.

[43] J. G. Fossum, V. P. Trivedi, and K. Wu, "Extremely scaled fully depleted SOI CMOS," *IEEE International SOI Conference, Williamsburg,* pp. 135-136, 2002.

[44] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 522-538, Jun. 2003.

[45] T. Elewa, B. Boukriss, H. S. Haddara, A. Chovet, and S. Cristoloveanu, "Low-frequency noise in depletion-mode SIMOX MOS transistors," *IEEE Trans. Electron Dev.*, vol. 38, 323-327, 1991.

[46] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, and C. Claeys, "Back and front interface related generation-recombination noise in buried-channel SOI pMOSFET's," *IEEE Trans. Electron Dev.*, vol. 43, 417-423, 1996.

[47] D. S. Ang, Z. Lun, C. H. Ling, "Generation-recombination noise in the near fully depleted SIMOX SOI n-MOSFET-physical characteristics and modeling," *IEEE Trans. Electron Dev.*, vol. 50, 2490-2498, 2003.

[48] J. Chen, P. Fang, R. Solomon, T. Chan, P. Ko, and C. Hu, "Interface quality of sOI MOSFET's reflected in noise and mobility," *Proc. Of the 1991 Int. SOI Conf.*, pp 100-101. The IEEE, New York, 1991.

[49] J. A. Felix, D. M. Fleetwood, R. D. Schrimpf, J. G. Hong, G. Lucovsky, J. R. Schwank, and M. R. Shaneyfelt, "Total-dose radiation response of hafnium-silicate capacitors," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3191-3196, Dec. 2002.

[50] J. A. Felix, M. R. Shaneyfelt, D. M. Fleetwood, T. L. Meisenheimer, J. R. Schwank, R. D. Schrimpf, P. E. Dodd, E. P. Gusev, and C. D'Emic, "Radiation-induced charge trapping in thin Al_2O_3/SiOxNy/Si(100) gate dielectric stacks," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 1910-1918, Dec. 2003.

[51] M. Fadlahhah, A. Szewczyk, C. Giannakopoulos, B. Cretu, F. Monsieur, T. Devoivre, J. Jomaah, and G. Ghibaudo, "Low frequency noise and reliability properties of 0.12 μm CMOS devices with Ta_2O_5 as gate dielectrics," *Microelectron. Reliab.,* vol. 41, pp. 1361-1366, 2001.

[52] W. B. Davenport and W. L. Root, *An introduction to the theory of random signals and noise.* New York, McGraw-Hill, 1958.

[53] A. Ambrozy, *Electronic Noise.* New York: McGraw-Hill, 1982.

[54] A. van der Ziel, *Noise in solid state devices and circuits.* New York: John Wiley & Sons, 1986.

[55] A. A. Balandin, *Noise and fluctuations control in electronic devices.* American Scientific Publishers, 2002.

[56] J. J. Simonne, G. Blasquez, and G. Barbottin, "1/*f* noise in MOSFETs," in *Instabilities in Silicon Devices: Silicon Passivation and Related Instabilities*, vol. 2, (Elsevier, Amsterdam, 1989), pp. 639-657.

[57] S. Christensson, I. Lundstrom, and C. Svensson, "Low frequency noise in MOS transistors," *Solid-State Electronics*, vol. 11, pp. 797-812, 1968.

[58] F. Berz, "Theory of low frequency noise in Si MOSTs," *Solid-State Electronics*, vol. 13, pp. 631-647, 1970.

[59] S. T. Hsu, "Surface state related 1/f noise in MOS transistors," *Solid-State Electronics,* vol. 13, pp. 1451-1459, 1970.

[60] A. van der Ziel, "Flicker noise in electronic devices," in *Advances in Electronics and Electron Physics*, vol. 49, edited by Martin and Martin (Academic Press, New York, 1979), pp. 225-297.

[61] G. Blasquez and A. Boukabache, "Origins of 1/f noise in MOS transistors," in *Noise in Physical Systems and 1/f Noise*, edited by H. Savelli, G. Lecoy, and J. P. Nougier (Elsevier, Amsterdam, 1983), pp. 303-306.

[62] Zeynep Celik and T. Y. Hsiang, "Study of 1/f noise in n-MOSFETs: linear regime," *IEEE Trans. Electron. Dev.,* vol. 32, pp. 2797-2801, 1985.

[63] O. Jantsch and B. Borchert, "Determination of interface state density especially at the band edges by noise measurements on MOSFETs," *Solid-State Electronics,* vol. 30, pp. 1013-1015, 1987.

[64] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron. Dev.,* vol. 37, pp. 654-665, 1990.

[65] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, " A physical-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron. Dev.,* vol. 37, pp. 1323-1333, 1990.

[66] F. B. McLean and T. R. Oldham, “Basic mechanisms of radiation effects in electronic materials and devices,” Harry Diamond Laboratories technical report, No. HDL-TR-2129, September 1987.

[67] J. R. Schwank, “Basic mechanisms of radiation effects in the natural space environment,” *IEEE NSREC Short Course*, pp. 1-109, 1994.

[68] J. R. Schwank, “Total dose effects in MOS devices,” *IEEE NSREC Short Course*, pp. 1-123, 2002.

[69] A. J. Lelis, H. E. Boesch, Jr., T. R. Oldham, and F. B. McLean, “Reversibility of trapped hole annealing,” *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1186-1191, Dec. 1988.

[70] A. J. Lelis, T. R. Oldham, H. E. Boesch, Jr., and F. B. McLean, “The nature of the trapped hole annealing process,” *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 1808-1815, Dec. 1989.

[71] A. J. Lelis and T. R. Oldham, “Time dependence of switching oxide traps,” *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1835-1843, Dec. 1994.

[72] T. R. Oldham and F. B. McLean, “Total ionizing dose effects in MOS oxides and devices,” *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 483-499, June 2003.

[73] F. J. Feigl, W. B. Fowler, and K. L. Yip, “Oxygen vacancy model for the E_1' center in SiO_2,” *Solid State Commun.,* vol. 14, p. 225, 1974.

[74] P. M. Lenahan and P. V. Dressendorfer, “Hole traps and trivalent silicon centers in metal/oxide/silicon devices,” J. Appl. Phys., vol. 55, pp. 3495-3499, 1984.

[75] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, “Physical mechanisms contributing to device “Rebound,” *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1434-1438, Dec. 1984.

[76] J. H. Scofield, M. Trawick, P. Klimecky, and D. M. Fleetwood, “Correlation between preirradiation channel mobility and radiation-induced interface-trap charge in metal-oxide-semiconductor transistors,” *Appl. Phys. Lett,* vol. 58, pp. 2782-2784, 1991.

[77] J. H. Scofield, N. Borland, and D. M. Fleetwood, "Reconciliation of different gate-voltage dependencies of 1/*f* noise in *n* and *p*MOS Transistors," *IEEE Trans. Electron Dev.*, vol. 41, 1946-1952, 1994.

[78] H. D. Xiong, D. M. Fleetwood, B. K. Choi and A. L. Sternberg, “Temperature dependence and irradiation response of 1/*f*-noise in MOSFETs,” *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 2718-2723, 2002.

[79] D. M. Fleetwood, H. D. Xiong, Z.-Y. Lu, C. J. Nicklaw, J. A. Felix, R. D. Schrimpf, and S. T. Pantelides, “Unified model of hole trapping, 1/*f* noise, and thermally stimulated current in MOS devices,” *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 2674-2683, Dec. 2002.

[80] T. H. Ning, C. M. Osburn, and H. N. Yu, "Effect of electron trapping in IGFET characteristics," *J. Electron. Mat.*, vol. 6, 1977.

[81] P. Gentil and S. Chausse, "Low frequency noise measurements on silicon-on-sapphire (SOS) MOS transistors," Solid State Electron., vol. 20, pp.935-940, 1977.

[82] J. Chen, P. Fang, P. K. Ko, C. Hu, R. Solomon, T. Y. Chan, and C. G. Sodini, "Noise overshoot at drain current kink in SOI MOSFET," *Proc. IEEE SOI Conf.*, pp. 40-41, 1990.

[83] E. Simoen and C. Claeys, "Evidence for an alternative, hole-trapping related random telegraph signal mechanism in n-channel silicon-on-insulator metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 62, pp. 876-878, 1993.

[84] E. Simoen, U. Magnusson, A. L. P. Rotondaro, and C. Claeys, "The kink-related excess low-frequency noise in silicon-on-insulator MOSTs," *IEEE Trans. Electron Devices*, vol. 41, pp. 330-339, 1994.

[85] Y.-C. Tseng, W.-L. M. Huang, P. J. Welch, J. M. Ford, and J. C. S. Woo, "Empirical correlation between AC kink and low-frequency noise overshoot in SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 19, pp. 157-159, 1998.

[86] F. Faccio, F. Anghinolfi, E. H. M. Heijne, P. Jarron, and S. Cristoloveanu, "Noise contribution of the body resistance in partially-depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 45, pp. 1033-1038, 1998.

[87] W. Jin, P. C. H. Chan, S. K. H. Fung, and P. K. Ko, "Shot-noise-induced excess low-frequency noise in floating-body partially depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, pp. 1180-1185, 1999.

[88] Y.-C Tseng, W. M. Huang, V. Ilderem, and J. C. S. Woo, "Floating body induced pre-kink excess low-frequency noise in submicron SOI CMOSFET technology, "*IEEE Trans. Electron Device Lett.*, vol. 20, pp. 484-486, 1999.

[89] N. B. Lukyanchikova, M. V. Petrichuk, N. P. Garbar, E. Simoen, and C. Claeys, "Non-trivial GR and 1/*f* noise generated in the p-Si layer of SOI and SOS MOSFETs near the inverted front or buried p-Si/SiO_2 interface," *Semicond. Sci. Technol.*, vol. 14, pp. 775-783, 1999.

[90] G. O. Workman and J. G. Fossum, "Physical noise modeling of SOI MOSFETs with analysis of the Lorentzian component in the low-frequency noise spectrum," *IEEE Trans. Electron Devices*, vol. 47, pp. 1192-1201, 2000.

[91] Y.-C. Tseng, W. M. Huang, M. Mendicino, D. J. Monk, P. J. Welch, and J. C. S. Woo, "Comprehensive study on low-frequency noise characteristics in surface channel SOI CMOSFETs and device design optimization for RF ICs," *IEEE Trans. Electron Devices*, vol. 48, pp. 1428-1437, 2001.

[92] F. Faccio, M. Bianchi, M. Fornasari, E. H. M. Heijne, P. Jarron, G. Rossi, G. Borel, and J. Redolfi, "Noise characterization of transistors in a 1.2 μm CMOS-SOI technology up to a total-dose of 12 Mrad(Si)," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2310-2316, 1994.

[93] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction and valence band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, pp. 1366-1373, 2001.

[94] A. Mercha, J. M. Rafi, E. Simoen, E. Augendre, and C. Claeys, "Linear Kink Effect induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, pp. 1675-1682, 2003.

[95] N. B. Lukyanchikova, M. V. Petrichuk, N. P. Garbar, A. Mercha, E. Simoen, and C. Claeys, "Electron valence-band tunneling-induced Lorentzian noise in deep submicron silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 94, pp. 4461-4469, 2003.

[96] E. Simoen, A. Mercha, J. M. Rafi, C. Claeys, N. B. Lukyanchikova, A. M. Smolanka, and N. P. Garbar, "High-energy proton irradiation induced changes in the linear-kink noise overshoot of 0.10 μm partially depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 95, pp. 4084-4092, 2004.

[97] H. D. Xiong, D. M. Fleetwood, and J. R. Schwank, "Low frequency noise and radiation response of buried oxides in SOI nMOS transistors," *IEE Proc.-Circuits Devices Syst.*, vol. 151, pp. 118-124, 2004.

[98] P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the radiation response of MOS capacitors and transistors," *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1453-1460, Dec. 1984.

[99] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in MOS transistors," *Appl. Phys. Lett.*, vol. 48, pp. 133-135, 1986.

[100] E. P. Gusev, E. Cartier, D. A. Buchanan, M. A. Gribelyuk, M. Copel, H. Okorn-Schmidt, C. D'Emic, "Ultrathin high-κ metal oxides on silicon: processing, characterization and integration issues," Microelectron. Eng. **59**, pp. 341-349, 2001.

[101] J. R. Schwank, D. M. Fleetwood, H. D. Xiong, M. R. Shaneyfelt, and B. L. Draper, "Generation of metastable electron traps in the near interfacial region of SOI buried oxides by ion implantation and their effect on device properties," *Microelectron. Eng.*, vol. 72, pp. 362-366, 2004.

[102] M. L. Green, E.P. Gusev, R. Degrave, and E. Garfunkel, "Ultrathin (< 4 nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: understanding the processing, structure, and physical and electrical limits," *J. Appl. Phys.*, vol. 90, pp. 2057-2121, 2001.

[103] G.D.Wilk, R.M. Wallace, and J.M. Anthony, "High-κ gate dielectrics: current status and materials properties considerations," *J. Appl. Phys., vol.* 89, pp. 5243-5275, 2001.

[104] M. Copel, E. Cartier, E.P. Gusev, S. Guha, N. Bojarczuk, and M. Poppeller, "Robustness of ultrathin aluminum oxide dielectrics on Si(001)," *Appl. Phys. Lett.,* vol.78, pp. 2670-2672, 2001.

[105] S. Guha, E. Cartier, N.A. Bojarczuk, J. Bruley, L. Gignac, and J. Karasinski, "High-quality aluminum oxide gate dielectrics by ultra-high-vacuum reactive atomic-beam deposition," *J. Appl. Phys.*, vol. 90, pp. 512-514, 2001.

[106] Y. Nemirovsky, I. Brouk, and C.G. Jakobson, "1/*f* noise in CMOS transistors for analog applications," *IEEE Trans. Electron Dev.*, vol. 48, pp. 921-927, 2001.

[107] J. N. Burghartz, M. Hargrove, C. S. Webster, R. A. Groves, M. Keene, K. A. Jenkins, R. Logan, and E. Nowak, "RF potential of a 0.18-μm CMOS logic device technology," *IEEE Trans. Electron Dev.*, vol. 47, pp. 864-870, 2000.

[108] Z. Butler and T.Y. Hsiang, "Determination of Si-SiO_2 interface trap density by 1/*f* noise measurements," *IEEE Trans. Electron Dev.*, vol. 35, pp. 1651-1655, 1988.

[109] C. Surya and T.Y. Hsiang, "A thermal-activation model for $1/f^{\gamma}$ noise in Si-MOSFETs," *Solid-St. Electron.*, vol. 31, pp. 959-964, 1988.

[110] M. Da Rold, E. Simoen, S. Mertens, M. Schaekers, G. Badenes, and S. Decoutere, "Impact of gate oxide nitridation process on 1/*f* noise in 0.18 μm CMOS," *Microelectron. Reliab.,* vol. 41, pp. 1933-1938, 2001.

[111] N. Lukyanchikova, M. Petrchuk, N. Garbar, E. Simoen, A. Mercha, C. Claeys, H. van Meer, and K. De Meyer, "The $1/f^{1.7}$ noise in submicron SOI MOSFETs with 2.5 nm nitrided gate oxide," *IEEE Trans. Electron Dev.*, vol. 49, pp. 2367-2370, 2002.

[112] J. M. Benedetto, and H.E. Boesch Jr., "The relationship between Co-60 and 10-keV X-ray-damage in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 33, pp. 1318-1323, Dec. 1986.

[113] M.R. Shaneyfelt, D.M. Fleetwood, J.R. Schwank, and K.L. Hughes, "Charge yield for Co-60 and 10-keV X-ray irradiation of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1187-1194, Dec. 1991.

[114] V.V. Afanas'ev, A. Stesmans, B.J. Mrstik, and C. Zhao, "Impact of annealing-induced compaction on electronic properties of atomic-layer-deposited Al_2O_3," *Appl. Phys. Lett.*, vol. 81, pp. 1678-1680, Aug. 2002.

[115] W.L. Warren, M.R. Shaneyfelt, D.M. Fleetwood, J.R. Schwank, P.S. Winokur, and R.A.B. Devine, "Microscopic nature of border traps in MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1817-1827, Dec. 1994.

[116] R. E. Stahlbush, G. J. Campisi, J. B. McKitterick, W. P. Maszara, P. Roitman, and G. A. Brown, "Electron and hole trapping in irradiated SIMOX, ZMR and BESOI buried oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 2086-2097, Dec. 1992.

[117] W. L. Warren, M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, R. A. B. Devine, W. P. Maszara, and J. B. McKitterick, "Paramagnetic defect centers in BESOI and SIMOX buried oxide," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1755-1764, Jun. 1993.

[118] B. J. Mrstik,. H. L. Hughes, P. J. McMarr, R. K. Lawrence, D. I. Ma, I. P. Isaacson, and R. A. Walker, "Hole and electron trapping in ion implanted thermal oxides and SIMOX," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2189-2195, Dec. 2000.

[119] B. J. Mrstik, H. L. Hughes, P. J. McMarr, and P. Gouker, "Electron and hole trapping in thermal oxides that have been ion implanted," *Microelectron. Eng.*, vol. 59, pp. 285-289, 2001.

[120] B. J. Mrstik, H. L. Hughes, P. Gouker, R. K. Lawrence, and P. J. McMarr, "The role of nanoclusters in reducing hole trapping in ion implanted oxides," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 1947-1953, Dec. 2003.

[121] C. J. Nicklaw, M. P. Pagey, S. T. Pantelides, D. M. Fleetwood, R. D. Schrimpf, K. F. Galloway, J. E. Wittig, B. M. Howard, E. Taw, W. H. McNeil, and J. F. Conley, Jr., "Defects and nanocrystals generated by Si implantation into a-SiO_2," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2269-2275, Dec. 2000.

[122] J. H. Scofield and D. M. Fleetwood, "Physical basis for nondestructive tests of MOS radiation hardness," *IEEE Trans. Nucl. Sci.*, vol. 38, pp. 1567-1577, Dec. 1991.

[123] H. Neitzert, M. Offenberg, and P. Balk, "Hole capture in SiO_2 films after ion implantation," *Appl. Surf. Sci.*, vol. 30, pp. 272-277, 1987.

[124] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*. New York: Wiley-Interscience, 1989.

[125] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides, Advances in Solid State Electronics and Technology (ASSET) Series*. Singapore: World Scientific, 1999.

[126] J. A. Felix, H. D. Xiong, D. M. Fleetwood, E. P. Gusev, R. D. Schrimpf, A. L. Sternberg, and C. D'Emic, "Interface trapping properties of nMOSFETs with Al_2O_3/SiOxNy/Si(100) gate dielectric stacks after exposure to ionizing radiation," *Microelectron. Eng.*, vol. 72, pp. 50-54, 2004.

[127] H.D. Xiong, D.M. Fleetwood, J.A. Felix, E.P. Gusev, and C. D'Emic, "Low frequency noise and radiation response of metal-oxide-semiconductor transistors with Al_2O_3/SiOxNy/Si(100) gate dielectrics," *Appl. Phys. Lett,* vol. 83, pp. 5232-5234, Dec. 2003.

[128] D. J. Wouters, M. R. Tack, G. V. Groeseneken, H. E. Maes, and C. L. Claeys, "Characterization of front and back Si-SiO_2 interfaces in thick-film and thin-film silicon-on-insulator MOS structures by the charge-pumping technique," *IEEE Trans. Electron Dev.*, vol. 36, pp. 1746-1750, Sep. 1989.

[129] J. A. Martino, E. Simoen, C. L. Claeys, "A new method for determining the front and back interface-trap densities of accumulation-mode SOI MOSFETs at 77 K," *Solid State Electron.*, vol. 38, pp. 1799-1803, 1995.

[130] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion – a new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. 8, pp. 410-412, Sep. 1987.

[131] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *J. Appl. Phys.,* vol. 93, pp. 4955-4978, May 2003.

[132] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately thin double-gate SOI MOSFETs," *IEEE Trans. Electron Dev.*, vol. 50, pp. 830-838, March 2003.

[133] E. Simoen, A. Mercha, C. Claeys, N. Lukyanchikova, and N. Garbar, "Critical discussion of the front-back gate coupling effect on the low-frequency noise in fully depleted SOI MOSFETs," *IEEE Trans. Electron Dev.*, vol. 51, pp. 1008-1016, June 2004.

[134] R. A. B. Devine , W. L. Warren, J. B. Xu, I. H. Wilson, P. Paillet, and J. L. Leray, "Oxygen gettering and oxide degradation during annealing of Si/SiO_2/Si structures," *J. Appl. Phys.*, vol. 77, pp. 175-186, 1995.

[135] B. Jun, H. D. Xiong, C. R. Cirba, R.D. Schrimpf, D.M. Fleetwood, and S. Cristoloveanu, "Total dose effects on double gate operated fully depleted SOI transistors**,"** *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, accepted for publication, Dec. 2004.

[136] H. K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator SOI MOSFETs," *IEEE Trans. Electron Dev.*, vol. 30, pp. 1244-1251, 1983.

[137] D.M. Fleetwood, L.C. Riewe, J.R. Schwank, S.C. Witczak and R.D. Schrimpf, "Radiation effects at low electric fields in thermal, SIMOX, and bipolar-base oxides," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2537-2546, Dec. 1996.

[138] H.E. Boesch Jr. and T. L. Taylor, “Time-dependent radiation-induced charge effects in wafer-bonded SOI buried oxides,” *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 2103-2113, Dec. 1992.

[139] H. E. Boesch Jr., T. L. Taylor, L. R. Hite, and W. E. Bailey, “Time-dependent hole and electron trapping effects in SIMOX buried oxides,” *IEEE Trans. Nucl. Sci.*, vol. 37, pp. 1982-1989, Dec. 1990.

[140] D. M. Fleetwood, S. L. Miller, R. A. Reber, Jr., P. J. McWhorter, P. S. Winokur, M. R. Shaneyfelt, and J. R. Schwank, "New insights into radiation-induced oxide-trap charge through TSC Measurement and Analysis," *IEEE Trans. Nucl. Sci*. vol. 39, pp. 2192-2203, Dec. 1992.

[141] D. M. Fleetwood, P.S. Winkur, M. R. Shaneyfelt, L.C. Riewe, O. Flament, P Paillet, and J. L. Leray, "Effects of isochronal annealing and irradiation temperature on radiation-induced trapped charge," *IEEE Trans. Nucl. Sci*., vol. 45, 2366-2374, Dec. 1998.

[142] D. M. Fleetwood, T. Postel, and N. Giordano, "Temperature dependence of the 1/*f* noise of carbon resistors," *J. Appl. Phys.*, vol. 56, pp. 3256-3260, 1984.

[143] J.H. Scofield and W.W. Webb, "Resistance Fluctuations due to hydrogen diffusion in Niobium thin films," *Phys. Rev. Lett.,* vol. 54, pp.352-356, 1985.

[144] J.H. Scofield, J.V. Mantese, and W.W. Webb, "Temperature dependence of noise processes in metals," *Phys. Rev. B,* vol. 34, pp. 723-731, 1986.

[145] N.M. Zimmerman and W.W. Webb, "Microscopic Scatterer Displacements Generate the 1/f resistance noise of H in Pd,” *Phys. Rev. Lett.,* vol. 61, pp.889-892, 1988.

[146] N.M. Zimmerman and W.W. Webb, "1/f resistance noise complements anelasticity measurements of hydrogen motion in amorphous $Pd_{80}Si_{20}$," *Phys. Rev. Lett.,* vol. 65, pp.1040-1043, 1990.

[147] K. Vanheusden, W. L. Warren, R. A. B. Devine, D. M. Fleetwood, J. R. Schwank, M. R. Shaneyfelt, P. S. Winokur, and Z. J. Lemnios, “Nonvolatile memory device based on mobile protons in SiO_2 thin films,” *Nature* 386, 587-589, 1997.

[148] W. L. Warren, D. M. Fleetwood, J. R. Schwank, M. R. Shaneyfelt, B. L. Draper, P. S. Winokur, M. G. Knoll, K. Vanheusden, R. A. B. Devine, L. B. Archer, and R. M. Wallace, “Protonic nonvolatile field effect transistor memories in $Si/SiO_2/Si$ structures,” *IEEE Trans. Nucl. Sci.* 44, 1789-1798, 1997.

[149] K. Vanheusden, R. A. B. Devine, J. R. Schwank, D. M. Fleetwood, R. G. Polcawich, W. L. Warren, S. P. Karna, and R. D. Pugh, “Irradiation response of mobile protons in buried SiO_2 films,” *IEEE Trans. Nucl. Sci.* 44, 2087-2094, 1997.

[150] D. M. Fleetwood, M. J. Johnson, T. L. Meisenheimer, P. S. Winokur, W. L. Warren, and S. C. Witczak, "1/*f* noise, hydrogen transport, and latent interface-trap buildup in irradiated MOS devices," *IEEE Trans. Nucl. Sci.* 44, 1810-1817, 1997.