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Design of Low Power SRAM Cell Using 10Transistors

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Abstract
The primary aim of electronics is to design low power devices due to the frequent usage of powered widget. The memory cell operation containing low voltage consumption hasbecome a major interest in designing of memory cells due to its applications in very low energy computing.Due to specification modifications in scaled methodologies, the only critical method isstable operation of SRAM for the success of low voltage design of SRAM. Along with the power and voltage consumption, due to unwanted switching actions of transistors, the access time of the SRAM is also considered as a complex parameter and it is used for different blocks like, designed SRAM cell, access transistors, pre-charge circuit, decoders and sense amplifiers.The conventional 6T SRAM are unable toachievethe less delay and sub threshold operation. The proposed design is designed by using the sleep transistor circuits. The sleep transistor circuits are turned to be ON in active state and in OFF state during passive state.A supply voltage of 1.8V is used which enough for low power applications in energy computing. The designed SRAM cell has conducting pMOS circuit, which can also reduces the total power dissipation. The designed 10T SRAM cell reduces 40.56% of total power and 17.86% of total delay compared with the conventional 6T SRAM cell.The structured SRAM cell is reproduced by utilizing Cadence device of 180nm innovation.

Keywords: *Conducting pMOS, Sleep Transistor, SRAM,*

INTRODUCTION

Very Large Scale Integration (VLSI) is defined as a single chip integrated circuit consist of transistors and it is a single silicon chip containing the collections of gates fabricated. In VLSI chips, the power consumption has increased constantly. Moore'slaw states that VLSI method is used to increases inclock frequencies and transistor density continuously. The VLSI trend technology scaling in the few years show that40% increase in number of on chip in transistors and 30% increase in frequency operation of VLSI systems. The supply voltage and capacitance scale down the VLSI chips power consumptions and it is increasing continuously. For the high performance VLSI chip design, back end and front end methodology has an important impact on the design time, design power, design speed, design delay and design cost.

EXISTING METHOD - 6T SRAM

A low power 6T SRAM cell is designed by using two cross coupled CMOS inverters. The main advantage of the circuit is that static power dissipation issmall and it is limited by the leakagecurrent [13]. Because of high noise margin, the existing circuit has high noise immunity. The word lines are activated for the read and write operations. The SRAM cells are connected with the bit cells sothat, the access transistors are turned to be in ON state [20]. The information that is stored in the cell doesn't get destroyed by the read operation. This circuit can operate in low voltage power supply. The inverter of the CMOS circuits are in back to back connections in the memory cell SRAM design and they areprovided with

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two access transistors at the end. The size of the cells in the circuit is larger in size. The cell allows the modified information that is stored during write operation.

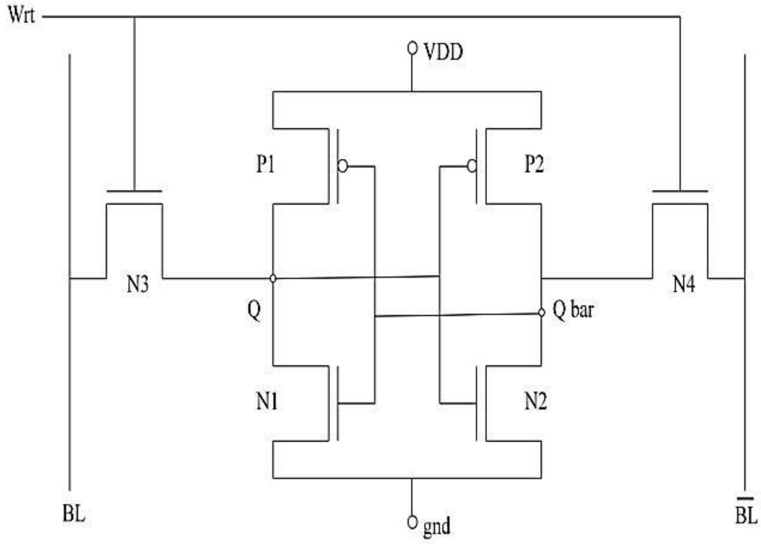

Figure 1: *Circuit diagram of 6T SRAM.*

The basic SRAM is shown in the above Fig.1.To perform the both read stability and write stability, the nMOS act as pull down transistor in the cross coupled inverters and it has the current carrying capacity as high, the access transistors has the strength as higher and the pMOS act as pull up transistors and it is weak.The bit lines are connected with the access transistors N3 and N4 [9]. In this circuit, two inverter circuits are connected as crossly and coupled called as cross coupled inverters. The access transistors are always in ON state by connecting them with the write line by providing write line as 1.The Q and Qbar are termed as output terminals.

PROPOSED METHOD - 10T SRAM

The designed 10T SRAM cell contains two access transistors, three sleeping transistors, two conducting PMOS circuits and one inverting circuit. The designed 10T SRAM cell using sleep circuit and conducting pMOS is shown in Fig. 2.

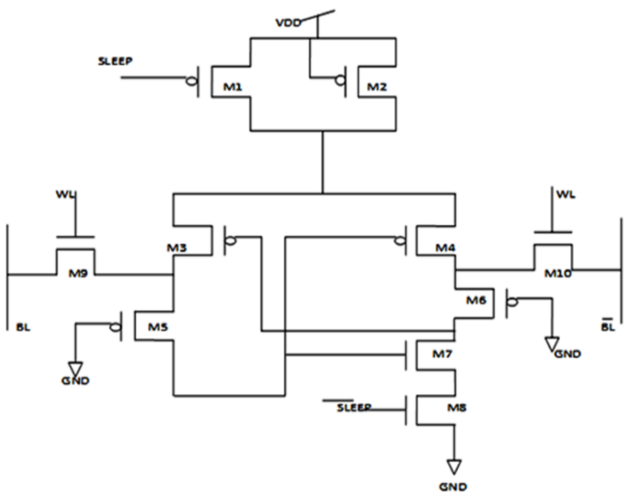

Figure 2: *Circuit diagram of 10T SRAM.*

Operation of conducting pMOS

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The conducting pMOS circuits have both read and write operations. In the read operation, word line is activated and the external word line driver is said to be disabled. The value can be determined by using the external logic [25]. The bit lines B and Bbar of the cell are pre-charged in the write operation.In the read mode, the bit lines will disturb the charges that are stored in the internal nodes, and if the inverters are not strong and that the bit line does not discharge to the expected values.The unbroken connection path is from ground to theoutput node. During the write mode of operation, the access transistors are enabled by applying word line signal WL equal to'1' to the gates [6]. When data '0' is to be written to storage node storing '1', the corresponding bit line is applied with voltage equal to '0', resultingin a current flow through pull up device to the bit line through the storage node storing high, which is pulled low [11]. The unbroken connection path is from ground to output node.

Operation of sleep transistor

A sleep transistor can be either a pMOS or nMOS of having high threshold voltage transistor [5]. They are used as switch inorder to shutdown the power supplies to the designed circuits in the standby mode of SRAM operations.

When the logic is said to be 1,during the active mode of operation the nMOS transistor will be in conducting mode and the pMOS transistor is in off state [16]. The sleep transistor circuit connects the power supply with the SRAM cell circuit. The sleep transistors are used as switches.They are header switches and footer switches. The header switches are connected with the V_{dd} and the footer switches are connected with the ground. The circuits are in ON state during the active mode of operation of the SRAM cell and the circuit are in OFF state during the idle mode of operation and it is also called as standby mode of operations. The stability of the circuit gets increased due to sleep transistors [4]. It reduces the unwanted switching. So, the power of designed circuit gets reduced.

Read operation of 10T SRAM cell

In the read operation, the external drivers' access transistors operate the bit lines in the circuits. The input data that are provide to the input terminals will allow the data to enter into the main cell of the SRAM design [3]. When the write line is high, it will turn on the access transistors and it will be in active state. In read operation, the circuit reads the data in the output terminals that are provided in the input terminals. The output can be read by the sense amplifier in the circuit [23], [10].

Write operation of 10T SRAM cell

In the write operation, the bit lines are operated by the external drivers. The previous state of the cross-coupled inverters can be easily over writes because of the internal driver and it is smaller than the external drivers of the circuit. The word line of the transistors will shift the data, and the short-circuit will occurs. The transistors N3 and N4 are enabled by providing the word line signal as '1' to the transistors [27]. The data is to be written into the cell. The inverse should take place when the node voltage is '0'and the value'1' is to be written in the cell.When data '0' is to be written to storage node as '1', the bit-line will be provided with the voltage equal to '0',and there is a current flow through the pull up device.

SIMULATION RESULTS

Schematic in Cadence tool

In this SRAM design, the Cadence tool is used for the analysis of circuits in VLSI technology. It has the technology parameter of 180nm. The circuits are drawn on the screen by dragging them from the libraries and they are connected with the wires. The input and output terminals are selected and the input and output pins are connected with the terminals [17]. The supply voltage of 1.8V is provided separately by connecting them with the V_{dd} and the ground.

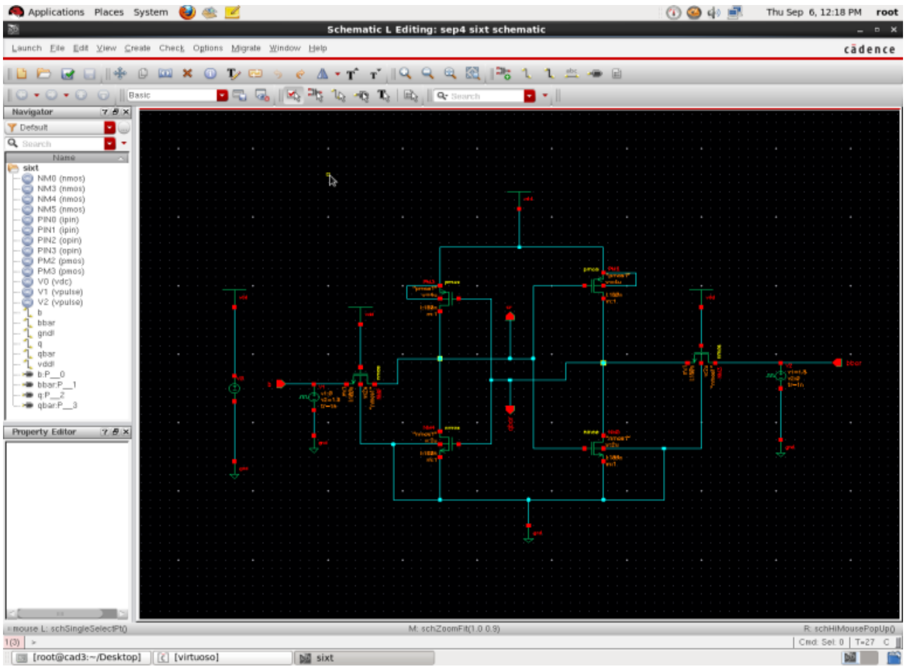

Figure 3: *Schematic of basic 6T SRAM cell.*

The above Fig. 3 shows the schematic of basic 6T SRAM cell. The above design contains two pass transistors or two access transistors and two cross coupledcMOS inverting circuits provided with V_{pulse}. The B and B bar nodes acts as input nodes[12].

The access transistors are turned on whenever a word line is activated for read or write operation, connecting the cell to the complementary bit line columns. The output can be taken from Q and Q bar nodes.

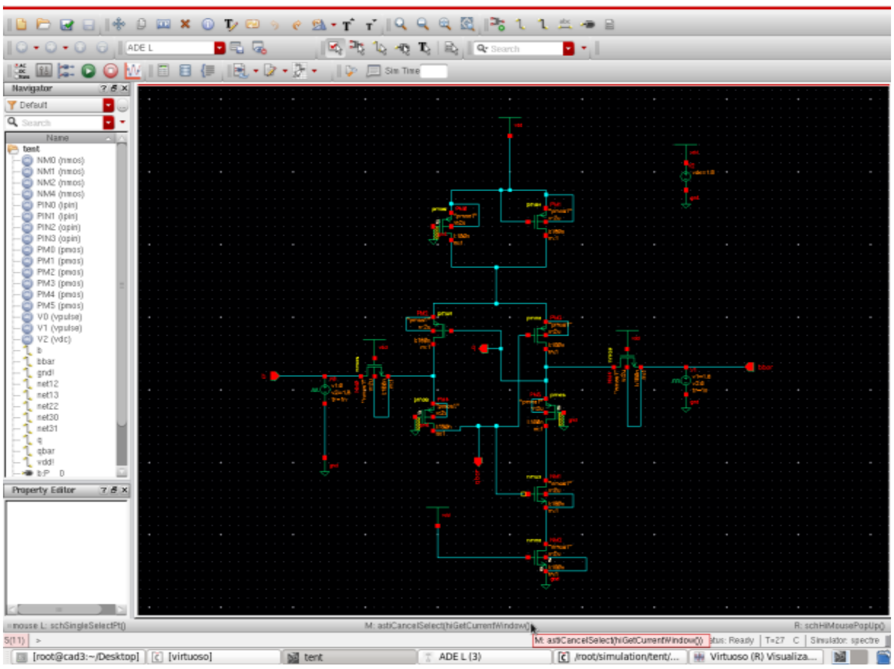

Figure 4: *Schematic of designed 10T SRAM cell.*

The Fig. 4 shows the schematic of designed 10T SRAM cell. The above design contains two access or pass transistors, two sleep transistors, two conducting pMOS transistors and one inverting circuits provided with V_{pulse}. The sleep transistor reduces the short circuit power consumption [8]. The sleep transistors are connected at the header and footer of the circuit. The inverting circuit is replaced by conducting pMOScircuit. So here there is only one inverting circuit is present. The circuit are simulated using the 180nm technology.

Output waveform

The output waveforms are drawn for the nodes B, Bbar, Q and Qbar. The four different node outputs are shown in the below Fig. 5. It shows that the B and Qbar values are in inversion manner and similarly Bbar and Q arein inversion manner.

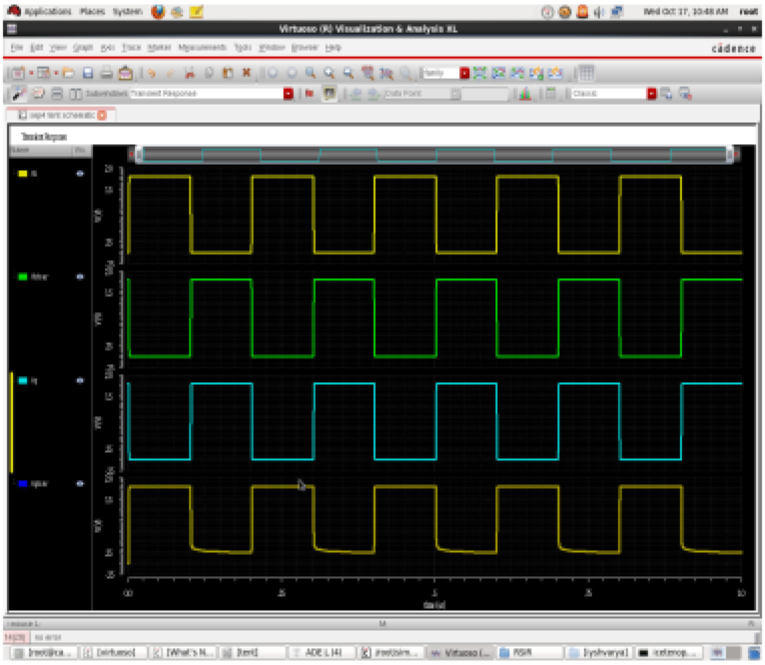

Figure 5: *Output waveform of 10T SRAM.*

The designed 10T SRAM design having the time delay that occurs between the B and Qbar and also between the Bbar and Q and they are reduced by using sleep transistor and conducting pMOS, that are shown in the output waveform of the designed 10TSRAM design [7].The output can be obtained by using 180nm technology. Whenever a word line is activated for read or write and thatthe access transistors are turned to be in ON state.In the read output, whenever the external word line driver is disabled the corresponding word line said to be in active mode. The value that are produced can be determined by external bit lines of the cell that are to be pre-charged. The data to be written into the cell [15]. The access transistors are enabled by applying word line signal to the transistors by providing the strong 1. When data '0' is to be written to the data note it stores '1' and the bit-line is applied with voltage valuethat are equal to '0', The inverse can be takes place when thestorage voltage is '0' and it can be written as '1'.

Delay and power of basic 6T SRAM

Delay and power consumption of the basic 6T SRAM design are designed using cadence.It shows the delay between Q and B bar line as well as B and Q bar lines i.e., bit line input to bit line output on both ways as the input andoutput of the cross coupled inverters in the SRAM cell [19]. Here delay of the active transistors is calculated. The delay is increased due to the presence of two cross coupled inverters and the delay of the conventional 6T SRAM is measured as 355ns across the voltage source using cadence tool. The power consumed by the circuit of 6T SRAM is measured as 812µW using cadence tool.Delay of theconventional6TSRAMismeasuredas322 ns using the cadence tool.

Delay and power of designed 10T SRAM

Delay and power consumption of designed 10T SRAM design are designed using cadence tool. The delay is calculated between Q and B bar line as well as B andQ bar lines of the conducting pMOS and inverting circuit in the SRAM cell [17]. In the proposed delay, the header and footer circuits are not involved due to the usage of sleep transistor circuits. It reduces the unwanted switching activities. The SRAM cell will beactive during the active mode only. So the delay of the designed circuit is reduced and then the delay of the designed 10T SRAM is measured as 144ns using cadence tool.In the proposed design the180 nm technology is used. The power consumed by the circuit is primarily due to the current drawn from the power supply [28]. Here, conductingpMOS are used instead of inverting circuit. The conductingpMOS are used to provide strong one and strong zero. So the unwanted power supply to the transistors are get reduced and then the power of the designed 10T SRAM is measured as 149µW using cadence tool.Delay of the designed 10T SRAM cell is calculated as 144ns and power consumption of the same is measured as 149µW using cadence tool.

In order to analyze the improvement in the designed 10T SRAM design, thecomparison of the same with the basic 6T SRAM design is needed.

Power and delay using cadence

Table 1: *Comparison table of 6T and 10T SRAM.*

Design	Power	Delay
Basic 6T SRAM	812µW	322ns
Designed 10T SRAM	149µW	144ns

Table 1 shows the power and delay of the basic 6T and designed 10T SRAM design by using cadence tool of 180nm technology.The conventional 6T SRAM cell has the power of 812µW and the designed 10T SRAM cell has the power value of 149µW. The designed 10T SRAM cell power is reduced by 40.56% frombasic 6T SRAM design.The conventional 6T SRAM cell has the delay of 322nsand the designed 10T SRAM cell has the delay value of 144ns. The designed 10T SRAM cell delay is reduced by 17.86% from basic 6T SRAM design.

CONCLUSION

Low power and delay are the primary concerns for better SRAM design. Sleep transistor is used to avoid the power dissipation by preventing the direct path creation between supply and ground. Conducting pMOS circuits are also reduced the static power consumption and also the delay. The designed 10T SRAM cell achieves delay of 144ns and power consumption of 149µW. While, the conventional 6T SRAM cell has delay of 322ns and power consumption of 812µW.

REFERENCES

1. Abdul Quaiyum Ansari, Javed Akhtar Ansari (2015), “Design of 7T SRAM cell for low power applications”, *IEEETransactions on VLSI Systems*, Volume 39, Issue 22, pp. 218−222.
2. Amalraj. K, Sathishkumar. P, Vigneshraja. K, Arunkumar. N, Anjo.

C.A(2012), “Nano scaled low power leakage St- based SRAM”, *IEEE Transactions on Electron Devices*, Vololume 56, Issue 5, pp. 1215−1220.
3. Apoorva Pathak, DivyeshSachan, Harish Peta, Manish Goswami (2016), “AmodifiedSRAMbasedlowpowermemorydesign”, *International Journal of Engineering and Manufacturing,*Volume 2, Issue 5, pp. 1781−1784.
4. Ashish Kumar Sharma (2017), “A novel method for design and implementation of low power high stable SRAM cell”, *International Conference on VLSI Design,*Volume 47, Issue 2, pp. 1218−1223.
5. Chung. Y, Lee. D. Y (2010), “Differential-read symmetrical 8T SRAM bit-cell with enhanced data stability”, *Electronics Letters*, Volume 46, Issue 18, pp. 658−663.
6. DeeptiKanoujia, Vishal Moyal (2014), “Survey on various works done in reducing static power in various SRAM cells”, *International Journal of technology enhancements and emerging engineering research*, Volume 2, Issue 11, pp. 1420−1426.
7. Dhanumjaya. K, Giri Prasad. M. N, Padmaraju. K, Raja Reddy. M (2011), “Design of low power SRAM in 45 nm CMOS technology”, *International Journal of Engineering Research and Applications*, Volume 1, Issue 4, pp.2040−2045.
8. Dinesh Chand Gupta, Ashish Raman (2012), “Analysis of leakage current reduction techniques in SRAM cell in 90nm CMOS technology”, *International Journal of Computer Applications*, Volume 50, Issue 19, pp. 128−134.
9. Gaurav HemantPatil, Irene Susan Jacob, Dada BhagwanSargar, SnehaRevankar (2015), “Design and implementation of SRAM”, *IRF International Conference*, Volume 28, Issue 3, pp. 305−326.
10. Gaurav Kumar,Rajpal Sharma (2014), “Analytical study of sense amplifier”, *International Journal of Advanced Research in Computer Science and Software Engineering*, Volume 4, Issue 5,pp. 365−371.
11. Govind Prasad, GandeBhargav, SrikarDatta (2016), “Novel low power 10T SRAM cell on 90nm CMOS”, *International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics,*Volume 2, Issue 2, pp. 1352−1357.
12. Gyan Prakash, Umesh Dutta, MohdTauheed Khan (2012), “Dynamic power reduction in SRAM”, *International Journal of Engineering Research and Applications*, Volume 2, Issue 5, pp.1781−1784.
13. Hiroki Noguchi, Masahiko Yoshimoto (2008), “Which is the Best Dual Port SRAM in 45-nm Process Technology”, *IEEE Transactions on VLSI Systems*, Volume 41, Issue 3, pp. 1568−1573.
14. IkJoon Chang, Jae-Joon Kim, Sang Phill Park, Kaushik Roy (2009), “A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS”, *IEEE Journal of Solid-state Circuits*, Volume 44, Issue 2.
15. Islam. A,Hasan. M (2012), “Leakage Characterization of 10T SRAM Cell”, *IEEE Transactions on Electron Devices*, Volume 59, Issue 3 pp. 1118−1125.
16. Jagadeesh. C, Nagendra. R, NeelimaKoppala (2013), “Design &analysis of different types of sleepy methods for future technologies”, *International Journal of Engineering Trends and Technology*, Volume 4, Issue 4, pp. 278−283.
17. Kanika Kaur, Anurag Arora (2013), “Performance of low power SRAM cells on SNM and power dissipation”, *International Journal of Emerging Trends & Technology in Computer*

Science, Volume 2, Issue 2, pp. 1352−1357.
18. Ken Martin (2000), "Digital Integrated Circuit Design", *Oxford University Press, Inc.*,Volume 16, Issue 4, pp. 437−452.
19. Kulkarni. J. P, Kim. K, Roy. K (2007), "A 160 mV robust Schmitt trigger based sub threshold SRAM", *IEEE J. Solid-State Circuits*, Volume 42, Issue 10, pp. 2303–2313.
20. KundanVanama, RithwikGunnuthula, Govind Prasad (2014), "Design of low power stable SRAM cell", *International Conference on Circuit, Power and Computing Technologies*. Volume 11, Issue 14, pp. 288−345.
21. Liu. Z,Kursun. V (2008), "Characterization of a novel nine transistor SRAM cell",*IEEE Trans. VLSI Syst*., Volume 16, Issue 4, pp. 488−492.
22. Manish Shrivas, SaimaAyyub,PareshRawat (2015), "Review on Performance of different Low Power SRAM Cell Structures", *International Journal of Computer Applications*, Volume 127,Issue 3, pp. 2318−2323.
23. Meenakshi Thakur, Rajesh Mehra (2016), "An efficient sense amplifier for SRAM using body biasing", *International Journal of Engineering Trends and Technology*, Volume 37, Issue 4, pp. 856−862.
24. Rabaey. J. M, Chandrakasan. A, Nikolic. B (2005), "Digital Integrated Circuits: A Design Perspective", *2nd ed. New Delhi, India: Prentice- Hall*, Volume 6, Issue 34, pp. 95−134.
25. Ravi Dutt and Abhijeet (2012), "Current mode sense amplifier for SRAM memory", *International Journal of Engineering Research& Technology*,Volume 1, Issue 3, pp. 1065−1071.
26. Shiny Grace.P, Sivamangai.N.M (2016), "Design of 10T SRAM cell for high SNM and low power", *International Conference on Devices, Circuits and Systems*, Volume 8, Issue 15, pp. 36−41.
27. Vaddi. R, Dasgupta. S, Agarwal. R. P (2010), "Device and circuit co design robustness studies in the sub threshold logic for ultralow-power applications for 32 nm CMOS", *IEEE Trans. Electron Devices*, Volume 57, Issue 3, pp. 654–664.
28. VamsiKiran, Nikhil Saxena (2015), "Design and analysis of different types SRAM cell topologies", *International Conference on Electronics and Communication System*, Volume 28, Issue 5, pp. 2136−2141.
29. Verma. N, Kong. J,Chandrakasan. A. P (2008), "Nanometer MOSFET variation in minimum energy sub threshold circuits", *IEEE Trans. Electronic Devices*, Volume 55, pp. 163−174.
30. Yuan-YuanWang,Zi-OuWang,Li-JunZhang(2012),"Anew6-Transistor SRAM cell for low power cache design"', *IEEE Transactions on VLSI System*, Volume 28, Issue 5, pp. 2136−2141.

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