Swarm Optimization-Based Modified Selective Harmonic Elimination PWM Technique Application in Symmetrical H-Bridge Type Multilevel Inverters

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***Abstract*—The problem of elimination of harmonics and the need of a large number of switches in multilevel inverters (MLIs) have been a hot topic of research over the last decades. In this paper, a new variant swarm optimization (SO) based selective harmonic elimination (SHE) technique is described to minimize harmonics in MLIs, which is a complex optimization problem involving non-linear transcendental equation. Optimum switching angles are calculated by the proposed algorithms considering minimum total harmonic distortion (THD) and the best results are taken for controlling the operation of MLIs. The performance of the proposed algorithm is compared with the genetic algorithm (GA). Conventional MLIs have some disadvantages such as the requirement of a large number of circuit components, complex control, and voltage balancing problems. A novel seven-level reduced switch multilevel inverter (RS MLI) is proposed in this paper to recoup the need of a large number of switches. Matlab/Simulink software is used for the simulation of two symmetrical topologies, i.e., a seven-level cascaded H-bridge multilevel inverter (CHB MLI) and a seven-level (RS MLI). Simulation results are validated by developing a prototype of both MLIs. The enhancement of the output voltage waveform confirms the effectiveness of the proposed SO SHE approach.**

Keywords-swarm optimization; selective harmonic elimination; multilevel inverter; cascaded H-bridge multilevel inverter; genetic algorithm; reduced switch multilevel inverter; selected harmonic elimination; total harmonic distortion; modulation index

I. INTRODUCTION

Nowadays many industrial drives require high or medium power for their operation and some require high power with medium voltage. Recently [1, 2], multilevel inverters are evolving as an alternative in high output power and medium voltage applications. MLI consists of many power semiconductor switches and a number of voltage sources, allowing integration of renewable energy sources with it [3-6]. MLI produces a staircase voltage output thus reducing the THD as the output waveform in close proximity to sinusoidal waveform [7-9]. As the number of level increases, harmonic distortion reduces more, but not without increasing the cost and complicacy. MLIs are generally categorized into three types: diode clamped MLI (DC MLI) [10], flying capacitor MLI (FC MLI) [11], and CHB MLI. DC MLI requires a large number of diodes, FC MLI requires voltage balancing of more capacitors and thereby has augmented cost. CHB MLI is more advantageous in respect to low *dv/dt* stress, less EMI noise and less THD than the other types [12, 13]. CHB MLI is made up of a series connected separate single phase bridge inverters, which operate with separate DC voltage source. This paper presents the design of a single phase seven-level cascaded H-bridge MLI using 12 switches aiming to reduce lower order harmonics which produce staircase voltage output waveform. The output voltage waveform is not purely sinusoidal, and it contains a number of odd order harmonics. The higher order harmonics can be easily reduced by using filters, but the lower order dominant harmonics are difficult to reduce. Authors in [14-16] explained different methods to reduce harmonics using pulse width modulation (PWM) and selected harmonic elimination (SHE) method. Lower-order harmonics are dominant in nature and complete elimination of these harmonics is not possible using conventional PWM techniques. SHE or programmed PWM technique [17] approach is thus used to eliminate specific order harmonics by calculating optimal switching angles. Switching angles are calculated by solving transcendental non-linear equations. Iterative techniques such as Newton-Raphson (NR) method [18] and mathematical resultant theory method [19] suffer from many disadvantages in doing so. The former approach fails at a good initial guess and results in only a few sets of solution. The degree of polynomial becomes large when the later approach is applied to higher level asymmetrical MLIs as the number of harmonics to be eliminated increases. Active harmonic elimination method [20] is another combinational approach of NR and resultant theory method for eliminating any number of specific harmonics. This method doesn't suggest finding all possible solutions for the infeasible modulation index.

Evolutionary algorithms have been further developed to overcome shortcomings of conventional methods. GA was an early developed stochastic algorithm that dealt with the SHE problem widely used in the literature [21, 29]. Particle swarm

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optimization (PSO) [22, 23, 32] is another such bio-inspired algorithm mostly used to eliminate harmonics in MLIs. However, for complex multi-minima functions, PSO fails to locate global optima and also reduces the speed of convergence [22]. A hybrid GA-PSO approach considering THD as a fitness function has been successfully demonstrated for CHB MLI in [7]. Authors in [24] report an analytical solution for harmonic elimination using bee algorithm for a symmetrical seven-level MLI and proved its superiority over GA. The low-order 5th and 7th harmonics are effectively suppressed assuming constant magnitude of DC sources. However, the magnitude of the DC source can be fluctuating when MLI is used in applications such as drives, renewable energy sources, and FACTS devices. In such cases, new expression needs to be considered which leads to a complex calculation of switching angles for each set of modulation index. In this regard, a new group of optimal harmonic minimization techniques has been investigated in [25-27] considering variable DC-link voltage. An analytical solution for THD minimization using online switching angle calculation for equal voltage sources has been suggested in [19]. In [28], an online switching angle calculation approach using artificial neural networks has been discussed considering unequal DC sources. However, equal values of DC sources are considered in the present study and a novel optimization approach is developed to deal with the SHE problem.

In this paper, advanced SHE technique was utilized in order to reduce specific lower order harmonics, such as the 5th and the 7th, from the output voltage. The technique solves different non-linear equations and gives best optimized results. Furthermore, this paper reports the development of a reduced switch seven-level MLI (RS MLI) topology which uses 7 switches and requires less number of driver circuits. RS MLI produces the same voltage output as CHB MLI and involves less expenditure. Calculation of THD as an optimization problem is also described. GA [29, 30] and SO SHE approach are applied to solve non-linear equations for reducing THD. Also, a comparison study drawn between GA and SO SHE approach is provided. The calculated SO SHE data are used for developing simulation models and hardware design. The proposed topology is validated by comparing the results obtained from the simulation and the experimental model.

II. CASCADED H-BRIDGE MLI TOPOLOGY (CHB MLI)

For a single phase 7-level CHB MLI, the structure is shown in Figure 1(a). In this circuit, each voltage source is connected in cascade with other voltage sources via 3 H-bridge circuits. Each H-bridge consists of 4 power semiconductor switches which produce 3 level outputs, i.e., $+V_{dc}$, 0 or $-V_{dc}$ [13]. At any instant of time, (N_l-1) numbers of switches are in the current path in a CHB MLI, which incurs more conduction loss. The final voltage in the *+ve* half cycle is $+3V_{dc}$ and in *–ve* half cycle is $-3V_{dc}$. The number of levels in an N_l-level MLI is given by $2N_{DC}+1$, where N_{DC} denotes the number of DC sources used. Output voltage waveform pattern for the 7-level CHB MLI is shown in Figure 1(b). The overall output voltage of MLI is given by $V=V_{dc1}+V_{dc2}+V_{dc3}$. In this paper, all three voltage levels are taken equal, i.e. $V_{dc1}=V_{dc2}=V_{dc3}=V_{dc}$. In Figure 1(b), α_1, α_2, and α_3 are three switching angles needed to be calculated by solving non-linear equations to minimize THD.

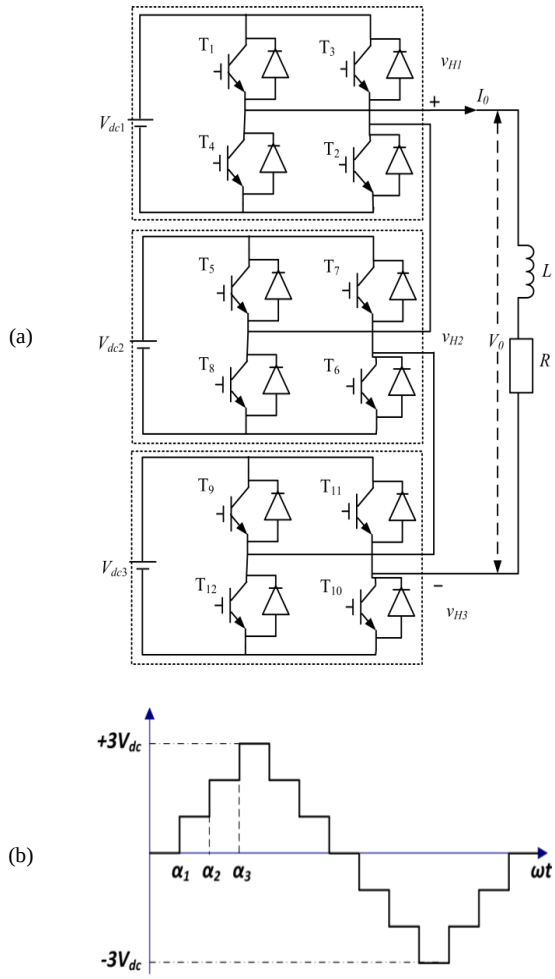

Fig. 1. (a) Structure of single phase seven-level CHB MLI, (b) Output voltage waveform of single phase seven-level MLI

III. PROPOSED REDUCED SWITCH MLI

The number of switches in MLI defines cost, circuit size, reliability and complexity. So the key element in designing a MLI is the number of required switches against the required voltage level. To construct the same output obtained as in a seven-level CHB MLI, a new circuit topology has been developed with a reduced number of switches without increasing the number of H-bridges. Figure 2(a) shows the proposed MLI structure and Figure 2(b) shows the proposed MLI output voltage waveform with corresponding switching states. The H-bridge switches (or polarity generation switches) operate at low switching frequency whereas the level generation switches T_1-T_3 operate at high switching frequency. Hence, a cost effective solution is to choose low switching power components for the H-bridge and high switching power components for the level generation. In comparison to a CHB MLI the required number of switches in RS MLI is smaller. In CHB MLI 12 switches are used, whereas only 7 switches with 2 discrete diodes are used in design of RS MLI. The working principle of RS MLI is summarized in the following modes:

- Mode a: When T_1 is ON, current flows through the two diodes, both H-bridge switches S_1 and S_2. So, voltage output is $+V_{dc}$ across the load (Figure 3(a)). Similarly when S_3 and S_4 are switched ON, voltage output is $-V_{dc}$.
- Mode b: In this mode, switch T_2 is made ON. Current flows through diode D_2, and switches S_1 and S_2. So, output voltage is $+2V_{dc}$ across the load (Figure 3(b)). Similarly when S_3 and S_4 are switched ON, voltage output is $-2V_{dc}$.
- Mode c: When T_3 is ON, this mode of operation starts. Current flows through switches S_1 and S_2, so voltage output is $+3V_{dc}$ across the load. Diodes D_1 and D_2 are reverse biased (Figure 3(c)). Similarly when S_3 and S_4 are switched ON, voltage output is $-3V_{dc}$.
- Mode d: Both S_1 and S_3 or S_2 and S_4 are ON in this mode. Switches T_1, T_2 and T_3 are in OFF state. Voltage output obtained across the load is zero (Figure 3(d)).

The switching scheme of RS MLI is depicted in Table I. Output voltage obtained from a RS MLI with corresponding switching states has been depicted in Figure 2. Although the output voltage is the same, the switching stress in RS MLI is less and the voltage profile can be improved by proper control.

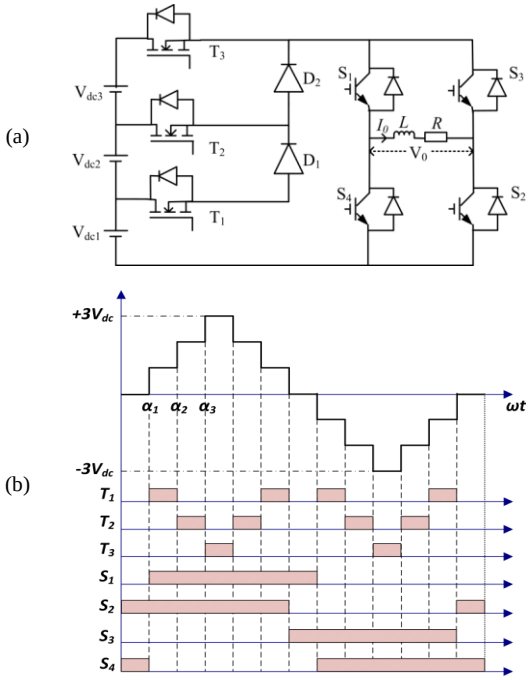

Fig. 2. (a) Structure of single phase seven-level RSMLI, (b) Output voltage waveform with corresponding switching states

A. Comparison of Conventional and Proposed MLI Topology

In this section the proposed MLI topology is been compared with the conventional CHB MLI, DC MLI, and FC MLI. For generating N_l output voltage levels, the proposed RS MLI requires only $(N_l+7)/2$ switches (N_{sw}), whereas conventional MLI topologies need $2(N_l-1)$ per phase switches.

TABLE I. SWITHCING SCHEME OF SEVEN-LEVL RS MLI

Switching state	T_1	T_2	T_3	S_1	S_2	S_3	S_4	D_1	D_2
$+3V_{dc}$	0	0	1	1	1	0	0	×	×
$+2V_{dc}$	0	1	0	1	1	0	0	×	✓
$+V_{dc}$	1	0	0	1	1	0	0	✓	✓
0	0	0	0	1	0	1	0	×	×
0	0	0	0	0	1	0	1	×	×
$-V_{dc}$	1	0	0	0	0	1	1	✓	✓
$-2V_{dc}$	0	1	0	0	0	1	1	×	✓
$-3V_{dc}$	0	0	1	0	0	1	1	×	×

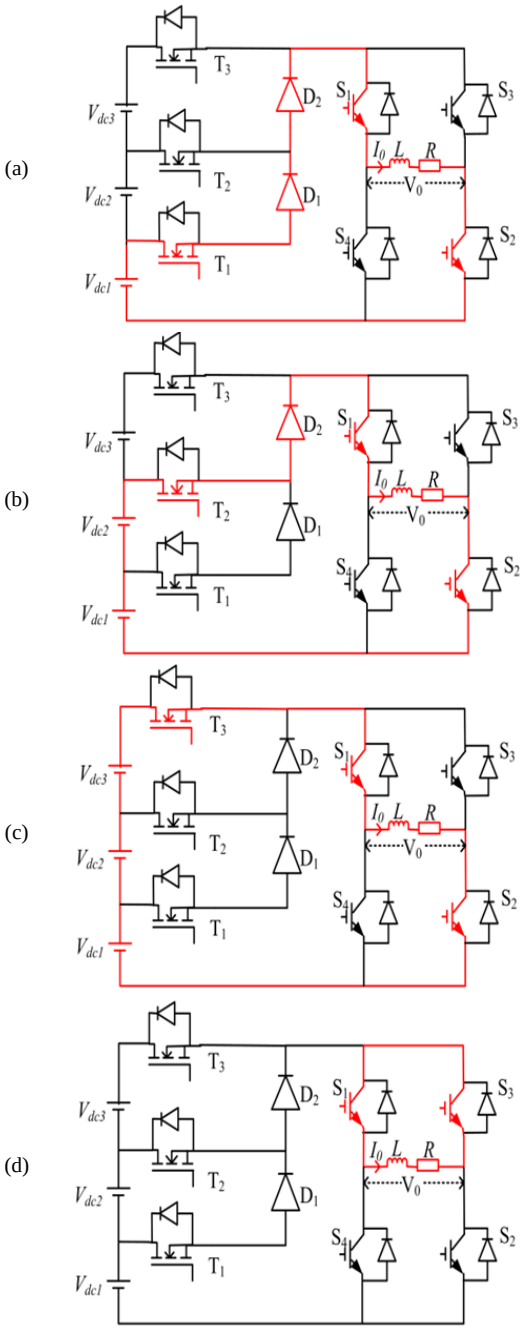

Fig. 3. Operation of proposed RS MLI for generating positive output voltage levels: (a) Mode a, (b) Mode b, (c) Mode c, (d) Mode d

As shown in Figure 4(a), the proposed inverter requires fewer switches to realize N_l voltage levels at the output. It is important to note that the required number of driver circuits (N_{driver}) is the same as N_{sw} for all aforementioned topologies. Figure 4(b) compares the number of DC voltage sources with the aforementioned MLI topologies. For realizing N_l voltage levels, CHB MLI and the proposed topology needs (N_l-1)/2 DC voltage sources, whereas DC MLI and FC MLI topologies need only 1 DC source with (N_l-1) dc bus capacitors. However, the proposed topology doesn't need any clamping diodes or clamping capacitors similar to a CHB MLI. But, DC MLI needs (N_l-1)×(N_l-2) extra clamping diodes per phase and FC MLI needs (N_l-1)×(N_l-2)/2 clamping capacitors per phase.

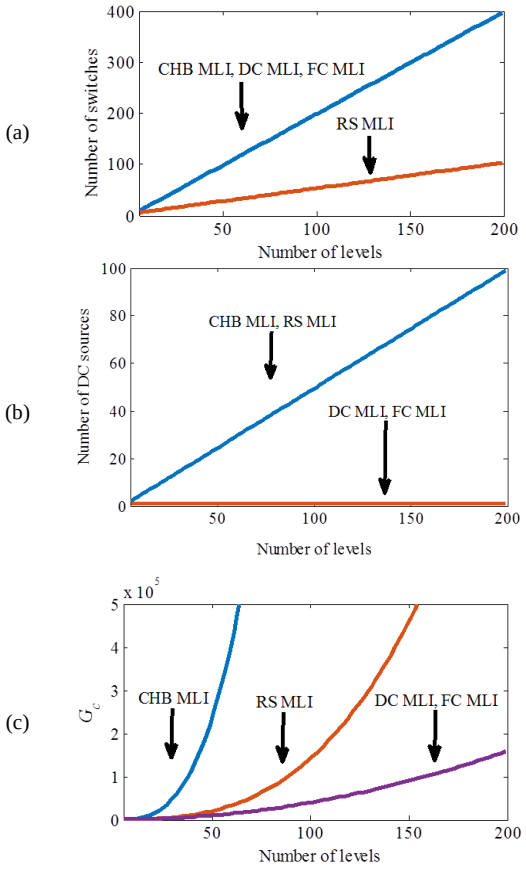

Fig. 4. Comparison of the proposed RS MLI with the conventional topologies: (a) Number of semiconductor switches against the number of voltage levels, (b) Number of DC voltage sources against the number of voltage levels, (c) *Gc* variation against the number of voltage levels

Another comparison index, G_c is taken from the viewpoint of volume, size, and cost of the MLI. The coefficient G_c can be defined as:

$$G_c = N_{DC} \times N_{sw} \times N_{driver} \times N_{vr} \quad (1)$$

Figure 4(c) shows the variation of the coefficient G_c with respect to N_l voltage levels. The CHB MLI topology has very high value of G_c as compared to the DC MLI and FC MLI topologies. The proposed RS MLI topology has lower G_c coefficient than CHB MLI topology. This signifies that the size and overall cost in designing the RS MLI are smaller than the conventional and other H-bridge based MLI topologies. Here, the required number of clamping diodes and clamping capacitors are not taken into account when calculating G_c. So, it is much lower for DC MLI and FC MLI topologies. But, practically the overall cost of DC MLI and FC MLI topologies is more than the one of the other mentioned topologies due to the presence of additional clamping diodes and capacitors.

B. Comparison of Proposed MLI with Recently Developed Well-Known MLI Topologies

The comparison presented above is extended for the recently developed MLI topologies, MLI 1 [1], MLI 2 [29], MLI 3 [7], MLI 4 [2], MLI 5 [34], MLI 6 [36] in terms of number of dc sources (N_{dc}), number of switches (N_{sw}), number of diodes (N_d), number of capacitors (N_c), and number of transformers (N_{tr}). MLI 1 and 2 require the same number of components, whereas the switch count has been reduced in MLI 3, but the total number of components is the same as in MLI 1 and 2 due to the addition of discrete diodes and capacitors. In this regard, MLI 4 requires less components than the afore-mentioned topologies. Furthermore, a few transformer-based topologies are also developed, such as MLI 5 which uses single dc source but also a transformer for producing 7 levels. Other single dc source MLIs reported in [33, 35, 36] utilize fewer semiconductor switches, smaller total number of components, and thus are superior among the discussed topologies with regard to cost and volume. But, as MLI 6 consists of a capacitor, thus for higher voltage level application, capacitor voltage balancing may be a measure issue in such an MLI. The requirement of components for a 7-level RS MLI is summarized in Table II. Although the proposed topology requires a number of dc sources which increases as the voltage level increases, this can be of use in multiple renewable energy source based applications.

TABLE II. PROPOSED RS MLI - WELL KNOWN 7-LEVEL MLI TOPOLOGIES COMPARISON

MLI Topologies	N_{dc}	N_{sw}	N_d	N_c	N_{tr}	Total
MLI 1 [1]	3	10	0	0	0	13
MLI 2 [29]	3	10	0	0	0	13
MLI 3 [7]	1	8	2	2	0	13
MLI 4 [2]	3	8	0	0	0	11
MLI 5 [34]	1	8	0	0	1	10
MLI 6 [36]	1	6	0	1	0	8
Proposed RS MLI	3	7	2	0	0	12

IV. THD CALCULATION USING OPTIMIZATION ALGORITHM

As described above, the SHE technique is currently being prominently used to synthesize output voltage of multilevel inverters. The configuration showed in Figures 1(a) and 2(a) produces similar patterns of output voltage. In the output voltage waveform the positive half cycle is equal to the negative half cycle, i.e. quarter wave symmetrical output. The output voltage waveform shown in Figure 2(b) can be expressed in Fourier series as:

$$V(t) = \sum_{n=1}^{\infty} V_n \sin(n\alpha_n) + B_n \cos(n\alpha_n) \quad (2)$$

The even order harmonics automatically get canceled due to quarter wave symmetry, i.e. B_n=0 for all n. So the new equation of output voltage becomes:

$$V(t) = \sum_{n=1}^{\infty} V_n \sin(n\alpha_n) \quad (3)$$

The amplitude V_n can be expressed in terms of Fourier series with α varies in the range of 0 to π/2:

$$V_n = \frac{4V_{dc}}{n\pi}(\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3) \quad (4)$$

The three switching angles α_1 , α_2 , and α_3 and the fundamental component of output voltage are controlled using the modulation index. The dominant lower order harmonics need to be eliminated from the output phase voltage. Accordingly, the three non-liner equations for the solution of the problem are taken in this work as:

$$\begin{aligned} V_1 &= \frac{4V_{dc}}{\pi}(\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3) = m \\ V_5 &= \frac{4V_{dc}}{5\pi}(\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3) = 0 \\ V_7 &= \frac{4V_{dc}}{7\pi}(\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3) = 0 \end{aligned} \quad (5)$$

where, $m = \frac{V_f}{(4V_{dc}/\pi)}$, modulation index = $M = m / N_{DC}$, N_{DC} is the number of DC sources, and V_f is the required value of fundamental voltage.

Fifth and 7th order harmonics are targeted for elimination by solving the above non-linear equations. The solution of these equations leads to discontinuity for the certain modulation index. So, the non-linear equations of the SHE problem are solved as an optimization problem. Conventional technique uses NR method to solve the above problem which involves more computation time and complicated mathematical calculations. In order to reduce this, SO SHE is developed which solves the objective function at optimal value of switching angles. The suitable fitness function is chosen to eliminate 5th and 7th order harmonics at different value of switching angle and to satisfy the fundamental component as under:

$$FF = \frac{1}{h} * \left[\left| M - \frac{|V_1|}{N_{DC}V_{DC}} \right| + \left(\frac{|V_5| + |V_7|}{N_{DC}V_{DC}} \right) \right] \quad (6)$$

Subject to the condition that:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2} \quad (7)$$

To obtain the least THD with feasible modulation index the whole term in (6) is multiplied with a factor 1/h. The fundamental value and the targeted 5th and 7th order harmonics are kept within 1% (i.e., h=0.01) error limit. To check the quality of voltage waveform, THD can be defined and calculated as:

$$\text{THD}\ (\%) = \left[\frac{1}{V_1^2} \sum_{k=2}^{\infty} (V_k)^2 \right]^{\frac{1}{2}} \times 100 \quad (8)$$

where V_k is the voltage of particular harmonics.

V. GENETIC ALGORITHM

GA [29, 30] is a method of random search process used to find approximate solutions of optimization problems. It is a local search technique inspired by biological evolution. The evolution starts from a random initial population and repeatedly modifies the solution in each generation. Over a successive generation, multiple individuals (switching angle) are selected from the current population and are used in the next iteration of the algorithm until it reaches an optimal solution. GA uses three main rules in each step to create the next generation of the current population, which contributes for the desired results to select the population. Crossover and mutation are used to simulate the natural reproduction and mutation. In crossover, selected individuals are combined and swapped to produce new offspring. With a continuous number of generations and a large population in each generation, the algorithm optimizes a set of solutions of the problem. It computes the different values of the three switching angles to obtain the minimum *FF* keeping the harmonics within the limit. The GA toolbox is an inbuilt graphical user interface that allows using GA in MATLAB environment without working at the command line [17]. The GA toolbox results are shown in Figure 5. Results obtained from GA are summarized in Table III. To use the GA toolbox, the following information should be entered.

- Fitness function**:** The fitness function as given in (6) has been entered in the form *@FF*, where *FF.m* is a program file that computes the fitness function.
- No of variables: The length of input vector to the fitness function is entered. The three switching angles are considered as variables.
- Constraint function for the problems can be specified in the constraints panel of toolbox. Boundary variables can be specified as well. Population size, initial population and display command are set in the options panel.

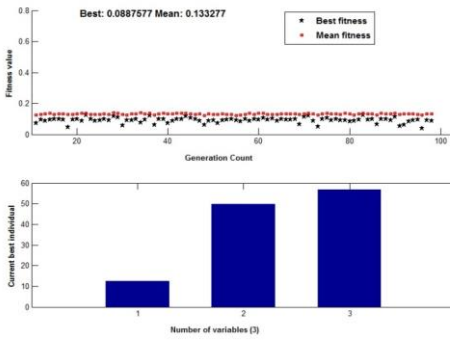

Fig. 5. Best fitness and no. of variables obtained using GA

TABLE III. RESULTS OBTAINED FROM GA

Results obtained from GA	Generation count	Obtained switching angles (in degree)			Mean fitness	Best fitness
	100	α_1	α_2	α_3	0.133	0.088
		12.56	49.69	56.89		

VI. SO SHE TECHNIQUE

A new variant swarm optimization based algorithm called SO SHE is analyzed in this paper. The theory of SO SHE has been influenced from the same phenomenon as PSO, i.e., bird flocking in which it helps the swarm or particle (bird) in dodging from predators. Similar to the conventional PSO algorithm, SO SHE has a cognitive and a social behavior component. Both these components are composed of best and worst values, but PSO considers only the best value in successive iterations. Including both best and worst values enhances the swarm's ability to follow the best possible solution. The particles progress in the search space with certain velocities and may reach a best or worst solution. The best and worst positions are stored in the memory as good and bad experience components respectively. The food location is modeled as the best solution point and a predator is modeled as the worst position [31, 32, 37]. The new velocity-position update equation in SO SHE model is accordingly modified by (9) and (10) for *i*th particle in *d* dimensional space as:

$$V_{ij}^{r+1} = \delta^r v_{ij}^r + C_1R_1\left(Pb_{ij}^r - P_{ij}^r\right) + C_2R_2\left(Pw_{ij}^r - P_{ij}^r\right) + C_3R_3\left(Gb_j^r - P_{ij}^r\right) + C_4R_4\left(Gw_j^r - P_{ij}^r\right) \quad (9)$$

$$P_{ij}^{r+1} = P_{ij}^r + V_{ij}^{r+1} \quad (10)$$

where i=1, 2, …., n; j=1, 2, …., d; r is the iteration number and r+1 index denotes the next iteration, δ is the inertia weight which can be defined as:

$$\delta = (\delta_{max} - \delta_{min}) \times \frac{iter_m - iter}{iter_m} + \delta_{min} \quad (11)$$

where $iter_m$ is the maximum number of allowable iterations and *iter* is the current iteration. δ_{max} is set to 0.9 and δ_{min} is 0.4.

VII. SO SHE ALGORITHM FOR FITNESS EVALUATION

- Initialization: Initialize modulation index (M), size of population, maximum number of iteration (itermax) and the acceleration coefficients C_1, C_2, C_3 and C_4. The acceleration coefficients' values are set to 1.5, 0.55, 1.75 and 0.35 respectively. $R_1$to R_4 are random numbers between [0, 1]. Randomly create a set of the three switching angles.
- Fitness function (*FF)* evaluation: Evaluate the FF for each of the switching angles.
- The initial positions until iteration r are considered as the local best position of each particle, i.e., Pb_i^r and the global best position Gb^r is the minimum value of the *FF*. Similarly, the final positions are considered as the local worst position, i.e., Pw_i^r and the global worst position Gw^r is the maximum value of *FF*.
- Condition check: Switching angles must satisfy the feasibility criteria that they lie between 0 to π/2 as in (7).
- Updating velocity and position: In this step the particles follow a velocity and position update rule given in (9) and (10). New best and worst values are stored in the memory. Iteration continues in the same way until the counter reaches the maximum set value and the new positions of the particles are then calculated.
- Termination**:** If the iteration count reaches the maximum set value then calculate the fitness function by varying the M from 0 to 1, otherwise repeat the updating procedure.

VIII. GA - PROPOSED SO SHE ALGORITHM COMPARISON

The behaviors of GA and SO SHE algorithm are compared and it is observed that both algorithms converge with acceptable solutions for different modulation indices. Figure 6(a) shows the variation of switching angles obtained using SO SHE for different M. The switching angles satisfy the condition (7). The THD obtained using both algorithms against M is plotted in Figure 6(b) taking a population size of 100 individuals. Lesser THD is obtained at full range of M using SO SHE as compared to GA. This as well signifies that SO SHE converges to a better solution than GA. THD decreases with increase in M, which satisfies the operational principle of MLIs. Figure 6(c) shows the harmonic profile versus the M obtained using the SO SHE algorithm.

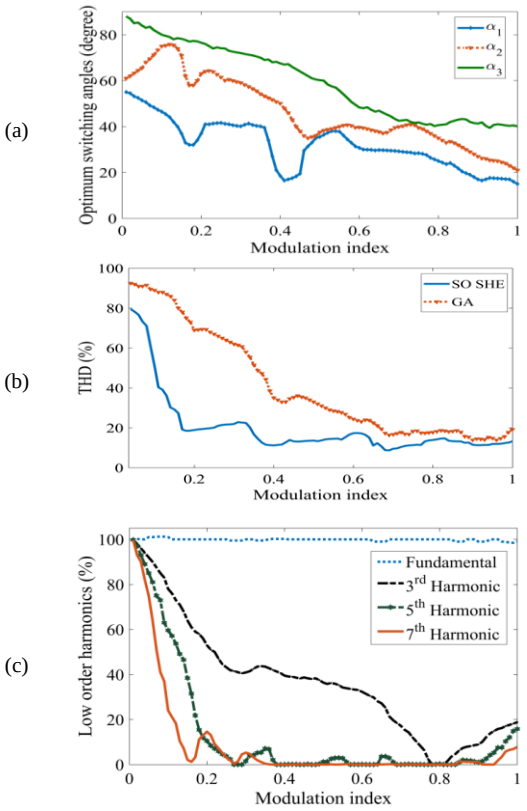

Fig. 6. (a) Switching angles obtained using SO SHE, (b) Comparison of THD (%) against M for GA and SO SHE, (c) Low order harmonics profile against M.

The 3rd harmonic is as high as expected at the whole range of M. Keeping in mind future applications of the algorithm to 3

phase systems, triple harmonic content is not chosen to be eliminated in this paper. Triple harmonics are absent in line to line voltage of a 3 phase balanced system. 5th and 7th harmonics are nearly zero at almost all values of *M* which shows the effectiveness of the proposed SO SHE algorithm. Furthermore, to prove the robustness of the algorithm, a test is conducted in MATLAB environment on an Intel(R) core (TM), i5, 2.60 GHz processor taking computational time and attained objective value into consideration when all other conditions are kept unchanged. With 100 individuals per population, both algorithms run 20 times and the results are tabulated at 0.5, 0.7 and 0.9 modulation indices. Table IV shows the best objective value and corresponding computational times for 50, 150 & 300 iterations. The comparison in Table IV summarizes that under the same conditions, SO SHE always converges faster than GA and also approaches to a better solution.

TABLE IV. GA AND SO SHE BEHAVIOR COMPARISON

M	iteration=50		iteration=150		iteration=300	
	GA	SO SHE	GA	SO SHE	GA	SO SHE
Best objective value in 20 runs, in %						
0.5	18.7894	17.95	13.919	13.729	8.9312	6.8966
0.7	15.5441	14.8122	11.127	8.1018	6.1201	4.1911
0.9	13.9921	11.1216	6.1132	5.1101	4.0319	3.0113
Computational time, in sec.						
0.5	99	77	141	134	197	173
0.7	89	69	136	133	191	173
0.9	83	65	132	129	196	168

Population=100

IX. SIMULATION AND HARDWARE RESULTS

In order to validate the proposed MLI topology, simulations have been carried out using MATLAB/Simulink for the seven-level CHB MLI and RS MLI. The value of all three DC sources is taken equal to 35V and the frequency of output voltage is assumed to be 50Hz. A series resistive-inductive load of 100Ω - 150mH is taken in both cases. The calculated switching angles using SO SHE algorithm at 0.91 modulation index (Table IV) are applied to the simulation and experimental models. The SO SHE programming code run integrated to the simulation model and results are obtained.

A. Simulation of CHB MLI

Insulated gate bipolar transistors (IGBTs) are considered as switching devices for simulation and hardware design of seven-level CHB MLIs. Required PWM signals for one switch of each H-bridge (T_1, T_5 and T_9) are shown in Figure 7(a). Figures 7(b) and 7(c) show the simulated output voltage and current waveform, respectively, of a seven-level CHB MLI. The output voltage results in very small THD of 14.33% are shown in Figure 7(d).

B. Simulation of RS MLI

Four IGBTs and three MOSFETs with two discrete diodes were used for designing a seven-level RS MLI. Generated PWM signals for the level generation switches T_1, T_2 and T_3 are shown in Figure 8(a). The simulated output voltage and current waveform of seven-level RS MLI are shown in Figures 8(b) and 8(c). The FFT analysis of the output voltage waveform is shown in Figure 8(d). It is observed that the 5th and 7th order harmonics are nearly 0.01% and 0.025%, respectively which is negligible. A comparison of MLI topologies described in this study has been presented in Table V.

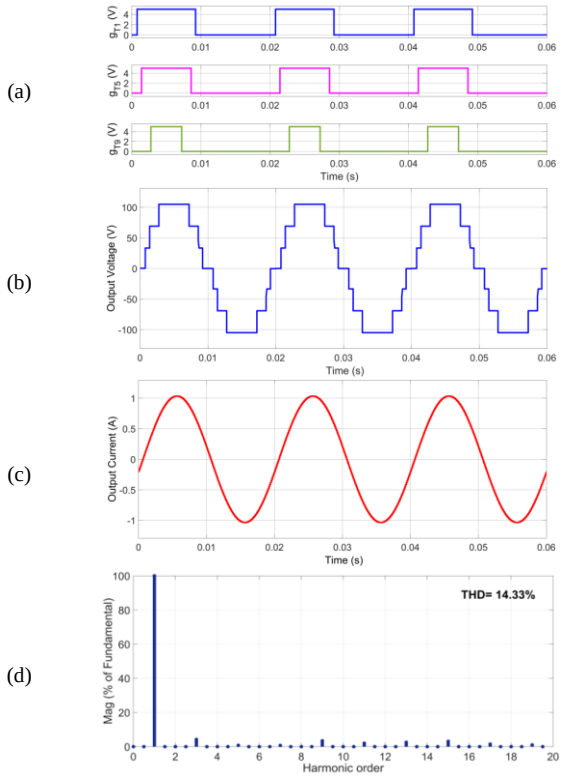

Fig. 7. Simulation results obtained for seven-level CHB MLI: (a) PWM signals for switches T1, T5, and T9, (b) Output voltage waveform, (c) Output current waveform, (d) FFT analysis of load voltage

TABLE V. COMPARISON OF MLI TOPOLOGIES

Different topology		**7-level CHBMLI**	**7-level RSMLI**	
No.of switches		**12 [2(N_l-1)]**	**7 [(N_l+7)/2]**	
Switching loss		**More**	**Less**	
Switching angle *	α_1 =16.5°	For H-bridge 1	For T_1	Switches S_1 and S_2 are continuously ON for *+ve* half cycle (0°-180°)
	α_2 =26.2°	For H-bridge 2	For T_2	
	α_3 =41.8°	For H-bridge 3	For T_3	Switches S_3 and S_4 are continuously ON for *-ve* half cycle (180°-360°)
THD	**(in %)**	**14.33**	**11.84**	

* using SO SHE at M=0.91 (°)

C. Hardware Design of CHB MLI

The simulation results are validated by a prototype laboratory setup of seven-level CHB MLI with three isolated DC sources, each of constant voltage 25V. Gate pulse for the switches is generated using an ATmega16 microcontroller. A series resistive-inductive load of 80Ω - 50mH is used. The components used for the hardware design of the seven-level CHB MLI are given in Table VI. Figure 9(a) shows the PWM pulses for the switches T_1, T_5, and T_9. The feasible switching angles at *M*=0.91 given in Table IV are calculated offline using SO SHE algorithm, and were programmed into the microcontroller using WINAVR programmer.

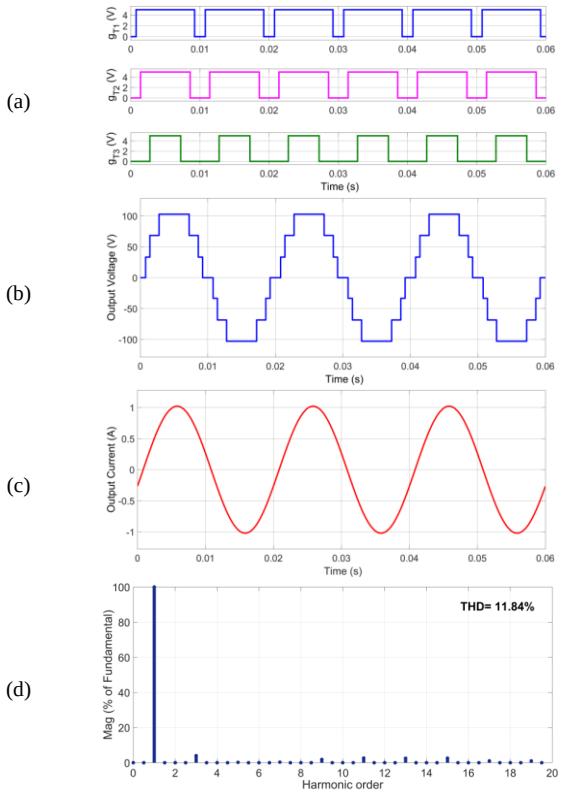

Fig. 8. Simulation results obtained for seven-level RS MLI: (a) PWM signals for level generation switches T_1, T_2, and T_3, (b) Output voltage waveform, (c) Output current waveform, (d) FFT analysis of load voltage

TLP250 opto-coupler was used as driver and for the isolation. All waveforms were acquired using Tektronix TPS2014B digital storage oscilloscope (DSO) and post-processed using MATLAB to obtain the harmonic spectrum. Figure 9(b) shows the staircase 7-level output. The sinusoidal output current is shown in Figure 9(c). Figure 9(d) shows the harmonic spectrum, in this case the value of THD is 14.91%.

TABLE VI. 7-LEVEL CHB MLI: COMPONENTS USED FOR

Components/parameters	Specification
power switches (IGBT)	FGA25N120
driver	TLP250
processor	ATmega 16 microcontroller
isolated DC supply	25V
nominal frequency	50Hz
linear *R-L* load	(0-100)Ω, 50mH

D. Hardware Design of RS MLI

A 7-level RS MLI setup is developed consisting of 4 IGBTs and 3 MOSFETs. Similar setup as for CHB MLI is developed and the output is obtained across the *RL* load. The components used for design of RS MLI are given in Table VII. Figure 10(a) shows the PWM signal for H-bridge S_1 and the level generation switches T_1, T_2, and T_3. The offline calculated switching angles are programmed into the ATmega16 microcontroller using a burner circuit. The generated pulses drive the power semiconductor switches. Output voltage and current obtained for the proposed RS MLI across a *RL* load (80Ω, 50mH) is shown in Figures 10(b) and 10(c). The FFT analysis of the voltage waveform obtained is shown in Figure 10(d). It is evident from the results that the proposed seven-level RS MLI has better performance, less requirements of components, and low %THD compared to the seven-level CHB MLI.

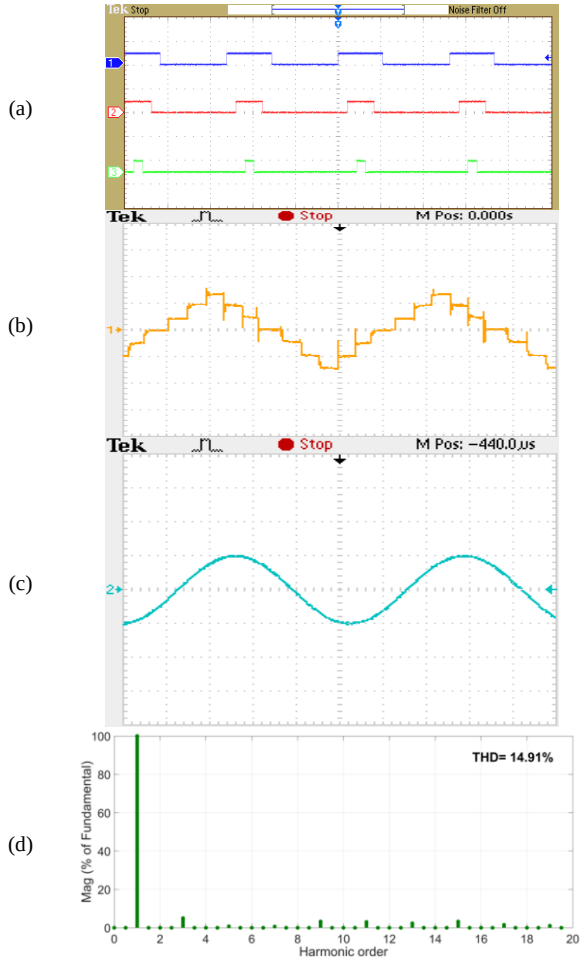

Fig. 9. Experimental results for 7-level CHB MLI: (a) PWM signals for switches T_1, T_5, and T_9 (y-axis 20V/div, x-axis 2ms/div), (b) Output voltage waveform (y-axis 50V/div, x-axis 1ms/div), (c) Output current waveform (y-axis 1A/div, x-axis 1ms/div), (d) FFT analysis of load voltage

TABLE VII. 7-LEVEL RS MLI: COMPONENTS USED

Components/parameters	Specification
power switches (MOSFET & IGBT)	IRFP250 & FGA25N120
diode	RHRP840
driver	TLP250
processor	ATmega 16 microcontroller
isolated DC supply	25V
nominal frequency	50Hz
linear *R-L* load	(0-100)Ω, 50mH

X. CONCLUSION

In this paper, a new RS MLI topology using reduced switch count was presented and compared with the conventional CHB MLI topology. The total number of switches is nearly halved when compared to the CHB MLI topology. So, switching loss is expected to be reduced drastically while the cost is minimized.

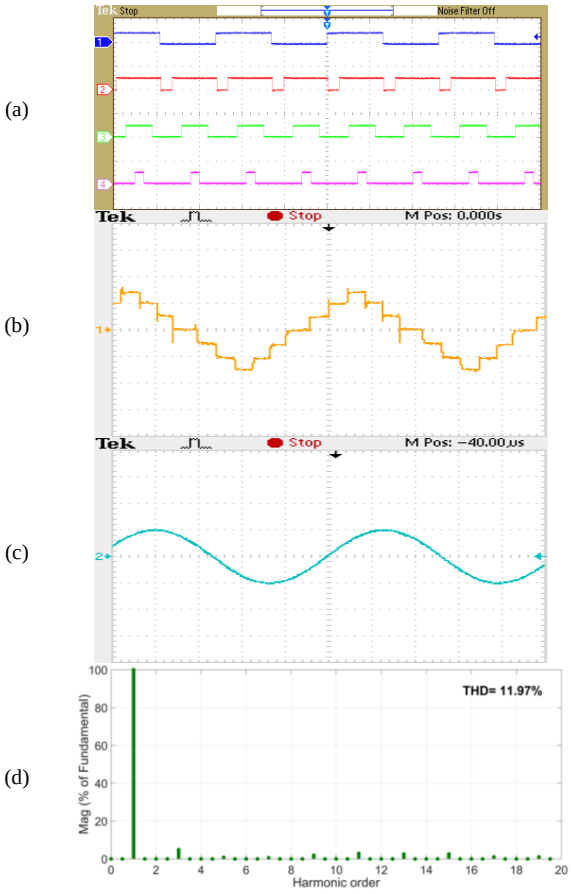

Fig. 10. Experimental results obtained for 7-level RS MLI: (a) PWM signals for polarity generation switch S_1, level generation switches T_1, T_2, and T_3 (y-axis 20V/div, x-axis 2ms/div), (b) Output voltage waveform (y-axis 50V/div, x-axis 1ms/div), (c) Output current waveform (y-axis 1A/div, x-axis 1ms/div), (d) FFT analysis of load voltage

For the proposed RS MLI, a total number of $(N_l+3)/2$ switches including discrete diodes are in the current path at any time whereas (N_l-1) switches are in the current path for the CHB MLI. This indicates that the conduction loss and voltage drop are also less for the proposed MLI when compared to a CHB MLI. A comparison in view of cost, size and volume is also drawn among seven-level MLI types. Novel SO SHE algorithm is used to determine the optimum switching angles for selectively eliminating voltage harmonics as detailed in the *FF*. A delineative analysis shows that the proposed SO SHE approach successfully reaches a feasible solution in minimum time compared to GA. Offline calculated switching angles using SO SHE are then applied to the simulation circuit and to the hardware design of both presented MLIs. Simulations and experimental results show that the undesired 5^{th} and 7^{th} harmonics are very negligible in the output voltage waveform and THD is reduced by around 3% in seven-level RS MLI in comparison with a CHB MLI. Although the presented scheme has been applied to a single phase seven-level MLI structure, this methodology can easily be extended for developing N_l-level MLI consisting of different loads with succeeding reduction in THD and switching loss further.

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