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Diffusion of Adhesion Layer Metals Controls Nanoscale Memristive Switching

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First prominent more than 40 years ago,[1] electrical resistance switching in conductor/insulator/conductor structures has regained significant attention in the last decade,[2–16] motivated by the search for alternatives to conventional semiconductor electronics.[17] Recent results have shown promising device behaviors, such as reversible, non-volatile, fast (<10 ns), low-power (~1 pJ/operation) and multiple-state switching,[18–26] which are suitable for applications in non-volatile random access memory (NVRAM),[27–30] synaptic computing,[31] and other circuit families.[32–35]

Among different types of resistance switches, metal/oxide/metal junctions are one of the most extensively studied.[1–4,6,8–11,13,14,16,22,36–40] It was recently demonstrated that bipolar Pt/TiO_2/Pt switches are memristive devices,[20,41] which means that they are two-terminal passive devices with state (in other words, they 'remember' their history without storing charge or energy). Memristors were predicted theoretically in 1971 as the fourth passive circuit element, complementing the resistor, capacitor and inductor, with a range of unique and potentially useful circuit properties.[42,43] Memristive switching in semiconductor thin films arises from the coupling between solid-state electronic and ionic (dopant) transport under an applied electrical bias.[41] For memristive switches based on TiO_2, the switching is caused by the drift of oxygen vacancies (VOs), which are positively charged dopants, into and out of an insulating interface region,[20] and a family of reconfigurable nanodevices has been demonstrated with a rich set of device behaviors.[26]

In order to make these switches useful in electrical circuits, a high device yield and an engineering control over device properties, such as switching polarity, are needed. However, the yield of devices has historically been low and the variance between different switching cycles or different devices has been large for these metal/oxide/metal structures after an electroforming step. Electroforming is a process to pre-condition the as-prepared junctions into a reversible switching state by applying a high electric field across the junction, which creates localized conductance channels of low resistance via an electro-reduction process.[44,45] These conductance channels are the sites for the subsequent switching. The electroforming process is often poorly controlled, leading to a broad distribution of post-forming states for the devices, including a significant resistance variance, uncontrolled switching polarity and even unswitchable failed devices as a result of excessive forming damage. Physical understanding and control over this electroforming is essential before repeatable, engineered switching can be guaranteed.

In this paper, we show that electroforming and thus the subsequent switching of TiO_2 metal oxide switches can be controlled by the diffusion of trace 'adhesion layer' reactive metal atoms through the contact electrodes to the metal oxide switching layer. Many previous studies have focused on the as-deposited metal/oxide/metal tri-layer that nominally defines the device. However, an adhesion layer is often used to help the bottom electrode better adhere to a substrate, and the possible influence of that layer on device properties has been ignored. For a multilayered material stack that is only tens of nanometers thick, the final structure is usually different from what is nominally deposited because of strong chemical and/or physical interactions among the layers.[46] Therefore, the entire device stack should be considered as a single material system. We show that the adhesion layer material and anneal history plays a critical role in determining switching device properties, including switchable device yield, initial state conductance and switching polarity.

Devices with a junction area of 5 µm × 5 µm were built to demonstrate the role of the adhesion layer on device behaviors, since such large devices have adequate junction areas for some typical material characterization techniques. Three multilayered samples were fabricated on Si/SiO_2 wafers: a sample with a 5 nm Ti adhesion layer, a sample with a 5 nm Cr adhesion layer and a control sample without any adhesion layer. Next, a trilayer of Pt (15nm)/TiO_2 (40nm)/Pt (30 nm) was deposited in the same experimental run to complete these three samples and ensure that the 'active layers' of the devices were identical, as illustrated schematically in **Figure 1a**. The TiO_2 layer was deposited at 250 °C and then the samples were transferred in air to an evaporation chamber for the 30 nm Pt top electrode deposition at ambient temperature. Figure 1b presents typical *I-V* curves of the virgin states for these three samples, which display significant differences among the three samples. The

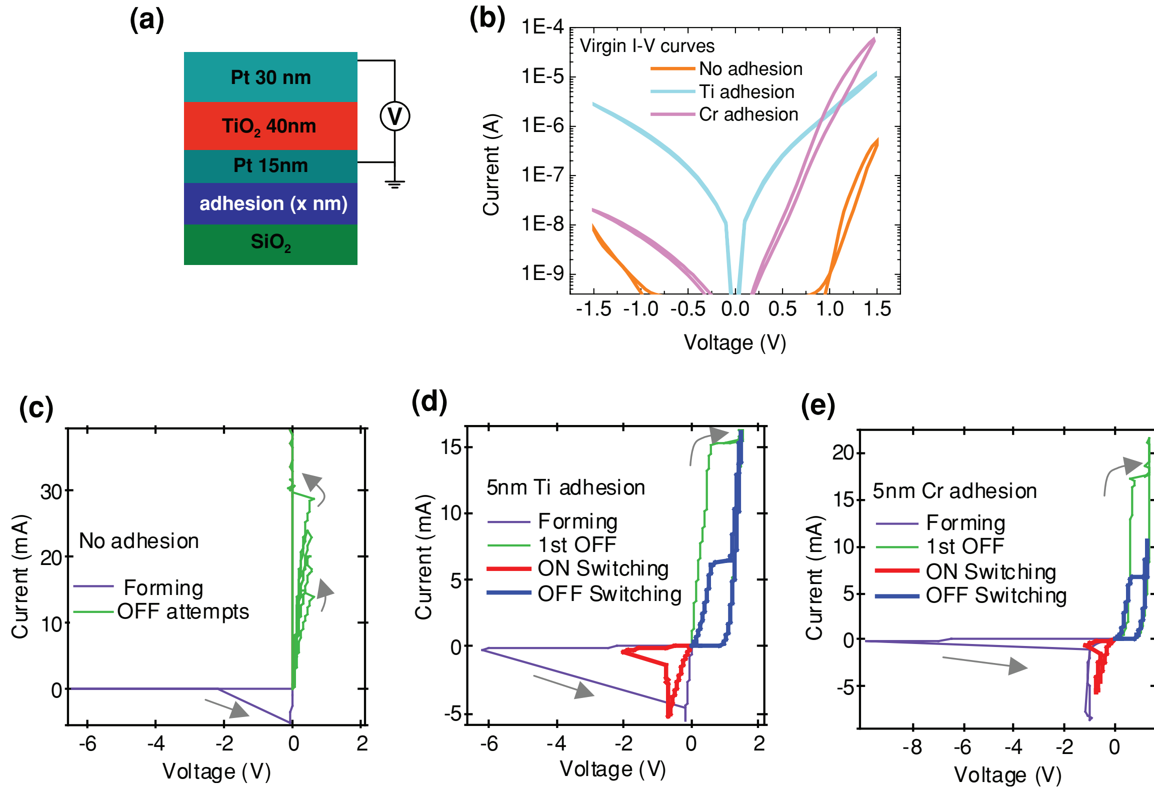

Figure 1. The effect of an adhesion layer on the electrical behavior of Pt/TiO_2/Pt crosspoint junctions. (a) Schematic of the junction structure and the electrical configuration during the measurement. (b) The virgin state *I-V* curves from three identical devices with different adhesion layers. (c), (d), (e) Electroforming and switching I-V loops for the three devices. The junction with no adhesion layer was formed, but could not be switched OFF even with very high current level. This device was shorted after experiencing a high current level (>30 mA). In contrast, the devices with a 5 nm Ti or Cr adhesion layer were formed and then readily switched OFF by an opposite bias.

measurement convention is that voltages were applied on the top electrode and the bottom electrode was grounded during the four-probe DC electrical measurements. The device with no adhesion layer had the lowest conductance and the one with the Ti adhesion layer had the highest conductance in the virgin state. Figure 1 c–e present the typical electroforming and switching I-V curves for these three samples. The devices with a 5 nm Ti or Cr adhesion layer were electroformed by a negative voltage sweep (magnitude > 6V) and then switched OFF with a positive 1 V bias (< 20 mA). Devices with no adhesion layer were also electroformed by a negative voltage, but they could not be switched OFF, as illustrated by several OFF switching attempts in Figure 1c. These devices were electrically shorted after experiencing a large current (~40 mA). Approximately 50 devices of each type were measured. The switchable device yield for the samples with either a 5 nm Ti or Cr adhesion layer was 98%. In sharp contrast, the no adhesion layer device yield was less than 10%.

The electrical results of these devices agree with the scenario that Ti or Cr can diffuse through the 15 nm bottom Pt electrode to react with the TiO_2 at the bottom interface during hot deposition of TiO_2 and form a locally reduced oxide, denoted TiO_{2-x} (i.e. an oxide characterized by significant oxygen vacancies). We propose this diffusion creates the seeds for subsequent growth of conducting channels during the electroforming process, significantly improving the post-electroforming switchable device yield and reducing the device variance compared to the samples prepared with no adhesion layer. This asymmetric diffusion-created oxygen vacancy profile also dictates the switching polarity of the device: switching ON typically occurs by applying a negative bias and OFF via a positive bias on the top electrode, independent of the subsequent electroforming process.[44]

The electronic transport of the device can be understood by considering the asymmetry of the top and bottom metal/oxide interfaces. The top interface can be described by a Schottky-like barrier while the bottom interface is typically much more electrically conductive due to the diffusion-created oxygen vacancy dopants. During switching, the conductive bottom interface sees a much smaller electric field than the Schottky-like top interface does and thus remains essentially unchanged. For switching ON, the drift of positively charged VOs in the electric field toward the negatively biased top interface effectively decreases the thickness of the insulating layer between the conducting channel and the top electrode, which decreases the device resistance. A positive bias repels the VOs away from the top interface and restores the insulating barrier, switching the junction back to the OFF state.[20] Since Cr metal has a weaker capability to reduce TiO_2 than Ti metal does due to a smaller free energy of formation for the Cr oxide, it produces fewer vacancies at the bottom interface and a more resistive

virgin state than the device with a Ti adhesion layer. The enthalpies of formation for TiO_2 and Cr_2O_3 are about 316 J/mole-atom and 226 J/mole-atom, respectively.[47] Therefore, Cr can reduce TiO_2 to a certain Ti sub-oxide but not to Ti metal. The device with no adhesion layer is the most resistive one in the virgin state because of the absence of oxygen vacancies created by the diffusion of an adhesion metal.

While the electrical results demonstrate the impact of the adhesion layer on the device properties, physical evidence is essential to confirm any diffusion of the adhesion metal. The interdiffusion of Ti and Pt layers has been studied over large areas at high temperatures of ~600 °C typical for ferroelectric device processing,[48,49] since this effect significantly degrades the electrical device properties in many cases.[50] We seek instead to understand diffusion effects with nanometer resolution for memristive Ti/Pt/oxide devices processed at low temperatures 150–250 °C, and thereby better exploit these effects to control and improve the performance of nanoscale memristive switches.

X-ray photoelectron spectroscopy (XPS) combined with ultra-high vacuum (UHV) sample annealing showed the appearance of buried adhesion layer Ti on top of an upper Pt film after annealing. A 5 nm Ti and then a 15 nm Pt film were evaporated on a Si/SiO_2 substrate. The sample was then transferred into an XPS chamber equipped with in-situ annealing capability. In the annealing process, the temperature was set to ramp up in 10 minutes, remain at the annealing temperature for 20 minutes and cool down in 30 minutes, duplicating as closely as possible the temperature conditions experienced by the Ti/Pt bottom electrode during TiO_2 sputtering for memristive device fabrication. XPS spectra shown in **Figure 2** were collected before and after in-situ annealing at different temperatures.

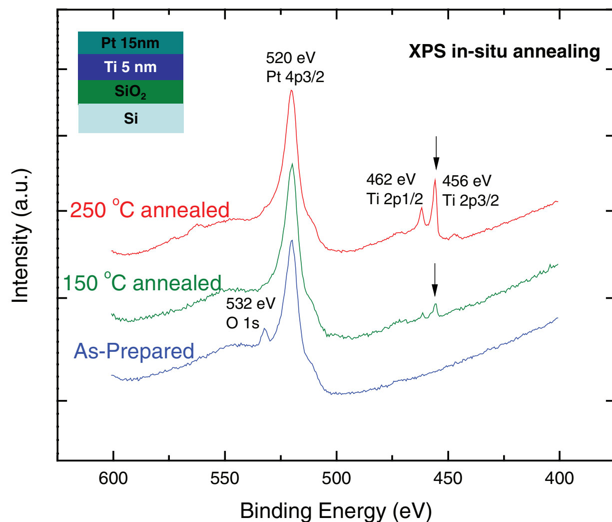

Figure 2. XPS spectra of Si/SiO_2/5nm Ti/15 nm Pt in the as-prepared, post 150 °C annealed and post 250 °C annealed states. The photoemission peak from Pt $4p_{3/2}$ at 520 eV suggests a metallic Pt before and after annealing. The annealing was done in-situ in the XPS UHV chamber. The small amount oxygen absorbed at the Pt surface disappeared after annealing. Ti 2p peaks started to be visible after 1 hr annealing at 150 °C and became significant after 1hr annealing at 250 °C. The energy of Ti peaks corresponds to Ti with some degree of oxidation.

The photoemission peak from Pt $4p_{3/2}$ at 520 eV corresponds to metallic Pt before and after annealing. The small amount of adsorbed oxygen on the Pt surface disappeared after annealing. No Ti peak was seen on the as-prepared sample. However, the Ti 2p peaks were visible (green in Figure 2) after annealing at 150 °C, indicating diffusion of the Ti adhesion layer though the 15 nm Pt layer. Further annealing of the sample at 250 °C resulted in a significant diffusion of Ti, as evidenced by the intense Ti 2p peaks (red in Figure 2). The binding energy of the Ti peaks ($2p_{3/2}$ at 456 eV and $2p_{1/2}$ at 460 eV) corresponds to Ti with some higher oxidation state, rather than metallic Ti.

Atomic level mapping of the diffused Ti via transmission electron microscopy (TEM) confirms inhomogeneous grain-boundary mediated diffusion of the Ti through the Pt electrode. In order to unambiguously identify the source of the diffused Ti atoms in the TEM sample, the Ti/Pt bottom electrode was annealed without sputtering TiO_2 on top of it. Cross-sectional energy-filtered transmission electron microscopy (EF-TEM) characterization was carried out for both as-prepared and 250 °C annealed samples. Similar to electron energy loss spectroscopy (EELS), EF-TEM filters transmitted electrons by energy, enabling chemical selectivity when the energy filter is modulated near a strongly absorbing element-specific ionization energy. EF-TEM maps were overlaid on high resolution TEM (HR-TEM) images shown in **Figure 3**, where the green dots represent the Ti-specific signal. As expected, the 15 nm Pt is a polycrystalline film with grain boundaries (GBs) visible in the HRTEM images. The grain size of the ambient temperature e-beam evaporated thin Pt layer (15~30 nm) is typically 5–10 nm (see Figure S1). For the as-prepared Ti/Pt bi-layer shown in Figure 3 a, the 5 nm Ti layer is uniformly distributed under the Pt layer with almost no Ti observed in the Pt layer. In sharp contrast, after annealing at 250 °C the thickness of the Ti adhesion layer is significantly reduced and many channels consisting of Ti are seen along the GBs of the Pt layer (Figure 3b). GB diffusion is typically 4 to 8 orders of magnitude faster than volume diffusion depending on the temperature, primarily due to the difference in the diffusion activation energies.[51–53] This results in nanoscale channels of diffused Ti atoms, which are about 0.5~1 nm in diameter in Figure 3 b, consistent with GB width in diffusion theory.[54]

The nanoscale Ti channels make thermal diffusion a very interesting approach for engineering the switching seed creation. The reasons are twofold: (i) this approach remains effective when the devices are scaled down to a few nanometers and (ii) ultra-small switching channels consume ultra-low power for switching operations. The density of the switching channel seeds may be manipulated by varying the grain size and thus the density of grain boundaries in the Pt layer (or other bottom electrode material). Deposition conditions can control the grain size of a pure Pt layer to some degree. The grain size can also be efficiently controlled by co-depositing a second element.[55] Direct lithographic patterning of the Ti adhesion layer would offer control over the switching site position. Selection of the adhesion layer material and annealing parameters further offers a large parameter space for device optimization, which may eventually lead to electroforming-free devices.

Engineered nanodevices validate the switching seed creation approach. Junctions of area 50×50 nm^2 and a nominal structure

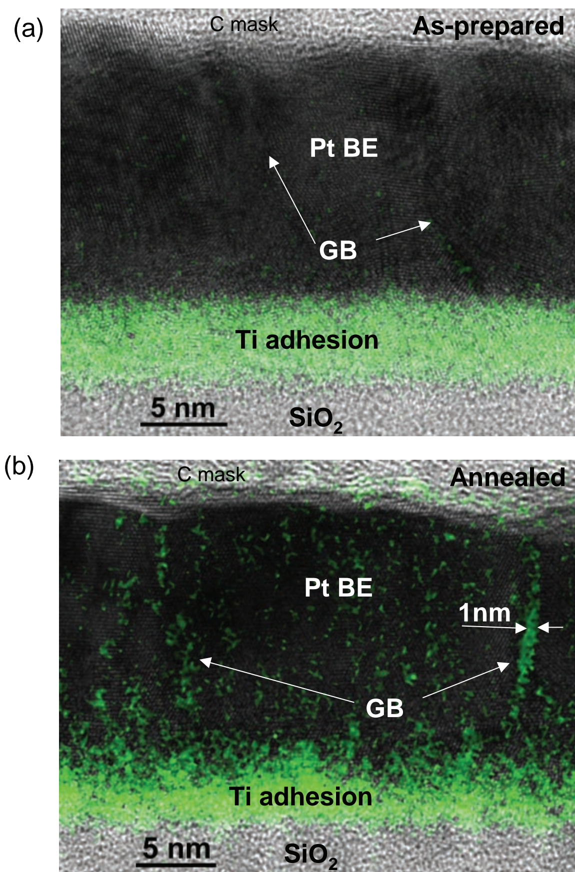

Figure 3. EFTEM maps of Ti overlaid on HRTEM images for the as-prepared (a) and 250 °C 1 hr UHV in-situ annealed (b) samples. The sample structure was Si/SiO_2 100 nm/Ti 5nm/Pt 15 nm and the C mask for TEM sample preparation with Focused ion beam (FIB) can also be seen on top of the Pt layer. The 5 nm Ti layer diffused though the Pt grain boundaries (GBs) after annealing. The width of the diffused Ti atom channels are about 0.5 ~ 1 nm.

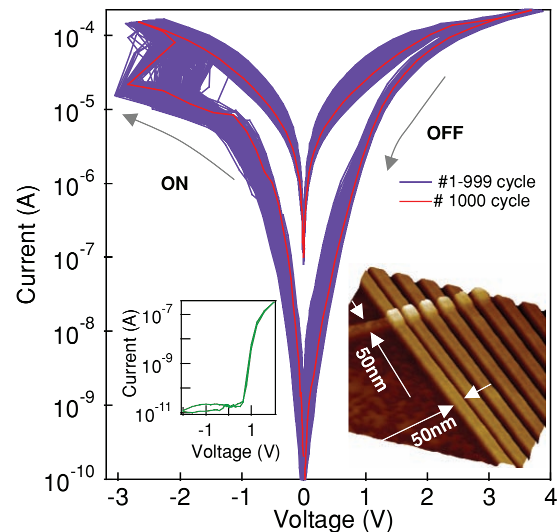

Figure 4. 1000 consecutive reversible bi-polar nonvolatile switching *I-V* loops from a Si/SiO_2/Ti (5nm)/Pt (15 nm)/TiO_{2-x} (40 nm)/Pt (30 nm) nano cross-point device. OFF/ON resistance ratio remains about 10^3 and no obvious degradation is observed after the 1000th switching loop (red). The inset on right presents the AFM image of 6 nano-junctions with the junction area of 50 nm × 50 nm. The virgin state *I-V* is highly rectified (inset on left) and this rectification orientation dictates the switching polarity of the junction. Voltages are applied on the top electrode and the bottom electrode is grounded for all these measurements.

of Si/SiO_2 (100 nm)/Ti (2 nm)/Pt (9 nm)/TiO_2 (40 nm)/Pt (11 nm) were fabricated by nanoimprint lithography. Ti metal from the underlying 2 nm Ti layer was diffused though the 9 nm Pt bottom electrode during the hot deposition of the TiO_2 layer at 250 °C. The electrical measurement results are given in **Figure 4**, where 1000 consecutive switching I-V loops were obtained with fixed ON and OFF switching voltage sweeps. After the 1000th switching loop (shown in red in Figure 4), no obvious degradation was observed and the ON/OFF conductance ratio remained about 10^3. The forming and switching voltages from device to device had narrow distributions with a spread of less than 1 V around their average values. A highly rectifying I-V curve was observed in the virgin state (inset) and the rectification direction and subsequent switching polarity both support the model of a top interface Schottky-like contact and a bottom interface Ohmic-like contact, consistent with the bottom interface heavily doped by Ti diffusion-created oxygen vacancies.

In conclusion, we have demonstrated a novel approach to seed nanoscale switching centers in memristive metal oxide switches by thermal diffusion of a reactive auxiliary metal through the electrode layer. These data highlight the unexpectedly important role that metal 'adhesion layers' can play in these oxide switches, which needs to be well understood in some medium or high temperature processes, such as the integration of resistance switches in a CMOS process. In the Ti/Pt/TiO_x/Pt devices studied here, thermally diffused Ti atoms formed nanoscale channels along Pt grain boundaries to penetrate the Pt electrode layer and locally reduce the TiO_x material at the Pt/TiO_x interface. Subsequent electroforming and electrical switching behavior was controlled by the diffusion materials. Engineering the nanoscale diffusion and 'seeding' improved the switchable device yield to 98% and controlled the switching polarity. Nanodevices of 50 × 50 nm^2 size validated the engineered diffusion approach. This engineering control may be expected to scale to devices as small as a few nanometers without significant difficulty, and may also transfer to other nitride- or sulfide-based memristive devices.

Experimental Section

The TiO_2 layer is amorphous according to X-ray diffraction (XRD) and transmission electron microscopy (TEM) (see Figure S2), and its composition is essentially stoichiometric TiO_2 according to the Rutherford backscattering (RBS) measurement (Figure S3). XPS depth profiles for the as-prepared and 300 °C 1 hr annealed micro devices confirmed the diffusion of Cr adhesion layer into the TiO_2 layer through the Pt bottom electrode. (Figure S4). The nanodevice has a junction area of 50 × 50 nm^2 with the nanowire electrodes fabricated by nanoimprint lithography (NIL). For micro-devices, both the top and bottom electrodes were patterned into 'dog-bone' structures by evaporation through a metal shadow mask to generate crosspoint junctions with an area of 5 × 5 μm^2. The electrical characteristics of the devices were carried out using the standard DC 4-point probe method and the voltage was applied

on the top electrode with the bottom electrode grounded. An HP 4155 semiconductor parameter analyzer was used without any additional circuit for the switching loop measurement. The TEM samples were coated with carbon and Ir as protective masks during focused ion beam preparation of ex-situ lift-out TEM cross-sections. TEM and EFTEM analyses were performed in a JEM2500SE with 200 kV accelerating voltage.

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