High Speed Differential Protection for Smart DC Distribution Systems

Steven D. A. Fletcher, Member, IEEE, Patrick J. Norman, Kenny Fong, Stuart J. Galloway, Graeme M. Burt, Member, IEEE

Abstract— This paper presents a high speed current differential implementation approach for smart dc distribution systems capable of sub-millisecond fault detection. The approach utilizes the natural characteristics of dc differential current measurements to significantly reduce fault detection times compared to standard applications and hence meet requirements for dc converter protection (around 2ms). Analysis is first developed to help quantify protection implementation challenges for a given dc system. Options for implementing the proposed technique are then illustrated. Results of scaled hardware testing are presented which validate the overall protection operating times in a low voltage environment. These results show the implementation approach can consistently achieve protection system operating within the order of a few microseconds.

Index Terms— Power system protection, dc power systems, microgrid, Fault currents

I. Introduction

THE use of dc for primary power distribution has the potential to bring significant design, cost and efficiency benefits to a range of power transmission and distribution applications. These advantages have been shown within microgrids, with [1], [2] showing that the possible reduction in conversion stages can equate to significant efficiency, and hence cost, savings. As a result of these and other benefits, dc systems are also being increasingly considered for use within aircraft [3] and shipboard [4], [5] applications, where the potential reduction in system weight (through the elimination of converters) could reduce fuel burn, and therefore provide system through-life cost reduction.

The use of active converter technologies within these networks is a key enabler for these benefits to be realized; however their integration can lead to exceptionally demanding electrical fault protection requirements. This is particularly true of standard Voltage Source Converters (VSC). These strict protection requirements result from the possibility of extremely high transient fault currents and severe transient voltage conditions within faulted converter interfaced networks, coupled with the relatively low fault tolerance of the converters [6], [7], [8]. Previous work from the authors [9] investigated a range of protection solutions and found that the use of unit protection schemes, and in particular current differential methods (which operate by comparing the magnitudes and/or relative directions of each current at the boundaries of a specified element within a network [10]), are required to meet these converter-driven protection requirements. However, economic and technical barriers still exist in the deployment of such schemes in smart dc distribution systems.

First, the need for device communication means that the installation costs of a current differential scheme can be substantial compared to an overcurrent scheme. This can also increase the weight and size of the protection system, negating some of the inherent benefits of adopting a dc distribution system. However, given the likely increase in the extent of sensor and communications infrastructures within distribution networks as smart grid concepts develop (both within microgrid and broader applications) [11], [12], [13], much of the required infrastructure may already be in place. This provides a natural route for the integration of more selective, communication-based, protection schemes which utilize this advanced infrastructure.

Second, whilst current differential protection methods are far less susceptible to the effects of variable fault levels and impedances than non-unit methods, achieving fault detection within the desired time frame in smart dc distribution systems is still a major challenge. Current differential protection applied in ac systems typically has a target operation time of 1–2 cycles (around 20 ms) [14], [15], which is an order of magnitude above that derived for compact converter fed dc networks (2ms was derived in [8]). One factor which prevents the reduction in operating time of an ac current differential system is the need for individual phase current measurement and phasor comparison [10]. This requirement does not exist for dc implementation, where only current magnitudes need to be compared. Furthermore, as dc current will be measured using a current transducer (such as a Hall Effect device) rather than via a current transformer, the sensor output will be voltage and this facilitates easier integration with digital processing devices. This paper presents an implementation method which utilizes these natural characteristics to significantly shorten the time for fault detection.

The paper will begin by presenting an analysis of the fault response of converter interfaced dc systems, with particular emphasis on how transient system behavior impacts the operation of current differential protection schemes. This

The authors are with the Institute for Energy and Environment, Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow G1 1XW, U.K. (e-mail: steven.fletcher@strath.ac.uk; patrick.norman@.strath.ac.uk; kenny.fong@.strath.ac.uk; stuart.galloway@strath.ac.uk; graeme.burt@strath.ac.uk).

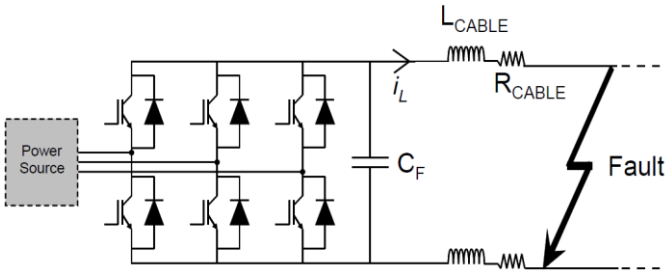

Fig. 1. Equivalent circuit of a faulted converter interfaced dc network

analysis will enable the quantification of the necessary protection system response times for fast and accurate fault detection. These will facilitate the identification of opportunities and challenges in utilizing smart grid communication infrastructure to fulfill protection functions in future smart dc distribution systems.

II. Analysis of Unit Protection Implementation Within DC Networks

To investigate the effectiveness of unit protection in achieving rapid fault detection and reliable selectivity for dc networks, this section will analyze the response of a current differential scheme for a typical section of dc network. This analysis builds on previous work by the authors (as summarized in section II-A1) which has been advanced to specifically enable the challenges in implementing current differential protection, such that the desired performance is achieved, to be quantified.

A. Differential current behavior

This section will first define expressions for the two measured currents at the input and output of the differential protection zone and their difference under various loading and fault conditions. This analysis helps to define the expected protection system operation times and assess the effect of measurement synchronization errors for the different load connections.

1) DC fault analysis building blocks

The equations which will be used to analyze converter interfaced dc networks have been presented by the authors in previous publications [9], [16] and are based on RLC analysis of the equivalent circuit in Fig. 1. These have been broken down into their constituent parts below to aid clarity and easy reference in later analysis. These equations are

$$i_{un}(t) = i_{un_v}(t) + i_{un_i}(t), \tag{1}$$

$$i_{un_v}(t) = \frac{v_{c_F}(0)}{L\omega_d} e^{-\alpha t}\sin(\omega_d t), \tag{2}$$

$$i_{un_i}(t) = i_L(0)e^{-\alpha t}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right], \tag{3}$$

$$i_{ov}(t) = i_{ov_v}(t) + i_{ov_i}(t), \tag{4}$$

$$i_{ov_v}(t) = \frac{v_{c_F}(0)}{L(s_1 - s_2)}(e^{s_1 t} - e^{s_2 t}), \tag{5}$$

$$i_{ov_i}(t) = \frac{i_L(0)}{(s_1 - s_2)}\left[e^{s_2 t}\left(s_1 + \frac{R}{L}\right) - e^{s_1 t}\left(s_2 + \frac{R}{L}\right)\right], \tag{6}$$

$$i_{(R-L)}(t) = i_L(0)e^{-\alpha t}. \tag{7}$$

The terms used in these equations are defined within Table I. The relative magnitudes of α^2 and ω_0^2 determine the form of the current response (and hence which equation is used), where $\alpha^2 > \omega_0^2$, $\alpha^2 = \omega_0^2$ and $\alpha^2 < \omega_0^2$ represent over, critically (not considered here) and underdamped fault responses respectively. A combination of the above equations will be exploited to examine the differential current response and define operating requirements for different circuit and fault conditions.

TABLE I
DEFINITION OF TERMS WITHIN EQUATIONS

Symbol	Definition
C_F	Converter output filter capacitance
v_{C_F}	Voltage across C_F
i_L	Current through line inductance
R	Fault path resistance (inc. line, fault, C_F ESR)
L	Fault path inductance
i_{un}	Underdamped current i_L
i_{ov}	Overdamped current i_L
i_{un/ov_v}	Part of $i_{un/ov}$ determined by $v_{C_F}(0)$
i_{un/ov_i}	Part of $i_{un/ov}$ determined by i_L (0)
$i_{(R\text{-}L)}$	Current response of a R-L circuit
α	$\alpha = \frac{R}{2L}$
ω_0	$\omega_0 = \frac{1}{\sqrt{LC_F}}$
ω_d	$\omega_d = \sqrt{\omega_0^2 - \alpha^2}$
$s_{1,2}$	$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}$

2) Analysis of response for internal zone faults

The current differential scheme should trip for faults inside this protected zone and remain immune to any external fault, and therefore it is important to be able to define the behavior of these fault types and establish expected protection system operation times. The following subsections illustrate how this can be achieved for different loading conditions. In order to provide greater clarity in the findings, analysis is presented for a single load connected to the supply converter and initial case studies contain only a single protection zone.

a) Fault response with passive load

To illustrate the operation of the current differential scheme with the connection of a passive load, consider the network in Fig. 2.

The current differential scheme detects faults on the generator to busbar line by comparing the difference between i_a and i_b , i.e. $\Delta i = i_a - i_b$. To analytically quantify the response of the scheme to a fault within the protection zone, i_a and i_b must be defined. Within Fig. 1 i_a flows around an RLC circuit, meaning its response will be second order. i_b flows around a

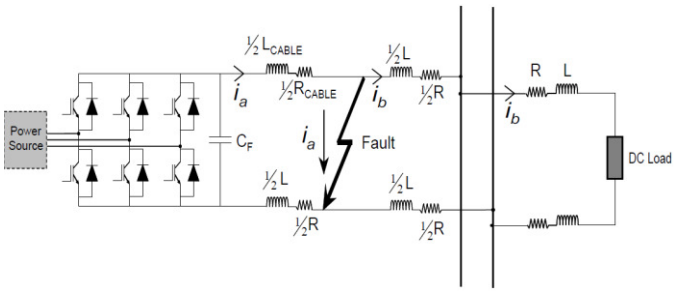

Fig. 2. Current differential scheme with passive load connected

section of circuit containing only resistors and inductors and its response will be first order. For these two currents to be clearly defined, it is assumed that no current from i_a flows into i_b and vice versa. This gives an accurate response for short circuit faults but is more approximate for impedance faults.

The form of the expression will depend on the damping conditions in the circuit. For underdamped circuit conditions $i_a = i_{un_a}$. Here i_b will be driven only by the stored energy in the inductance and therefore $i_b = i_{(R\text{-}L)_b}$. As stated, the differential current sum is equal to

$$\Delta i = i_a(t) + i_b(t), \tag{8}$$

Substituting for the above i_a and i_b into (8) it becomes

$$\Delta i = i_{un_a}(t) + i_{(R-L)_b}(t). \tag{9}$$

Some simplification of (9) is possible through the collection of equal terms but this does not provide significant additional insight into the differential current behavior.

Where overdamped circuit conditions exist $i_a = i_{ov_a}$ but the expression for i_b remains the same. The expression for Δi now becomes

$$\Delta i = i_{ov_a}(t) + i_{(R-L)_b}(t). \tag{10}$$

In equations (9) and (10) the dominant term will come from v_{C_F} (0) (as established in [9], [16]). Yet when assessing differential current, the initial current may have more impact as the energy stored in the line inductance initially maintains current flow to the load. This will affect the time at which Δi exceeds the threshold level (the threshold being the magnitude of Δi at which the differential scheme operates; this is non-zero due to measurement uncertainty [10]). The extent to which this current is maintained is dependent on the ratio of R_b and L_b, as shown by the exponential term in (7).

As (9) and (10) show the expected differential current behavior, they facilitate the accurate evaluation and assessment of associated protection schemes. For example, (9) and (10) could potentially be used when establishing the expected protection operating time for a range of current difference thresholds.

b) Fault response with active load

The response of the current differential scheme will change with the connection of a converter interfaced (also known as active) load type due to the contribution of the load capacitor into the fault. This can be seen from the network diagram in Fig. 3.

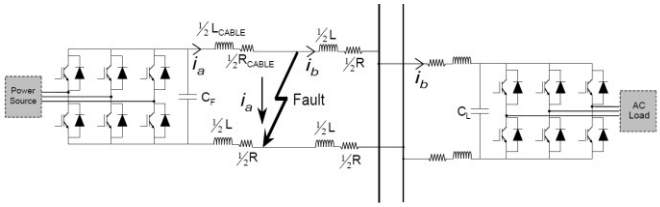

Fig. 3. Current differential scheme with active load connected

First, assuming underdamped conditions for both i_a and i_b, Δi is given by

$$\Delta i = i_{un_a} - \left(-i_{un_{v_b}} + i_{un_{i_b}}\right) \tag{11}$$

which becomes

$$\Delta i = \left(i_{un_{v_a}} + i_{un_{v_b}}\right) + \left(i_{un_{i_a}} - i_{un_{i_b}}\right) \tag{12}$$

Equation (12) shows that the two initial voltage terms sum to increase Δi compared to the passive load case. This is due to the opposite polarity of the two fault currents. This will lead to any operating threshold being met more quickly and hence faster operation of protection (provided current is measured directionally as opposed to purely on magnitude).

As the two RLC circuits have a distinct response, the discharge current behavior is different for the two circuits. Therefore the damping conditions for the two circuits are not necessarily the same. If necessary, alternative damping cases can be investigated by substituting appropriate current equations from section II-A1 into (12).

3) Response for external zone faults

For any fault external to the protected current differential zone it has been assumed that $i_a(t) = i_b(t)$ as current flow in line capacitance should be negligible given the large difference between network filter capacitance and anticipated line capacitance for applications considered in this paper (for example, [15] quotes line capacitance of 0.1nF/m).

III. Quantification of Inherent Implementation Challenges

Reference [9] introduced two key challenges in the implementation of unit protection schemes within dc networks. These were:

1) The synchronization of current measurements under high di/dt conditions.
2) The comparison of current measurements and subsequent output of trip signals within the required time frame.

The following sections will demonstrate how the previous analysis can be used to quantify the above issues and hence define the protection implementation requirements for a given network and set of fault conditions.

A. Implementation challenges when operating under high rate of change of current fault conditions

Time synchronized measurements are required for a current differential scheme to operate accurately [10]; otherwise errors can occur in the differential sum. However where a high di/dt exists (often the case during faults in compact dc systems), this can be difficult to achieve.

There are a number of sources of this poor time synchronization. These include timing errors between communicating devices (even where devices are synchronized through GPS time stamping) [14] and non-synchronous current sampling, with differences considered negligible in the time scales of traditional protection system implementation still potentially problematic for fast acting protection. In terms of network protection, the main impact of poor time synchronization would be to reduce the stability of the protection system during faults outside of the current differential zone (reducing the capability of the protection scheme to not operate for faults external to its zone of protection). Some operating time delay would be anticipated for internal faults but not to the extent that it would significantly impact protection functionality (this can be investigated using equations in section II-A2).

For any fault external to the protected current differential zone $i_a(t) = i_b(t)$ and so the differential sum should be equal to zero (again with the exception of current flow in and out of line capacitance). However, where current measurements are not exactly synchronized, a non-zero differential sum may result during periods of high di/dt. For these cases the current differential expression is now

$$\Delta i = i_a(t) + i_b(t + \Delta t), \tag{13}$$

where Δt is the difference in measurement time between i_a and i_b. di/dt is likely to be greatest with underdamped circuit conditions, which will be considered here to assess the worst case scenario. Substituting underdamped expressions, (13) becomes

$$\Delta i = i_{un_a}(t) + i_{un_b}(t + \Delta t). \tag{14}$$

Fig. 4 provides an example of how (14) can be used to quantify the current error caused by measurement non-synchronization for a relevant sample of measurement time differences (fault occurs at t=0). This plot considers the output of the source converter capacitance for a short circuit fault on a passive load within a dc network, such as that illustrated in Fig. 2. Example network parameters are shown in table II. These are derived from [15], with distance to fault (d_f) representative of microgrid systems and $i_L(0)$ based on a pre-fault supply to a 50kW load at 400V.

Fig. 4 shows that the difference in the time at which i_a and i_b are measured causes a non-zero current differential sum over the initial capacitor discharge period. The magnitude of this error is proportional to the difference in measurement time. The figure shows that there are short periods of high differential current and more importantly plot (c) shows that

TABLE II
EXAMPLE DC MICROGRID NETWORK PARAMETERS

$v_{C_F}(0)$	$i_L(0)$	R/metre	L/metre	C_F	$C_{F_{ESR}}$	d_f
400V	125A	0.64mΩ	0.34μH	56mF	2mΩ	35m

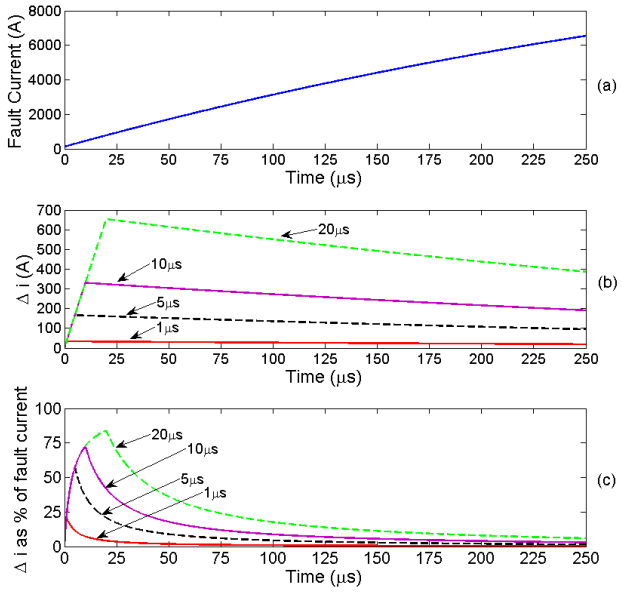

Fig. 4. Calculated DC microgrid response for: (a) fault current (b) Δi for a range of time synchronization errors (c) Δi as a percentage of fault current

this current can initially be high proportion of overall fault current. This would potentially cause major issues for protection coordination in unit schemes, particularly where proportional current biasing is employed [10]. As it is desirable that the scheme correctly detects faults under transient conditions it will not necessarily be possible to wait an extended period of time to filter out these erroneous current differences. Therefore it is essential that these synchronization issues are accounted for in the protection scheme design. An approach to achieving this is presented in later sections.

B. Assessment of differential current scheme response within target operating time

The previous analysis allows for the derivation of the time at which a certain differential current threshold would be reached. Combining this derived time parameter, termed $t_{\Delta i}$, with the overall required operating time (t_{op} - determined by the robustness of the specific converter and associated components) enables the time allowed for the current differential relay/decision making element stage of the protection operation process (t_{dp}) to be quantified.

Also including the circuit breaker operating time (t_{cb} - identified in [16] as an important aspect to consider when implementing fast acting protection), the required differential device calculation time can be defined as

$$t_{dp} = t_{op} - t_{cb} - t_{\Delta i}. \tag{15}$$

The term t_{dp} in (15) enables the selection of an appropriate

processing technology to meet the protection criteria. This can be highlighted with an example calculation. For this calculation the same network parameters as described in table II will be applied with the exception of d_f , which will be reduced to 20m to represent an internal zone fault, and the additional of an arbitrary constant differential current threshold of 100A (i.e. once $\Delta i \geq 100A$ then the protection should operate). A constant current threshold, as opposed to a percentage bias, has simply been chosen for clarity.

For the scenario described, the time at which $\Delta i \geq 100A$ can be calculated to be 0.9µs (from (9)). If this time is substituted into (5) along with the target maximum operating time (say 2ms in this case, as derived in [8]) and an appropriate circuit breaker operating time ([10] presents a hybrid breaker option which can operate in the order of 500µs), (15) becomes

$$t_{dp} < 2000\mu - 500\mu - 0.9\mu. \quad (16)$$

The allowed processing time of the differential device would therefore be approximately $t_{dp} < 1.5$ms, which is far shorter than the traditional operating speed of differential protection systems. The following sections will however present an implementation method which can easily meet this operating requirement.

IV. Proposed Method of High Speed DC Differential Protection Scheme Implementation

To achieve fast coordinated protection system operation whilst also overcoming any synchronization issues, the authors propose the use of a central processing device to compare current measurements (a concept initially introduced in [16]). This could involve either physically summing currents prior to the central device or the direct input of analogue measurements to the central device, where analogue to digital conversion would take place, before the sum of currents is compared to the trip threshold and a decision sent to the circuit breakers. This type of approach takes advantage of the natural properties of dc differential implementation - the necessity for only magnitude and polarity comparison, sensor output in the form of voltage and inherently higher bandwidth sensors (compared to current transformer interfaces) - to reduce fault detection time by at least an order of magnitude below that of standard AC current differential schemes. A proposal for how this may be implemented is described in the following subsection. The subsequent sections go on to demonstrate the successful implementation this approach in a scaled down hardware environment.

A. Current differential scheme with sampled current summing

One means of implementing the proposed protection method is to use a central microcontroller which converts all analogue measurements to digital form before they are summed and compared to a trip threshold. Fig 5 illustrates

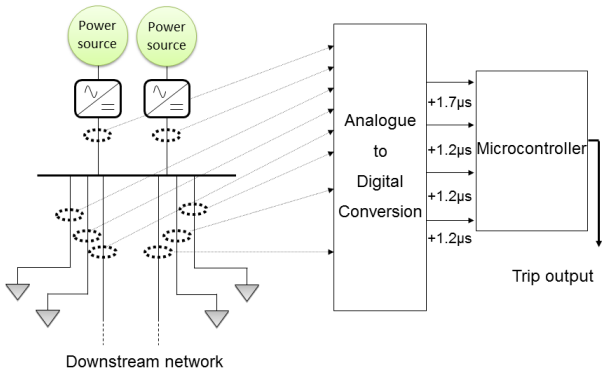

Fig 5. Proposed current differential scheme with individually sampled currents digitally summed

how this may look on an example network. This approach performs the differential calculation on the microcontroller itself. Its performance partly depends on the capability of the chosen processing device to implement an A/D conversion on multiple current measurements and so ensure synchronization of compared currents.

To provide an example of how this might impact functionality, consider a device such as Freescale's MCF52235 Coldfire Microprocessor [18] fulfilling this function. This particular device has two A/D converters, allowing two measurements to be converted simultaneously. These are stored in memory as the subsequent two measurements are converted and so on until all inputs are converted (with a maximum of 8 inputs). At this point the summing and comparing algorithm is run. As all inputs are not converted simultaneously, the synchronization error between each pair of measurements is equal to the time taken to convert the previous inputs. The first conversion takes 1.7µs with subsequent conversions taking 1.2µs, as Fig. 5 highlights, meaning that many microseconds of synchronization error can develop where more than two measurements are compared (such as for busbar protection).

Despite these issues, this approach also has the potential to deliver the fast decision making time required by the fault detection systems. The following section describes how the key performance assumptions within the proposed sampled current differential implementation methods have been validated in hardware.

V. Scaled Hardware Demonstration of Sampled Current Differential Scheme

Preliminary validation of high speed differential protection has been performed within a low voltage laboratory environment using the experiment set up represented in Fig. 6. This set up was designed to capture the main circuit elements which influence converter interfaced dc networks' fault response whilst being robust enough to safely emulate fault conditions. With the lower voltage and energy levels considered (compared to full scale application) the experimental emphasis was on: data acquisition; implementation of protection algorithms and subsequent

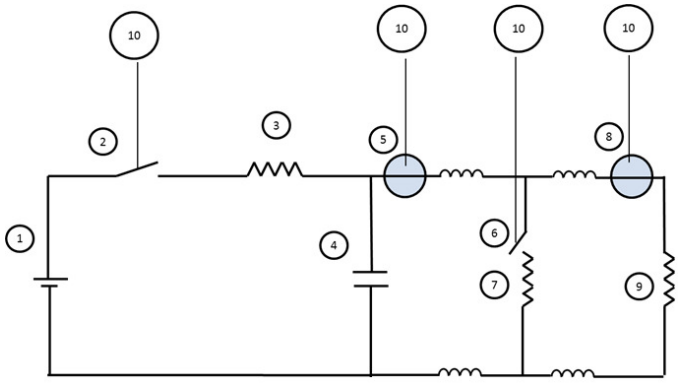

Fig 6. Low voltage high speed DC differential lab based validation set up

TABLE III
DETAILS OF EXPERIMENTAL HARDWARE

No.	Function	Hardware	Experimental test settings
1	Power supply	30V, 2A Bench Power Supply	Set to 18V constant voltage
2	Disconnect supply prior to fault	Semikron SKM 111 AR MOSFET [20]	100V nominal, 200A nominal (600A max)
3	Current limiting	Resistors	2.2Ohms
4	Emulate power converter interface capacitor	BHC Components ALS30A103KE100 capacitor	10mF, Charged to 16-17V ($v_C(t)$).
5	$i_a(t)$ Current measurement	LEM HAS 200S [21]	50A/V measurement ratio
6	Introduce fault path	Semikron SKM 111 AR MOSFET [20]	100V and 200A nominal (600A max), switching times ≈200ns - 1µs (possible from datasheet)
7	Fault current path	Cable and other in series resistance	4 m of 10mm^2 (≈1.2µH) AWG cable.
8	$i_b(t)$ Current measurement	LEM HAS 200S [21]	50A/V measurement ratio
9	Representative load	Resistors	75Ohm
10	A/D conversion, current comparison, protection signaling	NI CRIO-9114 FPGA [19], NI 9223 AI module [22], NI 9401 DO/DI module [23]	1MS/s/channel analogue input, 10MS/s/channel digital output. Control loops set at ≈ 1µs (FPGA can provide ≥300ns possible)

signaling; and the circuit breaker/protection system interface and associated switching times, all against a realistic fault current profile.

The experimental set up replicates a rail to rail short circuit fault occurring between the boundaries of the power converter interface capacitor and the subsequent electrical zone/s. The response time of the power converter control itself is beyond that of the initial transient and as such can be neglected for the purposes of this experiment. Table III details the components utilized, with the numbered rows relating to the components in Fig. 6. From the table, i_a (t) and i_b (t) are the current measurements at the respective boundaries of the differential protection scheme. The data acquisition and control functions were built around a NI CRIO based FPGA to help accelerate available processing speed [19]. The use of the FPGA front end also ensures measurement synchronization through the input of analogue measurements to simultaneously sampled channels. The fault introduction and tripping function made use of a common MOSFET switch. This also allowed the demonstration of achievable speeds using a solid state circuit breaking solution within the circuit (the operating time of which makes best use of high speed detection).

Using the equipment described, the outline of the experimental procedure is as follows:

1) Connect source to circuit containing capacitor and resistive loading at establish initial conditions (by closing 2 in Fig. 6)
2) User command for fault introduction sequence (10). This includes:
    a) Disconnecting source from circuit at 100µs before fault introduction (by opening 2)
    b) Initiating the protection algorithms (10). Continuously measure (5) and (8) and compare against protection thresholds
    c) Introducing low impedance fault path (by closing 6)
3) Protection algorithm continuously monitoring measurements (5) and (8) as before until threshold is exceeded
4) Once exceeded generate trip signal and remove fault path (by opening 6)

The fault response of the experimental setup is shown in Fig. 7 (a) without the operation of any protection devices. Within this figure, i_a (t) carries the main fault current component and has a peak of around 280A occurring at approximately 240µs after fault initiation. Capacitor voltage $v_c(t)$ decays over the period of the fault (measured at a 6:1 ratio) and $i_b(t)$ is minimal as expected (given the current mainly flows through the fault path once it is introduced). Finally, the output labelled as 'Trip Indicator' remains 'on' (the MOSFET driver circuit TTL signal where the 5V high occurs when the MOSFET switch is closed) which indicates the protection system does not operate.

Fig. 7 (b) and (c) illustrate the protection system operation for two specific Δi threshold settings. Within Fig. 7 (b), the threshold is set to 90A. The figure demonstrates that as i_a (t) approaches this current (Δi approximately equals i_a (t) due to the small magnitude of $i_b(t)$) then the protection system rapidly responds by issuing a trip signal and opening the MOSFET switch. This is issued at 41.31µs, with much of this time owed to the development of the current up to the threshold level. The positive impact of this quick operation is also evident from Fig. 7 (b), where it can be seen that both peak fault current and voltage depression is minimized. This performance could lead to wider system operating benefits. The potential of the implemented method is demonstrated further in Fig. 7 (c) (which is on a smaller timescale), where threshold is set to 0.6A. In this case, protection operation begins at just 7.37µs. This result highlights that protection operating times can be brought down to just a few microseconds where smaller thresholds are acceptable (though

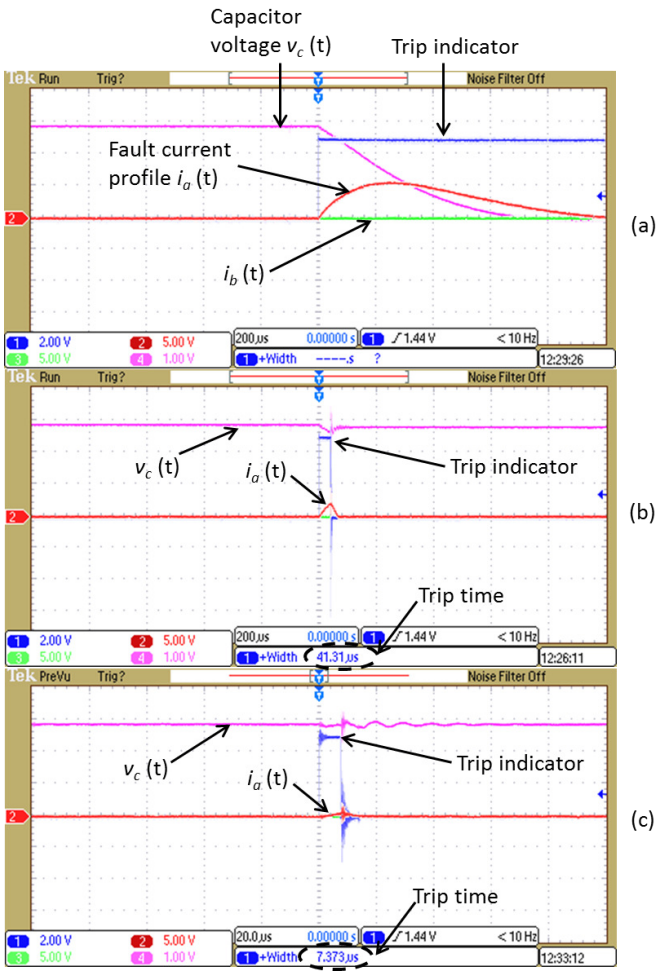

Fig. 7. Oscilloscope traces of the fault response of the experimental setup with (a) no protection operation, (b) protection set to a threshold of Δi=90A,(c) protection set to a threshold of Δi=0.6A (zoomed view)

TABLE IV
DIFFERENTIAL PROTECTION SYSTEM OPERATING SPEEDS FOR VARIOUS CURRENT THRESHOLDS

Test	Operating threshold for $\Delta i(t) = i_a(t) - i_b(t)$	Response
1	0.6A	Trip begins at ≈ 7.37μs
2	6A	Trip begins at ≈ 9.53μs
3	10.5A	Trip begins at ≈ 11.21μs
4	21A	Trip begins at ≈ 13.59μs
5	30A	Trip begins at ≈ 17.8μs
6	60A	Trip begins at ≈ 27.53μs
7	90A	Trip begins at ≈ 41.01μs
8	285A	No Trip

this will be application specific).

A number of additional test scenarios were run using the experimental set up to assess the operating time of the proposed approach for a wide range of trip current thresholds. Table IV summarizes the results from the full suite of tests performed.

These results provide a strong validation of the proposed protection concepts - with the trip signal being generated in a matter of microseconds for the various test scenarios. The main factor varying the operating time for these scenarios is the increase in current threshold, where a longer time is taken to reach this threshold (as is predictable from earlier analysis). Therefore the complete protection system can consistently be operated within a few microseconds.

This conclusion demonstrates the ability of the proposed method to meet the operating requirements derived in section III. Therefore, in conjunction with appropriate circuit breakers, the method is shown to be a viable method of delivering very fast, coordinated protection operation.

VI. FUTURE WORK

With the preliminary set of results obtained, the next stage is to increase the operating level of the system to be more representative levels of practical applications. Within this higher voltage environment a number additional functions and tests are planned to prove the validity of the proposed implementation method. These include: the incorporation of a dedicated circuit breaker in addition to the fault path switch and more rigorous testing of protection scheme stability (to external zone faults) and reliability (for both internal and external faults).

Methods of overcoming measurement synchronization errors will also be studied to accommodate cases where the physical connection of analogue measurements to a central point may be more difficult to achieve, such as for physically larger networks or in an electrically noisy environment, in which case communications would likely be employed. Further areas of work will also look to develop more readily deployable processing technology to fulfill the functionality described in previous sections.

VII. CONCLUSIONS

The adoption of fast acting fault detection technologies is a key step in overcoming the protection challenges associated with dc networks. It enables better use of high speed circuit breaking technologies (hybrid and solid state) which in turn meets the requirement for converter protection against dc side faults. This paper investigates the potential for current differential protection to provide this fast detection function. It presents a number of analytical steps to quantify network fault response and subsequent detection and operational challenges. A method of implementing current differential protection is then presented which overcomes these challenges. The method utilizes the natural characteristics of dc differential current measurement to achieve very fast fault detection. Scaled hardware results of this method show the potential for consistent protection system operation within only a few microseconds. This is a significant reduction in detection time compared to traditional application of current differential protection. Successful replication of these results at a larger scale would be a significant step towards achieving highly effective protection for dc networks.

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Steven Fletcher (M'13) received his BEng degree in electrical and electronic engineering from the University of Strathclyde, Glasgow, U.K in 2007 and his PhD degree from University of Strathclyde in 2013, following research into dc network protection. He is currently a research associate within the Institute for Energy and Environment at Strathclyde. His research interests include the design, modelling and protection of microgrid, marine and aerospace power systems.

Patrick Norman is a lecturer within the Institute for Energy and Environment at the University of Strathclyde. He received his BEng (Hons) degree in electrical and mechanical engineering and PhD in electrical engineering from the University of Strathclyde. His research interests lie in the modelling and simulation, design, control, protection of aircraft secondary power offtake and distribution systems, microgrid and shipboard power systems.

Kenny Fong received his MEng degree in electrical and mechanical engineering from the University of Strathclyde, Glasgow, U.K in 2008. He is currently a research assistant within the Institute for Energy and Environment at Strathclyde and is working towards an engineering doctorate. His main research interests are in dc protection and shunt active filtering for aerospace applications.

Stuart Galloway received his Bachelors degree in Mathematical Sciences form the University of Paisley in 1992. He obtained his M.Sc. degree in Non-linear Modelling (1993) and PhD in Numerical Analysis (1998) from the University of Edinburgh, UK. Since 1998 he has been researching optimisation problems in power systems, electricity markets and novel architectures relating to aero and marine electrical systems. He is currently a Reader in the Institute for Energy and Environment at the University of Strathclyde.

Graeme M. Burt (M'95) received the B.Eng. degree in electrical and electronic engineering from the University of Strathclyde, Glasgow, UK, in 1988, and the Ph.D. degree from the University of Strathclyde in 1992, following research into fault diagnostic techniques for power networks. He is currently a Director of the Institute for Energy and Environment at the University of Strathclyde, where he also directs the University Technology Centre in Electrical Power Systems sponsored by Rolls-Royce. He is a professor of electrical power engineering, and has research interests in the areas of: integration of distributed generation; power system modelling, real-time simulation, protection and control; microgrids and more-electric systems.