CMOS MESFET Cascode Amplifiers for RFIC Applications

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved March 2019 by the
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May 2019

ABSTRACT

There is an ever-increasing demand for higher bandwidth and data rate ensuing from exploding number of radio frequency integrated systems and devices. As stated in the Shannon-Hartley theorem, the maximum achievable data rate of a communication channel is linearly proportional to the system bandwidth. This is the main driving force behind pushing wireless systems towards millimeter-wave frequency range, where larger bandwidth is available at a higher carrier frequency. Observing the Moor's law, highly scaled complementary metal–oxide–semiconductor (CMOS) technologies provide fast transistors with a high unity power gain frequency which enables operating at millimeter-wave frequency range. CMOS is the compelling choice for digital and signal processing modules which concurrently offers high computation speed, low power consumption, and mass integration at a high manufacturing yield. One of the main shortcomings of the sub-micron CMOS technologies is the low breakdown voltage of the transistors that limits the dynamic range of the radio frequency (RF) power blocks, especially with the power amplifiers. Low voltage swing restricts the achievable output power which translates into low signal to noise ratio and degraded linearity. Extensive research has been done on proposing new design and IC fabrication techniques with the goal of generating higher output power in CMOS technology. The prominent drawbacks of these solutions are an increased die area, higher cost per design, and lower overall efficiency due to lossy passive components. In this dissertation, CMOS compatible metal–semiconductor field-effect transistor (MESFETs) are utilized to put forward a new solution to enhance the power amplifier's breakdown voltage, gain and maximum output power. Requiring no change to the conventional CMOS process flow, this low cost approach allows direct incorporation of high voltage power MESFETs into silicon. High voltage MESFETs were employed in a cascode structure to push the amplifier's cutoff frequency and unity power gain frequency

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to the 5G and *K*-band frequency range. This dissertation begins with CMOS compatible MESFET modeling and fabrication steps, and culminates in the discussion of amplifier design and optimization methodology, parasitic de-embedding steps, simulation and measurement results, and high resistivity RF substrate characterization.

# DEDICATION

*To my parents and sister*

# EPIGRAPH

"If you're on the path

Don't despair of the distance

Arrival is the art of stepping through time

What fear of darkness?

When my soul ignites fires

And a hundred dormant suns

From my cold ashes rise"

—H. E. Sayeh

answered my endless questions with patience and a welcoming smile and helped me with all the documentations.

Last but not least, I am fully indebted to my parents, Parisa and Alireza, to whom I owe all that I am. They have unconditionally loved and supported me through thick and thin, and their selfless sacrifices have been the wind beneath my wings. I am blessed to have a little angel by my side; my sister Pegah who has always been there for me. I express my gratitude to my grandmother, Parvin, and my aunt, Pooneh, who always inspired me. Ever since I left the motherland, my family has been present in my heart perpetually. Finally, I am grateful to my nurturing cousin, Ramin, whose support was not withdrawn momentarily.

Payam Mehr
Scottsdale, AZ
February 2019

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CHAPTER 1

INTRODUCTION

The semiconductor industry is trending towards circuit manufacturing technologies which are lower in cost, higher in efficiency and integration of features, and more reliable. Complementary metal-oxide semiconductor (CMOS) is widely adopted since it offers mass integration of MOSFET transistors with lower cost. Silicon on insulator (SOI) substrates are also used in CMOS processes since they reduce parasitic capacitances, leakage current, have better sub-threshold swing and higher drive current [1]. CMOS technology is continuously scaled down to decrease the feature size and increase the integration of transistors, as well as lowering the supply voltage and power of the system which are all advantages for digital designers. However, the maximum allowable voltage on the scaled technology nodes is limited and is getting lower still as the technology is further scaled down. Lower voltages means lower output power and is not desirable for RF designers. RF blocks such as power amplifiers (PA) are high power devices (preferably more than a Watt) and the lower supply voltage of scaled technology nodes impose an undesirable restriction for the RF designers to achieve high powers. This problem will limit the usefulness of SOI CMOS technology for RF applications despite of all its advantages.

To overcome the low-output-power problem in scaled technology nodes, PAs are mostly fabricated in GaAs technologies which are more expensive, but offer higher cutoff frequency ($f_t$), operating voltage, and better linearity. On the other hand, the mobile communications industry is pushing towards fully integrated CMOS processes due to the aforementioned reasons [2]. Furthermore, high transistor cutoff frequencies are now attainable in deep sub-micron technologies and integration of RF and digital CMOS circuits is now feasible. Hence, it is worth investigating solutions to increase the operating

voltage of deep sub-micron technologies. As the transistor size becomes smaller, the breakdown voltage of the transistor also decreases and this is the main reason why we cannot apply higher operating voltages. Lateral-diffused MOSFETs (LD-MOSFET) were developed to increase the breakdown voltage to possibly over 100V by creating a lateral-drift region between the end of the channel and the drain region [3]. To fabricate LD-MOSFETs, some process modifications need to be made to the CMOS process which make them more expensive and not suitable for all applications. This type of transistor also uses a thicker gate oxide which degrades the frequency performance of the device. Another technique is higher impedance transformation which reduces voltage swings on the transistor which leads to higher supply voltage value. But this technique causes more losses in the matching network and the overall efficiency is not high [4]. Another common solution is to use several die which have been fabricated in different technologies and embed them into one module. These modules usually contain a GaAs power amplifier, a pseudomorphic high-electron-mobility-transistor RF switch, and a high voltage CMOS power management die which are all bounded to a laminate [5]. Obviously, we need different technologies and processes to make such a module and the final price of the product will be high.

One of the best solutions to increase the operating voltage of deep sub-micron technologies which has been studied by our group is using SOI metal-semiconductor-field-effect-transistors (MESFET). Silicon on insulator MESFETs are CMOS compatible devices and can be fabricated with no change to the process [6]. More well-known GaAs MESFETs are not CMOS compatible. The breakdown voltage of the MESFET depends on the transistor size and geometry and also the process technology, and is at least 2-15 times greater than MOSFET transistors. Other advantages of MESFETs are depletion mode operation [7] and radiation tolerance [8].

CHAPTER 2

CMOS SOI MESFETs

The demand for low-cost CMOS RFICs is being driven by a number of rapidly growing markets including consumer wireless devices, automotive electronics as well as the anticipated Internet of Things. High-volume CMOS foundries are well positioned to support this anticipated demand using commercially successful digital platforms. However, the low operating voltage of the digital CMOS is challenging for RFIC design, especially for any power blocks including the RF power amplifier (PA). In this chapter the enhanced voltage handling capability of a CMOS-compatible MESFET is investigated as an approach which can be adopted to generate higher output power level PAs than conventional methods and transistors in CMOS technology. The device structure and manufacturing considerations, design tradeoffs, DC and RF characterization, the effect of substrate bias on DC performance, and modeling of the CMOS compatible MESFETs are discussed in this chapter.

2.1.    CMOS MESFET Fabrication

MESFETs can be fabricated with no changes to the standard CMOS process flow [9]. The key process requirement is the availability of a silicide block step, which is commonly available to form passive resistor components in the active silicon layer. For MESFET fabrication the silicide block is used to create spacer regions between the gate and the source (source access length, $L_{aS}$), and between the gate and the drain (drain access length, $L_{aD}$). The gate length ($L_G$) is also controlled by the distance between the source and drain spacers. The MESFET cross section is shown in Figure 2.1.

The transistor gate oxide breakdown is an important limitation in increasing the operating voltage in CMOS technology. As the technology scales down, the transistor gate oxide thickness decreases. Large voltages applied to the transistor gate increases the electrical stress on the device:

$$E = \frac{V_{ox}}{t_{ox}} \tag{2.1}$$

Narrower gate oxide increases the electric field intensity at the gate terminal of the transistor and to avoid the oxide breakdown, lower voltages should be applied. The gate of the MESFET transistor as shown in Figure 2.1, does not have an oxide layer and consists of a silicide layer which is formed above the lightly doped n-channel. Therefore, the gate is a metal-semiconductor junction and behaves like a Schottky diode and the barrier height controls the voltage swing on the gate [6]. Hence, the MESFET gate can tolerate higher voltages which comes at a price however. The current leakage flowing through the Schottky junction is large and varies exponentially with the voltage on the transistor gate. This can generate large gate leakage currents flowing out of the gate at higher supply voltages and increases the power dissipation.

Another cause of the transistor breakdown in deep sub-micron technologies is the drain-source breakdown which happens due to the strong electric field between the two terminals as the supply voltage increases. The MESFET contacts are not self-aligned and this characteristic can be used to increase the voltage handling capability of the device. If the drain and source access lengths are increased, the electric field between the gate and source/drain junctions also plummets. The source of the transistor is often grounded. The quiescent gate voltage is also set to be close to 0 V in the scope of this thesis as a $V_{GS} \sim 0$ V maximizes the MESFET transconductance which will be discussed later. As a result, a huge voltage drop across the gate-source junction is not expected and $L_{aS}$ does not need to be

extended extravagantly. However, the main purpose of deploying MESFETs is increasing the supply voltage (as high as 15 V) to increase the output power. Considering the range of voltages on the gate terminal, the electric field on the gate-drain junction will be much more intense, and $L_{aD}$ should be elongated more than $L_{aS}$ to mitigate the electric field at the gate-drain junction if higher breakdown voltage is needed.
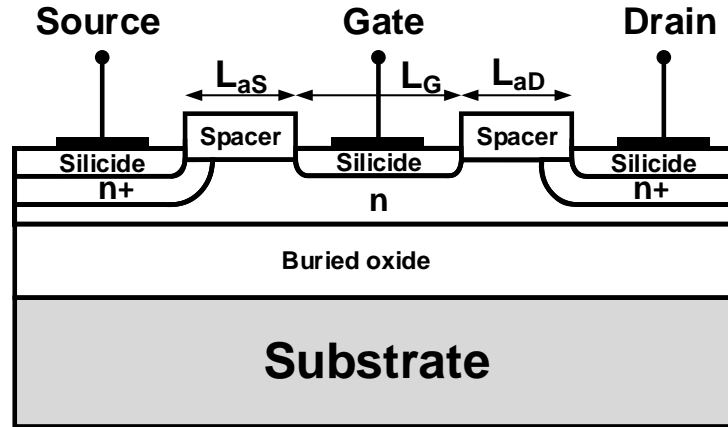


Fig. 2.1. Cross section view of an N-type SOI MESFET transistor on a P-type substrate.

The silicide over the highly doped n regions in Figure 2.1 forms the low resistance source and drain ohmic contacts, as the highly doped n regions have much higher conductivity. These ohmic contacts won't impede with the electric current flow in the transistor from the source to the drain. The drain and source access lengths play an important role in the DC and RF performance of the MESFET, and can be varied to reach a trade-off to fit the desired application. The longer the access lengths, the larger the breakdown voltage ($V_{BD}$) and the parasitic resistance stemming from the long spacer regions. As a result, the transistor current drive and cutoff frequency ($f_T$) degrades. A higher voltage can also be applied to the gate terminal of the device since there is no gate oxide. MESFETs were initially fabricated with GaAs technology [10], but it would not be possible to integrate such transistors with other blocks which mostly are built in CMOS.

Consequently, SOI MESFET transistors are a suitable choice to design high output stages which can be integrated on wafer with CMOS technology.

MESFET breakdown mostly happens due to impact ionization and avalanche breakdown, which is categorized into soft breakdown and hard breakdown. Soft breakdown, unlike hard breakdown, doesn't cause a permanent damage to the transistor and can be reversed by reducing the local electric field, or annealing the device at higher temperatures which repairs the traps close to the metal-semiconductor interface. The transistor performance can be almost fully recovered after a soft breakdown. The reason behind the breakdown mechanism is large local electric fields applied to the transistor. When the supply voltage increases, it creates stronger electric fields and provides more energy to the electrons in the conduction or valence bands. The semiconductor Fermi level, unlike the constant metal Fermi level, changes under the external electric field and reduces the barrier height at the gate. The electron tunneling probability becomes higher as a consequence, and more electrons can tunnel from the gate metal into the transistor channel. This is how more current is generated through impact ionization. If the supply voltage further increases, it will eventually cause an avalanche breakdown which causes much larger current flow during stress.

The zero bias depletion region under the silicide Schottky gate is less than the thickness of the SOI channel. As a result, the MESFETs operate as depletion mode devices with a negative threshold voltage ($V_{th}$).

SOI transistors suffer from body effects such as the kink effect. To solve this issue, a body contact is needed in SOI CMOS technology to eliminate the body effects. Since MESFETs are majority carrier devices, body effects do not appear and no body contact is needed, thereby simplifying the design of the SOI MESFET. MESFETs can be fabricated using partially depleted (PD) and also fully depleted (FD) CMOS technology. We concentrate on partially depleted MESFETs in this research project. The depletion layer width is less than the silicon layer under the gate in PD MESFETs, and the gate voltage adjusts the width of the depletion region and the current flow in the channel.
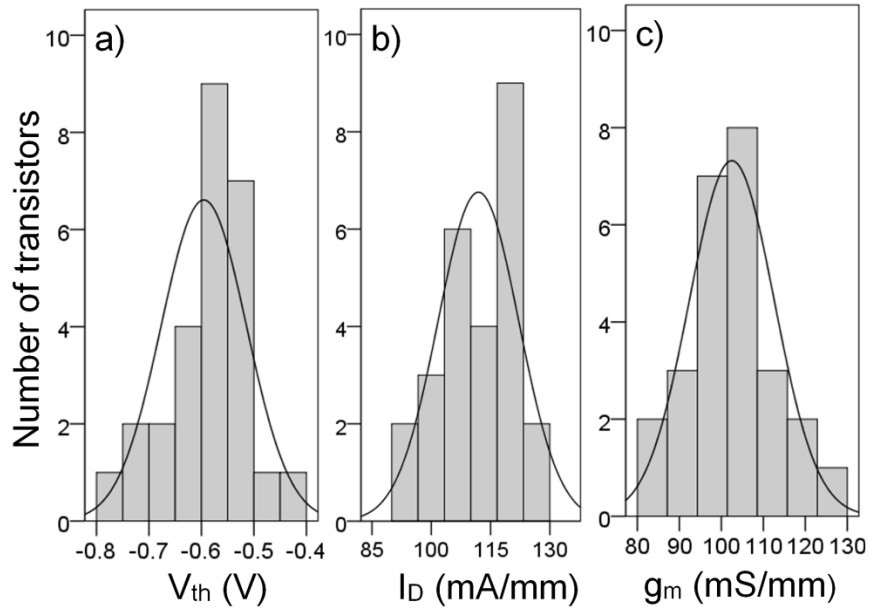


Fig. 2.2. Measured distributions in a) threshold voltage, b) current drive, and c) transconductance from three different multi-project wafer runs. The fitted bell curves are used to extract the mean and standard deviations [11].

The run-to-run variations in the MESFET characteristics depend largely on the thickness of the self-aligned silicide (salicide) layer, and the variations in $L_{aS}$ and $L_{aD}$. These parameters are well-controlled during the 45 nm CMOS fabrication, allowing for good MESFET manufacturability. Process monitor devices with minimum size dimensions of $L_G = L_{aS} = L_{aD} = 200$ nm were fabricated during three separate multi-project wafer runs, each separated by 3-4 months. Figure 2.2 [11] shows preliminary

measurements of the distributions in the threshold voltage, current drive and transconductance for 26 devices.

## 2.2. MESFET Operating Regions

MESFETs are depletion mode devices and they can be turned on and enter the saturation region when $V_{GS}$ has a negative value. Same as with MOSFETs, three regions of operation are defined for MESFET transistors as shown in Figure 2.3.
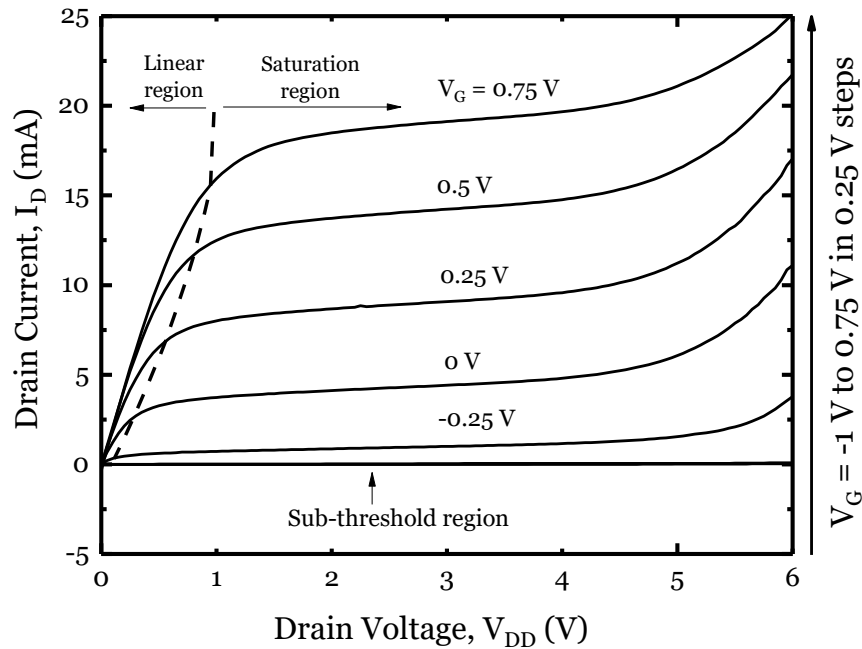
Fig. 2.3. Family of curves (FOC) of a 45 nm SOI MESFET (W=300 μm, $L_G = L_{aD} = L_{aS} = 200$ μm), $V_{BS} = 0$V.

- Sub-threshold region

When the gate voltage is lower than the threshold voltage, there is an exponential relation between the gate voltage and drain current:

$$I_{sub}=I_0 \cdot e^{\frac{V_{GS}-V_t}{N_G \cdot V_t}}\left(1-e^{\frac{-V_{DS}}{V_t}}\right) \tag{2.2}$$

where

$N_G$ = ideality factor of the Schottky gate junction

$I_S$ = saturation current

Based on the above formula, the drain voltage in the sub-threshold region has a low impact on the drain current, especially when $V_{DS}$ is at least three times greater than $V_{th}$. In this region, $I_D$ is the result of carrier diffusion. Since there is a lightly doped channel in the diode, the mobility of the carriers are higher than MOSFET transistors and the cutoff frequency of MESFETs in sub-threshold region is almost five times higher than MOSFETs with the same sizing [12]. MESFETs in the sub-threshold region can be used in micro power applications and the reverse gate leakage current can be used to control the drain current [13]. If a negative gate voltage is applied to the device, the gate leakage current will increase until it dominates the drain diffusion current.

- Linear region

A depletion region is formed under the Schottky barrier when $V_{GS} > V_{th}$ which is wider at the drain end since the drain voltage creates a reverse bias across the channel-gate junction. In this region, when $V_{DS}$ is small, the drain current will increase linearly as the drain voltage is increased and that is the reason why it is called the linear region [14]. The drain current, $I_D$, of the linear region can be calculated using the following formula:

$$I_D=\frac{q\,\mu_n\,N_d\,d_{eff}\,W}{L_G}\left(V_D-\frac{2}{3\sqrt{V_p}}\left(\sqrt{(\varphi_i-V_{GS}+V_{DS})^3}-\sqrt{(\varphi_i-V_{GS})^3}\right)\right) \tag{2.3}$$

Where

$\mu_n$ = channel mobility (cm$^2$/ Vs)

$d_{eff}$ = undepleted channel width (cm)

W = channel width (m)

$L_G$ = channel length (m)

$N_d$ = channel doping density (cm$^{-3}$)

$\varphi_i$ = gate built-in potential (eV)

Linear increase in the drain current with increasing drain voltage continues until the width of the depletion region is equal to the channel thickness [15]. This point is called the pinch-off point and the corresponding drain voltage is called "saturated drain voltage ($V_{Dsat}$). Any increase in the drain voltage beyond this point will not change the width of the depletion region and $I_D$ becomes saturated; Equation 2.3 will no longer be valid.

- Saturation region

Ideally, if $V_D > V_{Dsat}$, the drain current is independent of drain voltage. But since the increase in the drain voltage reduces the effective channel length, $I_D$ slightly increases with $V_D$ after the pinch-off point. Hence, a channel length modulation factor should be added to Equation 2.3:

$$I_D = \frac{q\,\mu_n\,N_d\,d_{eff}\,W}{L_g}\left(V_D - \frac{2}{3\sqrt{V_p}}\left(\sqrt{(\varphi_i - V_{GS} + V_{DS})^3} - \sqrt{(\varphi_i - V_{GS})^3}\right)\right)(1 + \lambda V_{DS}) \qquad (2.4)$$

- High voltage region

If we keep increasing the drain voltage, breakdown happens due to the gate-drain junction tunneling and avalanche mechanisms [6]. The MESFET breakdown voltage is

higher than that of a MOSFETs with the same size since they don't have a thin oxide layer at the gate. In addition, the access region between the gate and source and also drain in MESFETs, increases the breakdown voltage.

Figure 2.4 shows the Gummel plots of the same MESFET transistor used in Figure 2.3. The gate voltage is swept from -1.5 V to 0.75 V for different values of drain voltage (0.025, 0.25, 0.5, 1, 2 and 4 V). As can be seen, the transistor turns on and enters the saturation region for negative gate voltages ($V_{th}$ is negative) since it is a depletion mode device. $V_{th}$ is also slightly changing with drain voltage. The transistor is off when $V_{GS} < V_{th}$ and if the gate voltage is decreased below $V_{th}$, the reverse bias voltage on the Schottky gate will increase which leads to an increasing gate leakage current. As explained, there is a direction change in the gate current and $I_G$ values vary from negative (leakage) to positive (forward bias) and has a zero crossing. Since a logarithmic scale is used on the vertical axis and log (0) is not defined, a low value discontinuity is created.
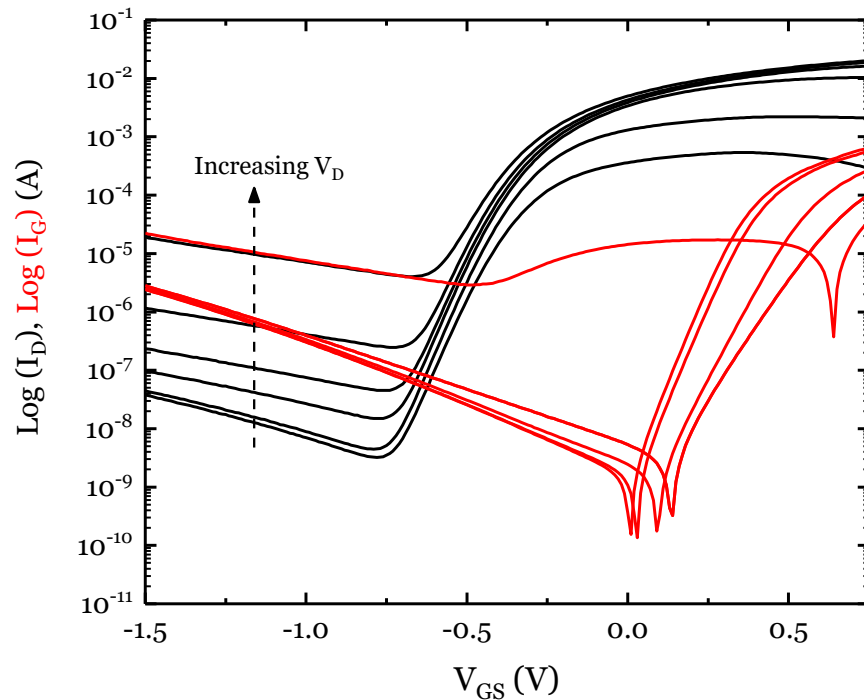


Fig. 2.4. Gummel plots of a 45 nm SOI MESFET (W = 300 μm, $L_G = L_{aD} = L_{aS}$ = 200 μm), $V_{BS} = 0$ V, -1.5 V < $V_{GS}$ < 0.5 V, $V_D$ = 0.025, 0.25, 0.5, 1, 2 and 4 V.

## 2.3.    MESFET DC and RF Characterization

Figures 2.3 and 2.4 illustrated typical family of curves (FOC) and Gummel plots for a 300 μm wide MESFET transistor with $L_G = L_{aD} = L_{aS} = 200$ μm. As explained in 2.1, extending the drain side silicide spacer in order to increase $L_{aD}$ will increase the drain-source junction break-down voltage, as it diminishes the electric field intensity at this critical junction. However, the further parasitic resistance introduced by the larger spacer block reduces the current flowing into the drain terminal, also degrades the RF performance of the device. Figure 2.5 shows the family of curves for two MESFETs with different drain access lengths. The MESFET body terminal is connected to the die substrate, which is referred to as the global ground in Cadence layout. The probe station chuck was grounded for the measurements. Hence, when the die is placed on top of the chuck, its substrate is grounded as well and results in $V_{body} = 0$ V.
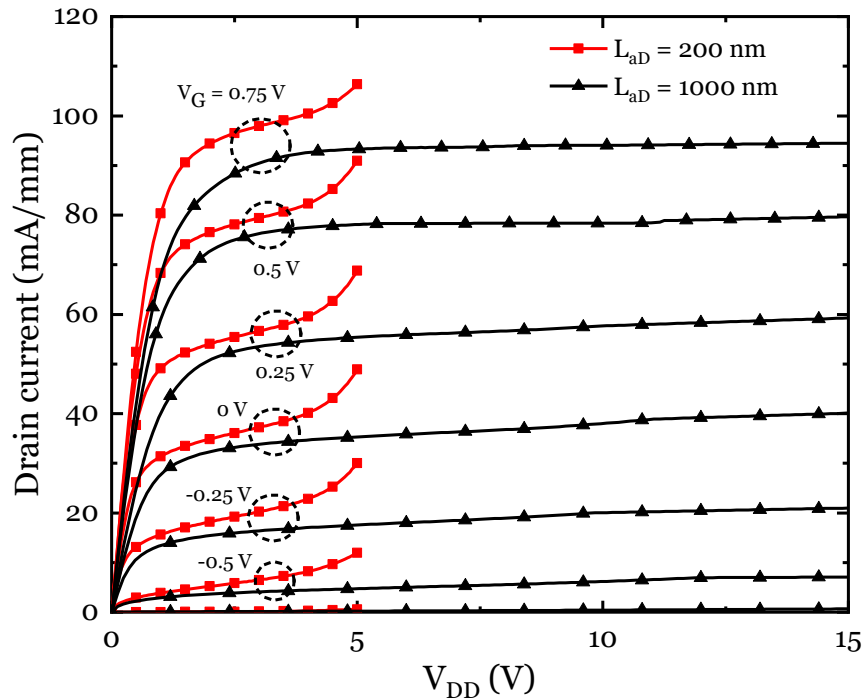


Fig. 2.5. The family of curves for MESFETs with drain access lengths of 200 nm (squares) and 1000 nm (triangles). For both devices $L_G = L_{aS} = 200$ nm.

As expected, the device with $L_{aD}$ = 200 nm has a higher current drive and lower on-resistance, while the device with $L_{aD}$ = 1000 nm has a significantly higher breakdown voltage, along with an increased saturated output resistance. The device with a shorter $L_{aD}$ has a soft breakdown voltage of ~ 4 V, above which the drain current slowly rolls off with increasing $V_{DD}$ due to leakage from the drain-gate junction of the MESFET [6]. Measurements of the turn-on characteristics of each device indicate similar threshold voltages of approximately -0.65 V for both devices.

The high breakdown voltage of the MESFET with $L_{aD}$ = 1000 nm sacrifices the RF performance of the device. To study the RF performance degradation, two of the RF figures of merit are compared for the two MESFET sizes mentioned above:

- Cut-off frequency ($f_T$): the transition frequency at which the transistor's small signal current gain equals to unity:

$$A_i(j\omega) = \frac{I_{out}(j\omega)}{I_{in}(j\omega)} = 1 \qquad (2.5)$$

$$f_T = \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)} \qquad (2.6)$$

$f_T$ is an intrinsic characteristic of the transistor, meaning that the effect of the parasitics stemming from the pads and layout interconnects needs to be removed from the measurements. For $f > f_T$, the transistor will not be able to provide any current gain. Throughout this thesis, $f_T$ was derived from the DUT S-parameter measurements, and calculation of the forward current gain ($h_{21}$) zero crossing. The relation between $h_{21}$ and S-parameters is as below:

$$h_{21} = \frac{-2\,S_{21}}{S_{21}S_{12} + (1 - S_{11})(1 + S_{22})} \tag{2.7}$$

As expected, the forward current gain (h21) is also dependent on the transistor biasing and intrinsic capacitances:

$$h_{21} = \frac{g_m - j\omega C_{gd}}{j\omega\,(C_{gs} + C_{gd})} \tag{2.8}$$

- Maximum oscillation frequency ($f_{max}$): the frequency at which the transistor's maximum power gain reaches 0 dB.

$$f_{max} = \frac{f_T}{2\sqrt{2\pi\,f_T\,R_G\,C_{gd} + \dfrac{R_G + R_S}{r_o}}} \approx \frac{f_T}{\sqrt{8\pi\,R_G\,C_{gd}}} \tag{2.9}$$

For frequencies greater than $f_{max}$, the transistor won't provide any power gain and there is no point in utilizing that. To find $f_{max}$, the maximum available gain (*MAG*, also called $G_{max}$) can be plotted versus frequency and the zero crossing will give the $f_{max}$ value. The *MAG* equation assumes the transistor is conjugate matched to the input and output ports for the maximum power transfer at each frequency. *MAG* is not defined for unstable two port networks. K-Δ test is a prevalent way to verify the stability of the DUT. For a two port to be stable, Δ (determinant of the S-parameters matrix) should be less than one, and the Rollett's stability factor (*K*) should be greater than 1:

K-Δ test for two port stability
$$\begin{cases} \Delta = S_{11}S_{22} - S_{21}S_{12} < 1 & (2.10) \\[2em] K = \dfrac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}|\,|S_{21}|} \geq 1 & (2.11) \end{cases}$$

Keysight ADS software was used to analyze the measured S-parameter data. If the measured S-parameters matrix give $K < 1$, the software automatically sets $K = 1$ to ensure the two port stability requirement is met. This means the MAG and $f_{max}$ values that the software reports are under the assumption that the two port is stabilized, and conjugate matched to the input and output ports which can be considered as the potential capability of the DUT. Last but not least, $MAG$ is calculated through Equation 2.12:

$$MAG = \frac{|S_{21}|}{|S_{12}|} \left(K - \sqrt{K^2 - 1}\right)$$ (2.12)

### 2.3.1. MESFET DC and RF Performance Dependence on $L_{aD}$

To study the effect of longer drain access lengths on the MESFET RF performance, the h21 and MAG plots are compared for 3 different $L_{aD}$ values (200 nm, 500 nm and 1000 nm) in Figures 2.6 and 2.7 respectively. All the MESFETs have an equal width of 300 μm. The MESFETs were designed with a ground-signal-ground (GSG) pad configuration to allow DC and RF probing of individual die to measure the S-parameters using an 8510C vector network analyzer under different bias conditions. The plots show the maximum measured $h_{21}$ and $MAG$, which means $V_{GS}$ was set to 0.1 V which maximizes the MESFET gm. The S-parameter measurements and pad parasitic de-embedding were done in Cascade Microtech Wincal software. Open GSG pads were used to de-embed the measured S-parameters to obtain the intrinsic forward current gain, $h_{21}$, and the maximum available gain (MAG). As expected, the higher voltage devices with $L_{aD}$ of 1000 nm have lower peak cutoff frequency, $f_T$ and lower maximum oscillation frequency, $f_{max}$ than the $L_{aD} = 200$ nm and 500 nm devices. Figure 2.8 summarizes the measurement results and illustrates the possible design choices that are available when considering trade-offs between high voltage and high frequency operation. The MESFET with $L_{aD} = 200$ nm exhibits the maximum measured $f_T$ of 27.7 GHz. As $L_{aD}$ is extended to 500 nm and 1000 nm, $f_T$

experiences a drop to 21.2 GHz and 17.2 GHz respectively. Likewise, the measured $f_{max}$ for $L_{aD}$ = 200 nm, 500 nm and 1000 nm was 30.8 GHz, 26.4 GHz and 23.6 GHz respectively.

The insets in Figures 2.6 and 2.7 emphasize the importance of DC biasing on the RF figures of merit. As the drain current increases with biasing, $f_T$ and $f_{max}$ values also increase, until the drain current starts to saturate and reduces the transistor $g_m$. This phenomenon can also be seen in the FOC in Figure 2.5. For a fixed $V_{DD}$ value, the distance between the current curves ($g_m$) gets reduced as $V_{GS}$ is increased. So there exists a biasing sweet spot which maximizes the $g_m$ and RF figures of merit. To clearly illustrate the MESFET $g_m$ variations with respect to $I_D$, Figure 2.9 is presented which shows the measured results for a MESFET with all the access lengths equal to 200 nm while biased with $V_{DD}$ = 2 V.
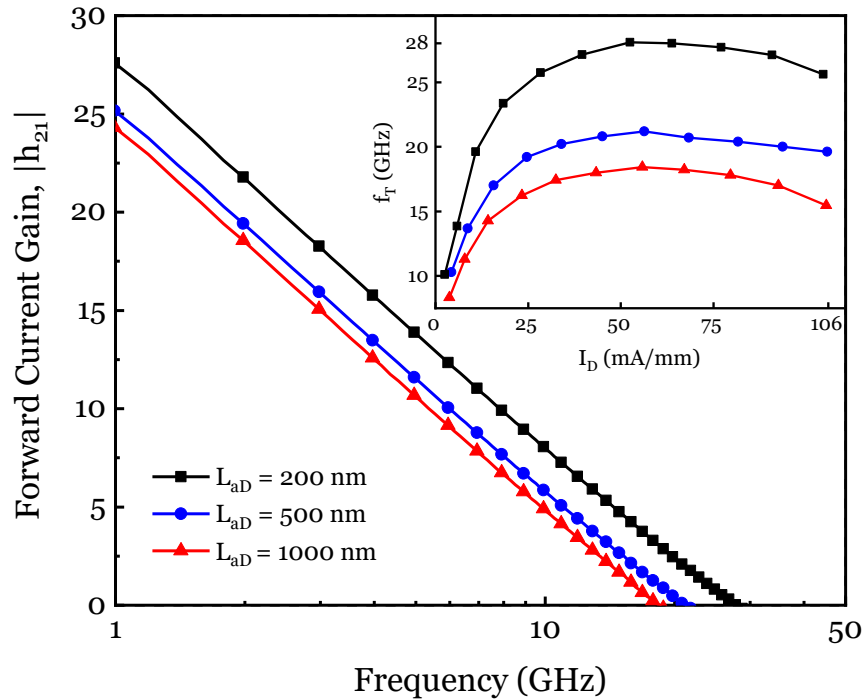


Fig. 2.6. The de-embedded $h_{21}$ as a function of frequency for devices with different drain access lengths of 200 nm, 500 nm and 1000 nm. The devices were biased with $V_{GS}$ = 0.1 V and $V_{DS}$ = 3 V.
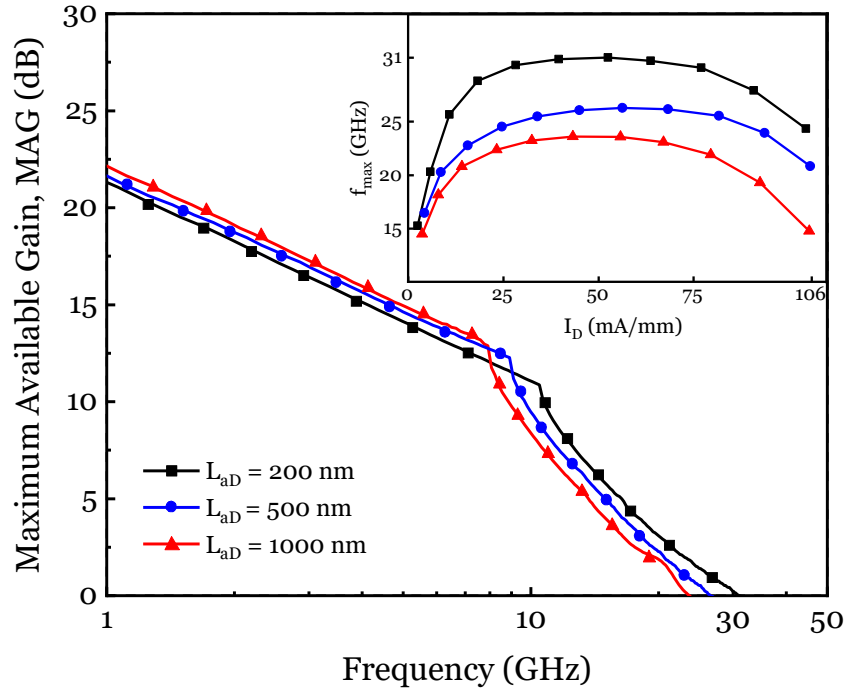
Fig. 2.7. The de-embedded MAG as a function of frequency for devices with different drain access lengths of 200 nm, 500 nm and 1000 nm. The devices were biased with $V_{GS}$ = 0.1 V and $V_{DS}$ = 3 V.
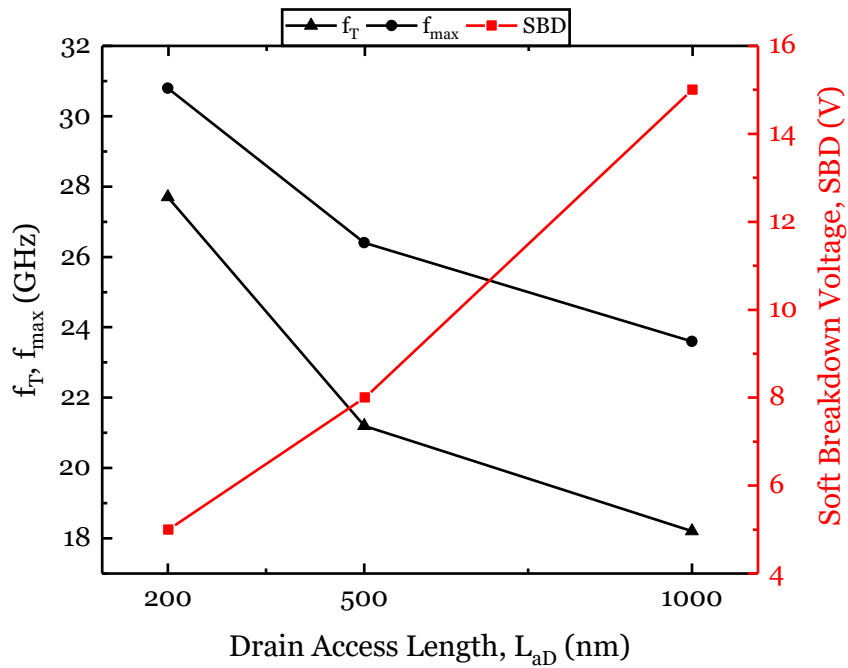


Fig. 2.8. MESFET $f_T$, $f_{max}$ and breakdown voltage variations with respect to $L_{aD}$ ($L_G$ = 200 nm)
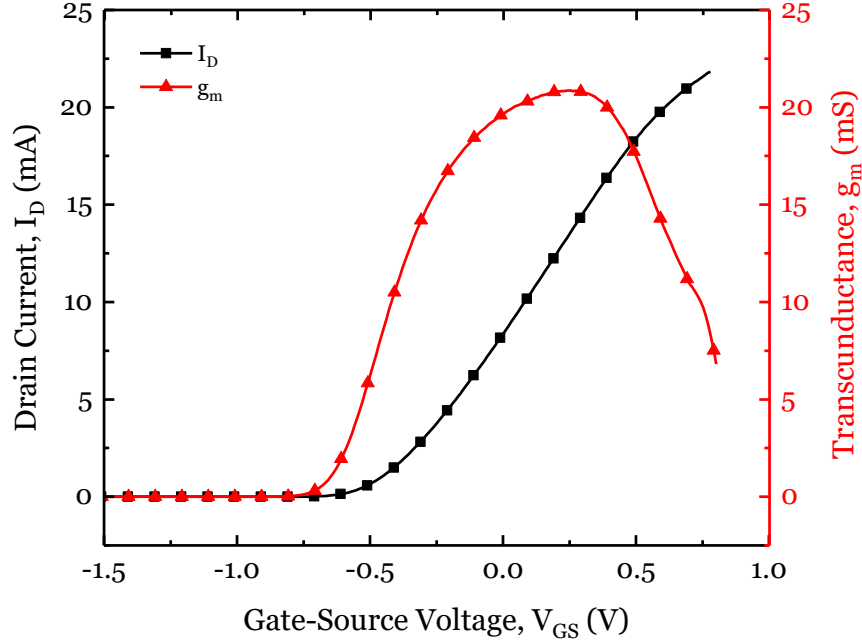
Fig. 2.9. MESFET $g_m$ and $I_D$ variation with respect to $V_{GS}$ ($V_{DD}$ = 2 V, $L_{aD}$ = $L_{aS}$ = $L_G$ = 200 nm).

### 2.3.2.  MESFET DC and RF Performance Dependence on $L_G$

Another takeaway from Equation 2.6 is the inverse relation between $f_T$ and the transistor gate length. So far, the impact of the MESFET drain access length on the RF performance has been studied in this chapter. To increase the operating frequency of the MESFET, it is worth investigating the gate length ($L_G$) reduction as well. To address this question, a MESFET with a 25% shorter gate length, i.e. $L_G$ = 150 nm compared to the 200 nm gate length MESFET was studied. Both transistors were 300 μm wide. Furthermore, to enhance the voltage capability of the 150 nm gate length MESFET alongside its RF performance, the drain and source access lengths were also increased by 50%, i.e. $L_{aD}$ = $L_{aS}$ = 300 nm. The expectation should be increased $V_{BD}$ due to longer silicide spacers, and higher $f_T$ in comparison to the $L_{aD}$ = $L_{aS}$ = $L_G$ = 200 nm MESFET.

As the measured FOC in Figure 2.10 shows, both the current drive ability and transconductance of the MESFET with $L_G$ = 150 nm, $L_{aD}$ = $L_{aS}$ = 300 nm are substantially greater than the $L_G$ = $L_{aD}$ = $L_{aS}$ = 200 nm counterpart due to shorter gate length. Although the source and drain access lengths of the $L_G$ = 150 nm MESFET are longer and introduce higher parasitic resistance values, the effect of the reduced gate length is dominant and the overall DC performance of the MESFET is superior to the $L_G$ = 200 nm MESFET. While the drain current in the $L_G$ = 200 nm MESFET starts to roll off close to $V_{DD}$ = 5 V, the $L_G$ = 150 nm MESFET exhibits a steady performance up until $V_{DD}$ = 8 V thanks to its longer $L_{aD}$ (300 nm, vs. 200 nm for the $L_G$ = 200 nm MESFET). It should be emphasized that both of these devices are fabricated on a 1 V technology node.
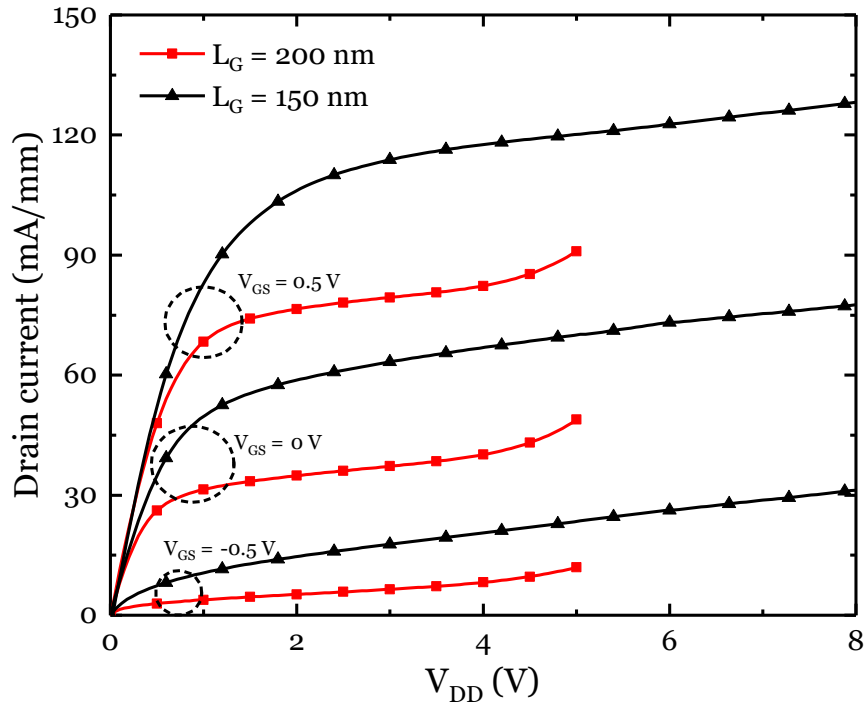


Fig. 2.10. FOC comparison between $L_G$ = $L_{aD}$ = $L_{aS}$ = 200 nm, and $L_G$ = 150 nm, $L_{aD}$ = $L_{aS}$ = 300 nm MESFETs.

Apart from the DC performance, reducing the MESFET gate length by 50% results in a ~ 12.5% increase in the device $f_T$. The forward current gain of the $L_G$ = 200 nm

MESFET in Figure 2.6 is compared to the $L_G$ = 150 nm MESFET, and the results are presented in Figure 2.11. $V_{GS}$ was set to 0.1 V for both devices, but $V_{DS}$ of the $L_G$ = 150 nm MESFET was increased to 5 V due to its higher voltage handling capability, while $V_{DS}$ was kept at 3 V as before for the $L_G$ = 200 nm device. The measured $f_T$ of the $L_G$ = 150 nm MESFET is increased to 31.5 GHz with respect to $f_T$ = 28 GHz for the $L_G$ = 200 nm MESFET, which concludes that the RF performance is also superior.
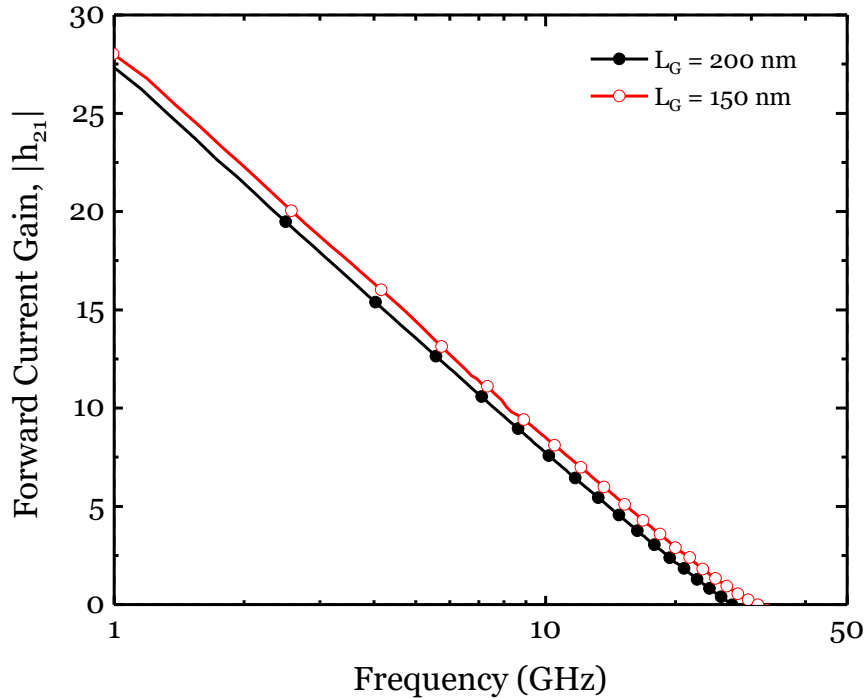


Fig. 2.11. MESFET Cut-off frequency ($f_T$) dependence on the gate length ($L_G$).

Since $f_{max}$ is proportional to $f_T$, a higher $f_{max}$ is expected for the $L_G$ = 150 nm MESFET as well. Under the same biasing conditions as in Figure 2.11, the -20 dB/dec extrapolation line (dashed) in Figure 2.12 suggests a $f_{max}$ ~ 44 GHz for the $L_G$ = 150 nm MESFET, increased from $f_{max}$ ~ 31 GHz for the $L_G$ = 200 nm MESFET. Overall, considering the trade-off between the DC and RF performance of the MESFET, the transistor layout can be engineered to deliver the optimum performance which fits the application requirements the best.
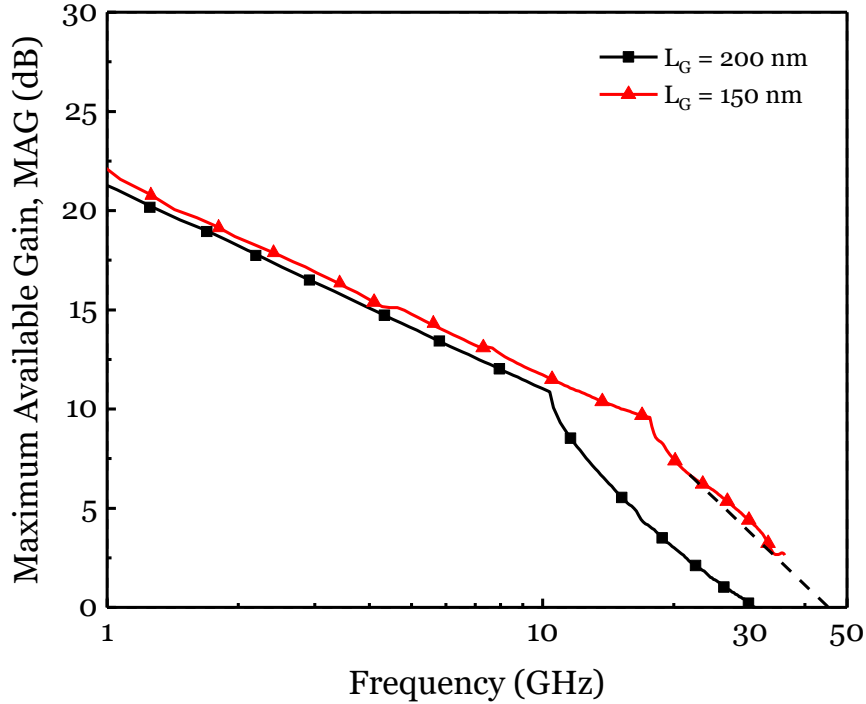
Fig. 2.12. Maximum oscillation frequency ($f_{max}$) dependence on the gate length ($L_G$).

### 2.3.3. MESFET RF Performance Dependence on the Gate Finger Width ($W_f$)

Another parameter which can be taken into consideration while optimizing the MESFET layout design is the number of gate fingers ($N$) and the width of individual gate fingers ($W_f$). To make the layout of a large transistor more compact, get a more reasonable aspect ratio, and reduce the total gate resistance the transistor can be divided into multiple fingers. The total transistor width ($W_T$) will be:

$$W_T = N \times W_f \qquad (2.13)$$

Figure 2.13 illustrates the idea behind the multi-finger transistors. The drain/source area is in common between two adjacent transistors and reduced the total occupied space. The effective width ($W_{eff}$) of the transistor with two fingers is twice as much as the single finger transistor, while the gate length of the two is the same.
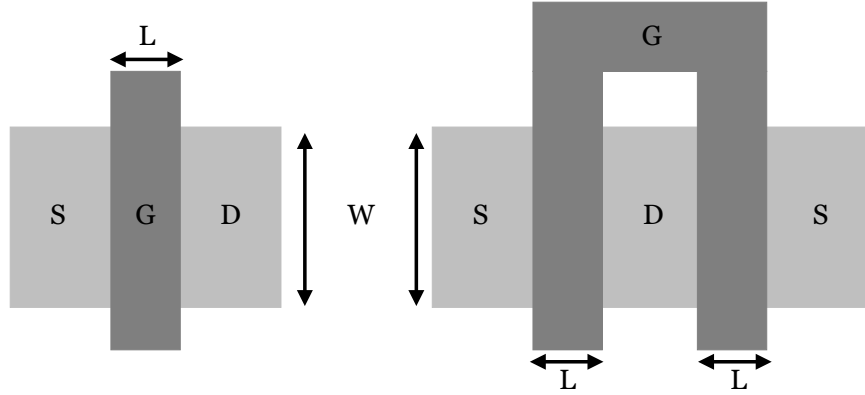
Fig. 2.13. left: single finger transistor, right: transistor with two fingers ($W_{eff}$ = 2W, $L_{eff}$ = L).

The gate finger width ($W_f$) and the total number of gate fingers affect the RF performance of the MESFET. Albeit, no noticeable dependency was detected in the DC measurement results of the MESFETs with different $W_f$. To clearly show the RF performance dependency on $W_f$, the intrinsic $f_T$ and $f_{max}$ of separate MESFETs with equal total width ($W_T$) of 300 μm and different gate finger widths ($W_f$) of 2.4 μm, 4 μm, 8 μm, 12 μm and 15 μm were measured and compared. All the MESFETs had gate and access lengths of $L_G = L_{aD} = L_{aS}$ = 200 nm. The total number of fingers can be calculated from Equation 2.13. The comparison results are presented in Figure 2.14, which are in accordance with the reported trends in literature [16].
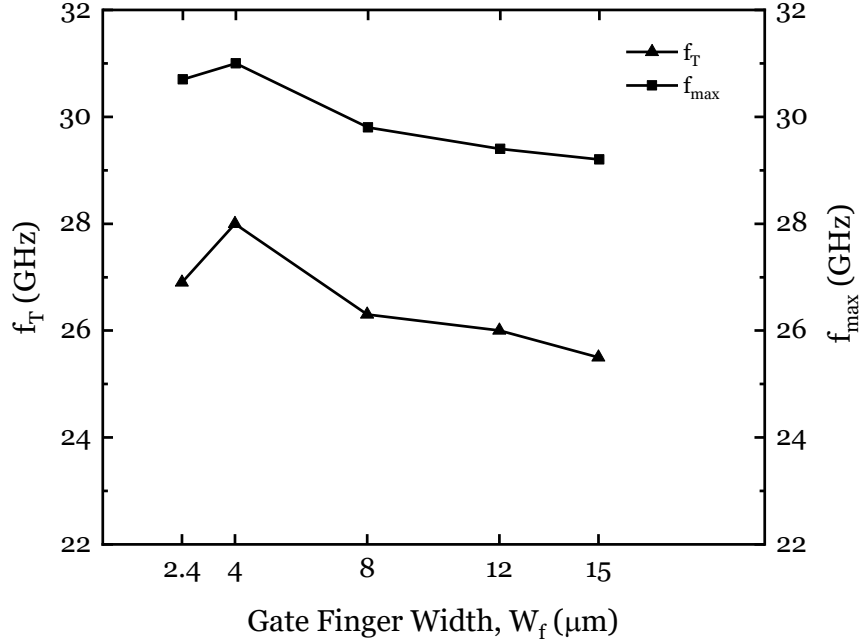
Fig. 2.14. $f_T$ and $f_{max}$ variations with respect to the gate finger width ($W_f$).

Parasitic capacitances increase as the finger width gets larger and as Equation 2.6 suggests, $f_T$ drops with increasing parasitic capacitances. Another parameter which attributes to the $f_T$ dependency on $W_f$ is the transistor distributed gate resistance ($R_G$). The cutoff frequency equation does not contain $R_G$, as $f_T$ excludes the transistor junction parasitics such as $R_G$, sidewall junction capacitances, etc. by definition [17]. Consequently, to calculate the cutoff frequency, the transistor is considered as an ideal current source. The distributed gate resistance however, forms an RC filter with the transistor capacitances which can eventually restrict the switching speed. $R_G$ can be calculated through Equation 2.14:

$$R_G = \frac{R_{sh}\, W_f}{3\, n^2\, L_G}$$

(2.14)

where

$R_{sh}$ = sheet resistance of silicide

$W_f$ = gate finger width

n = number of gate contacts

As the above equation suggests, larger $W_f$ leads to higher gate resistance which reduces $f_T$. An inconsistency is witnessed between 2.4 µm and 4 um finger widths, which is believed to ensue from the total number of gate fingers. To construct a 300 µm wide MESFET, 67% more gate fingers are required when using 2.4 µm wide fingers instead of 4 µm (125 versus 75). The extravagantly increased number of fingers contribute to the total parasitic capacitances and become the dominant parameter which degrades $f_T$. The conclusion which can be drawn is there should be a lower limit in reducing $W_f$.

$f_{max}$ is proportional to $f_T$ based on Equation 2.9, so the same trend is expected for $f_{max}$ variations with respect to $W_f$.

## 2.4.    4-Terminal MESFET DC Measurements

In many applications such as cascode amplifiers, there is a voltage difference between the source and body (bulk) terminals. Non-zero $V_{SB}$ changes the depletion layer width and affects the threshold voltage. The body terminal can be considered as a back gate and its effect should be taken into account for device modeling and circuit design.
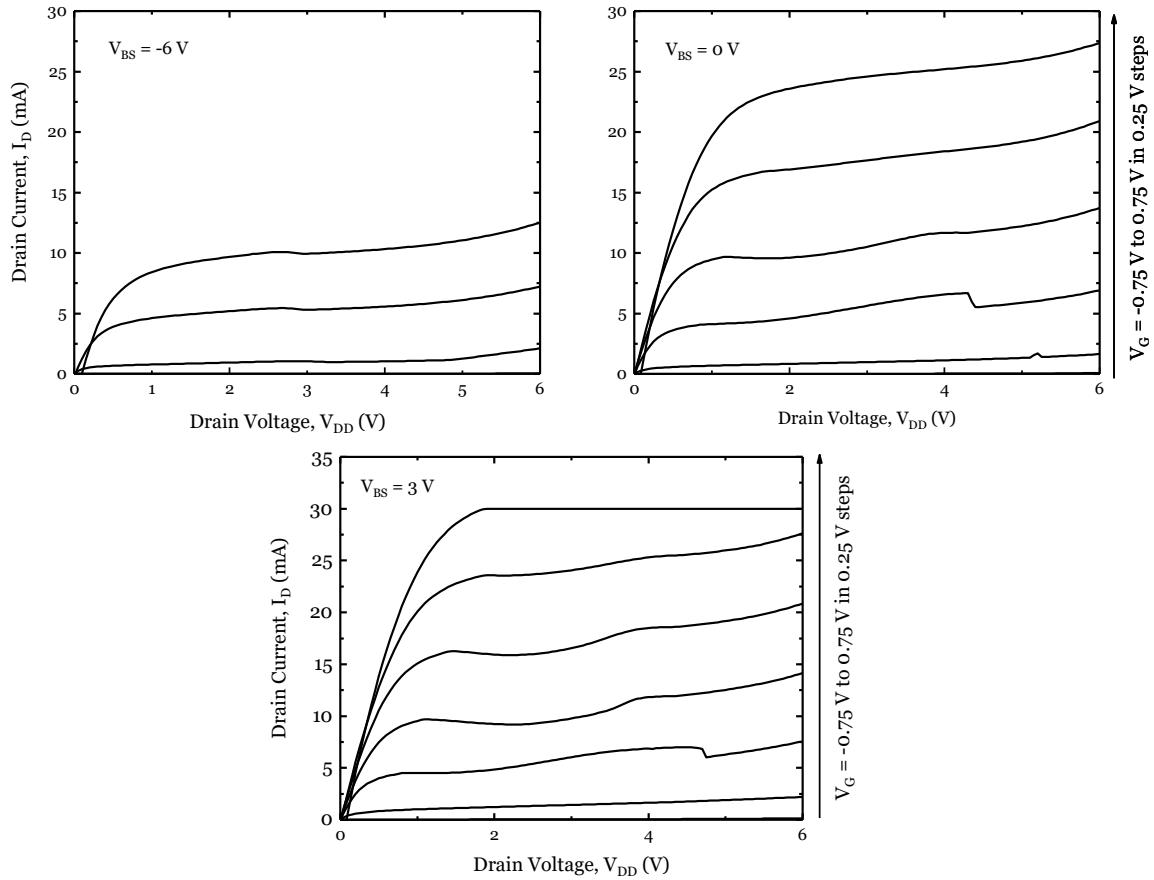


Fig. 2.15. Drain current versus drain voltage of a SOI MESFET ($W$=300 μm, $L_G$ = 200 μm) for different substrate voltages. $I_D$ increases as $V_{BS}$ is raised.

Figure 2.16 shows the effect of the substrate bias on the drain current and threshold voltage. If a negative voltage is applied to the bulk terminal ($V_{BS} < 0$), it creates an opposing electric field which hardens the transistor turn-on, or tapers the depletion layer width and reduces the current flowing through drain. If the bulk-source terminal is forward biased

($V_{BS} > 0$), it makes channel formation easier or it widens the depletion region and we expect an increase in $I_D$ and lower threshold voltage.
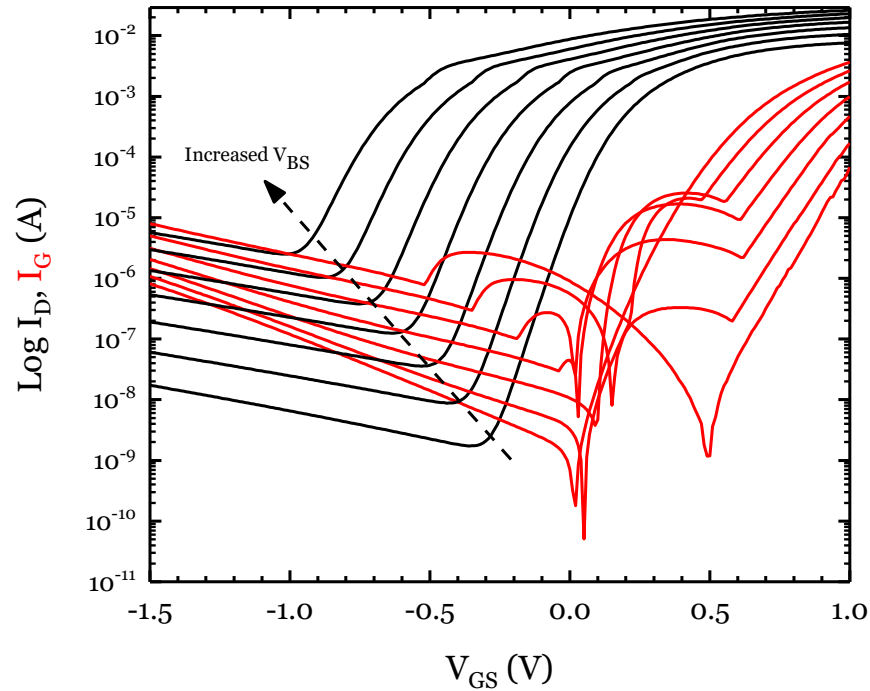


Fig. 2.16. Drain and gate currents of a SOI MESFET ($W$ = 300 µm, $L_G$ = 200 µm) as a function of gate voltage, while $V_{DD}$ is kept constant at 2 V. $V_{BS}$ is swept from -6 V to 3 V in 1.5 V steps in the direction of the arrow.

## 2.5.    MESFET Models

Simulations are an essential part of the design process, tape-out and fabrication will be based on the simulation results. In order to get accurate simulation results, a precise device model is needed to predict the behavior of the device under different operating conditions. Device models need to be run on different popular CAD platforms such as Cadence or Agilent ADS to be convenient and useful. Device models can be categorized into 2 different categories:

- Physical Models

These models are derived based on the physical parameters such as material properties, device physics, geometry, etc. and different variables are used to model each parameter [15]. Many of these parameters are nonlinear and they change with frequency. In addition, many approximations and hypotheses are being made to analyze the behavior of the device. For this reason, physical models are not the best choices for circuits design and simulation. But physical models provide detailed information about the device operation, and the device can be optimized itself using the physical parameters. Process variations can also be predicted by changing the physical parameters of the device. The latter can cause difficulties for the circuit designers as well since one may not be familiar with physical parameters and how to adjust them for the optimized device behavior.

- Table based models

These types of models are developed based on hands-on measurements of different parameters such as terminal currents, charges or other characteristics. Typically one thousand measurement points are needed for an accurate model which can be time consuming. The measured data are stored in lookup tables and the device behavior is predicted by interpolating the lookup table data during simulations. The simulation results, however, cannot be trusted out of the measurements range or conditions.

- Empirical Models

Empirical models fit mathematical functions to DC and AC measurement results. In order to extend the model out of the measurement range, an equivalent circuit can be introduced and its parameters can be replaced in the fitting functions to extrapolate the results. Such extrapolation is an ultimate goal for most of the models which may not be fully realized. Measurement errors can disrupt the final precision of the model and multiple measurements need to be done as sanity checks to assure the model's fidelity. If

the device characteristics (e.g. materials, geometry, etc.) change, new sets of measurements and new device characterization should be done.

Empirical models are usually favored over the other two as they offer higher computational efficiency and don't require complicated physical parameters. There are different models available for MESFET transistors including Triquint models (e.g. TOM3), Curtice, Statz and Angelov (Chalmers). A short description of these models are provided here:

### 2.5.1. Curtice Quadratic Model

The Curtice model is one of the first MESFET models which is not complicated and includes important transistor parameters such as pinch-off voltage and transconductance. It suggests a Taylor series expansion around the threshold voltage to calculate the drain current [18]:

$$I_{DS} = \beta(V_{GS} - V_{T0})^2 \tanh(\alpha V_{DS})(1 + \lambda V_{DS}) \tag{2.15}$$

Where

$\beta$ = Transconductance parameter (mA/V$^2$)

$V_{T0}$ = Pinch-off voltage (V)

$\alpha$ = Slope of $I_{DS}$ VS. $V_{DS}$ in the linear region (V$^{-1}$)

$\lambda$ = Slope of $I_{DS}$ VS. $V_{DS}$ in the saturation region (V$^{-1}$)

The *tanh* function is used to describe the current in the linear region. The Curtice model is valid above the threshold voltage and not accurate when the transistor is reversed biased or when $V_{DS} = 0$.

### 2.5.2.  Statz Model

In the Statz model —which is a modification of the Curtice model— the *tanh* function is replaced with a third order polynomial [10], and the square law is only valid for small gate over drive voltages ($V_{GS} - V_{To}$). $I_{DS}$ becomes linear for higher gate over drive voltages.

$$I_{DS} = \frac{\beta(V_{GS}-V_{To})^2(1+\lambda V_{DS})\left(1-\left(1-\frac{\alpha V_{DS}}{3}\right)^3\right)}{1+b(V_{GS}-V_{To})} \tag{2.16}$$

Where $\left(1-\left(1-\frac{\alpha V_{DS}}{3}\right)^3\right)$ is the truncated series representation of the $\tanh(\alpha V_{DS})$ function. The Statz approach fails to model the drain conductance for higher values of $V_D$.

### 2.5.3.  Triquint Own Model (TOM3)

There is not a square law relation between the gate over drive voltage and $I_{DS}$ for all devices. The TOM3 model changes the constant exponent in this expression from 2 to a variable number and represents a continuous expression for $I_{DS}$ in all operation regions [19]. Previously, our group developed a 3-terminal TOM3 MESFET model in simulations. As explained before, in some circuit architectures such as cascode amplifiers, there is a voltage difference between the body and source terminals and the body effect needs to be taken into account since it modifies the drain current. That is why a 4-terminal Angelov model was developed to generate more accurate simulation results.

### 2.5.4. Angelov (Chalmers) Model

Currently, the Angelov model is the most popular MESFET model in the industry, especially for GaN technology. This is the reason why we chose the Angelov model to model the CMOS compatible MESFETs. Some parameters of the fitting mathematical equations need to be changed as the size and geometry of the device change. Therefore, the model is developed in Verilog-A which enables us to easily make the needed changes to tune the model. The Angelov model directly uses hands-on measurement results to estimate different parameters [20], [21]. All model parameters have continuous derivatives without poles. The Angelov's equivalent circuit diagram is shown in Figure 2.17.
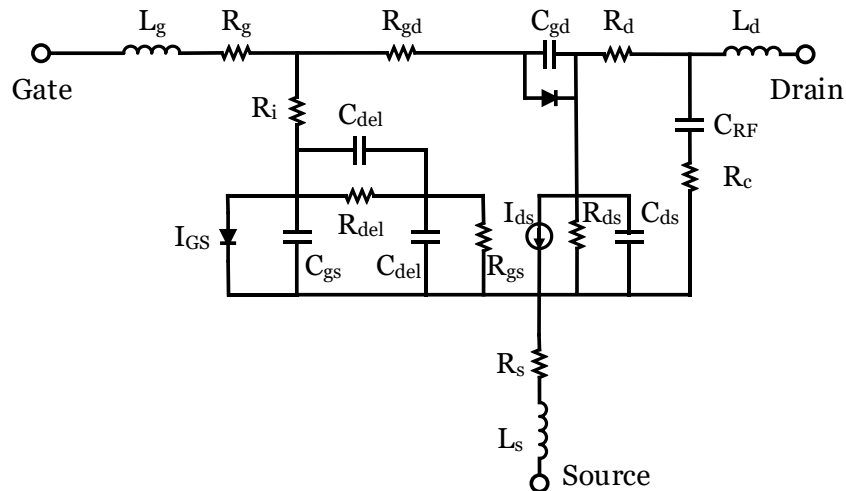


Fig. 2.17. Angelov circuit diagram [23] including a current source, parasitic capacitances and resistances. Since the gate forms a Schottky contact, two diodes between the gate and source/drain terminals are used to model the leakage current.

There are several DC and AC fitting parameters used in the Angelov model, which call for extensive measurements of both types. The DC measurements are usually done first and $I_{DS}$ of the MESFET is recorded versus $V_{DS}$ (family of curves) and $V_{GS}$ (Gummel plots) in order to extract the related DC parameters. Followed by the DC measurements are S-parameter measurements at different bias points to find the nonlinear and parasitic

elements of the model. To evaluate the DC and small signal performance of the Angelov model, I-V curves and S-parameters can be compared to their respective measured values. The large signal performance of the model is usually compared to the load-pull results at a specific frequency.

The basic Angelov model proposes an equation for $I_{DS}$ which has a bell-shaped derivative, same as the measured transconductance. The first order Angelov model consists of five parameters including $I_{pks}$, $V_{pks}$, $P_{1m}$, $\alpha_s$ and $\lambda$ which can be extracted using direct measurements. The essential measurement biasing points to extract the model parameters are low and high current quiescent points with low and high $V_{ds}$. Thus, FOC measurements can be a good start for the model extraction as $V_{DS}$ and $V_{GS}$ both get swept and various current levels are generated. Channel length modulation ($\lambda$) and two saturation parameters ($\alpha_r$, $\alpha_s$) can be found from the FOC plot as shown in Figure 2.18. The parameter $\alpha_s$ defines the slope of $I_{DS}$ versus $V_{DS}$ at high saturated currents with small drain voltages where $V_{DS} < V_{knee}$. $\lambda$ defines the slope of a low drain current curve for higher drain voltages, where $V_{DS} > V_{knee}$.
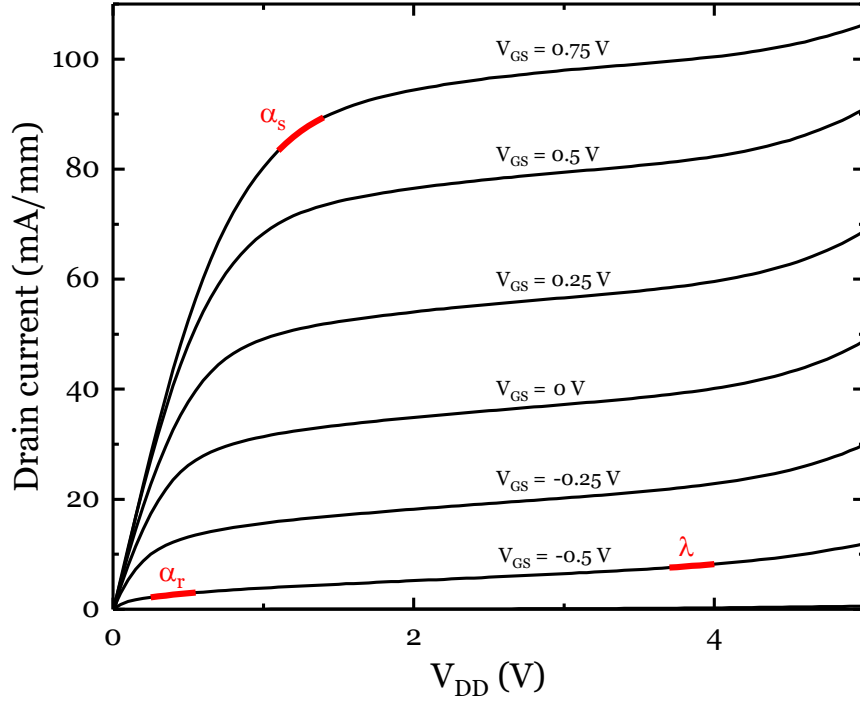
Fig. 2.18. Angelov slope parameters extraction from a 300 μm wide MESFET FOC with $L_G = L_{aD} = L_{aS} = 200$ nm.

The remaining parameters can be calculated by plotting the transistor transconductance at one low and one high $V_{DS}$ value as shown in Figure 2.19. In this figure, the measured $I_{DS}$ and $g_m$ results versus $V_{GS}$ for a 300 μm wide MESFET fabricated on 180 nm Jazz Semiconductor technology. The current and transconductance should be measured for high and low $V_{DS}$ values, which were selected as $V_{DS} = 2$ V, 0.1 V in Figure 2.19. $\Psi_p$ is a power series function centered at $V_{pk}$ and varies with $V_{gs}$. For the first order model, $\Psi_p$ is a simple first order polynomial.
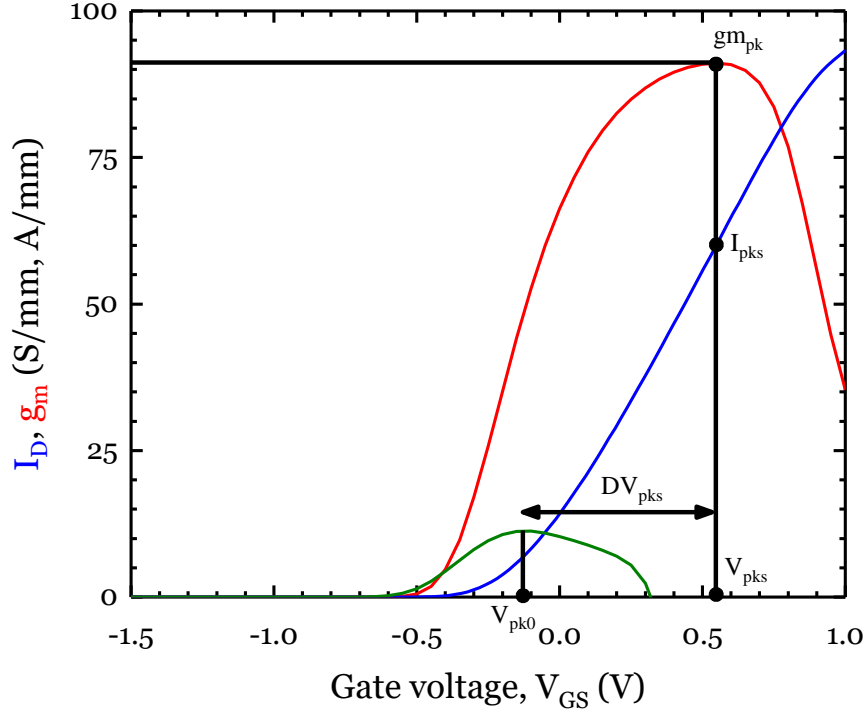
Fig. 2.19. Parameter extraction for the first order Angelov model using measurement results of a MESFET with $L_G = 500$ μm, $W = 300$ μm which was fabricated on the 180 nm Jazz Semiconductor technology.

$$I_{DS} = I_{pks} \left(1+\tanh\left(\Psi_p\right)\right) \tanh\left(\alpha_s V_{DS}\right)(1+\lambda V_{DS}) \qquad (2.17)$$

$$\Psi_p = P_{1m} \left(V_{GS} - V_{pks}\right) \qquad (2.18)$$

$$P_{1m} = \frac{g_{m\text{-}pk}}{I_{pks}} \qquad (2.19)$$

Where

$I_{pks}$ = drain current at which the transconductance is maximized

$P_{1m}$ = polynomial coefficient for channel current

$\alpha_s$ = saturation voltage parameter

$\lambda$ = channel length modulation

$V_{pks}$ = gate voltage at which the transconductance is maximized

$g_{m\text{-}pk}$ = maximum transconductance

$D_{vpks}$ = change in $V_{pk}$ versus $V_{ds}$

The first-order Angelov model typically generates results with less than 10% global error [18] which can predict the I-V curves and transconductance trends. The first order model can be can be extended to get more accurate results. In the next step, 6 more model parameters can be added to the first order model to construct an 11 parameter model. The equations will be updated as follows [18]:

$$D_{vpks} = V_{pks} - V_{pks0} \tag{2.20}$$

$$\Psi_p = P_{1m}\left(\left(V_{GS} - V_{pk0}\right) + P_2\left(V_{GS} - V_{pks}\right)^2 + P_3\left(V_{GS} - V_{pkm}\right)^3\right) \tag{2.21}$$

$$V_{pk}\left(V_{DS}\right) = V_{pks} - DV_{pks} + DV_{pks}\tanh(\alpha_s V_{DS}) \tag{2.22}$$

$$P_{1m} = \frac{g_{m\text{-}pk}}{I_{pks}}\left[\left(1+\Delta P_1\right)\left(1+\tanh(\Psi_p)\right)\right] \tag{2.23}$$

$$\alpha = \alpha_r + \alpha_s\left(1+\tanh(\Psi_p)\right) \tag{2.24}$$

$\Psi_p$ power series which was chosen to be a first order polynomial in the first order model, can be extended to higher order polynomials for more accuracy. $\Delta P_1$ accounts for the $P_{1m}$ reduction at high $V_{DS}$ values by modifying the gain of the transistor. As a result of the higher gain, the voltage swing on the gate will be less, which degrades linearity and intermodulation characteristics. $P_2$ and $P_3$ introduce higher order polynomial coefficients for channel current to adjust different $g_m$ shapes. $B_1$ and $B_2$ are the unsaturated coefficients for $P_1$ and $P_2$ and track $\Delta P_1$ changes with respect to $V_{ds}$. $D_{vpks}$ models the effect of the drain voltage changes on $V_{pks}$, which is partially due to the voltage drop on the source resistance.

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The parameter α$_r$ controls the slope of low $I_{DS,}$ for lower values of $V_{DS}$ and $V_{GS}$. $α_s$ sets the slope of saturated $I_{DS}$ for low values of $V_{DS}$ and higher $V_{GS}$ values. 7 important parameters including $I_{pks}$, $V_{pks}$, $P_{1m}$, $α_s$, $α_r$, $λ$ and $D_{vpks}$ can be directly found from the measurements, and a CAD tool such as Cadence can be used for fine tuning and optimization.

The next step is fitting the simulated S-parameters to their respective measured values at RF frequencies. Since S-parameters can be converted to $h_{21}$, forward current gain and its corresponding cutoff frequency can also be considered as the comparison basis. To complete the small signal model and get accurate simulation results at higher frequencies, layout parasitic components such as $R_g$, $R_d$, $R_s$, $R_i$, $C_{ds}$, $L_g$, $L_d$ and $L_s$ should be extracted from S-parameter measurements at different biasing points. Initial estimate for these parameters can be found through ColdFET measurements which are described in details in Chapters 3 and 4. Examples of extracted model parameters and intrinsic/parasitic components through DC and ColdFET measurements for individual CMOS compatible MESFETs can be found in [22], [23].

Finally, the following are some other fitting parameters which are very useful in controlling the high frequency performance of the Angelov model. Frequency dependent anomalies caused by deep level traps at surface or channel-substrate interface prompt frequency dispersion of $g_m$, I-V characteristics and output conductance [21], [24]. The S-parameters and RF figures of merit are also affected consequently. To model dispersion, $R_C$ in series with $C_{rf}$ is added to the small signal equivalent circuit (Figure 2.17) between drain and source terminals, which controls the frequency dependent output transconductance. At frequencies higher than the MESFET cutoff frequency, $R_C$ shunts the output and decreases the transconductance. $C_{RF}$ determines the time constant of this RC network. In the Angelov Verilog-A model, a similar RC network is added to the transistor input port, between gate and source terminals, due to the symmetry of the

transistor. To account for the input dispersion, $R_{cin}$ and $C_{rfin}$ in the Angelov Verilog-A model control the frequency dependent input conductance. If the desired RF simulation accuracy is not attained via the aforementioned 4 dispersion variables, 3 more parameters including $R_{del}$, $C_{del}$ and $K_{bgate}$ are available in the Angelov model which provide more control knobs. $R_{del}$ and $C_{del}$ shunt the gate control node to change the frequency dependent gate control and delay. As the frequency is increased, the gate control is delayed further which is why RF devices don't respond instantly to excitation. The delay RC network ($R_{del}$, $C_{del}$) generates high frequency delay by changing the input conductance. $K_{bgate}$ enables the back gate parasitic feedback to the gate control voltage in the Angelov Verilog-A model which changes the effective $V_{GS}$.

To acquire an accurate RF fit to the S-parameters, the frequency dispersion parameters along with the parasitic and intrinsic component values can be modified around the initial estimations in the Angelov Verilog-A model. A close simulation result can be achieved by iteration.

### 2.6.    4-Terminal Angelov Modeling

The 4-terminal Angelov model was presented by our group for the first time [23] to incorporate the substrate bias effects into the initial Angelov model. To start, an initial drain current model was presented at $V_{bs}$ = 0 V for a 45 nm SOI MESFET with $L_G = L_{aS} = L_{aD}$ = 200 nm and W = 300 μm. A device with average behavior was chosen to develop the model. Different DC measurements were done to produce enough data points and extract five basic Angelov model parameters as explained in Section 2.5.4 (Equations 2.17 through 2.19). Parameter extraction results at $V_{BS}$ = 0 were as follows:

Table 2.1. Extracted DC Parameters from a CMOS MESFET for the First Order Angelov Model

| $g_{mpks}$ (mS/mm) | $I_{pks}$ (mA/mm) | $V_{pks}$ (V) | $\alpha_s$ ($V^{-1}$) | $\alpha_r$ ($V^{-1}$) | $\lambda$ |
|---|---|---|---|---|---|
| 91.7 | 66.3 | 0.59 | 0.005 | 1.8 | 0.045 |

The major change in the 4-terminal Angelov model is added gate current equations to account for the forward and reverse gate leakage diodes. The Schottky gate contact in the MESFET forms two current paths to the source and drain regions as shown in Figure 2.20[23].
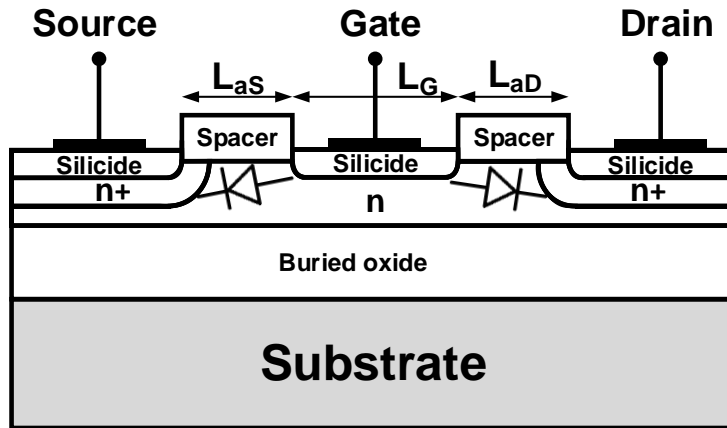


Fig. 2.20. Current paths between the Schottky gate and source/drain junctions in a CMOS MESFET transistor.

The gate to source leakage current equation in the initial Angelov model [18] is:

$$I_{gs}=I_j \left( \exp \left( P_g . \tanh(V_{gsi} - V_{jg})\right) - \exp(-P_g . V_{jg})\right)$$ (2.25)

Where

$I_j$ = gate forward saturation current

$P_g = \dfrac{kT}{N_e \cdot q}$ (gate current parameter)

$V_{gsi}$ = internal gate node voltage

$V_{jg}$ = fitting offset in the gate current parameter

$P_g$ needs to be divided into two parts, forward ($P_{gF}$) and reverse ($P_{gR}$) to incorporate the forward and reverse gate leakage currents. Adding $P_{gF}$ and $P_{gR}$ to Equation 2.25 will change it to:

$$I_{gs} = I_j \left( \exp \left( P_{gF} \cdot \tanh \left( V_{gsi} - V_{jg} \right) \right) - \exp \left( -P_{gR} \cdot V_{jg} \right) \right) \qquad (2.26)$$

The same argument applies to the gate-drain leakage current equation and two new $P_g$ parameters can be introduced to model the gate-drain forward and reverse leakage currents. The basic $I_{gd}$ equation presented in [18] suggests one leakage current path for the gate-drain junction:

$$I_{gd} = I_j \left( \exp \left( P_g \cdot \tanh(V_{gdi} - V_{jg}) \right) - \exp(-P_g \cdot V_{jg}) \right) \qquad (2.27)$$

Which will be updated to Equation 2.28 by separating the forward and reverse leakage paths:

$$I_{gd} = I_j \left( \exp \left( P_{gF}' \cdot \tanh \left( V_{gdi} - V_{jg} \right) \right) - \exp \left( -P_{gR}' \cdot V_{jg} \right) \right) \qquad (2.28)$$

Substrate bias acts as a second gate and changes the width of the depletion region under the Schottky gate and needs to be modeled to provide a 4-terminal Angelov model. The substrate bias effect increases as the buried oxide becomes narrower. In order to model substrate bias effects, several measurements were done and the proposed gate and drain leakage current parameters as well as Angelov model parameters were extracted and

added to the model. Figure 2.21 illustrates the comparison between the measured and simulated transconductance and drain current for 3 different $V_{bs}$ values.
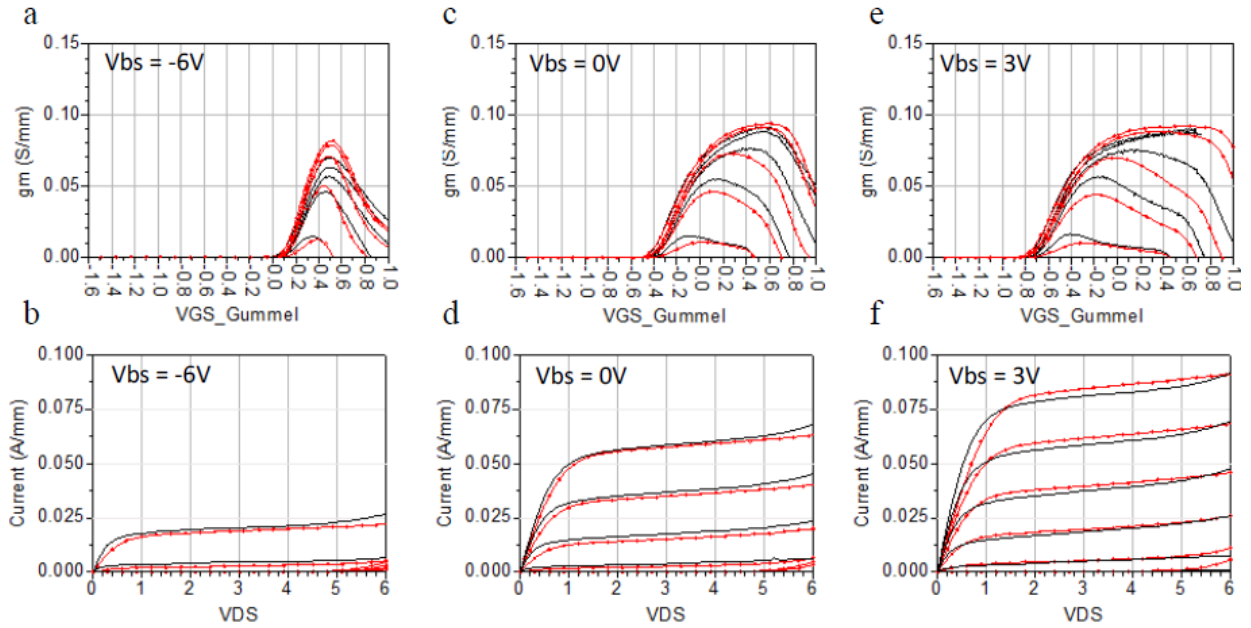


Fig. 2.21. DC model fit for gm and FOC for different substrate bias voltages. $V_{GS}$ in FOC plots was swept from -0.75 V to 0.5 V in 0.25 V steps, and $V_D$ in gm plots are 0.1, 0.5, 1, 2 and 4 V [23].

The 4-terminal Angelov model was optimized for RF applications and the parasitic capacitances such as $C_{gs}$ and $C_{gd}$ to fit the measured S-parameters of the MESFET within the frequency range of 100 MHz to 20 GHz. These results were published in [23]. As a result of accurate parasitic capacitance and S-parameter fitting, simulated $h_{21}$ and power gain also fit to the measured results. To validate the large signal RF behavior of the Verilog-A model, a load-pull analysis was done at 2.5 GHz with a scaled device (W = 5.04 mm).

## 2.7.    Summary and Discussion

This chapter introduced SOI CMOS compatible MESFETs, their superior voltage handling capabilities, and explained the fabrication steps in conventional CMOS technologies. The DC and RF performances were characterized and the key transistor design parameters and their influence on the device behavior was analyzed. CMOS integration makes the MESFETs with a high breakdown voltage a viable alternative to CMOS power generating blocks, suggest and effective solution to realizing a single chip transceiver, and reduce the total fabrication cost of the design. The first 4-terminal Angelov model with substrate bias inclusion and updated gate current equations was presented to simulate the silicon MESFET performance in CAD software. This model showed improved simulation results of gm and gate leakage compared to earlier works. The CMOS MESFET PAs have a compact layout with the potential for highly integrated RFIC applications.

CHAPTER 3

TRAP-RICH SUBSTRATES FOR RF PERFORMANCE IMPROVEMENT

In this chapter, the DC and RF characteristics of metal-semiconductor field-effect-transistors (MESFETs) on conventional CMOS silicon-on-insulator (SOI) substrates are compared to nominally identical devices on high-resistivity, trap-rich SOI substrates [22]. While the DC transfer characteristics are statistically identical on either substrate, the maximum available gain at GHz frequencies is enhanced by ~ 2 dB when using the trap-rich substrates, with maximum operating frequencies, $f_{max}$, that are approximately 5-10% higher. The increased $f_{max}$ is explained by the reduced substrate conduction at GHz frequencies using a lumped-element, small-signal model.

3.1.    High-Resistivity Silicon Substrates

High resistivity silicon substrates are important for CMOS radio frequency integrated circuits (RFICs) to minimize RF power loss in active and passive devices [25], [26] and reduce crosstalk between components [27]. Early work on high resistivity, float zone silicon-on-insulator (SOI) substrates with resistivity up to 10 kΩ.cm confirmed reduced conduction loss in co-planar waveguides (CPW), and higher quality factor inductors [26] compared to similar components on conventional low resistivity (e.g. ~ 20 Ω.cm) substrates. However, the low conduction loss measured in CPW fabricated directly on high resistivity substrates [28], increases when the CPW is fabricated on an oxide layer above the substrate [29], [30]. The increase in the conduction loss is attributed to a parasitic electron accumulation layer at the Si:SiO$_2$ interface due to the positive fixed oxide charge (Fig. 3.1), which creates a parasitic surface conduction (PSC) region. The accumulation layer reduces the effective resistivity of the substrate by allowing a parasitic conduction path at GHz frequencies that increases parasitic coupling and crosstalk,

substrate RF loss and harmonic distortion. Various methods have been demonstrated to mitigate the effects of the parasitic conduction layer and recover a high resistivity substrate. One of the most effective solutions has been introducing trap-rich layers between the silicon substrate and the buried oxide [30]–[33]. The silicon dangling bonds in the trap-rich layer absorb the free electrons that form the PSC region to neutralize the fixed oxide charge. As a result the conductivity of the parasitic channel at the $Si:SiO_2$ interface is greatly reduced and retains a high nominal substrate resistivity.
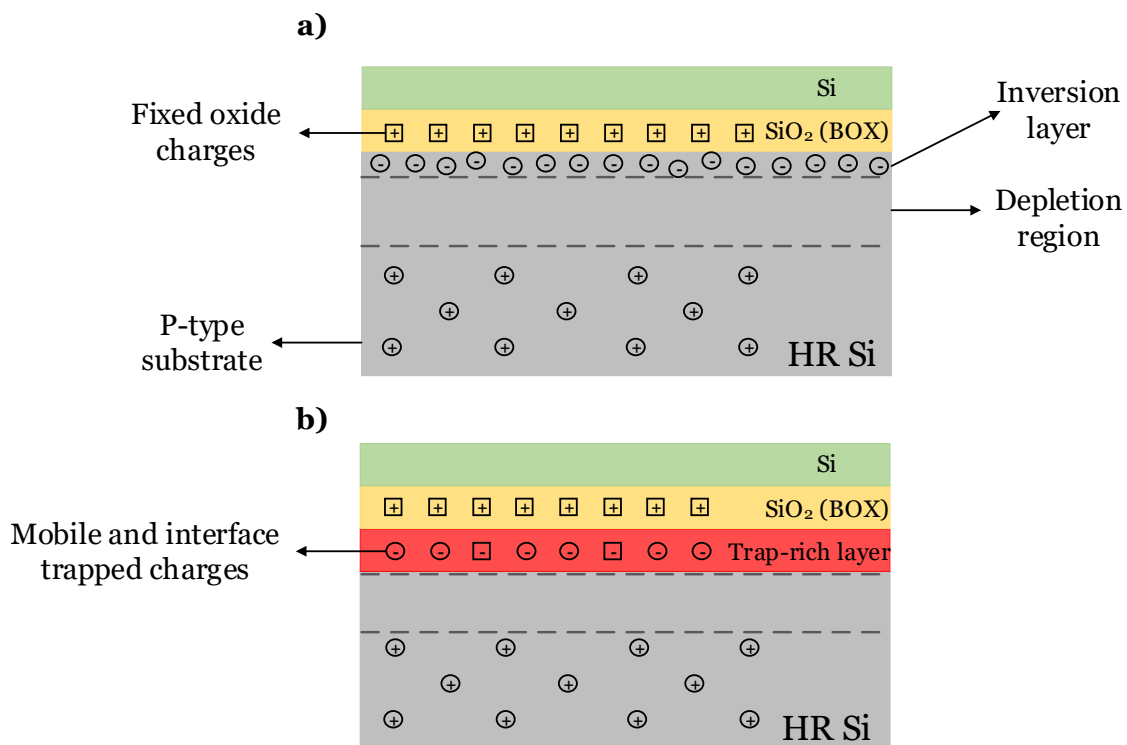


Fig. 3.1. a) Conventional high resistivity SOI substrate b) Trap-rich SOI substrate.

To satisfy the expected demand for low-cost RF components that support the 5G communication bands of 28-32GHz and beyond, trap-rich, high resistivity substrates are being used as part of a 45nm SOI CMOS technology optimized for RFIC applications [34], [35]. The trap-rich substrate is combined with thick copper layers for low-loss CPW and high Q-factor inductors. A digital version of the 45 nm SOI CMOS process has been used

to demonstrate MESFETs on conventional, low resistivity substrates [36]. The MESFETs have soft breakdown voltages exceeding 20 V [9], [37], [38], significantly higher than the nominal 1 V breakdown of the baseline CMOS. The SOI MESFETs are therefore attractive for RFIC and power amplifier applications where the high operating swing allows for RF output powers exceeding 1 Watt [37]. In this paper we compare the DC and RF characteristics of nominally identical MESFETs on low resistivity and trap-rich substrates, fabricated as part of the same wafer-lot fabricated using the 45nm RF SOI CMOS process. The DC characteristics of the devices on the different substrates are statistically identical, as are the small-signal forward current gain $h_{21}$, and cut-off frequency $f_T$. However, the maximum available gain (MAG) and unilateral gain (U) are higher on the trap-rich substrates leading to maximum operating frequencies, $f_{max}$, that are approximately 5-10 % larger.

### 3.2. MESFETs on Trap-Rich Substrates

A cross-section of the SOI MESFET on a trap-rich substrate is shown in Figure 3.1. The devices are fabricated with no changes to the CMOS process flow as described in detail in reference [36]. For this study, the process flow made use of a split wafer lot to compare nominally identical devices fabricated on both trap-rich and conventional low resistivity substrates. The trap-rich substrates are manufactured using high-resistivity, float-zone silicon with a nominal resistivity of >1000 $\Omega$.cm. To suppress the parasitic accumulation layer at the interface between the buried oxide and the substrate an approximately 2 μm thick trap-rich poly-crystalline silicon layer is introduced by chemical vapor deposition prior to the growth of the oxide layer [30]. Transmission line measurements indicate that the effective bulk resistivity of the trap-rich substrate is >900 $\Omega$.cm compared to 10 $\Omega$.cm for the conventional CMOS substrates.

The MESFETs used for this study had device dimensions of $L_g = L_{aS} = L_{aD} = 200$ nm, which are the minimum feature sizes that can be drawn without violating the design rules of the 45 nm RF SOI CMOS technology. A ground-signal-ground (GSG) pad cage allowed for both DC and RF probing. The DC transfer characteristics of the MESFETs fabricated on the trap-rich and low resistivity substrates are described in Section 3.3.
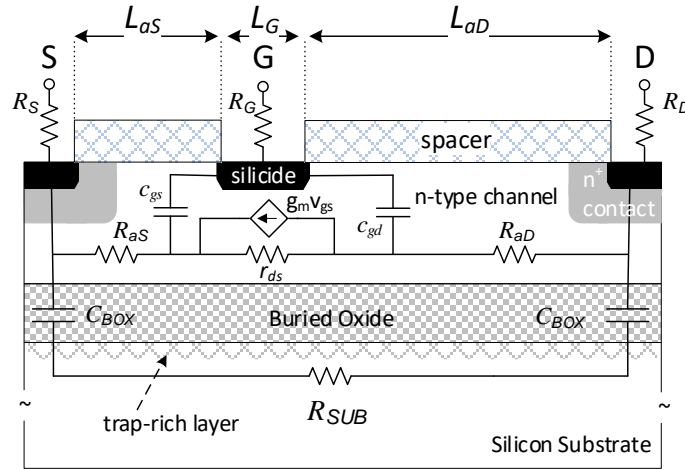


Fig. 3.2. Schematic cross-section of an SOI MESFET [22] with the lumped element components used in the small-signal model.

### 3.3. DC Transfer Characteristics

To compare the DC electrical characteristics of the MESFETs on the conducting and trap-rich substrates we performed a series of measurements that included the family of curves (drain current vs. drain voltage for different front gate bias) and Gummel plots of drain current and gate current on semi-log plots as a function gate voltage. Figure 3.2 shows the family of curves taken from an average of measurements from five devices on each substrate. For these devices with a drain access length of $L_{aD} = 200$ nm we expect a soft breakdown voltage due to impact ionization and avalanche breakdown for $V_D > 6$ V [39], [40]. The FOC shows good output current saturation to $V_D = 5$ V, significantly higher than the nominal 1 V operating voltage of the baseline CMOS. The error bars in Figure 3.2

44

indicates the root-mean-square (RMS) variation in the measurements of the saturated drain current. Based on these results there is little to distinguish between devices on the two substrates in terms of the saturated output current.
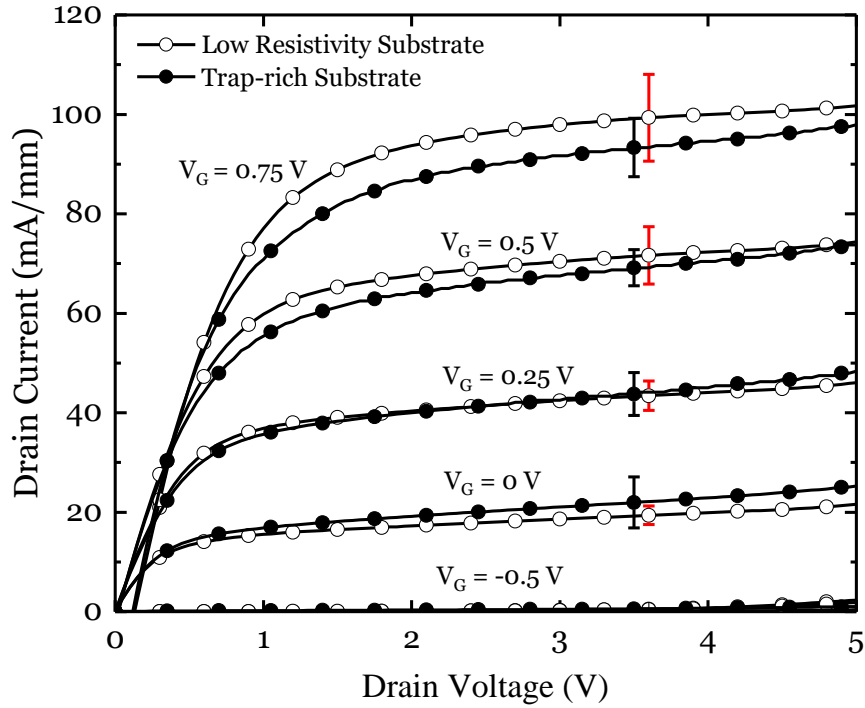


Fig. 3.3. The averaged family of curves (FOC) for MESFETs on trap-rich substrates (solid symbols) and low resistivity substrates (open symbols).

The Gummel plot in Figure 3.3 confirms that the devices have very similar turn-on characteristics. For these plots, drain biases of 25 mV and 3 V are applied, and the drain and gate currents measured as a function of gate voltage. The average drain current for the devices on different substrates is essentially indistinguishable in the strong accumulation regime, well above threshold. Some difference can be seen in the weak accumulation regime but this is likely due to threshold voltage variations ($\Delta V_{th} \sim 25$ mV) that have a more pronounced influence due to the exponential nature of the drain current close to threshold. Likewise, there is an observable difference in the gate current, but the variation is less than the RMS error and is therefore probably not statistically significant.
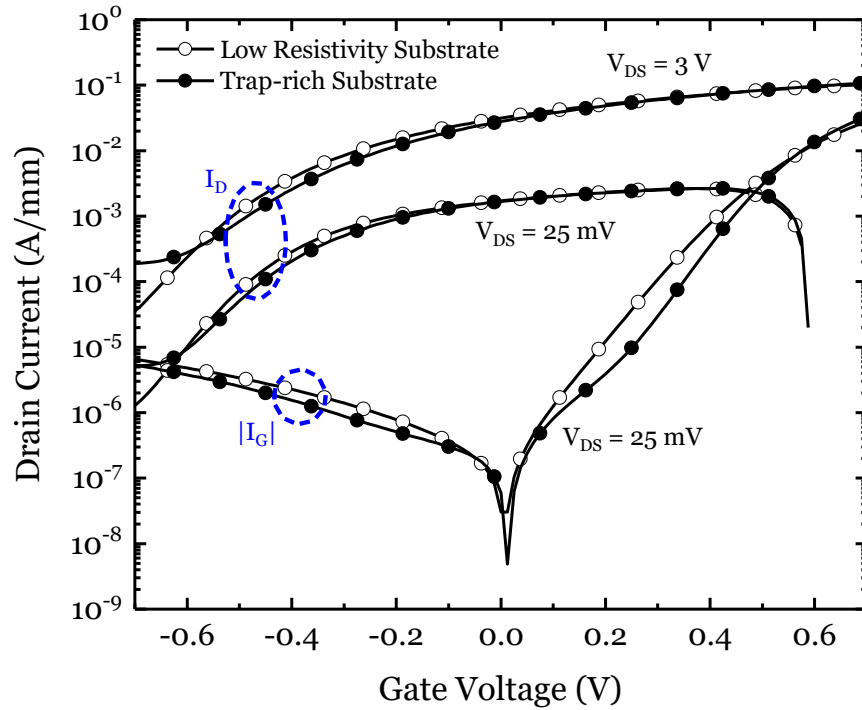
Fig. 3.4. The drain current and gate current magnitude as a function of gate voltage showing the turn-on characteristics of the MESFETs on the two different substrates.

The average transconductance, $g_m$, shown in Figure 3.4 has the same trends i.e. almost identical in strong accumulation with some variation close to threshold that is less than the RMS variation in the measurement. The data in Figures 3.2, 3.3, and 3.4 confirms that the DC transfer characteristics of the MESFETs are essentially identical on the two substrates. A similar conclusion has been reached for n-channel MOSFETs fabricated using different generations of high resistivity and trap-rich substrates [33].
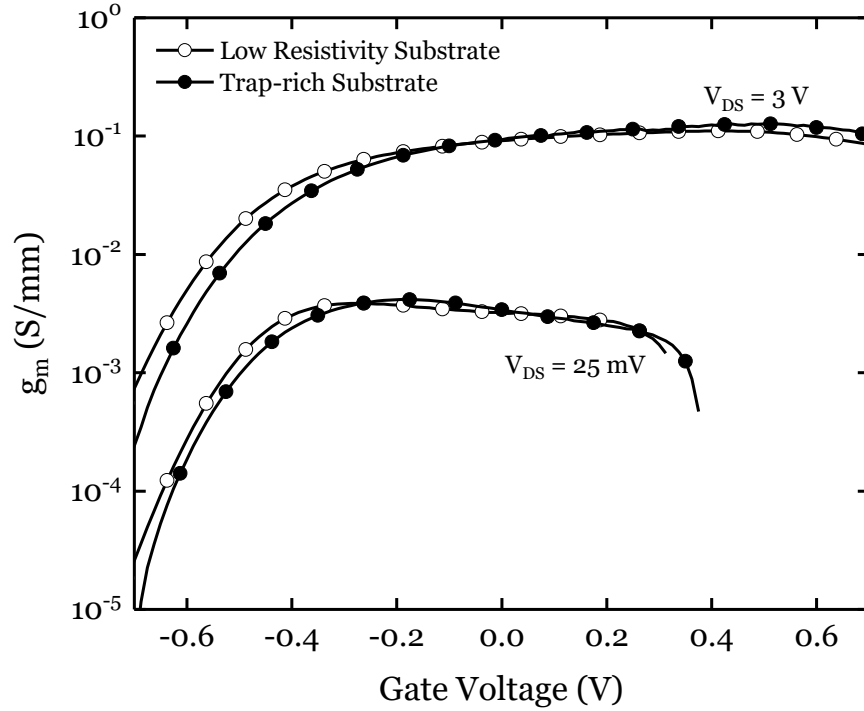
Fig. 3.5. The transconductance derived from the data in Figure 3.4. The peak transconductance at a drain voltage of 3 V is ~110 mS/mm for devices on both types of substrate.

## 3.4. RF Gain Characteristics

The small-signal devices had a multi-finger geometry, with 20 fingers each of width 15 µm for a total device width of 300 µm and their RF characteristics were measured using an Agilent 8510C network analyzer. The parasitic components associated with the GSG pads were de-embedded using open pad structures. The forward current gain, $h_{21}$, maximum available gain, MAG, and unilateral gain, U, were extracted from the S-parameters using Agilent Design Suite (ADS) for different drain current bias. Figures 3.6 and 3.7 show results for $h_{21}$ and the power gains MAG and U, respectively, from a pair of devices on trap rich and low resistivity substrates, after de-embedding the pad parasitics. The MESFETs show highest gain when biased with $V_{GS}$ close to 0.1 V which is the value used for the measurements in Figures 3.6 and 3.7. Extrapolation of the de-embedded $h_{21}$

to 0 dB with a slope of -20 dB/decade (dashed line in Figure 3.6) gives the corrected cut-off frequency, $f_T$.
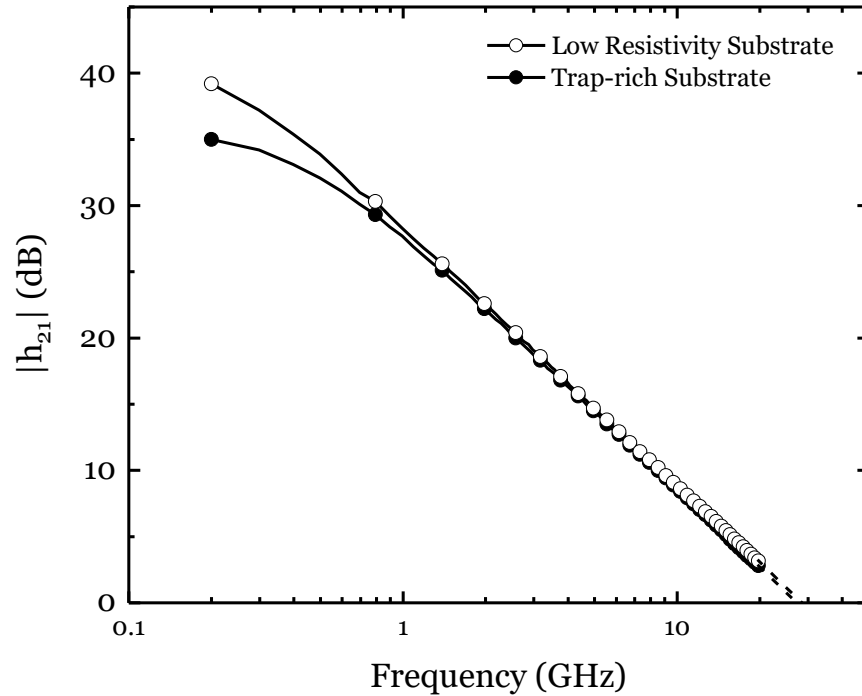


Fig. 3.6. $h_{21}$ for $V_{DS}$ = 5 V and $V_{GS}$ = 0.1 V as a function of frequency to confirm the similar cut-off frequency of 27.5 GHz for MESFETs on trap-rich, and low resistivity substrates.

For the range of frequencies in Figure 3.7 the maximum available gain transitions between unstable and stable regimes that are separated by a cusp at ~ 2 GHz for the low resistivity substrates and ~ 3.5 GHz for the trap-rich substrates. For frequencies above the cusp, MAG and the unilateral gain approach the same asymptote that extrapolates to 0 dB with a slope of -20 dB/decade to determine $f_{max}$. It is evident from the data that while $h_{21}$ and $f_T$ are essentially the same for devices on the two different substrates, the values of MAG and U are larger for the trap-rich substrates, leading to higher values of $f_{max}$.
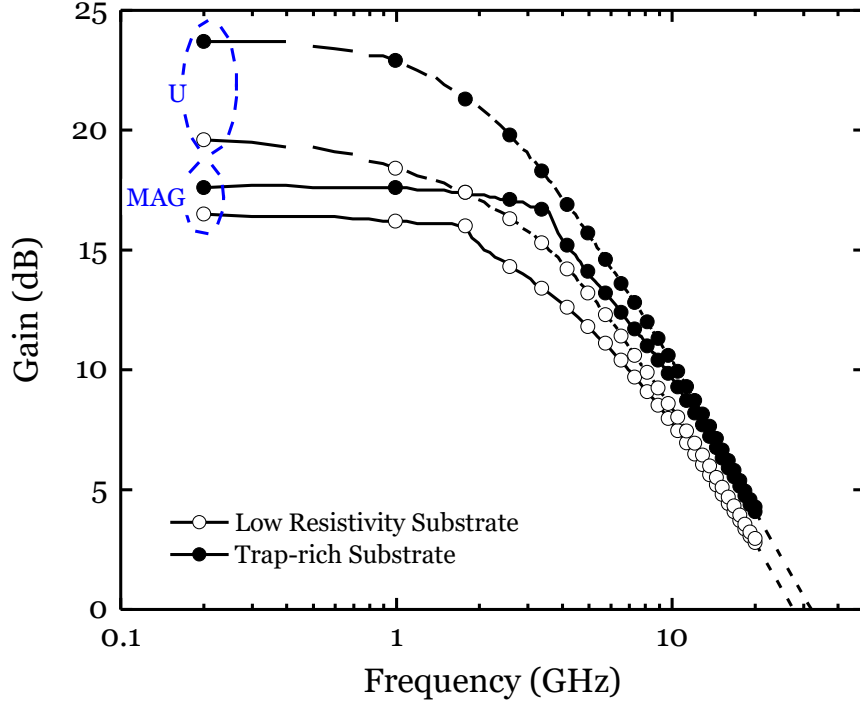
Fig. 3.7. The MAG and U plotted against frequency for $V_{DS}$ = 5 V and $V_{GS}$ = 0.1 V, illustrating the higher $f_{max}$ for the MESFETs on trap-rich substrates (31.5 GHz) in comparison to the MESFETs on conventional low resistivity substrates (29 GHz).

To confirm the increased $f_{max}$ on trap-rich substrates we plot the average values of the de-embedded $f_T$ and $f_{max}$ as a function of drain current in Figure 3.8. The drain current is increased by stepping the gate voltage from −0.1 V to +0.4 V in 0.1 V increments. The RMS variation between the individual measurements of $f_T$ and $f_{max}$ is approximately ± 0.5 GHz as indicated by the error bars. Over a range of drain current bias that encompasses much of the saturated device operation (see Figure 3.2), the maximum operating frequency is consistently 5-10 % higher for the devices on the trap-rich substrates, while the cut-off frequency is essentially the same for both substrates, to within the measurement uncertainty. We explain the enhanced $f_{max}$ in terms of the reduced parasitic conduction in the trap-rich substrates using a lumped element circuit model described in Section 3.5.
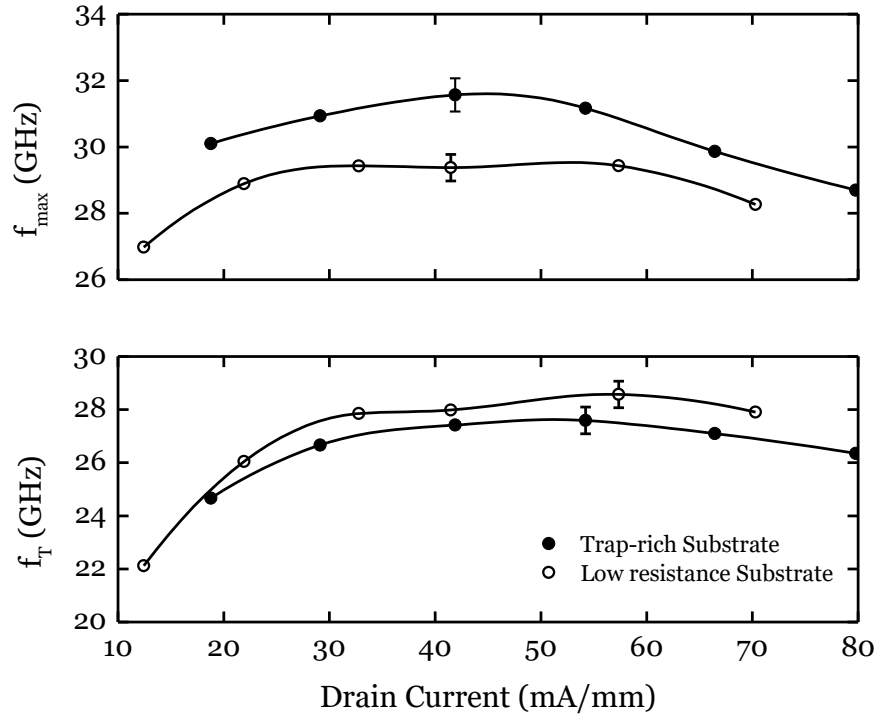
Fig. 3.8. The average values of $f_T$ and $f_{max}$ as a function of drain current for $V_D = 5$ V.

## 3.5. Lumped Element Circuit

The device cross-section of Figure 3.2 includes the main electrical elements of the SOI MESFET approximated as lumped element components. If we ignore the resistance of the channel access regions, $R_{aS}$ and $R_{aD}$, as being negligible compared to the output resistance of the transistor in saturation, $r_{ds}$, we arrive at the small-signal equivalent circuit of Figure 3.9.
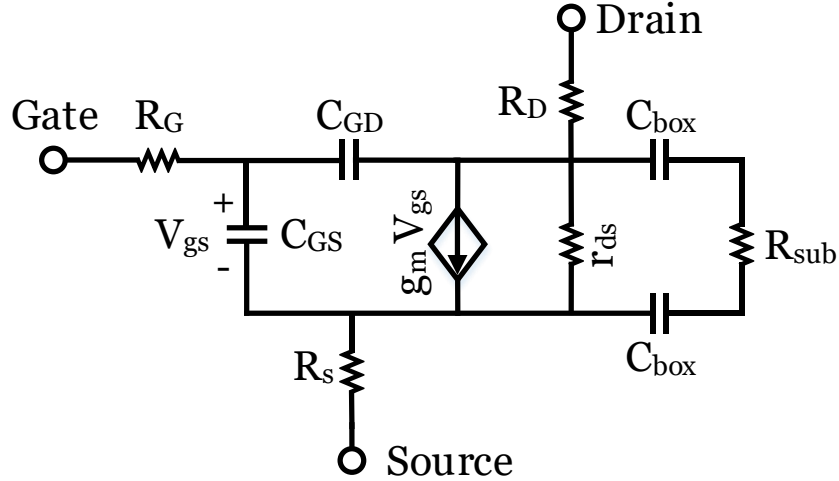
Fig. 3.9. The small-signal equivalent circuit of the SOI MESFETs as interpreted from the cross-section of Figure 3.2.

The circuit is similar to one used earlier for MESFETs from a 350 nm, 3.3 V technology [41], but with the explicit inclusion of the parasitic conduction layer resulting from the buried oxide capacitance, $C_{BOX}$ and the substrate resistance $R_{SUB}$. By shorting the source and drain connections to derive the short-circuit forward current gain, $h_{21}$, it is apparent that no current flows through $R_{SUB}$, and we obtain the usual expression for $f_T$, i.e.

$$f_t = \frac{1}{2\pi} \left[ \frac{C_{gs} + C_{gd}}{g_m} + C_{gd} (R_S + R_D) \right]^{-1} \tag{3.1}$$

The expression in equation (3.1) includes the parasitic source and drain resistances, but does not depend on the extrinsic components associated with the substrate, namely $C_{BOX}$ and $R_{SUB}$. This explains why the measured values of $f_T$ are nominally the same for MESFETs fabricated on the two different substrates.

The maximum available gain is calculated from the S-parameter measurements under the assumption of ideal conjugate matching at the input and output terminals. To take account of the parasitic substrate conduction we modify the usual expression for $f_{max}$ [42] to include $R_{SUB}$ and $C_{BOX}$ in the admittance, $Y_{out}$, that the MESFET presents to a

conjugate matched load. The susceptance of the conjugate load cancels the imaginary part of $Y_{out}$ resulting in equation (3.2).

$$f_{max} = \frac{1}{2} \; f_T \left[ g_m (R_G + R_S) \frac{C_{gd}}{C_{gd} + C_{gs}} + (R_G + R_S) Re[Y_{out}] \right]^{-1/2} \tag{3.2}$$

For the purposes of estimating $Y_{out}$, we can assume that $R_S$ and $R_D$ in Figure 3.9 are small compared to $r_{ds}$, and we arrive at equation (3.3),

$$Re(Y_{out}) = \left[ \frac{1}{r_{ds}} + \frac{4 \; R_{SUB} \; X_c^2}{1 + 4 \; R_{SUB}^2 \; X_c^2} \right] \tag{3.3}$$

where

$$X_c = \omega \; C_{BOX}$$

The area of each of the ten source/drain contacts is 15 μm x 0.52 μm and assuming a buried oxide thickness of 225 nm [43] we estimate the value of $X_c$ to be 0.002 $\Omega^{-1}$ at a frequency of 30 GHz, neglecting any fringing capacitance and depletion at the silicon-BOX interface. To calculate $R_{SUB}$ as a function of the substrate resistivity, $\rho$, we make use of equation (3.4) that is derived [44], [45] for the resistance between two rectangular contacts of length, L, and width, W, separated by a distance, d, on a substrate with thickness, t, that is much larger than the contact dimensions as shown in Figure 3.10. Equation 3.4 assumes the substrate is semi-infinite and its resistivity is homogeneous. The rectangular contacts are approximated with elliptic contacts which have equal area and equal aspect ratio to the rectangular contacts, i.e. a = $\frac{L}{\sqrt{\pi}}$ and b = $\frac{W}{\sqrt{\pi}}$ . The spreading resistance between the two contacts can be approximated as the surface potential of the ellipse S1 (or S2) which passes through the center of the other approximated elliptic

contact. In equation (3.4), $F(\theta\,|\,m)$ is the elliptic integral of the first kind as defined in equation (3.5).

$$R_{SUB} = \frac{\rho}{2a}\left[F\left(\frac{\pi}{2}\,\Big|\,1-\frac{b^2}{a^2}\right)-F\left(\sin^{-1}\left(\frac{a}{\sqrt{a^2+d^2-b^2}}\right)\,\Big|\,1-\frac{b^2}{a^2}\right)\right] \qquad (3.4)$$

$$F(\phi|m) = \int_0^\phi \frac{d\theta}{\sqrt{1-m\sin^2(\theta)}} \qquad (3.5)$$
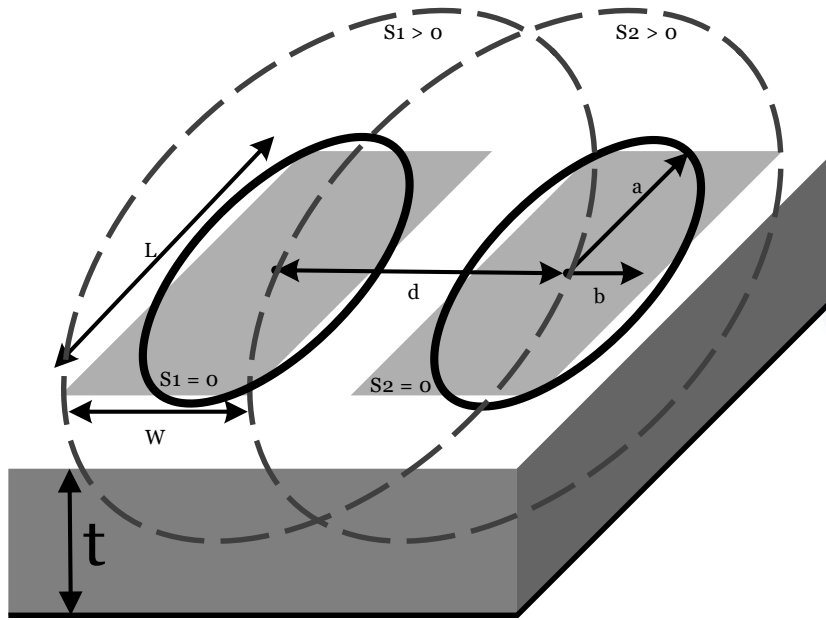


Fig. 3.10. Two rectangular contacts approximated as elliptic contacts to approximate the spreading resistance between the contacts and an infinite backplane.

The small-signal parameters for use in equations (3.2) and (3.3) are extracted as follows [46]–[49]. The MESFET is biased with $V_{DS}$ = 0 V and $V_{GS}$ = -0.7 V (cold FET, reverse bias) and the measured S-parameters converted to Y-parameters, from which the parasitic capacitance at the source, drain and gate are extracted. Next, the device gate is forward biased ($V_{gs}$ = 0.7 V) and the S-parameters are measured under cold-FET conditions with $V_{DS}$ = 0 V. The measured S-parameters are then converted to Z-parameters

to extract $R_G$, $R_D$, and $R_S$. Finally, the intrinsic parameters (i.e. $C_{gd}$, $C_{gs}$, $g_m$, and $r_{ds}$) are determined from Y-parameters derived from the S-parameters measured with the device biased in the active region i.e. with $V_{gs} = 0.1$ V and $V_{DS} = 2.5$ V. The values of the small-signal parameters are summarized in Table 3.1.

TABLE 3.1. SMALL-SIGNAL COMPONENT VALUES EXTRACTED FOR THE SOI MESFETS
ON TRAP-RICH AND LOW RESISTIVITY SUBSTRATES

| $R_G$ | $R_S$ | $R_D$ | $C_{gd}$ | $C_{gs}$ | $g_m$ | $r_{ds}$ |
|---|---|---|---|---|---|---|
| 16 Ω | 6 Ω | 12 Ω | 30 fF | 95 fF | 32 mS | 1200 Ω |
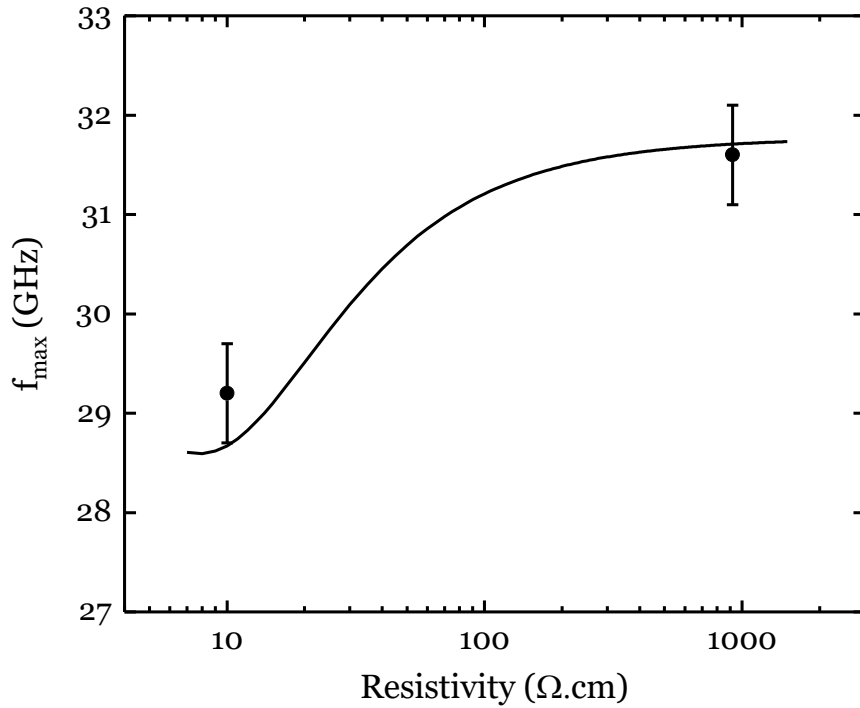


Fig. 3.11. $f_{max}$ as a function of substrate resistivity calculated using equations (3.2) – (3.4). The symbols are the average values measured from the devices on the low resistivity and high resistivity, trap-rich substrates.

The value of $f_{max}$ calculated using equations (3.2) – (3.5) is plotted as a function of substrate resistivity in Figure 3.11. At higher resistivity (i.e. for trap-rich substrates), the value of $R_{SUB}$ is large enough that negligible current flows in the substrate and the power loss can be ignored. As a result, the gain is almost independent of substrate resistivity and $f_{max}$ approaches an asymptotic limit of ~ 31.5 GHz for these devices. But as the substrate resistivity and $R_{SUB}$ decrease, the power loss in the substrate can be significant, thereby reducing the overall power gain and along with it the value of $f_{max}$. The average peak $f_{max}$ measured with devices from the high-resistivity (900 Ω.cm) and conventional CMOS (10 Ω.cm) substrates are also shown in Figure 3.11. The agreement between the measured and calculated values of $f_{max}$ is very reasonable given that no fitting parameters are used for the small-signal model. The measured values are within the ±0.5 GHz RMS variation that is observed in the small-signal model.

### 3.6. Summary and Discussion

SOI MESFETs fabricated on high resistivity, trap-rich substrates have DC characteristics and forward current gain, $h_{21}$, that are essentially identical to similar geometry devices fabricated on conventional low resistivity substrates. However, the maximum available gain is 1-2 dB larger for the devices on the trap-rich substrates, resulting in maximum operating frequencies that are 5-10% higher. The higher power gain and increased operating frequency are attributed to the reduced parasitic conduction in the high resistivity substrate. While the increase in gain and operating frequency are rather small in absolute terms, it illustrates the importance of substrate engineering when it comes to maximizing the performance of devices for RFIC applications.

CHAPTER 4

MOSFET-MESFET CMOS CASCODE AMPLIFIERS

Cascode amplifiers, comprising a common-source MOSFET integrated with a common-gate metal-semiconductor-field-effect-transistor (MESFET), were designed and manufactured using GlobalFoundries commercial 45 nm silicon-on-insulator RF CMOS process. The enhanced breakdown voltage of the MESFETs, combined with the high-speed of the RF MOSFETs, resulted in a maximum measured cut-off frequency of up to 70 GHz, with a maximum available gain of 19 dB at $K$-band frequencies (18-27 GHz) using a 6 V supply voltage [11]. This high frequency operation makes the proposed amplifier a prospective candidate for 5G and millimeter wave applications. This chapter concentrates on the design steps, DC measurements, small-signal RF measurements, and parasitics de-embedding.

4.1. Overview

The demand for low-cost CMOS radio frequency integrated circuits (RFICs) is being driven by a number of rapidly growing markets including consumer wireless devices, automotive electronics, and the anticipated Internet of Things (IoT). High-volume CMOS foundries are well positioned to support this anticipated demand using commercially successful digital platforms. However, the low operating voltage of the digital CMOS is challenging for RFIC design, especially for any power blocks including the RF power amplifier (PA).

An increase in either the voltage or the current (or both) result in a higher output power. As the CMOS technology scales down, the voltage handling capability of the transistors degrades and more junction breakdown voltage restrictions apply which limit the transistor's output power. Thus, achieving power requirements under much lower

voltage ranges calls for excessively increased current levels. The power dissipated in the transistor is proportional to the square of the transistor current. Hence, the higher the transistor current, the higher the power loss in the transistor. Consequently, in order to reduce the transistor power loss and increase the amplifier efficiency at the same time, it's favorable to realize low-current, high-voltage operation. Designing a high power and efficient PA in CMOS technology necessitates seeking ways to safely increase the transistor's maximum tolerable voltage.

Multifarious designs and approaches have been studied to achieve higher levels of output power in CMOS technology. These techniques either focus on increasing the PA's output voltage swing, or its overall output current to deliver a higher output power. To increase the overall current, multiple transistors can be connected in parallel [50], which reduces the total input and output impedance of the PA. Wide multi-finger PA transistors have small optimum resistances, and using them in a parallel combination structure lowers the optimum resistance further. Consequently, high impedance ratio input and output matching networks are required for maximum power transfer. Passive components being lossy in CMOS technology, the final design will suffer from output power degradation and presents a narrower bandwidth. Higher current levels also increase the power loss as explained earlier, and lower power efficiency is another undesirable effect of the parallel connection technique.

To increase the output power of a PA through increasing the output voltage swing, multiple transistors can be connected in series to form a stacked structure [51]. The output voltage signal of each transistor contributes to generate a large overall output voltage swing, and the output impedance of the transistor stack is also higher than an individual transistor. Generally, the transistor gate oxide breakdown, drain to source punch-through breakdown, and substrate breakdown are the design challenges which are needed to be

addressed. The buried oxide layer in the SOI technology shields the substrate from getting exposed to high voltage swings, and allows a constructive summation of the transistor's output voltage signals. Dynamic biasing is also a prevalent approach to avoid the transistor gate junction breakdown, albeit it making the design process more challenging. Theoretically, the simple cascode structure can tolerate a supply voltage which is twice as big in comparison to a single CS transistor. Obviously, the maximum tolerable voltage of the cascode cell changes if custom made transistors are used (such as thick oxide transistors, MESFETs, etc.). Following the same trend, a triple cascode structure consisting of one input CS and two CG transistors can provide 3 times larger output voltage swings compared to a single CS stage. As expected, increasing the number of stacked transistors will enable the use of larger supply voltage values and improves the maximum output power. However, the maximum number of stacked transistors (stages) reported in the literature is four [52], [53]. The limitation in increasing the number of stacked transistors beyond 4 is mainly due to the on-chip bypass capacitors connected to the gate of the CG transistors. As we go up in the stack, the bypass capacitor value decreases, and the bypass capacitor connected to the gate of the output stage approaches the transistor's parasitic capacitances which leads to an impractical design. Other transistor stacking approaches such as [54] use multiple CS stages, each connected to input transformers which increases the die area while reducing the overall PA efficiency.

Power combining techniques deploy multiple amplifiers and drivers to generate a larger output voltage and current signal to boost the overall output power [55]–[58]. One of the widely adopted combining techniques in CMOS technology is realized through transmission line transformers. CMOS transformers are lossy, and their relatively large size increases the total die area and the chip cost. Transformers also introduce inter-winding capacitances due to electrostatic coupling between different inductor turns, which

makes the output signal of the PAs out of phase. Separate signal paths also contribute to the signal phase difference at the output of each stage. Asymmetric signals won't get added efficiently and causes an increase in the power loss and a reduction in the PA efficiency. Matching network design complexity is another disadvantage of the power combining technique which arises from the fact that differently biased and sized PAs with different output optimum load values are supposed to concurrently match to the load. Wilkinson power combiners also require a large die area and don't offer a large bandwidth. Much recent studies targeting the bandwidth improvement of the Wilkinson power combiners have been reported [59]–[61]. Intricate design and limited maximum number of PAs (usually between two to four) in one Wilkinson unit in scaled CMOS technology are however the challenges in employing this solution. To sum up, larger die area that augments the total fabrication cost, higher power loss due to larger parasitic capacitances, and lower quality factor of passive components on CMOS, and limited bandwidth, output power and efficiency are the downsides of power combining methods.

Using modified CMOS technologies such as laterally diffused MOS (LDMOS) [62] and III-V technologies [63]–[66], can also provide higher output power thanks to their much increased transistor $V_{BD}$. However the former requires changes to the conventional CMOS process and a more complicated transistor structure, and the latter raises the total die cost as it employs other technologies, which doesn't help the realization of a fully integrated transceiver.

As explained, FET-stacking [4], [67]–[70] is a well-received solution as it offers compact designs with higher voltage swing and output power, higher optimum loadline impedance with respect to large multi-finger transistors, and potentially higher efficiency as the need for on-chip impedance transformation network is eliminated. Our group's previous work has demonstrated that commercial SOI CMOS foundries can be used to

fabricate MESFETs with no changes to the process flow [7], [37], [71]–[74]. In this chapter, the design, simulation and measurement results of a MOSFET-MESFET cascode cell is presented. These small signal cascode cells were fabricated using the Global Foundries 45 nm SOI CMOS technology. The same technology has been used for MESFET based RF PAs operating up to Watt output levels [37], [72] as well for unconditionally stable, low dropout linear regulators [73]. The main advantage of the approach presented in 4.2 over the conventional stacked CMOS amplifiers is that much higher supply voltage ranges (up to 15 times the nominal transistor breakdown voltage in 45 nm SOI CMOS) can be achieved by using only two transistors in a cascode structure. The presented design greatly simplifies the design, and reduces the die area and the total fabrication cost.

As explained, MOSFET transistors cannot tolerate high voltages and as the technology scales down, their breakdown voltage is reduced. Different techniques can be used to increase the breakdown voltage such as thick oxide transistors, parallel amplification, high voltage devices and cascode architecture. Cascode amplifiers consists of an input transistor which is in a common source (CS) configuration (transconductance amplifier) and another common gate (CG) transistor at the output of the input transistor which acts as a current buffer.

The main advantage of the cascode amplifier is that it provides higher voltage gain as it improves the output resistance ($R_o$). The CG transistor raises the output resistance of the input device by a factor of $g_m r_o$ which equals to its intrinsic gain. The CS stage which acts as a transconductance amplifier provides a current equal to $g_m V_i$ which is passed to the output node by the CG transistor as its current gain is close to one. It is worth pointing out that the overall $G_m$ of the cascode device is equal to the transconductance of the input transistor. Other advantages of the cascode architecture are:

- Increased supply voltage: as explained before, the supply voltage is divided between the cascoded transistors, as in a voltage divider. Therefore, a higher supply voltage can be used as just a portion of that is applied and tolerated by each transistor.

- Better input-output isolation: there is no direct coupling between the input and output which improves the reverse transmission (isolation).

- Higher bandwidth: since there is less direct coupling between the input and output, Miller multiplication of the coupling capacitances reduces and improves the bandwidth.

4.2.    MOSFET-MESFET Cascode Architecture

The cascode architecture divides the supply voltage between the transistors, and a higher supply voltage can be utilized. The most important advantage of the mixed MOSFET-MESFET cascode structure (Figure 4.1) over the classic NMOS-NMOS is increased output power since a much higher supply voltage can be used due to the higher breakdown voltage of the MESFET. The total transconductance of the cascode device and consequently the unity gain frequency is mostly determined by the input transistor. The input transistor is chosen to be an NFET since it has a higher transconductance and unity gain frequency. A MESFET transistor is used as the current drive device which needs to be connected to the supply voltage. In the GlobalFoundries 45RFSOI technology, the maximum drain to source voltage of the NFET transistor should not exceed 1 V. Using the proposed mixed cascode architecture, the supply voltage can be extended beyond 1 V since the breakdown voltage of the MESFET transistor is higher (> 5 V, depending on the transistor characteristics and the biasing condition).
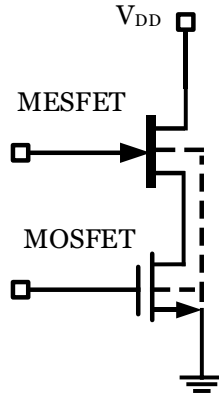
Fig. 4.1. Cascode MOSFET-MESFET RF power amplifier.

A cross-sectional view of the cascode architecture is illustrated in Figure 4.2. Both the NFET and MESFET transistors are fabricated on a common SOI trap-rich substrate, which presents a higher effective substrate resistivity than a conventional high resistivity silicon substrate, and reduces substrate RF losses and crosstalk, leading to superior RF performance [75]. The gate of the MESFET transistor is a Schottky junction which is more robust than the MOS gate of the NFET. As a result, the MESFET can support higher drain voltages than the nominal 1 V breakdown of the body contacted NFETs with gate lengths between 56 nm and 232 nm. Silicide block spacers determine the distance between the gate and drain ($L_{aD}$), and the gate and source ($L_{aS}$). The MESFET gate length ($L_G$) along with the source and drain access length control the transistor breakdown voltage and RF characteristics. Larger $L_{aD}$ forms a longer drift region which increases the breakdown voltage but decreases the cut-off frequency, $f_T$, and maximum oscillating frequency, $f_{max}$. The MESFET access lengths should be set in such a way to represent a reasonable trade-off between the DC and RF performance.
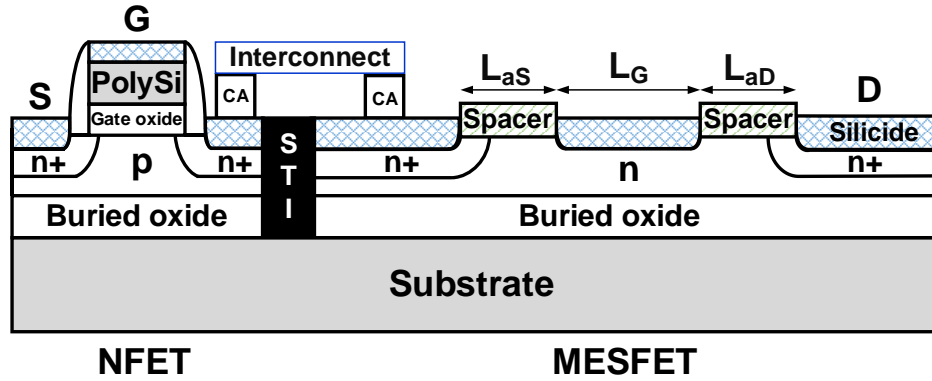
Fig. 4.2. Cascode amplifier cross-section, integrated on a SOI RF substrate.

## 4.3.    MOSFET-MESFET Cascode Design

Figure 4.3 presents the design layout and the die photograph. The MOSFET transistor for this technology has a maximum $f_T$ and $f_{max}$ of 296 GHz and 342 GHz, respectively [34]. It is employed as the input common source (CS) transistor, since the $f_T$ of the cascode is dominated by the input device. The MESFET is the common gate (CG) output of the cascode, connected to the DC voltage supply which can tolerate voltages much higher than the 1 V maximum allowable voltage limit. The initial design challenge is determining the optimum ratio for the width of the MESFET relative to the width of the MOSFET. Since the current drive and transconductance of the MOSFET is higher than the MESFET, a larger total width is expected for the latter. Various designs were simulated using the Verilog-A 4-terminal Angelov model for SOI CMOS MESFETs explained in Section 2.3, along with the 45RFSOI MOSFET models in the process design kit for different transistor widths, with the goal that both devices would be in saturation over the largest range of bias conditions. Based on Cadence simulations, a total width ratio of 1:10 between the MOSFET and the MESFET trades off between the DC and RF performance of the cascode cell. This transistor width ratio is kept for the results presented in this chapter, as the measured amplifiers either have a width ratio of $\frac{W_{MOSFET}}{W_{MESFET}} = \frac{20 \; \mu m}{200 \; \mu m}$ or $\frac{W_{MOSFET}}{W_{MESFET}} = \frac{30 \; \mu m}{300 \; \mu m}$.

Also three different MOSFET gate lengths, i.e. 40 nm, 56 nm and 112 nm which were available to us were used to design three different cascode cells. The cascode cell with the shortest gate length input device is expected to realize the highest $f_T$ and $f_{max}$.
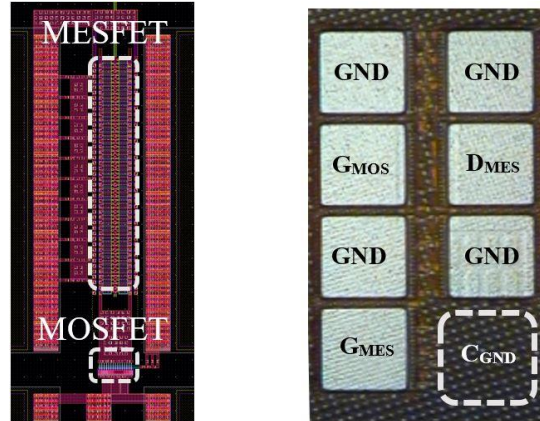


Fig. 4.3. Left: Screen shot of the CG MESFET and CS MOSFET cascode layout using silicon area of 84.7 µm × 13.4 µm. Right: Photograph of the die including GSG pads and integrated capacitor. Silicon area is 414 µm×216.6 µm.

The input and output of the cascode were connected to ground-signal-ground (GSG) pads for RF probing. A separate pad was used to provide the MESFET gate bias. The distance between two transistors is close to the minimum space allowed by layout rules to minimize parasitics. Higher metal layers with lower resistivity were used for the pad connections. Another important design requirement is choosing the value of capacitance used to provide the AC ground at the gate of the MESFET, as indicated by $C_{GND}$ in Figure 4.3. For this design, we wanted to maximize the value of $C_{GND}$ without unduly increasing the silicon area used. Figure 4.3 also illustrates a photograph of the final design that includes the five DC and RF probing pads. By consuming the available unused silicon area roughly equal to the size of one bond pad a value for $C_{GND}$ of 52 pF was obtained. The schematic of the proposed cascode cell is shown in Figure 4.4.
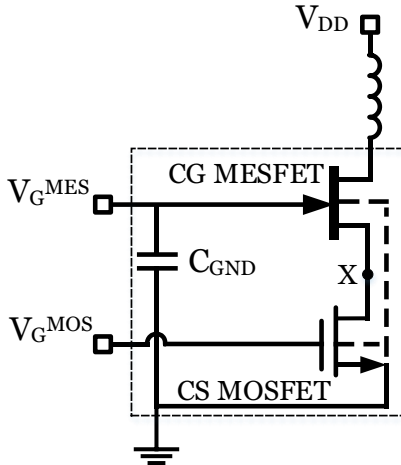
Fig. 4.4. MOSFET-MESFET cascode cell schematic with a $C_{GND}$ = 52 pF.

The biasing condition of the input MOSFET mostly determines the overall DC current of the cascode cell. When a fixed DC biasing voltage is applied to the gate of the MESFET transistor, it automatically adapts to a Vgs which accommodates the required quiescent current which is set by the NFET. If the applied gate voltage is too low, setting the $V_{GS\text{-}MESFET}$ will enforce a low voltage value on the drain of the MOSFET (marked as node "X" in Figure 4.4), pushing that into the linear region. On the contrary, if the applied MESFET gate voltage is too high, setting the MESFET $V_{GS\text{-}MESFET}$ will enforce a high voltage value on the drain of the MOSFET, which can reach the breakdown voltage limit of the transistor. By carefully choosing the gate voltage of the MESFET, the drain voltage of the MOSFET can be kept below $V_{BD}$ (~ 1 V), while accommodating the quiescent current. Due to the extended $L_{aD}$ of the MESFET (200 nm), the voltage supply ($V_{DD}$) can be taken as high as 6 V, without damaging the low voltage CS MOSFET. As the MOSFET has a higher current drive and transconductance ($g_m$) than the MESFET, the size ratio between the transistors needs to be determined and optimized.

## 4.4.    Cascode DC Characterization

As formerly explained, finding the optimum biasing point plays an important role in the performance of the cascode amplifier cell. To begin the DC measurements, a starting quiescent point and a safe DC operating voltage range needs to be determined. The input MOSFET sets the overall current of the amplifier, and its high $f_T$ dominates the overall cut-off frequency, as $f_{T\text{-}cascode}$ approximately equals to the geometric mean of the two transistors in the cell. As Figure 1 in [34] shows, the $f_T$ of the MOSFET is at its highest when $V_{GS}$ is between 0.5 V to 0.7 V. As will be shown later, $V_{GS}$ ~ 0.7 V maximizes the overall amplifier transconductance and $f_T$, and also produces a higher gain than $V_{GS}$ = 0.5 V as there is more DC current passing through the amplifier. Focusing on small-signal measurements, a small output voltage and current signal swing is expected at the amplifier output node. Therefore, a supply voltage value as high as 6 V can be utilized without facing the risk of transistor breakdown.

The last measurement parameter to set is $V_{G\text{-}MESFET}$. It's important to select a value which keeps the MOSFET in saturation region, while protecting that from breakdown. As the MOSFET drain is not connected to a separate pad, it's not possible to monitor its voltage value. The Verilog-A 4-terminal Angelov model can be used to predict the voltage changes of node "X". Figure 4.5 depicts the simulated voltage variation of the intermediate node "X", when a constant $V_{DD}$ = 6 V and $V_{G\text{-}MOSFET}$ = 0.7 V is applied and the MESFET gate voltage, $V_{G\text{-}MESFET}$, is swept from -0.2 V to 1.2 V. The width ratio between the MOSFET and MESFET transistors is 1:10, with the MOSFET width being 30 μm. Based on the simulation result, the voltage range between 0.4 V to 1.2 V would be possible to be used on the MESFET gate to provide a safe operating point for the MOSFET. The important take-away from Figure 4.5 is that the amplifier output current greatly changes with varying $V_{G\text{-}MESFET}$, although the input transistor gate biasing, $V_{G\text{-}MOSFET}$, is kept constant. The

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reason for that is the varying MOSFET overdrive voltage, and the non-constant MESFET gate current flowing into the MOSFET's drain terminal. These parameters should also be accounted for while establishing a biasing point for the amplifier. As can be seen, the quiescent point is dynamic and changes with any of the biasing (controlling) parameters.
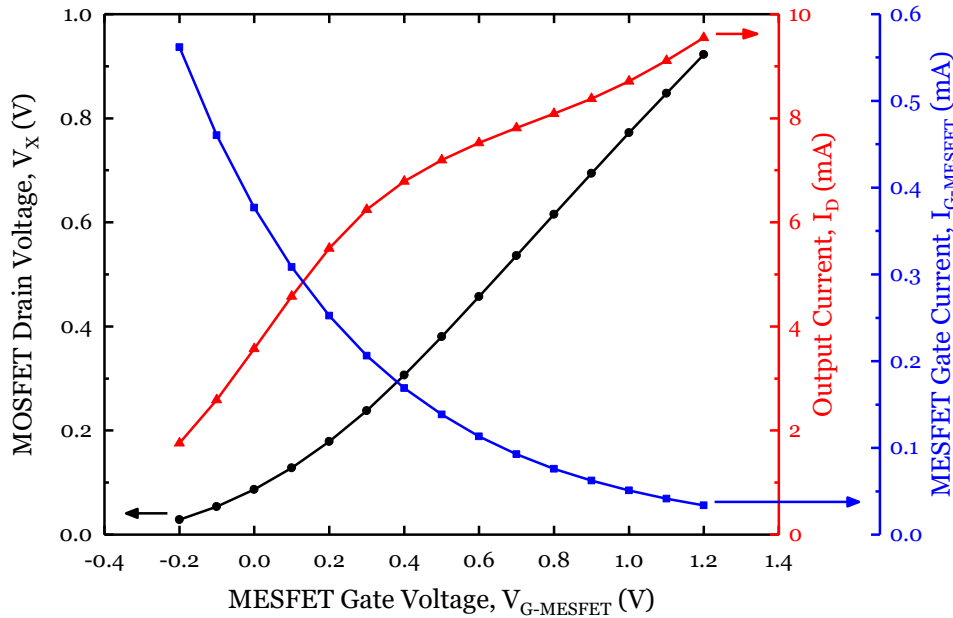


Fig. 4.5. Simulated MOSFET drain voltage ($V_X$), the amplifier output current ($I_D$), and The MESFET gate current ($I_{G-MESFET}$) variations with $V_{G-MESFET}$, while $V_{DD}$ = 6 V and $V_{G-MOSFET}$ = 0.7 V. The width ratio between the MOSFET and MESFET transistors is 1:10, with the MOSFET width being 30 μm.

Notwithstanding the fact that $V_{G-MESFET}$ changes over a 1 V range, its $V_{GS}$ which is the gate-source voltage drop only changes by ~ 0.4 V. So if a large $V_{GS}$ variation is needed, $V_{G-MESFET}$ should be changed over a larger voltage range. $I_{G-MESFET}$ however, undergoes a 76% decrease. This change is due to the large reverse voltage on the gate-drain junction at the beginning of the voltage sweep. With the supply voltage being fixed at 6 V, the large reverse voltage being applied to the gate-drain junctions gets close to the reverse breakdown voltage and the current gets increased exponentially. As $V_{G-MESFET}$ is increased, the reverse voltage is alleviated, and the gate leakage current also decreases. This should

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absolutely be considered when measuring larger PAs, since the leakage current becomes as large as tens of milliamps.

A Cascade Microtech 11000 probe station (Figure 4.6) was used to run the DC measurements such as the family of curves (FOC). The probe station was connected to a HP 4156B Parameter Analyzer and the measurements were set and done using Agilent IC-CAP software. The measured drain current as a function of drain voltage of the cascode cell consisting of a MOSFET with $L_G$ = 112 nm and a total width of 30 μm as the input device, and a 300 μm wide MESFET with all its access lengths equal to 200 nm as the CG device, is shown in Figure 4.7. Compared to Figure 3.1, it is obvious that the cascode architecture extends the breakdown voltage of the individual MESFET to beyond 6 V, and there is no sign of soft breakdown until 6 V.
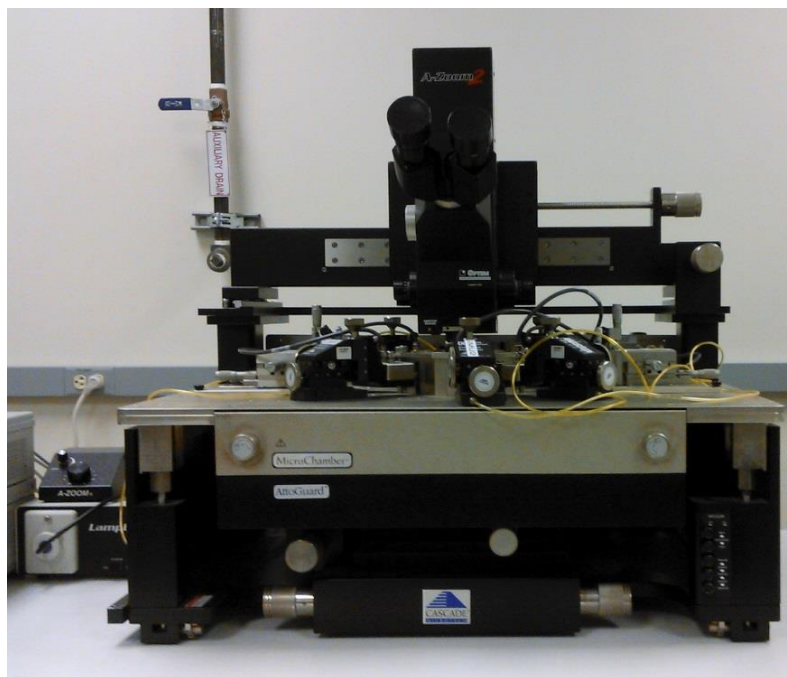


Fig.  4.6. Cascade Microtech 11000 probe station.
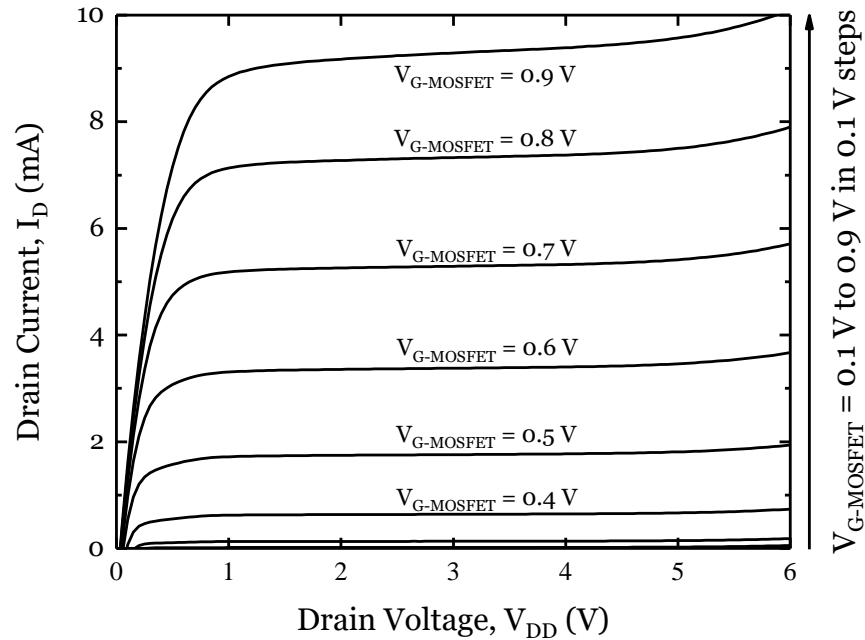
Fig. 4.7. Output current ($I_D$) of the cascode with $L_G$ = 112 nm MOSFET versus output voltage ($V_{DD}$) measurement results, demonstrate an increased $V_{BD}$ from 1 V to more than 6 V. The cascode is biased with $V_{G\text{-}MES}$ = 0.5 V, while $V_{G\text{-}MOS}$ is increased from 0.1 V to 0.9 V.

Figure 4.8 presents the drain current as a function of the MOSFET gate voltage which clearly illustrates that the cascode cell is an enhancement mode device, with a threshold voltage ($V_{th}$) of ~ 0.25 V.
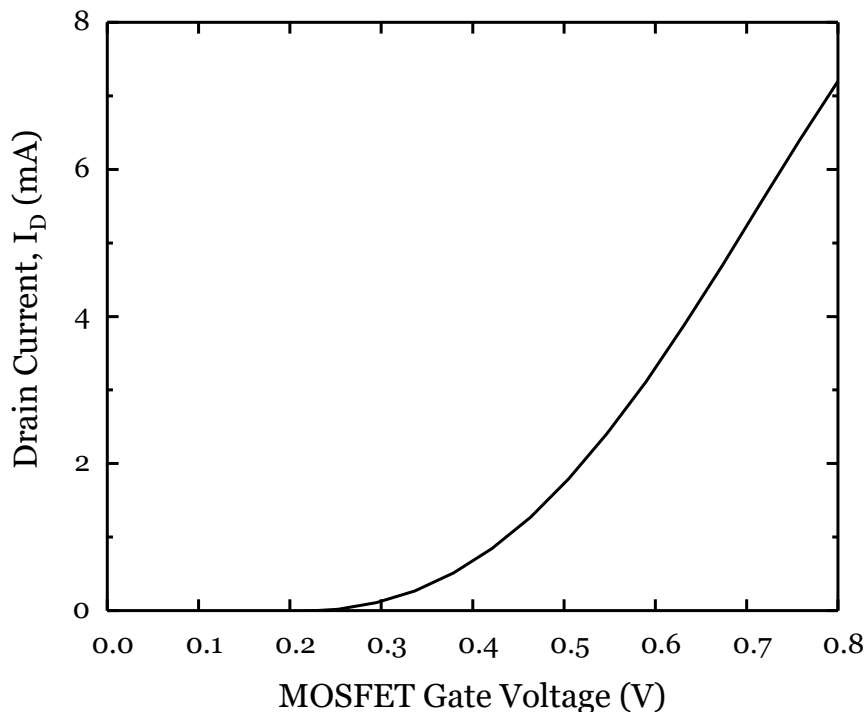
Fig. 4.8. The turn-on characteristics of the cascode with a $L_G$ = 112 nm MOSFET and a 300 μm wide MESFET, for $V_{G\text{-}MES}$ = 0.5 V, $V_{DD}$ = 2 V.

To illustrate how extending the $L_{aD}$ of the MESFET affects the DC performance of the cascode cell, two sets of measurements of the cascodes with the same MOSFET and different MESFET characteristics are presented in Figure 4.9. As expected, the device with $L_{aD}$ = 200 nm MESFET has a higher current drive and lower on-resistance, while the device with $L_{aD}$ = 1000 nm MESFET has a significantly higher breakdown voltage, along with an increased saturated output resistance. The device with a shorter $L_{aD}$ has a soft breakdown voltage of ~ 4 V, above which the drain current slowly increases with increasing $V_{DD}$ due to leakage from the drain-gate junction of the MESFET [9].

By extending the MESFET's drain access length ($L_{aD}$), a $V_{BD}$ greater than 17 V will be achievable which is 17 times higher than the $V_{BD}$ of the body-contacted and the floating body MOSFETs in this technology node. The MESFET with a longer $L_{aD}$ has a larger parasitic resistance, but since the current in the cascode cell is being determined by the

input MOSFET transistor, the drain current levels are almost the same as Figure 4.7 where the drain current of a cascode cell with $L_{aD}$ = 200 nm MESFET is shown.
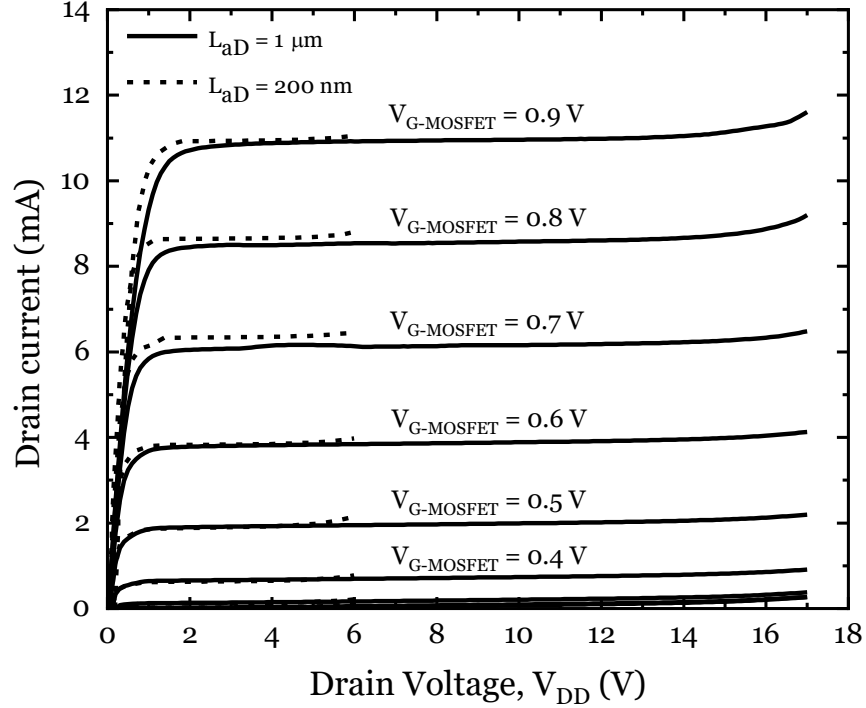


Fig. 4.9. The measured drain current of the cascode amplifier as a function of supply voltage ($V_{DD}$) for MESFETs with $L_{aD}$ of 200 nm and 1000 nm. MOSFET gate voltages are 0.1 V to 0.9 V in 0.1 V steps. A fixed MESFET gate voltage of 0.5 V is applied.

To attain a superior RF performance, the input MOSFET transistor can be substituted with another MOSFET with a shorter $L_G$ available in this technology. Since the $f_T$ and $f_{max}$ are inversely proportional to the transistor's $L_G$, and the total $f_T$ and $f_{max}$ of the cascode cell is dominated by the input MOSFET, a cascode cell operating at higher frequencies can be designed. Using the smaller $L_G$ input MOSFET transistor leads to a slightly higher DC quiescent current as the MOSFET's drain current:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{4.1}$$
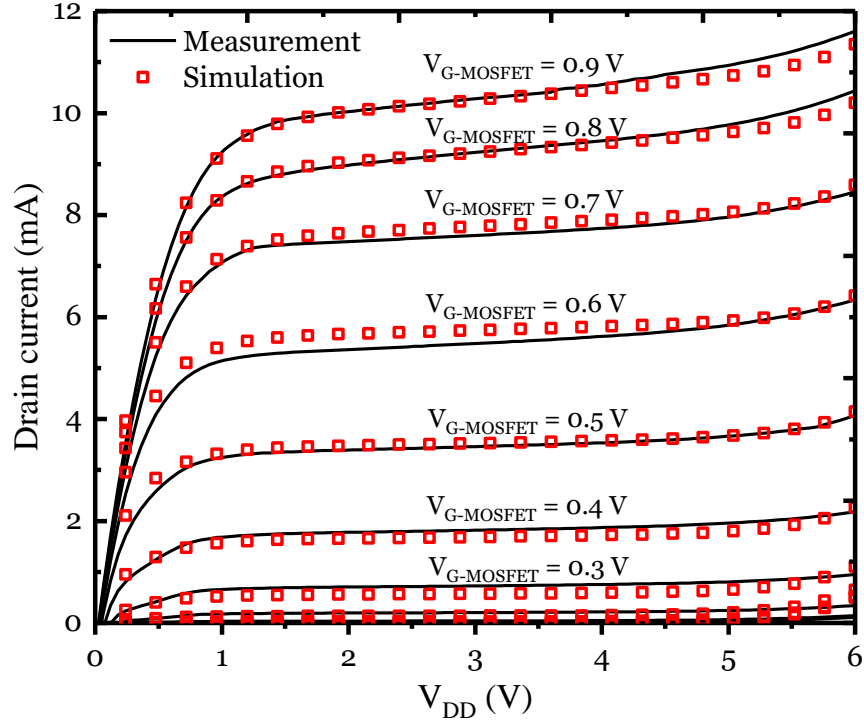
Fig. 4.10. Cascode with $L_G$ = 40 nm MOSFET and $L_{aD}$ = $L_{aS}$ = $L_G$ = 200 nm MESFET output current ($I_D$) versus output voltage ($V_{DD}$) measurement (line) and simulation (symbol) results. The MOSFET to MESFET width ratio is 20 µm to 200 µm. The cascode is biased with $V_{G\text{-}MES}$.

As an example, the measured output current ($I_D$) of a Cascode cell with $L_G$ = 40 nm versus output voltage ($V_{DD}$) is shown in figure 4.10. The width ratio between the MOSFET and MESFET width is 20 µm to 200 µm, and all the MESFET access lengths are 200 nm. To emphasize the accuracy of the 4-terminal Angelov MESFET model introduced in Section 2.4, the simulated current results are also provided in Figure 4.10 which was exported from a Cadence test-bench that utilized the foundry MOSFET models and the 4-terminal Angelov MESFET model.

The measured and simulated drain current and transconductance as a function of gate voltage are also shown in Figure 4.11. The cascode cell dimensions are the same as the one used in Figure 4.10. Both of these figures illustrate a reasonable agreement between the measured data and simulated results.
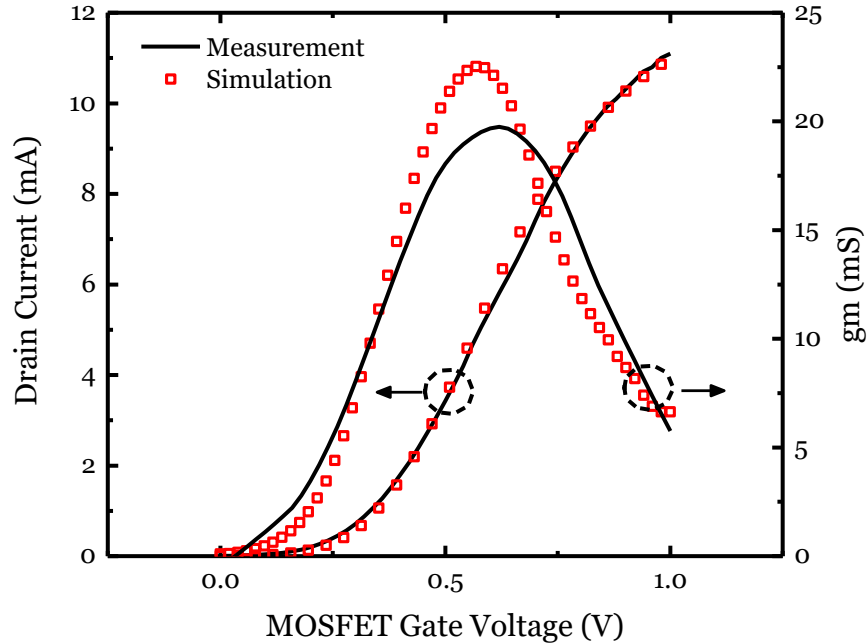
Fig. 4.11. The measured drain current and transconductance as a function of the MOSFET gate voltage. The CS MOSFET has $L_G$ = 40 nm and $W_G$ = 20 μm, while the MESFET has $L_G$ = 200 nm and $W_G$ = 200 mm. The MESFET gate bias is fixed at $V_{G-MES}$ = 0.5 V and $V_{DD}$ = 6 V.

As Figure 4.11 illustrates, the maximum transconductance of the cascode cell is achieved when the MOSFET gate voltage is between 0.5 V to 0.7 V. Since the maximum transconductance leads to a maximum $f_T$ and $f_{max}$, this optimum voltage range should be taken into account while the cascode cell is biased for an optimum RF performance.

### 4.5. Cascode RF Characterization

After completing the DC measurements, RF characterization of the cascode amplifier should be done. The Cascade Microtech Microwave R&D probe station was used for the RF measurements. Other equipment used for the RF measurements are an Agilent vector network analyzer (VNA) 8510C, and an HP 8517B S-parameter test set. An important part of the mixed cascode design project is to have an understanding of the behavior of each transistor and the corresponding characteristics. Since the total cut-off

frequency of the cascode device is the approximately the geometric mean of the cut-off frequency of each transistor, by knowing the value of each $f_t$, a good approximation of the total $f_t$ can be made.

Before starting the RF measurements, the network analyzer needs to be adjusted to the required measurement settings such as frequency range, averaging, etc. Then the network analyzer should be calibrated which ensures the accuracy of the measurements by vector error corrections (this removes the measurement errors in the VNA, cables, adapters, etc.). Calibration can be done using WinCal software supplied by Cascade Microtech. The VNA calibration helps us determine the actual performance of the intrinsic amplifier by removing (i.e. de-embedding) the effect of cables, pads and interconnection parasitics and improves the accuracy of the measurements. However, the resulting S-parameters which are referred to as the intrinsic S-parameters are more prone to additional calculation errors and uncertainties. Among different calibration methods, two were often used [76]–[80]:

Short-Open-Load-Thru (SOLT): It is available on most of the VNAs and requires a calibration kit (CalKit). For probe measurements, well defined open, short, load and thru standards which have fully known behavior and S-parameters are required. By measuring the standards and comparing the measured S-parameters to what is expected, the errors contributed by the cables, pads and interconnects can be calculated. SOLT calibration utilizes a 12 parameter model containing 12 equations and 12 unknowns to address the error sources. Calibration for a characteristic impedance of 50 Ω was chosen which removes the systematic error terms and the calibration can be performed across a wide frequency range, but also suffer from probe placement sensitivity, and increasing error with frequency.

Line-Reflect-Reflect-Match (LRRM): which requires the delay value corresponding to the thru standard and also resistance of the match. The match is the only impedance which needs to be defined and is usually a laser-trimmed co-planar resistor. Hence the errors stemming from the non-ideal definitions of the open and short are avoided. The reflect standards are significantly different (e.g. an open and a short), but each reflect standard should be the same at each port. LRRM calibration is not self-consistent, meaning that the reflect standards are not forced to present a perfect behavior and any error will show as a magnitude, but no reflection coefficient will be greater than one. Since LRRM calibration is less sensitive to the standards and also probe placement variations, it was mainly used before the measurements as the preferred calibration technique.

A Cascade Microtech Impedance Standard Substrate (ISS) was used for the calibrations which is shown in Figure 4.12.
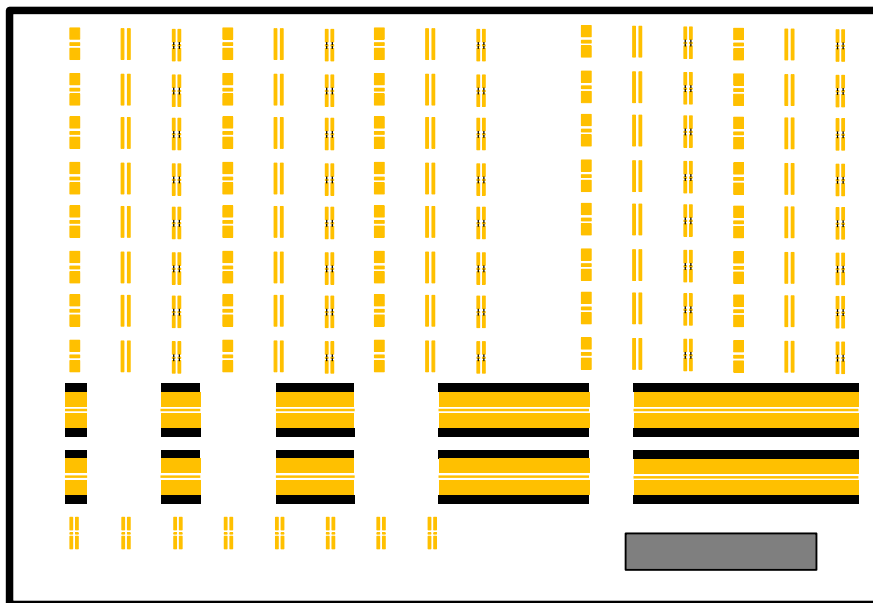


Fig. 4.12. Cascade Microtech Impedance Standard Substrate (ISS).

Air Co-Planar Transition (ACP) probes which were used in the RF probe station for wafer probing utilize low loss Teflon dielectric coaxial microwave absorbers [80] to offer rigid high power measurement capability. Its contact resistance is report to be only 30 mΩ [76] which hardly affects the DC biasing points.
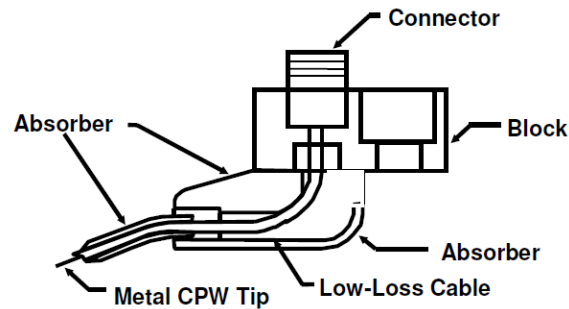


Fig. 4.13. Air Co-Planar Transition (ACP) probe structure [76].

System stability can be checked after the VNA calibration which shows whether the calibration is acceptable or not.

4.6.     Parasitics De-embedding Procedure

After the system calibration is done, open, shorted and thru dummy devices fabricated on the same die as the amplifier is located, should be measured and compared to the calibrated system S-parameters to allow the calculation of the parasitics resulting from the die pads and interconnects. For a single transistor such as a stand-alone MESFET, this can be achieved through WinCal software from Cascade Microtech. The software asks to place the probes on open, shorted and thru pads individually and in turns, then measures and stores the corresponding S-parameters. Parasitics will then get calculated automatically using an algorithm developed by the company which is unknown to the user. The next step will be biasing the amplifier itself and measuring its S-parameters at this specific biasing point which can be referred to as extrinsic S-

parameters. Extrinsic S-parameters reflect the effects of the parasitics on the die as well, and to find the intrinsic S-parameters of the amplifier for further analysis, the calculated parasitics should be de-embedded. This step is called Pad Parasitic Removal (PPR) in WinCal software and intrinsic S-parameters with the effects of the parasitics removed will be provided afterwards. During PPR, S-parameters of the dummy open and short devices on the die (Figure 4.14) are measured and saved. After measuring the S-parameters of the main device, all S-parameters are converted to Y or Z parameters and the dummy device results are subtracted from the main device results.
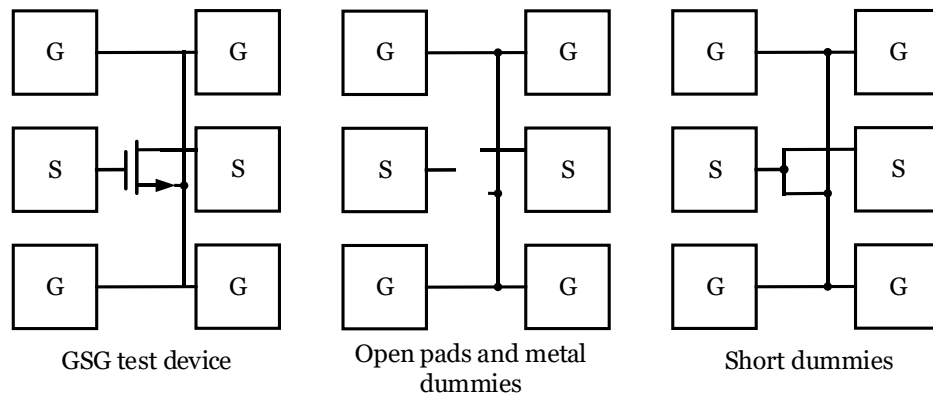


Fig.  4.14. General PPR steps in WinCal.

There are two limitations regarding WinCal PPR for the MOSFET-MESFET cascode amplifiers. Firstly, only open pads were fabricated on the die for the de-embedding step and shorted and thru pads were not available. The reason was the variable width ratio between the MOSFET and the MESFET in the cascode amplifier, and also different interconnect layouts ensued from the variable size ratio. Secondly, PPR mostly applies to a single transistor, and does not provide accurate results for more complicated device under tests (DUTs). The mixed cascode amplifier consists of one enhancement mode and one depletion mode transistor which has an extra pad connected to the gate of the common gate device (MESFET). WinCal PPR didn't generate logical results for the de-

embedded cascode amplifier S-parameters and another solution had to be sought to accomplish de-embedding.

### 4.6.1. Cold-FET Measurement

The Cold-FET measurement is a widely used method to extract the external parasitics [81]–[83]. By adjusting the DC biasing points, it can be modified to be applied to the cascode amplifier and approximate the parallel and series parasitic values. A general two-port equivalent circuit as in Figure 4.15 can be assumed for external parasitic components. $C_{P\text{-}GD}$ is the coupling capacitance between the input and output port which is caused by the substrate interaction and fringing capacitances.
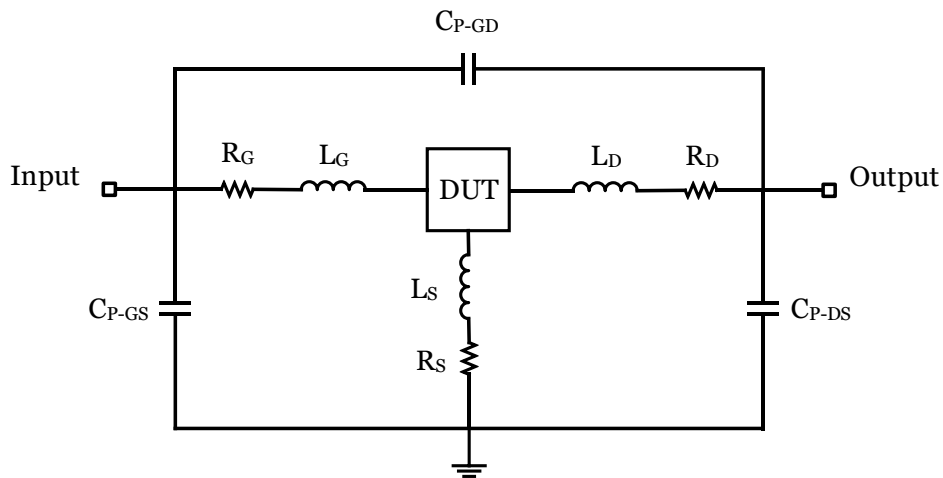


Fig. 4.15. Cold-FET two port equivalent circuit.

With the additional MESFET gate pad and parasitic capacitances in the cascode cell, the equivalent circuit should be assessed to see if it is applicable to the cascode cell or not. Figure 4.16 depicts all the pads, parasitic capacitances, and coupling parasitic capacitances in the cascode cell. $C_{GND}$ is the 52 pF on chip AC ground capacitor connected to the MESFET gate. As will be explained later, the DUT will be considered as an open circuit during the first step of the Cold-FET measurement, and parasitic capacitances can

be calculated. As shown in Figure 4.16, the gate of the MESFET is an AC ground during the RF measurements, so $C_{GND}$ can be ignored as it doesn't affect the rest of the parasitic components.
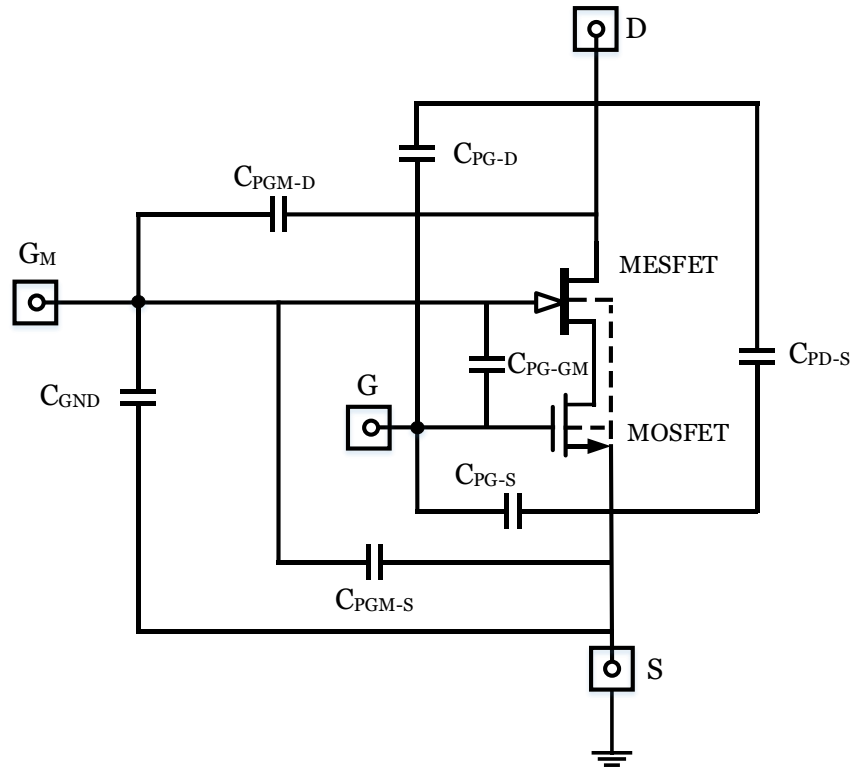


Fig. 4.16. Pad and coupling parasitic capacitances in the cascode cell.

Where

$C_{PG-S}$ : parasitic capacitance between MOSFET gate and source

$C_{PS-GM}$ : parasitic capacitance between MESFET gate and MOSFET source

$C_{PD-S}$ : parasitic capacitance between MESFET drain and MOSFET source

$C_{PG-D}$ : parasitic capacitance between MOSFET gate and MESFET drain

$C_{PD-GM}$ : parasitic capacitance between MESFET gate and drain

$C_{PG-GM}$ : parasitic capacitance between MESFET gate and MOSFET gate

Since the source of the MOSFET in the cascode cell will also be grounded during the RF measurements as well, the parasitic capacitance between MESFET gate and MOSFET source pads can also be ignored, and the parasitic capacitances will reduce to Figure 4.17.
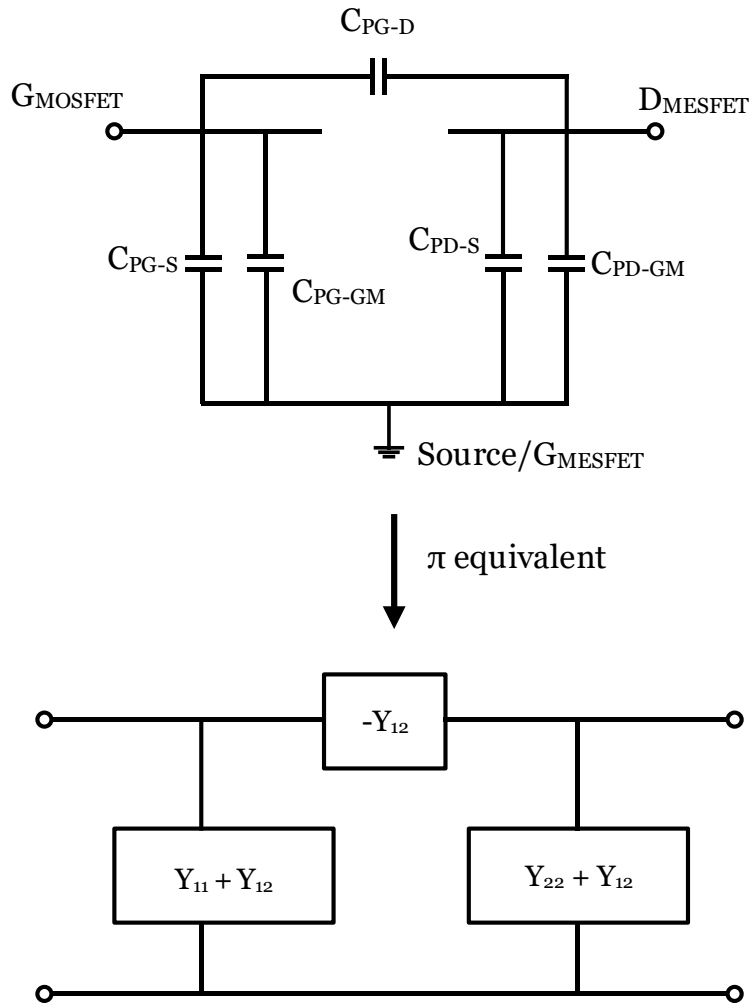


Fig. 4.17. Cascode cell parasitic capacitances $\pi$ equivalent model.

From Figure 4.17, we can find each of the admittance blocks in the $\pi$ equivalent model:

$$C_{PG-D} = Y_3 = \text{Im}\left(\frac{-Y_{12}}{\omega}\right) \tag{4.2}$$

$$C_{PG-S} + C_{PG-GM} = Y_1 = \text{Im}\left(\frac{Y_{11}}{\omega}\right) + \text{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{4.3}$$

$$C_{PD-S} + C_{PD-GM} = Y_2 = \text{Im}\left(\frac{Y_{22}}{\omega}\right) + \text{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{4.4}$$

A similar approach can be adopted to prove that the cascode cell's series parasitic components can be summarized to what is shown in Figure 4.15. As will be explained, series parasitic components will be calculated during the Cold-FET measurement's second step where the DUT can be considered as a short circuit. With the pad parasitic components removed and the DUT shorted, the series parasitic resistance and inductance in the MOSFET gate and source, and MESFET gate and drain path can be summarized to Figure 4.18.

$Z_{12}$ can be calculated as follows:

$$Z_{12} = (R_S + j\omega L_S)\|(R_{GM} j\omega L_{GM}) = \frac{R_S R_{GM} - \omega^2(L_S L_{GM}) + j\omega(R_{GM}L_S + R_S L_{GM})}{R_S + R_{GM} + j\omega(L_S + L_{GM})} \tag{4.5}$$

Assuming an operating frequency of 10 GHz and parasitic inductances in pH range:

$$\omega^2 \times L^2 = 10^{20} \times 10^{-30} \tag{4.6}$$

Equation (4.6) results in a negligible value which can be disregarded. By eliminating the terms containing $\omega^2 \times L^2$, $Z_{12}$ can be simplified to equation (4.9).
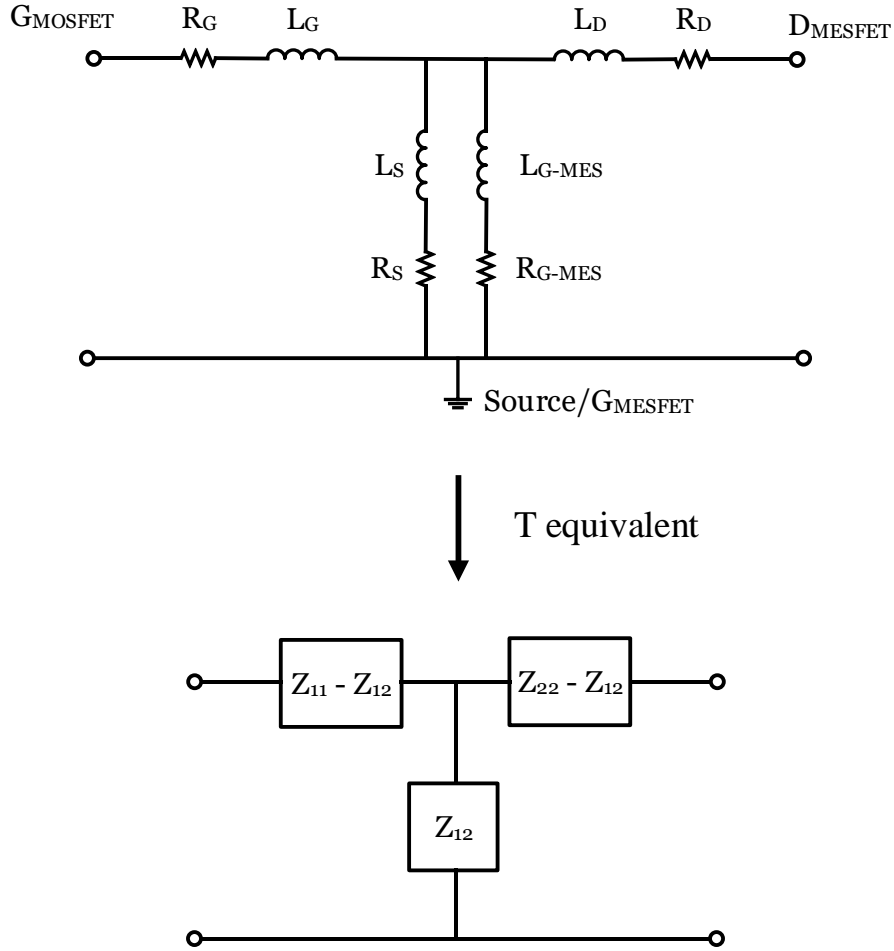
Fig. 4.18. Cascode cell series parasitics T equivalent model.

Impedance parameters of the T model can be calculated using equations (4.5) through (4.9).

$$Z_{11}\text{-}Z_{12}=R_G+X_{LG} \tag{4.7}$$

$$Z_{22}\text{-}Z_{12}=R_D+X_{LD} \tag{4.8}$$

$$Z_{12}=Z_{21}\frac{R_S R_{GM}}{R_S+R_{GM}}+j\omega\left(\frac{(R_{GM}L_S+R_S L_{GM})}{R_S+R_{GM}}-\frac{(L_S+L_{GM})R_S R_{GM}}{(R_S+R_{GM})^2}\right) \tag{4.9}$$

Cold-FET measurement imitates the behavior of a reciprocal two port network since the equivalent circuits shown in Figures 4.17 and 4.18 do not contain any non-

reciprocal components (i.e. active devices, ferrites, etc.). Hence, $Z_{12} = Z_{21}$ in equation (4.9) and the DUT structure is assumed to be symmetric during the Cold-FET measurement ($V_{DS}$ = 0). To conclude, Cold-FET measurement can be applied to the cascode cell under study to de-embed the external parasitics and find the intrinsic S-parameters.

As discussed earlier, there are two main steps in the Cold-FET measurement. In the first step, the DUT should be reverse biased which leads to finding the shunt parasitic capacitances. The DUT is supposed to get completely turned off and can be considered as an open circuit. Therefore, the equivalent circuit will be simplified to Figure 4.19 and the series parasitic components will be floating.
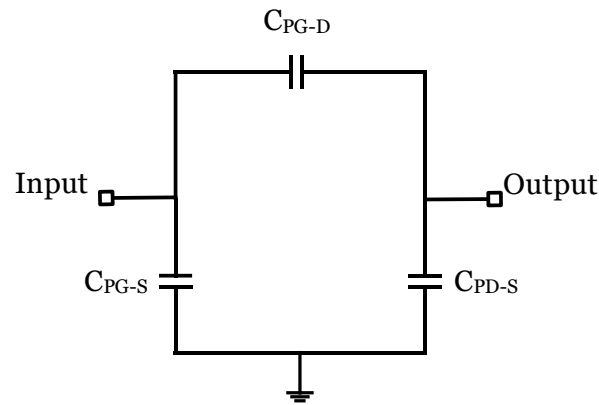


Fig. 4.19. Reverse biased equivalent circuit with the series parasitics removed.

If the DUT is assumed to be a single transistor for the reverse biased Cold-FET step, the $V_{gs}$ of the transistor should be well below the threshold voltage, with $V_{DS}$ = 0, to ensure no current is flowing through DUT, no carrier is drifting from source to drain and it can be eliminated from the equivalent circuit. The same condition should be applied to the cascode amplifier as well, with the difference that the biasing condition should be selected in such a way that both of the transistors are off. After trying biasing conditions, $V_{G\text{-}MOSFET}$ = -0.7 V, $V_{G\text{-}MESFET}$ = -1 V, $V_{D\text{-}MESFET}$ = 0 V was found to be the optimum biasing point for the reverse Cold-FET step. When the current flowing through the DUT is set to

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be close to zero, the S-parameters of the reverse biased cascode amplifier should be measured in order to approximate the pad parasitic capacitances. The measured S-parameters of the reverse biased DUT can be converted to admittance parameters and the pad parasitics will be as follows:

$$C_{\text{P-GD}}=\text{Im}\left(\frac{-Y_{12}}{\omega}\right) \tag{4.10}$$

$$C_{\text{P-GS}}=\text{Im}\left(\frac{Y_{11}}{\omega}\right)+\text{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{4.11}$$

$$C_{\text{P-DS}}=\text{Im}\left(\frac{Y_{22}}{\omega}\right)+\text{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{4.12}$$

Measuring the pad parasitic capacitances using the explained procedure, equations and biasing conditions led to ~ 68 fF parasitic capacitance for $C_{P\text{-}GS}$ and $C_{P\text{-}DS}$. All the calculations on the S-parameters files were done in the Keysight Advanced Design Systems (ADS) after importing the measured S-parameter files. To verify the accuracy of the measured pad parasitic capacitances, Calibre RC Extraction (PEX) was done in Cadence on the open pads layout shown in Figure 4.20. This layout is identical to Figure 4.19, and does not contain any series parasitic component. As a result, it can be evaluated to find the pad parasitic capacitances.
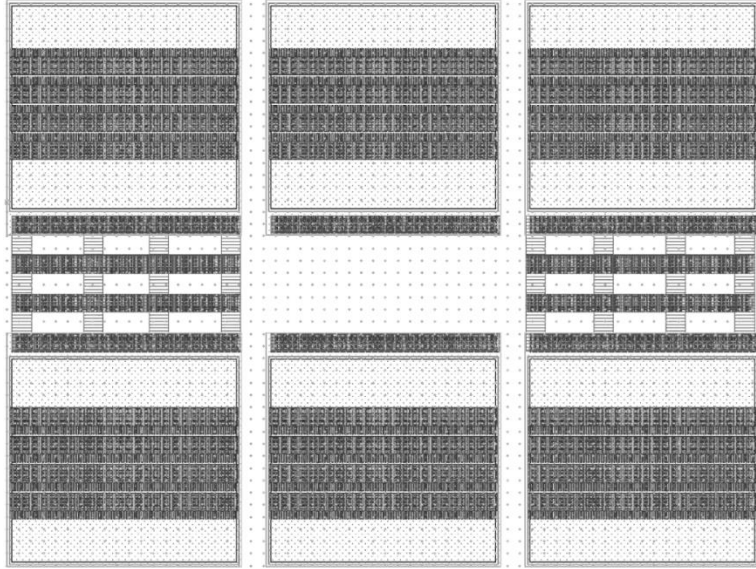
Fig. 4.20. Open pads layout evaluated in Calibre PEX.

The calculated pad parasitic capacitances through reverse biased Cold-FET S-parameter measurement and Calibre PEX are presented in Figure 4.21. There is a reasonable agreement between the results, and the parasitic capacitance values used in equations (4.13) – (4.16) are provided in Table 4.1:

Table 4.1. CASCODE AMPLIFIER PARALLEL PARASITIC CAPACITANCE VALUES

| $C_{P\text{-}GS} \sim 68$ fF | $C_{P\text{-}GD} \sim 7$ fF | $C_{P\text{-}DS} \sim 68$ fF |
|---|---|---|

There is one more step before getting the intrinsic cascode amplifier S-parameters, which is removing the series parasitic components from the calculated Y-parameters in equations (4.5) – (4.8). After removing the parallel parasitic capacitances, the equivalent circuit illustrated in Figure 4.15 is reduced to the circuit in Figure 4.22.
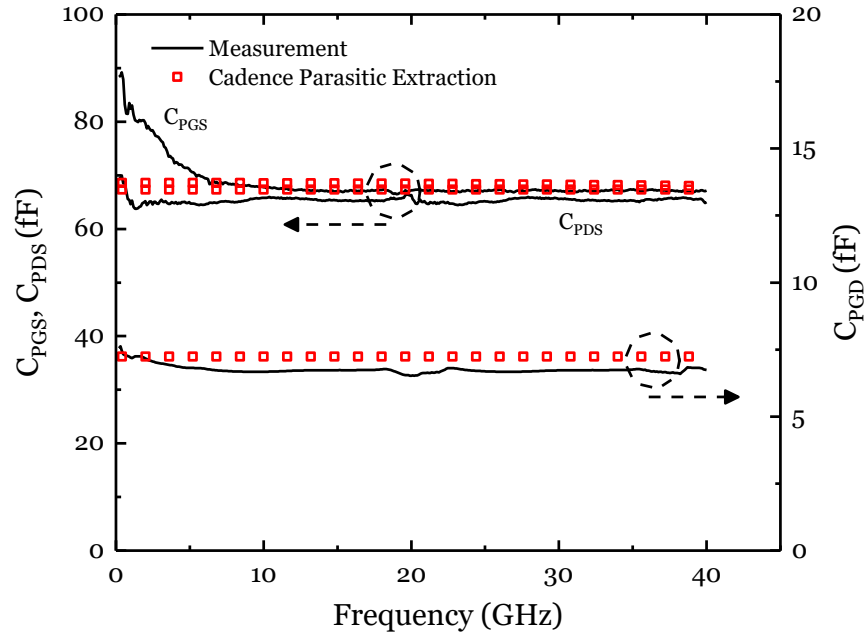
Fig. 4.21. Solid lines: calculated pad parasitic capacitances through reverse biased Cold-FET measurement. Symbols: calculated pad parasitic capacitances through Calibre PEX in Cadence.

The second and last step in the Cold-FET measurement is called the forward biased Cold-FET which allows the extraction of the series parasitic components in the equivalent circuit. If the DUT is assumed to be a simple three terminal transistor, it should be kept under the zero bias condition ($V_{DS}$ = 0) with the gate-source and gate-drain junctions forward biased. The gate is strongly forward biased to make the intrinsic capacitances negligible and reduce the channel impedance. As a result, the contribution of the channel's RC network can be ignored. With the transistor's drain and gate terminals being at the same potential, the drain-source voltage equals to zero and no current flows between the two and through the channel. But since the gate-source and the gate-drain junctions are forward biased, there will be a gate current flowing through each junction. The gate current values should be close if the drain and source access lengths are equal. Under the forward-biased Cold-FET biasing condition, the DUT in Figure 4.22 can be approximated with a short circuit. To create the forward biased Cold-FET biasing condition for the

cascode cell, $V_{G\text{-}MOSFET} = 1$ V, $V_{G\text{-}MESFET} = 0.8$ V, $V_{D\text{-}MESFET} = 0$ V was found to be the optimum biasing point for the forward Cold-FET measurement. The S-parameters of the forward biased cascode cell should be measured again under the mentioned forward biasing condition. The calculated pad and coupling parasitic capacitances should then be subtracted from the measured forward biased S-parameters, as shown in equations (4.13) – (4.16) which results in the simplified equivalent circuit of Figure 4.22.

With the parallel parasitic capacitance values in hand, they can be subtracted from the measured DUT Y-parameters, which are the admittance parameters of the measured DUT S-parameters of the forward biased Cold-FET. The parallel parasitic capacitance de-embedding is shown in equations (4.13) – (4.16).
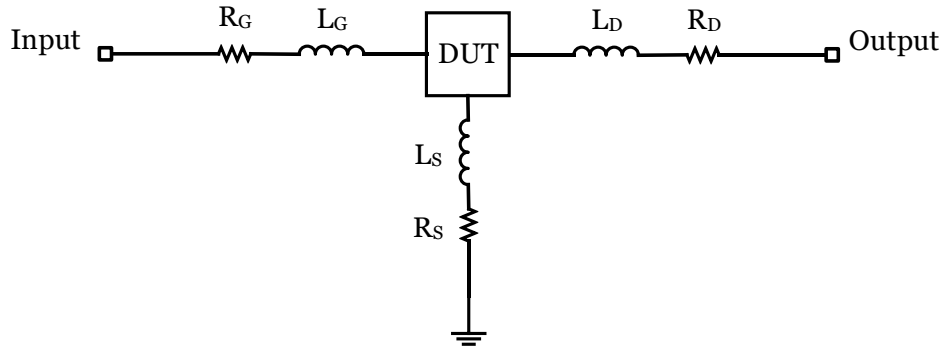


Fig. 4.22. Simplified Cold-FET two port equivalent circuit in Figure 4.15 after pad parasitic capacitances removal.

$$Y_{11}^{'} = Y_{11} - j\omega \left( C_{P\text{-}GS} + C_{P\text{-}GD} \right) \tag{4.13}$$

$$Y_{12}^{'} = Y_{12} + j\omega \, C_{P\text{-}GD} \tag{4.14}$$

$$Y_{21}^{'} = Y_{21} + j\omega \, C_{P\text{-}GD} \tag{4.15}$$

$$Y_{22}^{'} = Y_{22} - j\omega \left( C_{P\text{-}DS} + C_{P\text{-}GD} \right) \tag{4.16}$$

After removing the parasitic capacitances from the measured forward bias Cold-FET Y-parameters using equations (4.13) – (4.16) in ADS, the resultant admittance matrix should be converted to impedance parameters matrix [48], [83] for the rest of the calculations to find the series parasitic components. The impedance matrix elements are as follows:

$$Z_{11} = R_G + R_S + j\omega(L_G + L_S) \tag{4.17}$$

$$Z_{21} = Z_{12} = R_S + j\omega L_S \tag{4.18}$$

$$Z_{22} = R_D + R_S + j\omega(L_D + L_S) \tag{4.19}$$

The value of each of the series parasitic components shown in Figure 4.21 can be calculated through equations (4.20) – (4.25).

$$R_S = Re(Z_{12}) \tag{4.20}$$

$$R_G = Re(Z_{11}) - R_S \tag{4.21}$$

$$R_D = Re(Z_{22}) - R_S \tag{4.22}$$

$$L_S = \frac{Im(Z_{12})}{\omega} \tag{4.23}$$

$$L_D = \frac{Im(Z_{22})}{\omega} - L_S \tag{4.24}$$

$$L_G = \frac{Im(Z_{11})}{\omega} - L_S \tag{4.25}$$

Figure 4.23 presents the measured series parasitic resistance results of the forward biased Cold-FET measurement, along with the Calibre PEX simulated results in Cadence for a frequency range of 1 to 40 GHz. As in the parasitic capacitances measurement and

PEX results, an acceptable agreement is witnessed between the series parasitics measured and PEX results.
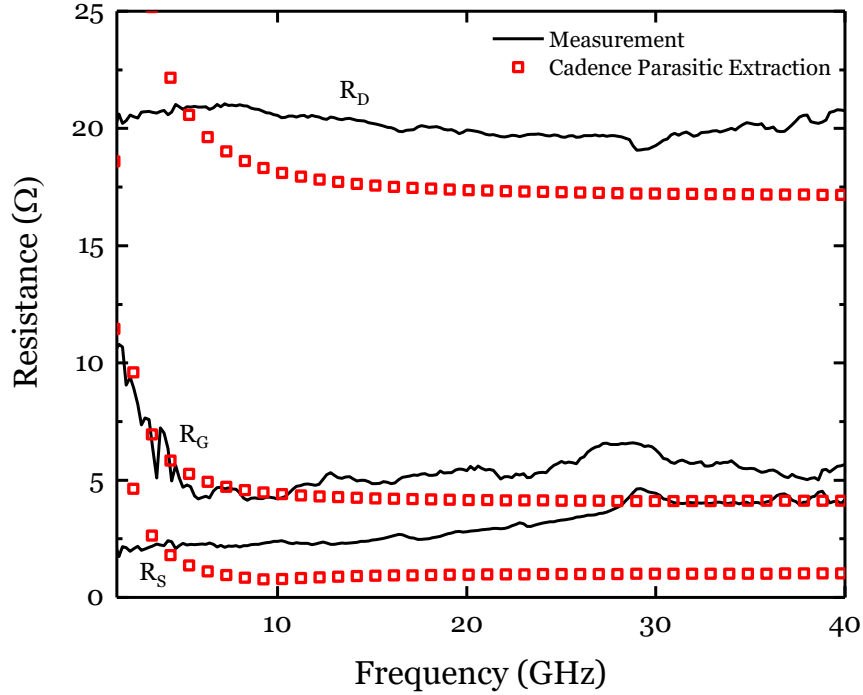


Fig. 4.23. Solid lines: calculated series parasitic resistances through forward biased Cold-FET measurement. Symbols: calculated series parasitic resistances through Calibre PEX in Cadence.

Since the GlobalFoundries 45RFSOI process design kit available to us at the moment this thesis is being transcribed does not support the self and coupling inductance extraction, simulated parasitic inductance plots could not be presented and the measured parasitic inductances in Figure 4.24 were used in the parasitics de-embedding process. The approximate values used in the cascode cell's parasitics de-embedding (Section 4.7) are given in Table 4.2.
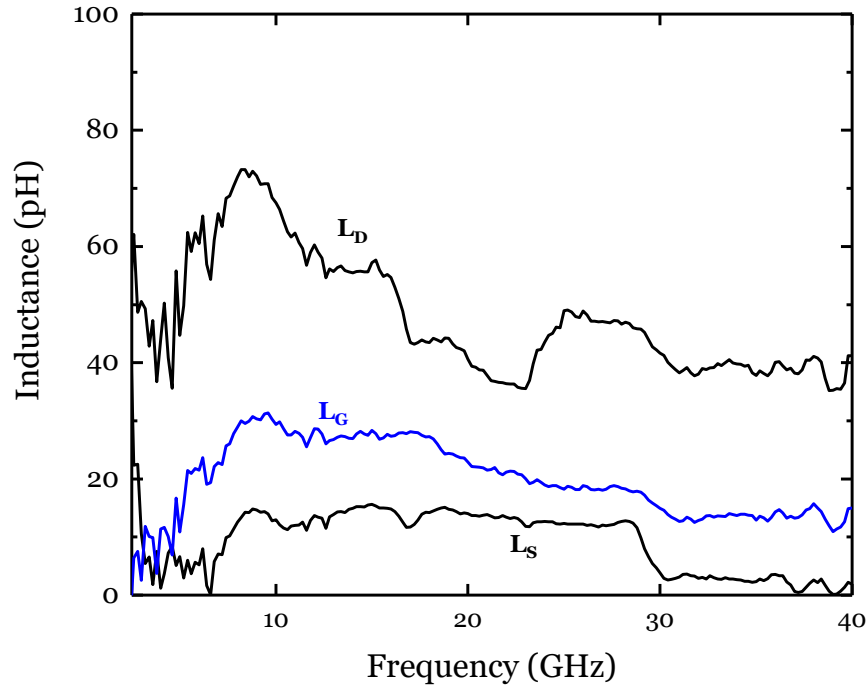
Fig. 4.24. Calculated series parasitic inductances through forward biased Cold-FET measurement.

Table 4.2. CASCODE AMPLIFIER SERIES PARASITIC
RESISTANCE AND INDUCTANCE VALUES

| | |
|---|---|
| $R_G$ | ~ 4 $\Omega$ |
| $R_D$ | ~ 17 $\Omega$ |
| $R_S$ | ~ 0.8 $\Omega$ |
| $L_G$ | ~ 20 pH |
| $L_D$ | ~ 50 pH |
| $L_S$ | ~ 10 pH |

4.7.    Cascode RF De-embedded Results

As explained in Section 4.6, de-embedding the layout parasitics from the measured

DUT S-parameters is essential to evaluate the true performance of the cascode amplifier.

Once all the parasitic component values are calculated, the cascode amplifier can be biased

at an optimum DC biasing point for small signal S-parameter measurement. Then all the parasitics can be de-embedded from the measured DUT S-parameters using the presented equations in Section 4.6. Another more convenient and faster solution for de-embedding is using the ADS de-embed component. As figure 4.25 shows, the ADS de-embed component negates the defined circuit to nullify its corresponding effects.
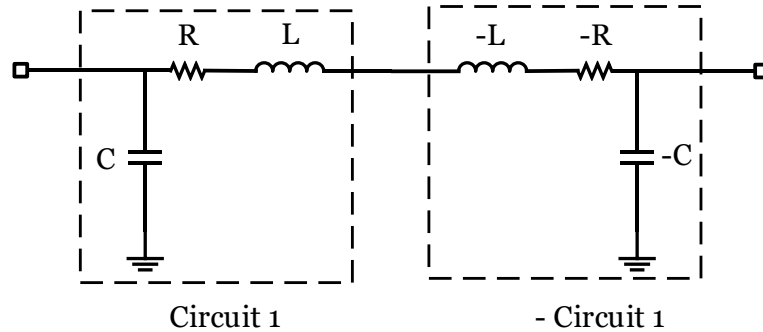


Fig. 4.25. Keysight ADS de-embed component usage.

To reduce the parasitic de-embedding time, the measured DUT S-parameters (extrinsic S-parameters) can be imported into ADS and one individual de-embed component can be utilized at the cascode cell RF input (MOSFET gate), MOSFET source, RF output (MESFET drain), and between the input and output ports. As Figure 4.26 illustrates, each of the de-embed components contain the related portion of the parasitic components, and they form an architecture similar to Figure 4.15. After running the S-parameter analysis in ADS, the de-embed components cancel out the effect of the corresponding parasitics, and the intrinsic S-parameters matrix will be achieved which can be used to study the actual performance of the cascode amplifier. The component values inside each of the de-embed components are calculated as explained in Section 4.6.
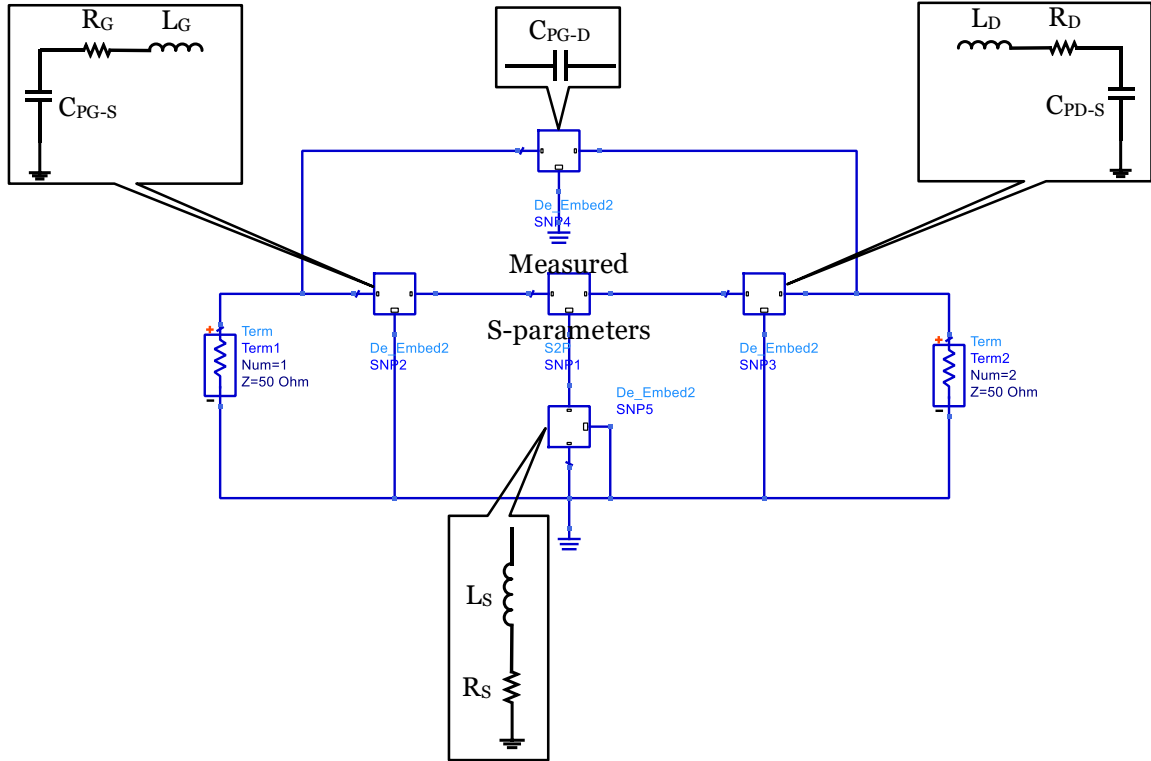
Fig. 4.26. Cascode cell parasitics de-embedding schematic in ADS.

A comparison between the measured extrinsic and intrinsic cascode amplifier performance is shown in Figure 4.27. In this figure, the forward current gain ($h_{21}$) is calculated though equation (4.26) using the extrinsic (measured) and intrinsic (de-embedded parasitics) S-parameters. The DUT is a cascode amplifier with a total width ratio of $\frac{W_{MOSFET}}{W_{MESFET}} = \frac{30\ \mu m}{300\ \mu m}$ between the two transistors, with the MOSFET $L_G = 112$ nm.

$$h_{21} = \frac{-2\ S_{21}}{[(1 - S_{11})(1 + S_{22})] \times (S_{12}\ S_{21})} \qquad (4.26)$$
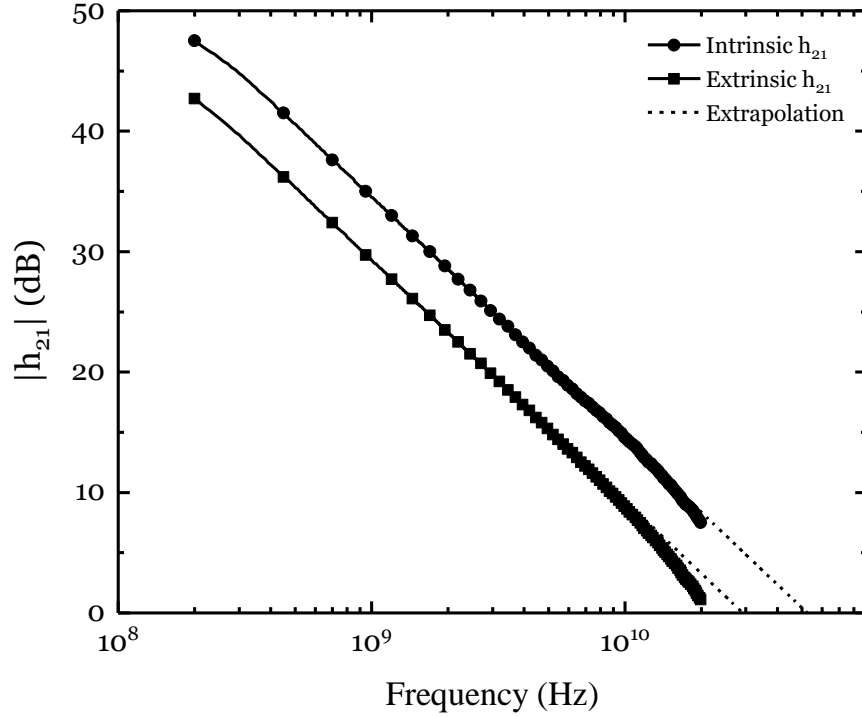
Fig. 4.27. Comparison between the intrinsic and extrinsic h21 for a cascode cell with $L_{G\text{-}MOSFET}$ = 112 nm. The dashed line is a fit to a -20 dB/decade slope indicating an intrinsic $f_T$ = 50 GHz. ($V_{DD}$ = 6 V, $V_{G\text{-}MOS}$ = 0.7 V, $V_{G\text{-}MES}$ = 0.8 V).

To verify the accuracy of the Cold-FET measurement and the parasitics de-embedding method described above, the final intrinsic figures of merit such as the cascode amplifier's $f_T$ and $f_{max}$ which are derived from the intrinsic S-parameters can be compared to the Cadence simulation results utilizing the 4-terminal Angelov MESFET model presented in Section 2.4, and the foundry MOSFET model. The accuracy of the DC simulation results using these models versus the DC measurements were already shown in Figures 4.10 and 4.11. The Cadence schematic should be similar to Figure 4.4 without any extra parasitic components connected to the cascode amplifier's terminals to replicate the expected intrinsic S-parameters of the amplifier. To study the RF performance dependence of the cascode amplifier on the MOSFET transistor gate length, three separate amplifiers are studied and reported in this section which are enlisted in Table 4.3.

Table 4.3. CHARACTERISTICS OF THE COMPARED MESFET AND CASCODE AMPLIFIERS

| Type | $L_{aD\text{-}MES} = L_{aS\text{-}MES}$ $= L_{aG\text{-}MES}$ (nm) | $W_{MES}$ (µm) | $L_{G\text{-}MOS}$ (nm) | $W_{MOS}$ (µm) |
|---|---|---|---|---|
| Stand-alone MESFET | 200 | 300 | NA | - |
| MOSFET-MESFET cascode | 200 | 300 | 112 | 30 |
| MOSFET-MESFET cascode | 200 | 200 | 40 | 20 |

The forward current gain, $h_{21}$, is expected to be higher for the cascodes than the CS MESFET. As equation (4.27) states, the $f_T$ of a MOSFET transistor is inversely proportional to the square root of its gate length. As explained before, the $f_T$ of the cascode amplifier is also dominated by the input transistor which is the MOSFET. So it is expected to observe an increasing cascode amplifier $f_T$ as the $L_{G\text{-}MOSFET}$ gets shorter. As Figure 4.28 shows, $h_{21}$ increases as the CS MOSFET gate length is reduced from 112 nm to 40 nm. Below 20 GHz the measured $h_{21}$ data show the expected -20 dB/decade slope which extrapolates (dashed lines) to give cut-off frequencies, $f_T$, of 31, 47, and 95 GHz for the MESFET, 112 nm and 40 nm cascodes respectively. However, for the cascode cells, $h_{21}$ falls faster than -20 dB/decade above 20 GHz, behavior that is reproduced by the simulations. From the simulated $h_{21}$, the $f_T$ of the CS MESFET, 112 nm and 40 nm cascodes are 33, 45, and 70 GHz respectively.

$$f_T = \frac{gm}{2\pi(C_{gs} + C_{gd})} \tag{4.27}$$
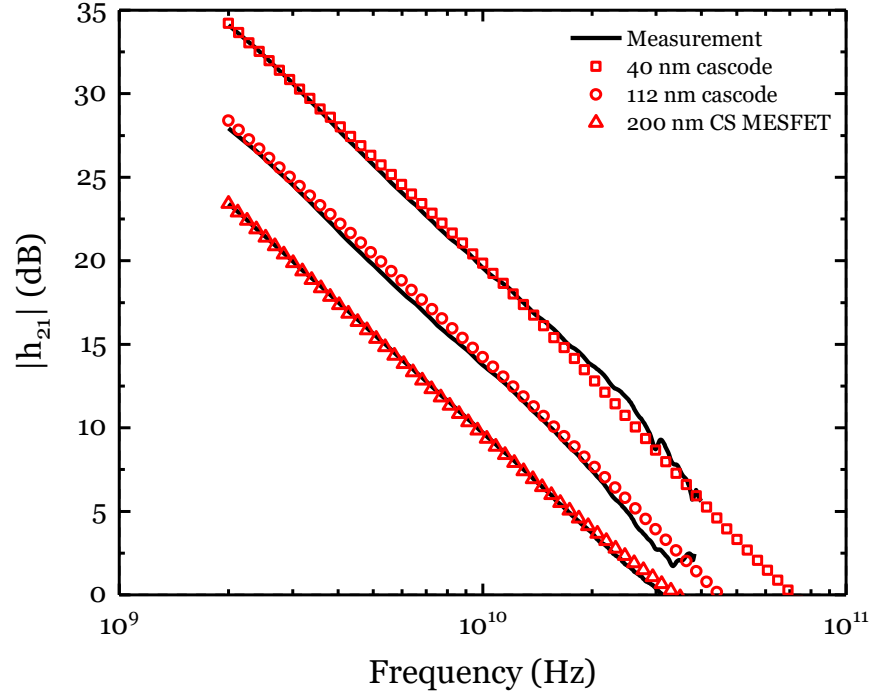
Fig. 4.28. The measured (solid lines) and simulated (symbols) forward current gain (*h21*) of the CS MESFET and cascode cells. The CS MESFET is biased with $V_G$ = 0.1 V, and $V_{DD}$ = 4 V. For the cascodes $V_{DD}$ = 6 V, $V_{G\text{-}MOS}$ = 0.7 V, $V_{G\text{-}MES}$ = 0.8 V.

Based on equation (3.2), $f_{max}$ is also proportional to $f_T$ and it's expected to see an increasing $f_{max}$ trend as the cascode MOSFET $L_G$ gets shorter. To find $f_{max}$, MAG of the MESFET and cascode amplifiers were calculated and plotted using the measured intrinsic S-Parameters, which are illustrated in Figure 4.29. The simulated MAG reproduces the measured CS MESFET data well and clearly shows the transition at 9.5 GHz from maximum stable gain, falling with a slope of -10 dB/decade, to stable MAG with a slope of -20 dB/decade. For the cascodes, the model also captures the stable to unstable transition but differs from the measured data by 1-2 dB. We attribute this difference to additional parasitics from the layout connecting the multi-finger MOSFET and MESFET that are not captured by the model and PEX extraction. Above the stable transition, the MAG of the cascodes falls off faster than -20 dB/decade, and when extrapolated (dashed lines) the

values of $f_{max}$ are lower than those from the simulations. The values of the extrapolated and simulated $f_T$ and $f_{max}$ are given in Table 4.4.

Table 4.4. SUMMARY OF THE CASCODE AMPLIFIERS RF PERFORMANCE

|  | $f_T / f_{max}$ (GHz) | | |
|---|---|---|---|
|  | measured | extrapolated | model |
| CS MESFET | 31 / 29 | 31 / 31 | 33 / 29 |
| 112 nm cascode | N/A | 47 / 55 | 45 / 69 |
| 40 nm cascode | N/A | 95 / 68 | 70 / 95 |
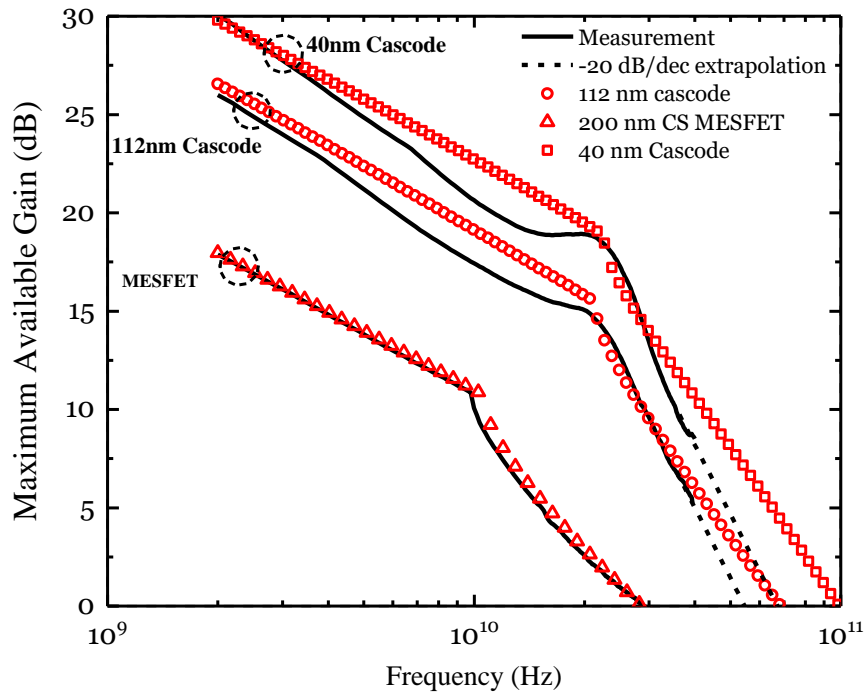


Fig. 4.29. The measured (solid lines) and simulated (symbols) maximum available gain of the CS MESFET and cascode cells. The biasing conditions are the same as Figure 4.28.

As reported in Table 4.4, $f_T$ and $f_{max}$ of the presented cascode amplifiers make them an appropriate choice for 5G and K-band amplifiers. Thanks to the MESFET's higher $V_{BD}$ in comparison to the conventional MOSFETs, these cascode cells are expected to generate a higher output power in comparison to the MOSFET-only amplifiers with a comparable size in the CMOS technology. To provide an insight regarding the superior performance of the discussed cascode amplifiers with respect to similar CMOS amplifiers, Table 4.5 provides a short comparison.

Table 4.5. PERFORMANCE COMPARISON OF $K$-BAND STACKED AMPLIFIERS

| Cascode architecture | f (GHz) | gain (dB) | $V_{DD}$ (V) | Technology |
|---|---|---|---|---|
| 2-stack NFET [84] | 24 | 14 | 2.4 | 90nm bulk CMOS |
| 3-stack NFET [34] | 24 | 13 | 2.9 | 45nm SOI CMOS |
| 2-stack SiGe HBT [85] | 24 | 10 | 5.1 | 120nm SiGe BiCMOS |
| 2-stack NFET-MESFET [this work] | 24 | 18 | 6 | 45nm SOI CMOS |

## 4.8. Summary and Discussion

Measurements and simulations of the first integrated n-channel MOSFET-MESFET cascode amplifiers demonstrated > 15 dB of gain at $K$-band frequencies (18 – 27 GHz) using a 45 nm SOI CMOS technology. The cascode architecture combined the enhanced voltage operation of the MESFET with the high frequency capability of the scaled MOSFET. The resulting small-signal amplifiers demonstrated a maximum $f_T$ = 70 GHz when operated with supply voltages of 4 V. The 4-terminal Verilog-A Angelov MESFET model introduced in Chapter 2 was used for simulations, along with the foundry's native MOSFET models. Compared to a single MESFET amplifier design the cascode showed the expected increase in breakdown voltage, gain, bandwidth and reverse isolation.

CHAPTER 5

SCALED UP MOSFET-MESFET POWER AMPLIFIERS

Small signal cascode amplifiers discussed in Chapter 4 were scaled up with the goal of constructing power amplifiers (PA) that deliver the calculated gain (G) and output power ($P_{out}$). A two-layer FR-4 printed circuit board (PCB) was designed for DC and RF measurements of the initial PA design. On account of the fact that the bondwires on the PCB degraded the operating frequency and the output power of the PA, a design with ground-signal-ground (GSG) input and output pads was presented to enable on-chip measurements. The on-chip measurements of the optimized PA design showed a maximum saturated power ($P_{sat}$) of 20.4 dBm, maximum gain of 19.1 dB, and maximum power added efficiency (PAE) of 52.6% while operating at 5 GHz. To further improve the design, an on-chip input matching network was then embedded in the design to decrease the input return loss and improve the maximum $P_{sat}$ and efficiency.

5.1.    Cascode Power Amplifier Initial Design

The first MOSFET-MESFET cascode PA was designed in GlobalFoundries 45 nm 12SOI process. The small signal amplifiers discussed in Chapter 4 were not available and characterized at time of submitting the PA design to the foundry for fabrication. As a result, the initial PA was mostly developed based on the performance of the individual transistors characterized prior to the tape-out. A common source MESFET PA similar to the one presented in [37] was chosen as the design starting point, as it delivered outstanding voltage handling capability and output power level. The MESFET employed in [37], however, has a source and drain access length of 1000 nm. To improve the frequency response of the MESFET while retaining the high voltage operation, $L_{aS}$ was reduced to 200 nm and $L_{aD}$ was kept at 1000 nm. This helps reduce the parasitic resistance

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at the gate-source junction to achieve higher speed. The gate-drain junction which tolerates the output voltage swing also tolerates a less intense electric field due to the longer drain access length, and higher supply voltage can be applied to the transistor due to the increased breakdown voltage.

Based on the simulation results using the available models, a transistor width ratio of 23 between the MESFET with $L_G = L_{aS}$ = 200 nm, $L_{aD}$ = 1000 nm and a minimum gate length body-contacted MOSFET with $L_G$ = 56 nm estimated a similar DC performance for either of the transistors. This transistor width ratio was then proven to be excessively large after characterizing the small signal amplifiers, as indicated by the results presented in Chapter 4.

To build the wide input MOSFET, 40 smaller NFET cells were connected in parallel. The distance between the NFET cells were reduced as much as allowed by the PDK design rules. Likewise, the gates polysilicon pitch, and the gates polysilicon strap extensions were minimized to reduce the associated parasitics. Top copper metal layers with lower sheet resistance, as well as a high density of metal vias between them were used for routing to minimize the parasitics introduced by the interconnects.

After connecting the input MOSFET drain to the common gate MESFET source, the area underneath the MESFET drain pads was used to connect a large AC ground capacitor to the MESFET gate. Thick oxide NMOS varactors (dgncap) which were accessible in the 12SOI PDK were manually sized and connected in parallel to construct an 800 pF capacitor without violating the maximum density design rules. Using a metal-insulator-metal (MIM) capacitor would have been more convenient if available, as the varactor's capacitance is dependent on the voltage across that and changes about 56% in value based on the foundry model. However, since the resulting AC ground capacitor value

was very large considering the aimed operating frequency, the capacitance variations with voltage was not expected to impair the design. As this design was intended to be wire bonded on a PCB board and characterized by small signal and load pull measurements, no on-chip impedance transform matching network was designed at this design stage. The layout of the initial cascode PA is shown in Figure 5.1.
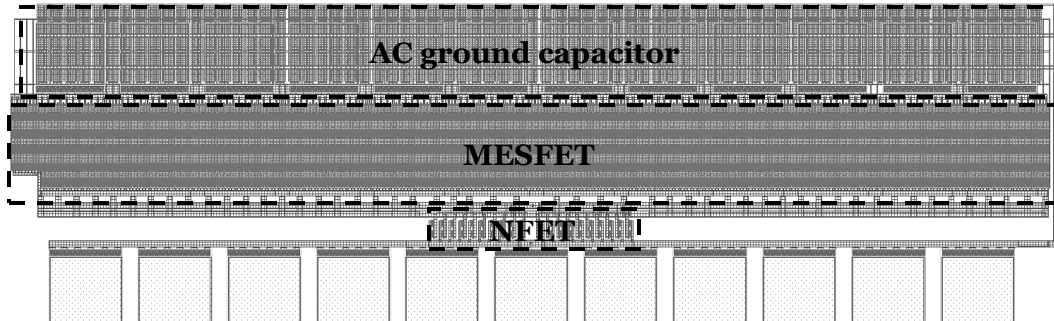


Fig. 5.1. Initial PA design comprising a 1.8 mm MOSFET and 41 mm MESFET.

A two layer PCB made of FR-4 material with a thickness of 31 mil (787.4 µm) was designed in ADS Momentum for measurement purposes. The board comprised of a bottom ground layer and a top conductive (2 oz. copper, thickness = 71.12 µm) layer to form the transmission lines and the ground planes. The die pads and bondwire pads were made of gold. Vertical copper vias connected the top layer to the ground where needed.

Figure 5.2 shows the mounted die on the PCB, with the gold die stand in the middle. 3 separate 50 Ohm tracks were designed to provide the required DC voltages for $V_{G\text{-}MOSFET}$, $V_{G\text{-}MESFET}$ and $V_{DD}$. DC supplies were directly fed on the board through pigtail connectors soldered to the DC paths. Sufficient space area was predicted between the DC tracks and their adjacent ground planes to accommodate DC decoupling capacitors in order to suppress the supply voltage noise. Four surface mount decoupling capacitors of 10 pF, 100 pF, 1 nF and 100 nF were soldered on the DC feed lines to reject the low frequency supply noise. The input and output RF tracks were 50 Ohm transmission lines. The RF paths were

connected to standard SMA connectors. To prevent RF signal leakage into the DC paths, two Coilcraft surface mount 47 nH inductors with a self-resonance frequency of 2.2 GHz were used as RF chokes. Considering the expected DC current levels presented in Figures 5.1 and 5.2, the RF chokes need to conduct a quiescent current as large as 500 mA. High input RF signal levels will swing the total current to the Ampere range. A high inductance value is of the interest for the RF choke to introduce high impedance to the RF signal and prevent signal leakage to the DC feeding lines. The self-resonant frequency of high inductance, high current surface mount RF chokes are usually low, restricted to 2.2 GHz in this case which introduces an upper bound for the operating frequency of the PA. The conventional method to block the AC signal at higher frequencies is designing an on-chip quarter wavelength stub [86].
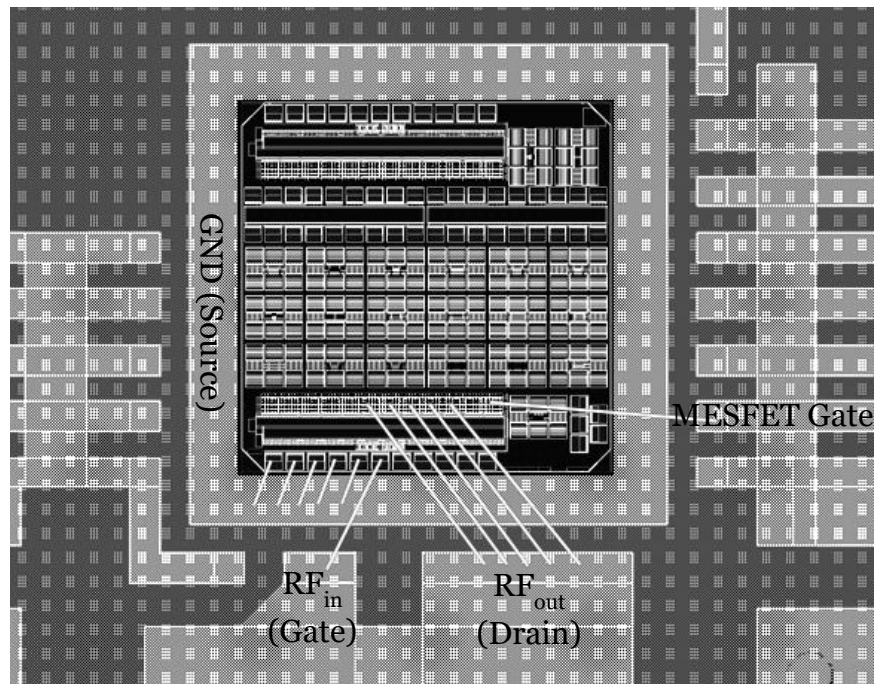


Fig. 5.2. Cascode PA wire bonded on the PCB.

The die was mounted on the board with epoxy, and aluminum bondwires connected the die pads to the gold straps on the PCB. Each bondwire introduces undesired

parasitic inductance which is approximately 1 nH/mm as a rule of thumb. To minimize source degeneration, the number of bondwires connected to the MOSFET source should be increased to as many as possible to reduce the total inductance of the bondwires. As Figure 5.2 shows, a total number of 5 bondwires could be fitted on the board for each of the source and drain terminals.

DC measurement results of the PA presented a breakdown voltage of approximately 15 V on the 1 V technology node. However, the small input NFET could not keep up with the DC performance of the large MESFET and needed a high $V_{GS}$. Layout parasitic resistances associated with the metal interconnects can greatly decrease the current drive capability of the MOSFET as well. Consequently, the MOSFET cannot provide the DC current required by the large sized MESFET and its transconductance is reduced. The saturation of the input device causes the clipping of the RF voltage and increases the PA nonlinearity. The MOSFET being incapable of providing a large current swing, the large signal gain of the amplifier is degraded. Based on the power sweep results, the PA was highly nonlinear which leaded to spectral regrowth and adjacent channel interference (ACI) which corrupts data. Adjacent channel suppression is nominally on the order of 70 dB or higher [87] which is difficult to achieve.

Numerous MESFET fingers and a high multiplicity needed to build the 41 mm wide MESFET, on the other hand, lowers the output impedance ($Z_{out}$) of the transistor. Low $Z_{out}$ which in this PA is far away from the 50 Ω characteristic impedance of the transmission line connected to the MESFET drain, produces a large output current and makes the PA sensitive to parasitic resistances. Sensitivity to parasitics ensues from the fact that there will be a large power loss originated from the parasitic resistances at high DC current levels ($P = R_{parasitic} \times I^2$).

The source degeneration introduced by the wire bonds connecting the source of the MOSFET to the PCB ground plane has a detrimental effect on the PA gain as well. At the PA's frequency of operation, the impedance corresponding to each of the 5 wire bonds attached to the MOSFET source is approximately j10 to j15 Ohms (1 to 1.5 nH), considering their length. Ignoring the pad parasitic capacitance and metal interconnect parasitic resistances between the two adjacent bond wires, they can be assumed to be in parallel with each other. Thus, the total parasitic impedance at the MOSFET source is approximately j3 Ohms. The voltage drop across the parasitic source degeneration inductance can be calculated from Equation 5.1:

$$V_s = X_L \times i = 2\pi f. \, L \times i \tag{5.1}$$

So a source degeneration of j3 Ohms at f = 1.5 GHz and under an AC current swing of 100 mA consumes 2.83 V of the voltage swing due to the voltage drop across itself. This is another reason for the gain and linearity degradation of the PA.

## 5.2. Optimized Cascode Power Amplifier Design

In order to optimize the PA design and mitigate the source degeneration, a probe-able design inside a ground-signal-ground (GSG) cage with updated transistor width ratio was presented. Direct on-chip measurements obviated the need to wirebond the die onto a PCB and the resulting source degeneration effects and performance restrictions. An input NFET PCell with $L_G$ = 40 nm was designed by Dr. Chaojiang Li of GlobalFoundires with optimized layout to minimize the parasitic resistances and capacitances and enhance the RF performance and $f_T$ of the transistor. The MESFET layout was also transferred to GlobalFoundries 45RFSOI technology node.

### 5.2.1. MESFET PCell in 45RF SOI Technology

Before optimizing the PA, the parameterized cell (PCell) of the MESFET needed to be updated in Cadence Layout Editor environment since the 45 nm 12SOI technology (which had been the technology node for the designs presented in this dissertation) was not supported by GlobalFoundries anymore. The back-end-of-line (BEOL) was migrated to a new metallization layer called 45RF SOI technology, to further enhance the performance of the circuit components. Since the CMOS SOI MESFET is a custom-made transistor which is not part of the process design kit (PDK), technology variations do not reflect in its model and layout automatically. The most important changes that influenced the PA design were: 1) Elimination of 3 copper metal layers, and the replacement of the topmost copper metal layer with a wider aluminum metal layer. The total number of available metal layers were reduced to 8 from 11 as a result. 2) Metal-insulator-metal (MIM) capacitors were made available, which enabled designing high density, compact and voltage independent capacitors.

The MESFET PCell layout was updated to remove the eliminated metal layers and replace them with the new layers. The new MESFET layout needed to be compliant with the new design rules as well, to pass the design rule check (DRC). After making the adjustments, a new PA targeted to deliver a saturated output power of >20 dBm at 5 GHz was designed as will be explained.

### 5.2.2. NFET Layout Optimization

The layout of the NFET was another improvement which was represented in the new design to diminish the performance deterioration due to parasitics. The Pcell designed and made available by Dr. Chaojiang Li of GlobalFoundries [34], [88] was

modified to construct the 280 μm wide input transistor. Multi-finger NFET structure allowed reducing the width of each finger and the gate parasitic resistance associated with each finger. Based on Equation 3.2, a lower transistor gate resistance improves $f_{max}$, as the two parameters are inversely proportional. The increased number of gate fingers is a disadvantage of multi-finger transistors which causes increased transistor aspect ratio and higher gate parasitic capacitances which both increase with number of fingers. This technology offers regular and relaxed gate polysilicon pitch options, with the gate pitch in the relaxed option being twice as large as the regular option. The relaxed pitch option was chosen over the regular pitch as it provides higher transconductance and $f_T$ [90]. Two dummy polysilicon strips were placed on each side of the NFET cell to prevent the outermost fingers being over-etched and cause mismatch between the inner and outer gate fingers [91]. Double-sided gate polysilicon contacts were connected to each side of the gate fingers in the NFET cells to minimize the gate series parasitic resistance. Each polysilicon strap had two columns of minimum spaced gate contacts, as close to one another as allowed by the design rules. The gate contacts connect the gate polysilicon to the first copper metal layer (M1) for further routing. Two U-shaped M1 interconnects at the top and bottom of the NFET cell link the left and right polysilicon straps.

The sources and drain contacts of each cell were connected to higher level copper metal layers (C1 and UA) through M1 to OA via stacks. C1 and OA copper interconnects tie the source and drain contacts of adjacent NFETs. Using higher level metal layers with lower sheet resistance for routing reduces the parasitic capacitances of source and drain terminals to improve the transistor's gain and speed. Figure 5.3 illustrates two connected adjacent NFET cells. The NFET cells can be expanded in symmetric arrays to attain the targeted NFET width.
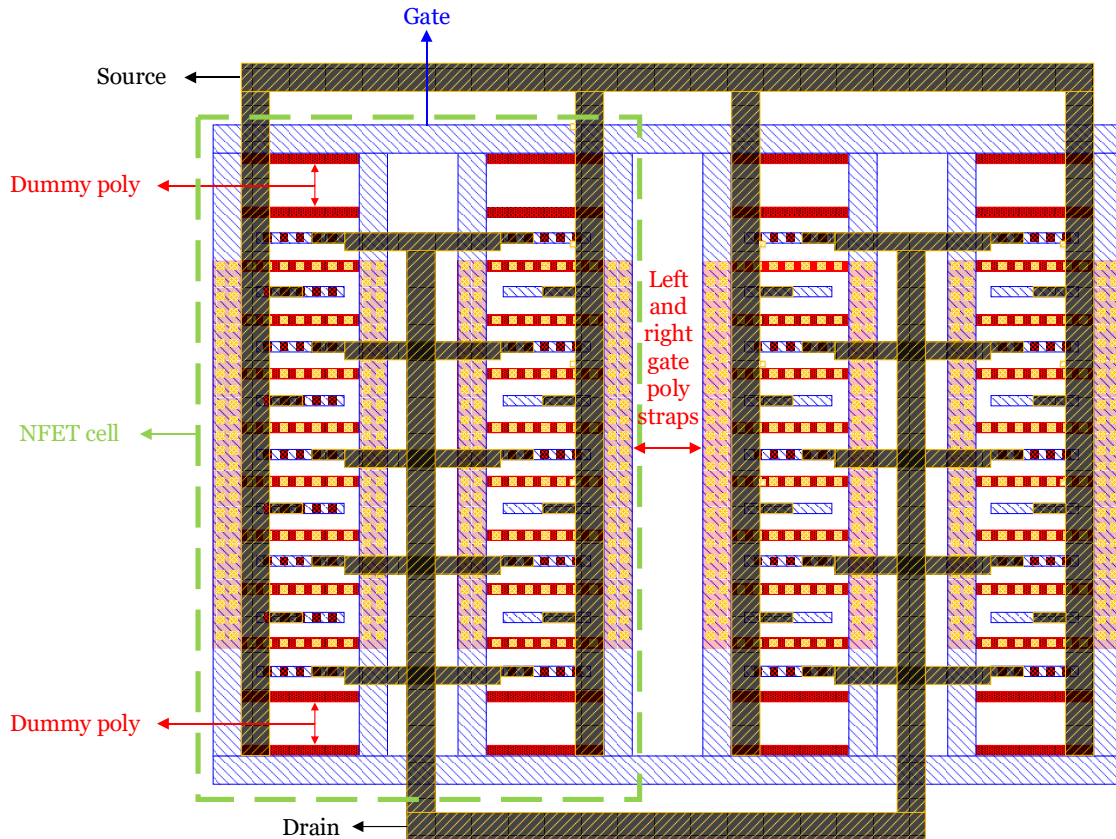
Fig. 5.3. Optimized NFET layout.

### 5.2.3. Transistors Width Ratio

As understood from Section 5.1, the width ratio between the two transistors in the PA needed to be reduced. The target quiescent current of the PA was ~ 280 mA. The $L_G$ = 40 nm NFETs in the 45RF SOI technology generate approximately 1 mA/μm of current when biased in the middle region of the FOC. In the new design, a $L_G$ = 40 nm NFET with a total width of 280 μm was selected as the input transistor to generate up to 280 mA of quiescent current, which can support an almost equal amount of AC current swing. DC measurements of a MESFET with $L_G$ = 200 nm suggested a total width of ~ 1.5 mm to keep abreast with the 280 μm wide NFET DC results. The MESFET is 5.4 times wider than the NFET in the new design. It should be noted that the MESFET to NFET width ratio of 10

which was suggested in Chapter 4 was an approximation related to small signal amplifiers on the 45 nm 12SOI technology node. The PA utilizing the new 45RF transistor layouts worked best with the updated width ratio. The layout of the optimized cascode PA is shown in Figure 5.4.
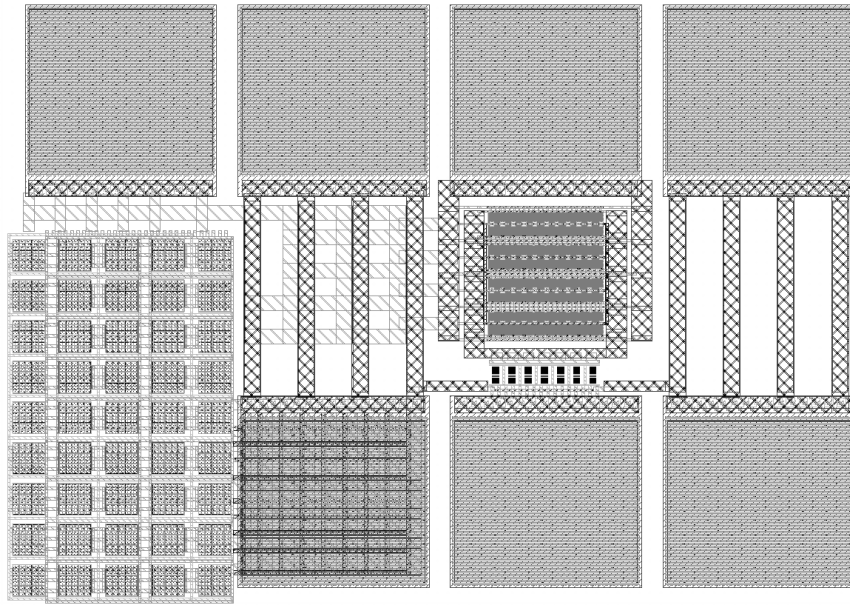


Fig. 5.4. Layout of the optimized MOSFET-MESFET cascode PA

### 5.3. Optimized Cascode Power Amplifier Characterization

### 5.3.1. DC Measurements

A setup similar to Figure 4.6 was used for DC measurements to determine the DC performance of the PA and find an optimum quiescent point. The MOSFET being an enhancement mode device and the MESFET being a depletion mode device, the turn-on sequence should be to err on the side of caution to prevent any damage to the transistors. The MESFET is a normally on device and owing to its large gate width, starts to conduct large amounts of current with small drain voltages. This large current flows into the MOSFET drain and will lead to damage if the MOSFET is in the off state or triode region. Specifically, the MOSFET gate is very sensitive and its gate voltage and current should be constantly monitored. It can intuitively be understood that the MOSFET should be turned on before the common gate MESFET to create a conducting path to the ground. By applying a gate voltage greater than the MOSFET threshold voltage ($\sim$ 0.2 V) to its gate, the generated current can flow through the normally on MESFET. It is important to increase the voltage applied to each terminal gradually and let the currents settle before increasing the voltages any further. From another point of view, any instability can create a positive feedback and may lead to instantaneous and unbounded current swing. A source of positive feedback is the large parasitic $C_{gd}$ of the wide transistors, and the parasitic coupling capacitance between the input and output pads (referred to as $C_{PG-D}$ in Chapter 4). The following steps were followed as the turn on and turn off protocols:

- Connecting the input and output RF probes
- Connecting the MESFET gate to ground. Since the supply voltage ($V_{DD}$) is not yet applied, no current should flow at this step.

- Connecting the MOSFET gate to ground, and gradually ramping $V_{G\text{-}MOSFET}$ slightly over the threshold voltage (e.g. 0.4 V) to create a current conduction path to ground through the MOSFET channel.

- Applying the supply voltage to MESFET drain. Since the MESFET is a depletion mode device and its gate is already connected to ground (0 V), it turns on.

- Slowly increasing $V_{G\text{-}MOSFET}$, $V_{G\text{-}MESFET}$ and $V_{DD}$ to the value of interest.

The MESFET gate voltage should be kept lower than its drain so as not to forward bias the gate-drain junction diode. It's important to set proper current compliance levels for each current path to restrict the current flow. Due to the large size of the transistors, voltage increment should be in small steps to avoid sudden current rise. To turn the PA off, the turn on steps are reversed.

Measurement equipment current compliance is another parameter needed to be considered while setting up the DC measurements. Figure 5.5 depicts the measured FOC of the PA up to $V_{DD}$ = 6 V with a 0.1 W power limitation in which the MOSFET and MESFET gate voltages were raised as high as 0.9 V and 0.6 V respectively. The supply and biasing voltages were not increased any further so as not to expose the PA to high quiescent.
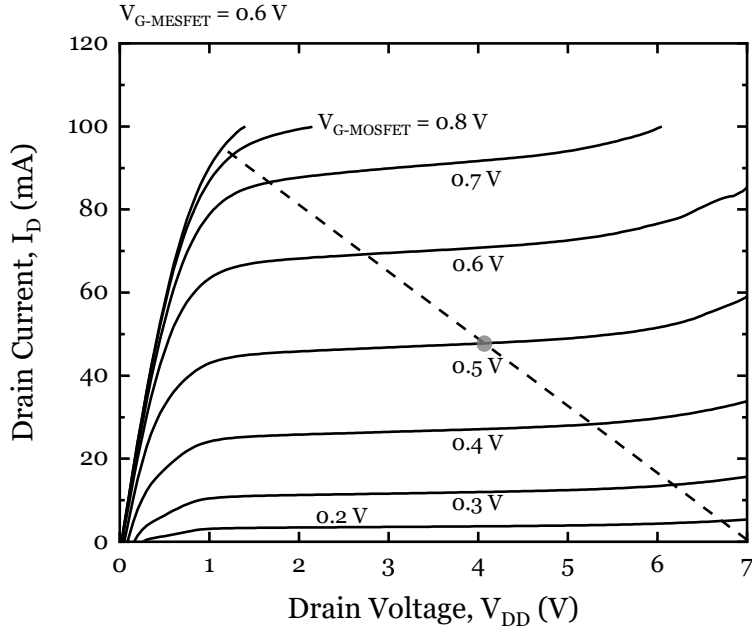
Fig. 5.5. The 0.28 mm-1.1 mm MOSFET-MESFET power amplifier FOC with a 0.1 W power limitation.

It is worth mentioning again that the drain voltage of the MOSFET is set by the MESFET gate-source voltage. It can be understood from Figure 2.10 that the maximum transconductance of the MESFET is achieved when its gate-source voltage is in the 0 V to 0.2 V range. So biasing the MESFET in this region will provide a ~ 0.8 V maximum quiescent voltage on the MOSFET drain when $V_{G-MESFET}$ = 0.6 V.

### 5.3.2.  Cascode Power Amplifier S-parameters Measurements

The next step after confirming the functionality of the PA is the small signal S-parameter measurements to find the return losses and the stable region of operation of the PA. The power loss of the setup including the RF cables and probes should be removed to find the intrinsic S-parameters of the PA. An HP 8753D network analyzer was used for the small signal measurements with an upper frequency limit of 6GHz. The S-parameters were measured from 4 GHz to 6 GHz with $V_{G-NFET}$ = 0.5 V, $V_{G-MES}$ = 1 V and $V_{DD}$ = 4 V which

is presented in Figure 5.6. The reverse isolation ($S_{12}$) maintains lower than approximately -40 dB in the measured bandwidth, asserting the advantage of the cascode architecture in presenting an improved $S_{12}$. The forward gain ($S_{21}$) remains above 20 dB, which is the herald of an auspicious small signal gain. The low input and output return losses ($S_{11}$, $S_{22}$) at in the measured frequency bandwidth however are a sign of poor input and output matching which necessitates the use of input and output matching networks for optimum power transfer.
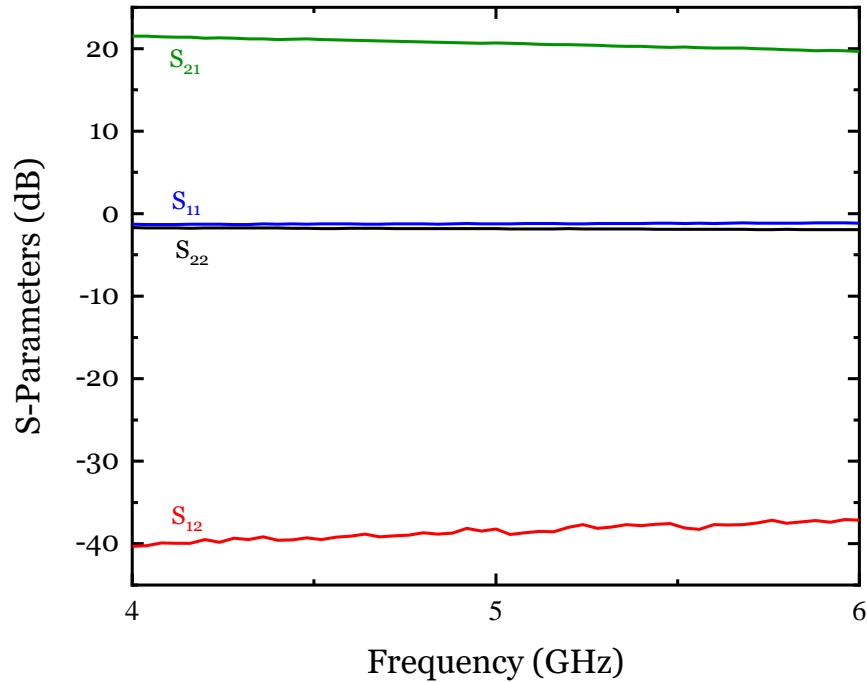


Fig. 5.6. Measured S-parameters of the cascode PA for $V_{G\text{-}NFET}$ = 0.5 V, $V_{G\text{-}MES}$ = 1 V and $V_{DD}$ = 4 V.

$S_{11}$ and $S_{22}$ have comparable values which get as low as approximately -3 dB at 5 GHz. The input and output reflection coefficients calculated through equation 5.2 give a high value of 0.71, which should be 0 in case of ideal matching to 50 Ω.

$$\Gamma = 10^{\left(\frac{-\text{ Return loss}}{20}\right)} \tag{5.2}$$

Consequently, the voltage standing wave ratio (VSWR) of the PA is high as well and equals to 5.9, calculated through Equation 5.3.

$$\text{VSWR} = \frac{1+ |\Gamma|}{1- |\Gamma|} \tag{5.3}$$

A ramification of this high VSWR value is a 50.4% reflected power, 49.6% through power and 3.05 dB mismatch loss (Equations 5.4 to 5.6) which restricts the output saturated power ($P_{sat}$), output 1-dB compression point ($OP_{1dB}$) and power efficiency ($\eta$) of the PA. High return loss urges the need for an on-chip matching network to transform the impedance which will be discussed in Section 5.4.

$$\text{Reflected power (\%)} = 100 \times \Gamma^{2} \tag{5.4}$$

$$\text{Through power (\%)} = 100 \times \left(1\text{-}\Gamma^{2}\right) \tag{5.5}$$

$$\text{Mismatch loss (dB)} = 10 \log\left(1\text{-}\Gamma^{2}\right) \tag{5.6}$$

From another perspective, the input and output impedances ($Z_{in}$, $Z_{out}$) of the PA calculated from the measured S-parameters are presented in Figure 5.7. While the real part of $Z_{in}$ and $Z_{out}$ are approximately 25 Ω, the plot reveals they are highly capacitive at the frequency of operation. This fact is reflected in the high measured input and output return loss values. An on-chip impedance transform network can help cancel out the imaginary part and increase the real part to make the input and output impedances closer to 50 Ω.
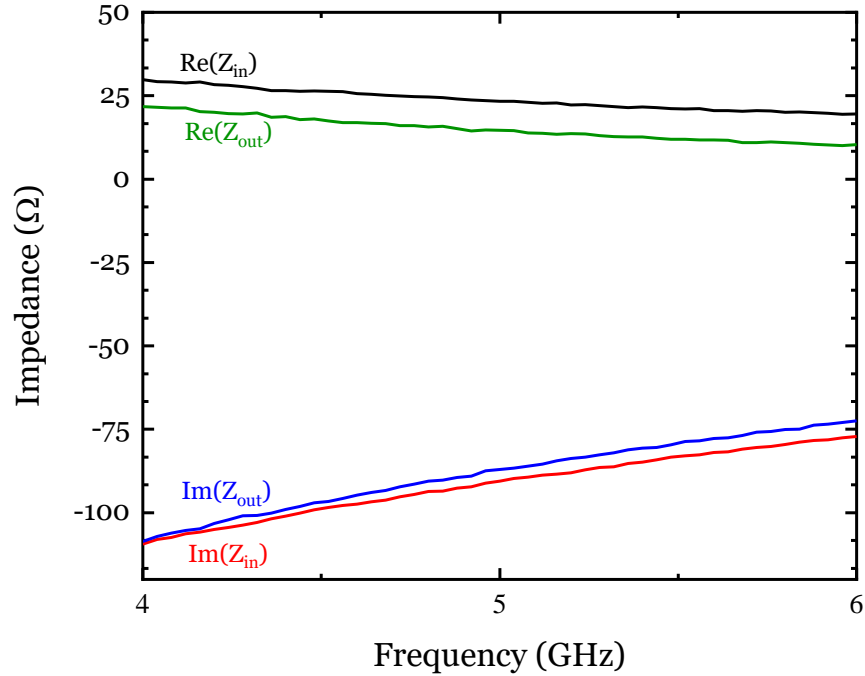
Fig. 5.7. Measured input and output impedances of the PA in the 4-6 GHz frequency range.

The measured S-parameters were also used to calculate the maximum available gain (MAG) of the PA in the measured frequency range. As shown in Figure 5.8, MAG exhibits a behavior similar to $S_{21}$ and a maximum small signal gain of 29.5 dB is expected at 5 GHz in case of simultaneous input and output matching. The S-parameters of the PA are bias dependent and finding the optimum biasing point helps improving the MAG. At a specific supply voltage, there are two degrees of freedom to set the biasing scheme which are the gate of each transistor. Extrapolating the measured MAG plot suggests a ~ 17 dB of small signal gain at 24 GHz, a frequency which the design will be optimized for later on in this chapter.

Increasing the biasing voltages at a fixed frequency improves the maximum available gain at the cost of more DC power consumption which can degrade the power added efficiency (PAE). However as stated before, maximum available gain is a figure of

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merit that assumes conjugate matching at the input and output ports. It should be investigated to find out if the perfect input and output matching conditions results in a stable amplifier or not. Source and load stability circles can be plotted using the measured S-parameters to find out all the source and load impedances under which the amplifier is stable.
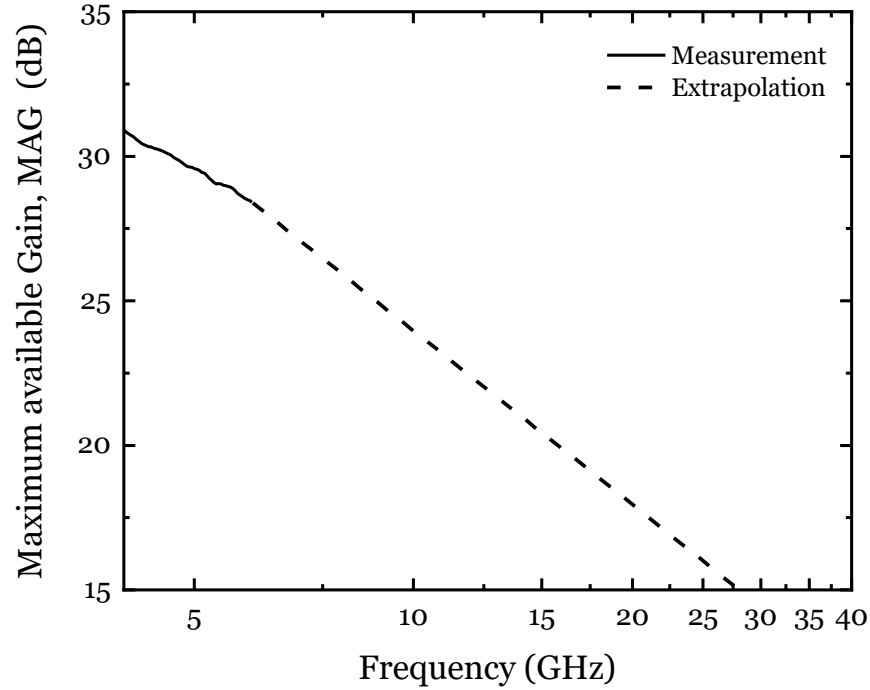


Fig. 5.8. MAG of the PA calculated based on the measured S-parameters.

When $|\Gamma| = 1$, the amplifier operates at the verge of stability and instability. So the contour of all the points with $|\Gamma| = 1$ helps visualizing the amplifier stability boundary on the Smith chart. In a general two port network, the source (input) reflection coefficient can be written as:

$$\Gamma_s = S_{11} + \frac{S_{12}\,S_{21}\,\Gamma_L}{1 - \Gamma_L\,S_{22}} = \frac{S_{11} - \Delta\Gamma_L}{1 - \Gamma_L\,S_{22}} \tag{5.7}$$

The same equation can be written for the load (output) reflection coefficient. In order to find the region associated with $|\Gamma_S| = 1$, we can write:

$$| \Gamma_S | = \left| \frac{S_{11} - \Delta\Gamma_L}{1 - \Gamma_L S_{22}} \right| = 1 \tag{5.8}$$

$$\left| \Gamma_S - \frac{S_{22}^* - \Delta^* S_{11}}{|S_{22}|^2 - |\Delta|^2} \right| = \frac{|S_{12} S_{21}|}{|S_{22}|^2 - |\Delta|^2} \tag{5.9}$$

Equation 5.9 is the equation of a circle which divides the Smith chart between stable and unstable regions. This circle is referred to as the source stability circle and determines the input reflection coefficient values that make the PA unstable. Similarly, the equation for the load stability circle can be derived which provides the output reflection coefficient values to design a stable PA. Both the source and load stability circles of the measured S-parameters are shown below. In order to have a stable PA, $\Gamma_S$ and $\Gamma_L$ should be within the stable region, which is indicated by arrows and encompasses the vast majority of the Smith chart area. When the optimum source and load values to attain input and output conjugate matching are calculated, it should be checked to see if they generate a $\Gamma_S$ and $\Gamma_L$ within the stable region. Otherwise, the gain magnitude should be sacrificed in order to stabilize the amplifier by moving $\Gamma_S$ and $\Gamma_L$ inside the stability circles and farther from the ideal conjugate match point.
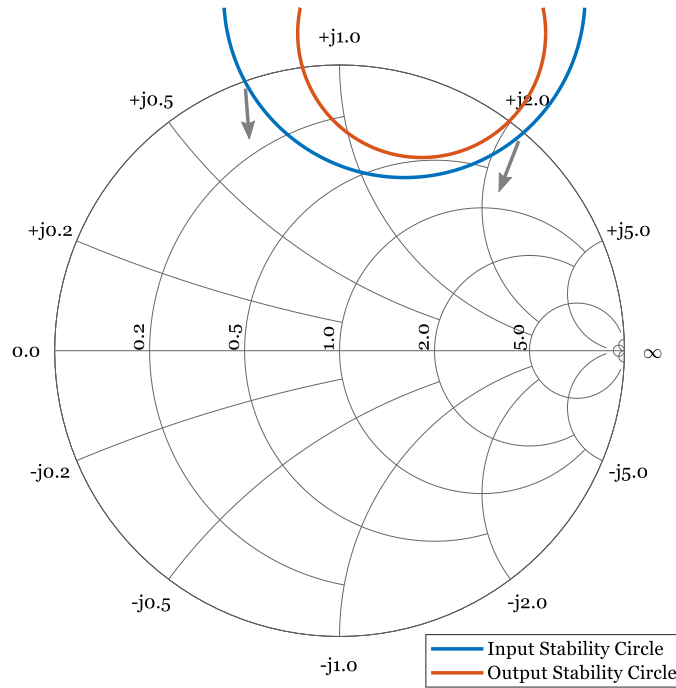
Fig. 5.9. Input and output stability circles of the PA at 5 GHz.

### 5.3.3.  Cascode Power Amplifier Large Signal Measurements

The setup block diagram used for the large signal measurements is illustrated in Figure 5.10. Prior to the DUT measurements, the power loss of the RF cables, bias-tees, connectors and each of the power blocks in the path of power flow was measured at the frequency of operation to account for the total power loss associated with the measurement setup. The available $P_{in}$ is generated and shown by the Agilent N5182A vector signal generator. $P_{in}$ delivered to the DUT reference planes is calculated by subtracting the components' power loss placed in between the signal generator and the input port GSG probe from the available $P_{in}$. This step was done using a high precision thru connector from the Impedance Standard Substrate (ISS) shown in Figure 4.12. The thru connector is considered to be ideal and no power loss is associated with that. Likewise, $P_{out}$ is determined by adding the power loss of the components connected

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between the output power sensor and the DUT output reference planes to the value measured by the Agilent E4417 power meter.
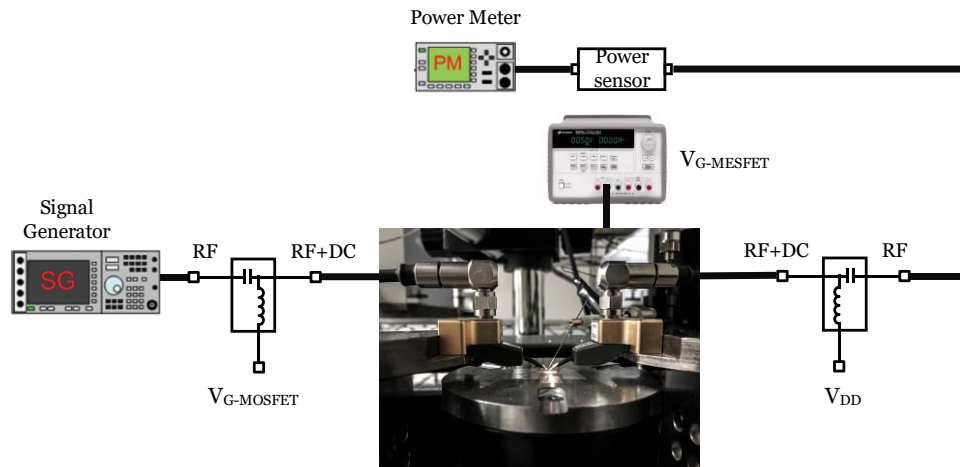


Fig. 5.10. Large signal measurements setup

After characterizing the setup, the PA was connected to the system as the DUT and was biased using the turn on steps provided in Section 5.3.1 to operate in deep class-AB. A 0.25 V biasing voltage was applied to the input port GSG probe (MOSFET gate). The gate of the MESFET was set to 0.8 V to generate sufficient DC voltage at the MOSFET drain terminal and push the transistor into saturation region. Once a supply voltage of 3 V was applied to the output port GSG probe (MESFET drain), the output quiescent current was increased to 11 mA. Inferring from the measured I-V characteristics of a narrower 300 µm wide MESFET with the same gate and access lengths presented in Figure 2.4, the voltage drop on the MESFET's gate-source junction is approximated to be ~ 0.1 V. Thus, ~ 0.7 V is presented to the MOSFET's drain which ensures its saturation region operation considering a ~ 0.05 V overdrive voltage at this biasing condition.
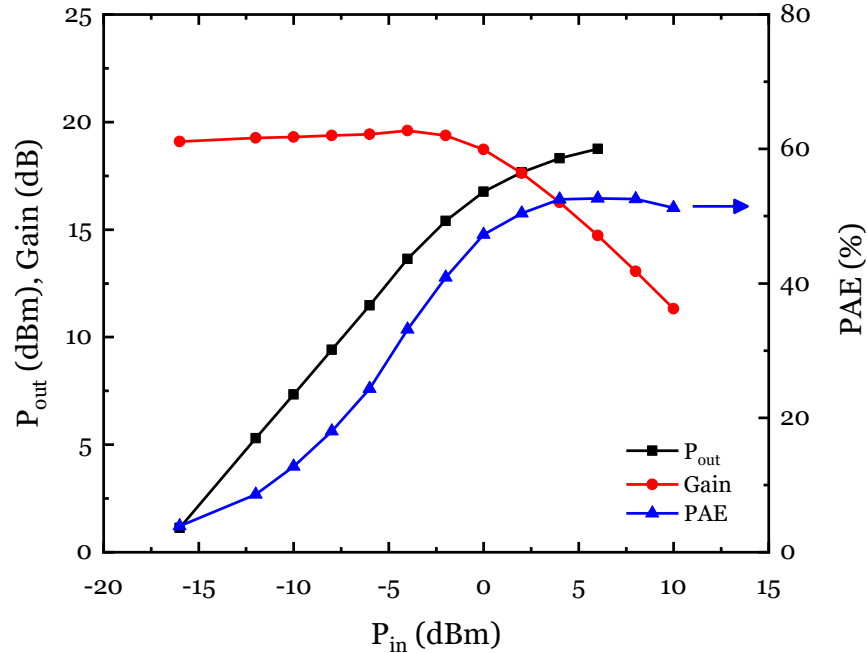
Fig. 5.11. Gain, PAE and output power of the cascode PA plotted versus input power at 5 GHz for $V_{G\text{-}MOSFET}$ = 0.25 V, $V_{G\text{-}MESFET}$ = 1 V and $V_{DD}$ = 3 V.

The input power ($P_{in}$) was swept from -16 dBm to 10 dBm in Figure 5.11 at 5 GHz. It is requisite to de-embed the loss associated with the setup from the measurements to evaluate the authentic performance of the PA at the device reference planes. The PA's measured characteristics after excluding the system power loss resulted in a maximum power gain of 19.1 dB, a saturated output power of 19.4 dB, an output 1-dB compression point of 16 dB, and a maximum PAE of 52.6%. The RMS output current increases to 52 mA when a 10 dBm input power is fed into the amplifier.

The input power sweep was repeated in the 4 GHz to 6 GHz frequency range in 0.5 GHz steps under the same biasing conditions. The upper frequency limit was imposed by the signal generator which was 6 GHz. At each frequency, the figures of merit including OP1dB, $P_{sat}$, PAE and maximum power gain were measured as presented in Figure 5.12.
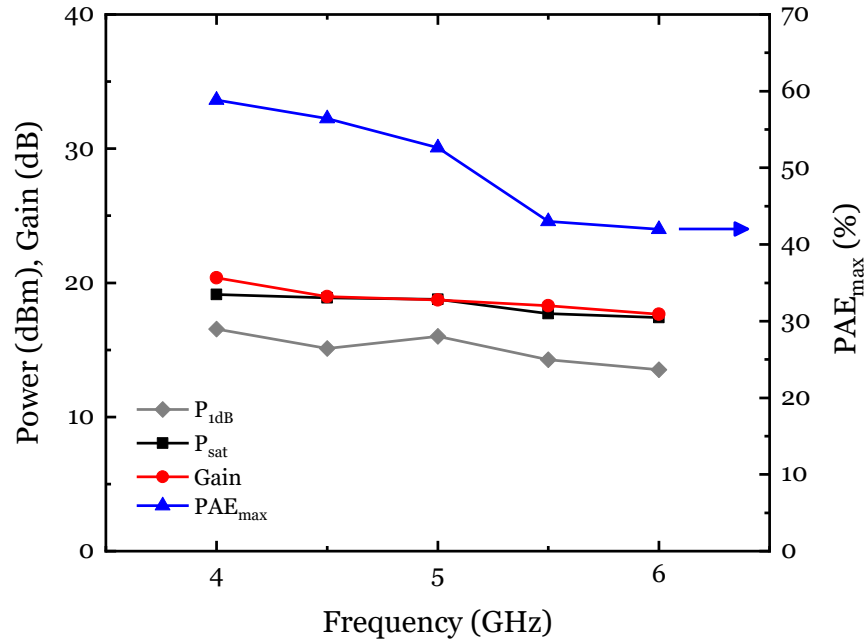
Fig. 5.12. Measured large signal performance versus frequency under the same biasing conditions as in Figure 5.11.

The saturated power 1dB bandwidth is from 4 GHz to 5 GHz, presenting a 20% fractional bandwidth. PAE and OP1dB remain above 42% and 13.5 dBm in the measured frequency band, peaking to 59% and 16.7 dBm at 4 GHz respectively. The power gain at the OP1dB point drops from 20.4 dB at 4 GHz to 17.7 dB at 6 GHz, resulting in a 3 dB bandwidth greater than 2 GHz (3 dB fractional bandwidth >40 %).

Increasing $V_{G-MOSFET}$ to 0.5 V enables class-A operation until $P_{in}$ ~ 2 dBm, where the input signal reaches $V_{peak}$ = 0.4 V. Larger input powers will swing $V_{G-MOSFET}$ below $V_{th}$ and turn the PA off. With $V_{DD}$ increased to 5 V to accommodate larger output signal swing and $V_{G-MESFET}$ = 1 V, the quiescent current grew to 70 mA and a maximum power gain of 24.4 dB, saturated power of 20.6 dBm, OP1dB of 17.5 dBm and maximum PAE of 28.5% was recorded. Stressing the PA by applying larger biasing and supply voltages elevate the $P_{sat}$ and power gain values, which was avoided so as not to damage the device.

TABLE 5.1. PERFORMANCE COMPARISON TO STATE-OF-THE-ART PAs AT ~ 5 GHz

| | Process | $f_C$ (GHz) | $P_{sat}$ (dBm) | Gain (dB) | PAE (%) | Supply (V) | Area (mm²) |
|---|---|---|---|---|---|---|---|
| MTT 17 [89] | 130-nm CMOS | 5 | 18.5 | NR | 40 | 3.6 | 0.62 |
| JSSC 16 [90] | 65-nm CMOS | 4.75 | 26 | NR | 21.2 | 3 | 2.25 |
| JSSC 15 [91] | 40-nm CMOS | 5 | 24 | 10 | 35 | 2.5 | 1.07 |
| JSSC 15 [92] | 65-nm CMOS | 4 | 27.3 | 16.8 | 32.5* | 3 | 2.1 |
| JSSC 10 [93] | 65-nm CMOS | 5 | 26.7 | 12.5 | 25.3* | 3.3 | 0.27 |
| SiRF 13 [94] | 180-nm CMOS | 5 | 15.4 | NR | 40.6 | 2 | 0.81 |
| S3S 17 [95] | 22-nm FDSOI | 5.4 | 26 | 20 | 31 | 2.7 | 0.2 |
| This work | 45-nm CMOS | 5 | 24.4 / 20.4 | 20.6 / 19.1 | 29 / 52.6 | 5 / 3 | 1.11 w pads / 0.006 wo pads |

*Drain efficiency (%)

The performance of the PA at 5 GHz is summarized and compared to other state of the art CMOS PAs in Table 5.1. The highest power gain, PAE and supply voltage is achieved by this compact MOSFET-MESFET cascode design. As mentioned before, there is large power loss at the input of the PA due to impedance mismatch and the achieved results can be improved by adding an on-chip matching network.

## 5.4. On-chip Input Matching and Future Work

One of the targeted applications of this PA is the anticipated 5G cellular network. That being so, the center operating frequency of the PA was extended to 24 GHz in an upgraded design as explained below. Referring back to Figure 5.8, the expected small signal MAG of the PA is approximately 17 dB at 24 GHz. The substantial achievable gain of the PA at the aimed operating frequency asserts the objective of a *K*-band frequency PA design is well founded. The concern of the PA impedance mismatch should also be addressed in the new design. The S-parameters of the PA were measured at a higher frequency range than Section 5.3.2, and the input impedance of the PA was derived to design an on-chip input L-match network for impedance transformation. Due to the limited quality factor of on-chip reactive components on CMOS technology at high frequency ranges, on-chip matching networks are inherently lossy and cause performance degradation [96]. The lowest quality factor (Q-factor) pertains to spiral inductors which are modeled as an ideal lossless inductor in parallel with a resistor [97]. The parasitic loss of the conductive silicon substrates in CMOS technologies is one of the reasons behind the finite Q-factor inductors. Higher resistivity of the trap-rich silicon substrates described in Chapter 3 helps alleviate the substrate loss. Relatively narrow metal stacks and their proximity to the lossy substrate increase the resistive loss of the interconnects as well, and lower the total stored energy in the inductor [98]. The required inductance for mm-wave applications is typically of the order of 100 pH which makes the inductor footprint small and causes lower substrate coupling loss [99]. The thickness of the top aluminum metal layer available in the 45RFSOI technology is greater than the skin depth (how deep an RF signal penetrates a material) at 24 GHz (~ 0.5 μm), and makes the usage of the inductor plausible.

However, similar to [88], the matching network was only designed for the input port of the PA due to lower signal swing compared to the output port. High gain of the PA generates a larger signal swing and higher power levels at the output port, and employing a finite Q-factor inductor at the output port suppresses the power efficiency and $P_{sat}$ by introducing a higher loss.

### 5.4.1.   On-chip Input Matching Network Design

The intent on designing a PCB for the initial cascode PA design was finding the optimum input and output matching impedances through load/source pull measurements and providing the input and output matching networks using surface mound device (SMD) component. High insertion loss inflicted by the SMD components at 5G frequencies and their restricted resonant frequency, motivated adopting an approach similar to [88] to design an on-chip L-match input matching network. The mediocre Q-factor of the passive elements in $K$-band frequencies motivated the design of an input matching network at the NFET gate which hosts low current levels.

The output impedance of the PA was designed to get closer to 50 Ohms by reducing the MESFET size. The PA load line can also be adjusted during the DC biasing process to present a higher output impedance. The schematic of the proposed PA is illustrated in Figure 5.13. The RF choke inductors will be provided by the off-chip bias tees connected to the GSG RF probes.
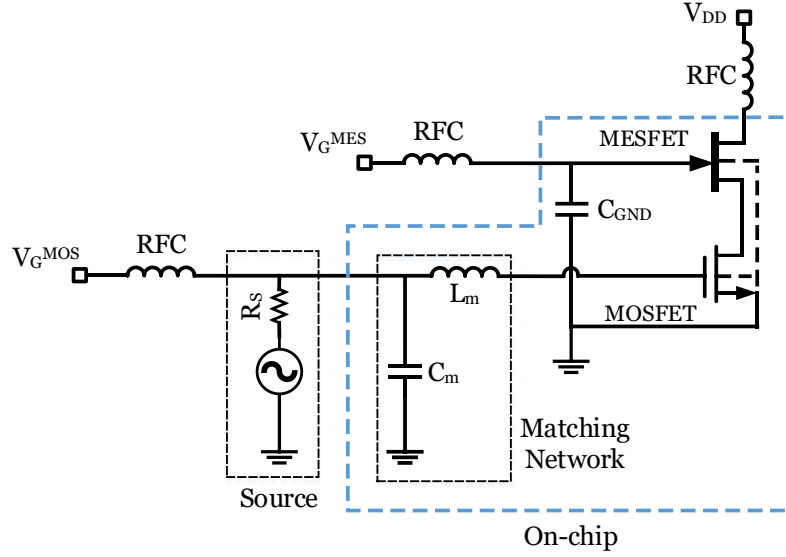
Fig. 5.13. The schematic of the optimized $K$-band RF PA.

The S-parameter measurement results of an identical PA without an on-chip input matching network showed an input impedance of $Z_{in} = 5 - j20$. Figure 5.14 shows the Cadence simulation result of the designed input on-chip L-match frequency response at 24 GHz. Since the input RF pad generates a $\sim$ 70 fF parasitic capacitance as reported in Table 4.1, it was integrated into the input matching network to reduce the capacitance value needed for the shunt $C_m$.

A single layer symmetric rectangular spiral inductor was used as the series $L_m$. An approximation for the inductance of a planar spiral inductor was presented in [100]:

$$L = \frac{\mu \, n^2 \, d_{avg} \, C_1}{2} \left( \ln\left(\frac{C_2}{\rho}\right) + C_3\rho + C_4\rho^2 \right) \tag{5.5}$$

Where

$C_i$ = Inductor layout dependent coefficients

$d_{avg} = \frac{d_{in} + d_{out}}{2}$

N = Number of spiral turns

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$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$$

Among the 3 aspect ratio options available in this technology, an aspect ratio of 1 with a turn width of 6 μm gave the desirable inductance for the matching network inductor. The shunt capacitor ($C_m$) was also realized through a high Q-factor metal-insulator-metal (MIM) capacitor with a capacitance per unit area of 0.2 $\frac{fF}{\mu m^2}$ .
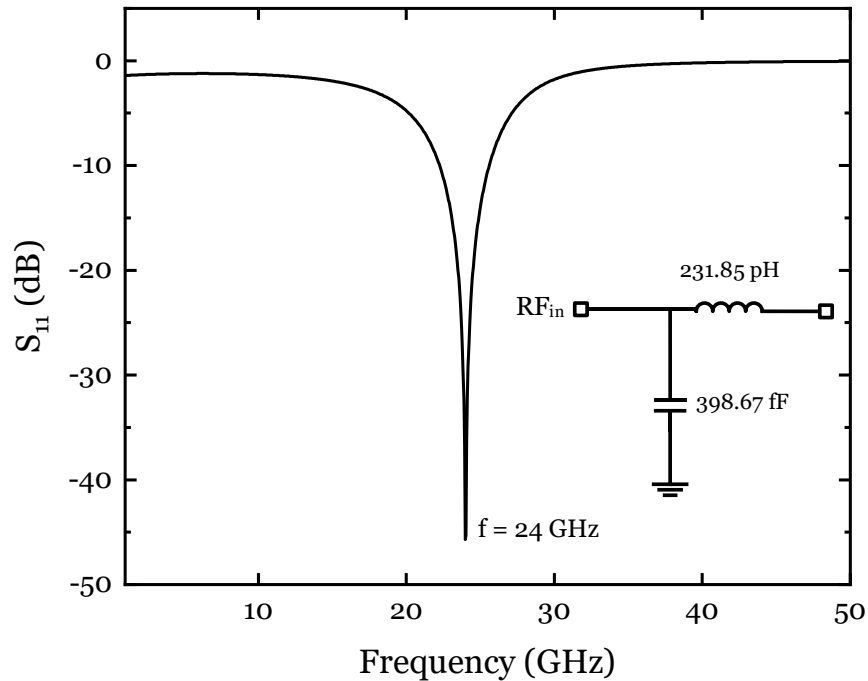


Fig. 5.14. The on-chip input matching network.

To fabricate the high Q-factor capacitor, an additional mask (QT) is placed between the topmost metal layer (LD) which is made of aluminum and the last copper metal layer below that (OB). The top aluminum metal layer and the new QT mask form the top and bottom parallel plates of the capacitor respectively. Figure 5.15 presents the layout of the on-chip input matching network consisting of a shunt MIM capacitor ($C_m$) and a series inductor ($L_m$).
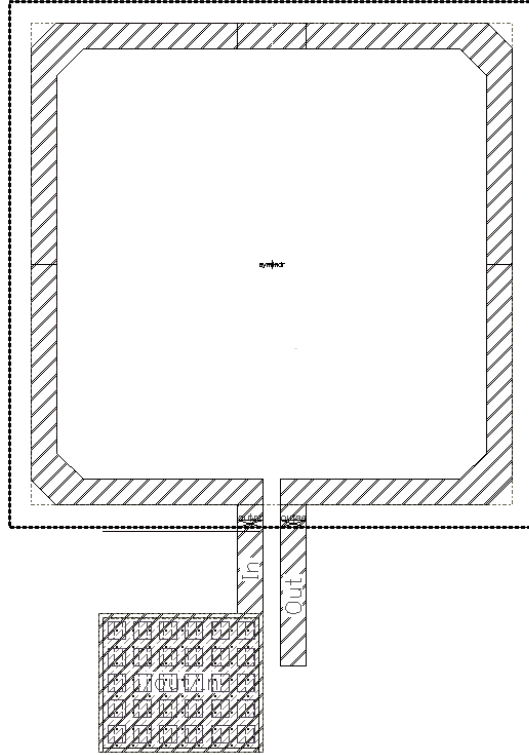
Fig. 5.15. On-chip input matching network layout.

The final layout of the optimized PA is shown in Figure 5.16, which is being fabricated at the time this dissertation is being presented. The input and output GSG pads make the on-chip probe measurements possible to eliminate the need for wire bonding the die onto a test board. An extra pad provides a DC path to the MESFET gate, while the DC biasing voltage of the NFET and the supply voltage can be applied to the pads using input and output bias tees. The input L-match circuit is expected to mitigate the input impedance mismatch and the associated input power loss. The new transistor width ratio is targeted to provide >24 dBm of $P_{sat}$ at 24 GHz, with a maximum quiescent current and voltage of ~ 200 mA and 4 V respectively. Finally, the common gate MESFET is also connected to a 160 pF AC ground capacitor to suppress the AC swings.
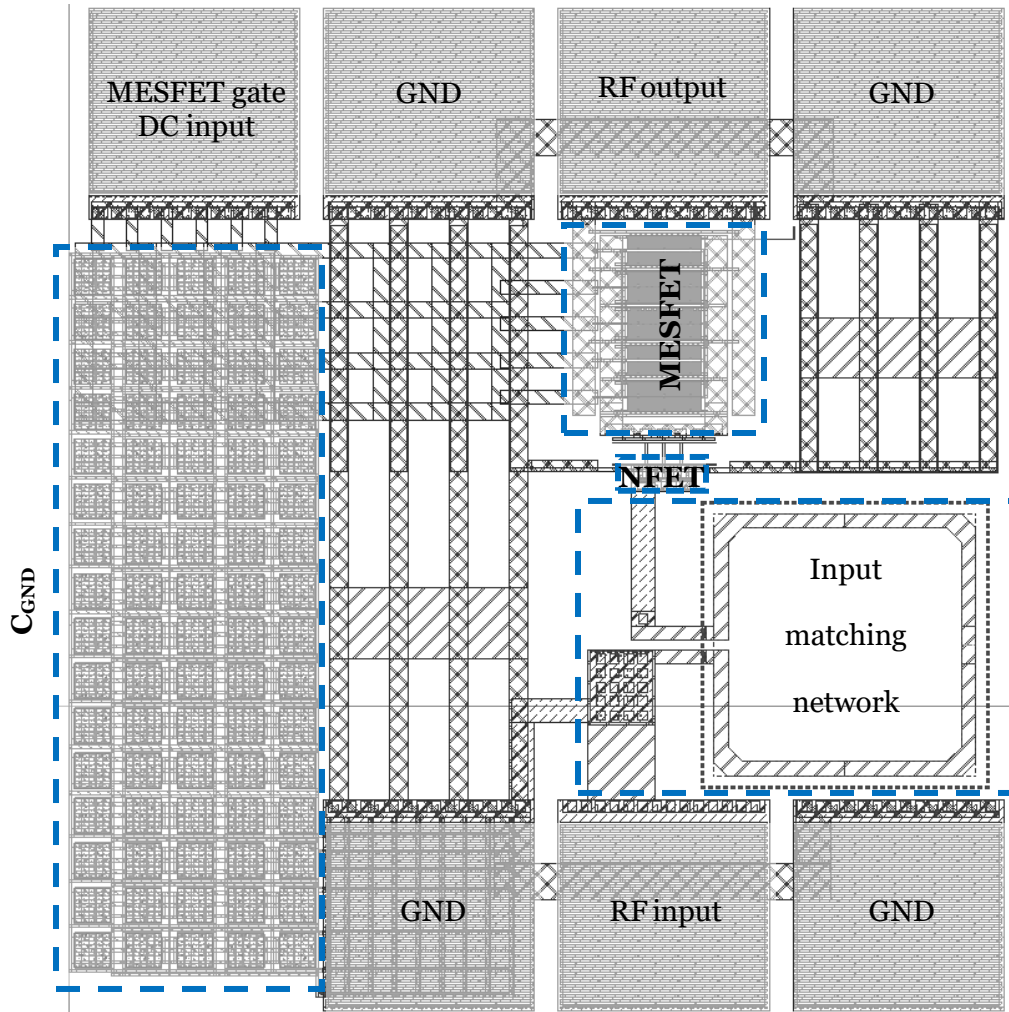
Fig. 5.16. Layout of the optimized PA in 45RF SOI technology.

## 5.5.    Summary and Discussion

The design, implementation and measurement results of the MOSFET-MESFET cascode PA were presented in this chapter. On-chip measurements using GSG input and output pads were preferred over the PCB board measurements as the undesired need for bond wires is obviated.  A maximum PAE of 52.6%, $P_{sat}$ of 20.4 dBm, gain of 19.1 dB and OP1dB of 17.5 dBm was measured at 5 GHz. For the next phase of the project, an on-chip input matching network was designed at 24 GHz to mitigate the input return loss of the PA. The next steps for optimizing the design would be confirming the input impedance

matching by measuring the S-parameters of the PA, optimizing the MESFET layout in the 45RFSOI technology for reduced parasitics and higher total output impedance, checking the spectral efficiency and linearity figures of merit such as EVM for digital modulations (e.g. QAM, PSK, etc.) once the impedance matching and transistor width ratio are confirmed.

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