THÈSE

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Titre

CONVERTISSEURS MULTINIVEAUX A BUS CONTINU AVEC POINT MILIEU. NOUVELLES TOPOLOGIES ET STRATEGIES DE CONTROLES

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Unité de recherche : *LAPLACE*
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THESIS

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Issued by *INPT, Institut National Polytechnique de Toulouse*
Discipline : *Power electronics*

Presented and defended by

Christoph Haederli

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Title

MULTI LEVEL VOLTAGE SOURCE CONVERTERS WITH 3-L DC LINK, NEW TOPOLOGIES AND CONTROL STRATEGIES

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I dedicate this thesis to my family. Without the grant of some extra time, this would not have been possible. But I also thank Esther and our kids for reminding me that there are other, more important things besides writing a thesis… I started the thesis four years ago, just about when our first child was born. To accompany and guide a child in his first steps in this world is one of the greatest things to experience. And one of the most amazing things too: Our daughter can now walk, talk, sing, paint, argue, dance, and even ride a bycicle — whereas I have merely written this thesis.

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1 RESUME FRANÇAIS (FRENCH SUMMARY)

Cette thèse concerne l'analyse et la synthèse des onduleurs de tension de multiniveaux, appelés dans la littérature anglo-saxonne *« Multi-Level Voltage Source Converters » (*ML-VSC). Les ML-VSC synthétisent une tension de sortie AC par une approximation avec de multiples niveaux de tension modulés en largeur d'impulsion *(PWM : pulse width modulation)* conformément à la Figure 1. De nouvelles topologies ML (*Multi Level*) et des techniques spécifiques de contrôle des grandeurs internes (tension du bus continu et des condensateurs flottants) sont introduites et évaluées. .

L'étude concerne principalement les convertisseurs *à bus continu avec point milieu*, une famille de convertisseurs dont la performance opérationnelle est bonne et dont les exigences en ressource sont modestes.

Les convertisseurs ML sont largement utilisés dans diverses applications industrielles. Celles-ci sont la colonne vertébrale d'une partie importante des activités d'ABB (Asea Brown Boveri Corporation), en particulier pour les applications MV (medium voltage) et HV (high voltage).

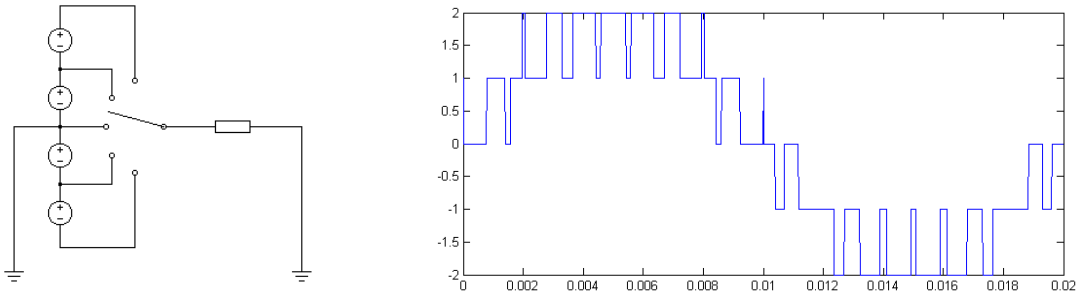


Figure 1, Convertisseur générique 5-L avec la courbe de sortie de tension correspondante

1.1 Topologies

Nous introduisons une structure générique permettant l'exploration des différentes topologies de ML- VSC, (Figure 2). Cette structure décrite à la Figure 2 correspond à l'approche proposée par F. Z. Peng. Il s'agit d'une représentation triangulaire pour l'analyse et la synthèse de convertisseurs ML. Cette structure ML contient beaucoup de redondances et différents convertisseurs ML peuvent être obtenus en éliminant systématiquement des composants du circuit (interrupteurs actifs, diodes, condensateurs). La plupart des ML VSC connus aujourd'hui peuvent être obtenus de cette manière et rentrent ainsi dans le cadre de cette structure générique.

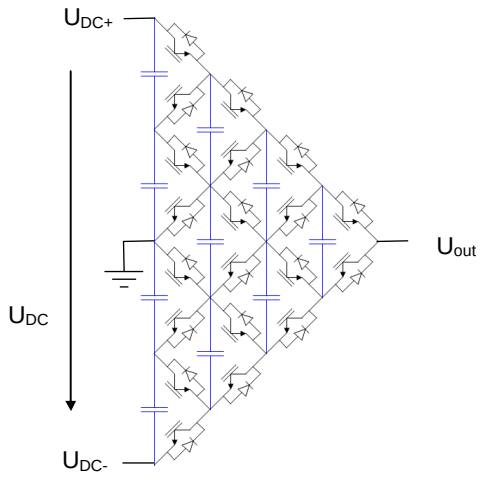


Figure 2, Structure d'un convertisseur ML générique en représentation triangulaire

La Figure 3 présente quatre exemples de topologies bien connues de convertisseurs ML

(a) Multi Level diode clamped converter (MLDC)

(b) Multi cell converter (MC) également connu comme flying capacitor converter

(c) Stacked multi cell converter (SMC)

(d) Active neutral point clamped converter (ANPC)

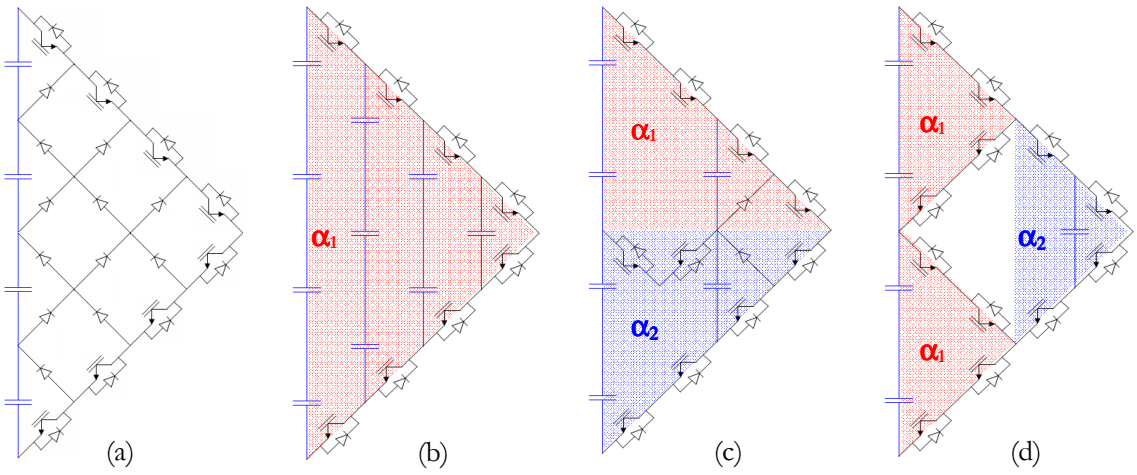


Figure 3, structure de convertisseurs 5-L: (a) MLDC, (b) MC, (c) SMC, (d) ANPC 1

α_1 et α_2 indiquent les rapport cycliques appliqués dans les convertisseurs partiels indiqués par les régions aux couleurs correspondantes. Notons que tous les composants représentés ici ont des tensions nominales identiques. Le nombre de composants connectés en série illustre donc les exigences de tension nominale indépendamment du nombre de composants effectivement utilisés. (Combinaison de composants connectés directement en série remplacée par un seul composant).

De nouvelles topologies ont ainsi été introduites, elles sont basées sur une approche systématique réduisant les composants dans le convertisseur généralisé. Le nombre de structures possibles augmente fortement avec le nombre de niveaux. Quelques exemples de conception de convertisseurs génériques 5-L, et les nouvelles topologies qui en résultent, sont présentés à la Figure 4. Ces nouvelles structures ont de propriétés très similaires à l'ANPC.

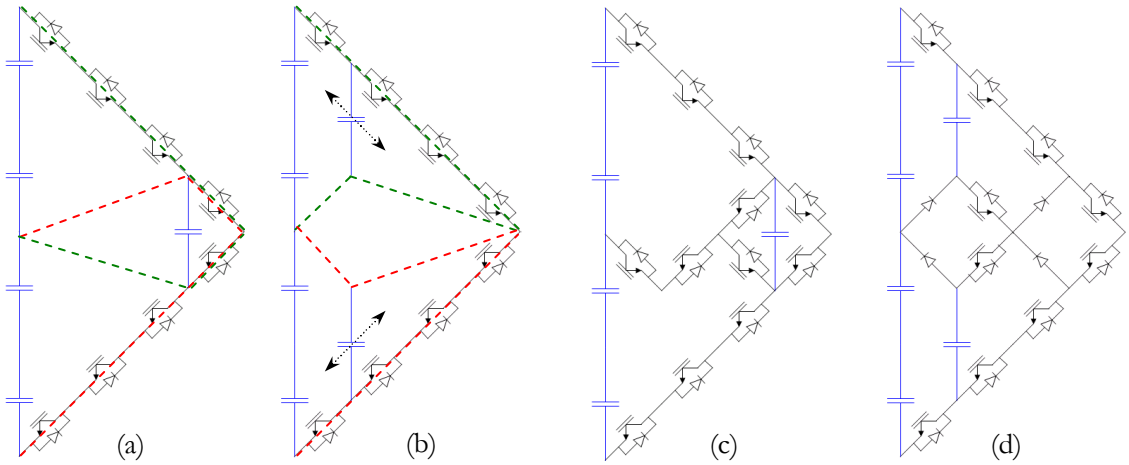


Figure 4, synthèse de 5-L génériques et deux exemples de nouvelles topologies qui en résultent

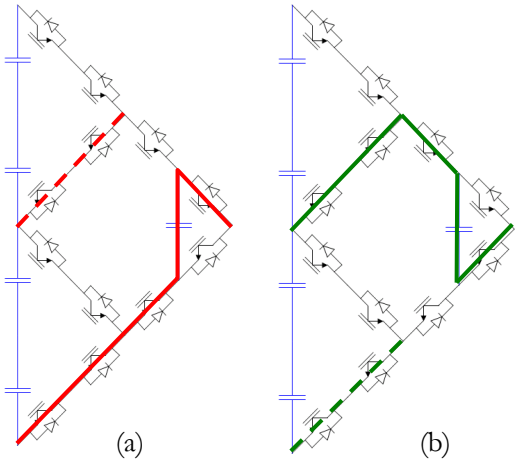
Un certain nombre de topologies ML sont comparées sur la base des contraintes sur les semi-conducteurs, des énergies stockées dans les condensateurs flottants et d'autres critères additionnels comme la contrôlabilité du point neutre. Les résultats principaux sont les suivants:

1. Le MC a les meilleures propriétés pour ce qui concerne le nombre de semi-conducteurs, mais une énergie importante est stockée dans les condensateurs flottants.
2. Le MLDC et les autres topologies avec plus de 3 niveaux d'entrée n'ont pas besoin, ou ont moins besoin d'énergie dans les condensateurs flottants. Par contre elles ont un plus grand nombre de semi-conducteurs (diodes) pour un nombre plus important de niveaux et ont de sérieuses limitations dans la plage de fonctionnement (profondeur de modulation et facteur de puissance de la charge)
3. Les convertisseurs *à bus continu avec point milieu* incluant des circuits MC multiples présentent un bon compromis entre le nombre de semi-conducteurs, l'énergie stockée dans les condensateurs flottants et la contrôlabilité. Le SMC et le ML ANPC (y inclus les nouvelles topologies proposées) sont des exemples significatifs de cette famille de topologies.

En se basant sur ces résultats, nous pouvons affirmer que les topologies à bus continu avec point milieu sont très intéressantes pour des applications MV de n'importe quel type. La suite de ce manuscrit de thèse se focalise donc sur une analyse approfondie de ces topologies.

1.2 Propriétés des convertisseurs à bus continu avec point milieu

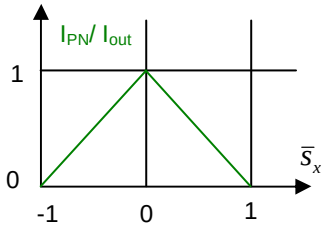
Les convertisseurs *à bus continu avec point milieu* utilisant des condensateurs flottants doivent contrôler la tension de condensateurs flottants (FC) et du point neutre (PN). Ceci est réalisé en premier lieu en utilisant des états redondants pour le contrôle des FC et la tension homopolaire pour le contrôle du PN. C'est la raison pour laquelle une analyse des états redondants d'une part, ainsi que du courant PN fonction de la tension homopolaire d'autre part, sont cruciaux pour la conception des contrôleurs.



État	Nombre de niveau et tension	I_{PN}	I_{CF}
0	0 ($-U_{DC}/2$)	0	0
1	1 ($-U_{DC}/4$)	0	$+I_{Out}$
2	1 ($-U_{DC}/4$)	$+I_{Out}$	$-I_{Out}$
3	2 (GND)	$+I_{Out}$	0
4	2 (GND)	$+I_{Out}$	0
5	3 ($+U_{DC}/4$)	$+I_{Out}$	$+I_{Out}$
6	3 ($+U_{DC}/4$)	0	$-I_{Out}$
7	4 ($+U_{DC}/2$)	0	0

Figure 5, ANPC de type 1 avec les états redondants mis en évidence pour le niveau 1.

Le 5-L ANPC présente 61 phaseurs spatiaux (mode différentiel, 2-D en alpha bêta) 125 phaseurs spatiaux et 525 états du convertisseurs. De façon évidente, il y a beaucoup d'états redondants pour la génération de la tension de sortie requise. La Figure 5 illustre deux exemples d'états redondants pour le 5-L ANPC 1, qui peuvent être utilisés pour équilibrer la tension des FC. L'impact sur le courant du PN est illustré dans le tableau ci-dessus. Le courant moyen du PN qui en résulte est défini statistiquement parce que les deux états redondants pour un niveau de tension de sortie donné doivent être appliqués avec le même rapport cyclique, de manière à maintenir la tension des FC équilibrée (en tout cas pour le cas des procédés de modulation standard avec un contrôle découplé des FC et du PN). Ceci est vrai pour tous les convertisseurs *à bus continu avec point milieu* ; le courant du PN est une fonction de la tension de sortie et cela peut facilement être déterminé à partir de la fonction de commutation $\bar{s}_x$, allant de -1 à 1 pour un niveau de sortie entre 0 et 4).



$$\bar{i}_{NP\_x} = (1 - abs(\bar{s}_x)) * \bar{i}_{out\_x}$$

Figure 6, Courant du PN par phase en fonction de la fonction de commutation

Cette fonction peut être étendue à un convertisseur triphasé. La Figure 61 (a) montre alors le courant PN instantané en fonction de la tension homopolaire pour un point spécifique de fonctionnement. La Figure 61 (b) montre la même chose en fonction de temps (indiqué par l'angle de tension, θ).

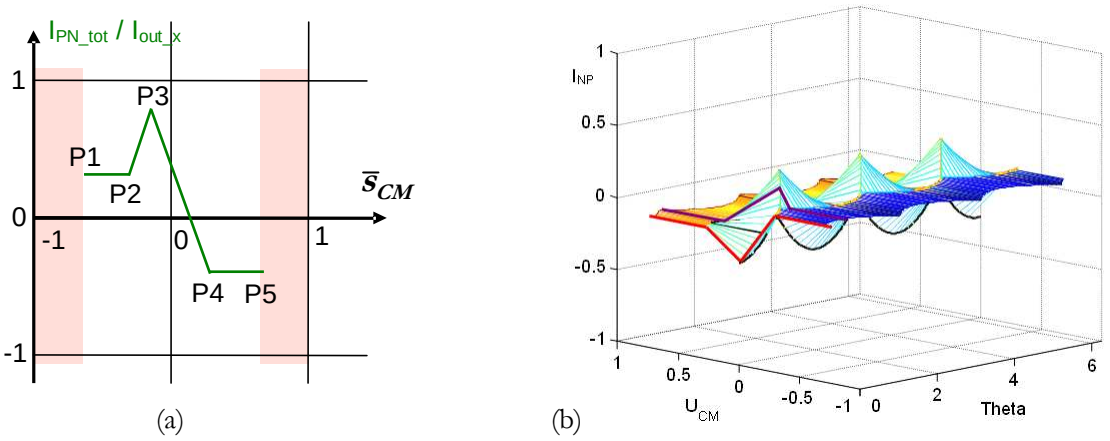


Figure 7: Courant du PN en tant que fonction de la tension homopolaire dans un système triphasé, (a) exemple pour un point de fonctionnement spécifique en compensateur d'énergie réactive, (b) fonction du courant du PN, m=0.3, φ =1.4

La connaissance des caractéristiques du courant du PN peuvent être utilisée pour déterminer le courant maximum (P3 dans la Figure 61 [a]) et minimum (P4 dans la Figure 61 [b]) du courant du PN. Ce dernier étant fonction de l'indice de modulation, du facteur de déplacement de la charge (cos φ) et de tension (θ), indiquant la capacité de contrôle du PN pour un point d'opération donné.

La relation entre le courant du PN, la fonction de commutation et le courant de charge a également été analysée dans le domaine fréquentiel. Ceci n'est pas mathématiquement évident dans la mesure où la fonction de courant du PN contient une fonction de valeur absolue qui ne peut pas être facilement représentée dans le domaine fréquentiel. Une approche complète avec une solution simple est présentée pour deux cas spécifiques.

1. Une fonction de commutation sinusoïdale à la fréquence fondamentale avec une compensation DC CM mais sans injection d'harmoniques.
2. Une fonction de commutation avec comportant une composante fondamentale, associée à une injection d'harmoniques, mais sans compensation DC CM.

Ces deux cas sont étudiés analytiquement. Le premier cas est évident (développement en série standard). Le deuxième peut être calculé en considérant chaque harmonique séparément dans la fonction de commutation et en utilisant les relations (1) et (2).

$$s_{trans\_x\_n}(t) = \sin(n * \omega t + \varphi_{nx}) * sign(\sin(\omega t + \varphi_{1x})) \quad (1)$$

$$S_{rect\_x}(\omega) = \sum_{n=1}^{\infty} S_{trans\_x\_n}(\omega) \quad (2)$$

Les deux cas sont très utiles pour une compréhension de base des caractéristiques du courant du PN et de son comportement dans des conditions perturbées. Ils ont été utilisés pour le design d'un contrôleur du courant PN, comme indiqué dans le prochain paragraphe.

Les résultats fondamentaux sur interactions des harmoniques sont les suivants:

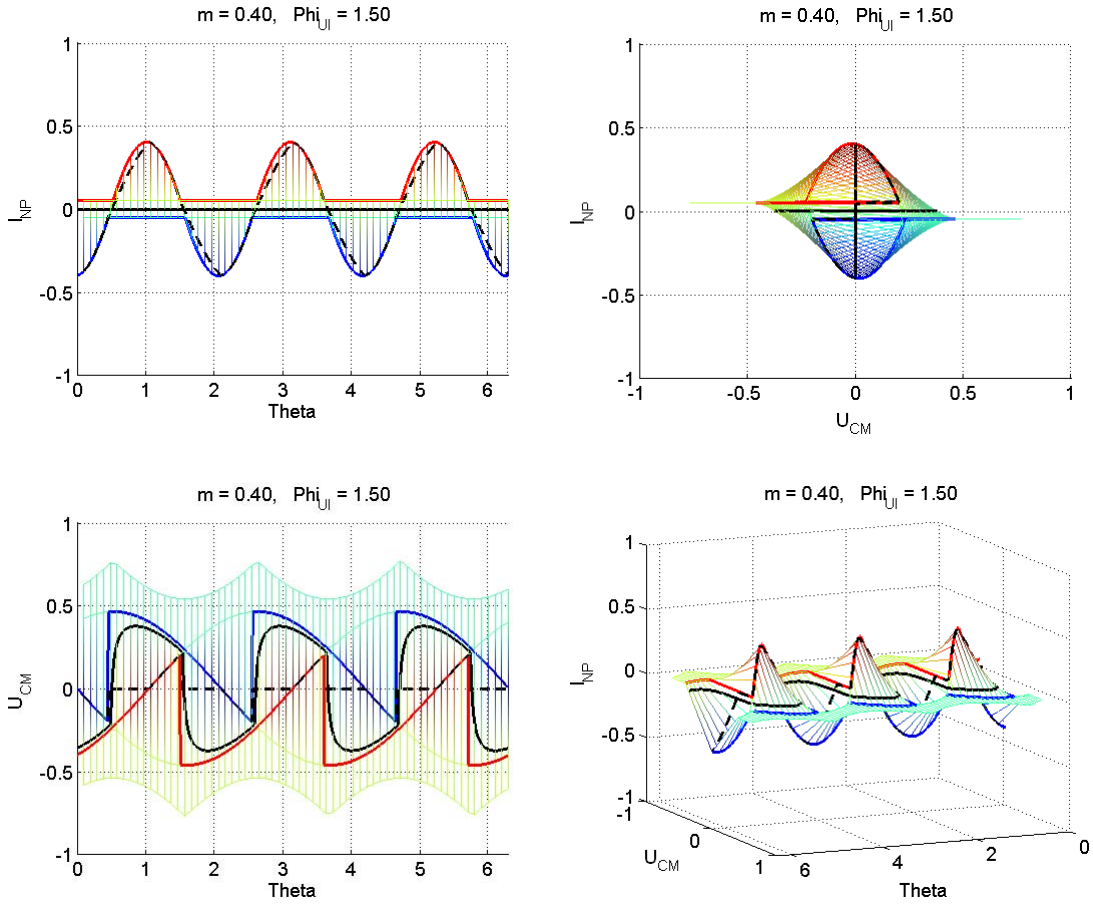
- Un harmonique de rang deux sur le courant AC génère un courant DC NP assez important en raison du fondamental et de la troisième harmonique de la fonction de commutation.
- Un harmonique de rang trois est présent dans le courant PN, s'il n'est pas compensée, en raison du fondamental et de l'harmonique de rang 3 dans la fonction de commutation.
- L'injection DC CM est la plus efficace pour la génération de courant DC NP dans des fonctionnements à facteur de puissance unitaire.
- Les deuxième et sixième harmoniques sont les plus efficaces pour la génération d'un courant DC NP dans un fonctionnement en compensation de puissance réactive.

1.3 Contrôle du PN avec modulation à base de porteuse

Un concept de contrôle du PN par injection « limitée » de tension homopolaire a été introduit. Ce concept utilise la fonction du courant PN, mais seulement la partie la plus utile est appliquée. Par exemple dans le cas de la Figure 61 (a), la tension homopolaire est limitée entre les points P3 et P4 ; dans la Figure 8, la tension homopolaire est limitée entre les trajectoires bleu et rouge. De cette manière les courants PN minimaux et maximaux peuvent être obtenus et une boucle de contrôle linéaire est possible.

Ce concept de contrôle est une amélioration importante en comparaison avec les concepts utilisant une tension homopolaire illimitée. Le concept fonctionne en compensation de puissance réactive et les dépassements de tension en basse modulation restent petits, tout en gardant la capacité de contrôle pour la tension du PN.

Pour garder la tension dans le PN, il faut générer un courant moyen de zéro sur un période fondamentale. Figure 8 montre deux trajectoires possibles pour obtenir un courant moyen de zéro avec deux stratégies très différentes. La trajectoire noire en ligne continue garde un courent PN zéro pendant toute la période mais introduit une tension homopolaire substantielle. La trajectoire noir en ligne pointillée garde une tension homopolaire la plus petite possible (entre les limites données) mais introduits une ondulation de courant PN ; le courant PN moyen reste zéro. Il y a donc un degré élevé de liberté dans le choix du point d'opération pour annuler l'erreur sur la tension PN; autre trajectoire pour l'injection homopolaire sont possible. Le système peut être optimisé avec des objectifs différents. Un objective pourrait être l'optimisation de la distorsion de sortie en appliquant par exemple une modulation CSPD PWM (Center Spaced Phase Disposition PWM).



Note: Phi_{UI} dans ce graphique est équivalent à φ, U_{CM} est équivalent à $\overline{s}_{CM}$.

Légende (valable pour tous les graphiques de ce type) :

- rouge: Trajectoire maximum du courant PN
- bleu: Trajectoire minimum du courant PN
- noir: trajectoire du courant PN base sur une stratégie d'injection
- lignes fines: Fonction du courant PN dans le temps

Figure 8, Projections de la fonction courant PN en trois dimensions pour m = 0.4 et φ = 1.5, deux types d'injection tension homopolaire montrés (noir et noir pointillé)

Un concept alternatif est proposé pour le fonctionnement en compensation de puissance réactive. On injecte une tension homopolaire en forme de 6ème harmonique. Cette approche est validée par l'analyse spectrale et le fonctionnement est aussi évident dans le domaine temporel. En compensation de puissance réactive, les trajectoires de minimum et maximum courant PN en fonction de θ sont bien différents du cas du fonctionnement à facteur de puissance unitaire. Une injection DC n'aurait pas d'impact sur le courant moyen PN. A contrario, l'injection d'un harmonique de rang 6 ne fonctionne pas du tout dans le fonctionnement à facteur de puissance unitaire. Comme les mêmes limites de tension homopolaire sont appliquées pour les deux concepts, la capacité de contrôle de la tension PN est égale dans les deux cas (si le contrôle est saturé). Les deux concepts fonctionnent pour tous les convertisseurs *à bus continu avec point milieu*, y compris le NPC. Ceux-ci ont été vérifié expérimentalement sur le prototype 5-L ANPC.

1.4 Modulateurs spécifiques pour le SMC

Une deuxième approche à base de porteuses est proposée pour des topologies spécifiques. Un exemple pour le SMC est ici illustré. Des états redondants sont utilisés pour générer des courants PN avec des caractéristiques différentes comparativement à la Figure 47. Les courants PN de phase pour des concepts différents pour le SMC sont présentés à la Figure 77 (Les rapports cycliques (α1, α2) sont définis à la Figure 3).

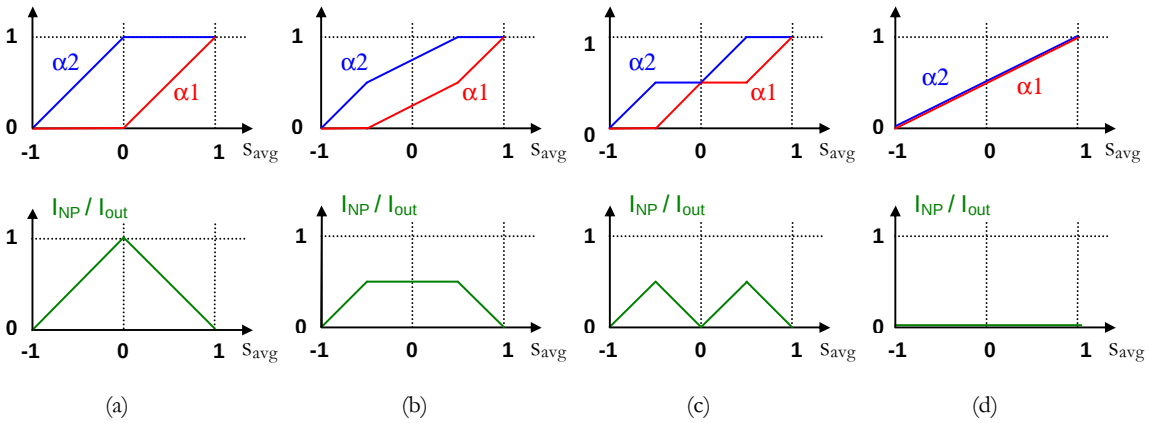


Figure 9, Courant PN par phase pour des différents concepts de modulation du SMC:
(a) modulation standard, (b) modulation type A, (c) modulation type B, (d) modulation type FC

Une combinaison des différents types de modulations pour les différentes phases dans un système triphasé permet d'obtenir un courant PN total fondamentalement différent (Figure 78). Selon le choix de modulation, différentes fonctions partiellement linéaires avec un maximum de 9 singularités sont générées. Il est possible de contrôler la tension PN indépendant de la tension homopolaire, uniquement avec le choix du type de modulation.

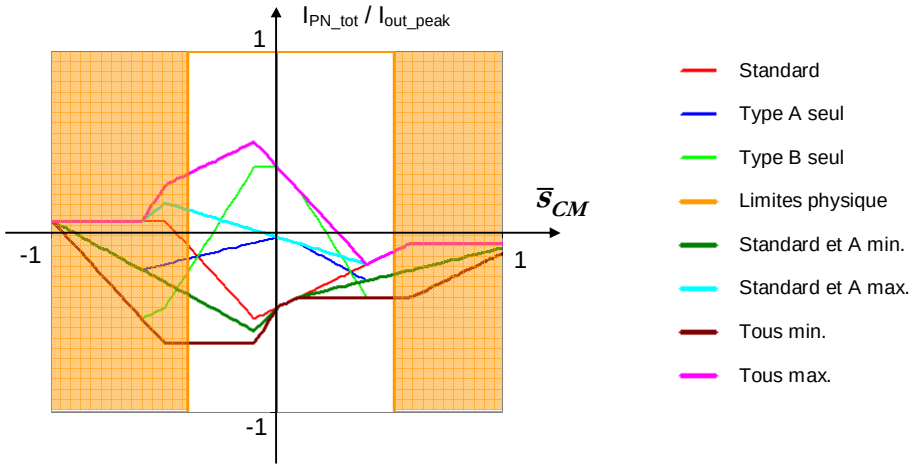


Figure 10, Courant PN avec structure de modulation étendue (α = 0.64, φ = 1.51, θ = 0.68) en fonction de la tension homopolaire

Le concept proposé a été implanté dans un régulateur à hystérésis et il a été vérifié expérimentalement sur le prototype de 5 niveaux SMC. Des caractéristiques similaires peuvent être obtenues avec des modulateurs spécifiques pour l'ANPC 3.

1.5 Concept de contrôle de tension PN à base de SVM à séquence optimale

Contrairement au ANPC 3 ou au SMC, la topologie ANPC 1 n'a pas d'états redondants mais il est possible de définir des vecteurs virtuels qui permettent de parvenir à une performance similaire à celle des concepts présentés pour l'ANPC 3 ou le SMC. Les vecteurs virtuels sont basés sur le fait que les courant de condensateurs flottants peuvent être compensés non seulement avec des états redondants mais aussi avec une combinaison des états générant différentes tensions de sortie. Spécifiquement, une combinaison des états pour +UDC/4 et –UDC/4 peuvent générer soit zéro courant dans le PN, soit 100% du courant de sortie, tout en gardant la tension dans le FC compensée. La Figure 87 montre ce concept d'état complémentaire. Des nouveaux phaseurs spatiaux peuvent être définis en combinant de multiples états qui contiennent au moins deux états complémentaires dans une phase. Si les états complémentaires sont sur des mêmes phaseurs spatiaux (2-D), on peut les appeler vecteurs modifiés. Si les états complémentaires sont sur des phaseurs spatiaux adjacents, on peut les appeler vecteurs virtuels de type 1. Si les états complémentaires sont sur des vecteurs plus éloignés, on peut les appeler vecteurs virtuels de type 2. La disponibilité de ces nouveaux phaseurs spatiaux en αβ est illustrée à la Figure 87 (c).

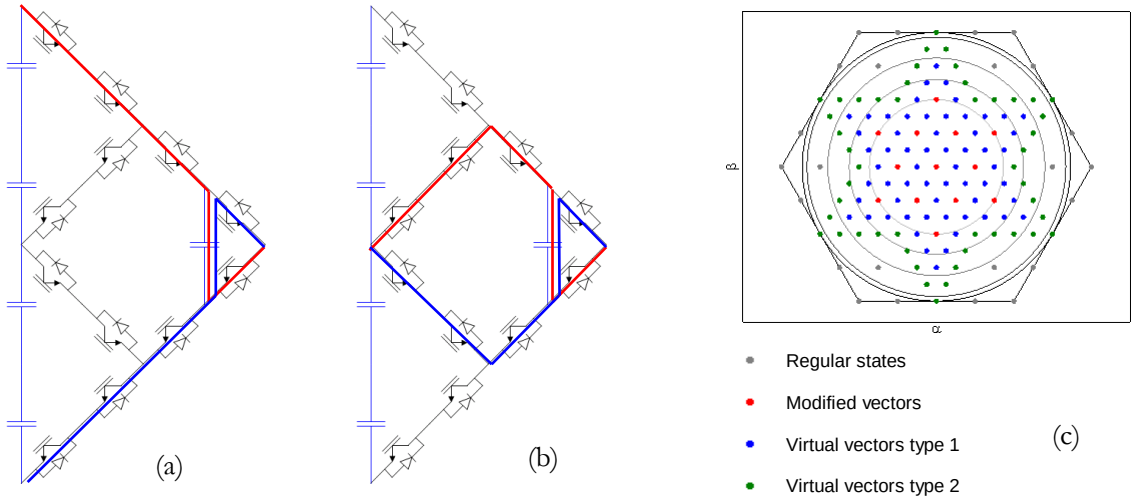
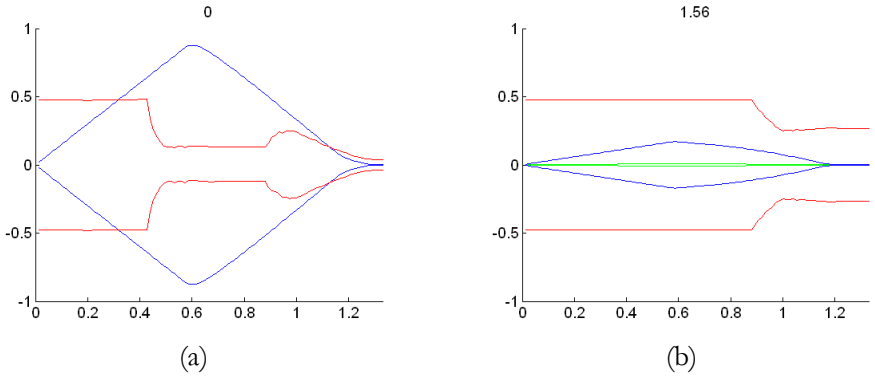


Figure 11, Combinaison d'états complémentaires: (a) zéro U_{out} avec zéro courant PN, (b) zéro U_{out} avec un courant PN maximum; (c) disponibilité de vecteurs virtuels bases sur des combinaisons d'états complémentaires

Tous ces vecteurs augmentent substantiellement la capacité de contrôle du courant PN. On peut les utiliser directement pour une modulation SVM de type NTV (les trois vecteurs les plus proche). Une autre approche choisie dans cette thèse est l'application de séquences prédéterminées. Ces séquences contiennent des états complémentaires mais les vecteurs virtuels ne sont plus visibles directement. Cette manière d'implantation est simple (à base de tableaux pré calculés) et très efficace pour une performance donnée.

La capacité de contrôle du PN est équivalente avec le courant PN moyen sur une période fondamentale, comme l'illustre la Figure 96 pour des différents types de modulation et de contrôle. Les vecteurs modifiés et virtuels sont efficaces en fonctionnement à facteur de puissance unitaire et

pour la profondeur de modulation soit faible ou proche de 1. En compensation de puissance réactive , ils sont efficaces pour toutes les profondeurs de modulation (Figure 96).



Rouge : structure du vecteur modifiée et virtuel
Bleu : structure du courant PN en temps réel
Vert : structure de l'injection DC CM non-contrainte

Figure 12, courants PN minimum et maximum en fonction de l'angle de charge, du type de modulation et de la profondeur de modulation, (a) φ = 0 [cos(φ) = 1], (b) φ = 1.56 [cos(φ) = 0.01]

On peut également calculer des séquences optimisées en temps réel. Une approche à base de MPC (model prédictive control) est aussi présentée dans cette thèse. De multiples objectifs, comme la fréquence de découpage, la distorsion harmonique de sortie, les pertes,…, peuvent être intégrés dans une seul fonction d'objectif.

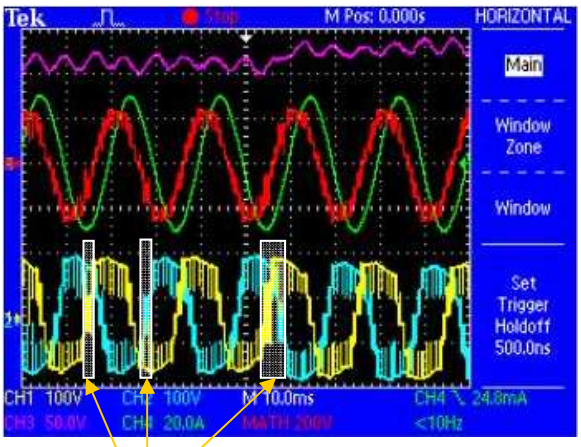
La NTV SMV régulière est utilisée dans le concept choisi, mais malheureusement, la complexité du problème augmente avec le cube de nombre de niveaux. Ainsi, pour un convertisseur de 5 niveaux, le nombre de séquences possibles peut dépasser 1000 pour certains points de fonctionnement. Une présélection de séquences raisonnables est donc nécessaire pour permettre une implantation efficace dans un système de contrôle numérique. Cette approche a été simulée avec des résultats prometteurs. Une étude spécifique est nécessaire pour implanter les algorithmes dans un circuit logique programmable (FPGA) et atteindre la performance dynamique requise pour un fonctionnement en temps réel.

1.6 Application et vérification expérimentale

Des différents concepts de modulation sont préférés en fonction des points de fonctionnement. Une approche de contrôle par hystérésis est proposée pour une meilleure utilisation de tous les concepts à disposition. La plupart des concepts de modulation sont alors vérifiés expérimentalement.

La vérification expérimentale est basée sur un contrôle par hystérésis simplifié avec deux types de modulateurs. La Figure 13 montre un exemple en compensation de puissance réactive (et pour une profondeur de modulation élevée en zone non linéaire). Le concept de fonction courant PN en temps réel ne peut plus contrôler la tension PN, celle-ci diverge lentement. L'application du concept des vecteurs virtuels ramène la tension PN à la valeur de référence dans une fraction de la

période fondamentale. En conséquence, l'impact au niveau des pertes et distorsions de sortie reste négligeable.



CH1 (jaune) : U_{out1}

CH2 (bleu-vert) : U_{out2}

CH3 (magenta) : U_{NP}

CH4 (vert): I_{out2}

MATH (rouge): U_{out1-2}

Temps/div: 10ms

Régions d'application de séquence de vecteurs virtuels

Autres régions : application de contrôle avec fonction courant PN en temps réelle

Figure 13, PERFORMANCE DE CONTROLE PAR HYSTERESIS EN COMPENSATION DE PUISSANCE REACTIVE EN SUR MODULATION [m = 1.1, COS(φ) = 0]

Les transitions entre les différents types de modulation doivent se faire sans difficultés pour permettre le contrôle par hystérésis. Cette propriété peut être observé dans la Figure 13, où les transitions n'ont pas d'impact visible sur les courant de phase (en vert).

1.7 Conclusions

Dans cette thèse, nous avons vu que toutes les topologies multiniveaux peuvent rentrer dans un cadre générique. Une étude comparative a montré que les topologies *à bus continu avec point milieu* ont des propriétés favorables du point de vue des contraintes sur les interrupteurs et sur l'énergie stockée dans les condensateurs flottants. Par rapport à l'état de l'art, les concepts de modulation et de contrôle du PN introduits dans cette thèse élargissent substantiellement le domaine d'application de cette famille de convertisseurs. En conséquence, les convertisseurs multiniveaux *à bus continu avec point milieu* et plus spécifiquement le SMC, ANPC 1 et ANPC 3 à partir de cinq niveaux sont plus robustes que les convertisseurs standards NPC de 3 niveaux. Cette famille de convertisseurs est donc très intéressante pour toutes les applications de moyenne tension.

1.8 Publications et applications de brevets en cours de thèse

[1] C. Haederli, P. Ladoux, T. Meynard, G. Gateau, and A.-M. Lienhardt, "Neutral point control in multi level converters applying novel modulation schemes," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1–8, June 2006.

[2] C. Haederli, "Converter circuit," Patent EP1701436, September, 2006.

[3] C. Haederli and S. Ponnaluri, "Switchgear cell and converter circuit for switching a large number of voltage levels," Patent WO2007087732A1, 2006.

[4] C. Haederli, P. Ladoux, and T. Meynard, "Variable dc link voltage source inverter for reactive power compensation in single phase 25kv ac railway systems," in *PCIM Europe*, PCIM. Mesago PCIM GmbH, 2007.

[5] T. Meynard, A. Lienhardt, G. Gateau, C. Haederli, and P. Barbosa, "Flying capacitor multicell converters with reduced stored energy," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2, 2006, pp. 914–918.

[6] P. Barbosa, M. Saeedifard, P. Steimer, and C. Haederli, "Space vector modulation control of a seven-level hybrid converter," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 4487–4493, June 2008.

1.9 Contributions significatives de cette thèse

- Introduction d'une structure générique pour la représentation, l'analyse et la synthèse des convertisseurs multiniveaux
    - La plupart de topologies connus rentre dans cette structure générique
    - Des nouvelles topologies sont introduites à partir de cette structure générique
- Plusieurs convertisseurs multiniveaux sont comparés sur la base de plusieurs critères, et notamment :
    - Du point de vue des contraintes en tension et courant sur les interrupteurs
    - Du point de vue de l'énergie totale stockée dans les condensateurs flottants
- Investigation de propriété de convertisseurs *a bus continu a point milieu*
    - Exploration des états redondants et introduction des vecteurs virtuels pour le 5-L ANPC type 1
    - Représentation du courant PN, en fonction de la tension homopolaire et θ afin de définir des nouvelles lois de commande.
- Introduction des nouveaux modulateurs et concepts de contrôle pour le courant PN
    - Injection d'une tension homopolaire à base de la fonction de courant PN en temps réelle, y compris l'injection d'un 6ème harmonique. Utilisable pour toutes les topologies de la famille *bus continu avec point milieu*.
    - Modulateurs spécifique pour le SMC et le ANPC 3 avec un élargissement significatif de la capacité de contrôle du PN
    - Modulation avec des séquences de vecteurs virtuels pour le ANPC 1 offrant beaucoup plus de capacité de contrôle pour le PN
        - Définition des régions d'existence des vecteurs modifiés et virtuels
    - Optimisation en ligne des séquences de modulation avec une bonne performance au niveau de pertes et de la distorsion harmonique de la tension de sortie
- Application de concepts multiples par un contrôle à hystérésis.

2 INTRODUCTION

This thesis is about the analysis and synthesis of ML-VSC (multi level voltage source converters). New ML (multi level) topologies and topology specific control techniques for converter internal quantities are introduced and evaluated, namely in the area of voltage control for the DC link and flying capacitors. The main focus is on 3-L DC link converters, a family of converters with good operational performance and reasonable resource requirements. The operating ranges regarding modulation depth and load angle are investigated for various topologies in this family and the impact of the new control and modulation schemes is demonstrated.

ML converters are used extensively in various industrial applications. They are the backbone of a significant part of ABB's (Asea Brown Boveri Corporation) business, namely in the area of MV (medium voltage) and HV (high voltage) applications. It is of high business relevance to find the best suitable topologies and secure the IP (intellectual property) in the field. Any given topology has operation and control requirements. Limits of operation are not always evident for new circuits and suitable control schemes need to be developed to make best use of the PE (power electronics) hardware and push the operating range to the theoretical physical limits. Therefore, the synthesis of new circuits and control schemes, the analysis of performance and operational limits, and the comparison with the state of the art are crucial.

2.1 Thesis structure

The starting point and main problem to be studied in this work on ML converters is the NP (neutral point) balancing problem of the 5-L ANPC. One of the key questions is, whether the 5-L ANPC and the 3-L NPC (neutral point clamped) converter (referred to as NPC in the remainder of the document) differ regarding NP controllability and operating range, or whether they behave the same and thus one can make use of all concepts published for the NPC. The NP balancing problem of the NPC has been investigated extensively by industry and academia. There are a large number of publications on the NPC covering NP control methods, natural balance, stability analysis as well as investigation of operational limitations. The 5-L ANPC (active neutral point clamped) converter [7] has been investigated much less, due to its relatively recent introduction in 2005. Hardly any publications can be found in the scientific literature (Status of 2008).

Based on the main problem statement and the opportunities for original contribution indentified in the first phase of the thesis work, the scope of the thesis has been widened to the synthesis of new ML converter topologies and also to an investigation on the properties of 3-L DC link converters in general including for example NPC and SMC (stacked multi cell converter). The term 3-L DC link converters refers to a whole family of converters featuring a DC link supply with 3 levels (DC+, DC- and NP) and a converter stage generating 3 or more output levels, e.g. by the use of flying capacitors.

2.1.1 Synthesis and analysis of ML converter topologies (chapter 3)

Many different ML topologies have been presented in the literature. There have been a few publications putting different converters in a common framework (e.g. [8]), but with limited scope. The approach in this thesis is to go one step further, unifying all major ML topologies in the same

framework and allowing for systematic synthesis of new topologies. There is an increasing number of different ways to design a ML converter when going to higher numbers of levels, which allows applying various criteria for the choice of the most suitable solution. Different applications have different criteria with the consequence that there is no single best topology but groups of suitable topologies for a given application.

The ML converters proposed in this thesis have different arrangements of capacitors and switches. This leads to different operating limitations. Control of internal quantities like capacitor voltages may only be achieved in a limited range of output voltage amplitude and cos(φ). Such limitations may be defined by the circuit physics or imposed by a chosen control scheme. In addition to the theoretically feasible operating range, there is the aspect of robustness. The NP controllability under disturbance conditions, input current distortion or supply unbalance can differ significantly depending on the chosen topology and control scheme. Different topologies may give the same output voltage waveform, but commutation schemes may differ. The resulting loss level and loss distribution will not be the same, having a significant impact on efficiency, maximum output switching frequency and power throughput. Other performance criteria need to be analyzed and used for benchmarking of any ML topology.

Two paths in the analysis and benchmarking of ML converters are pursued:

1. General evaluation of ML converters not considering control
2. Focus on 3-L DC link converters with specific control schemes for a more detailed analysis of operating range and controllability

The synthesis of ML converters and a general evaluation are covered in chapter 3. This evaluation of ML converters is done based on a simple set of criteria. These include converter key numbers like the number of components, the required total FC (flying capacitor) energy, semiconductor losses, and maximum apparent output switching frequency. The attractiveness of 3-L DC link converters is demonstrated and the remainder of the thesis is focusing on this family of converters.

2.1.2 Analysis of 3-L DC link converters (chapter 4)

Chapter 4 provides a more in depth analysis of the family of 3-L DC link converters as a basis for the synthesis of control schemes presented in the subsequent chapters. A general analysis of the NP current as a function of output current and switching function is presented, both in the time and frequency domains. The basics of NP and FC control are introduced. Chapter 4 also demonstrates that all NP control concepts used for 3-L converters can also be applied to the 5-L ANPC. However, the higher degree of freedom in the 5-L ANPC allows for new specific control schemes and operation beyond what the NPC can do. Operational limitations determined for the NPC do not necessarily hold true for the 5-L ANPC.

Redundant states of ML converters are of high importance for the control of flying capacitors. A capacitor without a separate supply requires a zero average current to maintain its reference voltage. Preferably, zero average current can be achieved within one modulation period, leading to a minimized voltage ripple in the capacitor. In some cases, this is not possible and control can only be achieved over a fundamental period or a fraction of it, leading to a low frequency voltage ripple (e.g. third harmonic) on the capacitor. The existence and the amplitude of such a low frequency voltage ripple depend on the topology, the operating point and the chosen control scheme. Optimization in that respect has an impact not only on the resulting voltages but can also result in

tighter capacitor dimensioning in the design phase. Charging and discharging of flying capacitors may also be achieved with non-redundant states. This approach may lead to operating limitations, but it can also be used systematically for new control schemes.

2.1.3 Synthesis and analysis of new NP control schemes (chapters 5 and 6)

ML converters need to control both internal and external quantities. External quantities like output current, machine torque etc. can be controlled by appropriate modulation and feedback control schemes. Such methods are application specific and are not treated in this thesis. On the other hand, the control of internal quantities is very topology specific and requires topology specific control schemes, which is the focus of this part of the thesis. Examples of internal quantities are not only capacitor voltages in the DC link or flying capacitors but also include optimization objectives like semiconductor losses (overall losses or loss distribution) or current THD in the capacitors. Control also has an impact on the design of ML converters, e.g. on capacitor dimensioning or required semiconductor blocking voltage.

The control issues dealt with in this thesis have a strong focus on NP control in 3-L DC link ML converters. Chapter 5 introduces new NP control schemes with CB (carrier based) PWM (pulse width modulation); chapter 6 introduces new NP control schemes based on SVM (space vector modulation).

2.1.4 Application and experimental verification (chapter 7)

Selected findings throughout the thesis have been experimentally verified. The most important topologies and control schemes have been tested with low power prototypes. Experimental verification of the proposed concepts is important as simulation is not likely to capture all aspects of a real world system. The following issues often differ between simulation and hardware implementation:

- Delays in the control loop including current sensing and gate drivers
- A/D and D/A conversion, delays, noise, and resolution
- General disturbances and environmental noise
- Algorithm execution times in the CPU and FPGA

It is not obvious that more complex control algorithms can run on a given control platform, especially in the case of algorithms requiring significant calculation time. Only prototyping can prove feasibility of the implementation. Experimental verification of the new control schemes is partially covered in chapters 5 and 6 where the basic waveforms are shown. Chapter 7 relates the ML topologies and the control schemes to specific operating conditions. This chapter also proposes a combination of several different control schemes introduced in this thesis within a hysteresis controller. Experimental verification in various operating conditions demonstrates the performance of the NP control schemes.

2.2 Applications background

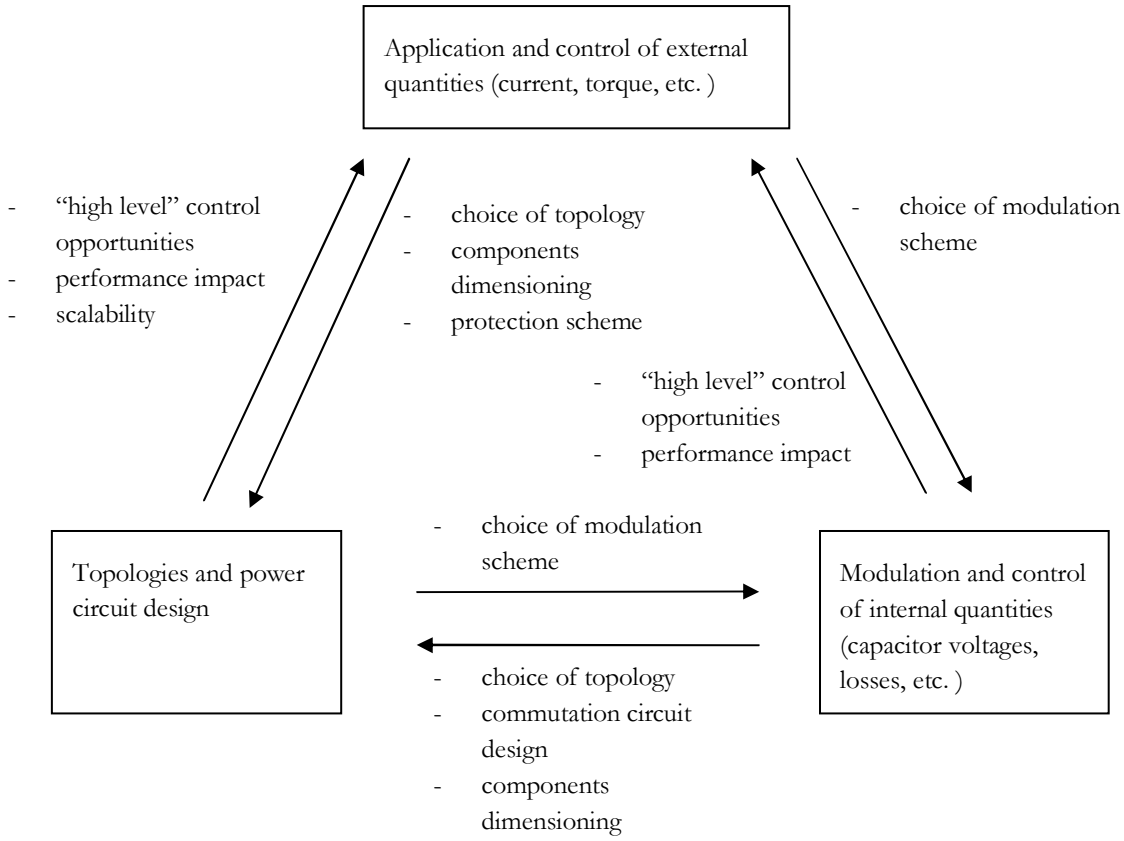


Figure 14, Application – Topology – Modulation – Triangle

The starting point for the specification of a PE system is always the application and its requirements, giving the boundary conditions both for design and control of a PE circuit. Figure 14 illustrates the relationship between application requirements, topology, and modulation scheme.

An individual optimization of the system for every application may lead to a multitude of different solutions, which would not be very practical. The aim is to find solutions for topology and modulation that satisfy the requirements of as many applications as possible.

2.2.1 Applications and their requirements

Split DC link ML converters are of primary interest for MV applications. Those applications do require series connection of switching devices due to the blocking voltages available. Furthermore, the highest blocking voltage devices available also feature relatively high switching losses. ML converters using lower voltage switching devices can have lower switching losses and better output waveform quality at the same time. Possible applications range from drives to rectifiers, reactive power compensators and other power system applications. Ideally, a given converter should be able serve a wide range of applications without any major changes to the main circuit and its control. The following table lists generic key applications with their most important features having an impact on the modulation and control of internal quantities.

TABLE 1, OPERATING RANGES AND CORRESPONDING APPLICATIONS

Modulation depth	m < 0.5		m > 0.5	
Load angle	cos(φ) < 0.15	cos(φ) > 0.15	cos(φ) < 0.15	cos(φ) > 0.15
AFE (active front end, line connected) applications				
			Reactive power compensators,	**Active rectifiers, harmonic filters**
NP control challenge			DC CM injection does not work for low cos(φ), standard carrier based schemes yield poor performance throughout the operating range	standard schemes give low NP control capacity for m>=1
Drives				
	Drive at low speed in idle	**Drive at low speed under load**	**Drive in idle**	**Drive under load**
NP control challenge	Very poor performance of standard schemes, but currents are low	Currents may be high in the case of constant torque applications, but standard schemes perform well due to the high cos(φ)	low control range but a drive in idle does not generate large NP currents	standard scheme give low NP control capacity for m>=1
	NP control scheme should introduce as little as possible CM voltage for motor compatibility (to keep bearing currents low)			

Most applications can be referred to one of the stated applications in TABLE 1 at least from requirements point of view. There are other important distinctive requirements of different applications, which have a significant impact on the choice of the modulator and control of internal quantities. TABLE 2 lists a number of such possible requirements.

TABLE 2, REQUIREMENTS AND IMPACT ON MODULATOR

Requirements	**Impact on Modulation**
Harmonic requirements	Choice of basic modulator (PD PWM, SVM, offline optimized, predictive PWM)
CM requirements	CM may be constrained due to earthing schemes or bearing current limitation. There can be a significant impact on the basic choice of the modulator (e.g. CM independent NP control scheme).
Output frequency	Very low output frequency: Instantaneous NP control rather than based on fundamental period. Very high output frequency: high f_{sw} or PD PWM alternative for low harmonics required, SHE
High f_{sw}	Restrictions regarding controller complexity and calculation time.
Low f_{sw} / f_{fund}	Delay between current measurement and pulse pattern application is significant. This needs to be considered namely with the schemes using the real time NP current function. Current prediction may improve performance.
Load perturbation (sags, distortion, unbalance)	Modulator must be capable of coping with load perturbations while keeping the NP balanced.
Control dynamics	To get high control bandwidth either a high switching frequency is required or a hysteresis type of controller needs to be applied. In any case, delays caused by the modulator should be minimized, which is easier to achieve with simple schemes.
Type of components and commutation schemes	The switching losses depend highly on the type of switch used. So does dead time and minimum on time. Topologies with high level of redundancy (e.g. ANPC 3 or SMC) should take this into account to determine an optimal modulation scheme keeping the losses in the system balanced.
Exception handling	In the case of short circuit (external or internal) or component failure, any converter should be able to safely shut down. Any modulation scheme needs to be compatible with the required exception handling sequences. This means primarily that the modulator shall not generate any states that would lead to immediate destruction of components in case of an exception, and it shall be able to switch over the exception handling sequence at any time.

2.3 Glossary

Note that this glossary only contains expressions that are either introduced by the author or expressions considered ambiguous.

TABLE 3, DEFINITION OF EXPRESSIONS

Expression	Explanation
3-L DC link ML converter	A family of converters with any number of levels starting from three. The "3-L" in the expression is referring to the number of levels in the DC link only: U_{DC-}, U_{NP}, U_{DC+}
ANPC (type) 1	ANPC converter with flying capacitors in the output converter stage only (common for upper and lower DC link)
ANPC (type) 2	ANPC converter with flying capacitors in DC link converter stages only (separate for upper and lower DC link)
ANPC (type) 3	ANPC converter with flying capacitors in all three converter stages (two adjacent to the DC link, one at the output)
Apparent output switching frequency	Frequency of switching actions observed at the output of the converter per phase (excluding glitches). This is not equal to the sum of the average cell frequencies, as multiple cells may switch at a time.
Average switching function $\bar{s}(t)$	Average value of the switching function over one modulation period (continuous function from -1 to 1). This value is equal to the output reference value if such a reference is used and is therefore a direct indicator of the output voltage (without correction according to actual DC link and flying capacitor voltages). For the 2-L converter, the duty cycle of the output half bridge could be used instead (0 to 1). For ML converters, there is no equivalent duty cycle with direct physical meaning (linked to a switching cell). However an equivalent phase leg duty cycle from 0 to 1 can be defined. The use of the average switching function is preferred in this thesis, due to its intuitive physical meaning and its good usability in equations.
CM Average switching function	Common mode average switching function. This equals to the average of the average switching function of all phases in a multiphase system. Consequently, it can range from -1 to 1 for m=0 and is physically constrained to smaller values for m>0.
Duty cycle	Ratio of on time versus total time of a switching cell (variable α used in this thesis) or a switching device (variable *d* used in this thesis) over one modulation period. It can also refer to the relative output voltage of a phase leg referred to the DC- potential (α_L used). However, such a duty cycle is not necessarily linked to a physical duty cycle of an individual device and its use in this thesis is very limited (see also above).

Modulation depth m	Output level reference in a 3 phase system. A DC value for modulation depth leads to sinusoidal operation of the converter.
NP control capacity	Average max. NP current minus average min. NP current over one fundamental period. This value is a measure for the controllability of the average NP current, thus NP control capacity
Optimum modulation	ML modulation scheme where only single level step changes are applied. This can refer to phase voltages or to the DM voltage in multi phase systems. Optimum modulation schemes typically have lower output voltage distortion than non optimum modulation schemes for a given switching frequency. Also switching losses are typically lower (topology dependent). Figure 15 (b) gives an example of an optimum modulation single phase waveform. Note that this term does not refer to the optimization of any specific quantity and includes a wide range of possible modulation schemes.
Partial MC converter	Subset of components in a split DC link ML converter forming an MC converter. Such a converter can be nested or overlapping with other parts of the converter. Components can also be shared with other partial converters.
Switching function *s(t)*	Instantaneous time dependant signal between -1 and 1 defining the output level of a converter phase leg. This signal can assume only -1 or 1 in 2-L converters, -1, 0 or 1 in 3-L converters etc.
Total (semiconductor) blocking voltage	Sum of blocking voltages of a defined set of devices (e.g. all IGBT's or all diodes in a converter)
Total IGBT blocking voltage ratio	Sum of blocking voltages of all IGBT's in a converter divided by the total blocking voltage required to block the DC link nominal voltage once. This corresponds with the total blocking voltage of one arm of a half bridge. Example: half bridges, MC converters and cascaded H-bridges have a total blocking voltage ratio of 2.
Zero NP-voltage-offset operating point	Operating point on the NP current as a function of CM for zero NP voltage offset. Or in other words: the CM value (and its associated NP current) that will be applied in the case of zero NP voltage error for a given strategy. This can be the point with minimum NP current, zero if possible. However, it doesn't necessarily have to. A strategy with a non minimum NP current ripple can be chosen instead.

2.4 Nomenclature

Note that this nomenclature is not comprehensive. It contains primarily terms that are either introduced by the author or considered ambiguous. Braces are used in various ways in this thesis, which is described in TABLE 4.

General variables and constants

d	Duty cycle (of an individual component or a specific converter state)
f	Frequency (periods per second, Hz)
k	Generic constant used in various occasions
m	Modulation depth, m=1 refers to maximum sinusoidal line to line voltage if not stated otherwise, this corresponds with m=sqrt(3)/2 for maximum sinusoidal line to neutral voltage and with m>1 for nonlinear over modulation range.
s	Switching function (time domain)
C	- Capacitance - Capacitor - Switching cell - Carrier function
E	Energy
M	- Number of cells in ANPC output stage - Maximum number of cells that can be operated interleaved
N	- Characteristic number corresponding with number of sections (Figure 35) or number of cells of (equivalent) MC converter - Number of cells in ANPC input stage - General numeration
S	- Apparent power - Converter state - Switching function (frequency domain)
T	Time constant
U	Voltage (rms), the letter V is not used
α	Duty cycle (for a specific commutation cell [α_x]or for a complete phase leg [α_L])
ϕ	Current angle (= θ - φ = ωt - φ for sinusoidal operation)
φ	Load angle (= $\theta - \phi$)
θ	Voltage angle (= $\phi + \varphi = \omega$t for sinusoidal operation)
ω	Angular velocity, angular frequency (radians per second)

Subscripts

1, 2, 3 …	Generic numbering of cells, phases etc.
CM	Common mode
DC	DC link
DC+	Upper rail of DC link
DC-	Lower rail of DC link
DM	Differential mode

L	Phase leg quantity, specifically in α_L for the phase leg duty cycle
MP	Modulation period
NP	Neutral point, DC link midpoint
P	Fundamental period
a, b, c	Phase numbering
avg	Average value (over one modulation period)
fund	Fundamental wave value
load	Load quantity
max	Maximum value
min	Minimum value
n	Generic number, e.g. cell numbers 1, 2, 3 etc.
out	Output quantity
p.u.	Per unit value
ref	Reference value
rms	RMS value
sw	Switching
tot	Total
x, y, z	Generic place holders
α	Real axis of stationary reference frame
β	Imaginary axis of stationary reference frame

Superscripts

$\hat{x}$	Peak value of x
$\overline{x}$	Average value of x over one modulation period

Operators

*	Multiplication
$\bullet$	Convolution

Acronyms

ABB	Asea Brown Boveri Corporation
AC	Alternating Current
AFE	Active Front End (Inverter for line applications)
ANPC	Active Neutral Point Clamped (Converter)
CB	Carrier Based (PWM)
CM	Common Mode
CPU	Central Processing Unit
CSPD PWM	Centre Spaced Phase Disposition Pulse Width Modulation (equivalent with CSVM)
CSVM	Centered Space Vector Modulation (equivalent with CSPD PWM)
DC	Direct Current
DM	Differential Mode
DQ	Direct-Quadrature (Coordinates)

DPC	Direct Power Control
DSP	Digital Signal Processor
DTC	Direct Torque Control
FC	Flying Capacitor (Converter), also known as Multi Cell (Converter)
FPGA	Field Programmable Gate Array
FS	Full Semiconductor (Converter)
HFT	Harmonic Flux Trajectory
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Controlled Thyristor
IP	Intellectual Property
LSB	Least Significant Bit
MC	Multi Cell (Converter), also known as Flying Capacitor (Converter)
ML	Multi Level
MLDC	Multi Level Diode Clamped (Converter)
MPC	Model Predictive Control
MPDTC	Model Predictive Direct Torque Control
MSB	Most Significant Bit
NP	Neutral Point, also known as mid point
NPC	Neutral Point Clamped (Converter)
NTV	Nearest Three Space Vector (Modulation)
NWTHD	Normalized Weighted Total Harmonic Distortion
OPCoDe	Optimized Process of Code Development, denotation for the design workflow of the AC 800PEC software with MATLAB/Simulink
PD-PWM	Phase Disposition Pulse Width Modulation
PE	Power Electronics
PEBB	Power Electronic Building Block
PI	Proportional Integral (Controller)
PID	Proportional Integral Derivative (Controller)
PLD	Programmable Logic Device
PWM	Pulse Width Modulation
RMS	Root Mean Square
SHC	Selective Harmonic Control
SHE	Selective Harmonic Elimination
SMC	Stacked Multi Cell (Converter)
SOA	Save Operating Area
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
WTHD	Weighted Total Harmonic Distortion

TABLE 4, USE OF BRACES

Syntax	Explanation
$\{010110101\}_{BS}$	Binary definition of a converter state each bit indicating the state of a switching cell.
$\{181\}_{DS}$	Decimal definition of a converter state.
$\{13\}_{DSa}$	Decimal definition of converter phase leg state.
$\{13 - 7 - 3\}_{DSa}$	Sequence of converter phase leg states.
$\{231\}_{3D}$	3-D space vector in abc coordinates
$\{120\}_{2D}$	2-D space vector using abc coordinates but referring to any vector with the same $\alpha\beta$ coordinates.
$\{234 - 224 - 223\}_{3D}$	Sequence of 3D space vectors generated by a modulator
$\{324 - 102\}_{MV}$	Modified vector
$\{310 - 431\}_{VV1}$	Virtual vector type 1
$\{410 - 430\}_{VV2}$	Virtual vector type 2
$\{C_1C_2C_3C_4\}$	Order of phase shifted carriers

2.5 Additional remarks

Some of the topology graphs in the beginning of the thesis include legends for GND, supply voltage and output voltage. This is omitted for the majority of graphs in the remainder of the thesis for simplicity. The same definitions also apply for those graphs.

3 ML CONVERTER TOPOLOGIES

This chapter introduces the most important existing ML topologies and puts them in a generic framework. This can then be used to study similarities and differences between different topologies and it can also be used to systematically come up with new circuits. The most important ML topologies are compared based on a set of criteria, including capacitor and semiconductor requirements. Different operating conditions (electrical and thermal limitations) are considered for the calculation of flying capacitor energy.

3.1 Multilevel Converters Background

Voltage source converters use switches (e.g. IGBT's or IGCT's with anti parallel diode) to connect an output port to at least two different supply voltages. Intermediate output voltages can be approximated by a PWM with a suitable duty cycle. ML converters can generate at least three distinct output voltages and can thus approximate an intermediate voltage with a lower THD (total harmonic distortion) than standard two level converters.

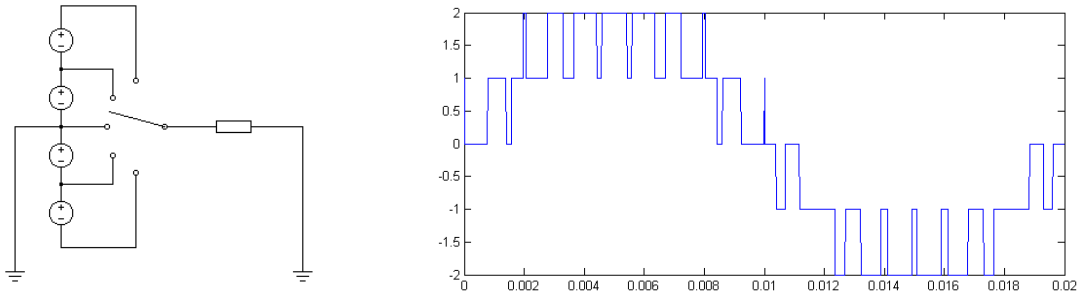


Figure 15, Generic 5-L converter with corresponding output voltage waveform

ML converters allow for reduced switching losses, reduced current distortion or reduced filter size. Therefore, a significant impact on system performance, size and cost can be achieved. Another interesting property of ML converters is the use of series connected switches. This allows for scaling up in voltage for a given switching devices (with a given blocking voltage) or it allows for a reduced blocking voltage device with a given output voltage.

ML converters have first been introduced in the form of cascaded converters in the 1960's. The NPC has been introduced independently by Baker and Nabae, Takahashi, Akagi. Baker was first to protect the circuit in 1979 ([9] patent filing date, patent published in 1981) whereas Nabae et al. first presented the same structure in 1980 [10]. The NPC is still the most widespread multilevel converter topology today (Figure 16 a). It is documented in various theory books and scientific publications. Many other ML topologies have been proposed in the mean time. [11] And [12] give a nice overview. The most recent innovations in the field of ML converters include the ML-ANPC converter proposed by Barbosa, Steinke, Steimer and Meynard (Figure 16 b) [7], the SMC (stacked

multi cell) converter by Gateau, Meynard and Foch (Figure 24 b, [13, 14, 15]) and the M²LC (modular multi level converter) proposed by Marquardt, Lesnicar and Hildinger (Figure 27, [16, 17]).

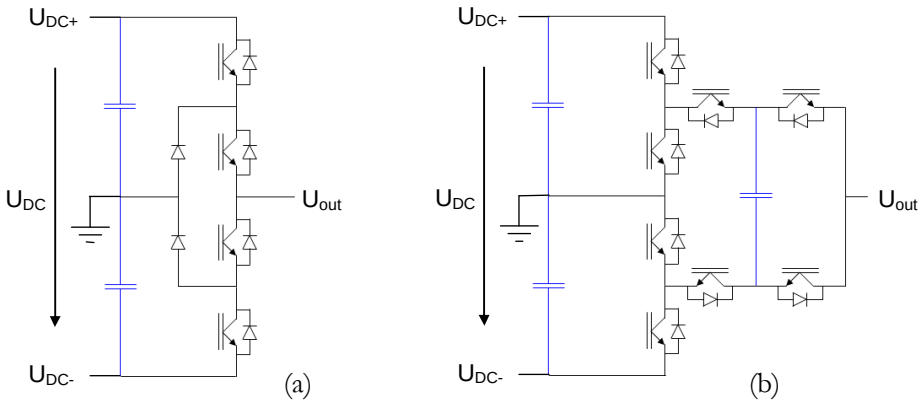


Figure 16, 3-L NPC converter and 5-L ANPC converter

3.2 Basic concepts used in ML converters

ML-VSC's are built from one or multiple voltage sources, a number of capacitors and a number of switches connecting input and output. Multiple current paths are provided to choose between different voltage levels. Two basic concepts are used in all topologies to generate output voltage levels:

- Voltage selectors as sketched in Figure 17 (a); also the 3-L NPC (Figure 16) is a simple voltage selector
- Series connection of voltage sources or switched capacitors (or flying capacitors) as sketched in Figure 17 (b)

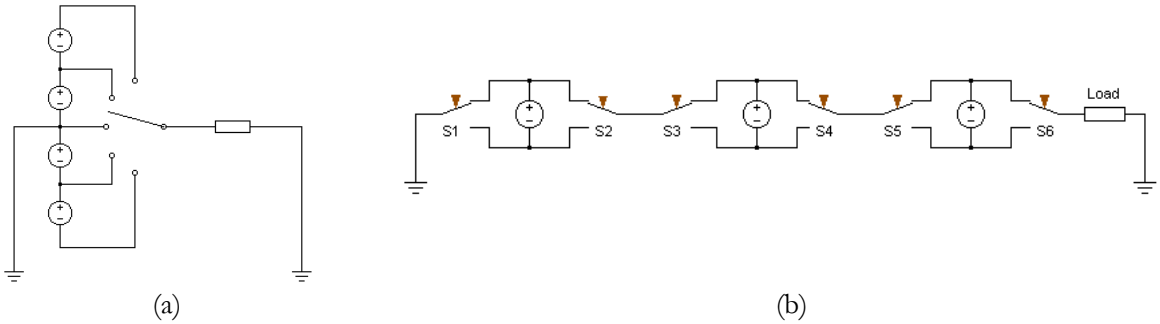


Figure 17, Basic multilevel generation concepts: voltage selector (a) and series connection of voltage sources (b)

Both concepts require either multiple supplies (e.g. cascaded H-bridges [18]) or they can apply capacitors (e.g. MC converter [19]), which need to be controlled. The two concepts can also be combined in a single converter, which can be illustrated with the 5-L ANPC [7] in Figure 16 (b).

The four switches connected to the DC supply constitute a 3-L voltage selector. The four switches on the output side can optionally series connect the flying capacitor. As the flying capacitor is controlled to one fourth of the total DC link voltage, a total of five output levels can be generated.

Output levels can be changed by commutations from one current path to another. The parts of the currents paths that are not shared form the commutation loop. Commutating from one path to the other corresponds with a current reversal in that loop. The commutation is initiated by the turn on or the turn off of the active device (e.g. IGBT, IGCT, MOSFET), so that the current is commutated between that device and a corresponding diode. Commutation loops can be rather complex or very simple. Compact commutation loops keep the stray inductances small and allow for fast switching with limited turn off voltage peaks on the switching devices.

3.2.1 Switching cell concept

The switching cell concept helps for both synthesis and analysis of converter structures. A switching cell is essentially the sum of all component in a given commutation loop. ML-VSC's can be assembled by a combination of multiple switching cells. This may be either by simple connection of switching cells or by building more complex structures with nested or overlapping cells. In the latter case, the actual switching cells are less obvious; however, the basic operating principle with predetermined commutation loops remains always the same.

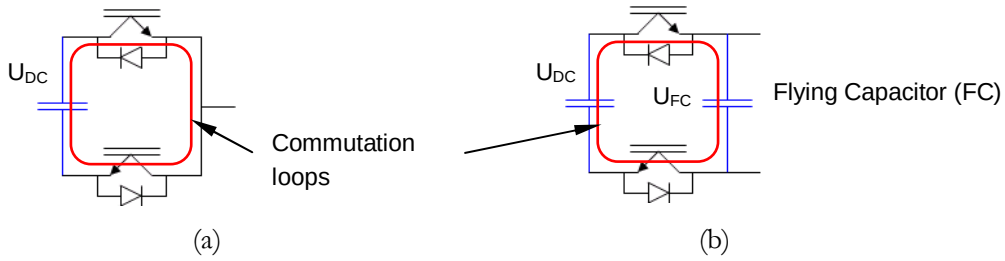


Figure 18, Basic switching cells: 2-L half bridge cell (a), flying capacitor switching cell (b)

The most important switching cells used in this document are the half bridge cell (2-level converter) and the flying capacitor cell as shown in Figure 18. The half bridge cell simply commutates between upper and lower branch and thus generates a 2 level output. The flying capacitor switching cell also has an input voltage and two adjacent switches, but instead of connecting those switches directly, there is the flying capacitor placed in between. Consequently, the flying capacitor switching cell is a 4-pole. The two output potentials on the flying capacitor are either U_{IN-} and (U_{IN-} + U_{CF}) or (U_{IN+} – U_{CF}) and U_{IN+}; they can further be connected to subsequent switching cells like a half bridge cell or another flying capacitor cell.

3.3 Fundamental converter types

3.3.1 Diode clamped converter

The NPC as shown in Figure 19 (a) contains two switching cells, one for the upper capacitor and one for the lower capacitors. The two cells share components and have overlapping commutation loops. Furthermore, there are different commutation loops for different current polarities (green for positive output current, red for negative output current, only upper DC link commutations shown). The loop for negative currents includes more series components and is thus more difficult to design for low stray inductance. The concept of the NPC can be extended to more levels by adding more intermediate points in the DC link and clamping those points with diodes to the appropriate active switch nodes (e.g. 4-L MLDC, Figure 19 b). The MLDC (Multi Level Diode Clamped) converter has already been included in Bakers patent from 1981 [9].

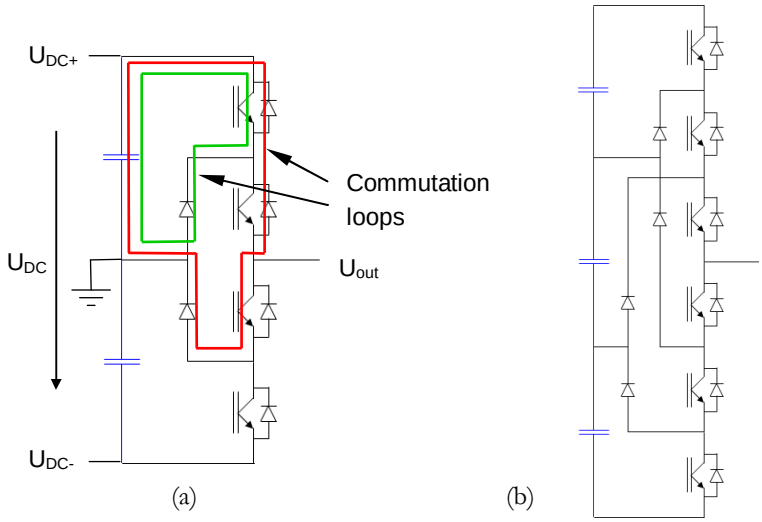


Figure 19, 3-L neutral point clamped converter (NPC) with commutation loops

3.3.2 MC converter

The connection of multiple flying capacitor switching cells and a final half bridge cell results in the MC converter or flying capacitor converter (Figure 20), which has been introduced by Meynard and Foch in 1992. Its design and functionality is presented in [19] and [20]. The circuit shown in Figure 20 is a 4 level converter requiring 3 switching cells and 2 flying capacitors.

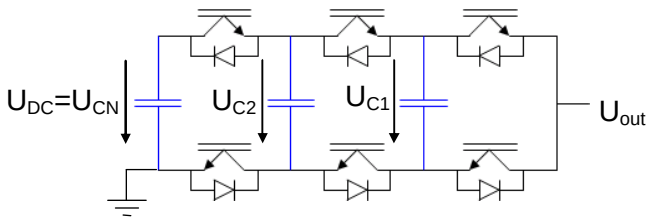


Figure 20, 4-L MC converter

Each switching cell has two possible states: upper switch active or lower switch active, which can be represented by the cell state s_x. The resulting output voltage is given by equation (3).

$$U_{out} = \sum_{x=1}^{N} s_x * (U_{Cx} - U_{C(x-1)}) \quad \text{with} \tag{3}$$

Preferably, capacitor voltages are chosen such that each cell is generating the same output voltage step. This dimensioning results in the availability of redundant states for all intermediate output voltages, which is key for the control of the flying capacitors not having separate supplies. This is the case if condition (4) is met.

$$U_{Cx} = x\frac{U_{DC}}{N} \tag{4}$$

Consequently, the number of available levels equals the number of cells plus one and the output voltage levels can be generated as follows (N: total number of switching cells, n_{active_cells}: number of active cells at a given point in time)

$$U_{out} = (n_{active\_levels})\frac{U_{DC}}{N} \tag{5}$$

The blocking voltage required in any flying capacitor switching cell is given by the adjacent capacitor voltages; only the difference between input voltage and output voltage needs to be blocked by any individual switch. Dimensioning according to (4) allows for all equal switching devices with the same blocking voltage. The concept of the MC converter is very fundamental and the same type of functionality can be found in many of the structures presented in the following paragraphs, even if the corresponding MC circuits may be hidden.

3.4 Generic ML VSC framework

ML converters can be built based on multiple different switching cells, connecting them in various different ways. A large number of different approaches are possible, leading to numerous different topologies. Even though several different types of switching cells are used, it is possible to present most ML-VSC topologies in one generic framework based on generically connected switching cells. The starting point is the generalized multilevel converter that has been presented in 2001 by Fang Zheng Peng [8]. This converter topology contains a maximum of switching cells connected in a triangle. A new way of representation is chosen in Figure 21 to improve the readability and ease the systematic design of new topologies.

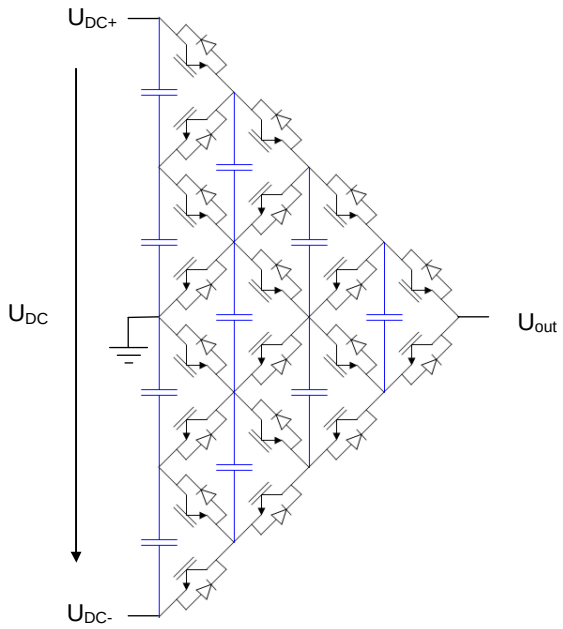


Figure 21, generalized multilevel converter by Fang Zheng Peng

Even though the basic switching cell is the half bridge, it can be seen that the other two types of switching cells are also hidden in that structure. Figure 22 shows the generalized ML converter with highlighted switching cells:

- Half bridge cells (a)
- Flying capacitor cell (b)
- Diode clamped cell (c)

The green paths indicate positive current flow; the red ones indicate negative current flow. The commutation takes place between diodes and IGBT's of the same color. The diode clamped cell does not have common current paths for positive and negative currents. Consequently, the commutation loop is not the same for the two polarities. In fact, the size of the commutation loop for negative current increases with the number of levels implemented in a MLDC converter. Converters based on half bridge or flying cap cells are good in the respect that the switching cell

size does not increase with the number of levels. The different cells can be operated essentially independently from each other from commutation point of view.

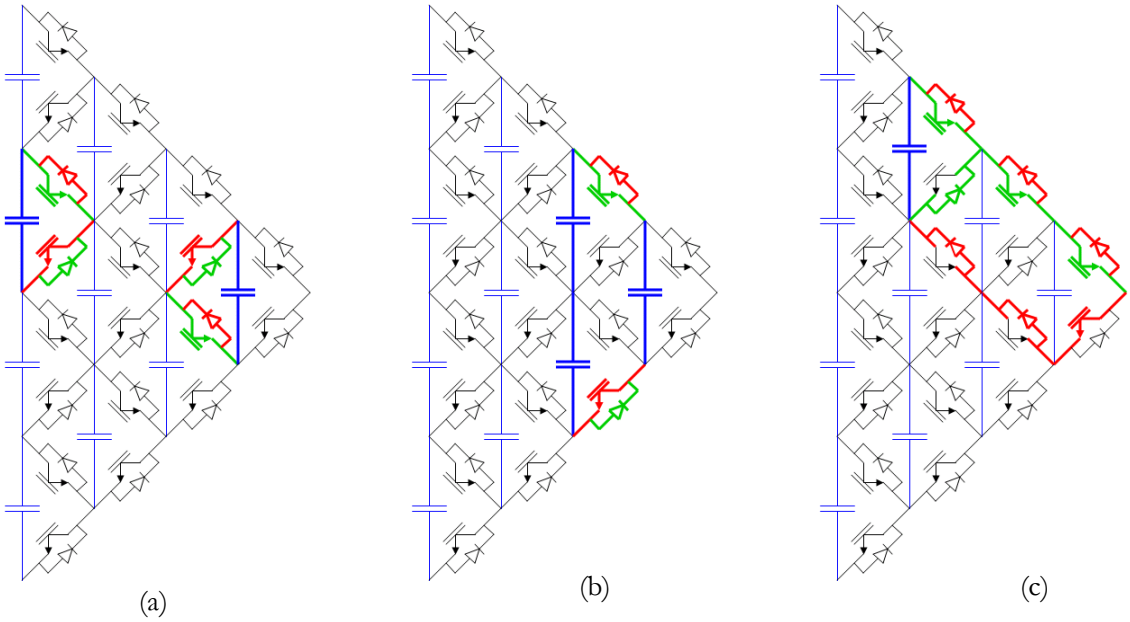


Figure 22, hidden switching cells in the generalized multilevel converter

Fang Zheng Peng proposes to fully implement the generalized ML converter and to operate all of its components. This requires a lot of components and has operational consequences, as capacitors are dynamically paralleled and disconnected again. There may be relatively large currents flowing between capacitors to balance the voltages.

The generalized multilevel converter contains a lot of redundancy that can be reduced by systematically removing redundant components. It has already been proposed by Fang Zheng Peng to reduce the structure to a MLDC or MC converter. However, the concept can be extended much further. The following graphs show that most popular ML topologies fit in the same framework. Note that series connected components without intermediate connection to other devices can be combined into single components. This is not done in the graphs throughout this document to illustrate the required voltage rating for switches and capacitors; the voltage rating is proportional to the number of series connected components.

The topologies presented in Figure 23 exhibit the two basic concepts used in ML converters:

1. Generation of levels by multilevel voltage supply with a selector circuit (MLDC and FS, full semiconductor converter)
2. Generation of levels by using a single voltage source with series connected switched capacitors (MC)

Both solutions need to control multiple capacitor voltages, assuming the MLDC has a single supply with a capacitive voltage divider. The control problem is quite different. Whereas the MC capacitors can be balanced quite easily also for a high number of levels and under all operating conditions, the MLDC has quite restrictive operating conditions and not all combinations of

modulation depth and load angle can be used [21]. The full semiconductor converter in Figure 23 (c) has the same functionality as the MLDC, as it only provides a voltage selector. However, it has a wider selection of possible current paths and can operate with more optimized commutations, reducing over voltages and switching losses. The FS converter can also serve as starting point for new converter topologies as presented in [5].

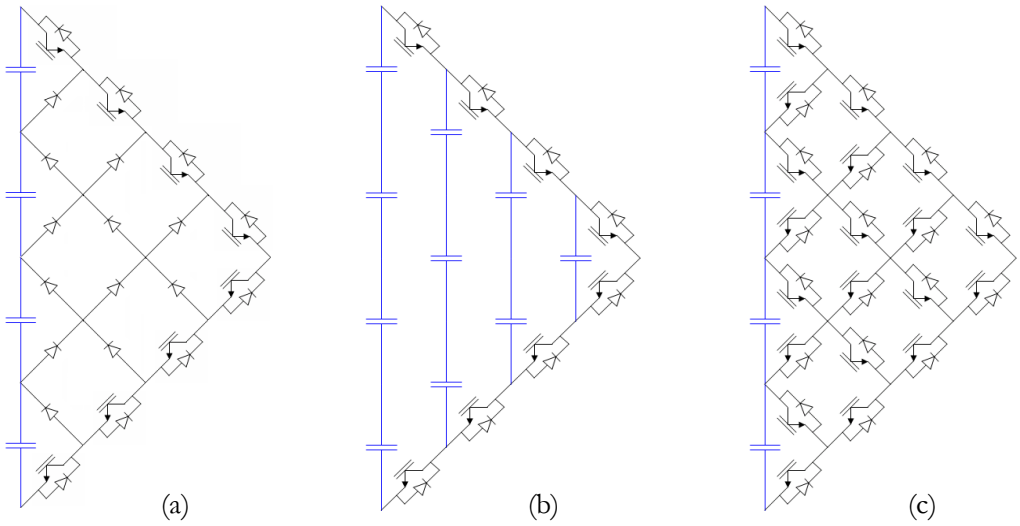


Figure 23, 5-L converter structures: multilevel diode clamped converter (MLDC), multi-cell converter (MC) or flying capacitor converter, full semiconductor (FS) converter

3.5 State of the art ML topologies

The two basic concepts can be combined in alternate converter structures. A multiple supply input can be combined with subsequent flying capacitor stages or vice versa. The following paragraphs present topologies according to the state of the art, fitting in the generic frame, but introduced earlier.

3.5.1 SMC (Stacked Multi Cell Converter)

The SMC has been introduced in 2000 [13, 15]. It uses a multilevel supply voltage; each of the capacitors in the supply has its own MC converter. Those converters are essentially stacked on top of each other as shown in Figure 24, hence the name SMC. The SMC makes use of switching cells and contains a lot of redundancy. This redundancy can be used to improve the control of the mid points in the split DC link supply. This is true namely for the neutral point voltage in the case of the 3-level supplied SMC, as is shown in chapter 1. Figure 24 does not reveal the fact that the two MC converters cannot be stacked directly as shown. The extension of possible output voltages leads to new blocking voltage requirements. Each of the switches in the upper rail and lower rail requires twice the blocking voltage of the simple MC converter. This can be seen much better when using the generic representation in triangle form (Figure 25). This converter is essentially the same as the one in Figure 24, with the only difference that it reveals required switch and capacitor voltages. It also uses an NPC output switching cell (instead of SMC), which uses less active switches.

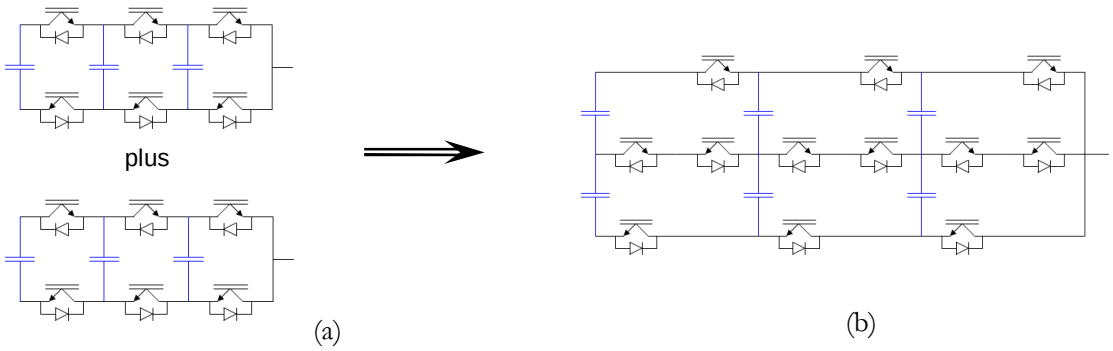


Figure 24, Generation of a 7-L SMC converter by stacking two 4-L MC converters

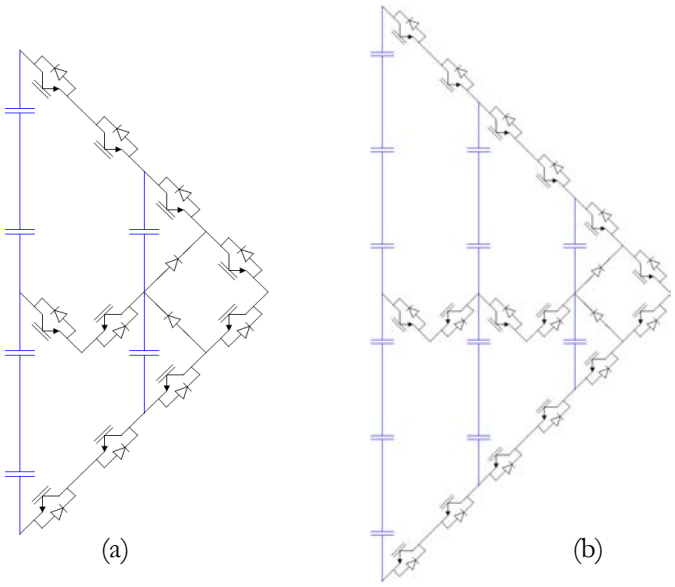


Figure 25, 5-L and 7-L stacked multi-cell converter (SMC)

3.5.2 Multi level active neutral point clamped converter ML ANPC

The ML ANPC is one possible alternative also using a multilevel supply combined with flying capacitors. However, the ML ANPC uses a different switch arrangement and allows for a reduced number of capacitors. The stacked capacitors of the SMC can be combined into a single flying capacitor. Unlike the SMC starting from the MC, the ML ANPC starts from a 3-L ANPC structure (which can also be considered a FS structure). Flying capacitors can be added in three positions in the ANPC: The two DC link switching cells and the output switching cell. The functionality is the same in all cases: both halves of the DC link form a MC converter with some of the capacitors. Figure 26 shows the different topologies possible. The multi cell stages are numbered from 1 to 3 to make general statements on the various possible converter implementations.

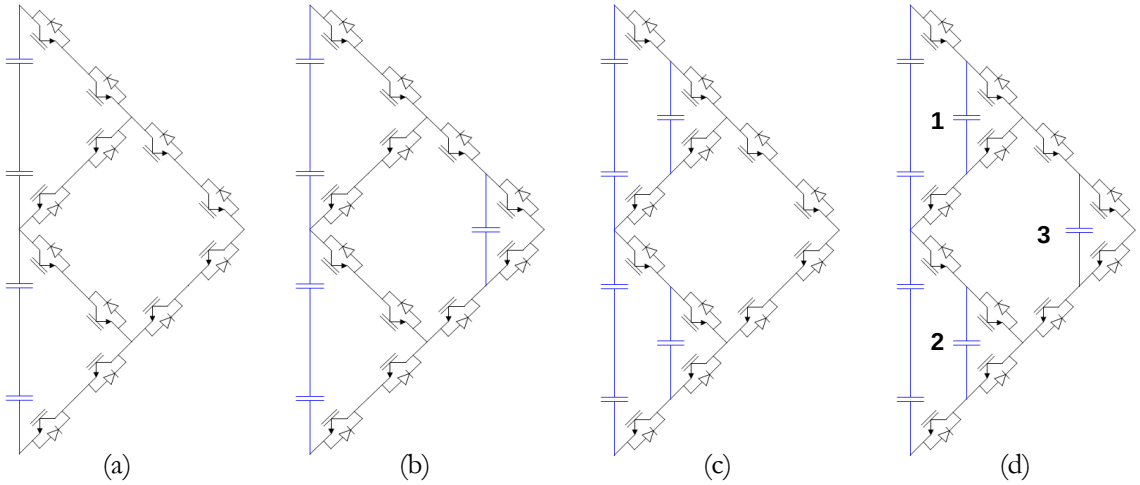


Figure 26, 3-L ANPC (a) and 5-L ANPC type 1 (b), type 2 (c) and type 3 (d)

TABLE 5, FEATURES OF THE GENERALIZED ML ANPC CONVERTER

1. Different number of flying capacitor commutation cells N1, N2 and M for the cells 1, 2 and 3 can be used in a general approach (N1, N2, M all >=1).
2. The number of capacitor required per cell stage is N-1, the number of resulting output levels per stage is N+1
3. Not all switches in a chosen configuration require the same blocking voltage. The blocking voltage depends on the number of cells within one stage. As N and M may be different, blocking voltage requirements may be different. This can be achieved by the application of different devices or by a series connection of switches.

TABLE 6, OVERVIEW OF GENERAL ML ANPC IMPLEMENTATIONS

Cell numbers	Description	Comments
N = M = 1	**3-L ANPC**	**In contrast to the NPC, the 3 level version of the ANPC allows for loss balancing [22].**
N = 1, M >= 2	**ML ANPC type 1** **Figure 26 (b)**	**Minimized capacitor count. The input stages are only used to switch between top and bottom input. High frequency modulation is done in the output stage only.**
N >= 2, M = 1	**ML ANPC type 2** **Figure 26 (c)** **stacked MC converters**	**The DC link stages consist of MC converters. These operate at high frequency modulation. The output stage is only used to switch between the two MC converters. This results in similar operating schemes as for the SMC.**
N = M >= 2	**ML ANPC type 3** **Figure 26 (d)**	**There is increased redundancy, which can be used for control performance or loss distribution. All stages can be operated either individually (to redistribute losses) or all together (to have an impact on the NP current). Interleaved operation allows for higher apparent output frequency, given a maximum device switching frequency.**

N >= 2, M >= 2 N <> M	**Generalized ML ANPC**	**A higher number of output levels are available. The smallest step possible at the output is smaller than the lowest capacitor voltage. Such small steps can only be achieved by simultaneous commutations. Non optimum modulation schemes have to be used in the case of single commutations.**

3.5.3 Modular multi level converter M²LC

The M²LC [17] applies two converter branches per phase leg, one connecting to the positive supply and one connecting to the negative supply. Both branches are made of switched capacitors that can either be series connected or bypassed, thus generating a controllable DC voltage. Both branches can generate the same output voltages and are applied simultaneously. If full bridges instead of half bridges are used in the two branches, an AC input voltage can be applied. Direct ML AC/AC conversion based on such cascaded H-bridges has been proposed by Erickson [23], and by Glinka and Marquardt [24].

Different ways of implementing the individual branches are possible as shown in Figure 27. Graph (a) and (b) show two possible implementations with 2-L half bridges, the AC output of every half bridge connecting to either DC+ or DC- of an adjacent cell. Graph (b) shows one cell at the output shared by both branches, which reduces parts count, but increases the losses in this cell. Graph (c) connects outputs of adjacent cells and also makes direct series connection of two cell capacitors. This may have an impact on the design but is exactly equivalent from operational point of view.

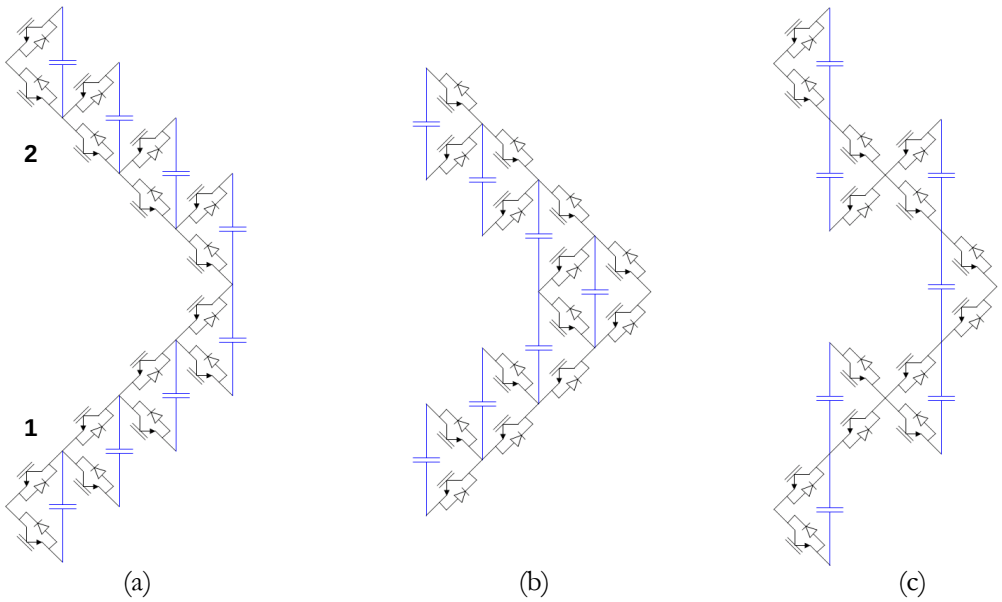


Figure 27, different implementations of the M²LC

The M²LC capacitors can be operated in steady state by maintaining the same average current in all capacitors, independently of absolute current and output voltage. Consequently, all capacitors

will charge and discharge simultaneously and the capacitor voltages stay balanced thanks to the symmetry of the AC output current. Additional control schemes are required to compensate for unbalance generated by any source of disturbance. Such schemes can be found in literature and are not subject of this thesis.

Appendix 9.1 describes the steady state operation of the M²LC. Those calculations result in the following condition for the flying capacitor size (per module, assuming the worst case operating point of m = 0, φ = 0).

$$C = \frac{\hat{I}_{out}}{4\omega\hat{U}_{cap\_ac}} \tag{6}$$

Equation (6) can be used directly for the dimensioning of the M²LC module capacitors (or flying capacitors) for a given maximum voltage ripple.

3.5.4 Other previously published topologies

3.5.4.1 Split DC link and FC based topologies

FC (flying capacitor) cells can be combined in many more ways than indicated in the previous paragraphs. More input levels than three can be chosen and FC cells can be combined quite flexibly with half bridge switching cells. An overview and comparison of possible arrangements is given in [5]. This paper notably discusses the trade off between semiconductors and capacitors and compares the different topologies regarding parts count and total required energy in the flying capacitors. Examples of such converters are shown in Figure 28. A related approach is presented in [6], where a 7-L converter is proposed based on a 4-L DC link with a DC link selector stage and a SMC output stage (Figure 28 a).

TABLE 7, NOMENCLATURE OF GENERAL SPLIT DC LINK CONVERTERS ACCORDING TO [5]

x1y1[*z1]+ x2y2[*z2]+ x3y3[*z3]+…	Topology name
$x_n \in \{FC, SC, FS, SMC\}$	Types of converter stages from DC link to AC output
FC	Flying capacitor converter
SC	Semiconductor converter stage (half bridge form)
FS	Full semiconductor stage
SMC	Stacked multi cell stage
$y_n \in \{1:N\}$	Number of cells in each converter stage
$z_n \in \{1:\infty\}$	Number of vertically stacked cells in each of the stages

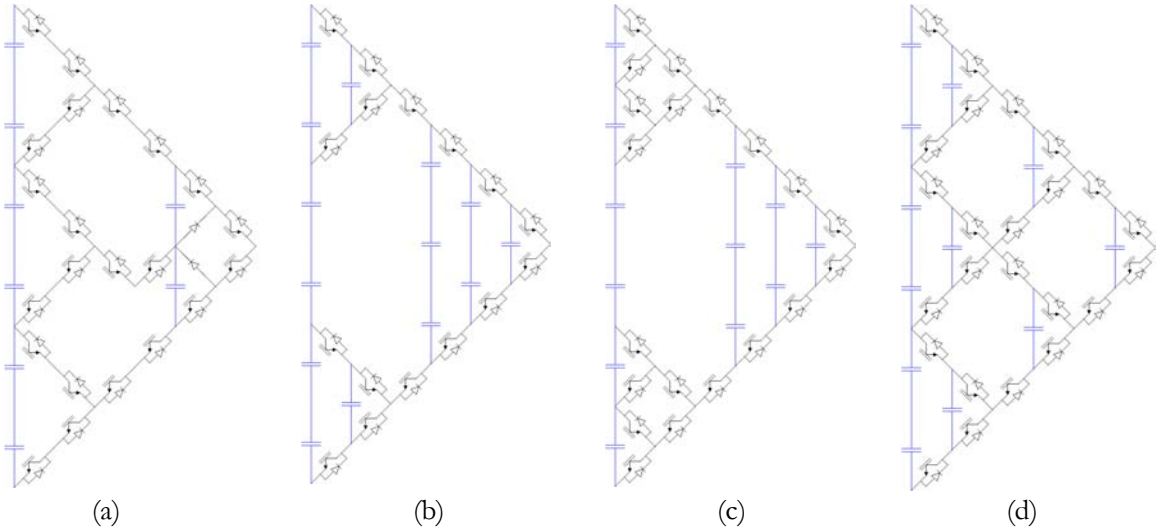


Figure 28, Trade off between flying capacitors and semiconductors in ML split DC link converters, (a) FS1*3 + SMC4, (b) FC2*2 + FC4, (c) FS2*2 + FC4, (d) FC2*3 + FC2*2 + FC2

A large number of different topologies can be designed based on that scheme. This is true especially if various different numbers of midpoints for the split DC link supply is considered. Only a reasonable subset will be included in the subsequent comparison.

3.5.4.2 Cascaded topologies

The cascaded H-bridge converter fits in the generic framework too (Figure 29 [b]). However, multiple supplies are required if active power shall be transmitted (as shown in Figure 29 [b]). The concept of cascading converters can also be used with different type of circuit leading to hybrid topologies. A combination of a VSI with subsequent H-bridges has been proposed by several authors. Examples are the structure without separate supply for the flying capacitor (e.g. by Veenstra [25], Figure 29 [c]) or asymmetric cascaded structures as proposed by Corzine [26] or C.K. Lee [27]. Hashad [28] proposes the use of orthogonal space vectors. The converter structure he proposes is essentially a standard ML converter with a VSI and cascaded separately supplied H-bridges (Figure 29 [c] with separate supply for the flying capacitor).

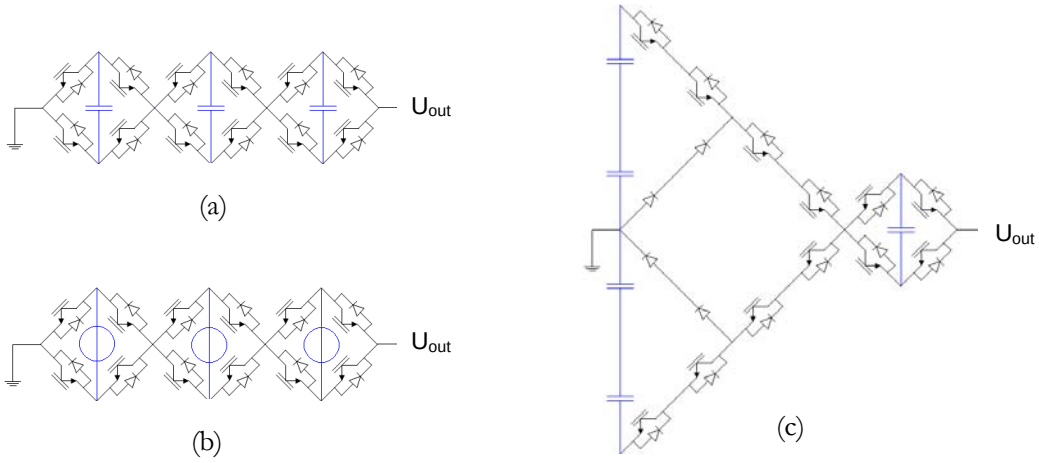


Figure 29, (a) + (b) cascaded H-bridge, (c) hybrid NPC – cascaded H-bridge topology

Cengelci [29] proposes to use VSI converter modules and put them together in new ways to increase output voltage and generate ML performance. This approach seems particularly attractive, as it applies standard 1-ph or 3-ph 2-L converter modules. Wen [30] starts from the same idea and presents a whole family of ML converters resulting from combinations of the basic building blocks.

T. Chaudhuri [31] modifies the ANPC with a common circuit for the three phases. This circuit allows increasing the number of available levels, while keeping the number of switches low.

3.6 Novel 5-L Topologies

The starting point for the invention of new circuits is the requirement that both upper and lower DC link shall be able to operate as MC converter. Based on this requirement and the generic framework, a flexible choice of FC and a flexible choice of switch arrangement are possible.

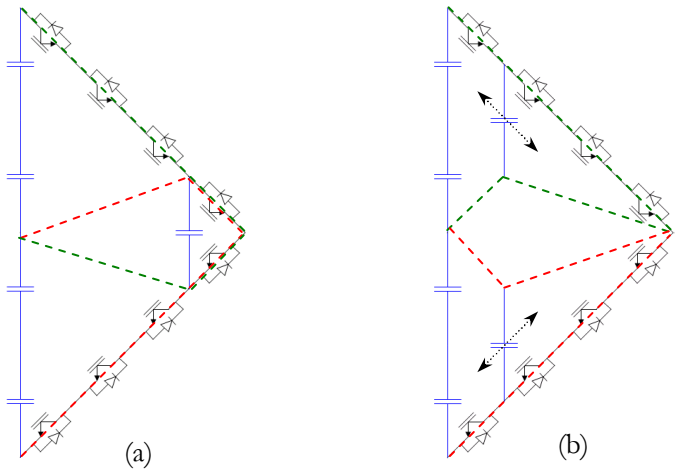


Figure 30, Topology synthesis: placement of flying capacitor, completion of partial MC converter by suitable current paths

Figure 30 illustrates the methodology for the synthesis of new split DC link ML topologies. Figure (a) proposes a shared flying capacitor both for upper (green dotted lines) and lower (red dotted lines) MC converter. Figure (b) proposes separate flying capacitor for the two MC converters. Such separate caps can be positioned along the outer rails of the switch triangle in quite flexible positions (indicated by black arrows). When the position of capacitors is chosen, the switch circuit needs to be designed such that it provides switchable paths along the dotted lines in Figure 30. Note that the upper and lower MC converter (green and red) overlap in Figure 30 (a), whereas they are totally separate in Figure 30 (b). Other capacitor placement can lead to one shared path connecting to the NP. Based on this approach, a number of new topologies could be invented (Figure 31). The functionality of all of them is very similar to standard topologies in spite of the different switch arrangement: Figure 31 (a) has the same functionality as the ANPC 1, with one shared FC. Figure 31 (b) to (e) have the same functionality as the ANPC 2 with an individual FC for upper and lower DC link. This is true both for capacitor dimensioning and control. In the following topology comparison, the ANPC 1 and the ANPC 2 shall also refer to these new topologies; these are not listed individually.

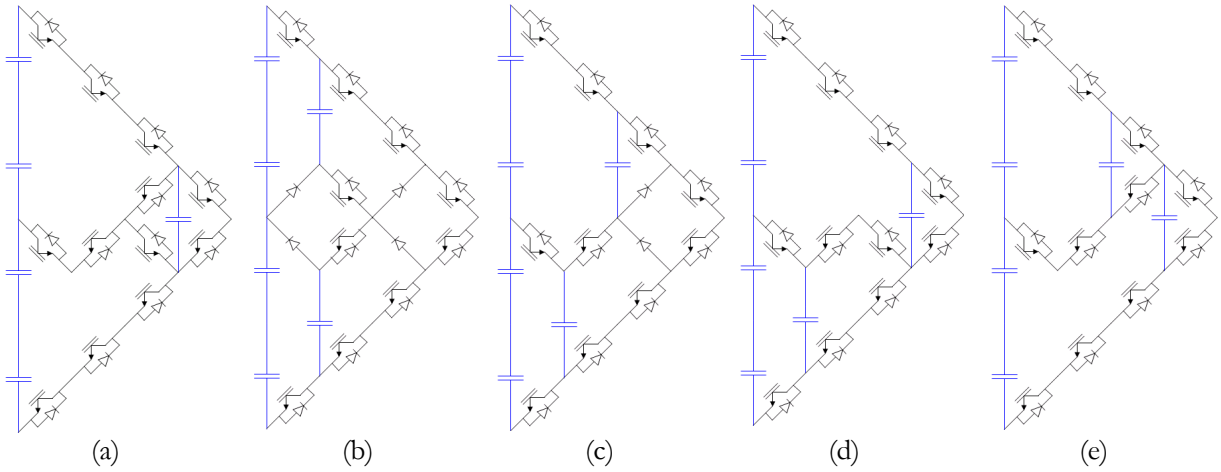


Figure 31, Novel 5-L ANPC variations with different flying cap arrangement

The current paths and switching states for these topologies are not listed here for the sake of brevity. However, they can be anticipated by comparing Figure 30 and Figure 31; Figure 33 illustrates a subset of converter states for Figure 31 (a).

Note that a switch in common path for upper MC operation and lower MC operation can always be replaced by two parallel or quasi parallel paths. For example the circuit in Figure 31 (d) can be transformed into the circuit in Figure 32, now featuring three distinct current paths (SMC type) with a more balanced loading of the switches than the circuit in Figure 31 (d). More ways of implementation are obviously possible (exchanging capacitor positioning in upper and lower DC link, exchanging NPC stage with SMC stage, etc.).

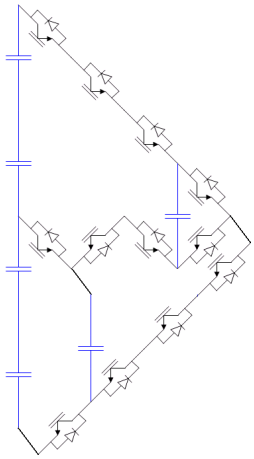


Figure 32, Novel 5-L topology with direct path from NP to output

All these concepts can also be extended to higher level converters, leading to a very vast number of different circuits. Most of them are not really attractive for industrial implementation, as they may be asymmetrical, feature a lot of different commutation loops to be designed and may have highly unbalanced losses. The topologies in Figure 31 (a) and (b) are notable exceptions as they are symmetrical.

3.6.1 Operation of the ANPC 1 variation with backward half bridge

The topology in Figure 31 (a) has a special feature making it interesting for implementation: The transition from upper to lower DC link and vice versa does not have to be done with a 2 level commutation as in the ANPC 1 but can be done with a commutation in the half bridge on the flying capacitor facing the DC link. This results in a very smooth glitch free operation of the converter (as is also the case for the SMC).

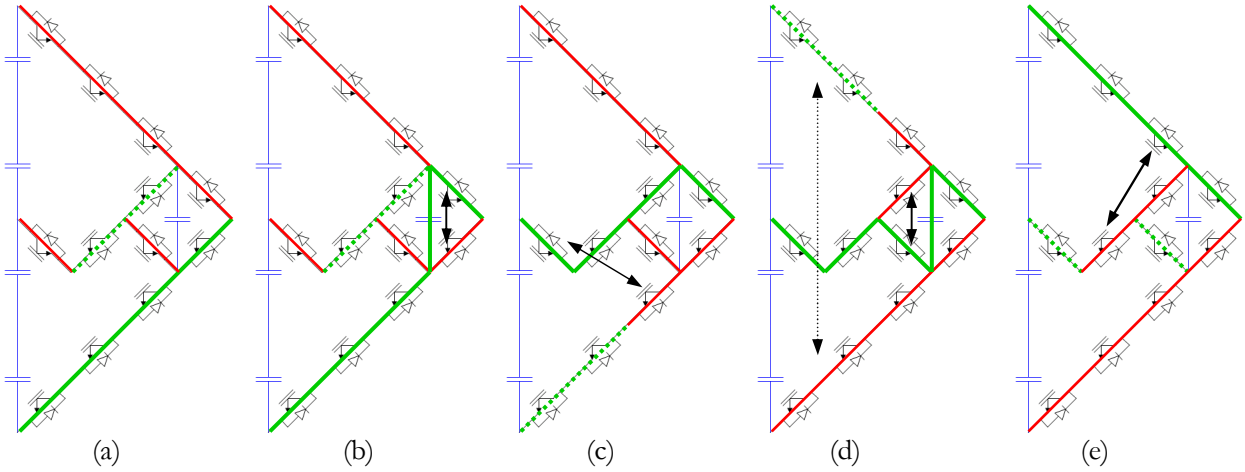


Figure 33, Commutations for the ANPC 1 variation with backward half bridge

A transition from level 0 (minimum output voltage) to level 4 (maximum output voltage) is shown in Figure 33. The commutation from (a), level 0 to (b), level 1 is a standard half bridge commutation of the output cell. The transition from (b), level 1 to (c), level 2 is between one of the switches connecting to the NP and any of the three switches connected to the lower DC link. Only one of the lower three switches is required for blocking during operation of the lower MC converter. The other two switches (indicated by the dotted green line in (c)) may stay on or also turn off. The active switch used may also alter, so that the switching losses are distributed among the three devices. The transition from (c), level 2 to (d), level 3 is the transition changing from lower MC operation to upper MC operation. The commutation is done with the backward oriented half bridge connected to the flying capacitor. This commutation is straight forward and can be done independently of current direction or level. Care must be taken with the outer switches. The following sequence must be used to not apply high voltage on any individual switch:

1. turn off all switches in outer paths (if not already off)
2. turn off conducting switch in backward oriented half bridge
3. turn on blocking switch in backward oriented half bridge
4. optionally turn on two of the outer switches connecting to the DC link (on the new active side of the DC link)

The additional transition of the outer switches does not create any losses as the load current is flowing in the middle path and there is no current in the outer paths connecting to the DC link.

In a practical implementation, the three series connected switches in the outer path do not need to be individual switches, but can be combined into one or two switches with higher blocking capability. If one device with high blocking capability is used and one with low blocking capability, the one with high blocking capability can be operated at fundamental frequency and only the switch with low blocking capability is used for the high frequency modulation.

3.7 Topology comparison

The comparison of topologies is very application specific. The required operating range in modulation depth and load angle φ, the converter voltage and power level, the type of switching device, and the capacitor technology to be used all have a significant impact on any topology benchmarking for a specific application. However, in a generic approach, these parameters are not defined. A thorough comparison for a specific application is a big task on its own, as has been done for example in [32]. A limitation to a set of generic criteria is therefore used in this chapter for a basic topology comparison.

TABLE 8, CRITERIA USED FOR THE TOPOLOGY COMPARISON

Operating range regarding mod index and cos(φ)	- Without considering disturbances
Total blocking voltage of active switches and minimum number of active switches	- Including scaling laws
Total blocking voltage of diodes and minimum number of diodes	- Including scaling laws
Number of parallel current paths	- Including impact on maximum duty cycle and peak current in any given device
Loss distribution	- Qualitative statements on inherent loss distribution and feasibility to control it
Number of input voltage levels	- Generated by series connected capacitors
Number of flying capacitors	- Including scaling laws
Total energy of flying capacitors	- Based on different operational limitations - Peak switching frequency limitation - Average switching frequency limitation - Given apparent output switching frequency
Modularity	- Feasibility of building blocks - Number of switches with different blocking voltage - Number of capacitors with different operating voltage

It is impossible to include all possible variations of ML converters in the comparison. Only converters with single supply (at least per phase) are considered, as other converters like cascaded

H-bridge converters with multiple supplies require a totally different supply scheme with different transformer configurations. TABLE 9 list the specific topologies included in this comparison:

TABLE 9, TOPOLOGIES INCLUDED IN COMPARISON

Single DC link voltage based	- MC (Multi Cell) converter, Figure 23 (b)
Split DC link with any number of midpoints	- MLDC (Multi Level Diode Clamped) converter, Figure 23 (a)
3-L DC link topologies	- SMC (Stacked Multi Cell) converter, Figure 25, refers to 3-L DC link based converters with two stacked MC converters only; high number of stacked MC converters is not considered in the following evaluation - ANPC 1 (Active Neutral Point Clamped) converter type 1, Figure 26 (b), includes the variation with backward half bridge according to Figure 31 (a) - ANPC 2, Figure 26 (c), includes the variations with different capacitor and switch arrangement according to Figure 31 (b) to (e) - ANPC 3, Figure 26 (d)
Topologies according to [5] with combinations of FS, SC and FC stages	- FSx + FCx - FC2*(N/2) + … + FC2, (FC2*x used as abbreviation in tables)
Cascaded structures with single supply	- M²LC

3.7.1 Operating range and number of devices

TABLE 10, OPERATING RANGE OF DIFFERENT ML CONVERTERS

MLDC	MC	SMC	ANPC 1, SCx+FCx	ANPC 2, FCx+SCx	ANPC 3, FCx+FCx	FSx+FCx	FC2 * x	M²LC
m*cos(φ) < 0.5	all	all	all	all	all	all Note 1	m*cos(φ) < 0.5	all

Note 1: may be reduced to m*cos(φ) < 0.5 if all available states are used

TABLE 10 indicates the minimum feasible operating ranges for the considered topologies. All topologies up to 3 input supply voltages can operate at all modulation indices and all cos(φ). Starting from 4 levels, the only guaranteed operating range is below m*cos(φ) = 0.5 (see [21]). In

reality, this limit depends on the exact number of levels and the limit may also be increased by tricks in modulation. However, the full operating range will only be possible if there is a separate unit balancing the input capacitors. This may also be an AFE (active front end) in a VSC in back to back configuration.

The total blocking voltage ratio V_{block} shall be defined as follows ($n_{all\_switches}$ referring to the total number of switches in an implementation with all equal switches and no switch combinations):

$$V_{block} = \frac{\sum_{all\_switches} V_{block\_switch}}{N * V_{block\_switch}} = \frac{n_{all\_switches}}{N} \tag{7}$$

TABLE 11, TOTAL BLOCKING VOLTAGE AND MINIMUM NUMBER OF ACTIVE SWITCHING DEVICES

	MLDC	**MC**	**SMC**	**ANPC 1 SCx+FCx**	**ANPC 2 FCx+SCx**	**ANPC 3 FCx+FCx**	**FSx+FCx**	**FC2 * x**	**M²LC**
V_{block}	2	2	3	3	3	3	N/2 + 2	N/2 + 1	4
Min. No. switches	2*N	2*N	2*N	2*N	2*N+2	3*N	N^2/2 + 2N	N^2/2 + N	4*N

The minimum feasible total blocking voltage ratio for any topology is 2. This value is only achieved by MLDC and MC. All others require a ratio of 3 or more. In case of the FSx+FCx and the FC2*x, the required blocking voltage rises linearly with the number of levels (at a given input voltage), and the minimum number of components rises with a square function. The M²LC requires twice as many components as the MC.

TABLE 12, TOTAL BLOCKING VOLTAGE AND MINIMUM NUMBER OF DIODES

	MLDC	**MC**	**SMC**	**ANPC 1 SCx+FCx**	**ANPC 2 FCx+SCx**	**ANPC 3 FCx+FCx**	**FSx+FCx**	**FC2 * x**	**M²LC**
V_{block}	N+1	2	3	3	3	3	N/2 + 2	N/2 + 1	4
Min. No. diodes	4*N-2	2*N	2*N	2*N	2*N+2	3*N	N^2/2 + 2N	N^2/2 + N	4*N

The blocking voltage and the number of diodes scale the same as the active switching devices except for the case of the MLDC, where the required blocking voltage rises linearly with the number of levels. This is prohibitive already for a relatively low number of levels.

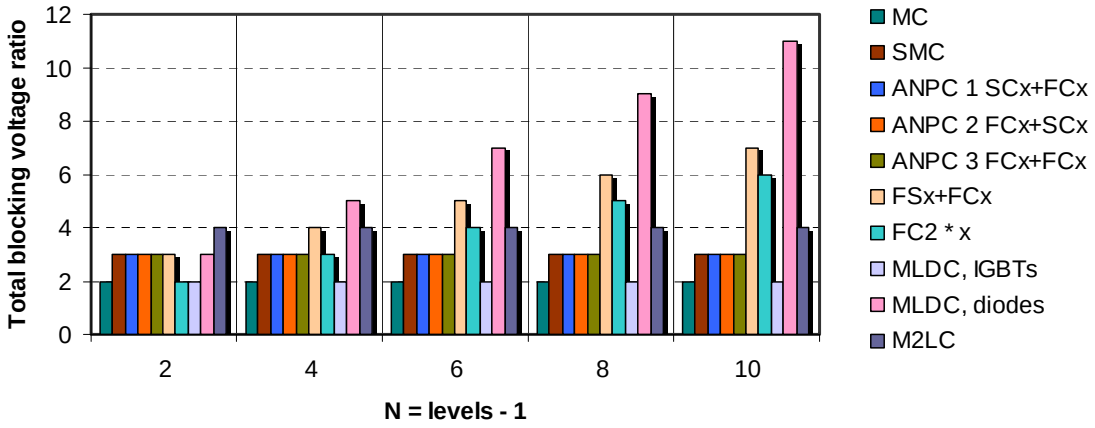


Figure 34, Total sum of required blocking voltages

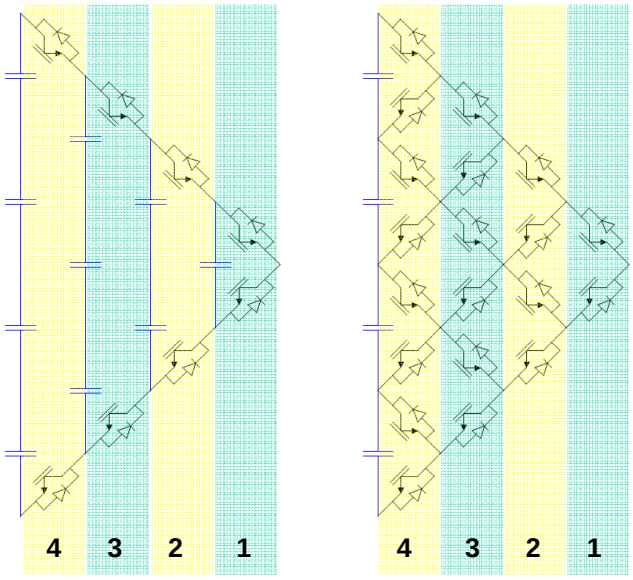
TABLE 13, NUMBER OF SOURCES, LEVELS AND FLYING CAPACITORS

	MLDC	MC	SMC	ANPC 1 SCx+FCx	ANPC 2 FCx+SCx	ANPC 3 FCx+FCx	FSx+FCx	FC2 * x	M²LC
No. of independent sources	1	1	1	1	1	1	1	1	1
No. of series connected input voltages	N	1	2	2	2	2	N	N/2	1
Resulting no. of input levels	N+1	2	3	3	3	3	N+1	N/2+1	2
No. of FC's (k)	0	N-1	N-2	N/2-1	N-2	3*N/2-3	N/2-1	N(N+2)/8	2*N
No. of groups of FC's (p)	0	1	2	1	2	3	1	N(N+2)/8	2*N
No. of FC's per group (k/p)	x	N-1	N/2-1	N/2-1	N/2-1	N/2-1	N/2-1	1	1
No. of cells operating interleaved (M)	x	N	N/2	N/2	N/2	N	N	N	N
Interleave ratio (M/N)	x	1	0.5	0.5	0.5	1	1	1	1

All considered topologies have a single source of supply, which is split into N series connected capacitors. The interleave ratio in TABLE 13 indicates the ratio of number of cells that can be operated interleaved, referenced to the MC. Notably the SMC and the ANPC types 1 and 2 cannot achieve the same interleave ratio in all operating points. Consequently, the duty cycles of the flying capacitor paths are longer, which must be taken into account when calculating the capacitor energies.

3.7.2 Parallel paths, current loading of switches and semiconductor losses

The current from DC to AC has multiple possible paths in any ML converter. Using the generic converter representation according to Figure 21, all converters considered can be divided in N sections (Figure 23).



(a) (b)

Figure 35, 5-L converter topologies with indicated sections: MC converter (a) and FS converter (b)

Each section provides a number of parallel paths. In each active state of the converter, the current is flowing in exactly one of the parallel paths. The individual switches (active switch and anti-parallel diode) are therefore operated with an average duty cycle reverse proportional to the number of paths in parallel. The MC converter (Figure 23 a) has two paths only in all sections, resulting in 50% average duty cycle in all switches. The FS converter (Figure 23 b) has an increasing number of parallel paths in the sections going from AC to DC: 2 paths in section 1, 4 paths in section 2, 6 paths in section 3 and 8 paths in section 4. This leads to very unbalanced average duty cycles between the different sections and also to a very low average duty cycle in section 4, with 12.5% versus 50% in section 1.

Parallel paths may be advantageous or disadvantageous, depending on application requirements and operating conditions. To make general statements on parallel current paths as in TABLE 14, the following design rule can be used: A good design hits current limitations (SOA, save operating area) and thermal limitations for all devices at the same time. In this case, the converter makes best use of the available resources, which is important as the main circuit (switches, bus bars, cooling system) is one of the main cost drivers in power converters. Most of the converter

topologies have differing numbers of parallel paths in the different sections, which complicates the design. A design according to TABLE 14 is not straight forward in this case. Typically, the section with the fewest parallel paths is stressed most and defines the design of the converter. If the same design is kept for the other sections, they will be over dimensioned and not fully utilized. This indicates that it is always better to have one common number of parallel paths in all sections.

TABLE 14, PRO AND CONTRA OF DIFFERENT NUMBERS OF PARALLEL CURRENT PATHS IN ML CONVERTERS

Operating conditions	Few parallel paths (e.g. 2)	More parallel paths
The converter is current limited (e.g. using a high performance cooling system and low switching frequency)	Pro: The few devices can handle the power dissipation.	Contra: The load current is limited by the SOA of an individual switch and parallel paths cannot increase the power throughput.
The converter is thermally limited (e.g. using a standard cooling system and high switching frequency)	Contra: The load current is thermally limited; the devices are operated far away from the SOA and are not fully utilized.	Pro: More parallel paths reduce the duty cycle and thus the losses in the individual switches. The devices can be operated closer to the SOA. The load current and the total power throughput can be increased, keeping the same switch type.

There are strategies to overcome the problem of unbalanced device loading. Suitable modulation strategies may shift switching losses between devices to level out the total losses in all devices. A good example are the active loss balancing strategies for the 3-L ANPC proposed by Brückner [22], where section 1 has two parallel paths and section 2 has four. Inherently, the average conduction loss per device in section 1 is only half of the conduction losses per device in section 2. A suitable modulation strategy allows generating the switching losses primarily in section 2, so that the total losses are balanced. Another example is the use of different device current ratings in the different sections. Even different device types are possible as presented by Steimer et al. [33], where a combination of IGCT's in sections 3 and 4 and IGBT's in sections 1 and 2 of a 5-L ANPC is proposed. In this case, it is possible to fully utilize the devices in spite of the different operating conditions.

TABLE 15, PARALLEL PATH CRITERIA

1.	The number of parallel paths in any given section should be as low as possible, to avoid excessive SOA limitation.
2.	The number of parallel paths in the different sections should not differ by more than a factor of 2 (active loss balancing is only reasonable up to a factor of 2).
3.	For a good dimensioning, all devices should ideally operate with the same thermal load, so that they are stressed the same and all limit the output power together. a. If the loss distribution is known in the design phase, it is possible to choose the semiconductors accordingly and make good use of all the silicon area (in the worst case operating point) in spite of a steady state loss unbalance.

TABLE 16, MAXIMUM NUMBER OF PARALLEL CURRENT PATHS AND PARALLEL CURRENT PATH RATIO

	MLDC	**MC**	**SMC** **Note 1**	**ANPC 1** **SCx+FCx**	**ANPC 2** **FCx+SCx**	**ANPC 3** **FCx+FCx**	**FSx+FCx**	**FC2 * x**	**M²LC**
Max. number of paths	2*N (diodes)	2	3	4	4	4	2*N	N	4
Max. divided by Min. number of paths	N	1	1 (full) 1.5 (NPC output)	2	2	2	N	N/2	1 (full) 2 (shared) output cell)

Note 1: including the ANPC variations in Figure 31 (c) – (e) and Figure 32

The MC provides the most favorable configuration regarding parallel paths and resulting loss distribution. MC converter and cascaded H-bridge converter have inherently balanced losses in all devices; all others have differing current distribution at low and high modulation depth. Also active schemes cannot fully balance the resulting losses. The SMC and its variations also provide a low number of maximum parallel paths and allows for designs with a constant number of paths. All ANPC variations have a higher maximum path number and always include sections with different path numbers. However, the maximum number of paths is constant and does not scale with N as for some other topologies. In addition, the strategies proposed above provide reasonable switch usage by proper balancing of the losses. The M²LC provides a constant number of parallel paths in all sections; on the other hand, the total number of switches is high.

3.7.2.1 Total semiconductor losses

Overall semiconductor losses are very similar in all of the presented topologies for a given average device switching frequency. This can be stated without detailed calculation based on the following two assumptions:

1. The current path is always through N switching devices (as there are N sections, see Figure 23), either active switch or diode, independently of topology. The share between IGBT and diode may vary slightly, but will have no significant impact on the overall conduction losses. All topologies perform very similar in that respect, unless a different switch dimensioning (silicon area) is used.
2. A change of one output level involves a commutation from one IGBT to one diode or vice versa for all topologies. A given output voltage waveform defines the number of commutations for all topologies, resulting in similar overall switching losses for all topologies.

Nevertheless, the considered topologies may vary a lot regarding loss distribution (as presented above) and the total switching losses: The design of different topologies may not be optimized for the same average switching frequency. To minimize capacitance, all cells generating single level steps should be operated at high frequency, whereas cells generating multiple level steps should be operated at low frequency. This means that topologies with a large number of high frequency switching cells are likely to generate higher losses. E.g. the ANPC 3 will generate more losses than

the ANPC 1 if capacitor energy is minimized, and the ANPC 3 will thus generate a high apparent output switching frequency and require less filtering and generate lower filter losses.

The degree of freedom in dimensioning components and choosing modulation schemes (with or without loss balancing scheme) is very high. A comparison of the considered topologies regarding losses is therefore only meaningful if a set of constraints based on a given application is given. As the approach in this chapter is very generic and meant for a wide variety of applications, such a comparison is not done here. A good comparison based on real converter dimensioning can be found in [32] for a number of topologies.

3.7.3 Modularity and Scalability

Modularity can be defined on different levels and in different dimensions. In the context of this topology comparison, the modularity of interest is on the main circuit level. For simple manufacturing and assembly, the main circuit can preferably be built from multiple PEBB's (power electronic building blocks). Several different PEBB's may be necessary to build a specific converter or one type may be sufficient in another case. Clearly, a low number of different building blocks required is best. A PEBB design may or may not simplify scalability of a concept. Ideally high voltage and higher power can be achieved by simply putting more PEBB's in parallel and in series. Unfortunately, this is not possible with all topologies. The only truly modular and scalable topology in TABLE 17 is the M²LC. MC and SMC also provide nice modularity regarding switch arrangement; however, capacitor voltages and isolation requirements vary.

Commutation is an important topic for all topologies. When scaling the concepts to higher voltages, insulation distances become larger and the capacitors have higher voltage rating. This introduces stray inductance in the commutation loops. The implementation becomes more difficult. Topologies using simple commutation loops and topologies using a small number of different commutation loops are therefore preferable, as each different loop needs to be designed carefully. In that respect, the M²LC performs best, as the individual cells can operate at relatively low voltage and all commutation loops are identical. Scalability is clearly best for this topology.

The FC2 * x also applies all identical modules. The voltage can simply be scaled up by putting another row of modules on the DC link side. However, commutation with multiple modules becomes very challenging. All modules make use of the DC link directly, which leads to very large commutation loops when scaling the concept to higher number of levels. The commutation loops could remain constant if additional clamping capacitors are added at each module input. However, this leads to operational problems with potentially large ringing as many capacitors are dynamically connected in parallel. The balancing currents are only limited by stray inductances in this case. Therefore, the scalability is not very good. This is even more emphasized considering that the number of all components is rising with a square function of the number of levels.

All MC based converters have good scalability but share the same problem of increasing capacitor voltages towards the supply side. The problem can be at least partially mitigated by splitting the DC link in two, resulting in the SMC and ANPC topologies. A PEBB based scaling is possible by may prove difficult in a practical implementation.

The MLDC converter has differing commutation loops depending on the direction of the current. The number of components in the commutation loops is also proportionally increasing with the number of levels. Both properties are not desirable and make the implementation of the MLDC for high voltage and current challenging.

TABLE 17, MODULARITY

Topology	Modules with identical structure per phase leg	Number of different modules per phase leg	Switch voltage rating of structurally identical modules	Capacitor voltage rating of structurally identical modules, isolation requirements	Comments, scaling by PEBB series connection
MLDC	1	1	n.a.		PEBB concept is only feasible on the phase leg level. No scaling by series connection of PEBB's
MC	N	1	Same	Different	PEBB concept feasible on the commutation cell level. Geometry according to largest required capacitor. Isolation requirements according to total output voltage. Scaling by series connection possible.
SMC	N/2	1	Same	Different	PEBB concept feasible for a six pole, including adjacent commutation cells in the upper and lower converter path. Geometry according to largest required capacitor. Isolation requirement according to total output voltage. Scaling by series connection possible.
ANPC 1	2 (DC link)	2	Same	Same	The DC link stages may have 2 identical half bridge PEBB's. No direct scaling.
ANPC 2	2 (DC link)	2	Same	Same	The DC link may have two identical MC PEBB's. No direct scaling
ANPC 3	3	1	Same	Same	Similar MC PEBB's can be used, but DC link PEBB's need higher capacitance. No direct scaling
ANPC x	N / 2	n.a.	Same	Different	Individual PEBB's could be used per commutation cell like in the MC converter. Applies also to the FSx + FCx. Scaling is possible but difficult (commutation loop design)
FSx + FCx	2	2	Same	n.a.	The same full semiconductor stage can be applied in the upper and the lower DC link.
FC2 * x	N(N/2+1)/4	1	Same	Same	Identical PEBB's can be used, although the PEBB's making up the DC link may require higher capacitance. Scaling possible.
M²LC	2 * N	1	Same	Same	Identical PEBB's can be used in this topology, applying the same switches and the same capacitors. Scaling possible.

3.7.4 Flying capacitor energy

When comparing the flying capacitor energy, two fundamentally different phenomena need to be taken into account. All MC based topologies can balance the flying capacitors with redundant states. The voltage ripple in the flying capacitors is given by the switching characteristics of the converter. The M²LC cannot be compared to the other converters directly regarding capacitive energy required, as there is a fundamental component in the flying capacitor current and the total energy doesn't depend on switching frequency. For a comparison of MC based converters and M²LC, specific switching frequencies and fundamental frequencies need to be assumed.

TABLE 18, ASSUMPTIONS FOR FC ENERGY COMPARISON

1.	Converters with a given input voltage and a given output voltage range are considered
	a. The choice of a higher number of levels reduces the voltage per level
2.	MC converter stages can operate the individual cells in an interleaved manner
	a. Each cell is operated at $f_{switch} = 1 / T_P$
	b. There is a phase shift of $2\pi / N$ from one cell to another
	c. Cells can be operated such that flying capacitors are only active for T_P / N. In the remaining time of the period, two adjacent cells have the same state and therefore no current is flowing in the flying capacitor
3.	For lowest energy in the flying capacitors, highest possible switching frequency is desired. However, the switching frequency is limited. The following types of limitations are possible.
	a. Peak switching frequency on device level
	i. Imposed by the peak device loss or by gate driver limitations
	b. Average switching frequency on device level
	i. Imposed by maximum average device loss or by gate driver limitations
	c. Apparent converter output switching frequency
	i. Imposed by maximum allowable total converter loss (cooling system limitations or efficiency requirements)
	ii. Load constraints like optimal switching frequency for filter design.

Each of the switching frequency limitations indicated in TABLE 18 leads to different capacitor dimensioning. In a given application, the appropriate type of limitation needs to be considered. The following comparison calculates the capacitor energies for all three cases.

3.7.4.1 Flying capacitor energy for MC based converters

All capacitors within one MC structure are operated with the same duty cycle and all capacitors may have the same absolute voltage ripple (independently of their voltage rating), which means the relative ripple decreases with increasing voltage. This is required to avoid over voltages on the switches of the individual cells. Consequently, all capacitors require the same capacitance C_0. In the case of the MC converter with interleaved operation, the following basic equations apply to all flying capacitors:

$$I_{FC} = C_0 * \frac{\Delta U_{FC}}{\Delta t_{FC}} \tag{8}$$

$$\Delta U_{FC\_\max} = k_1 \frac{U_{DC}}{N} = I_{FC\_\max} \frac{\Delta t_{FC\_\max}}{C_0} \tag{9}$$

With k_1 indicating the allowable maximum ripple ratio in function of the supply voltage and 1/N.

$$\Delta t_{FC\_\max} = k_2 T_{SP} \tag{10}$$

With T_{SP} as switching period time and k_2 indicating the maximum capacitor application time ratio in function of the switching period.

$$C_0 = I_{FC\_\max} \frac{\Delta t_{FC\_\max}}{\Delta U_{FC\_\max}} = \frac{I_{FC\_\max} N k_2 T_{SP}}{k_1 U_{DC}} = \frac{I_{FC\_\max} N k_2}{k_1 U_{DC} f_{sw}} \tag{11}$$

All parameters determining C_0 are either given from the system (I, N, U_{DC}) or can be chosen as operation parameter (k_1, f_{sw}); k_2 depends on the topology. It indicates the largest expected application time ratio of the capacitor before current reversal in the capacitor is possible. The following graph illustrates the maximum capacitor application time ratio in an MC converter.

Flying capacitors are charged or discharged by the corresponding output current, whenever the two adjacent cells do not have the same state. The current bypasses the flying capacitor when the two adjacent cells have the same state (either low or high). Figure 36 shows the example of a 4 cell MC converters with 4 carriers with regular phase shifts ($\pi/2$ between adjacent cells) and 5 sample references. For a given reference, the maximum capacitor application time corresponds with the phase shift between adjacent carriers, which is indicated with the bold sections of the reference lines. It can be seen from the figure that the capacitor application time is constant in the intermediate part of reference and going linearly to zero towards the upper and lower limits. The sign of the current in the flying capacitor can be chosen every time a state using a flying capacitor is applied.

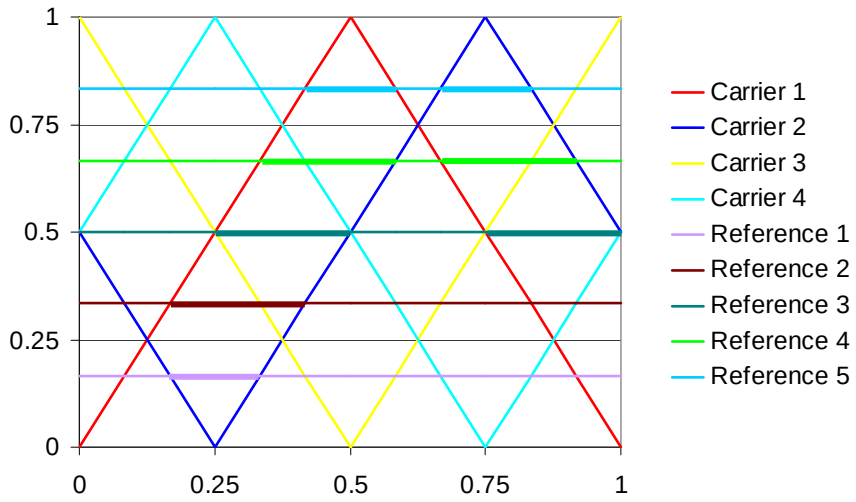


Figure 36, Carrier waveform, sample reference inputs and resulting flying capacitor application times

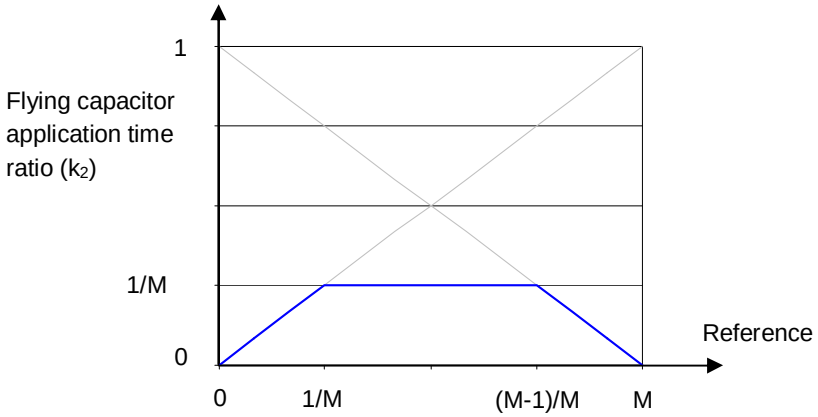


Figure 37, flying capacitor application time

Figure 37 indicates that there is a maximum k_2 of 1/M, M indicating the number of cells that can be operated interleaved. This can correspond with the number of cells within a given MC converter, or it can be a higher number based on series connected MC's or a combination of MC and FS cells. This number M does not necessarily correspond with N for all topologies. N is the ratio of input supply voltage of the converter over one output voltage level (or lowest capacitor voltage), whereas M can refer to only a portion of the whole converter. In the case of the MC converter N equals M; in the case of the SMC or the ANPC1 and ANPC2, N equals 2 times M. The switching frequency may also vary depending on topology and operating point. A factor k_{f_sw} shall be defined to express the actual switching frequency in function of a base frequency corresponding with a pure MC converter operation. Starting from Figure 37, the total flying capacitor energy of all considered topologies can be calculated.

$$f_{sw} = k_{f\_sw} * f_{sw\_base} \tag{12}$$

$$C_0 = \frac{I_{FC\_\max} N T_{SP}}{M k_1 U_{DC}} = \frac{I_{FC\_\max} N}{M k_1 U_{DC} f_{sw}} = \frac{I_{FC\_\max} N}{M k_1 U_{DC} f_{sw\_base} k_{f\_sw}} \tag{13}$$

$$C_1 = \frac{I_{FC\_\max}}{k_1 U_{DC} f_{sw\_base}} = \frac{I_{FC\_\max} N}{M k_1 U_{DC} f_{sw}} \frac{M k_{f\_sw}}{N} = C_0 \frac{M k_{f\_sw}}{N} \tag{14}$$

$$C_0 = C_1 \frac{N}{M k_{f\_sw}} \tag{15}$$

C_0 refers to the actual capacitance required, taking into account the level over interleaving and the applied switching frequency. C_1 is a generic value depending on maximum current, maximum voltage ripple and base switching frequency. It can be seen from (15) that a reduction of the number of cells can be compensated with higher switching frequency. With a total number of k flying capacitors, we get the total energy in the flying capacitors:

$$E_{tot} = \sum_{x=1}^{k} \frac{C_0 U_x^{\,2}}{2} = \sum_{x=1}^{k} \frac{C_1 N U_x^{\,2}}{2 M k_{f\_sw}} \tag{16}$$

A constant shall be defined as follows to compare different topologies without taking into account any absolute values from a given operating point.

$$E_{tot} = K_{E\_cap} \frac{C_1 U_{DC}^{\,2}}{2} = K_{E\_cap} \frac{I_{FC\_\max} U_{DC}}{2 k_1 f_{sw\_base}} \tag{17}$$

(18) follows directly from (16) and (17).

$$K_{E\_cap} = \frac{2 E_{tot}}{C_1 U_{DC}^{\,2}} = \frac{N}{M k_{f\_sw}} \sum_{x=1}^{k} \left(\frac{U_x}{U_{DC}} \right)^2 \tag{18}$$

In the case of p groups of flying capacitors with each group forming a MC, this can also be written as (k/p is the number of flying capacitors per group):

$$K_{E\_cap} = \frac{N}{M k_{f\_sw}} \sum_{x=0}^{p-1} \sum_{y=1}^{k/p} \left(\frac{U_{y+x*k/p}}{U_{DC}} \right)^2 \tag{19}$$

With p identical groups of flying capacitors this results in:

$$K_{E\_cap} = \frac{pN}{M k_{f\_sw}} \sum_{y=1}^{k/p} \left(\frac{U_y}{U_{DC}} \right)^2 \tag{20}$$

In a fully redundant MC converter, the voltage sequence in the capacitors is given:

$$U_y = \frac{yU_{DC}}{N} \tag{21}$$

This can be inserted in the equation above

$$K_{E\_cap} = \frac{pN}{Mk_{f\_sw}} \sum_{y=1}^{k/p} \left(\frac{yU_{DC}}{NU_{DC}} \right)^2 = \frac{p}{MNk_{f\_sw}} \sum_{y=1}^{k/p} y^2 \tag{22}$$

$$K_{E\_cap} = \frac{p}{MNk_{f\_sw}} \left(\frac{(k/p)^3}{3} + \frac{(k/p)^2}{2} + \frac{k/p}{6} \right) \tag{23}$$

$$E_{tot} = K_{E\_cap} \frac{I_{FC\_max} U_{DC}}{2k_1 f_{sw\_base}} = \frac{p}{MNk_{f\_sw}} \left(\frac{(k/p)^3}{3} + \frac{(k/p)^2}{2} + \frac{k/p}{6} \right) \frac{I_{FC\_max} U_{DC}}{2k_1 f_{sw\_base}} \tag{24}$$

Thanks to the parameterization, these equations can be used to calculate the total flying capacitor energy for a wide range of different topologies. The meaning of parameters shall be repeated here for clarity:

TABLE 19, PARAMETER DEFINITIONS

p	number of identical groups of MC converters (non overlapping)
k	total number of flying capacitors
M	number of cells that can be operated interleaved
N	input voltage divided by smallest capacitor voltage (number of cells in pure MC converter)
k_{f_sw}	switching frequency factor to get actual maximum switching frequency from maximum switching frequency that can be used in the MC converter (f_{sw_base})
k_1	maximum allowable voltage ripple ratio $\Delta U/U_N$

Depending on the given boundary conditions different parameters may be used. The following paragraphs list the resulting capacitor energies for three different operating conditions: Operational limitation by peak switching frequency of device, operational limitation by average switching frequency of device and operational limitation by apparent output switching frequency of converter. The corresponding tables are given in appendix 9.2.1.

3.7.4.1.1 Operational limitation by peak device switching frequency

Operational limitation of a converter may be given by the peak device switching frequency. This limitation may be based on two different reasons. The first one being gate driving limitation, for example in the case where IGCT are used. IGCT gate drivers always have limited operating frequency, optimized according to a trade of between cost and performance in its target application.

A second limitation limiting the peak device switching frequency may be peak loss. In normal operating conditions, this will not usually be the case, as the thermal capacitance will be sufficient to allow for an averaging of the switching losses over one fundamental period. However, if the fundamental frequency is very low, for example in the case of zero speed drive operation and a package with relatively low thermal capacitance is used, the allowable peak losses will limit the peak device switching frequency.

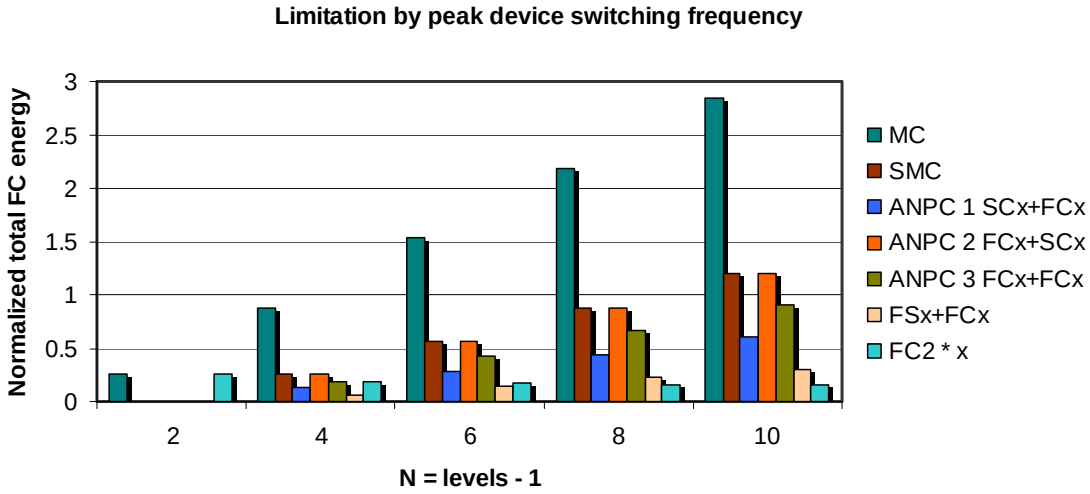


Figure 38, normalized FC energies in peak device switching frequency limitation

In the case of peak device switching frequency limitation, FC2*x requires the least amount of energy for N=8 and above. However, it has multiple input voltages that need to be balanced. The operating range will be limited and a low frequency ripple may appear on the flying capacitors depending on modulation strategy. Also the number of active switches and diodes is very high for those numbers of N. The same applies to the FSx+FCx. From the remaining topologies, the ANPC1 (SCx+FCx) features the lowest required flying capacitor energy with roughly one fourth of the MC converter requirements. For a low number of levels this factor is even higher; less than one sixth of the MC flying capacitor energy is required in the ANPC1 for N=4.

3.7.4.1.2 Operational limitation by average device switching frequency

The average device switching frequency limit corresponds with a limitation by average loss per device. The assumption is in this case that the fundamental frequency is sufficiently high to not generate a failure mode relevant thermal ripple in device and package. This is usually the case for line frequency applications.

The average device switching frequency also determines the converter losses. In case of a given required converter efficiency, this type of limitation also applies.

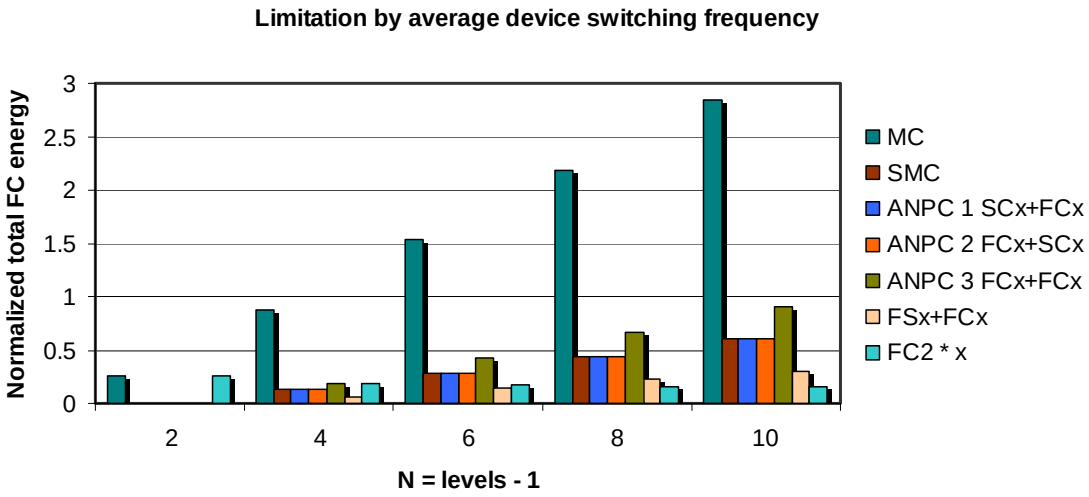


Figure 39, normalized FC energies in average device switching frequency limitation

In the case of a limitation by the average device switching frequency, SMC, ANPC1 and ANPC2 require the same total flying capacitor energy, which corresponds with the ANPC1 energy. At low number of levels, this number is even higher, e.g. more than 6 for N=4.

3.7.4.1.3 Operational limitation by apparent output switching frequency

Converter operation may also be given by a desired apparent output switching frequency. There are two cases that can be considered:

1. constant apparent output switching frequency independent of the number of levels
    a. the losses decrease and the efficiency increases with rising numbers of levels
2. the apparent output switching frequency scales with N
    a. the losses stay constant assuming the same device characteristics (scaled with voltage and current) even if the number of levels is changed

There are several cases where this type of limitation may be effective in reality:

1. Applications where the overall converter efficiency shall be maximized and where apparent output switching frequency requirements are met and an additional increase would not yield any benefit.
2. Applications where a very specific apparent output switching frequency is required due to
    a. The use of optimized pulse patterns at a given switching frequency
    b. External filters requiring a certain spectrum
    c. Limitation of the output spectrum due to EMC requirements

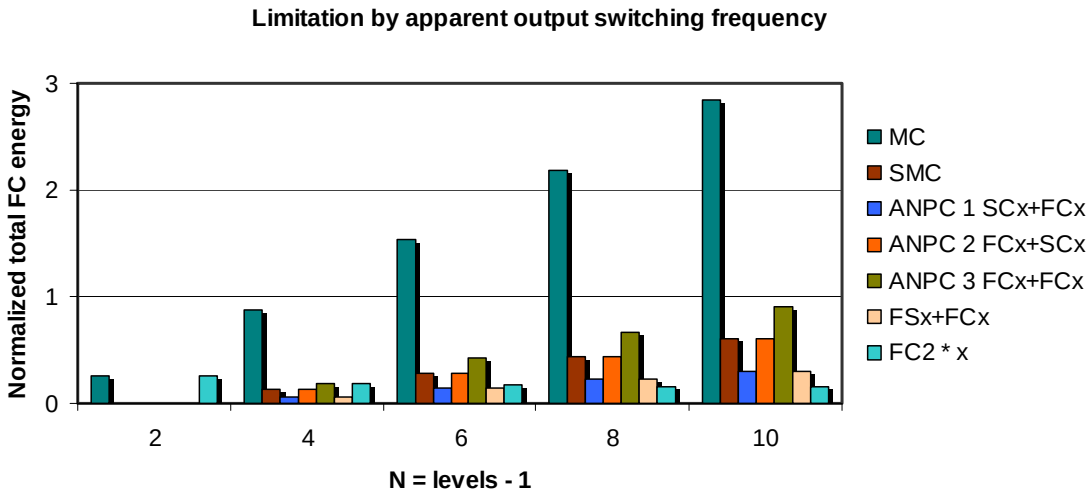


Figure 40, normalized FC energies for a given apparent output switching frequency scaling with N ($f_{out} = f_{base} * N$)

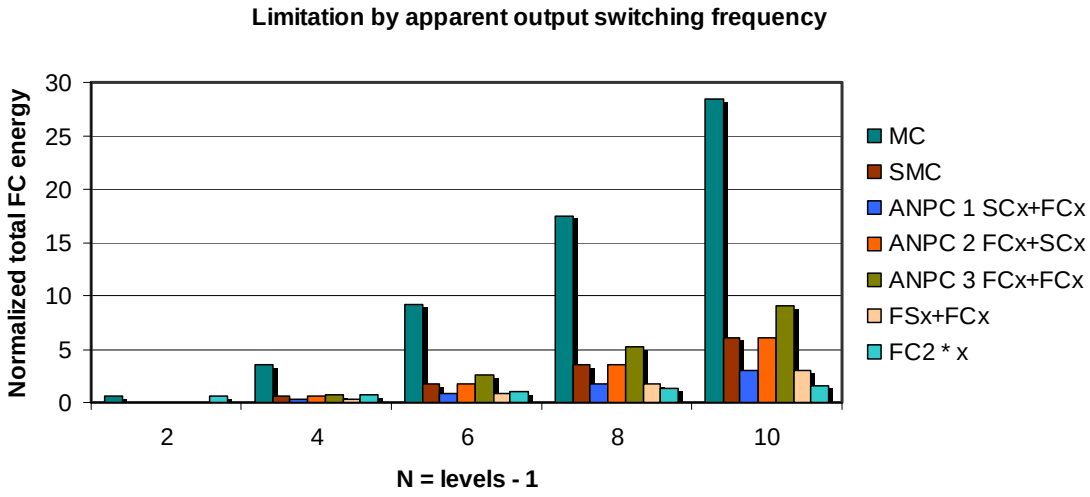


Figure 41, normalized FC energies for a given constant apparent output switching frequency ($f_{out} = f_{base}$)

Care must be taken when comparing the values from Figure 38 to Figure 41. Figure 38 and Figure 39 represent physical limitations given by the hardware design, whereas the apparent output frequency used as limiting factor in Figure 40 and Figure 41 can be chosen freely as long as it does not interfere with the physical limitations. Therefore, the amplitudes may vary according to the designer's choice. The scaling laws with increasing levels and the relationship between the requirements of the different topologies are the main interest in those two last figures.

3.7.5 Conclusion for MC based topologies

SMC, ANPC1, ANPC2 and ANPC3 seem to provide a good tradeoff between flying capacitor energy, switch requirement and controllability. SMC and ANPC2 provide lowest flying capacitor

energy in average switching frequency limitation while providing full output frequency. ANPC1 provides lowest flying capacitor energy but it does not yield the highest possible apparent output switching frequency in any of the cases. The ANPC3 provides highest apparent output switching frequency in all cases while resulting in reasonably low capacitor energies. Another benefit of the ANPC3 is its modular structure.

- The ANPC1 is the topology of choice for lowest possible flying capacitor energy if the apparent output switching frequency does not need to be maximized (independently of type of device switching frequency limitation) or in case an apparent output switching frequency is given.
- ANPC 2 and SMC are the best choice in average device switching frequency limited designs
- The ANPC3 is the best choice in systems where the limit is given by the maximum device switching frequency and the need of the highest possible apparent output switching frequency. Even though the ANPC3 has 3 times as many flying capacitors as the ANPC1, it can double the apparent output switching frequency with just 50% more total flying capacitor energy.

3.7.6 Comparison with M²LC

The M²LC has not been included in the previous paragraphs because its flying capacitor energy is given by the fundamental frequency rather than the switching frequency. A new constant including the switching frequency is defined in order to compare:

$$K_{2\_E\_cap} = \frac{K_{E\_cap}}{f_{sw\_base}} \tag{25}$$

With (24) we get

$$E_{tot} = K_{2\_E\_cap} \frac{I_{FC\_\max} U_{DC}}{2k_1} \tag{26}$$

$K_{2\_E\_cap}$ can also be defined for the M²LC. The energy in the M2LC flying capacitors can be calculated as follows, starting from (103) and (9).

$$E_{tot} = 2N \frac{CU_C{}^2}{2} = 2N \frac{\hat{I}_{out} * U_C{}^2}{4\omega \hat{U}_{cap\_ac} * 2} = N \frac{\hat{I}_{out} \left(\frac{U_{DC}}{N} \right)^2}{4\omega \frac{k_1 U_{DC}}{N}} = \frac{\hat{I}_{out} U_{DC}}{4\omega k_1} = \frac{I_{FC\_\max} U_{DC}}{4\omega k_1} \tag{27}$$

In order to be able to compare directly with MC based converters, we define:

$$K_{M2LC} = \frac{1}{2\omega} \tag{28}$$

$$E_{tot} = K_{M2LC} \frac{I_{FC\_max} U_{DC}}{2k_1} \tag{29}$$

The total required flying capacitor energy in MC based converters and M2LC converters is now possible based on (26) and (29), using only the constants $K_{2\_E\_cap}$ and K_{M2LC} without considering the converter voltage and current rating, nor the maximum tolerable voltage excursion of the flying capacitors.

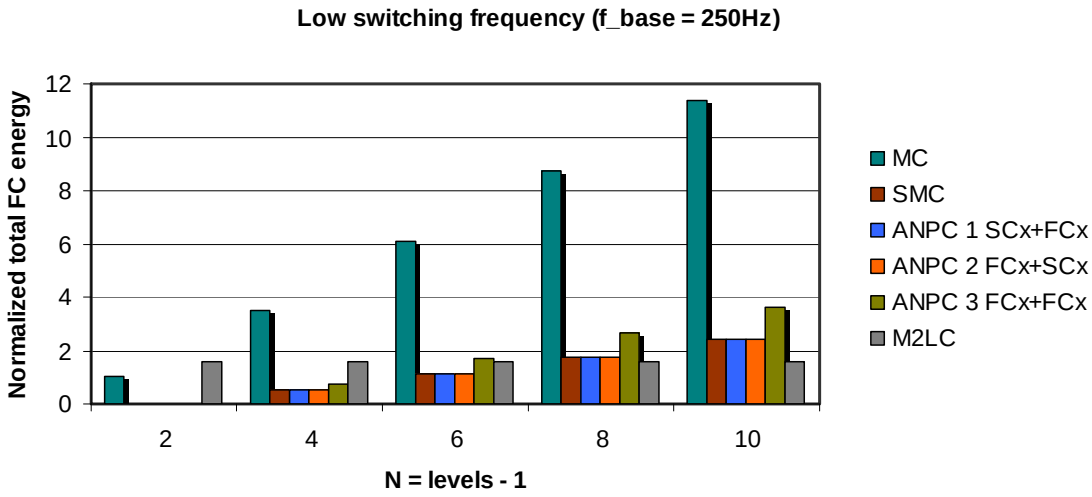


Figure 42, Normalized total flying capacitor energy at low switching frequency (f_{base} = 250 Hz) and average device switching frequency limitation

At a low device average switching frequency of 250 Hz, the transition point where the M2LC becomes more favorable is very low at N=8. Note that the apparent output switching frequency at this point is 2 kHz, which may already be sufficient for many applications.

At an intermediate device switching frequency of 1 kHz, the transition point where the M2LC becomes more favorable is at N=22. Note that the apparent output switching frequency at this point is 22 kHz, which is already very high considering the high number of levels. This leads to low filtering requirements at the output.

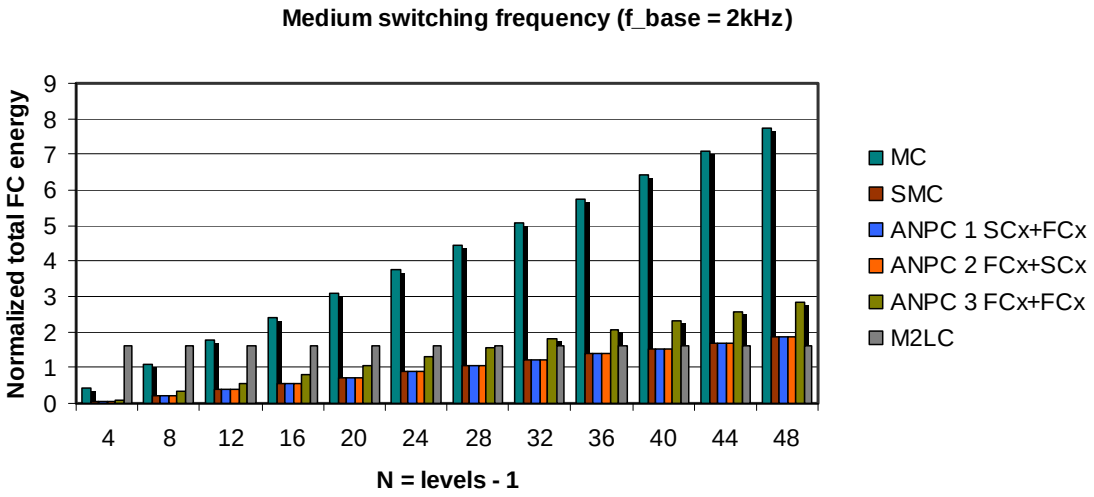


Figure 43, Normalized total flying capacitor energy at medium switching frequency (f_{base} = 2 kHz) and average device switching frequency limitation

At a device switching frequency of 2 kHz, the transition point where the M2LC becomes more favorable is at N=42. The apparent output switching frequency at this point is 84 kHz. For those values, output filtering is not a big issue any more for most applications. The design point for the switching frequency is rather given by the efficiency versus flying capacitor dimensioning trade off in this case.

The transition point scales linearly with the switching frequency. Accordingly, at 5 kHz, the transition point is expected around N=105.

3.8 Executive summary for chapter 3

A generic framework for the representation for ML VSC's has been introduced (see Figure 21 and Figure 22). This framework proves to be helpful both for analysis and synthesis of ML converters. Most ML VSC known today fit in that framework (Figure 23 to Figure 27). A systematic approach to come up with new topologies has been introduced: Choice of basic concept, positioning of flying capacitors, definition of suitable paths to operate converter. Several new topologies could be introduced that way, leading to two patent applications (one published by 2008: [4])

A number of different ML topologies have been compared and can be characterized as follows:

1. The MC has the best properties regarding semiconductor parts count, but it requires high flying capacitor energy.
2. MLDC and other topologies with more than 3 input levels require no or significantly less flying capacitor energy, but they have a higher semiconductor parts count (diodes) for higher number of levels and have serious operating range limitations (regarding modulation depth and load angle).
3. 3-L DC link based converters with multiple internal MC circuits provide a good trade off between semiconductor parts count, flying capacitor energy and controllability. Important examples in this family of topologies are the SMC and the ML ANPC.
4. M²LC has a high total semiconductor blocking voltage (twice the MC converter rating) and high flying capacitor energy, but both are independent of the number of levels. The M²LC requires less flying capacitor energy than MC based converters starting from a certain number of levels, which makes it attractive for high voltage applications. The M²LC is less suitable for low frequency applications as the module capacitors scale reverse proportionally with the fundamental output frequency.

Based on those findings, we can state that 3-L DC link based topologies with internal MC circuits are most attractive of all considered topologies for MV applications of any kind. This is in line with [5], which concludes with the statement that the 3-L based inverters SMC and ANPC offer a very good trade off between flying capacitor energy and total semiconductor blocking voltage.

The remainder of this thesis focuses on 3-L DC link topologies for more in depth analysis. Although, the balancing of the capacitors is inherently possible for those topologies, the limits of operation for the different topologies is not obvious and the NP current control capacity with state of the art control schemes is not good in certain operating points (very high and very low modulation depth, reactive power operation). New schemes extending the feasible operating range and improving the NP current control capacity are discussed in the following chapters.

4 3-L DC LINK ML CONVERTER PROPERTIES

This chapter explores the properties of 3-L DC link ML converters (SMC, ANPC, as introduced in the previous chapter) points out their limitations according to state of the art operation. The capacitor voltage control is a key aspect when applying those topologies. The flying capacitors can usually be controlled by the application of redundant states. Therefore, the main focus of the following investigations is on the controllability of the NP current. The two most powerful approaches for modifying the NP current are CM injection and use of redundant states. Consequently, there is a strong focus of this thesis on those two items. Other approaches have been proposed in literature (generation of output current harmonics, use of auxiliary circuits like break chopper) but are not investigated in depth in this thesis.

4.1 General converter properties

All 3-L DC link ML converters have some common properties as illustrated in Figure 44. There is a split DC link with the three supply potentials DC-, NP and DC+. The output current of one phase leg is supplied by any of these three potentials with some intermediate circuit that may contain switches and capacitors. The NP may be supplied by capacitors only or it may be connected to a separate supply. In case of a separate supply, there is no need for control of that potential. This thesis considers the case with supply for DC+ and DC- only, without separate supply for the NP. In this case, the potential in the NP needs to be balanced, either passively or actively.

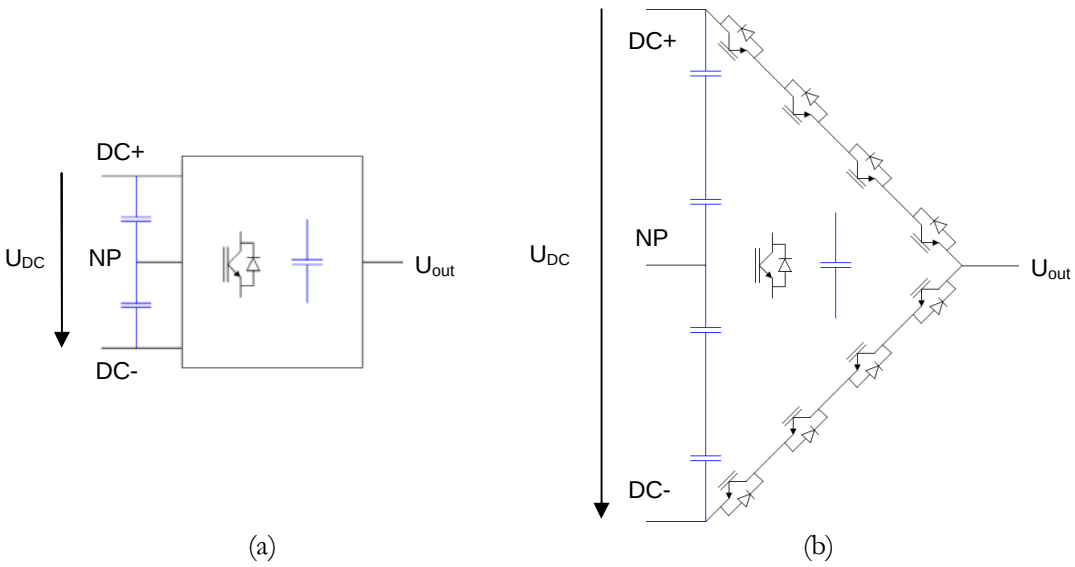


Figure 44, 3-L DC link converters, (a) general case, (b) triangle case

The very general case indicated in Figure 44 (a) includes hybrid converters as shown in Figure 29 (c). The analysis in this thesis is limited to the more constrained topology according to Figure 44

(b): all converters have series connected unipolar switches connecting the DC link directly to the output, and forming a generic triangle. The output voltage is thus constrained to within the DC link potential. No boosting is possible. Multiple flying capacitors can be integrated in a switch circuit within the triangle formed by the outer switches. The required blocking voltage in any switch position is indicated by the number of series connected devices in the generic representation. However, this doesn't necessarily mean commutation takes place with the according voltage. In the SMC for example, the outer switches need to block twice the voltage of an inner switch, but they only need to actively commutate a single level voltage. Double the blocking voltage is only required, as the output voltage may be pulled to the other rail by the opposite MC converter branch. The most important representatives of this family of converters are the previously introduced (A) NPC, the ML-ANPC, and the SMC shown in Figure 25 and Figure 26. The new topologies according to Figure 31 and Figure 32 also belong to that family and have similar properties as the ANPC 2. Operating principles according to the state of the art are described in this chapter. More sophisticated approaches are presented in the following chapters on new control and modulation schemes.

4.1.1 Some definitions

For the analysis of the converter properties, PWM is used (carrier based or SVM) and only optimal modulation is considered, applying only single level steps in the output. Average values are used for the description of the NP current. The impact of the current ripple is not considered. This can be done if the switching frequency is significantly higher than the fundamental frequency. Based on those assumptions, we can state the following:

- All currents in the system can be describes in function of load currents and duty cycles (α) of the commutation cells.

The following examples with the basic commutation cells illustrate the relationship between currents and duty cycles.

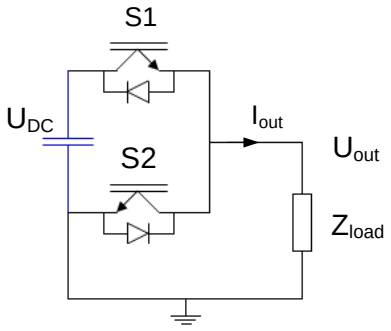


Figure 45, Half bridge with load

$$t_{S1\_on} = T_{MP} - t_{S1\_off} = T_{MP} - t_{S2\_on} = t_{S2\_off} \tag{30}$$

$$\alpha = d_1 = 1 - d_2 = \frac{t_{S1\_on}}{T_{MP}} \tag{31}$$

$$\bar{i}_{S1} = d_1 * \bar{i}_{out} = \alpha * \bar{i}_{out} \tag{32}$$

$$\bar{i}_{S2} = d2 * \bar{i}_{out} = (1-\alpha)\bar{i}_{out} \tag{33}$$

$$\bar{u}_{out\_DC-} = \alpha * U_{DC} \tag{34}$$

In flying capacitor stages, multiple commutation cells are connected in series. Each of the cells can have its own duty cycle α_x.

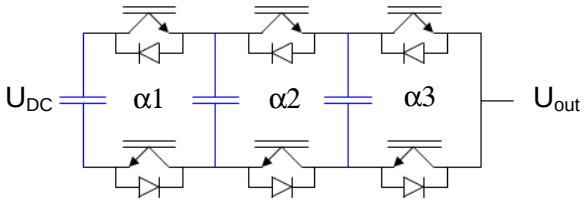


Figure 46, 4-L MC converter

To keep the flying capacitor voltages balanced, all upper switch average current must be equal and all lower switch average currents must be equal. According to Kirchhoff's law, the resulting flying capacitor average currents will be zero. As the switch currents are directly related to the duty cycles (32), (33), all duty cycles must be equal on average. Instantaneous values may differ. For a multi cell converter with n cells we can state that there is one common α:

$$x \in \{1,..,N\} \rightarrow \alpha_x = \alpha\,, \quad N = \textit{number of cells} \tag{35}$$

To get optimum modulation, the multiple cells need to be operated interleaved. There needs to be an according phase shift between the switching patterns of the individual cells. One simple way to implement that is with a carrier based PWM with phase shifted carriers. All of the phase angles in the set A are applied, none twice. The order does not need to be specific to assure balancing of the capacitors.

$$A = \{0, 2\pi/n, 4\pi/n, .., 2(n-1)\pi/n\} \tag{36}$$

$$x \in \{1,..,N\} \wedge y \in \{1,..,N\} \wedge x \neq y \rightarrow \varphi_x \in A \wedge \varphi_y \in A \wedge \varphi_x \neq \varphi_y \tag{37}$$

This type of modulation ensures the desired output voltage according to (34). The same average output voltage can also be obtained with different phase displacement, but no optimum modulation is achieved (for example: phase shift zero leads to synchronized switching and 2-L behavior, the advantage of multilevel operation is lost). The same concepts for calculations with average currents, voltages and duty cycles also apply to all combinations of commutation cells used in the 3-L DC link topologies. Specifically, we can also define a duty cycle α_L for a complete phase

leg. This duty cycle α_L will not necessarily correspond with any physical duty cycle of a commutation cell, as multiple cells within one phase may interact with differing duty cycles. In this case the duty cycle α_L rather defines the output voltage ratio U_{out} / U_{DC}, referenced to U_{DC-} and it can assume values from 0 to 1. The duty cycle α_L referring to a phase leg has a fixed relationship with the average switching function $\bar{s}$, as both are defining the output voltage ratio of a given phase. However, $\bar{s}$ is ranging from -1 to 1. The nomenclature s_{avg} is used for $\bar{s}$ in some parts of the thesis.

$$\alpha_L = \frac{\bar{u}_{out\_DC-}}{U_{DC}} \qquad \text{with } \bar{u}_{out\_DC-} \text{ referenced to } U_{DC-} \tag{38}$$

$$\bar{s} = s_{avg} = \frac{\bar{u}_{out\_NP}}{U_{DC}/2} \qquad \text{with } \bar{u}_{out\_NP} \text{ referenced to } U_{NP} \tag{39}$$

$$\alpha_L = \frac{\bar{s}+1}{2}, \qquad \bar{s} = s_{avg} = 2\alpha_L - 1 \tag{40}$$

The modulation depth m defines the amplitude of sinusoidal values. It is a constant number for a sine with constant amplitude. Each harmonic may also be assigned a modulation depth m_x. This is in contrast to the duty cycles and average switching function defined above, which are instantaneous values per phase, describing the operation of the converter in a given moment. A constant modulation depth m will generate sinusoidal duty cycles and average switching functions. The modulation depth m can be defined in different ways. This thesis uses the following convention (unless noted otherwise):

$m = \frac{\sqrt{3}}{2}$ for maximum sinusoidal line to neutral operation (no 3rd harmonic) (41)

$m = 1$ for maximum sinusoidal line to line operation (incl. 3rd harmonic or equivalent) (42)

$m > 1$ for the non-linear over modulation range (43)

4.2 Converter states

All considered ML topologies can be analyzed based on their commutation cells. Each of the converters has a number of commutation cells, some can be operated totally independently, and others may have some operational restrictions. To describe the status of the converter, we can assign one bit to each independent commutation cell. If some cells exclusively operate together, they can be described with one bit. We assign individual bits, if some cells partially operate together and partially operate independent. In this case, not all states in the table of all mathematically possible state are available. All physically possible states can be listed systematically in a table along with the key properties for each state. For a complete description of the converter, a table with a fraction of all possible converter states is sufficient due to symmetry.

4.2.1 5-L ANPC 1 converter states

The 5-L ANPC 1 has 4 commutation cells per phase, 3 of them are independent as indicated in Figure 47. The two cells connected to the DC link need to operate simultaneously to not violate blocking voltage requirements and to provide a reasonable input to the output MC stage.

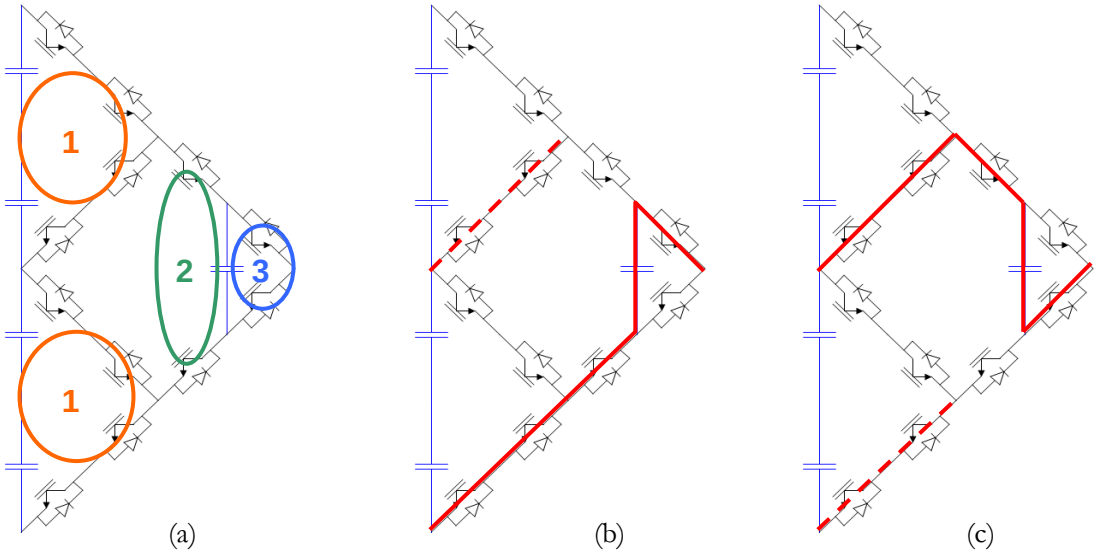


Figure 47, ANPC type 1 with numbered commutation cells (a), sample redundant states for $U_{out} = -U_{DC}/4$ (b) and (c), red line indicates conduction, dotted lines indicate paths where switches may be turned on (but having zero current)

The state for a single phase leg is described with the binary number $b_1b_2b_3$, the indices corresponding with the number of the switching cells, and b1 being the MSB, b3 being the LSB. The output current and the state of the phase leg determine the currents in NP and FC as shown in TABLE 20.

TABLE 20, STATES OF SINGLE PHASE LEG OF THE ANPC 1

State (decimal)	State (binary, $b_1b_2b_3$)	Level number and voltage	I_{NP}	I_{FC}
$\{0\}_{DS}$	$\{000\}_{BS}$	0 ($-U_{DC}/2$)	0	0
$\{1\}_{DS}$	$\{001\}_{BS}$	1 ($-U_{DC}/4$)	0	$+I_{Out}$
$\{2\}_{DS}$	$\{010\}_{BS}$	1 ($-U_{DC}/4$)	$+I_{Out}$	$-I_{Out}$
$\{3\}_{DS}$	$\{011\}_{BS}$	2 (GND)	$+I_{Out}$	0
$\{4\}_{DS}$	$\{100\}_{BS}$	2 (GND)	$+I_{Out}$	0
$\{5\}_{DS}$	$\{101\}_{BS}$	3 ($+U_{DC}/4$)	$+I_{Out}$	$+I_{Out}$
$\{6\}_{DS}$	$\{110\}_{BS}$	3 ($+U_{DC}/4$)	0	$-I_{Out}$
$\{7\}_{DS}$	$\{111\}_{BS}$	4 ($+U_{DC}/2$)	0	0

Note that level 0 and 4 have no redundant states. Level 1 and 3 have two redundant states each with differing NP and FC currents. Level 2 has two redundant states without impact on NP nor FC current. For a three phase system, we get the following number of available vectors and states:

TABLE 21, NUMBERS OF STATES OF THE 5-L ANPC TYPE 1

Number of discrete 2-D space vectors in αβ:	61
Number of discrete 3-D space vectors in abc:	125
Number of states generating different voltage, or NP or FC current (only considering 7 states per phase)	343
Total number of converter states for the 5-L ANPC (considering all 8 states per phase)	512

The large number of redundant states can be used to control NP and FC voltages (see paragraph 4.5.3.1), as well as for optimization of loss distribution or optimization of CM voltage. The total number of redundant states for a given topology is also a measure for the controllability of the converter. More redundant states indicate a higher degree of freedom and improved controllability of the converter.

FC currents are defined by the state of the corresponding phase leg alone; the NP current is defined by the states of all three phases: $I_{NP} = I_{NPa} + I_{NPb} + I_{NPc}$. For the case of $I_a + I_b + I_c = 0$, the NP current can be equal to an individual phase output current or the sum of two phase output currents, which is equal to minus any of the individual phase output currents. This means the NP current is zero, or plus or minus a given single phase current for any converter state.

Output voltage vectors can be described by grouping the output levels (from 0 to 4) of the three phases in braces: $\{abc\}_{3D}$. Note that such an output voltage vector does not contain any information on redundant states, but it can contain information on CM: $\{100\}_{3D}$ and $\{433\}_{3D}$ generate the same DM but different CM voltage. TABLE 22 shows all possible states for the differential vector $\{100\}_{2D}$, TABLE 84 in appendix 9.4 lists all states of the first 60° segment of an ANPC 1 converter with the corresponding NP and FC currents.

4.3 Space vector representation

Three phase values can be represented as vectors in a three dimensional space, directly using the phase quantities (e.g. phase output voltages) as variables for the three coordinates. The subspace of physically available voltage vectors for any three phase VSI is a cube, if each phase can independently assume minimum and maximum voltage.

In most applications, the differential mode (DM) voltage between the three phases is most important as it defines the main operation of the converter and is responsible for the power transfer. The common mode (CM) voltage on the other hand has no explicit function with respect to output quantities, but rather creates parasitic effects like stress of winding insulation in a transformer or generation of bearings currents in a motor. Therefore, the CM voltage can optimized for minimization of parasitic effects or it can be used for the control of converter internal quantities like NP voltage.

Due to the different functions of DM and CM, it is helpful to use a representation separating DM and CM. A coordinate transformation can be used to get two new coordinates representing the DM and one coordinate representing the CM (αβ0-system). Other systems are possible, for

example non perpendicular coordinate systems as proposed by N. Celanovic to simplify SVM calculation [34]. A similar approach is also used in this thesis in chapter 5 for the SVM calculation.

Representation of space vectors in αβ is equivalent to a projection of the vector space onto a plane. The projection of a cube onto a plane perpendicular to one of its large diagonals results in a hexagon. Such a hexagon represents the physically possible operating range of most 3 phase converters. Figure 48 and Figure 49 illustrate the above (maximum sinusoidal operation indicated with a red circle). The trajectory of a sample vector sequence is shown, connecting the minimum CM and maximum CM vectors $\{000\}_{3D}$ to $\{444\}_{3D}$. The light green hexagon indicates the intersection of the converter operation cube with the zero CM plane and indicates the limits of operation with zero CM voltage (sinusoidal zero CM operation indicated by a blue circle).

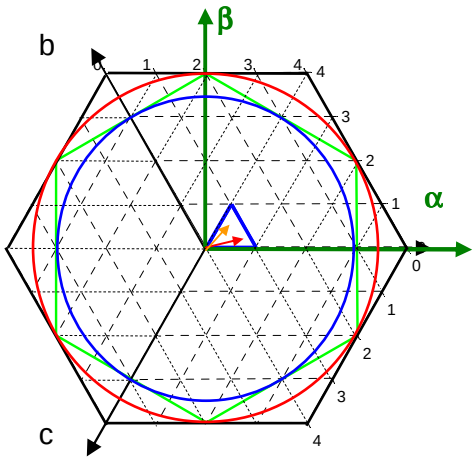


Figure 48, Triangular vector sequence in αβ–frame

In the αβ-frame, the vector sequence (blue) is only visible as a triangle as only three different DM voltage vector (equivalent to αβ-vectors) are applied. The CM voltage cannot be seen in that representation. The DM output voltage and therefore a 2-D representation of the converter state is sufficient for the control of the load (current, torque, etc.).

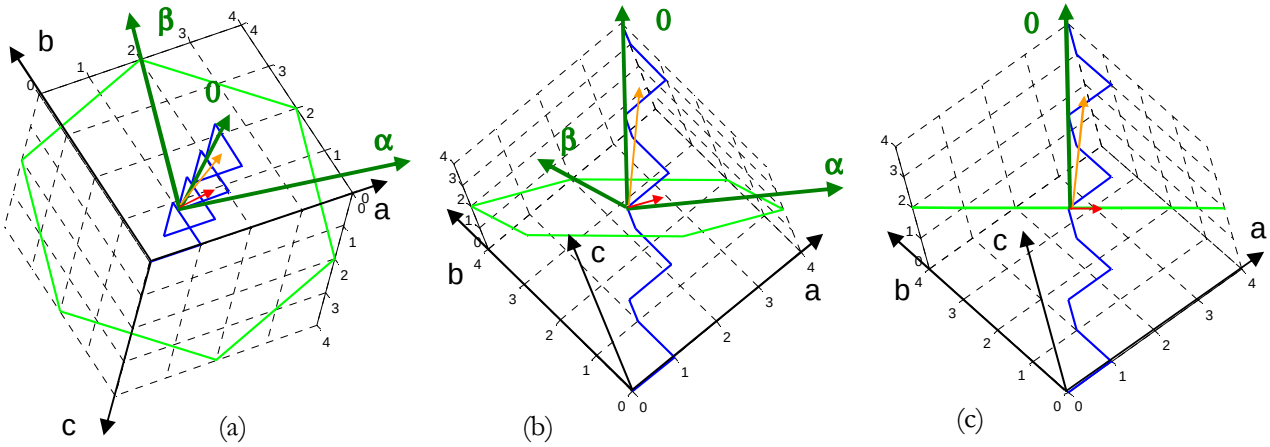


Figure 49, Cube in abc-frame with spiral vector sequence

In the tilted projection, it can be seen that the sequence is actually not a triangle, but a spiral type of trajectory, winding itself from $\{000\}_{3D}$ to $\{444\}_{3D}$. Note that there is only one trajectory enclosing each triangle of the αβ-plane. Trajectories in adjacent triangles always have different orientation: A clockwise trajectory in a triangle pointing upwards (in 2D) corresponds with decreasing CM voltage; a clockwise trajectory in a triangle pointing downwards corresponds with increasing CM voltage. That means that clockwise or counter clockwise trajectories can be chosen systematically in any modulation scheme to raise or lower the CM output, which is illustrated with a second set of sample graphs (Figure 50). No CM variation is visible in the αβ-projection (star shaped trajectory), whereas the 3-D representation reveals the change in CM based on two spirals.

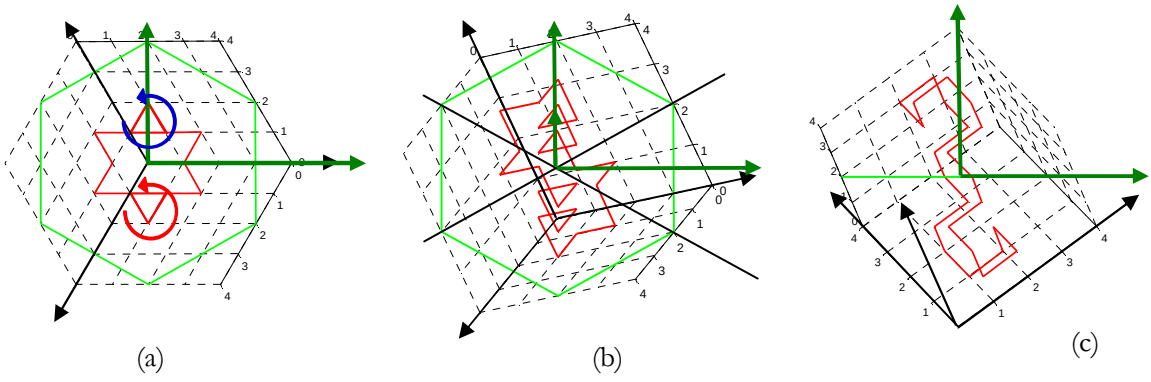


Figure 50, Example trajectory with CM variation; the blue arrow indicates increasing CM, the red arrow indicates decreasing CM voltage

4.3.1 Redundant states of the 5-L ANPC 1

The space vector representation in 3-D nicely represents the 125 available output voltage vectors. However, it can not distinguish different redundant converter states with the same output voltage vector. The following graph shows the location of redundant states of the 5-L ANPC in 3-D by means of small circles of different size and color.

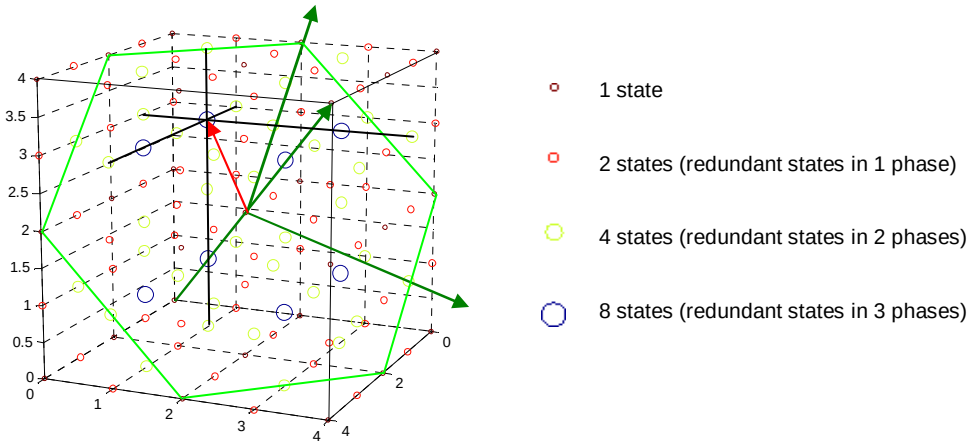


Figure 51, Redundant vectors with different FC or NP current in the 5-L ANPC1 (343 states)

The zero axis connects the output voltage vectors with zero output in αβ. A total number of 19 different states is possible for $\{000\}_{2D}$. All redundant states can be used for FC and NP control. If the redundant NP output states are considered too, the number of possible states is even higher. The red arrow in Figure 51 is pointing at the vector $\{131\}_{3D}$. This vector has redundant states in all three phases, resulting in eight available converter states. Figure 52 indicates the number of available redundant states with either differing CM voltage or differing NP or FC current in αβ. Obviously, there are many more redundant states available for the small vectors than for the large vectors. These numbers also show that the degree of freedom in defining a modulation and control scheme is siginificantly higher than for the NPC

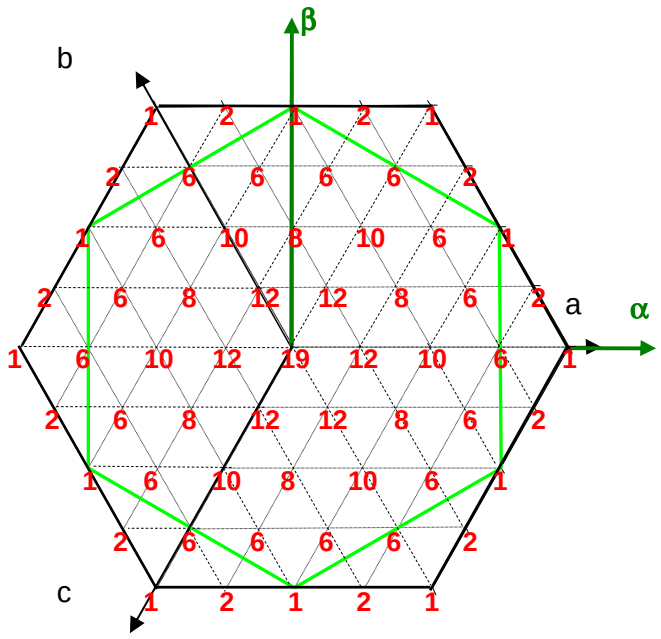


Figure 52, Redundant vectors with different FC or NP current in the 5-L ANPC1 (343 states)

4.4 Modulation

This paragraph introduces the fundamental PWM methods according to the state of the art and relates them to the work in this thesis.

4.4.1 CB PWM

Regarding CB (carrier based) PWM schemes, a lot of material has been published with respect to ML converters. Examples are the work by Holmes [35], McGrath [36] or Walker [37]. Li proposes overlapping carriers, which results in non-constant switching frequency, possibly non optimal modulation but reduces the output voltage distortion in the low modulation depth region [38]. PD (Phase Disposition) PWM with asymmetric sampling (constant reference for half a modulation period) is used in this thesis, as it is most favorable with respect to harmonics in 3 phase, 3 wire systems. The carriers can either be associated directly with a given phase and switching cell, or they can be generic (Figure 53) with a subsequent logic (state machine) to determine the actual states to be applied. Both approaches are used in this thesis.

A CM voltage needs to be applied to make full use of the available output voltage range. 3rd harmonic injection [39] is a good method to get smooth operation, CSPD PWM (Center Spaced PD PWM) yields best results regarding output harmonics. Both methods are applied in this thesis, both for simulation and experimental verification.

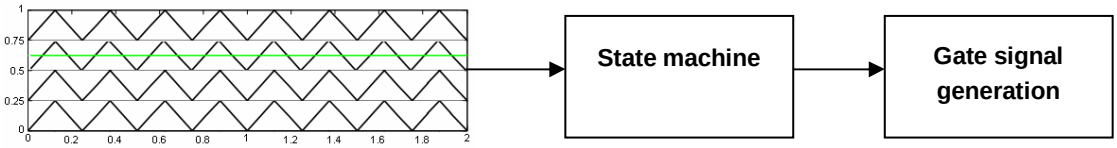


Figure 53, Generic 5-L PD PWM modulator with subsequent state machine

4.4.2 SVM

SVM (Space Vector Modulation) allows calculating states and their corresponding application times based on two or three dimensional vectors for all three phases at once, rather than per phase as in the carrier based PWM. SVM has been the subject of many publications (e.g. [40] for a basic 2-L performance analysis, [41] for ML SVM). Usually the NTV (Nearest Three Vectors) method is used for SVM to get optimum switching patterns. Other ways of SVM are possible. Fukuda is proposing to determine optimal switching sequences by means of optimal control [42, 43]. The optimal control approach is of specific interest if multiple quantities (like FC voltages in a ML converter) shall be controlled by the SVM modulator (e.g. [25]).

Several authors also have proposed 3-D SVM ([44], [45]). In this case, 3-D reference vectors are used (see also Figure 52) rather than 2-D vectors in $\alpha\beta$. Consequently, the reference also contains a part for the CM. Control schemes acting on CM may be applied in this case. This approach results in very similar results as the carrier based modulation schemes, as both are using a reference defined in all three dimensions. In fact, the carriers are only a graphical representation of an algorithm that can be used to calculate states and their application times based on a given 3-D space vector. This is specifically true in the case of use of generic carriers as in Figure 53.

CB PWM and SVM are closely related to each other and essentially represent two different mathematical methods to get the same (or similar) resulting pulse pattern. A number of publications analyze the relationship between CB PWM and SVM (e.g. [46], [47], [48],) or even propose hybrid CB / SVM schemes [49].

In this thesis an asymmetric SVM is used. Like in the case of PD PWM, there are two sampling periods per modulation period. 3 or 4 vectors are applied per sampling period.

4.4.3 Modulation by choice of "next best vector"

In contrast to the PWM schemes presented in the previous paragraphs, "next best vector" schemes do not pre-determine a sequence of states but only apply one state at a time. The duration is not known at the application time but determined dynamically, for example by means of a switching surface controller (or hysteresis controller). Many different schemes of that kind are possible. Typical representatives are DTC (direct torque control) and DPC (direct power control), which also have been adapted for ML converters (e.g. by L. Serpa [50]). These schemes are typically implemented by means of look up tables, but other solutions are possible. For example MPC (Model Predictive Control) [51] is a very powerful approach for effective implementation of DTC

[52, 53] and also for more standard modulators controlling the output current [54, 55]. These concepts also have been applied to NPC converters by [56, 57].

The higher the number of levels is, the less interesting those schemes are, as high apparent output switching frequencies can be achieved with low switching frequencies on the device level. Available calculation time becomes short, limiting the prediction horizon. However, some concepts like the virtual vectors (see chapter 5) can only be achieved with a long prediction horizon. Also, if the calculation time is too long, there may be multiple commutations to reach the next best vector. Output quality could be better if intermediate states would be applied too. Application of pre-determined sequences (standard CBPWM, SVM, or optimized sequences as proposed in chapter 6.2) may be more favorable.

True next best vector modulators are not discussed in this thesis. Note that the basic physical limitations explored apply to those modulators too. Also the possibilities regarding an extension of those limits by the application of redundant states are basically the same. However, the modulation and control schemes developed in this thesis cannot be applied directly to next best vecor modulationa schemes. Note that control schemes like DTC and DPC can also be applied using PWM techniques so that they become compatible with the modulators proposed.

4.4.4 Selective harmonic control

The first paper describing the NPC converter by Nabae et al. [58] has already described PWM methods for SHE (selective harmonic elimination). Multiple low order harmonics could be eliminated in order to operate a drive with very low switching frequency to get high efficiency. More generally, specific harmonics can be controlled to a maximum value rather than eliminated completely. Wells gives a very good overview of existing methods on SHC (selective harmonic control) in his dissertation [59] and extends the theory towards a GSHC (generalized selective harmonic control). He also introduces new methods with carrier based modulation and proposes an approach for optimal SHC based on a cost function including converter and load losses. Some of the methods proposed can be extended to ML waveforms and other publications focus entirely on ML SHC or SHE.

SHE pulse pattern have typically a time varying switching frequency and differentiate clearly from CB PWM and SVM in that respect. Calculation of SHE is usually done offline; online calculation is possible but usually constrained by the computational complexity. SHC is not a topic of this thesis. However, if a 3-L DC link converter should be operated with any of the methods proposed in literature, a suitable NP and FC balancing scheme is required (this is not usually discussed in SHC publications, as those treat the problem typically topology independent). The suitability for operation with SHC schemes is therefore interesting point of discussion for the NP control schemes presented in the following chapters.

4.4.5 General comments on ML modulation

4.4.5.1 Over modulation region

All of the modulation schemes above are limited to the same DM amplitude in linear operation, indicated with a red circle in Figure 48. The DM amplitude can be increased by extending beyond this red circle, up to full trapezoidal operation limited by the black hexagon. In the over modulation region, the DM voltage contains lower order harmonic (apart from the high order harmonics originating from the PWM), more specifically 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonic etc.

Methods to minimize the low order harmonics in the over modulation region have been proposed in literature ([60],[61] and [62]). Some of these methods can also be used in combination with the modulation schemes proposed in chapter 4 and 5.

Another aspect of over modulation is important for the NP control: The aforementioned harmonics will be apparent also in the output current of the converter and these currents will then interact with the rectified switching function. This is investigated in more detail in paragraph 4.8. With increasing degree of over modulation, there is an increasing probability of generating a DC NP current. On the other hand, the control principles introduced will still work but become less powerful, as the physically possible range for CM injection becomes very small. This means the robustness of the system is reduced and the risk of loosing control of the NP voltage is increased. The experimental results in chapter 7 in fact show instability in the over modulation range for the control schemes discussed in chapter 4. Chapter 5 introduces modulation schemes that improve NP voltage controllability significantly in the over modulation range.

4.4.5.2 Output voltage distortion

The modulation schemes discussed so far assume constant voltage sources (DC link, NP and flying capacitors) to compose a defined output voltage. A deviation of the DC voltage sources from their reference value leads to output voltage distortions, which has a negative impact on the control of both converter external and internal quantities. Such output voltage distortion can be avoided by appropriate feed forward control taking into account the instantaneous DC quantities. Appropriate schemes have been presented in multiple publications, e.g. [63], [64] or [65].

4.4.5.3 Switching frequency considerations

Carrier based PD PWM modulation generally results in very good harmonic performance [35]. This holds true as long as sufficient symmetry within one modulation period is obtained both for voltage and current. This is essentially true when voltage references and currents do not change much within one modulation period. If however, the voltage reference has moved far away, for example into a new triangle for the second half of the modulation period, a totally different pattern is generated in that second half and no symmetry required for the harmonic performance is obtained. PD PWM only provides good harmonic performance down to a certain switching frequency. Below, the requirements for the basic concept of PD PWM are not met anymore. The limits can not be stated in an absolute number for the switching frequency, but they depend highly on the number of levels used. The basic requirement for PD PWM is that the reference doesn't move too much within one triangle of three nearest space vectors. Performance will gradually decrease with lower switching frequency and smaller triangles. Consequently, this means that the minimum reasonable switching frequency will increase proportionally with the number of levels of a converter, as the triangles have inverse proportional size with the number of levels.

For a given harmonic performance, a converter with a high number of levels may operate with lower switching than a converter with a low number of levels. This would lead both to smaller triangles and lower switching frequency, whereas switching frequency should actually get higher to stay way from the operating limits of PD PWM. To conclude, we can state that ML converters are clearly more prone to hitting the limits of PD PWM as 2 or 3 level converters. Therefore two paths for modulation are considered in the following chapters:

1. Standard PD PWM or SVM with new CM injection concepts and subsequent state optimization for capacitor control for medium and high switching frequencies (chapter 4 and paragraph 6.1)
2. Optimal sequence SVM, with only 3 vectors to be applied per modulation period, applicable to low switching frequency applications (paragraph 6.2)

4.4.6 Modulator implementation and experimental verification

Different modulator implementations have been used in the frame of this thesis. The modulator for the experimental verification of the SMC schemes (5.3.4) has been implemented totally on an FPGA with a generic PD PWM modulator and a subsequent state machine choosing the appropriate converter states (Figure 53). This modulator runs on a DSP based control system by LAPLACE [66]. The optimal sequence modulator introduced in 6.2 runs on an industrial control system (AC 800PEC by ABB). The code is implemented in MATLAB/Simulink. OPCoDe (Optimized Process of Code Development) generates the runtime code automatically from the Simulink and Matlab files.

Figure 54, ABB's AC 800PEC, core of the OPCoDe system

A third separate modulator is running on the same OPCoDe system, is implemented also in Matlab but includes multiple modulators: all CB PWM schemes according to the paragraphs 5.1 and 5, as well as the SVM scheme with virtual vectors introduced in paragraph 6.1. These schemes are seamlessly integrated and can changeover from one to the other scheme in operation anytime. This feature is required by the hysteresis controller proposed in paragraph 7.3. The CB part of the modulator has asymmetric sampling, PD double edge modulation. Different PD PWM schemes (e.g. 3rd harmonic injection or CSPD PWM) can be chosen. Switching times are pre-calculated (rather than determined by an actual reference carrier comparison) and communicated to the FPGA for gate signal generation. In this way, the gate signal generation on the FPGA can easily be shared with the SVM schemes, which are based on the NTV method. A calculation method with non perpendicular coordinates similar to [34], [67] or [68] is used for fast calculation. The same implementation of the modulator (same m-file) is used for simulation and experimental verification, which ensures good correspondence between simulation and real operation of the converter.

A low power 5-L ANPC prototype (6kVA) has been used for all experimental verification regarding ANPC. The prototype has been specified for control investigations (rather than high power density) providing easy access to all relevant signals and flexible configuration of DC link and flying capacitors.

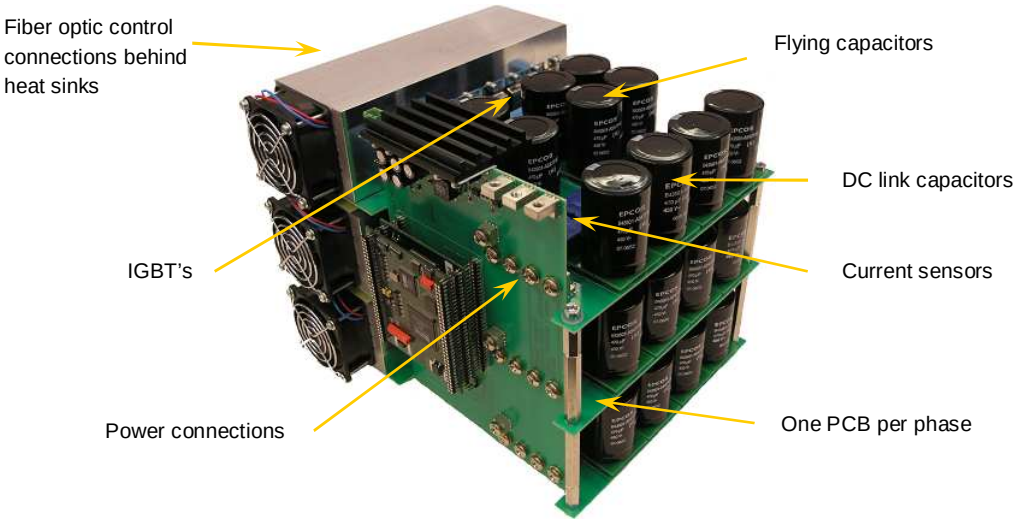
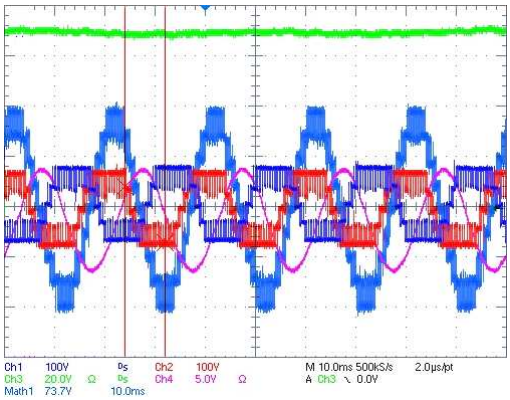


Figure 55, 6kVA 5-L ANPC



CH1 (dark blue): U_{out1}

CH2 (red): U_{out1}

CH3 (green): U_{NP}

CH4 (magenta): I_{out3}

Math1 (red): U_{out1_2}

Figure 56, 5-L ANPC waveforms at φ = 0.1, m = 0.9, PD PWM with 3rd harmonic injection

The optimum modulation waveform (only single level steps) with 5 levels in the phase voltage (red) and 9 levels in the phase to phase voltage (light blue) is nicely visible in Figure 56.

4.5 Introduction to NP and FC control in 3-L DC link converters

4.5.1 Sources of NP current

In order to effectively control the NP voltage 3-L DC link converters, the sources of NP current have to be known. These are primarily:

- Function of output current and switching pattern
- Uneven DC link load (by auxiliaries)
- Active balancing circuits
- Components characteristics

The first one is the most important. Relatively large DC NP current can be generated. Output current harmonics, combined with a given switching pattern, can generate undesired NP current leading to a shift in NP voltage. The switching pattern on the other hand is also the primary source of control for the NP current and voltage. In the frame of this thesis, only the first point is considered in detail, the additional sources of NP current are treated together as a random NP bias current without specifying the source.

4.5.2 NP control

The NP in 3-L DC link converters can be controlled by proper injection of zero sequence or CM voltage. Such a CM voltage has an immediate impact on the NP current, depending on modulation depth and load angle [69, 70, 71]. Various ways to generate a suitable CM voltage have been proposed and analyzed in literature both for CB PWM and SVM. The proposals are numerous and the following list can only give an overview of important publications without being comprehensive. Examples for CB PWM based NP control methods include [72, 73, 74, 75, 76, 77, 78]. Most of the SVM methods proposed use simple binary logic or lookup tables to determine the suitable redundant state for NP control without considering the CM associated with it: [79, 80, 34, 81, 67]. Although some of the proposed concepts are similar or even equal, most use different calculation methods and apply different constraints, with the result of have differing performance regarding NP control capability in function of the operation point (modulation depth and load angle). [82] and [83] compare different NP control methods. [84] describes physical limitations of optimum modulation schemes regarding NP control.

Some of the proposed NP control schemes generate non optimum pulse patterns (non-adjacent vectors are used in modulation) but increase the balancing capacity of the modulator. Bendre proposed to replace medium vectors by a linear combination of two large vectors [85], thus completely eliminating the low frequency ripple in the NP but increasing output voltage distortion. Another example is the virtual vector SVM proposed by Busquets-Monge [86]; a virtual space vector composed of two small vectors and one medium vector with resulting zero NP current is defined. This virtual vector can then be used to build new triangles with their own NTV SVM. Ustuntepe [87] starts from [85] and [86] and improves the output distortion performance by combining the two concepts, not eliminating the medium vectors completely, but including the small voltage vector redundancy optimization and medium voltage vector distribution ratio optimization in one algorithm. Pou and Zaragoza [88, 89] propose a carrier based algorithm

essentially giving the same result: medium vector application is reduced; the increased NP balance capacity allows for an elimination or reduction of the low frequency NP voltage ripple at the cost of increased switching frequency or output voltage distortion. Videt [90] is also applying a non optimum pulse pattern but with the aim to reduce CM voltage. In this case, he avoids the large vectors and there is only a minor impact on the NP balancing capacity.

A fundamentally different approach for NP control has been proposed by Marchesoni [91]. Instead of changing the switching waveforms spectrum (namely by adding a CM component) to interact with the load current fundamental, Marchesoni proposes to inject harmonics in the load current to interact with the switching pattern. This concept is not taken up to be developed further in the frame of this thesis, but the considerations on harmonics interaction in the following paragraphs help pointing out, how the concept works. It can be combined with most of the other concepts proposed in literature and in this thesis.

Active NP control hardware circuits avoid the need for sophisticated NP control schemes. [92] analyzes the NP current in function of input current harmonics but then proposes an additional charge balance leg to control the NP voltage.

Most of the publications above refer to the 3-L NPC. ML split DC link topologies differ from the 3-L NPC by the number of levels but also by the fact that the higher level converters feature redundant states. The question is, whether the existence of such additional redundant states offers new opportunities regarding operating limitations and NP control. For this investigation, the analysis of the NP current characteristics is very important. A large part of the following section is dedicated to that with special attention to CM impact, harmonics interaction and relevance of redundant states. It will be shown that all of the cited methods can be applied to any general 3-L DC link converter. The same controllers can be used and the same limitations apply (for a given method). However, some of the 3-L DC link converters with higher number of output levels allow for an operation and NP control capacity beyond what has been presented in any of publications above.

4.5.3 FC control

4.5.3.1 FC control by variation of duty cycle (carrier shifting)

A very simple flying capacitor control scheme can be implemented based on the variation of the individual duty cycles: A shift of those duty cycles against each other leads to non-zero average currents in the capacitors, which can be used to control their voltage. Note that a shift of individual duty cycles leads to an output voltage distortion. This approach is not very dynamic and can be insufficient with very distorted loads or highly dynamic operation with a lot of dynamics. In steady state operation, it is capable of giving very smooth FC control with minimum capacitor voltage ripple. A suitable offset in the reference signal gives exactly the same result. If the modulation is done by SVM, the duty cycles can easily be adapted by adding and subtracting the appropriate times from the duty cycles.

4.5.3.2 FC control by use of redundant states

Instead of a modification of duty cycles, a suitable choice of redundant states can be used for FC control. Vector $\{100\}_{2D}$ is used to illustrate the concept. Any two states of the same color in TABLE 22 results in zero average FC current in all three phases. The resulting NP current is $+i_a/2$ for low CM voltage and $-i_a/2$ for high CM voltages ($i_c + i_b$ equals $-i_a$). Therefore, a combination of

any of the upper six states in the table with FC balancing result in $+i_a/2$, a combination of any of the six lower states in the table with FC balancing results in $-i_a/2$.

TABLE 22, REDUNDANT STATES FOR VECTOR $\{100\}_{2D}$ AND COMBINATIONS OF STATES FOR BALANCED FC VOLTAGES

States				Levels			Currents			
Total	a	b	c	a	b	c	i-NP	i-FC-a	i-FC-b	i-FC-c
$\{1\}_{DS}$	1	0	0	1	0	0	0	ia	0	0
$\{2\}_{DS}$	2	0	0	1	0	0	ia	-ia	0	0
$\{75\}_{DS}$	3	1	1	2	1	1	ia	0	ib	Ic
$\{83\}_{DS}$	3	2	1	2	1	1	-ic	0	-ib	Ic
$\{139\}_{DS}$	3	1	2	2	1	1	-ib	0	ib	-ic
$\{147\}_{DS}$	3	2	2	2	1	1	0	0	-ib	-ic
$\{221\}_{DS}$	5	3	3	3	2	2	0	ia	0	0
$\{222\}_{DS}$	6	3	3	3	2	2	-ia	-ia	0	0
$\{367\}_{DS}$	7	5	5	4	3	3	-ia	0	ib	Ic
$\{375\}_{DS}$	7	6	5	4	3	3	ic	0	-ib	Ic
$\{431\}_{DS}$	7	5	6	4	3	3	ib	0	ib	-ic
$\{439\}_{DS}$	7	6	6	4	3	3	0	0	-ib	-ic

- States are defined as $\{c_1c_2c_3b_1b_2b_3a_1a_2a_3\}_{BS}$ (c_1 = MSB, a_3 = LSB).
- Output levels are numbered from 0 to 4.
- Currents are defined as positive when flowing out of the converter. Positive values indicate discharge of either NP and / or FC, negative currents are correspondingly charging NP or FC.

Any linear combination of states in the upper half and the lower half can be implemented, leading to any average NP current value between $-i_a/2$ and $+i_a/2$. This corresponds with what has been found in paragraph 4.7.1.2, the NP current can be described as a piecewise linear function of the CM voltage also in the operating point of a discrete vector. The same kind of behavior can be shown for any of the other space vectors. The same principles apply to any other 3-L DC link topology. Redundant states can be combined to balance the flying capacitors and the resulting groups of states can be combined again to control the NP current.

4.5.4 Interaction of NP and FC control

All 3-L DC link ML converters need both NP control and FC control. The two can be decoupled in all topologies in the following way:

- FC control by choice of redundant states
- NP control with CM based 3-L NP control schemes

However, when they are combined, there is a higher degree of freedom. Suitable combinations of redundant states act both on FC and NP at the same time, but there may also be conflicting targets. This is topology specific and is discussed in more detail in paragraph 5.3 and chapter 0 where control schemes acting on NP and FC at the same time are proposed.

4.5.5 Natural balancing

The split DC link converters have natural balancing properties for the flying capacitors and / or the NP voltage at least in some operating points. This has been analytically analyzed in various publications for NPC [93, 94], MC [95, 96, 97, 98, 99, 100], and SMC [101, 102]. [103] proposes a SVM scheme extending the natural balance capability of the NPC, allowing for smooth operation in

steady state. No publications on the natural balance properties of the ML ANPC are available so far. A self balancing feature is nice, as it allows applying optimal modulation schemes regarding harmonic performance without sacrificing that property for NP control. On the other hand, active balancing features are not very effective and in reality, all topologies may require active NP control during transients, with distorted or unbalanced loads or in specific operating point. Active NP control schemes can dramatically improve dynamics and steady state error in NP and FC voltages. The remainder of this thesis focuses fully on active methods and does not investigated natural balance any further.

4.6 NP current in function of output voltage in single phase legs

The neutral point current depends on the output currents and the duty cycles of the relevant switching cells. Many publications on NP control include an analysis of the NP current, however, this is usually limited to certain operating ranges and a limited set of topologies. The following paragraphs investigate the NP current for different topologies in detail to determine, whether the topology has an impact on the NP controllability and the control concepts to be applied.

4.6.1 NP current in the NPC

In the NPC, there are two commutation cells. The upper cell is controlled by S1 and S3, the lower cell is controlled by S2 and S4. The NP current can be calculated based on (32) and (33) on page 53. The corresponding duty cycles and the resulting NP current are indicated in Figure 57.

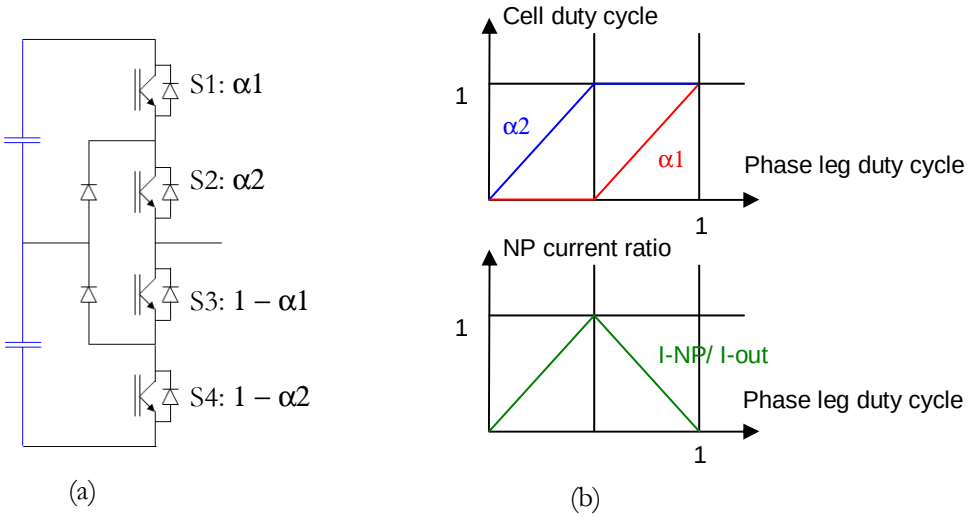


Figure 57, 3-L NPC with duty cycles of the individual switches and the resulting normalized NP current, b) also valid for standard SMC modulation

4.6.2 NP current in the 3-L ANPC

The ANPC allows for several different modulation schemes [22]. The different schemes are indicated in Figure 58. To calculate the NP current, the following equation can be derived from (32) and (33), assuming cell 1 and cell 2 to be operated in phase and cell 3 with a phase shift of π. $\alpha 2$ must always be larger than $\alpha 1$ to not violate any blocking voltage constraints.

$$\bar{i}_{NP} = \bar{i}_{out} * (1 - \max((\alpha_1 + \alpha_3 - 1),0) - \max((1 - \alpha_2 - \alpha_3),0)) \quad (44)$$

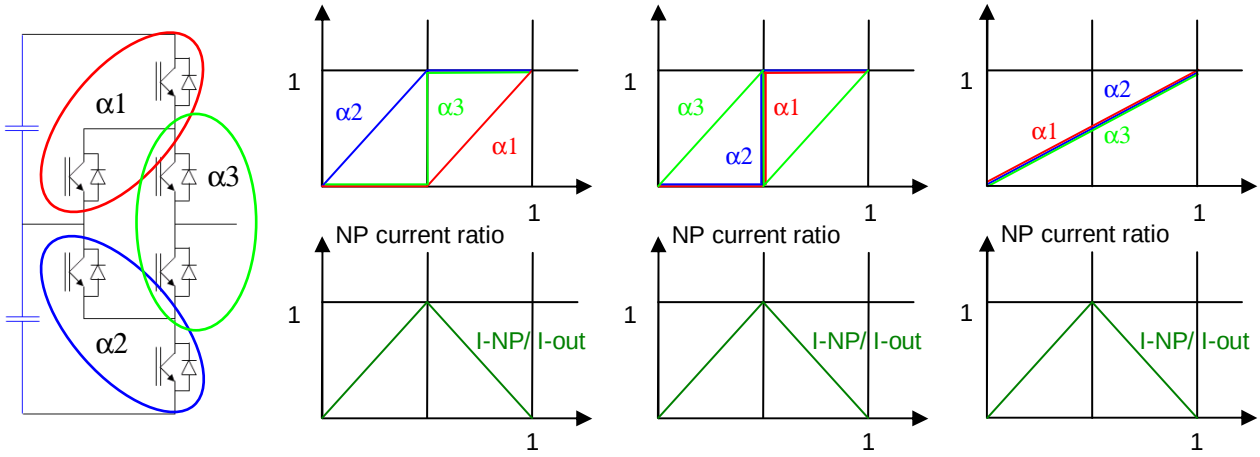


Figure 58, ANPC commutation cells, operating schemes and resulting NP current functions

As a fourth operating principle, the ANPC can be operated as the NPC. All types of operation can be combined to balance the losses. All modulation schemes result in the same NP current function, which comes as no surprise: No matter how the modulation is done, with optimum modulation, the output is always a linear combination of NP and one of the outer points of the DC link.

4.6.3 NP current in the ML ANPC

4.6.3.1 Type 1 and type 2 ML ANPC

The ML ANPC type 1, Figure 26 (b) and type 2, Figure 26 (c) have different restriction than the 3-L ANPC. Not all stages can be operated simultaneously as they do not all provide the required output levels. The ANPC type 1 can only be operated according to Figure 58 (c); the ANPC type 2 can only be operated according to Figure 58 (b). For the NP current, only the cells adjacent to the DC link are relevant. They determine the NP current independently of the status of all remaining cells. As all cells are operated with the same duty cycle α, also the relevant cell adjacent to the DC link is operated with that same duty cycle. Consequently, the resulting NP current functions correspond with (44) and the characteristic shown in Figure 58 (b) and (c).

4.6.3.2 Type 3 ML ANPC

The following constraints generally apply to the ML ANPC type 3 (Figure 26 d)):

1. Average input voltages U1, U2 and U3 for the converter stages 1 to 3 are equal
2. Dynamically, U3 (generated by stage 1 and stage 2) must be larger than the voltage in the first capacitor of stage 3, to avoid a discharge of that capacitor through the diodes.
3. This can only be guaranteed if stages 1 and 2 are either

a. Operated simultaneously or

b. At least one of the cells in one of the stages 1 or 2 is turned off completely to allow for a floating of the voltage in certain boundaries.

Based on those criteria, several operating schemes are possible:

1. Alternate operation of the three MC converter stages, either
   a. Stage 1 and 2 operated at fundamental frequency, stage 3 operated at high frequency or
   b. Stage 3 operated at fundamental frequency only, stage 1 operated at high frequency during positive output voltage, stage 2 operated at high frequency during negative output voltages.
2. Simultaneous operation of all three MC converter stages

The first option is straight forward: the modulator simply chooses between type 1 and type 2 modulations for a finite time and switches over between the two types. The strategy for switching between the two types of modulation can be based on fixed predetermined split of the fundamental period (e.g. a quarter wave period for each type at a time) or it can be based on an online loss distribution algorithm. Like in the case of the type 1 and type 2 converters, only the state of the operating cell adjacent to the DC link is relevant. This is either the first cell of stage 1, the first cell of stage 2 or the first cell of stage 3. Again, all these cells use the same duty cycle a, but are not operated simultaneously and therefore do not interfere with each other. Consequently, the NP current again is formed according to (44) and the characteristic shown in Figure 58 (b) and (c).

The second type of modulation scheme with simultaneous operation of all three MC converter stages is more complex regarding the balancing of flying capacitors and neutral point. A suitable strategy is introduced in paragraph 5.3.1.

4.6.4 SMC

The SMC can be operated like the ANPC type 2, with a totally separate modulation of the upper MC converter stage and the lower MC converter stage. This results in the exact same behavior regarding neutral point current (Figure 57 (b)). This kind of modulation scheme is the standard scheme as used in all publications on the SMC known to the author. However, the SMC is not restricted to that mode of operation. The flying capacitors can also be operated in series, which corresponds with a simultaneous operation of the two MC converter stages. Like in the case of the ANPC type 3, care must be taken with the balancing of capacitors and the NP. Suitable modulation schemes are introduced in 5.3.2.

4.6.5 NP current characteristics conclusion

All split DC-link topologies have the same NP current characteristics with standard modulation applied, independently of the number of levels and the flying capacitor arrangement. The characteristics of all standard and new modulation schemes with corresponding NP current functions are summarized in TABLE 82 in appendix 9.1. This common property for all topologies also means that all concepts for NP control in 3-L NPC converters according to the state of that

art, which are making use of the NP current – voltage characteristics can also be used for any of the proposed split DC-link topologies. This finding is rather important, as the published concepts are numerous and they can both be used as basis for the further development of control schemes and for the basic understanding of the ML converter properties.

The standard NP current function common for all 3-L DC link converters can be expressed as:

$$\bar{i}_{NP} = (1 - abs(\bar{s})) * \bar{i}_{out} \tag{45}$$

With the average switching function $\bar{s}$ from -1 to 1. Alternatively, the per phase duty cycle α_L can be used resulting in:

$$\bar{i}_{NP} = (1 - abs(2\alpha_L - 1)) * \bar{i}_{out} \tag{46}$$

4.7 NP current in multiphase systems

The findings from the previous paragraph on single phase leg properties can be used for the investigation of multi phase systems. The NP currents in function of the voltage in single phase legs (45) and (46) combine into characteristic NP currents in function of the CM voltage for a given DM output voltage. Based on the basic NP current functions, an analysis of the NP current spectrum can be made. Specifically, the DC NP current term relevant for NP voltage control can be determined in function of line currents and converter switching functions.

4.7.1 NP current in function of CM

4.7.1.1 H-bridge

In an H-bridge configuration, a single phase output voltage is created by connecting a load between two single phase legs. The output voltage is proportional to the difference of the two average switching functions $\bar{s}_a$ and $\bar{s}_b$. The two currents sum up to zero, as there is one single current loop.

$$\bar{u}_{out} = \bar{u}_{out\_a} - \bar{u}_{out\_b} = \frac{U_{DC}}{2} * (\bar{s}_a - \bar{s}_b) = \frac{U_{DC}}{2} * \bar{s}_{DM} \tag{47}$$

$$\bar{i}_{out\_a} = -\bar{i}_{out\_b} \tag{48}$$

$$\bar{i}_{NP} = \bar{i}_{out\_a} * ((1 - abs(\bar{s}_a)) - (1 - abs(\bar{s}_b))) = \bar{i}_{out\_a} * (abs(\bar{s}_b) - abs(\bar{s}_a)) \tag{49}$$

$$\bar{s}_a \le 0 \wedge \bar{s}_b \le 0 \rightarrow \bar{i}_{NP} = \bar{i}_{out\_a} * (\bar{s}_a - \bar{s}_b) = \bar{i}_{out\_a} * \bar{s}_{DM} \tag{50}$$

$$\bar{s}_a \ge 0 \wedge \bar{s}_b \ge 0 \rightarrow \bar{i}_{NP} = \bar{i}_{out\_a} * (\bar{s}_b - \bar{s}_a) = -\bar{i}_{out\_a} * \bar{s}_{DM} \tag{51}$$

$$\bar{s}_a \ge 0 \wedge \bar{s}_b \le 0 \rightarrow \bar{i}_{NP} = -\bar{i}_{out\_a} * (\bar{s}_b + \bar{s}_a) = -\bar{i}_{out\_a} * 2 * \bar{s}_{CM} \tag{52}$$

$$\bar{s}_a \le 0 \wedge \bar{s}_b \ge 0 \rightarrow \bar{i}_{NP} = \bar{i}_{out\_a} * (\bar{s}_b + \bar{s}_a) = \bar{i}_{out\_a} * 2 * \bar{s}_{CM} \tag{53}$$

The two phase legs can be operated with zero common mode (opposing output voltage ratios: $r_1 = -r_2$) to obtain symmetry; the resulting NP current is zero. If the two output voltage ratios have different signs, both gradients have the same sign and the resulting NP current is a linear function of the CM voltage. If both output voltage ratios have the same signs, the two gradients have opposing signs, so that the gradient of the sum of the two functions is zero. The total NP current is then defined by the DM voltage alone. The resulting function of the NP current in function of the CM voltage is a piecewise linear function as shown in Figure 59 b). This function is always monotonic but can go into saturation. A good control scheme for the NP current should take this into account and limit the CM voltage to the area, where there is an impact on the NP current.

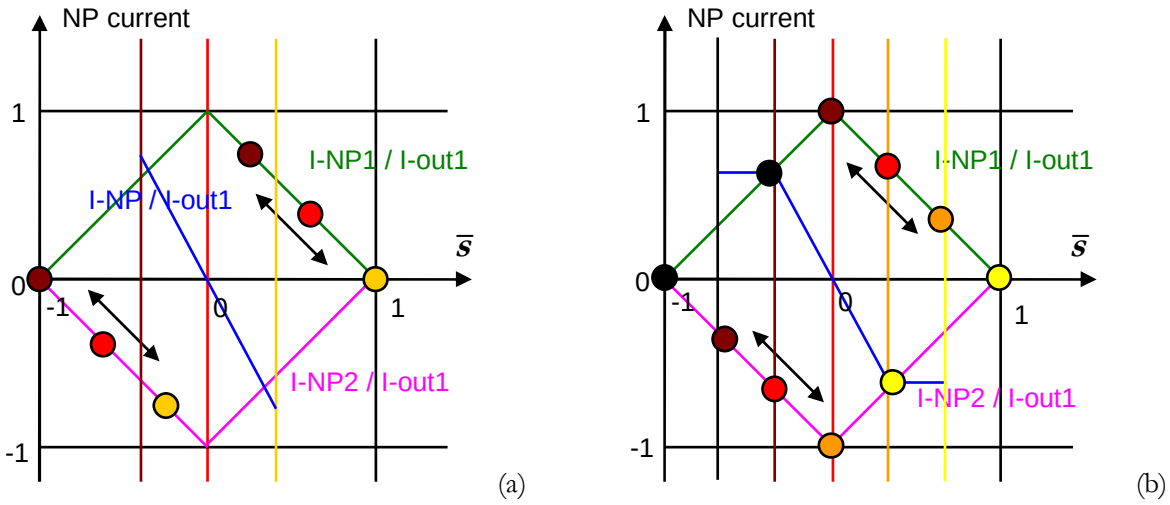


Figure 59, NP current range with H-bridge

4.7.1.2 Three phase system

In a typical three phase converter system, there are three phase legs sharing one common DC link. The load is not grounded in most application, which means there is no path for a CM current, the sum of the output currents is zero:

$$i_{out1} + i_{out2} + i_{out3} = 0 \tag{54}$$

The neutral point current is the sum of the three individual NP currents:

$$\bar{i}_{NPtot} = \bar{i}_{out1} * (1 - abs(\bar{s}_1)) + \bar{i}_{out2} * (1 - abs(\bar{s}_2)) + \bar{i}_{out3} * (1 - abs(\bar{s}_3)) \tag{55}$$

$$\bar{i}_{NPtot} = \bar{i}_{out1} - \bar{i}_{out1} * abs(\bar{s}_1) + \bar{i}_{out2} - \bar{i}_{out2} * abs(\bar{s}_2) + \bar{i}_{out3} - \bar{i}_{out3} * abs(\bar{s}_3) \tag{56}$$

$$\bar{i}_{NPtot} = -(\bar{i}_{out1} * abs(\bar{s}_1) + \bar{i}_{out2} * abs(\bar{s}_2) + \bar{i}_{out3} * abs(\bar{s}_3)) \tag{57}$$

The individual NP current function can be represented in a single graph with normalization with one of the three phase currents (e.g. the largest one) as indicated in Figure 60. The average switching function $\bar{s}$ is going from -1 to 1 for each phase.

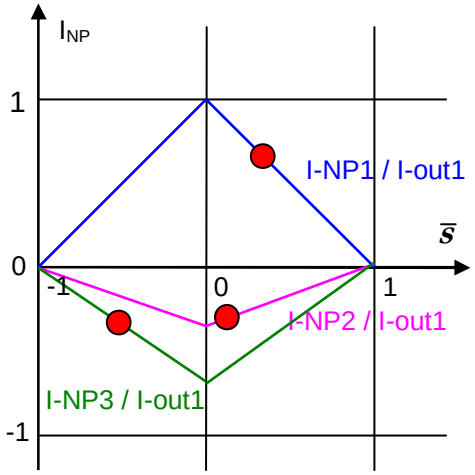


Figure 60, NP point currents in 3 phase system

It can be seen from (57) and Figure 60 that not only the output currents add up to zero, but also the gradients of the piecewise linear functions, if all $\bar{s}_x$ have the same sign.

$$\frac{d\bar{i}_{NP1}(\bar{s}_1<0)}{d\bar{s}_{CM}}+\frac{d\bar{i}_{NP2}(\bar{s}_2<0)}{d\bar{s}_{CM}}+\frac{d\bar{i}_{NP3}(\bar{s}_3<0)}{d\bar{s}_{CM}}=0 \tag{58}$$

$$\frac{d\bar{i}_{NP1}(\bar{s}_1>0)}{d\bar{s}_{CM}}+\frac{d\bar{i}_{NP2}(\bar{s}_2>0)}{d\bar{s}_{CM}}+\frac{d\bar{i}_{NP3}(\bar{s}_3>0)}{d\bar{s}_{CM}}=0 \tag{59}$$

The gradient functions for each phase only take on two distinct values, one positive and one negative number of the same absolute value with positive and negative sign. If a differential output voltage is given, the NP current can be calculated in function of the CM voltage. This means a CM term $\bar{s}_{CM}$ can be added to the given set of average switching functions. Based on the above, we can state that the gradient of the overall NP current function is constant for varying $\bar{s}_{CM}$ as long as none of the resulting phase modulation indices crosses the zero point. Each zero crossing the average switching function in any of the phases changes the overall NP current gradient, unless the current in the corresponding phase is zero. The resulting function is a piecewise linear function with a maximum of 3 singularities and 4 linear sections. The actual physically available range of that function is constrained as none of the voltages may assume values outside of the DC link voltage range. Therefore, five operating points define the Neutral point current in function of the applied common mode voltage (see Figure 61, five points per phase, P1 to P5). These points are defined by any one phase assuming the value -1, 0 or 1. This is valid independently of the balance and symmetry of the system, as it uses instantaneous values. Each color in Figure 61 is representing a certain common mode voltage (the line indicating the common mode voltage, the dots representing the individual average switching functions and the NP currents of the three phases).

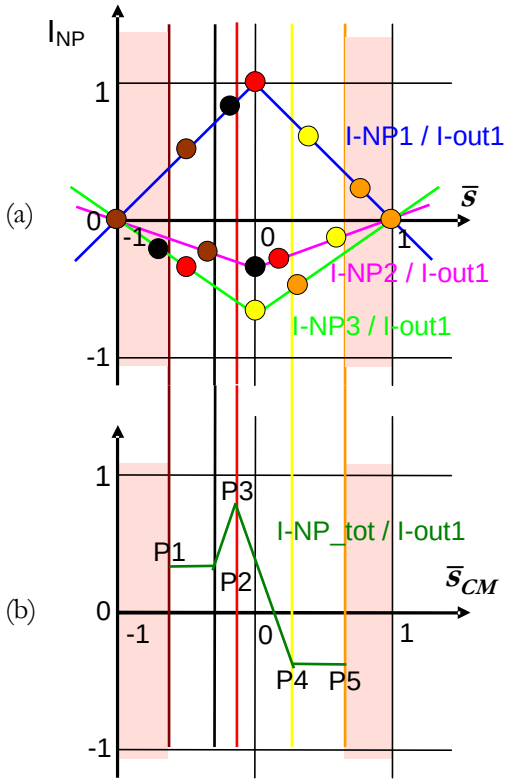


Figure 61: NP currents in 3-phase system (a), NP current in function of CM voltage (b)

The maximum of four linear sections in the piecewise linear NP current function are characterized by two horizontal sections at the beginning and the end (based on equations (58) and (59)) and by two inclined section in the middle. The NP current values for the horizontal sections and the singularity P3 of the piecewise linear function can be calculated directly from the triangular shape NP current function per phase (x, y and z referring to any of the phases a, b or c):

$$\bar{s}_x > 0 \wedge \bar{s}_y > 0 \wedge \bar{s}_z > 0 \rightarrow I_{NP}\big|_{P1} = I_{NP}\big|_{P2} = -\bar{s}_x i_x - \bar{s}_y i_y - \bar{s}_z i_z \tag{60}$$

$$\bar{s}_x < 0 \wedge \bar{s}_y < 0 \wedge \bar{s}_z < 0 \rightarrow I_{NP}\big|_{P4} = I_{NP}\big|_{P5} = \bar{s}_x i_x + \bar{s}_y i_y + \bar{s}_z i_z \tag{61}$$

$$\bar{s}_x < 0 \wedge \bar{s}_y = 0 \wedge \bar{s}_z > 0 \rightarrow I_{NP}\big|_{P3} = \bar{s}_x i_x - \bar{s}_z i_z \tag{62}$$

For the inclined section left of point P3 in Figure 61, two voltages are negative and one is positive; for the inclined section right of point 3, two voltages are positive and one is negative. Equivalent to (58) and (59), we can also state:

$$\bar{s}_x < 0 \wedge \bar{s}_y > 0 \wedge \bar{s}_z > 0 \rightarrow \frac{dI_{NPx}(\bar{s}_x)}{d\bar{s}_{CM}} = \frac{dI_{NPy}(\bar{s}_y)}{d\bar{s}_{CM}} + \frac{dI_{NPz}(\bar{s}_z)}{d\bar{s}_{CM}} \tag{63}$$

$$\bar{s}_x < 0 \wedge \bar{s}_y < 0 \wedge \bar{s}_z > 0 \rightarrow \frac{dI_{NPx}(\bar{s}_x)}{d\bar{s}_{CM}} + \frac{dI_{NPy}(\bar{s}_y)}{d\bar{s}_{CM}} = \frac{dI_{NPz}(\bar{s}_z)}{d\bar{s}_{CM}} \tag{64}$$

The individual gradients per phase are:

$$\bar{s}_x < 0 \rightarrow \frac{dI_{NPx}(\bar{s}_x)}{d\bar{s}_{CM}} = \frac{I_{outx}}{U_{DC}/2} = \frac{2I_{outx}}{U_{DC}} \tag{65}$$

$$\bar{s}_x > 0 \rightarrow \frac{dI_{NPx}(\bar{s}_x)}{d\bar{s}_{CM}} = -\frac{I_{outx}}{U_{DC}/2} = -\frac{2I_{outx}}{U_{DC}} \tag{66}$$

Using (63), (64), (65), and (66) we get:

$$\bar{s}_x < 0 \wedge \bar{s}_y > 0 \wedge \bar{s}_z > 0 \rightarrow \frac{dI_{NP\_tot}}{d\bar{s}_{CM}} = \frac{4I_{out\_x}}{U_{DC}} \tag{67}$$

$$\bar{s}_x < 0 \wedge \bar{s}_y < 0 \wedge \bar{s}_z > 0 \rightarrow \frac{dI_{NP\_tot}}{d\bar{s}_{CM}} = -\frac{4I_{out\_z}}{U_{DC}} \tag{68}$$

The gradient in the NP current function is always defined by the current in the phase with the unique sign in the average switching function. The two gradients in the middle section may have the same sign or a different sign, which means the function may be monotonic or non monotonic, depending on operating point. An analysis of all possible operating points shows that non-monotonic behavior occurs for low cos(φ). This function can be determined for every operating point with any given voltage and current vector. The function is dynamically changing with time. Accordingly, any control scheme making use of the true NP current function must either determine it online or pre-calculate all possible operating points. One example is given in Figure 62. An overview of different operating points is given in appendix 9.6.

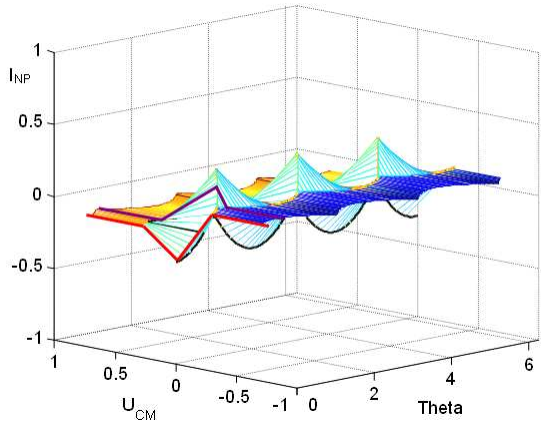


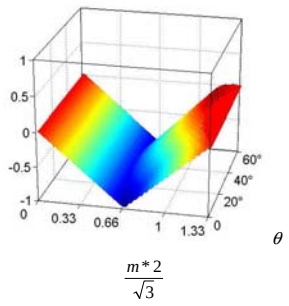
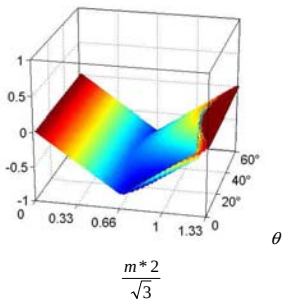
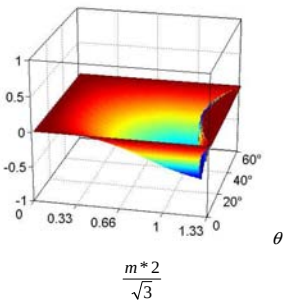
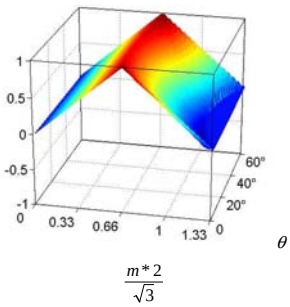
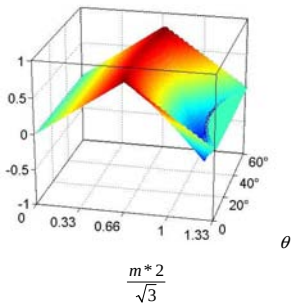
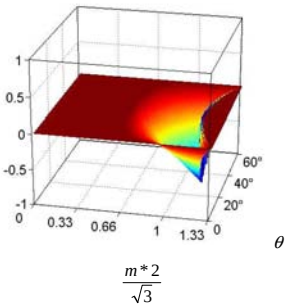
Figure 62, NP current as function of θ and CM voltage, m = 0.3, φ = 1.4

4.7.2 NP current characteristics as a function of m, φ and θ

Maximum and minimum achievable NP currents are a measure for the controllability of the NP voltage. High NP currents enable a fast change (and thus control) of the NP voltage. Minimum

and maximum NP currents can easily be determined by the known NP current function in each operating point as presented in the previous paragraph.

TABLE 23, MINIMUM AND MAXIMUM NP CURRENT IN DIFFERENT OPERATION POINTS APPLYING STANDARD MODULATION SCHEMES, APPLIES TO ALL TYPE OF 3-L DC LINK CONVERTERS

	cos(φ)=1	cos(φ)=0.81 (inductive)	cos(φ)=0 (inductive)
I_{NP}-min			
I_{NP}-max			

Appendix 9.5.1 gives an overview of maximum and minimum NP currents in different operating points.

4.7.3 Zero average NP current areas in function of CM

Zero NP current operation is desirable to keep the low frequency NP voltage ripple as low as possible. Limits of the zero average NP current can easily be determined from the NP current function. If the NP current function crosses the zero line within the allowable operating range of the CM voltage (e.g. as in Figure 61), zero neutral point current operation is possible in the given operating point with the appropriate CM voltage. If it does not cross the zero line, zero NP current is not possible. Figure 63 shows the zero average NP current limits for a variety of load angles.

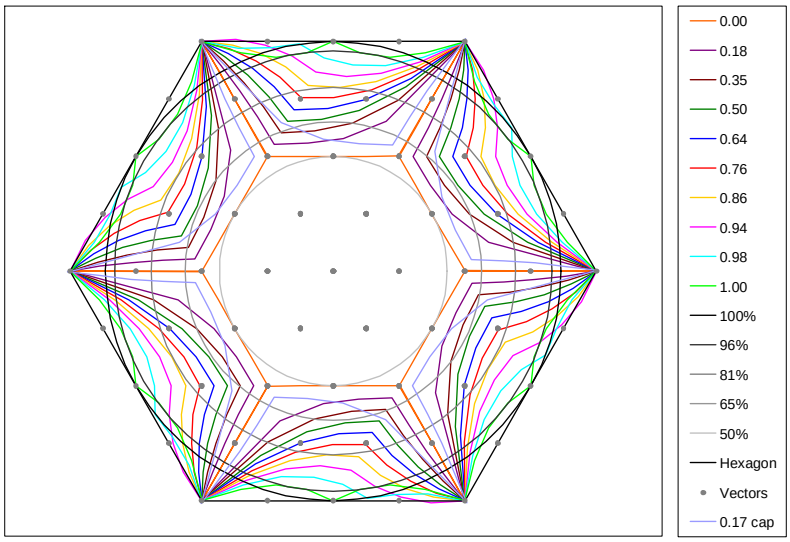


Figure 63, Zero average NP current limitations for standard modulation

Figure 63 can be read as follows:

1. The curves 0.00 to 1.00 indicate the operating limits for the corresponding cos(φ) with lagging output current (inductive operation).
2. Every point within (towards the center of the hexagon) the indicated operating limit can operate at zero average NP current (with a suitable CM voltage)
3. Every point outside the indicated operating limit cannot operate at zero average NP current. A low frequency NP current ripple will be generated.
4. The circles 50% to 100% indicate the modulation depth (m = 0.5 to 1) of balanced output voltages.
5. For leading currents, there is a symmetry as indicated with one example of cos(φ)=0.17 capacitive. The limiting curves for all other capacitive (load or generator) cos(φ) will look accordingly (mirrored from the inductive curves).

Jiang [84] has made an analysis of NP balance for the NPC based on SVM, including the calculation of zero average NP current limits. His results correspond exactly with Figure 63. The outcome of this analysis does not depend on the modulation scheme considered (as it should be). See appendix 9.6 for the shape of the minimum NP current outside of the zero NP current areas.

4.8 NP current as a function of input current and switching function harmonics

The NP current is a function of output currents and the switching functions of the inverter as shown in (45). The same relation ship is true if the instantaneous switching function $s_x(t)$ is used.

$$i_{NPx}(t) = i_x(t) * (1 - abs(s_x(t))) \tag{69}$$

To understand what impact harmonics in load current and in the switching function have, a relationship in the frequency domain is required. However, this is very complex, as there is no simple transformation of the absolute value function into the frequency domain. Phase and amplitude of all individual harmonics have an impact on the presence of zero crossings of $s_x(t)$ and therefore not just quantitatively but also qualitatively influence the absolute value function. A simple analytically closed solution has not been published so far and does not seem to be possible.

A few papers assume harmonics in the load current but sinusoidal modulation, which is mathematically less complex but still meaningful in practice. [104] determines the relevant current harmonics (non-triple even harmonics) generating a DC NP current. [92] gives some curves for the impact of specific harmonics (2nd and 4th) in the load current on the NP DC current. Marchesoni proposes a NP control schemes based on load harmonics [91] and needs a relationship between load harmonics and NP currents for that purpose. He too uses sinusoidal modulation and approximations due to the lack of precise analytical solutions. Pou [105] analyzes the impact of linear but unbalances systems (load currents composed only of positive and negative sequence fundamental components) as well as nonlinear load (specifically with 2nd and 4th order harmonics). As a result, he determines the limits of 2nd and 4th harmonic content for stable operation using SVM. Although he states the NP current in function of output currents and switching states, he does not need to establish a relationship between the spectrum of the switching function and the spectrum of the load current for his purpose.

Scheuer [106] proposes to use the square function in (70) to approximate (69). For a function s taking exclusively the values -1, 0 and 1 as would be the case for the discrete states in a 3-L converter, (69) and (70) are equal. This approximation can therefore be used if the exact switching pattern is used (no averaging) in the case of 3-L converters.

$$i_{NPx}(t) = i_x(t) * (1 - s_x^{\,2}(t)) \tag{70}$$

In contrast to the absolute value function the spectrum of $s_x^2(t)$ can be calculated. The resulting spectrum can then be combined with the input current spectrum to obtain the NP current spectrum. However, the two functions do not correspond if $s_x(t)$ assumes any other value than -1, 0 or 1. In the case of the 5-L converter $s_x(t)$ can assume also -0.5 and +0.5, resulting in a poor approximation of the true NP current. An approximation of (45) using the square of the average switching function is not possible at all as $\bar{s}_x(t)$ is a continuous function from -1 to 1. Therefore square approximation according to (70) is not used in this document.

Another type of simplification is proposed below, giving exact result in the considered operating range. If there is no DC offset and only a single zero crossing per half period, the

functions can be described in closed form. The result of the rectification can be calculated for each harmonic individually:

1. Each harmonic is inverted in the second half of the fundamental period (assuming zero phase shift of the fundamental)
2. As a result only the fundamental is rectified. All others remain AC values, but with a changed spectrum.
3. Harmonics can then be combined and the complex spectra can be added.
4. If the harmonics are injected without phase shift (which is the normal case for 3rd harmonic injection and 6th harmonic injection), the resulting harmonics of the new functions also have zero phase. This means the absolute values of the different spectra can be added directly.

In a general approach, the function $s_x(t)$ shall be constrained in the following way:

1. The function $s_x(t)$ shall contain either harmonics or a DC component, but not both at the same time
2. The function $s_x(t)$ shall have exactly two equidistant zero crossings per fundamental period.
3. The position of the zero crossings shall be determined by the fundamental term alone

Consequently, there are two distinct cases to be analyzed:

$$\bar{i}_{NPx}(t) = \bar{i}_x(t) * (1 - abs(k_x + m_x \sin(\omega t))) \tag{71}$$

Note that there is no general function $s_x(t)$ specified in (71) but the function $k_x+m_x sin(\omega t)$. This means the equation is only applicable for a pure sine with a DC component.

$$\bar{i}_{NPx}(t) = \bar{i}_x(t) * (1 - (\bar{s}_x(t) * sign(\sin(\omega t)))) \tag{72}$$

This is applicable for any function with a dominant fundamental according to the above constraints and no DC component. Both spectra can be determined in closed form. The imposed constraints are of course a restriction not applicable in all cases in reality. Nonetheless, it is possible to derive quite universal control laws, as will be shown in the next chapter.

4.8.1 DC offset analysis

A DC offset in the switching function $\bar{s}_x(t)$ results in specific harmonics in the rectified switching function $abs(\bar{s}_x(t))$.

TABLE 24, HARMONICS IN RECTIFIED SWITCHING FUNCTION ABS(S(T)) IN FUNCTION OF DC OFFSET

		DC offset in $\bar{s}_x(t)$ (fundamental_peak = 1)										
Harmonics in rectified function $abs(\bar{s}_x(t))$		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
DC		0.637	0.640	0.649	0.665	0.688	0.718	0.755	0.800	0.854	0.919	1.000
1st		**0.000**	**0.127**	**0.253**	**0.376**	**0.495**	**0.609**	**0.715**	**0.812**	**0.896**	**0.963**	**1.000**
2nd		0.424	0.418	0.399	0.368	0.327	0.276	0.217	0.155	0.092	0.035	0.000
3rd		0.000	0.042	0.080	0.111	0.131	0.138	0.130	0.108	0.073	0.032	0.000
4th		0.085	0.079	0.061	0.034	0.003	0.028	0.050	0.060	0.052	0.027	0.000
5th		0.000	0.024	0.043	0.050	0.045	0.028	0.003	0.020	0.031	0.022	0.000
6th		0.036	0.030	0.014	0.007	0.025	0.032	0.024	0.006	0.013	0.017	0.000
7th		0.000	0.017	0.026	0.022	0.008	0.010	0.020	0.016	0.000	0.012	0.000
8th		0.020	0.014	0.000	0.014	0.018	0.010	0.005	0.014	0.007	0.007	0.000
9th		0.000	0.012	0.015	0.006	0.007	0.014	0.007	0.006	0.009	0.003	0.000
10th		0.013	0.007	0.005	0.012	0.007	0.005	0.010	0.002	0.007	0.000	0.000
11th		0.000	0.009	0.008	0.002	0.009	0.005	0.006	0.006	0.004	0.002	0.000
12th		0.009	0.003	0.006	0.008	0.002	0.008	0.001	0.006	0.000	0.003	0.000
13th		0.000	0.007	0.004	0.005	0.006	0.003	0.005	0.003	0.003	0.003	0.000

Note that only even harmonics are present in the rectified switching function without DC offset. The DC component and the 2nd order harmonic are very dominant in this case. With rising DC offset, also odd harmonics appear with relatively low amplitude. Most importantly, a fundamental term steadily rising from 0 to 1 is generated with rising DC offset. This fundamental term is most relevant as it results into a DC NP current when combined with the input current (the multiplication in the time domain corresponds with a convolution in the frequency domain). This term is therefore very useful for the design of a NP controller, as well known from most concepts according to the state of the art. It is also well known that this only works for the active power component, as this is in phase with the fundamental component of the rectified switching function. The reactive power component of the input current is phase shifted by $\pi/2$ and does not generate any DC NP current. Alternate solutions are required for the pure reactive case.

There are three possibilities to generate a DC NP current besides the DC offset approach:

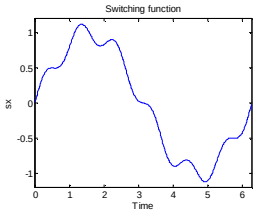
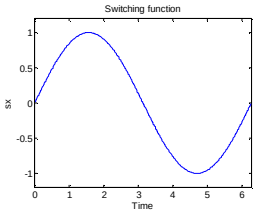
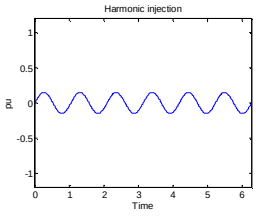
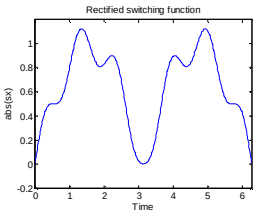
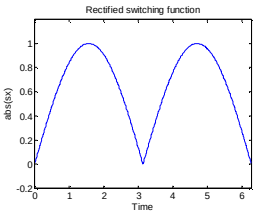
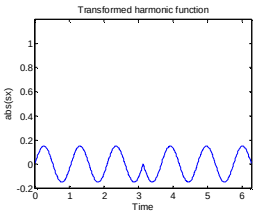
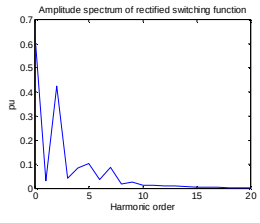
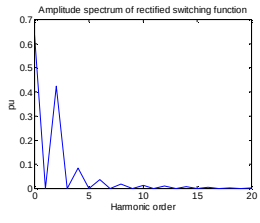
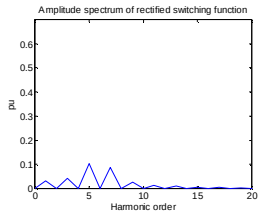
- A DC component in the input current
- Higher order harmonics in input current and rectified switching function can be used
- A fundamental with a $\pi/2$ (plus/minus) phase shift can be generated in the rectified switching function

The first possibility is not practical, as most applications do not allow having a DC CM current. The other two concepts are addressed in the following paragraphs.

4.8.2 Harmonic injection analysis

With a dominant fundamental component all harmonics are multiplied with the sign of the fundamental when rectified. This is illustrated with the example of a 6th harmonic component in TABLE 25.

TABLE 25, HARMONICS IN RECTIFIED SWITCHING FUNCTION ABS(S(T)) IN FUNCTION OF HARMONIC CONTENT OF S(T)

	Combined function	**Fundamental component**	**Harmonic component**
Switching function $\bar{s}_x(t)$	 (a)	 (b)	 (c)
Rectified switching function $abs(\bar{s}_x(t))$	 (d)	 (e)	 (f)
Spectrum of rectified switching function $S_x(\omega)$	 (g)	 (h)	 (i)

The total (complex) harmonic spectrum of the rectified switching function $S_{rect\_x}(\omega)$ is the sum of spectra of the individual transformed fundamental and harmonic components $S_{trans\_x\_n}(\omega)$, n indicating the harmonic order number starting from 1 (the DC component is zero as previously defined). Each phase has its own spectrum with x being the index for one of the three phases.

$$S_{rect\_x}(\omega) = \sum_{n=1}^{\infty} S_{trans\_x\_n}(\omega) \tag{73}$$

with

$$s_{trans\_x\_n}(t) = \sin(n * \omega t + \varphi_{nx}) * sign(\sin(\omega t + \varphi_{1x})) \quad (74)$$

The following table lists pre-calculated amplitude spectra of the transformed harmonic component. The first row corresponds with (h) in TABLE 25, the 6th row (scaled with 0.15) with (i). The fundamental term in the rectified switching function is very important, as it will generate a DC NP current component by multiplication with the fundamental output current. To generate a large DC NP current, large fundamental in the rectified switching function should be generated.

TABLE 26, HARMONICS IN RECTIFIED SWITCHING FUNCTION ABS(S(T)) IN FUNCTION OF HARMONIC COMPONENTS OF THE SWITCHING FUNCTION S(T)

	Harmonic component in switching function $\bar{s}_x(t)$								
Resulting harmonics in rectified function $abs(\bar{s}_x(t))$	1st	2nd	3rd	4th	5th	**6th**	7th	8th	9th
DC	0.637	0.000	0.212	0.000	0.127	**0.000**	0.091	0.000	0.071
1st	**0.000**	**0.849**	**0.000**	**0.340**	**0.000**	**0.218**	**0.000**	**0.162**	**0.000**
2nd	0.424	0.000	0.764	0.000	0.303	**0.000**	0.198	0.000	0.149
3rd	0.000	0.509	0.000	0.728	0.000	**0.283**	0.000	0.185	0.000
4th	0.085	0.000	0.546	0.000	0.707	**0.000**	0.270	0.000	0.176
5th	0.000	0.121	0.000	0.566	0.000	**0.694**	0.000	0.261	0.000
6th	0.036	0.000	0.141	0.000	0.579	**0.000**	0.686	0.000	0.255
7th	0.000	0.057	0.000	0.154	0.000	**0.588**	0.000	0.679	0.000
8th	0.020	0.000	0.069	0.000	0.163	**0.000**	0.594	0.000	0.674
9th	0.000	0.033	0.000	0.078	0.000	**0.170**	0.000	0.599	0.000
10th	0.013	0.000	0.042	0.000	0.085	**0.000**	0.175	0.000	0.603
11th	0.000	0.022	0.000	0.049	0.000	**0.090**	0.000	0.179	0.000
12th	0.009	0.000	0.028	0.000	0.054	**0.000**	0.094	0.000	0.182
13th	0.000	0.015	0.000	0.033	0.000	**0.057**	0.000	0.097	0.000

As can be seen from TABLE 26, any even harmonic in the switching function can be used to generate a fundamental term (or any other odd harmonic) in the rectified switching function. This is of interest, as a fundamental term in the rectified switching function interacts with the fundamental term of the output current and generates a DC NP current (see next paragraph). In practice, only zero sequence harmonic injection is useful, as all other harmonics lead either to a distortion of the output signal (if the harmonic injection is phase shifted) or to an unsymmetrical system (if there is the same CM harmonic injection without phase shift in all three phases). The sixth harmonic is the first and most powerful zero sequence harmonic with a generation of a

fundamental in the rectified switching function. This fundamental is phase shifted by $\pi/2$ compared to the one generated by DC CM injection.

4.8.3 Relationship between harmonic orders of input current and switching function

The preceding two paragraphs have pointed out the quantitative relationship between switching function harmonics and rectified switching function harmonics. This information can now be related to the input current harmonics.

As the input current needs to be multiplied with the rectified switching function as shown in (45), there is a convolution in the frequency domain.

$$S_{I\_NP\_x}(\omega) = S_{I\_out\_x}(\omega) \bullet S_{rect\_x}(\omega) \tag{75}$$

Accordingly, a qualitative relationship matrix can be established.

TABLE 27, RELATIONSHIP BETWEEN HARMONIC ORDERS OF LINE SIDE CURRENT, THE RECTIFIED SWITCHING AND THE NP CURRENT PER PHASE

	Harmonic order of I_{NP_x}									
Harmonic order of I_{out_x}	**DC**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
DC	DC	1	2	3	4	5	6	7	8	9
1	1	DC	1	2	3	4	5	6	7	8
2	2	1	DC	1	2	3	4	5	6	7
3	3	2	1	DC	1	2	3	4	5	6
4	4	3	2	1	DC	1	2	3	4	5
5	5	4	3	2	1	DC	1	2	3	4
6	6	5	4	3	2	1	DC	1	2	3
7	7	6	5	4	3	2	1	DC	1	2
8	8	7	6	5	4	3	2	1	DC	1
9	9	8	7	6	5	4	3	2	1	DC
	abs(s_x(t))									

The rectified switching function abs(s_x(t)) has normally predominantly even terms, based on the fundamental and the 3rd harmonic in the switching function s_x(t), as shown in TABLE 26 in the previous paragraph. In steady state operation without DC offset or additional harmonics and pure sinusoidal input current, this will generate all odd harmonics in the NP current, including a fundamental term.

A similar table as above can be drawn based on the actual switching function $s_x(t)$ instead of $abs(s_x(t))$. However, such a table includes much more components, as all the harmonic terms in $abs(s_x(t))$ can be generated by multiple terms in $s_x(t)$. TABLE 28 includes the most important components only; in reality an infinite number of higher harmonic terms apply to each field, with decreasing importance. All positive and negative sequence NP currents will cancel out in the neutral point, if the system is symmetrical and balanced. The remaining harmonics visible in the NP current and consequently in the NP voltage are 3rd, 9th, 15th etc. Therefore only zero sequence NP currents are shown in TABLE 28. On the line side only positive and negative sequence currents are considered, as zero sequence currents are not present in three wire systems.

TABLE 28, RELATIONSHIP BETWEEN HARMONIC ORDERS OF LINE SIDE CURRENT, THE SWITCHING FUNCTION S(T) AND THE OVERALL NP CURRENT

	I-NP									
AC side current	**DC**	1	2	**3**	4	5	**6**	7	8	**9**
DC										
1	**DC / 2nd / 6th**			**1st / 3rd**			4th / 6th			**7th** / 9th
2	**1st / 3rd**			DC / 2nd / 6th			3rd / 5th			6th / 8th
3										
4	3rd / 5th			DC / 2nd / 6th			1st / 3rd			4th / 6th
5	4th / **6th**			**1st / 3rd**			**DC** / 2nd / 6th			**3rd / 5th**
6										
7	**6th** / 8th			**3rd / 5th**			**DC** / 2nd / 6th			**1st / 3rd**
8	7th / 9th			4th / 6th			1st / 3rd			DC / 2nd / 6th
9										
	s(t)									

This overview helps to understand both how the NP can be disturbed and how it can be controlled. The input ideally only contains a fundamental and high order harmonics generated by the switching function as it is actively controlled. In reality, the input voltage (line voltage or motor back EMF) may contain low order harmonics also generating input current harmonics if not actively eliminated. These harmonics are typically odd harmonics. The convolution of input current and rectified switching function then leads primarily to odd NP current harmonics, as the rectified switching function contains primarily even harmonics (see TABLE 27). This is not very significant as there is no DC and amplitudes are low. If however there are odd harmonics in the rectified switching function, a DC NP current can be generated. If there are even harmonics present (2nd, 4th, etc.) in the output current, they interact with the fundamental and the 3rd of the switching function and result in a DC NP current.

To control the NP, it is best to focus on a scheme using the fundamental input current, as the presence of current harmonics is uncertain. This means that mainly a fundamental in the rectified switching function can be used to generate a DC NP current. A fundamental in the rectified switching function can be obtained by applying a DC offset or an even harmonic term to the

switching function, as pointed out in TABLE 24 and TABLE 26. This is also documented in TABLE 27, which qualitatively indicates how a suitable DC NP current can be generated. DC injection leads to a fundamental in the rectified switching function in phase with the fundamental of the switching function; harmonic injection leads to phase change of $\pi/2$ (note that this is only true for a dominant fundamental term in the switching function; otherwise, higher harmonic terms are predominantly generated). DC injection therefore works for active power, where the output current is in phase with the voltage; even harmonic injection works for reactive power, where current and voltage are phase shifted.

In the over modulation region, 3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} in the switching function $s_x(t)$ are very pronounced. Consequently, the rectified switching function has a high content of all even harmonics.

- Odd harmonics in the line current are likely to be present due to the harmonic content of the switching function in over-modulation. This couples back to odd multiples of three in the NP current.
- If there are even harmonics like 2^{nd} or 4^{th} present in the line current, they generate DC and even multiples of three in the NP current. Note that symmetrical over-modulation does not generate even harmonics in the line current, but they can be generated by an additional even term in the switching function.
- All mechanisms listed in the second column (I-NP / DC) of TABLE 28 can contribute to a DC NP current. These mechanisms may add up or compensate each other depending on the operating conditions. This is critical in over modulation, as standard NP control schemes are weak in this operating point.

4.9 Executive summary for chapter 4

3-L DC link converters with flying capacitors need voltage control both for flying capacitors and neutral point. An introduction to NP and FC control is given and the high importance of the redundant states for the controllability is demonstrated. An analysis of the converter states of the ANPC 1 reveals redundant states with the same output voltage but opposing currents in the flying capacitors. The flying capacitor can be fully controlled by appropriate application of those redundant states. The impact on the NP current is statistically cancelled out with standard modulation schemes.

Standard modulation schemes according to the state of the art use primarily CM voltage to control the NP current. It is therefore crucial to understand the relationship between CM voltage and NP current for the design of a proper controller. It is shown that all 3-L DC link topologies have the same NP current as a function of CM voltage, if any standard modulator with decoupled FC and NP control is used. More sophisticated modulation schemes utilizing redundant states also for NP control are possible and will be introduced in the following chapters.

The instantaneous NP current as a function of CM voltage for standard modulation is analyzed for multiphase systems in various operating points. It is shown that this is a time piecewise linear function that can easily be determined graphically and has the following properties:

1. There are always 3 singularities and 4 linear sections
2. The singularities are given by the placement of any of the three output voltages on the NP potential (zero output for one phase)
3. The two outer linear sections towards infinity always have zero gradient with the same NP current amplitude but opposite signs
4. The two inner linear sections connecting the singularities may have the same or different sign of the gradient depending on the operating point. The function may thus be monotonic or non monotonic
5. The NP current function is physically limited. All four, two inner or only one inner section may be physically reachable, depending on load angle and modulation depth.
6. Only the two inner sections are useful for NP control. Any change of CM voltage in the outer section region has no impact on the NP current.
7. The function depends on DM voltage and load current and therefore changes over time.

The shape of the NP current function is highly important for NP control. Namely for reactive power operation with non monotonic NP current characteristic, suitable NP control schemes are required. A simple proportional feedback with DC CM injection does not work in this case. More general schemes are proposed in the next chapter.

This chapter also analyzes the relationship between NP current, average switching function and load current in the frequency domain. This is mathematically not straight forward as the NP current as a function of the average switching function includes the absolute value function, which cannot be translated easily into the frequency domain. An approach with a simple closed solution for two specific special cases is presented.

- Sinusoidal average switching function with DC CM offset but no harmonics
- Sinusoidal average switching function with dominant fundamental, harmonics of any order but no DC CM offset.

These two cases can be analytically calculated in closed form. Both are highly useful for a basic understanding of NP current characteristics and its behavior under disturbance conditions. They can also be used for the design of a NP current controller, as will be demonstrated in the next chapter. The key findings regarding harmonic relationships are:

- A 2^{nd} harmonic on the line side generates a relatively large DC NP current due to the fundamental and the 3^{rd} harmonic in the switching function. This effect can also be used actively by generating a 2^{nd} line current harmonic on purpose.
- If there are 5^{th} and the 7^{th} harmonics in the line current, they predominantly result in 3^{rd} and 9^{th} harmonic in the NP current, as they are coupled through the fundamental and the 3^{rd} in the switching function. This is usually not very relevant in operation, as amplitudes are normally low.
- A third harmonic is present in the NP current, if not compensated, due to the fundamental and the 3^{rd} harmonic in the switching function.
- DC CM injection is most effective for DC NP current generation in active power operation.
- 2^{nd} and 6^{th} harmonic CM injection are most effective for DC NP current generation in reactive power operation.

5 NP CONTROL WITH CARRIER BASED PWM

This chapter introduces several new carrier based PWM schemes for improved NP and FC voltage control. The first two modulation schemes proposed use CM voltage injection only and can be applied to any 3-L DC link converter including the NPC. Knowledge of the NP current as a function of CM voltage is used in real-time to control the NP point. The first scheme proposed operates purely in time domain and injects a CM voltage based on instantaneous values. The second scheme makes use of harmonic relationships presented in chapter 4 and injects specific harmonics in the CM voltage. Both schemes offer the same NP current control capability as some SVM schemes proposed in literature. However, they offer a high degree of freedom regarding the base modulation type and thus allow including additional objectives like THD minimization (as for example optimized CB PWM schemes like CSPD PWM can be used) or switching loss minimization.

The carrier based schemes presented in the second part of the chapter are topology specific, as they make use of redundant states. Carrier waveforms are designed such that specific redundant states are combined. Solutions for very efficient NP control are proposed for the SMC and the ANPC type 3. The NP control capacity of these schemes is significantly beyond the capacity of standard schemes only utilizing CM voltage.

5.1 Real time NP current function control scheme

This scheme can be used for all 3-L DC link topologies.

5.1.1 Background

The neutral point in 3-L based (input) converter systems can be controlled by a CM voltage injection. In the case of active power, a DC common mode voltage will generate a DC NP current (with superimposed AC currents at various frequencies). This allows to implement relatively simple control schemes (although the exact relationship of common mode voltage with NP current is relatively complex) to control the NP voltage. In the case of reactive power, a DC common mode voltage will generate an AC NP current (at various frequencies), so the same control schemes as for active power cannot be applied anymore. In other words, unconstrained linear feedback control with DC CM injection based on a linear approximation of the NP current function works fine for a wide operating range but delivers poor results for low $\cos(\varphi)$. This is obvious when looking at the sample NP current function in Figure 64. The endpoints provide very low NP current and the useful range (between min. and max.) of the NP function is much smaller than the physically available range. If a single linearized function is used for feedback, the result may even be counter productive as the real non-monotonic function is changing its sign of the gradient. However, as Figure 64 indicates, a suitable CM injection based on the instantaneous characteristics of the function will generate a useful NP current.

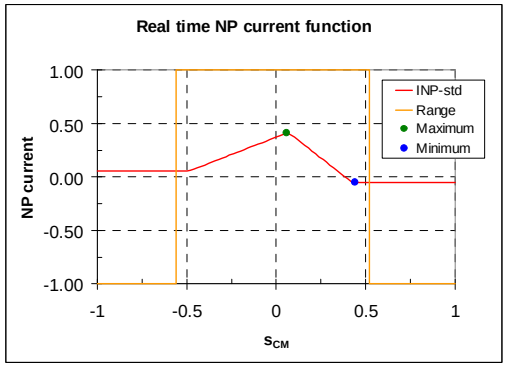
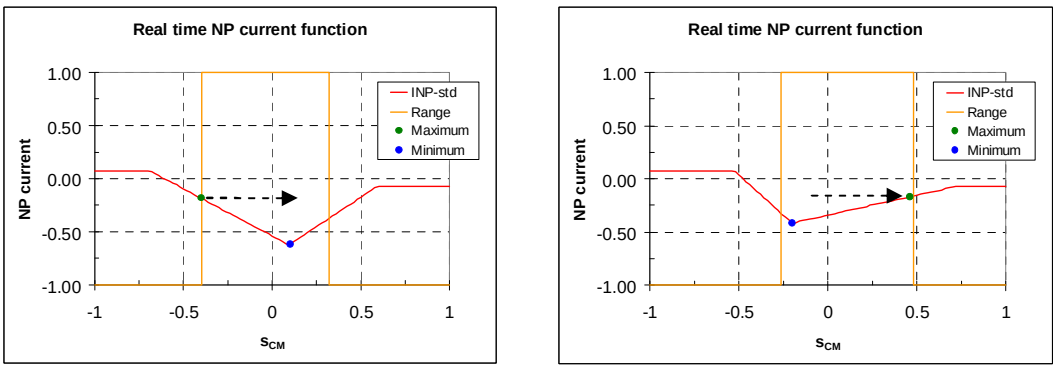


Figure 64, NP current function for m = 0.61, φ = 1.51, θ = 1.7

5.1.2 Definition of the NP control scheme

Only the linear sections of the NP current function between minimum and maximum NP current shall be considered. All CM values outside of those sections do not add to controllability but either keep the resulting NP current constant or even reduce the control performance (see Figure 64). The resulting function to be used for the feedback controller is always monotonic and consist of either one or two linear sections.

As can be seen from the example in Figure 62, the NP current function can change significantly over time. In non monotonic functions, the peak changes its direction, pointing up and down in alternation (see the two sample functions in red and purple). The maximum or minimum point of the NP current function may jump several times within one fundamental period (once per 60° segment, e.g. Figure 65, the CM for the maximum NP current [green dot] obviously changes from minimum CM to maximum CM and the gradient of the NP current function is changing its sign). Those jumps are not desirable, as the average switching frequency on the device level is increased and losses rise. An alternate approach using harmonic CM injection, which results in a more smooth CM operation, is proposed in the next section.



(a) (b)

Figure 65, Real time NP current function for a given load angle (φ = 1.51) and modulation depth (m = 0.87) for increasing angle θ during the fundamental period (a: θ = 0.4, b: θ = 0.8)

For best NP voltage control, the controller always applies the CM with the lowest possible NP current in case of zero NP voltage offset. However, it doesn't necessarily have to be that way. A strategy with a non minimum NP current ripple can be chosen instead, for example to minimize losses or output current distortion. The *zero NP-voltage-offset operating point* (see also glossary) can be chosen quite flexibly. A NP voltage feedback controller will then acts from this zero NP-voltage-offset operating point by adding or subtracting a suitable CM value as a function of NP voltage offset and controller gain.

The zero NP-voltage-offset operating point varies over time and describes a trajectory according to the black lines in the graphs of TABLE 30. The three columns describe different strategies for the definition of the zero NP-voltage-offset operating point trajectory over θ. Note that the four graphs in a given column describe the same function from a different viewpoint. This type of representation is used as a standard in all tables of that kind throughout the thesis.

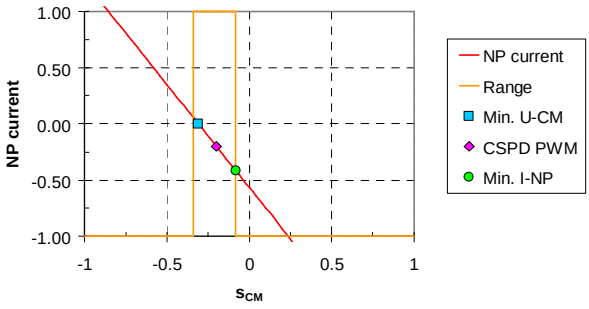
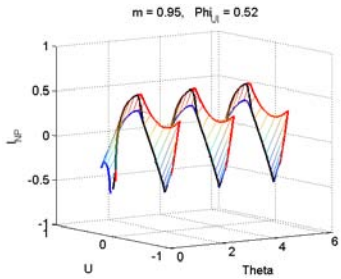
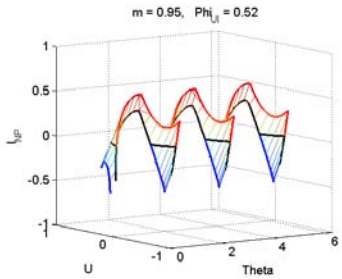
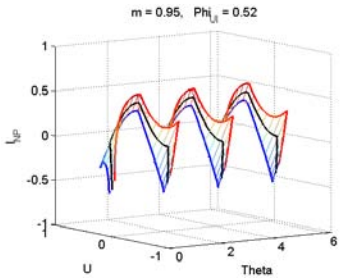
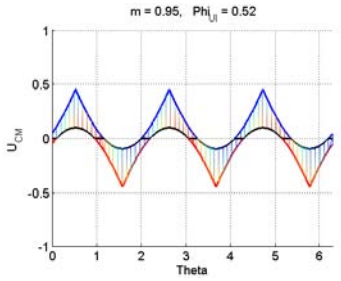
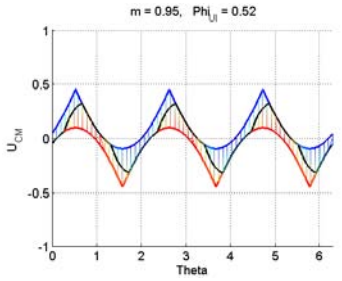
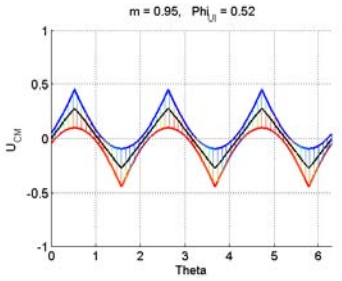
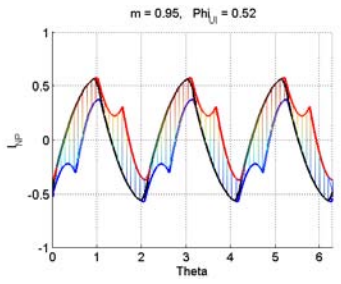
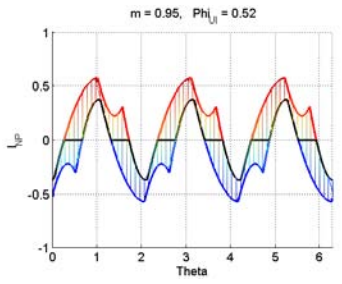
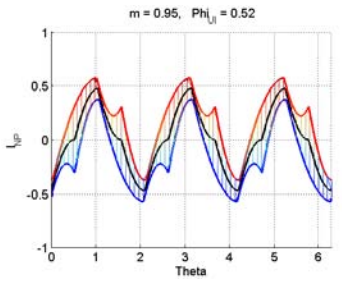
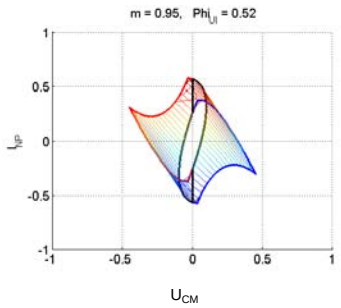
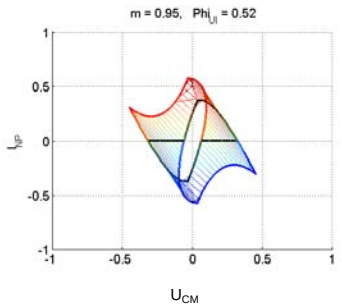
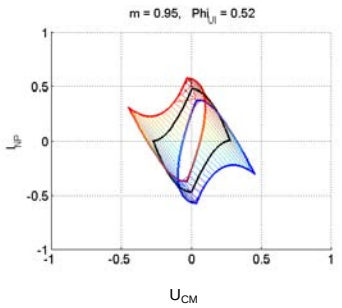


Figure 66, Different zero NP-voltage-offset operating points for m = 0.95, φ = 0.86, θ = 1.67

TABLE 29, DEFINITION OF REAL TIME NP CURRENT FUNCTION CONTROL SCHEME

1. Determine maximum and minimum NP current points of piecewise linear NP current function.
2. Constrain the CM to the range between the values generating maximum and minimum NP current.
3. Determine a suitable zero NP-voltage-offset operating point for the feedback controller a. Optimization for bearing current minimization: Lowest possible CM voltage (TABLE 30 [a]) b. Optimization for DC link design: Lowest possible NP current (TABLE 30 [b]) c. Optimization for DM waveforms (harmonic standards for AFE, motor losses in drives): Use of primary modulator of choice (e.g. CSPD PWM, TABLE 30 [c] or 3rd harmonic injection, offline optimized patterns etc.)
4. Determine the gain for the feedback controller a. Trade off between NP control dynamics and steady state performance according to the criteria under point 3 (a – c).

TABLE 30, OPTIONS FOR THE USE OF THE REAL TIME NP CURRENT FUNCTION WITH THE EXAMPLE OF m = 0.95 AND COS (φ) = 0.86, CALCULATED WAVEFORMS

(a) Lowest possible CM voltage	(b) Lowest possible NP current	(c) Optimization for output harmonics (CSPD PWM)
		
		
		
		

Note that Phi_{UI} (or $Phi_{U}I$) in these graphs is equivalent to φ, Phi_{U} is equivalent to θ, and U_{CM} is equivalent to $\overline{s}_{CM}$.

Legend (valid for all graphs of this type):

- red: maximum NP current trajectory
- blue: minimum NP current trajectory
- black: NP current trajectory based on CM injection strategy
- thin lines: NP current function over time

In order to keep the desired steady state performance (according to any of the schemes in TABLE 29 and TABLE 29), the gain of the controller should not be chosen too high. With a high gain, the controller will saturate and the CM trajectory will look the same for all configurations: it will simply follow the maximum (red) or minimum (blue) NP current trajectory and switch back and forth between the two. A hysteresis control scheme applying different gain values to get good steady state performance and powerful NP control at higher NP voltage deviations is proposed in chapter 7.

The real-time piecewise linear NP current function based controller presents a significant improvement over simple unconstrained DC CM linear feedback controllers. Using the real time NP current function for NP control yields the performance shown in TABLE 23. The full physically possible range of NP currents based on standard modulation schemes can be used. The concepts gives good performance for high and low modulation depth as well as high and low cos(φ). However, it cannot overcome the limits shown in TABLE 23, which can be critical for very low or very high modulation depth, especially in reactive power operation. The proposals with virtual vectors in the following chapter overcome those limits. Note that the concept characterized by the real time NP current function is not limited to any specific modulation scheme. The CM values for min. and max. NP current can be used as constraints both for CB PWM and SVM schemes. The scheme is topology independent (within the frame of the 3-L DC link converters) and works independently of the number of output levels.

5.1.2.1 Simulation and experimental verification

The proposed NP control concept based on a real time NP current function has been simulated and verified experimentally with the 5-L 6kVA ANPC prototype in ANPC1 configuration. The experimental measurements are presented in the next paragraph. NP current ripple minimization according to TABLE 30 (b) is used, leading to a large 3rd harmonic in the CM well visible in Figure 69 (a).

5.1.2.2 Comparison with state of the art

The calculation of a suitable CM voltage (or zero sequence voltage) has been proposed in literature by various authors. Pou [78] determines the maximum NP current points with their associated CM voltage and applies them directly depending on the sign of the deviation of the NP voltage. This gives the same result as the real-time NP current function scheme with high gain (controller in saturation). Always the maximal physically possible current is applied in that case. Some SVM schemes found in literature act in the same way (e.g. [80]). The space vector yielding the highest NP current with the correct sign is applied directly. Rodriguez [80] uses the output current reference instead of the measured current, assuming that the current controller performs as it should. The advantage is that the reference has a much lower ripple than the measured current and there are no delays from the measurement potentially degrading the performance of the NP control.

In reality, maximum NP current as obtained by the schemes above is not required. Yamanaka [81] calculates the optimal redundant states based on the output currents too, but he uses a redundancy function (duty cycle) for the application of the redundant states. This allows for the same kind of proportional feedback as with the real-time NP current function. However, the real-time NP current function offers a much higher degree of freedom in defining the PWM.

Song [76] analytically calculates the suitable zero sequence to be injected. The NP current is calculated as in (55), but rather than identifying the most interesting part of the piecewise linear function. Song uses a test-verify-revise algorithm where he starts from an initial assumption for the result of the sign functions in (55) and then revises if necessary. The actual NP control algorithms tries to generate a NP current to get to zero NP voltage deviation within one modulation period. If the controller goes into saturation, the CM voltage is only limited to the physical limitation, which will result in very poor performance of the scheme proposed in reactive power operation.

5.2 Harmonic injection NP control

The previous paragraph has described a new CM injection scheme based on the real time NP current function with all calculations done in time domain, . As an alternative, an approach in the frequency domain is proposed in this paragraph.

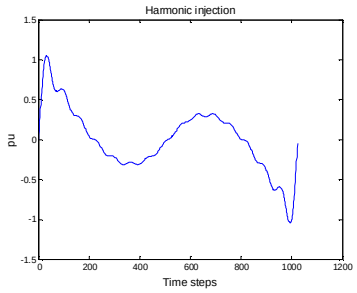
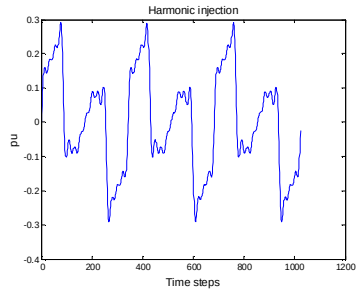
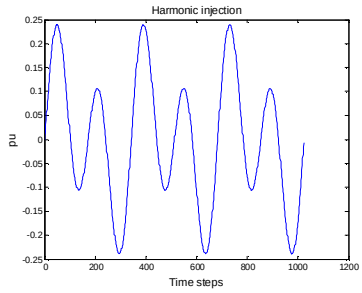
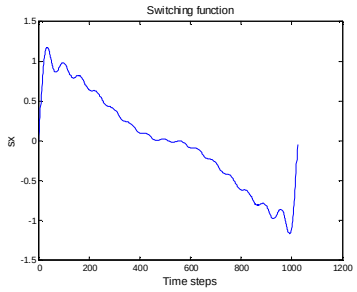
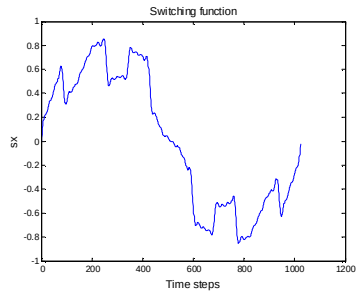
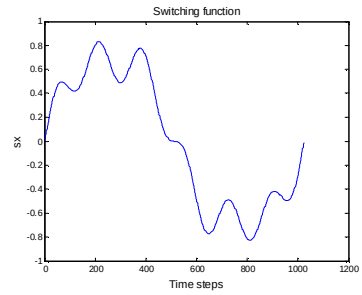
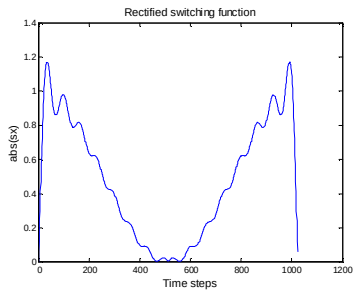
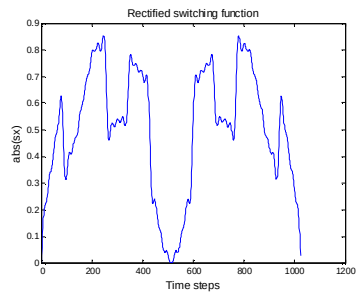
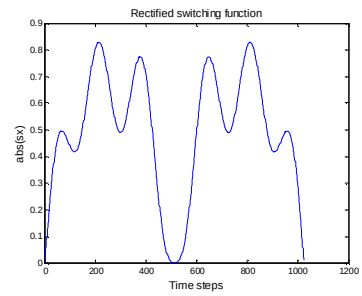
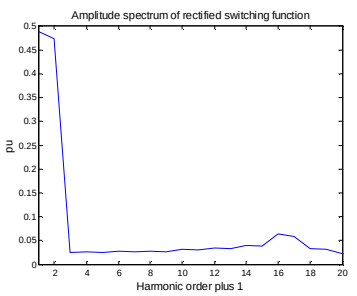
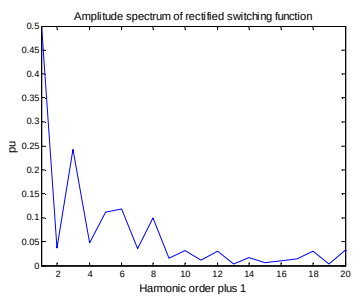
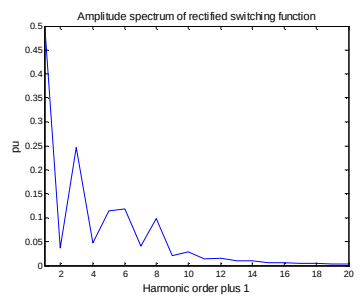
In active power operation, the gradient in the NP current function remains the same throughout the whole period, a DC CM offset creates a DC NP current and a linear feedback control can be used directly. In reactive power operation, a DC CM offset creates an AC NP current. To generate a DC NP current, higher order harmonics need to be injected instead. This is true also for the real-time NP current scheme presented in the previous paragraph, where the CM function is generated purely in the time domain. Also in that case, a set of higher order harmonics are injected as a result of the NP control. However, they do not need to be known at the time of application.

As an alternative, specific harmonics could be injected. A fundamental component needs to be generated in the rectified switching function to interact with the fundamental output current and generate a DC NP current (see TABLE 27). In active power operation, such a fundamental can easily be generated with a DC offset (see TABLE 24). For reactive power operation, a DC offset is not effective, as the fundamentals in the rectified switching function and the fundamental output current will have a phase shift of $\pi/2$. A fundamental without phase shift needs to be generated.

TABLE 31 gives three example of harmonic injection for the generation of a suitable fundamental component in the rectified function. The first example on the left used calculated harmonics from 2nd to 15th order based on a pure DC and fundamental in the rectified switching function. Obviously, the result is very powerful regarding NP control but the associated highly distorted switching function is not applicable in reality as it would generate a very large distortion in output voltage and current. In practice only zero sequence components are allowed and only with an amplitude that can physically be generated. The second column of TABLE 31 does exactly that by applying optimized multiples of 3rd harmonics up to the 42nd. The result is close to the ideal case which would be obtained by application of the real time NP current scheme with high gain. The CM jumps mentioned in paragraph 5.1.2 are actually nicely visible also with this harmonic injection approach (as relatively high frequencies are injected). The third column in TABLE 31 injects only a 3rd and a 6th harmonic. The resulting waveforms resemble the ones obtained with the harmonic injection up to the 42nd, but obviously it is much smoother and likely to generate less switching losses.

It is interesting to note that both cases result in almost the same value for the fundamental component in the rectified switching function. This indicates that the 6th harmonic is dominant over the higher order harmonics regarding the generation of a fundamental component.

TABLE 31, HARMONICS IN RECTIFIED SWITCHING FUNCTION ABS(S(T)) IN FUNCTION OF HARMONIC INJECTION IN S(T)

All 2nd to 15th harmonic injection including positive and negative sequence	Multiples of 3rd harmonic up to 42nd zero sequence only.	3rd and 6th harmonic injection
		
		
		
		

5.2.1 Constrained DC and 6th harmonic injection

It is proposed to only inject either DC or a 6th harmonic depending on the operating point of the converter, as a pure injection of a 6th harmonic is almost as effective as the optimized combination of higher harmonic terms in the case of reactive power; DC is best in the case of active power. A 6th harmonic injection has been proposed by Tallam in [77]. Note that the two methods are not related, as the 6th harmonic injection by Tallam is equivalent to driving DC CM injection into saturation (physical limitation) in predominantly active power operation (motor application).

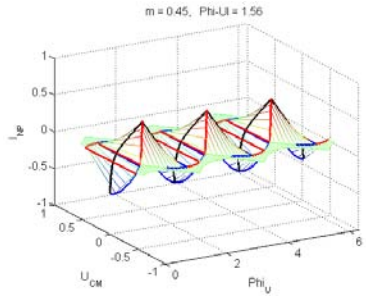
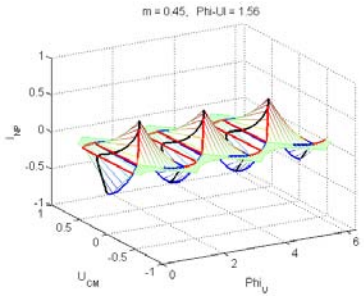
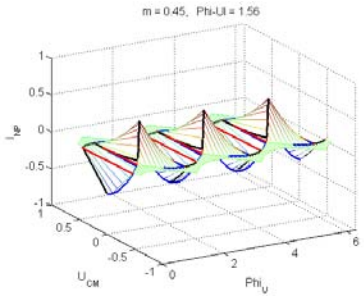
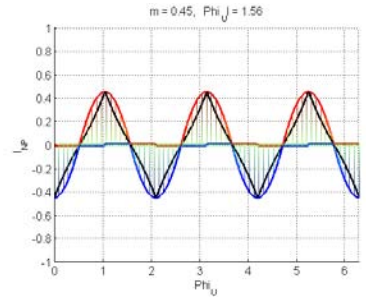
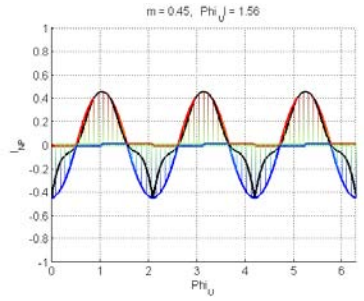
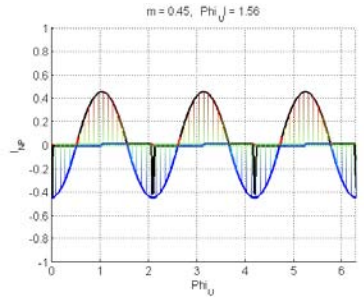
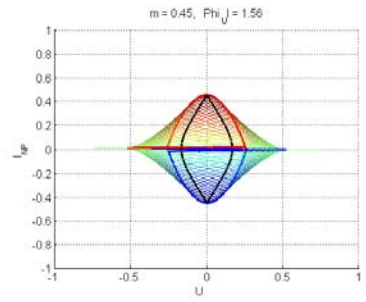
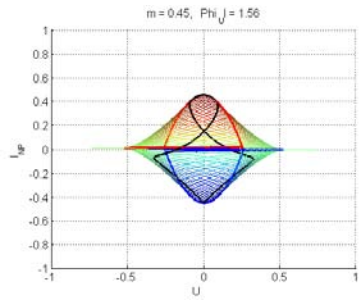
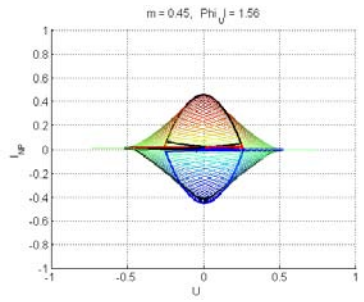
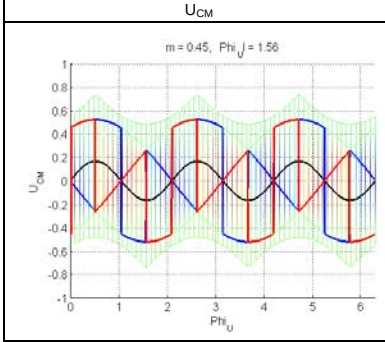
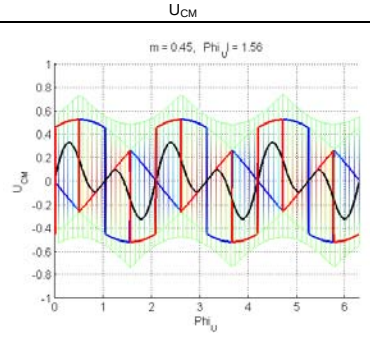
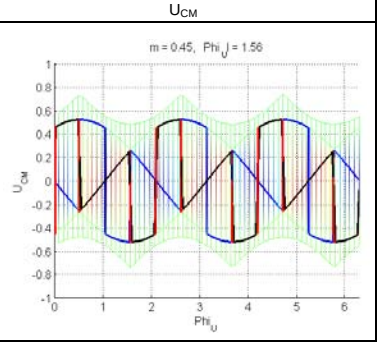
In case of 6th harmonic injection care needs to be taken with the amplitude. Without proper constraints, the DC NP current will increase with rising 6th harmonic amplitude, but then decrease again for even higher amplitudes. This is due to the non monotonic shape of the NP current function in reactive power operation. The CM voltage needs to be constrained to the range between the CM voltages generating minimum and maximum NP currents. A simple clamping to the minimum and maximum values is proposed. With rising amplitudes of the 6th harmonic, the switching function based on fundamental, 3rd and 6th harmonic will therefore be distorted, with the effect that additional harmonics are injected and the same endpoint can be reached as with the real-time NP current function. There is a linear region without saturation. Simulation shows that the NP current is linear to the injected 6th harmonic as expected. An implementation of a linear feedback controller is straight forward. Starting from the clamping region, the gain is reduced and the NP current asymptotically reaches its maximum value.

TABLE 32 shows 3-D plots of the NP current function over one period with different levels of constrained 6th harmonic CM injection. Note that the minimum and maximum NP current curves are not unique for pure reactive power operation and low modulation depth. NP currents are zero for both high and low CM voltage. If the intermediate sections of the piecewise linear NP current function are positive, the midpoint represents the maximum possible value, any of the adjacent singularities and the two outer sections of the piecewise linear function represent the minimum possible value. In case of negative values in the intermediate sections, the midpoint represents the minimum value and the adjacent singularities and the two outer sections of the piecewise linear function represent the maximum value. The transitions indicated in the $U_{CM}(Phi_U)$ functions for maximum NP current (see TABLE 32, lowest columns) could in fact take place in different positions and in different numbers. To be compatible with 6th harmonic injection, the CM functions for minimum and maximum NP current need to be defined as follows:

1. The CM function for minimum and maximum NP current have to be on the singularities of the piecewise linear function rather than within the outer sections to avoid useless application of CM jumps.
2. The ideal NP current function over time must not contain any DC component
3. The ideal NP current function over time must have the same zero crossings as a 6th harmonic with zero phase shift, leading to 9 vertical transitions in the U_{CM} function for maximum NP current as shown in TABLE 32, lowest columns.

The scheme proposed also corresponds qualitatively with the limiting function for higher modulation depth (see TABLE 33).

TABLE 32, CM VOLTAGE AND RESULTING NP CURRENT IN FUNCTION OF TIME WITH DIFFERENT LEVELS OF 6TH HARMONIC INJECTION, REACTIVE POWER OPERATION, MODERATE MODULATIN INDEX

Fundamental = 0.45*2/sqrt(3) **3rd harmonic = 0.167** **6th harmonic = 0**	**Fundamental = 0.45*2/sqrt(3)** **3rd harmonic = 0.167** **6th harmonic = 0.2**	**Fundamental = 0.45*2/sqrt(3)** **3rd harmonic = 0.167** **6th harmonic = 2**
		
		
		
		

For low modulation depth and cos(φ) not equal to zero, both outer sections of the piecewise linear function have the same absolute value but opposite signs. Maximum and minimum current functions (with lowest absolute value CM) are clearly defined. These maximum and minimum current functions have singularities with CM jumps as can be seen from TABLE 34. Nevertheless, continuous CM voltage operation is possible with suitable 3rd harmonic injection, as proposed in TABLE 34. The third harmonic required has significantly different amplitude and phase angle than the one use in TABLE 32. Of course, other strategies of CM injection staying within the minimum and maximum boundaries are possible, but a strategy leading to continuous CM injection function is preferable for commutation reasons; any jump in the CM function will generate multiple commutations simultaneously and lead to higher overall switching losses.

Note that minimum and maximum NP current CM values do not cross each other in this case (as opposed to the approach in TABLE 32). Consequently, no AC CM needs to be injected to generate a DC NP current, but a pure DC CM voltage injection can be used both for minimum and maximum DC NP current. This is shown in the third column TABLE 34. Note that there is a smooth transition possible from active to reactive power with this control scheme. The 3rd harmonic amplitude and phase can be defined as a continuous function of amplitude of the fundamental and the angle φ between voltage and current.

The 6th harmonic injection scheme can still be applied at low modulation depth and non zero cos(φ) if the CM function for minimum and maximum NP current are adapted accordingly, conforming with the constraints above. In fact the examples in TABLE 32 use a phase angle of 1.56, which leads to small but noticeable difference of NP currents in the two outer sections of the NP current functions. The performance impact is very low. Both schemes have very similar performance. The 6th harmonic injection scheme will have slightly reduced maximum and minimum NP currents but it has a higher degree of freedom regarding 3rd harmonic injection and it requires no DC CM injection for the NP control.

We can conclude that there are two almost equivalent concepts for NP current control for reactive power operation at low modulation depth. This is not true for high modulation depth, because the outer sections of the piecewise linear CM current function cannot physically be reached. Consequently, the minimum and maximum NP current functions are clearly defined. Only 6th harmonic injection is possible as shown in TABLE 33.

TABLE 33,CM VOLTAGE AND RESULTING NP CURRENT IN FUNCTION OF TIME WITH DIFFERENT LEVELS OF 6TH HARMONIC INJECTION, REACTIVE POWER OPERATION, HIGH MODULATIN INDEX

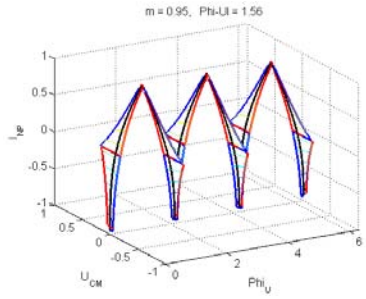
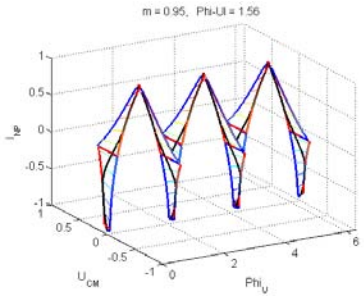
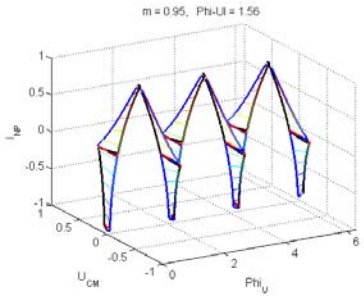
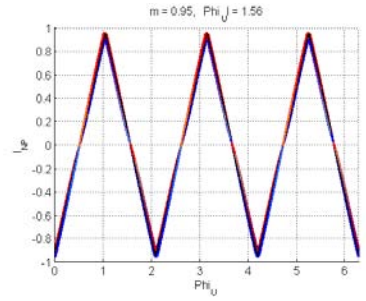
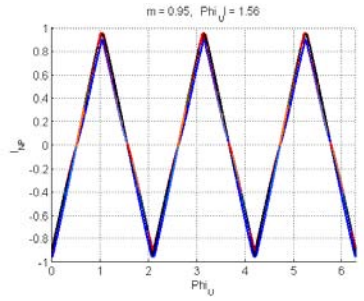
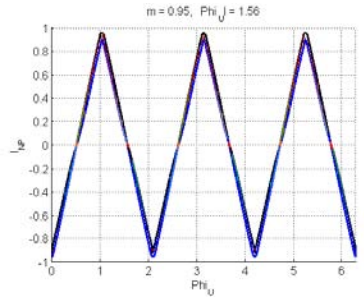
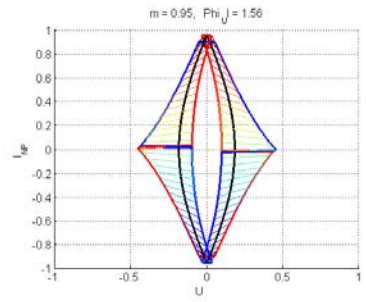
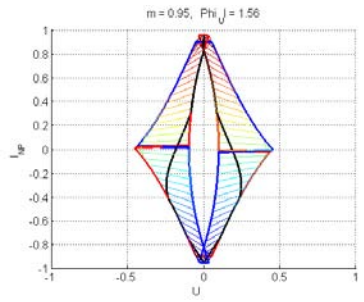
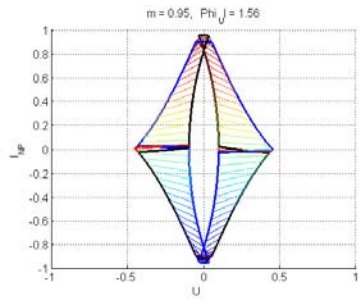
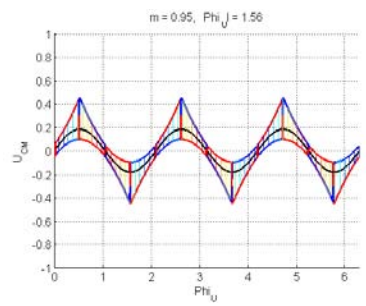
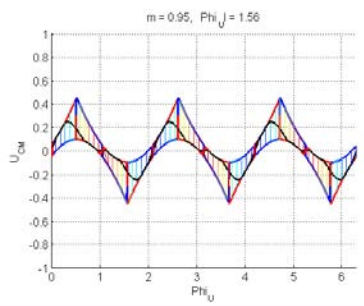
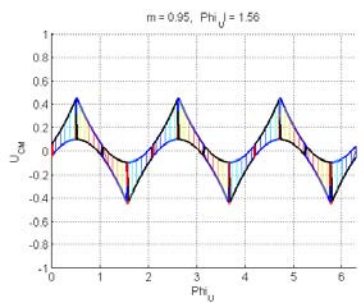
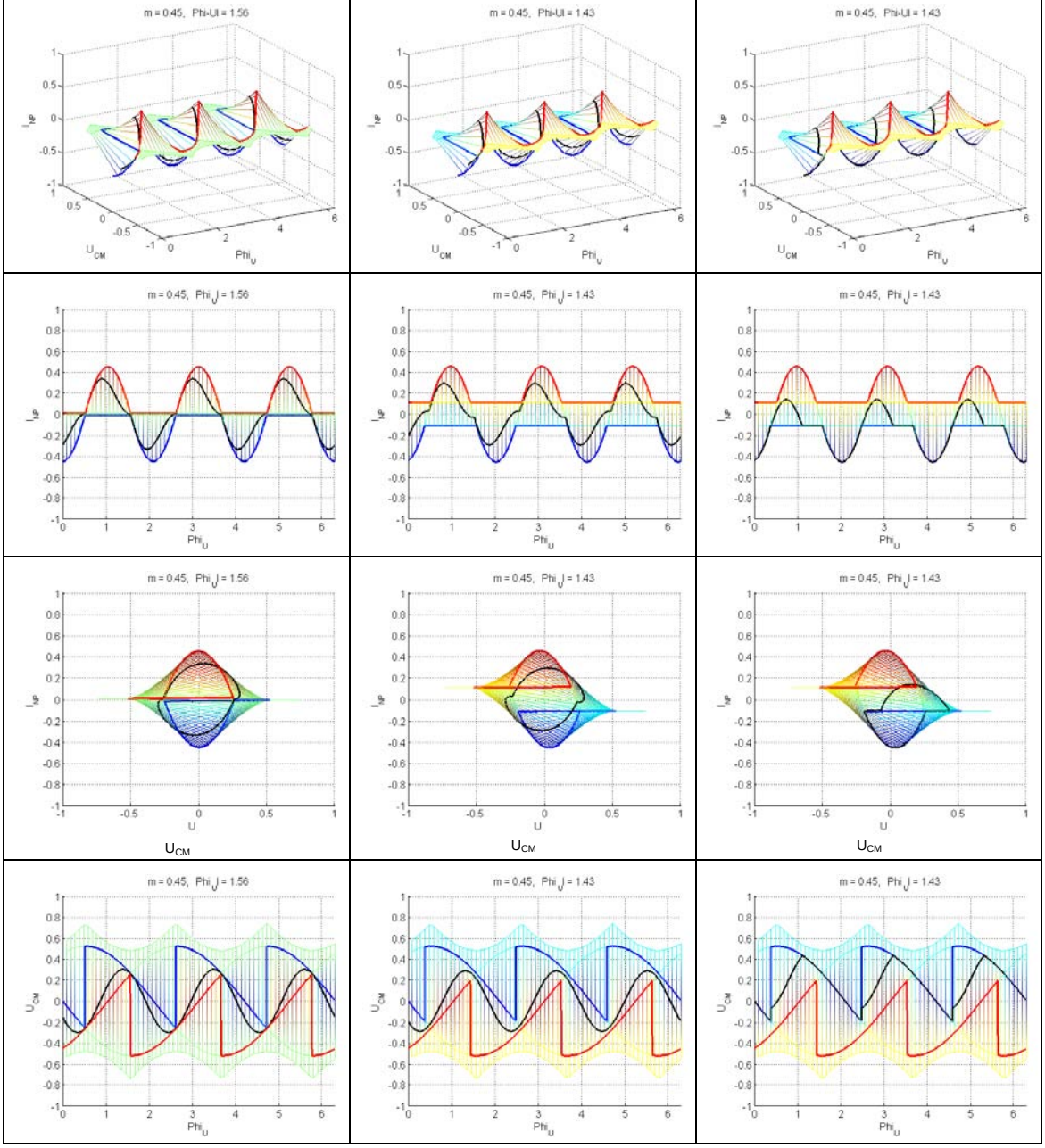
Fundamental = 0.95*2/sqrt(3) **3rd harmonic = 0.183** **6th harmonic = 0**	**Fundamental = 0.95*2/sqrt(3)** **3rd harmonic = 0.183** **6th harmonic = 0.1**	**Fundamental = 0.95*2/sqrt(3)** **3rd harmonic = 0.183** **6th harmonic = 2**
		
		
		
		

TABLE 34, TRUE MAXIMUM AND MINIMUM NP CURRENT FUNCTION FOR DIFFERENT LOAD ANGLES AT MODERATE MODULATION INDEX

φ= 1.56 **Fundamental = 0.45*2/sqrt(3)** **3rd harmonic amplitude = 0.299** **3rd harmonic angle = -2.6** **DC CM offset = 0**	**φ= 1.43** **Fundamental = 0.45*2/sqrt(3)** **3rd harmonic amplitude = 0.287** **3rd harmonic angle = -2.383** **DC CM offset = 0**	**φ= 1.43** **Fundamental = 0.45*2/sqrt(3)** **3rd harmonic amplitude = 0.287** **3rd harmonic angle = -2.383** **DC CM offset = 0.2**
		

It has been shown that both DC and 6th harmonic injection can be effective for NP current control depending on operating point. Both schemes have been evaluated for the full range of

modulation depth and load angle cos(φ) to determine the transition points to switch over from one scheme to another, which is illustrated in Figure 67. DC CM injection (with limitation to maximum NP current CM values as indicated in TABLE 33) is very effective over a very large range of operation, including reactive power at low modulation depth. However, it has very poor performance for pure reactive power at high modulation depth, which is pointed out by the zoom in Figure 67. In this region, clearly 6th harmonic injection performs better.

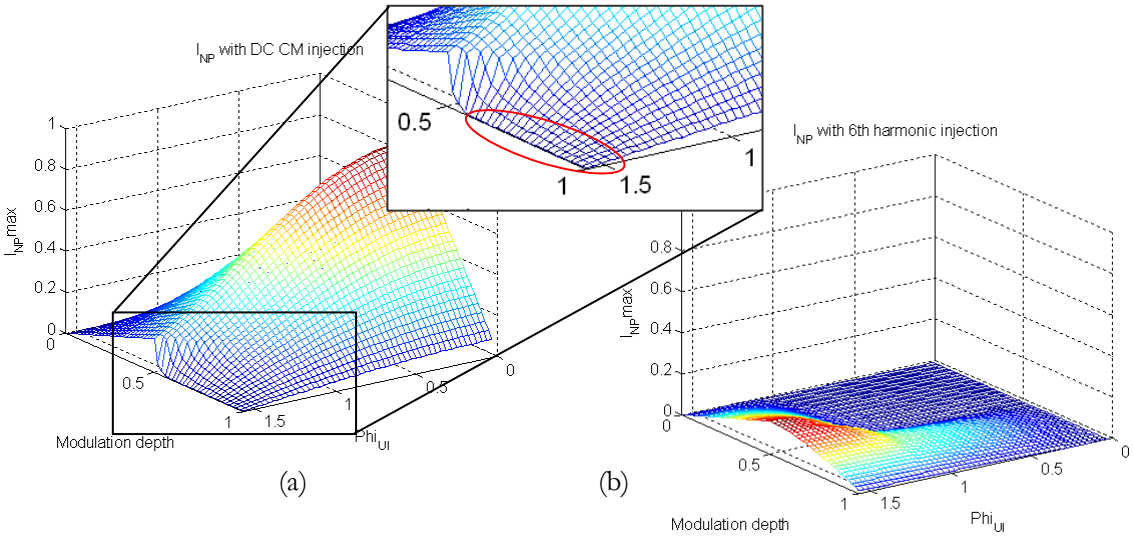


Figure 67, Maximum obtainable NP currents, a) DC CM injection, b) 6th harmonic injection

To determine the transition point, the two graphs have been combined into one (Figure 68 b). The area improved by the 6th harmonic injection is rather small. However, this is the area where STATCOM's are operating: high modulation index and very low cos(φ). The performance improvement is very significant in this case. This even holds true for pure reactive power and highest physically possible modulation index.

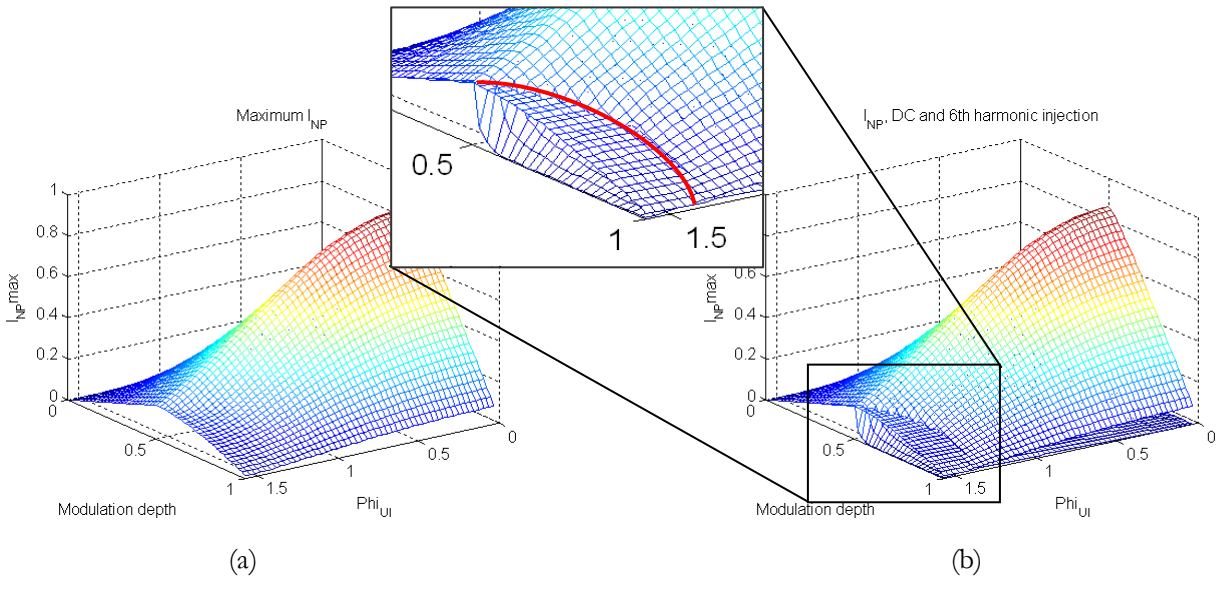


Figure 68, maximum obtainable NP currents, a) optimal CM injection based on true real time NP current function, b) constrained DC and 6th harmonic injection

Analytical calculation results in ~1% DC NP current for the case of cos(φ)=0 and m=1. This still is sufficient if there is no large bias current in the NP. For comparison, a graph with optimized, constrained CM injection based on the real time NP current function is shown in Figure 68 (a). This approach provides the highest possible NP current based on standard modulation schemes. The difference to the combined DC and 6th harmonic injection approach is very small, indicating that this latter approach can be used without any significant loss in performance. The major difference is in handling the discontinuity of the NP current function. When using the real time NP current function alone, the minimum NP current value is jumping form one side to the other at some point and the gradient of the function is changing abruptly (Figure 65). This leads to a CM jump that either generates additional losses or needs to be limited with a given rate of change. The 6th harmonic injection on the other hand also leads to a zero crossing in that point, however automatically limits the rate of change by its sinusoidal waveform. With increasing gain, almost the same peak NP current can be obtained. The NP control schemes "real time NP current function" and "6th harmonic injection" are therefore equivalent.

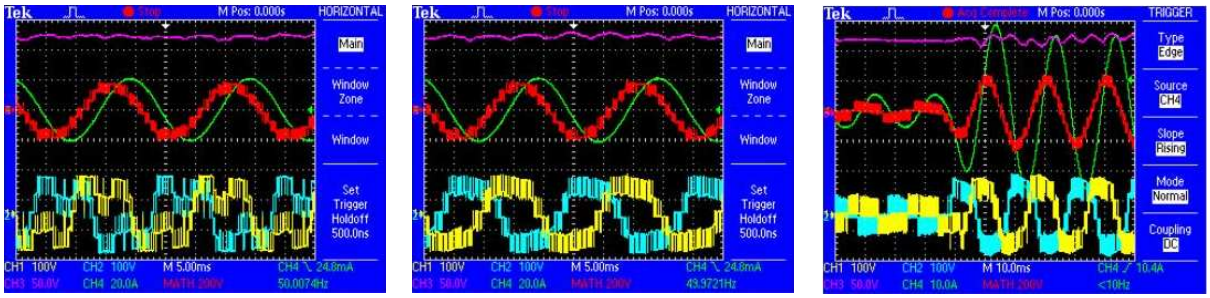
5.2.2 6th harmonic injection based NP control implementation

The 6th harmonic injection scheme has been integrated in a PD PWM as introduced in chapter 4. The actual 6th harmonic controller is only active in the area indicated with a red border line in Figure 68 in the zoomed area. Outside of that area, a DC CM injection is used.

A pure proportional feedback is considered sufficient for this application.

TABLE 35, OPERATING POINT FOR EXPERIMENTAL VERIFICATION OF REAL TIME NP CURRENT SCHEME AND 6TH HARMONIC INJECTION SCHEME

m	f_{out}	U_{DC}	U_{FC}	R_{load}	L_{load}	φ_{UI}	C_{DC}	C_{FC}	f_{sw}
0.75	50 Hz	240 V	60 V	0.5 Ω	14.2 mH	1.53	990µF	1120µF	2000 Hz



(a) (b) (c)

CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2}

Figure 69, Steady state operation with reactive load and two different NP control schemes applied: Real time NP current function m = 0.75 (a), 6th harmonic injection with m = 0.75 (b), 6th harmonic injection with step form 0.2 to 0.9

5.2.3 Performance evaluation

For the performance analysis of the controllers, a NP voltage reference step has been simulated. The Maximum dv/dt achieved is proportional to the maximum average NP current and is a measure for NP control capacity and thus the performance of the control scheme.

TABLE 36, OPERATING POINT FOR THE SIMULATIONS IN TABLE 37 TO TABLE 38

m	f_{out}	U_{DC}	U_{FC}	R_{load}	L_{load}	φ_{UI}	C_{DC}	C_{FC}	f_{sw}
0.6	50 Hz	240 V	60 V	0.5 Ω	14.2 mH	1.53	990µF	1120µF	2000 Hz

All simulations in this paragraph are based on balanced undistorted systems. The controller gain in the simulations has been chosen such that the controllers saturate at high voltage deviation in the NP, but have a low impact close to the set point.

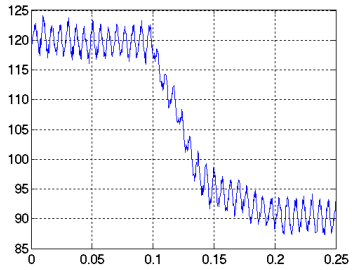
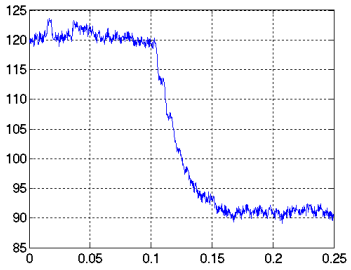
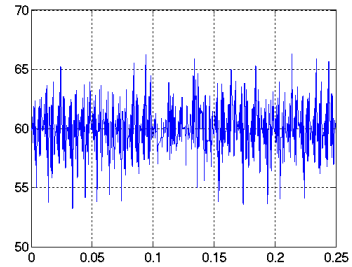
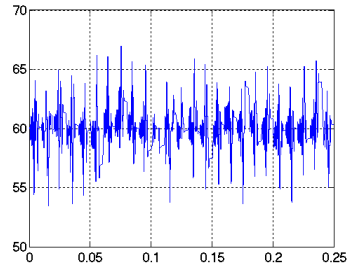
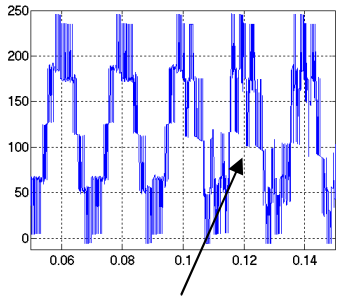
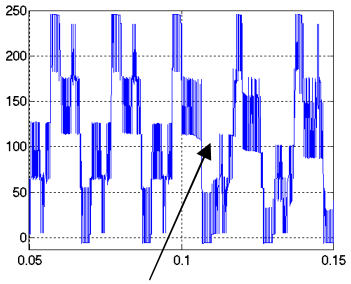
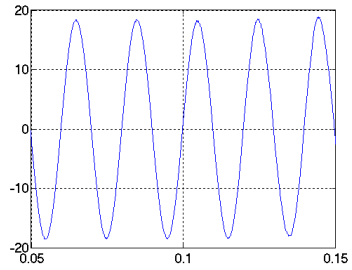
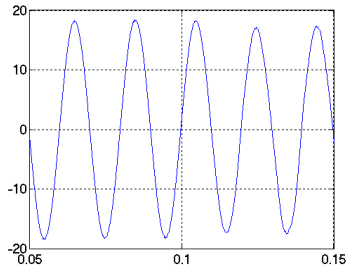
The dv/dt obtained with the real time NP current function is 800V/s (20V / 25ms in the graph). With an effective capacitance of 4mF (upper and lower DC link capacitors in parallel), we get a NP current of 3.2A during the transient corresponding with 18% of the peak phase current of 18A. The 6th harmonic injection has a dv/dt of 600 V/s resulting in an NP current of 2.4A, which corresponds with 13% of the peak phase current. This is a very good match with the values obtained by calculation and shown in Figure 68.

The two schemes provide very similar currents during transients and the new set point is reached after around 50ms. The phase output voltages in TABLE 37 show fundamentally different behavior for the two schemes: The 6th harmonic injection scheme has moderate 3rd harmonic in steady state; during transient operation, the 6th harmonic is clearly visible. The real time NP current function scheme applies a very high 3rd harmonic content in steady states, which minimizes the NP current ripple; in transient operation, a constrained DC is injected rather than a 6th harmonic. The 6th harmonic injection scheme results in a higher NP voltage ripple but yields smoother phase voltage waveforms. Note that this results depends largely on the choice of underlying modulation scheme and the controller gain.

The proposed modulation schemes keep the differential voltage and the resulting output currents undistorted. There is a difference in the switching frequency on the device level (at a given apparent output switching frequency) and the resulting losses. However the impact is relatively low in the given operating point. The steady state switching losses can be reduced by only 2% through the use of the 6th harmonic injection scheme.

Experimental results comparing the NP control performance of these schemes with the more powerful virtual vectors are given in paragraph 7.4.

TABLE 37, NP VOLTAGE REFERENCE STEP RESPONSE, M = 0.6, φ = 1.53, SIMULATION

	6th harmonic injection	Real time NP current function
NP voltage (V)		
Flying capacitor voltage (V)		
Phase output voltage (V)	 6th harmonic injection	 DC CM injection
Phase current (I)		
f_{switch}	2149 Hz (output) 2249 Hz (device)	2137 Hz (output) 2323 Hz (device)

Note the different time scales

The real time NP current functions have been recorded over time in those simulations.

TABLE 38, NP CURRENT FUNCTION OVER TIME IN STEADY STATE, M = 0.6, φ = 1.53, SIMULATION

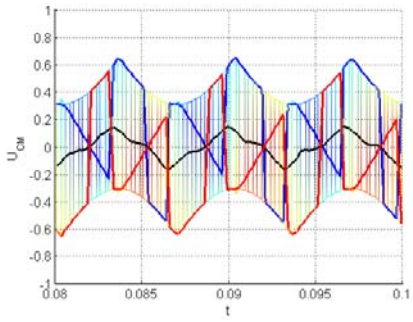
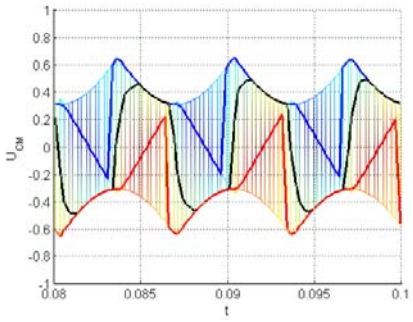
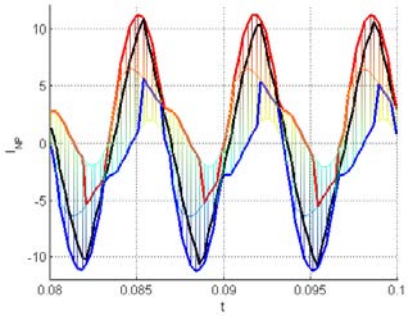
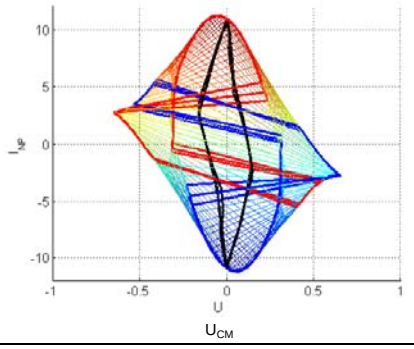
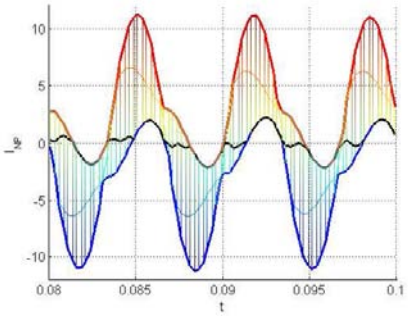
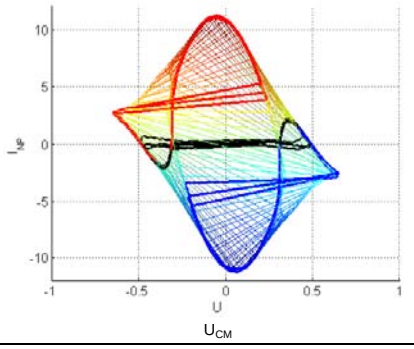
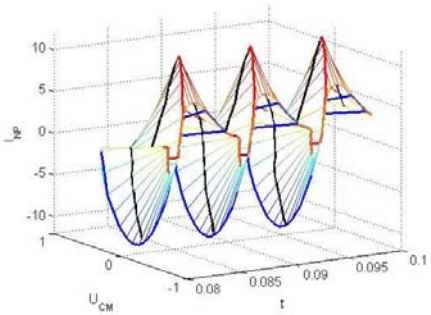
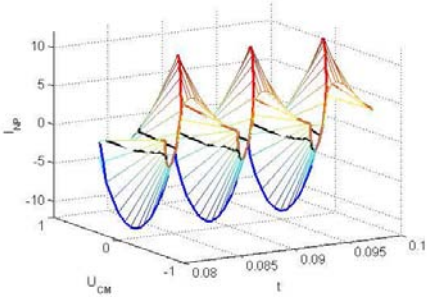
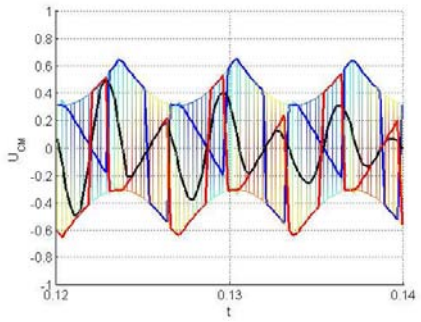
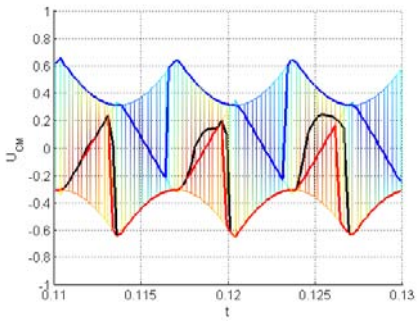
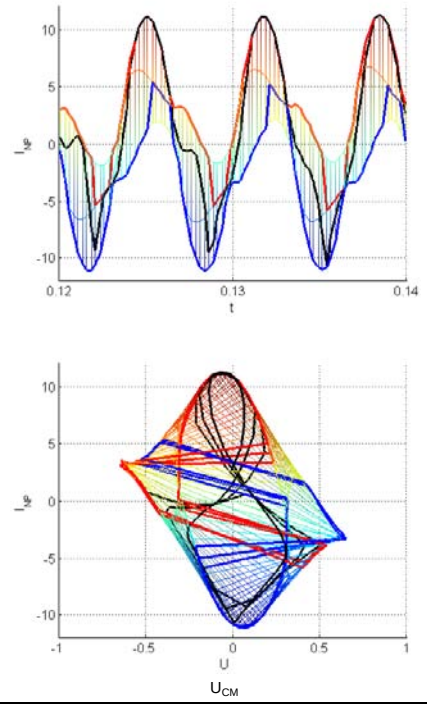
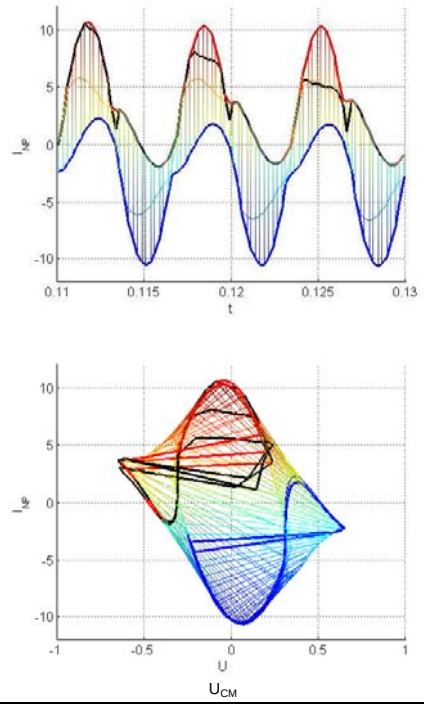
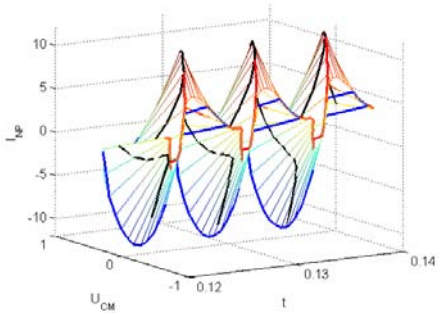
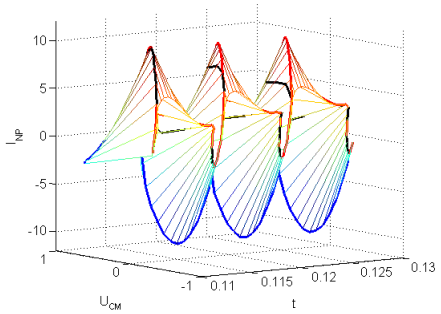
	6th harmonic injection	Real time NP current function (symmetrical)
CM voltage		
NP current	 	 
3D NP function		
losses	98 %	100%

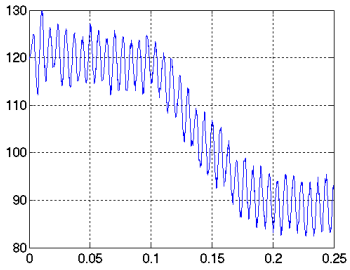
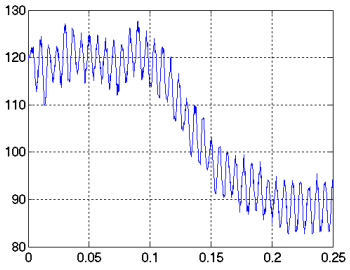
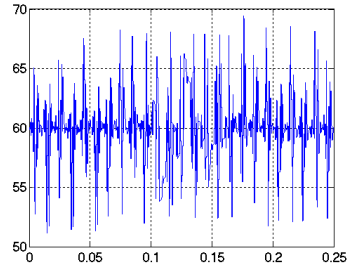
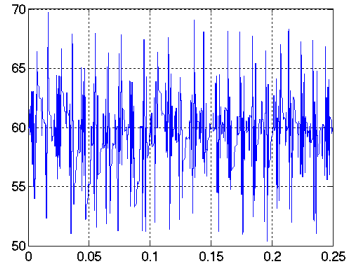
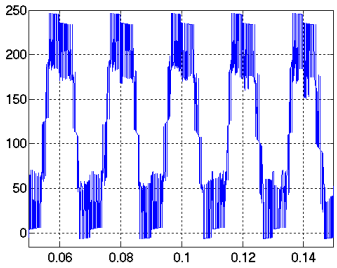
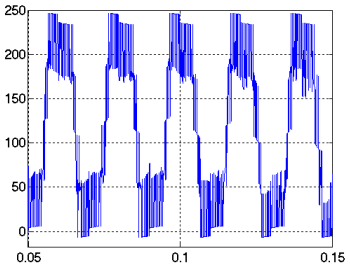
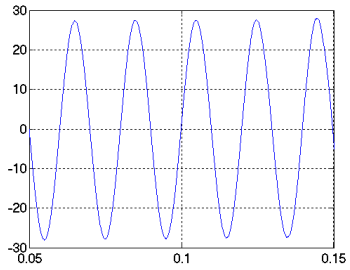
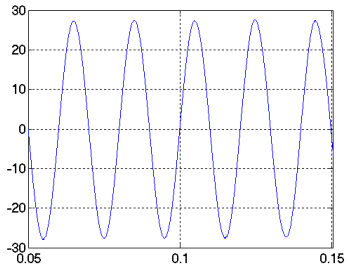
TABLE 39, NP CURRENT FUNCTION OVER TIME, TRANSIENT REGION, M = 0.6, φ = 1.53, SIMULATION

	6th harmonic injection	Real time NP current function
CM voltage		
NP current		
3D NP function		
losses	**105 %**	**93 %**

A second set of simulations for higher modulation index (m = 0.9) is documented subsequently. The maximum NP current is reduced, as can be anticipated from Figure 68. This operating point has also been verified experimentally (TABLE 74).

5.2.3.1 NP voltage reference step with m = 0.9

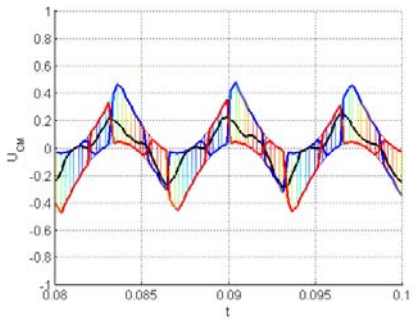
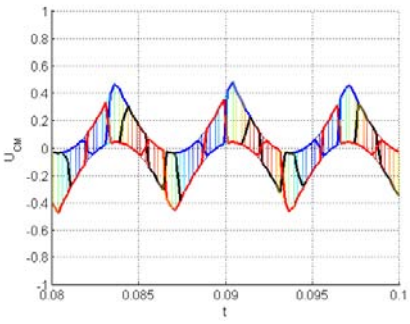
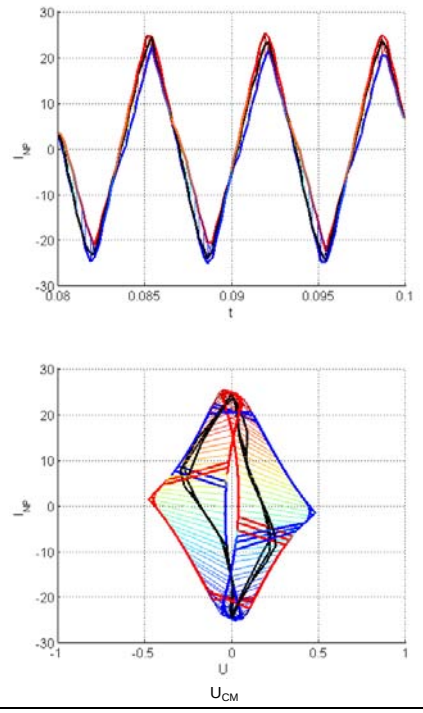
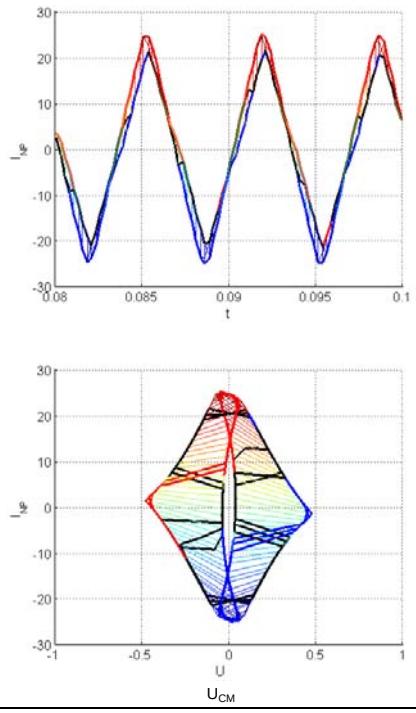
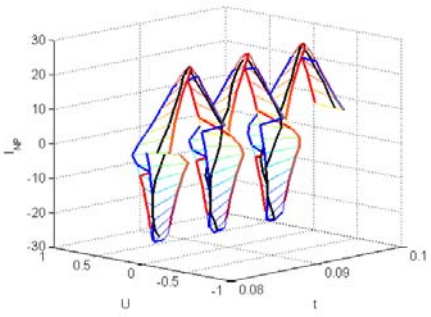
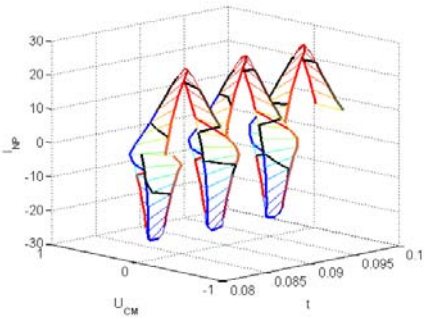
TABLE 40, NP VOLTAGE REFERENCE STEP RESPONSE WITH M = 0.9, φ = 1.53, SIMULATION

	6th harmonic injection	Real time NP current function
NP voltage (V)		
Flying capacitor voltage (V)		
Phase output voltage (V)		
Phase current (I)		
f_{switch}	**2136 Hz (output) 2205 Hz (device)**	**2231 Hz (output) 2301 Hz (device)**

Note the different time scales

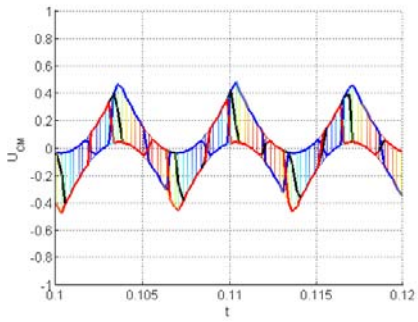
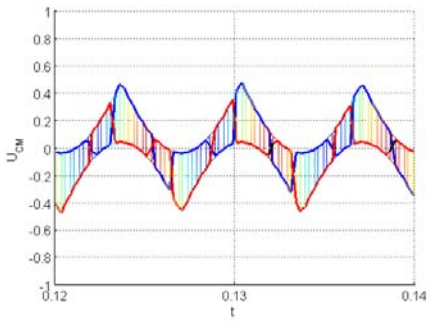
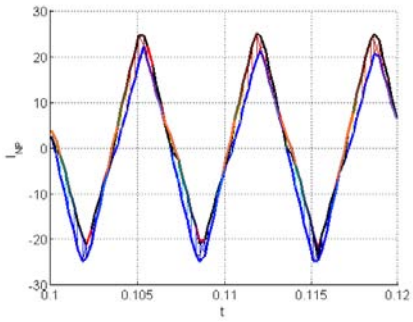
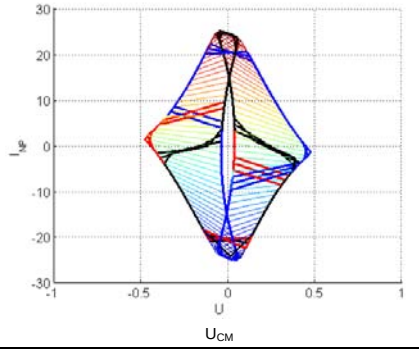
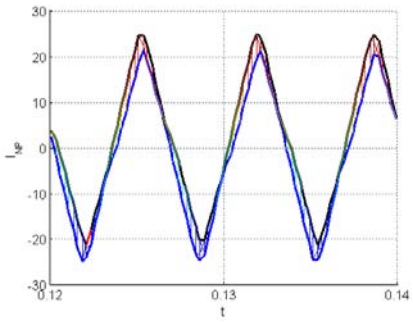
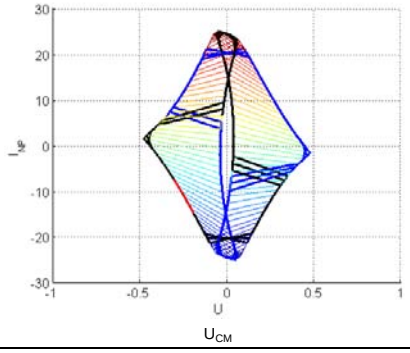
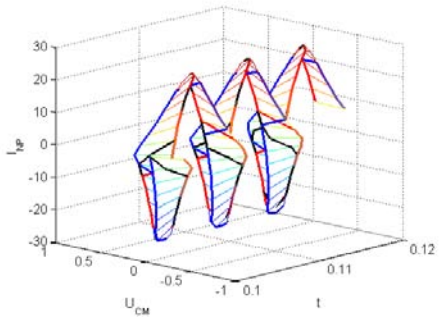
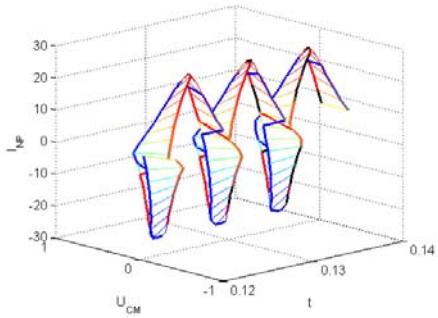
The difference between the two schemes at m = 0.9 is much smaller than at lower modulation depth. The reason for this can be explained with TABLE 42: Both schemes inject predominantly a 6th harmonic, based on the NP current function over time. Note the impact on NP current and voltage ripple is almost negligible (see TABLE 40).

TABLE 41, NP CURRENT FUNCTION OVER TIME IN STEADY STATE, M = 0.9, φ = 1.53, SIMULATION

	6th harmonic injection	Real time NP current function (symmetrical)
CM voltage		
NP current		
3D NP function		
losses	**94 %**	**100 %**

There is a significant difference in steady state operation: The 6th harmonic injection scheme gives smooth operation whereas the real time NP current scheme generates CM jumps. Consequently, the switching losses can be reduced by 6% with 6th harmonic injection.

TABLE 42, NP CURRENT FUNCTION OVER TIME, TRANSIENT REGION, M = 0.9, φ = 1.53, SIMULATION

	6th harmonic injection	Real time NP current function
CM voltage		
NP current	 	 
3D NP function		
losses	**94 %**	**97 %**

The small difference still visible originates from the active power part. At cos(φ) = 0, the two schemes are exactly identical in performance (when the controller is in saturation).

5.3 SMC and ANPC modulation using extra redundant states

Novel modulation schemes making use of redundant states are proposed for SMC and ANPC (topology specific). These are operating several converter stages simultaneously (opposed to the schemes in TABLE 82). The modulation schemes in this paragraph are constrained to optimum modulation. The purpose of these new schemes is:

- Extending the zero NP current areas to allow NP voltage "ripple free" operation in a wider area.
- Increasing the NP control capacity (range of possible NP current amplitudes) to improve controllability of the NP voltage.

5.3.1 ANPC type 3 modulation

A simple modulation concept for the ANPC type 3 has been introduced in 4.6.3.2 making use of the different MC converter stages by alternating between the modulation of a stage at the DC link and the modulation of the output stage. This simple concept does not make full use of the available state in the ANPC type 3. There is much higher redundancy than in the ANPC type 1 and 2 and this can be used effectively for an improved NP control. Figure 70 shows the physical relevance of the additional states and TABLE 43 gives the key properties.

TABLE 43, 5-L ANPC TYPE 3 STATES AND CORRESPONDING VOLTAGES AND CURRENTS

Nr.	Type	Cell 1	Cell 2	Cell 3	Cell 4	U_{out}	I_{NP}	I_{FC1}	I_{FC2}	I_{FC3}
0	all	0	0	0	0	$-U_{DC}/2$	0	0	0	0
1	1	0	0	0	1	$-U_{DC}/4$	0	0	0	-
2	1	0	0	1	0	$-U_{DC}/4$	1	0	0	+
3	all	0	0	1	1	0	1	0	0	0
4	2	0	1	0	0	$-U_{DC}/4$	0	0	-	0
5	3	0	1	0	1	0	0	0	-	-
6	3	0	1	1	0	0	1	-	0	+
7	2	0	1	1	1	$+U_{DC}/4$	1	-	0	0
8	2	1	0	0	0	$-U_{DC}/4$	1	0	+	0
9	3	1	0	0	1	0	1	0	+	-
10	3	1	0	1	0	0	0	+	0	+
11	2	1	0	1	1	$+U_{DC}/4$	0	+	0	0
12	all	1	1	0	0	0	1	0	0	0
13	1	1	1	0	1	$+U_{DC}/4$	1	0	0	-
14	1	1	1	1	0	$+U_{DC}/4$	0	0	0	+
15	all	1	1	1	1	$+U_{DC}/2$	0	0	0	0

Essentially, there are 4 new types of states indicated with type 3 in TABLE 43. All others correspond with the states of the type 1, type 2 converters or are available in all ML ANPC converters. Two of these extra states generate a zero output (neutral point output) without generating a NP current. These states alone cannot balance the FC voltages, so that they need to be combined with the other remaining new states as indicated in Figure 70.

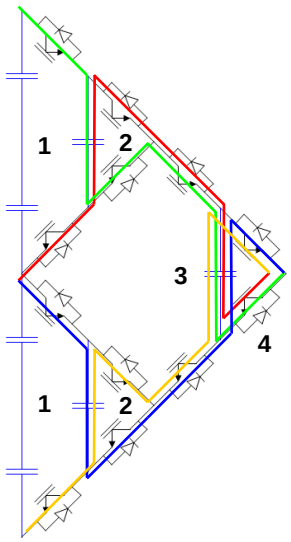


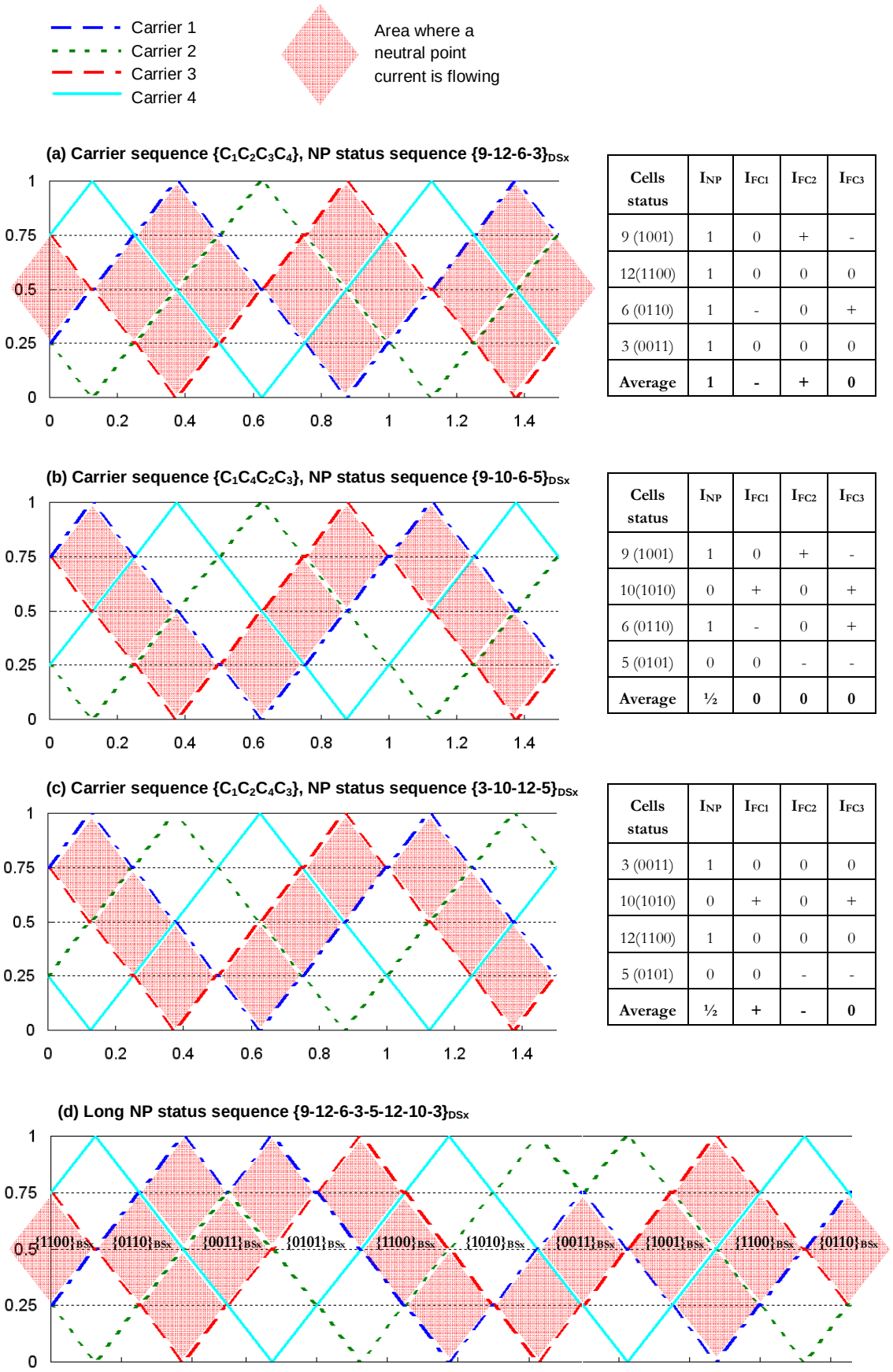
Figure 70, ANPC type 3 with type 3 zero voltage output states, coloring corresponds with TABLE 43

The resulting NP current for NP voltage output is ½ as can be seen from the table in Figure 71 (b). This corresponds with the NP current generated for $-U_{DC}/4$ and $+U_{DC}/4$. It can be expected that a proper modulation schemes making a linear combination of the required states will yield a constant NP current of ½ for V_{out} from $-U_{DC}/4$ to $+U_{DC}/4$. Outside of that range, there are no type 3 states available and the standard NP current function applies (see Figure 72 b).

5.3.1.1 Design of a suitable modulation scheme

The following modulation schemes apply single commutations between adjacent states only and make use of the available redundant states. The carrier based PWM applies phase shifted carriers for the 4 cells. There are 6 different sequences possible; always two of them are equivalent as the sequence is simply reversed. The 3 fundamentally different sequences are shown in Figure 71.

A current is flowing in the NP if the first cell of either stage 1 or stage 2 and the first cell of stage 3 are in different states. This corresponds with regions enclosed by carrier 1 and carrier 3 in Figure 71. Obviously, this region is larger in the case of a large phase shift and smaller for the case of a small phase shift, which is reflected in the average NP currents. Not all possible carrier sequences lead to a balanced operation. Sequence $\{C_1C_4C_2C_3\}$ applies type 3 zero outputs and results in all balanced flying capacitors. Sequence $\{C_1C_2C_3C_4\}$ and sequence $\{C_1C_2C_4C_3\}$ use type 3 and standard zero outputs and generate unbalance in the flying capacitors. All capacitors will be balanced if the two types of sequences are combined, resulting in a long sequence $\{C_1C_2C_3C_4C_1C_2C_4C_3\}$.



Cells status	I_{NP}	I_{FC1}	I_{FC2}	I_{FC3}
9 (1001)	1	0	+	-
12(1100)	1	0	0	0
6 (0110)	1	-	0	+
3 (0011)	1	0	0	0
Average	**1**	**-**	**+**	**0**

Cells status	I_{NP}	I_{FC1}	I_{FC2}	I_{FC3}
9 (1001)	1	0	+	-
10(1010)	0	+	0	+
6 (0110)	1	-	0	+
5 (0101)	0	0	-	-
Average	**½**	**0**	**0**	**0**

Cells status	I_{NP}	I_{FC1}	I_{FC2}	I_{FC3}
3 (0011)	1	0	0	0
10(1010)	0	+	0	+
12(1100)	1	0	0	0
5 (0101)	0	0	-	-
Average	**½**	**+**	**-**	**0**

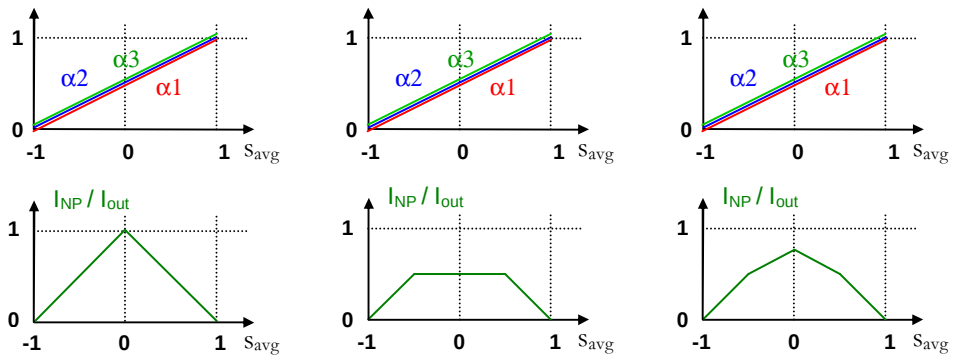
Figure 71, Carrier based PWM commutation schemes for the ANPC type 3

TABLE 44, CELL STATUS SEQUENCE FOR STATE MACHINE BASED MODULATOR

Cells status	I_{NP}	I_{FC1}	I_{FC2}	I_{FC3}
9 (1001)	1	0	+	-
12 (1100)	1	0	0	0
6 (0110)	1	-	0	+
3 (0011)	1	0	0	0
5 (0101)	0	0	-	-
12 (1100)	1	0	0	0
10 (1010)	0	+	0	+
3 (0011)	1	0	0	0
Average	¾	**0**	**0**	**0**

Note that the choice of sequence has an impact on the capacitor dimensioning. The sequence $\{9\text{-}10\text{-}6\text{-}5\}_{DSx}$ applying type 3 NP states only applies two charging or discharging states for the flying capacitor number 3 in a row. The mixed long sequence $\{9\text{-}12\text{-}6\text{-}3\text{-}5\text{-}12\text{-}10\text{-}3\}_{DSx}$ alternates current signs in all flying capacitors, which allows for half the capacitor size for a given switching frequency.

Carrier based modulation is possible also for the mixed sequences. However, the carriers for a specific cell are not purely triangular anymore. It is better to use generic carriers and then apply a state machine to determine the suitable cell states. A smooth transition from one modulation type to another is possible in this case. This approach with the generic carrier also allows using carriers in phase disposition (DP PWM with optimal harmonic performance).



(a) standard NP states only $\{3,12\}_{DSx}$ (b) type 3 NP states only $\{5,6,9,10\}_{DSx}$ (c) mixed NP states $\{3,5,6,9,10,12\}_{DSx}$

Figure 72, NP current functions of the 5-L ANPC 3 with different modulation schemes

5.3.1.1.1 Commutation in ANPC type 3

ANPC type 1 and type 2 generate 2 level steps at the output when the stage without flying capacitors is operated. The ANPC type 3 on the other hand, all three stages can generate the minimum voltage step required for optimum modulation, which means all three stages can be operated simultaneously.

5.3.2 SMC modulation

The following applies to the description of the subsequent modulation schemes:

- Dedicated carriers are used for each switching cell. This does not yield lowest harmonics in 3 phase systems but is nice to illustrate the concept. Implementation can later be done with generic carriers to achieve PD PWM.
- An index α_L (0 to 1) is used for the output voltages from $-U_{DC}/2$ to $U_{DC}/2$, α_1 is the duty cycle of the upper cell, and α_2 is the duty cycle of the lower cell.
- Ref is the reference (phase leg) duty cycle $\alpha_L = 0.625$ applied as an exemplary operating point.
- The commutation cells are numbered according to Figure 73

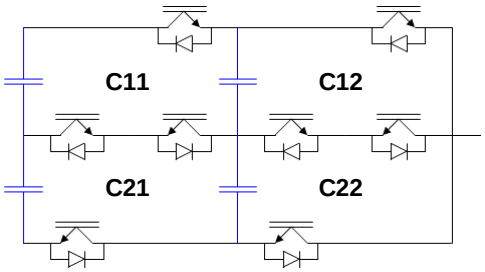


Figure 73, 5-L SMC and cell numbering

5.3.2.1 Standard SMC modulation

With the basic modulation scheme shown in Figure 74, only the upper FC converter of the SMC is modulated for output voltages above zero (α_L>0.5). It can be seen that the switching cells C21 and C22 are not used for the output voltage chosen in the given example. The resulting average phase NP current is 75% of the phase output current. The flying capacitor is operated with an AC current with its fundamental at twice the carrier frequency.

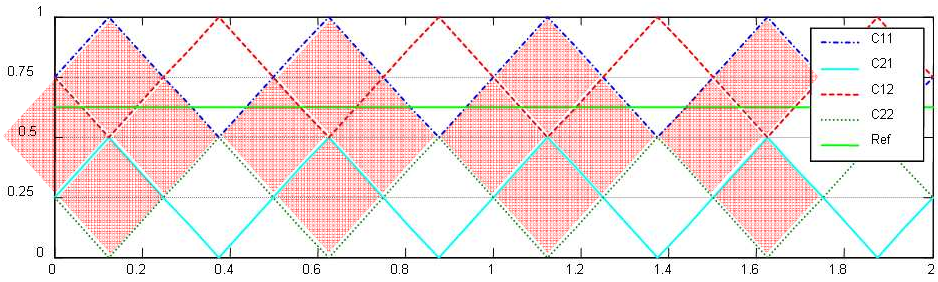


Figure 74, SMC standard modulation (α = 0.625)

5.3.2.2 Extended SMC modulation

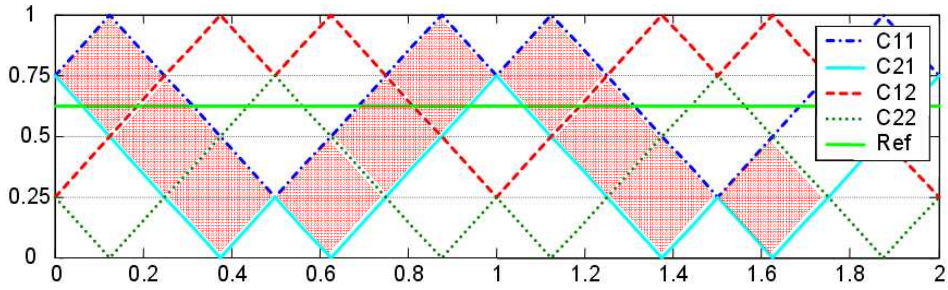


Figure 75, SMC A modulation (α = 0.625)

The modulation introduced in Figure 75 (SMC A modulation) applies both upper and lower FC converter stages for 0.25 <= α <= 0.75. It is optimized for low NP current while maintaining the same total number of switching events and keeping the symmetry in the output voltage. To obtain equidistant pulses of the same length at the output (optimum modulation), the following constraints apply:

$$\alpha_2 - \alpha_1 = 2x / N \qquad \text{with} \qquad (76)$$

$$\frac{1}{N} < \alpha_L < 1 - \frac{1}{N} \qquad (77)$$

(76) can only be satisfied in the range defined in (77). Outside of this region, standard modulation needs to be applied. To get lowest NP current, x needs to be as small as possible. In the case of the 5-L converter, N equals 4 and it follows directly:

$$\alpha_2 - \alpha_1 = 0.5 \qquad (N = 4) \qquad (78)$$

$$0.25 < \alpha_L < 0.75 \qquad (N = 4) \qquad (79)$$

The momentary switching frequency per cell is half; the resulting output modulation frequency remains the same. The same output voltage waveform is achieved as with the basic modulation scheme but the average neutral point current is reduced to 50% (Figure 77 b). Both flying capacitors are operated with an AC current with its fundamental component at one fourth of the carrier frequency (as opposed to one half in the standard case). This has a significant impact on the dimensioning of the flying capacitor and / or the applicable range of operation of the modulation scheme (trade off).

The proposed SMC modulation scheme B (Figure 76) applies the least possible NP current by consequently applying the states with the lowest NP current regardless of the required switching sequence. This is at the cost of increased switching frequency, but this may not be a problem if this type of modulation is only applied during transients or exception handling. There is the trade off between switching frequency, capacitor dimensioning and applicability of the modulation scheme.

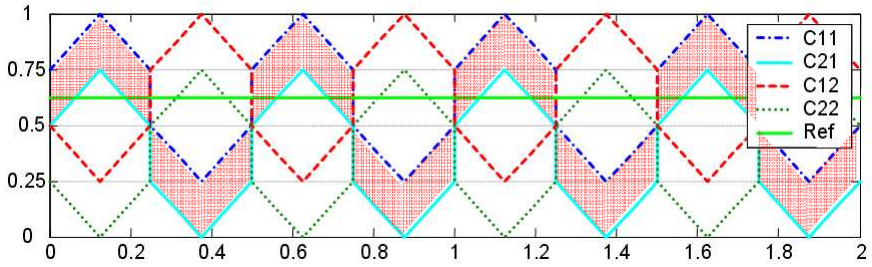


Figure 76, SMC B modulation ($\alpha = 0.625$)

The SMC can also be operated purely as a MC converter. Balancing of the flying capacitors is improved, there is no NP current, but the number of available levels is reduced to N/2+1 (from N+1).

5.3.2.3 NP current for single phase leg in function of the phase leg duty cycle

Figure 77 shows the NP current in function of the output voltage for the introduced modulation schemes. It can be seen that the NP current can effectively be reduced in the middle range of output voltages. Note that s_{avg} is used instead of α_L. See equation (40) for the relationship.

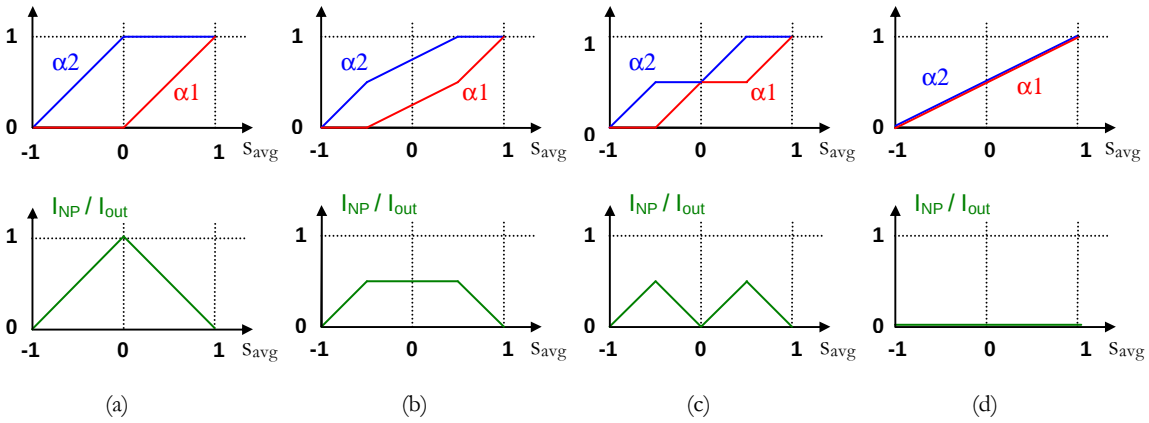


Figure 77, Single phase leg NP current functions for the different modulation schemes of the SMC: (a) standard modulation, (b) SMC A modulation, (c) SMC B modulation, (d) FC modulation

Figure 78 shows an example of the NP current in function of the CM voltage for the different modulation schemes and combinations thereof. The vertical lines indicate the limits of the physically possible operation (only inner section possible). The lower four functions combine different modulation schemes in the different phases to obtain the minimum and maximum possible values in function of the CM voltage; the total NP current can reach values not possible otherwise. While the NP current cannot reach zero for standard modulation (INP-std) or SMC A modulation (INP-SMCA), the combination thereof (I-std+A-max) crosses the zero line and does allow zero NP current operation with the appropriate CM voltage. The application of the new schemes increases the range of possible NP currents significantly and more powerful NP control is possible. Table 85 in the appendix shows absolute minimum and maximum functions for a wide range of operating points (any CM applied).Zero average NP current areas are increased as shown in Table 86 in the appendix.

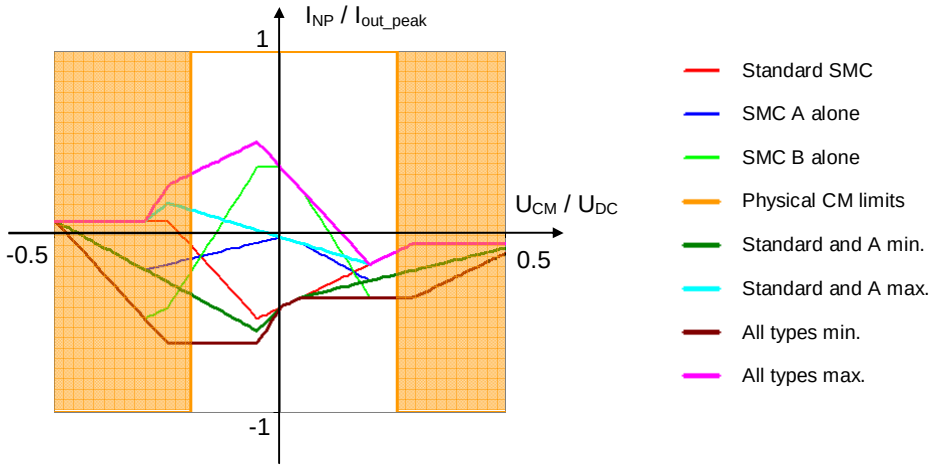


Figure 78, NP current with extended modulation scheme (α = 0.64, φ = 1.51, θ = 0.68) in function of CM voltage

It can be seen that the functions for the minimum and maximum NP currents are not trivial. They are piecewise linear functions, but now with up to 3 midpoints per phase, which all generate singularities in the resulting function. As there are three phases and each phase can make use of a different modulation scheme, there are a total of 27 individual NP current functions per operating point. All these 27 functions have up to 9 singularities. This is a level of complexity that can easily be calculated online if required for a given control scheme (see also 5.1.2 on NP control with real time NP current function).

5.3.3 NP control

The previous paragraph has shown the impact of the different modulation schemes on the NP current. Dynamic application of these schemes can be used to control the NP voltage. The following scheme applies to the SMC, a very similar scheme would be possible for the ANPC type 3 making use of the differing NP current function as shown in Figure 72. The proposed scheme does not make use of CM injection at all. It only makes use of the different modulation types to control the NP.

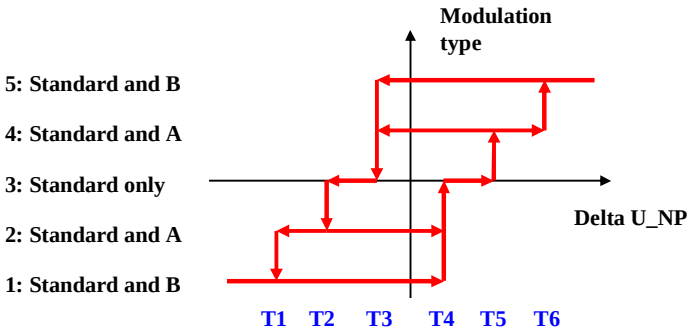


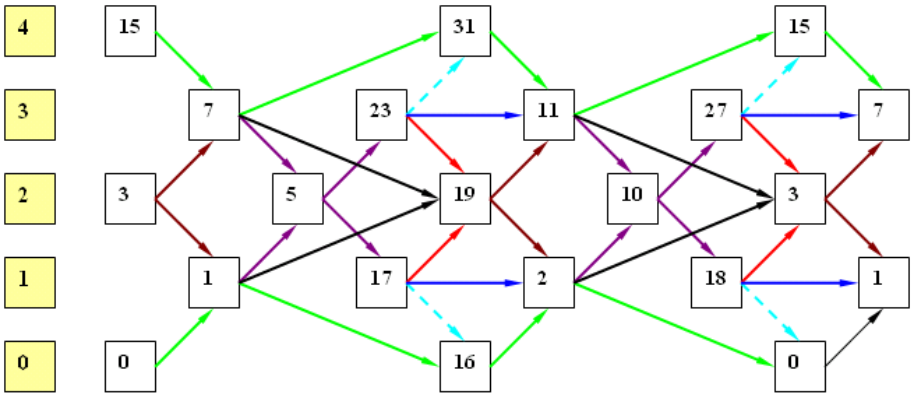
Figure 79, Hysteresis NP-voltage controller for SMC (thresholds: T1 to T6)

A hysteresis controller for the SMC with six thresholds is proposed. It is acting on a state machine with 5 states (Figure 79). The modulation type is then determined dynamically according

to Table 45. The modulation type in each phase (a,b,c) is chosen according to the state and the sign of the current in the corresponding phase output.

TABLE 45, DECISION TABLE FOR MODULATION TYPES

State	I_a: pos	I_a: neg	I_b: pos	I_b: neg	I_c: pos	I_c: neg
5	**Std**	**B**	**Std**	**B**	**Std**	**B**
4	**Std**	**A**	**Std**	**A**	**Std**	**A**
3	**Std**	**Std**	**Std**	**Std**	**Std**	**Std**
2	**A**	**Std**	**A**	**Std**	**A**	**Std**
1	**B**	**Std**	**B**	**Std**	**B**	**Std**



The yellow boxes on the left hand side indicate the output level of all states on that line (assuming correct state of NP voltage and FC voltages)

The white boxes indicate the states of the converter. The number of the state are numbered such that each bit corresponds with the state of an individual cell [c11 c12 c21 c22]. If a converter state is used twice in the state machine, the state gets an additional leading bit (e.g. states 7 and 23).

Green connectors indicate transitions for all modulation types

Black connectors indicate transitions for standard modulation type

Red connectors indicate transitions for modulation type A

Blue connectors indicate transitions for modulation type B

Brown connectors indicate transitions for modulation type standard and A

Purple connectors indicate transitions for modulation type A and B

Dotted cyan connectors indicate transitions used for transitions to other modulation level only

Figure 80, state machine for SMC modulation (standard, type A and type B)

Figure 80 shows the complete state machine for three SMC modulation types. The states are numbered such that each bit corresponds with the state of an individual cell {c11 c12 c21 c22}. Any generic PWM modulator can be used for the determination of the output levels of the individual phases.

5.3.4 Experimental verification

For the experimental verification, 5-level SMC (operated at 100V, 15A) has been used. The prototype features current sensors in the neutral point to observe and / or control the NP currents and voltages. One phase leg is shown in Figure 81.

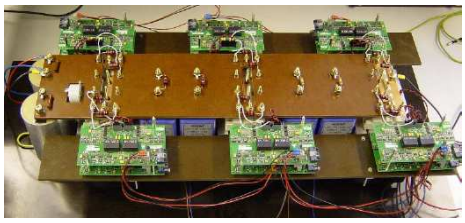


Figure 81, SMC phase leg (7-level, operated as 5-L)

5.3.4.1 Verification of NP currents

The NP current measurement is based on an H-bridge configuration to verify the NP currents in any given operating point (random voltage and current). One half bridge is operating as a voltage source in open loop. The other half bridge is controlling the current in the load (R-L load) in closed loop with a PID controller.

Experimental results for the NP current are shown in Figure 82. The operating point is chosen at α_L=0.625. The NP current either corresponds with the output current or remains at zero.

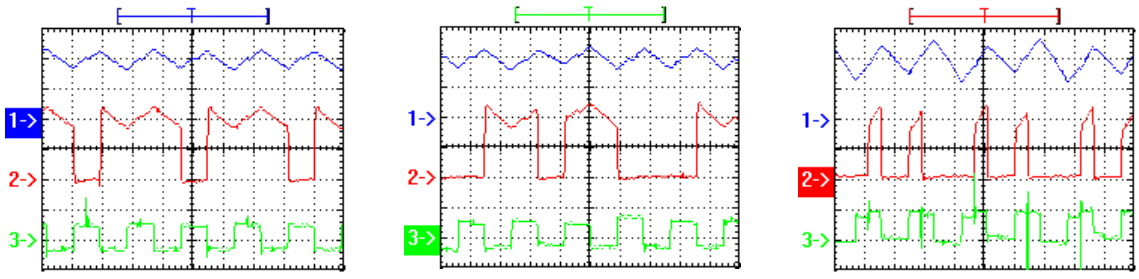


Figure 82, Measured data: standard type (left), type A (middle) and type B (right), Ch1 (blue): phase current, Ch2 (red): NP current, Ch3 (green): output voltage

The NP currents in the whole operating range of the converter has been verified by measuring the NP current in selected operating points (Figure 83).

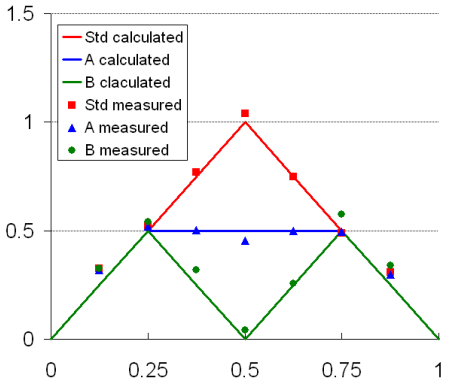


Figure 83, Calculated and measured NP currents in selected operating points (p.u. values)

There is a good match between experiment and theoretical characteristics.

5.3.4.2 Verification of NP control scheme

NP voltage control has been implemented with a hysteresis controller as presented in the previous chapter. A R-L load has been connected to the 3 phase SMC converter. The NP is not connected to any external source but is only controlled by the converter itself in this case.

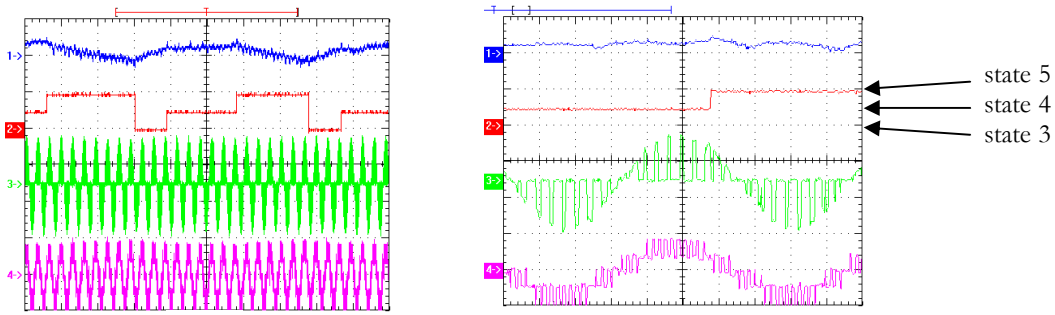


Figure 84, Measured data: NP control (left: 40ms/div, right: zoom with 2ms/div), m = 0.8, Ch1 (blue): NP voltage, Ch2 (red): state, Ch3 (green): NP current, Ch4 (purple): phase voltage

Figure 84 shows the NP control in operation. An unbalance current in the DC link leads to a voltage rise during the time with standard modulation. Note that the difference in NP current is only visible in the indicated areas, as the modulation types only differ in the middle output voltage regions. Figure shows a similar case with reduced modulation index. The difference in NP current is clearly visible for the three half waves (three different modulation types) in the plot.

The DC link unbalance is generated with a static CM offset in this case (ca. 10% V_{DC}), which is visible in the phase output voltage. The control method with modulation type can be combined with CM voltage variation without problems. This can either be used to improve NP control by using CM and modulation type variation together, or it can be used to introduce a CM voltage independently of the NP control (either for harmonic optimization or for CM voltage reduction on the motor for a reduction of the bearing currents).

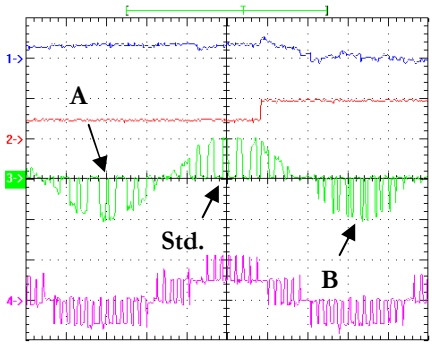


Figure 85, Measured data: NP control (2ms/div), m = 0.25 (Ch1 (blue): NP voltage, Ch2 (red): state, Ch3 (green): NP current, Ch4 (purple): phase voltage)

5.4 Executive summary for chapter 5

A NP control scheme with constrained CM voltage based on the real-time NP current as a function of the CM voltage has been introduced. The control schemes is a significant improvement over unconstrained DC injection schemes, as it also works for reactive power and keeps CM excursions limited in the low modulation depth region. For the proportional feedback controller, the NP current function can be used in different ways. Specifically, different optimization criteria can be used for the definition of the CM voltage for zero NP voltage offset. A trade off between NP voltage ripple, switching losses and output voltage distortion is possible in a straightforward way.

A second scheme using DC and 6th harmonic CM injection has been presented. The 6th harmonic injection is effective for reactive power operation, which corresponds with the region where unconstrained DC CM injection does not work anymore. A combination of constrained DC and 6th harmonic CM injection yields practically the same NP control capacity as the direct application of the real time NP current function in a proportional feedback controller. This can easily be explained by the fact that both schemes use essentially the same limits for saturation of the CM signal in the controller.

Both schemes presented are suitable for any topology in the 3-L DC link family including the NPC. They have both been experimentally verified on the 5-L ANPC prototype.

The second part of the chapter presents topology specific modulation schemes making use of extra redundant states. Both ANPC 3 and SMC feature redundant states using flying capacitors from different partial MC converters (hidden underlying MC converters, upper and lower). These redundant states allow for changing the NP current characteristics on the phase leg level. Suitable CB PWM schemes have been developed to make use of those redundant states. The modulation schemes proposed for the ANPC 3 allow for a reduction of the NP current to 50% for zero output voltage (referenced to the NP). The modulation schemes for the SMC go even further and can reduce the NP current to zero for zero output voltage (see TABLE 82 in appendix 9.3).

A combination of different modulation schemes for the 3 phases is possible, as the output voltage per phase is not influenced; the different modulation schemes only make a different choice of redundant states. Such a combination enables powerful NP voltage control schemes totally independently from CM voltage. A hysteresis controller for the SMC has been developed and it has been demonstrated both in simulation and experiment that the NP current control capacity is significantly increased over standard NP control schemes as for example presented in the first part of the chapter (see also TABLE 85 in appendix 9.5.1).

6 NP CONTROL WITH OPTIMAL SEQUENCE SVM

The ANPC 1 converter features redundant states that can be used not just for FC control but also for NP control. A suitable combination of states allows for an extension of the NP current control capacity as determined in chapter 4. For that purpose, the concept of modified and virtual vectors is introduced. These vectors can then be applied in optimized SVM sequences. At low modulation depth, this can be done without DM distortion; at high modulation depth, the high NP control capacity is traded for an increased DM distortion.

A second approach presented in this chapter proposes a calculation of optimized sequences online. A number of suitable sequences are determined based on commutation constraints. The best sequence is then chosen based on an objective function. Both modulation and control schemes in this chapter are presented for the ANPC1. They can also be applied to any other 3-L DC link topology with shared flying capacitors (by the two partial MC converters) with the appropriate modifications in the modulation scheme.

6.1 Offline calculated optimal sequences by the use of modified and virtual vectors

Paragraph 5.1.2 has described an approach for 5-L ANPC type 1 NP control improvement by use of a real time NP current function. However, the control can only perform according to the physical limits (within a modulation cycle) and the given boundary conditions. Modified and virtual vectors can extend those limits and improve NP voltage control, reaching similar performance as could be obtained with the additional redundant state for the ANPC type 3 and the SMC (chapter 5.3) The concept of virtual vectors has been proposed in literature (e.g. [86]). It combines specific converter states with fixed application times to compose a non-discrete (virtual) vector, like for the generation of a space vector based on NTV SVM. However, this new vector can be used as a vertex of a triangle with different shape and size for a new NTV SVM. The advantage over standard NTV SVM is that the specific virtual vector states can be chosen such that the NP current is reduced significantly.

Note that the concept introduced in this chapter proposes similar combinations of converter states as [86], but does not directly apply those modified and virtual vectors in a NTV SVM. It rather identifies optimized sequences making use of those virtual vector combinations. The concept is therefore not a direct extension of [86] to the 5-L ANPC as the name might imply.

6.1.1 Modified and virtual space vectors

In standard modulation, the control optimizes NP and FC voltage in each modulation cycle. Therefore, the tendency will be to alter redundant states in subsequent modulation cycles to immediately compensate the capacitor currents. One cycle may be charging a capacitor and the next one discharging, so that on average, the voltage stays balanced.

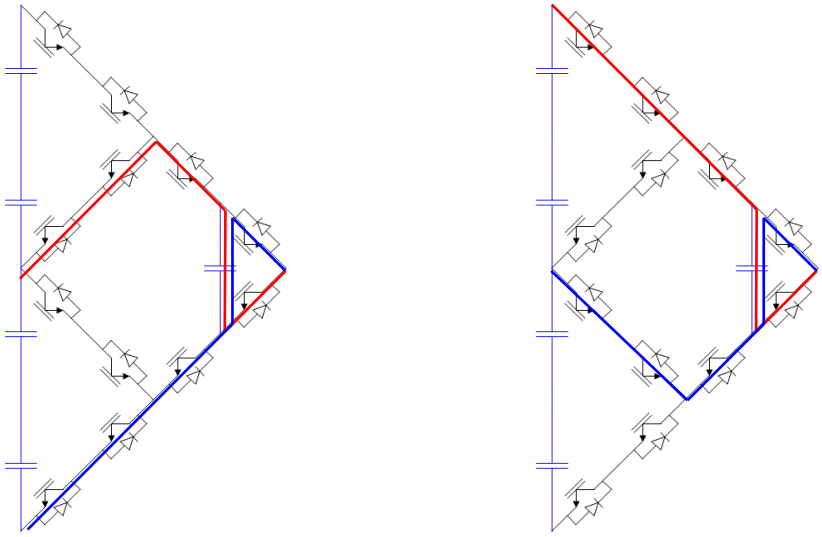


Figure 86, Redundant states for FC voltage control, (a) Uout = -U_{DC}/4, (b) Uout = +U_{DC}/4

Figure 86 shows two sets of redundant vectors with the same output voltage but opposite current sign in the flying capacitor. If two redundant states are applied for the same time on average (assuming high switching frequency in comparison with the rate of change of load current), the flying capacitor stays balanced. These two states will naturally be chosen to be applied subsequently, if an optimum PWM or a space vector modulator is applied. The resulting average neutral point current is half of the phase current for U_{out} = -U_{DC}/4 (or U_{out} = U_{DC}/4). In this standard case, the flying capacitor is balanced by the application of one output level only.

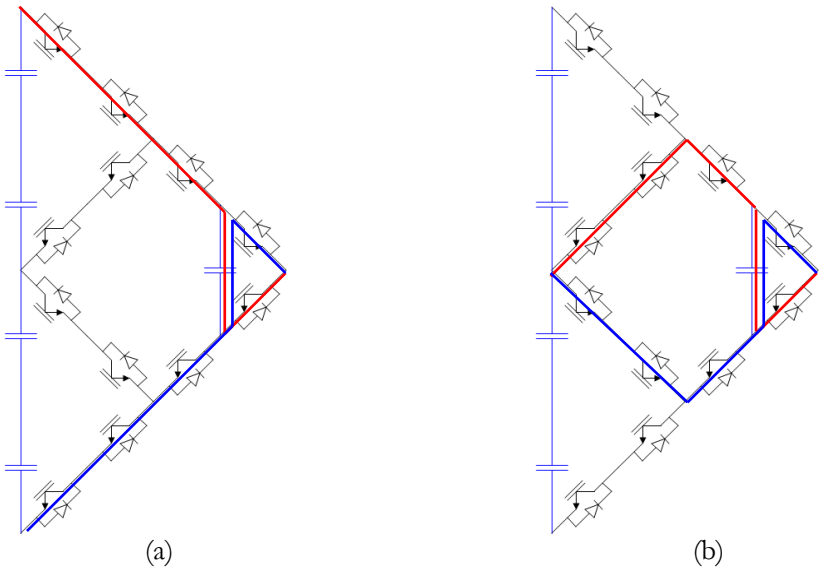


Figure 87, Combination of –U_{DC}/4 and U_{DC}/4 for FC balancing with non truly redundant states, (a) zero U_{out} with zero NP current, (b) zero U_{out} with maximum NP current

It is also possible to balance the flying capacitors with two different levels: $U_{DC}/4$ and $-U_{DC}/4$ with different current direction in the flying capacitor. Any two space vectors with a given phase at $-U_{DC}/4$ for one vector and the same phase at $+U_{DC}/4$ for the other vector can be combined according to Figure 87 (a) or (b) resulting in either no NP current or full NP current for the given phase. This deviates clearly from the standard approach previously presented.

The application of two non adjacent levels within one modulation period means that optimum modulation (as defined in the glossary) is no longer used on the phase leg level. However, optimum modulation can still be maintained in the phase to phase voltages, if steps are applied in the CM, allowing for an application of the partner states (see definition in TABLE 46 without generating any DM distortion.

TABLE 46, DEFINITION OF MODIFIED AND VIRTUAL SPACE VECTORS

Name	Description
Partner states	Two states according to Figure 87 (a) or (b), one generating $-U_{DC}/4$ the other $+U_{DC}/4$ (in the same phase) generating either zero or maximum NP current.
Modified vector	Space vector incorporating two partner states within the same 2-D vector.
Virtual vector type 2	Space vector incorporating two partner states within adjacent 2-D vector.
Virtual vector type 1	Space vector incorporating two partner states within not directly adjacent 2-D vectors but 2 levels apart.

These new type of combined vectors can be applied like real vectors in SVM, which means they can be used as vertices in a NTV SVM or they can be incorporated in vector sequences.

6.1.2 Availability of modified and virtual space vectors in the αβ-plane

The availability of the new space vectors can be investigated on one phase leg. The result can then be extended to all three phases. The example of phase b is chosen. There is a certain range, where phase b can be +UDC/4 and there is a certain range where b can be –UDC/4. The overlap or distance between these regions determines the type of new vector that is available in a given point.

Where the two areas in Figure 89 overlap, a combination of two partner states into a modified space vector (red) is possible (in the position of a discrete vector). Where two partner states (one in the red area, one in the blue area) are apart from each other by one level (adjacent discrete vectors), a virtual vector type 1 (blue) can be defined in the middle of the two (always between two discrete vectors). Where two partner states (one in the red area, one in the blue area) are apart from each other by two levels, a virtual vector type 2 (green) can be defined in the middle of the two. The same approach can be applied to all three phases resulting in the space vector graph in Figure 90.

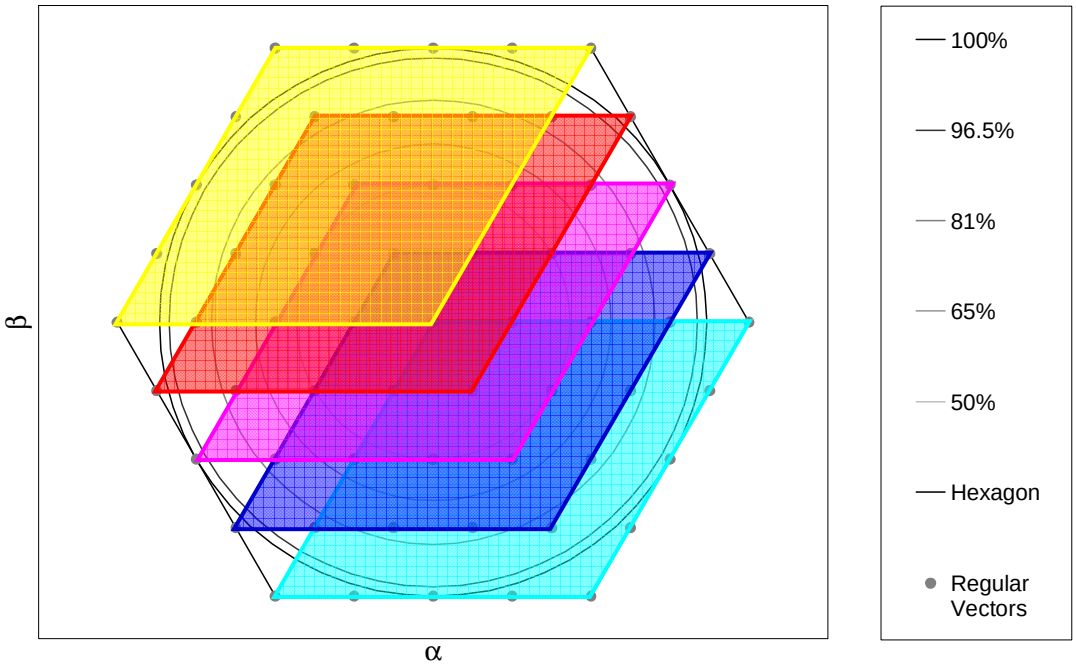


Figure 88, possible vector ranges for given output level in phase b
yellow: b = UDC/2, red: b = UDC/4, magenta: b = 0, blue: b = -UDC/4, cyan: b = -UDC/2

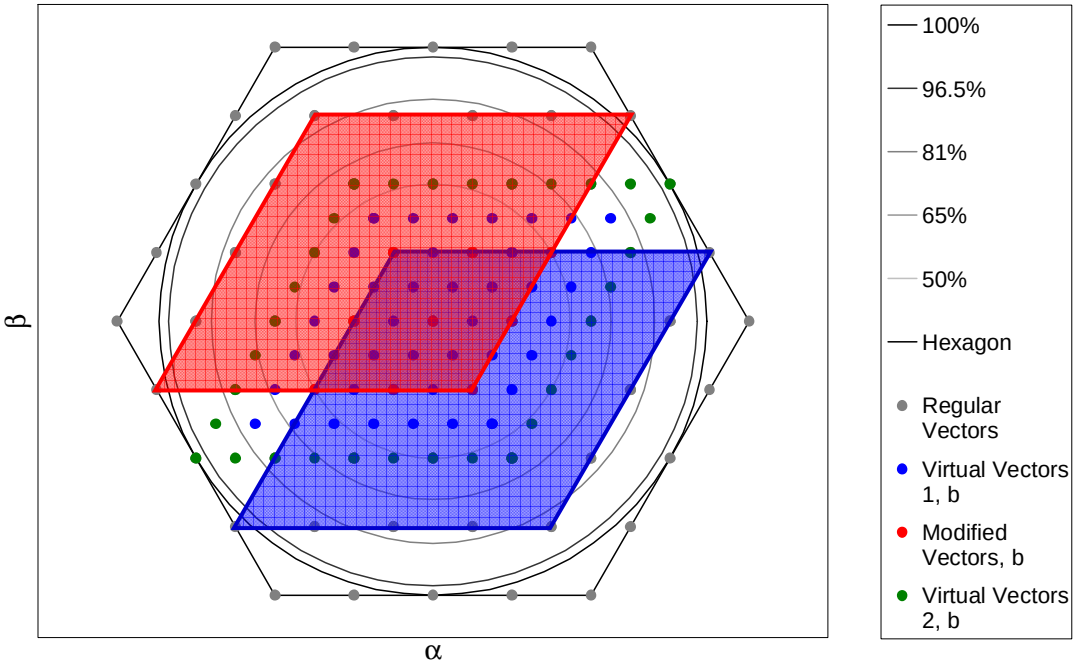


Figure 89, possible new vectors based on phase b
red: range for b = UDC/4, blue: range for b = -UDC/4

TABLE 47, PROPERTIES OF THE MODIFIED AND VIRTUAL VECTORS

All three types of vectors keep the FC voltages constant
All three types of vectors extend the range of available NP current
All three types involve high frequency CM voltage
The modified space vectors do not introduce any DM (differential mode) distortion
The virtual space vector type 1 may introduce moderate DM distortion but may also result in standard three nearest space vectors output depending on the reference vector.
The virtual space vector type 2 will always introduce some DM distortion as discrete vectors two levels apart are used (never results in three nearest space vector output).
Type 2 virtual space vectors are also available in all points of modified and type 1 virtual space vectors.
Type N virtual space vectors are also possible, making use of two partner states more than 2 levels apart. However, such vectors do not extend the range of available virtual space vectors and cannot increase the NP current range. They are not considered any further, as they introduce higher DM distortion and higher switching losses without any benefit.
The list of available vectors (as displayed in Figure 90) based on the principles of Figure 87 is comprehensive. No additional vectors of that type are possible (namely outside of the star shaped area).

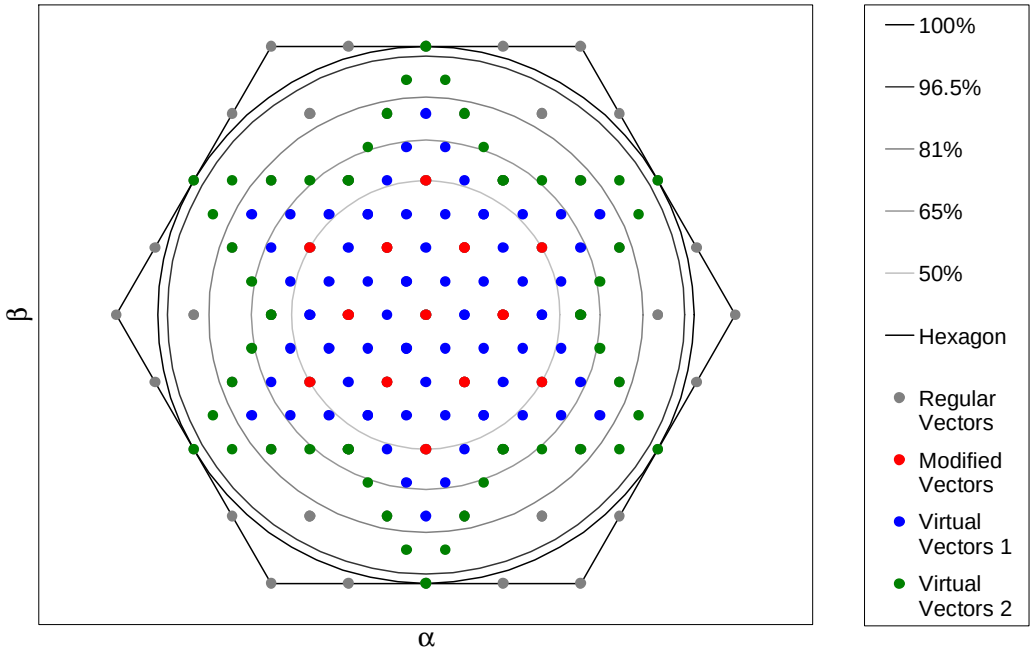


Figure 90, Full range of available modified and virtual space vectors

According to Figure 90, modified vectors are available up to 50% and useful up to around 65% of the full modulation index. The virtual vectors type 1 are available up to 75% and useful up to around 90% of the full modulation index. The virtual vectors type 2 are available up to 100% of the full modulation index.

6.1.3 Sample definitions of modified and virtual vectors

TABLE 48, REGULAR AND MODIFIED VECTORS {210}$_{2D}$

States				Levels			Currents			
Total	**a**	**b**	**c**	**a**	**b**	**c**	**i-NP**	**i-FC-a**	**i-FC-b**	**i-FC-c**
11&19	3	1&2	0	2	1	0	**ia +**	0	0	0
93&158	5&6	3	1&2	3	2	1	**ib/2**	0	0	0
239&247	7	5&6	3	4	3	2	**ic +**	0	0	0
11/12	¾	1	0	2	1	0	ia	0	ib	0
247/311	7	6	¾	4	3	2	ic	0	-ib	0
Average							**-ib/2**	0	0	0
19/20	¾	2	0	2	1	0	-ic	0	-ib	0
239/303	7	5	¾	4	3	2	-ia	0	ib	0
Average							**ib/2**	0	0	0

For pure reactive power, the current ib is dominant in this operating point ($i_a = i_c = -i_b/2$) Applying a linear combination of the regular vectors only (white fields), leads to any NP current from 0 to $i_b/2$. Usage of modified vectors (yellow and blue) results in an NP current between $-i_b/2$ to $i_b/2$. This is a very significant extension of the possible current range that can be used for NP control.

TABLE 49, TYPE 1 VIRTUAL VECTOR {3(1.5)0}$_{2D}$

States				Levels			Currents			
Total	**a**	**b**	**c**	**a**	**b**	**c**	**i-NP**	**i-FC-a**	**i-FC-b**	**i-FC-c**
	5&6	1&2	0	3	1	0	ia/2+ib/2	0	0	0
	7	5&6	1&2	4	3	1	ib/2+ic/2	0	0	0
Average							ib/4	0	0	0
	7	3	1&2	4	2	1	ib+ic/2	0	0	0
	5&6	3	0	3	2	0	ia/2+ib	0	0	0
Average							3ib/4	0	0	0
	5&6	1	0	3	1	0	ia/2	0	ib	0
	7	6	1&2	4	3	1	ic/2	0	-ib	0
Average							-ib/4	0	0	0
	5&6	2	0	3	1	0	ia/2+ib	0	0	0
	7	5	1&2	4	3	1	ic/2+ib	0	0	0
Average							3ib/4	0	0	0

In the case of the virtual vectors introduced in TABLE 49, the NP current range can be extended: standard schemes allow for $i_b/4$ to $3i_b/4$, the virtual vector for $-i_b/4$ to $3i_b/4$.

TABLE 50, TYPE 2 VIRTUAL VECTOR {420}$_{2D}$

States				Levels			Currents			
Total	**a**	**b**	**c**	**a**	**b**	**c**	**i-NP**	**i-FC-a**	**i-FC-b**	**i-FC-c**
	7	¾	0	4	2	0	ib	0	0	0
	7	1	0	4	1	0	0	0	ib	0
	7	6	0	4	3	0	0	0	-ib	0
Average							0	0	0	0
	7	2	0	4	1	0	ib	0	-ib	0
	7	5	0	4	3	0	ib	0	ib	0
Average							ib	0	0	0

The vector 420 has no redundant states; the NP current is always i_b. The application of virtual vector type 2 leads to a possible NP current range from 0 to i_b.

TABLE 51, POSSIBLE MODULATION SCHEMES MAKING USE OF MODIFIED AND VIRTUAL VECTORS

	Standard modulation scheme (NTV SVM, carrier based PWM, etc.)		**Predictive optimal sequence SVM**	**SVM based on alternate triangles**
	(a)	(b)	(c)	(d)
Definition of scheme	Replace individual vectors directly by the partner states of a modified or virtual vector.	Replace complete sequence within a given triangle by a predetermined sequence making use of modified and virtual vectors.	Evaluation of multiple sequence according to the POS (predictive optimal sequence) SVM scheme as proposed in paragraph 6.2	New small triangles can be defined based on the position of the type 1 virtual vectors.
Explanations and comments	This works fine for modified vector and virtual vectors type 2. Virtual vectors type 1 would still need to be implemented with an alternate algorithm. This scheme is likely to generate high switching losses as it applies CM jumps without considering the rest of the modulation sequence.	This approach allows making a pre-selection of modified and virtual vectors to be applied and determines all possible sequences off line. This scheme produces relatively low switching losses as the whole sequence can be optimized and partner states are not applied directly one after another. There is simple application at runtime, once a proper definition of sequences has been made offline.	This approach is really an extension of the POS SVM. The systematic inclusion of modified and virtual vectors in the sequences leads to high performance regarding NP and FC control. The calculating effort is even higher than for the pure POS SVM approach.	This requires new algorithms to determine application times of states in modified and virtual vectors, as well as algorithms for the choice of modulation type. The implementation of the actual nearest three vector modulation is equivalent to standard SVM. But an optimal choice of a set of vectors to be used is complex. If multiple modified and virtual vectors are used in one triangle, up to 12 states may need to be applied.

6.1.4 Application of modified or virtual vectors

Modified or virtual vectors can be applied in different ways as indicated in TABLE 51. The most obvious approach is the use of the modified and virtual vectors as vertices in NTV SVM. However, there is a lot of redundancy. The choice of base vectors to be used is not obvious. An online optimization is quite demanding and does not necessarily result in best performance. Furthermore, a direct application of virtual vectors without specifically integrating the states within a sequence will result in high switching losses due to the jumps in CM.

An offline sequence optimization applying modified and virtual vectors according to TABLE 51 (b) offers high performance at reasonable complexity. This approach has been chosen to be implemented for simulation and experimental verification.

6.1.4.1 Virtual vector sequences generation

The development of the virtual vector sequence modulation scheme can be illustrated with the following examples.

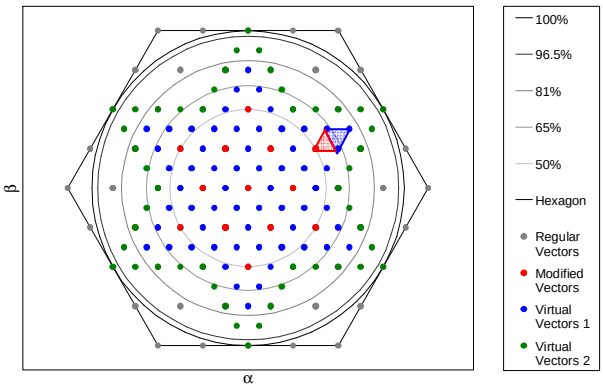


Figure 91, Sample triangle incorporating three virtual vectors type 1

The blue triangle in Figure 91 can generate the following three virtual vectors type 1:

- $\{432-310\}_{VV1}$
- $\{310-431\}_{VV1}$
- $\{431-210\}_{VV1}$

All these vectors can generate a current I_{NP_b} either of zero or the full phase current I_{out_b}. These three virtual vectors could be used for a SVM based on the blue triangle. A NTV algorithm for this small triangle could be applied. Each of the three virtual vectors would get its application time and would need to split it between the partner states. The partner state would then need to be put in an order to be physically applied.

A simpler implementation is possible based on the following observation: In all triangles incorporating modified and / or virtual vectors, some of the partner states coincide. This allows for easy optimization regarding losses. The states are simply aligned in ascending order regarding CM voltage. This results in the following sequence for the example from Figure 91:

- $\{210-310-431-432\}_{3D}$

Only four states instead of 6 need to be applied. These four states describe a regular sequence of 4 of the standard size triangle. The virtual vectors are not visible anymore as such. This chosen approach does not limit the NP control capacity in comparison with a 6 vector sequence. If the redundant states of the 6 vectors are all optimized for the same NP and FC control criteria, they always reduce to only 4 states automatically. In the phase featuring the partner states, only states according to Figure 87 (a) and (b) are chosen to get either maximum or minimum NP current.

The calculation of applications times could still be done on the small triangle level. However, it seems more straight forward to do the calculation directly for the standard size triangle.

The duty cycle d_{xyz} (= T_{xyz}/T_{MP}) of the two middle vectors in the sequence are given directly by the NTV SVM. The same is true for the sum of the duty cycles of the starting and the ending vectors:

$$d_{210} + d_{432} = 1 - d_{310} - d_{431} \tag{80}$$

The two redundant states $\{210\}_{3D}$ and $\{432\}_{3D}$ need to be timed such that the FC's stay balanced. This can be achieved by:

$$d_{210} + d_{310} = d_{431} + d_{432} = 0.5 \tag{81}$$

This condition can be met for all space vectors within the small blue triangle and more generally for:

$$(d_{310} < 0.5) AND (d_{431} < 0.5) \tag{82}$$

This means that the red triangle can use the same sequence. This can also be confirmed by the analysis of the vertices of the red triangle:

- $\{432 - 210\}_{MV}$
- $\{432 - 310\}_{VV1}$
- $\{431 - 210\}_{VV1}$

The resulting sequence is again (as predicted):

- $\{210 - 310 - 431 - 432\}_{3D}$

Likewise, many other small triangles share common sequences. However, this does not matter from implementation point of view. Simply identical sequences will be stored in certain parts of a look up table. Like with an individual virtual vector, the sequence can be used to choose the NP current generated by phase b. The states to generate levels 1 and 3 in phase b can be chosen to either have zero NP current ($I_{NP\_b} = 0$ if all states connecting to plus or minus of the DC link) or the full phase b current in the NP ($I_{NP\_b} = I_b$ for all states connecting to NP). The total NP current is the sum of the chosen phase b NP current and the phase a and phase c NP current, which depend on the state selector for the FC control in the corresponding phases. Obviously, this scheme is most powerful if the current in phase b is largest, which is the case for reactive power operation in the chosen triangle.

Outside of the star shaped area with blue dots in Figure 90, no virtual vectors type 1 are available. The proposed concept cannot be applied directly, but the same approach can be taken with larger triangles and virtual vectors type 2.

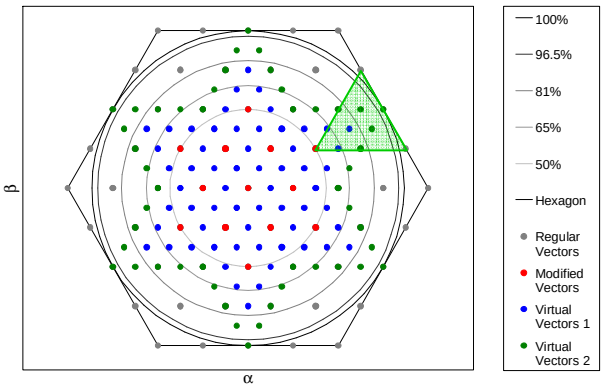


Figure 92, Sample triangle incorporating three virtual vectors type 2

The following virtual vectors type 2 can be generated with the green triangle:

- $\{432 - 410\}_{VV2}$
- $\{410 - 430\}_{VV2}$
- $\{210 - 432\}_{VV2}$

The resulting virtual vector sequence is:

- $\{210 - 410 - 430 - 432\}_{3D}$

The duty cycles of these states are easily calculated by an NTV SVM algorithm based on large size triangles. The sequence based virtual vectors type 2 is applied only, if no sequence based on virtual vectors type 1 is available. For example, the proposed triangle incorporates the small size triangles from the previous paragraph. The virtual vector 2 sequence could also be applied for those triangles, but the virtual vector 1 sequence is preferable regarding switching losses and output voltage distortion.

The yellow triangle in Figure 93 can be formed by modified and virtual vector states using partner states in any of the three phases a, b or c. Each phase offers several possible sequences with different starting point and different CM voltage. Examples for the different phases:

- Sequence for phase a: $\{100 - 110 - 321 - 322\}_{3D}$
- Sequence for phase b: $\{210 - 211 - 332 - 432\}_{3D}$
- Sequence for phase c: $\{221 - 321 - 433 - 443\}_{3D}$

The actual sequence depends on the small triangles. There will be multiple different sequences to be used within the yellow triangle. Depending on the current amplitudes in the three phases, one of the sequences can be chosen. As a consequence, this strategy is effective for any load angle for low modulation depth.

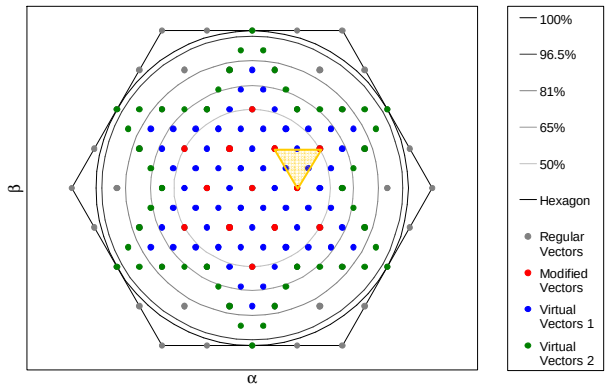


Figure 93, Sample small triangle with virtual vector sequences for all phases

TABLE 52, DEFINITION OF THE VIRTUAL VECTOR SEQUENCE MODULATION SCHEME

1. Predetermined sequences of 4 states shall be applied. This corresponds with half a SVM or CB PWM period. Two types of sequences are possible: a. Virtual vector sequence type 1 based on regular size triangles and incorporating only modified vectors or virtual vectors type 1. No DM distortion is generated in this case. b. Virtual vector sequence type 2 based on large size triangles and incorporating also virtual vectors type 2. DM distortion is generated in this case.
2. The choice of sequence is based on small triangles (according to virtual vector type 1 spacing)
3. The actual sequences to be applied are based on triangles of original or double size.
4. Some small triangles (e.g. outside the star region) refer to the same sequence.
5. Multiple sequences may be stored per triangle. The sequence to be applied is chosen based on operating point (load angle) or a chosen optimization criteria. Namely, there are several options in the low modulation depth range, where all phases feature partner states.
6. Redundant states in phases not related to the partner states are chosen online (modification of the predetermined sequences) according to the state selection scheme also used in the standard modulators (depending on FC voltage deviation and phase current)

6.1.4.2 Availability of virtual vector sequences

Four different regions have been identified:

1. Region at low modulation depth where virtual vector sequences type 1 are available for all of the three phases (yellow in Figure 94). This region performs well for all load angles.
2. Region at intermediate modulation depth where virtual vector sequences type 1 are available only for one phase (blue in Figure 94). This region extends the effective operating range, while keeping a non distorted DM output. This region performs best in reactive power operation.
3. Region at high modulation depth where virtual vector sequences type 2 are available for one phase (red in Figure 94). This region generates higher switching losses and increases DM distortion, but it is effective up to the over-modulation region. It performs best for reactive power but also improves the NP control capacity for active power operation.
4. Region at high modulation depth where no virtual vector sequences are available at all. In these regions, any standard modulation and NP control scheme can be applied.

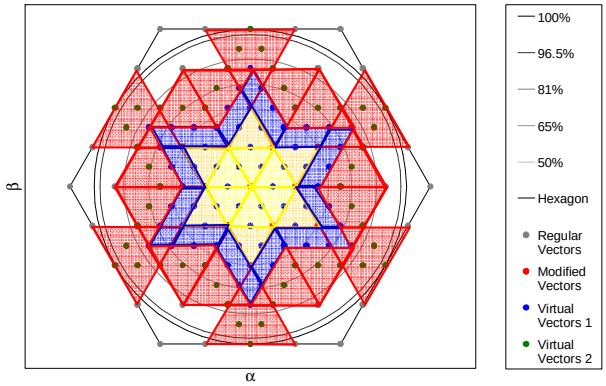


Figure 94, Availability of virtual vector sequences

The red area outside of the star shaped area defined by the green dots has virtual vector sequences type 2; however, there will be no perfect balance of the flying capacitors but improved NP controllability. A scheme without that extension can easily be implemented by a different sequence selection scheme. The whole area of the hexagon is covered well with virtual vector sequences, which indicates that the concept is powerful for all physically possible modulation depths including the non sinusoidal over modulation region.

6.1.5 Performance impact of modified and virtual vectors

6.1.5.1 Minimum and maximum NP currents in function of θ

Minimum and maximum NP currents can be calculated for balanced and undistorted operating conditions by simply applying a matrix of operating points to the controller. Limits for pure reactive power operation are given in Figure 95. The impact on minimum and maximum NP

current is obviously very large (compare with last column of TABLE 23). A full set of graphs for different load angles and modulation schemes is given in appendix 9.5.3.

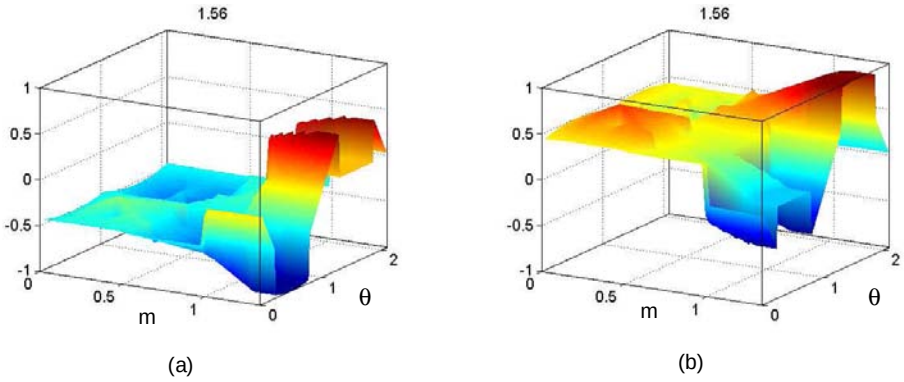


Figure 95, (a) Maximum and (b) minimum NP currents in function of modulation depth and voltage angle θ in pure reactive power operation

6.1.5.2 Average minimum and maximum NP currents

The average minimum and maximum NP currents over the fundamental period are a measure for the NP control capacity. For low modulation depth, virtual vector sequences are available for several phases. As a result, the NP current control capacity can be increased to 50% (of the peak phase current) for all load angles at low modulation depths down to zero. For high modulation depth, virtual vector sequences are available for one phase only and the effectiveness is depending on the load angle. Nevertheless, there is a significant impact on the NP current control capacity in both reactive and active power operation, as can be seen from Figure 96. Notably in the over modulation region, the modified and virtual vector scheme still provides effective NP control capacity. Note that for zero load angle, the unconstrained DC CM injection performs the same as the real time NP current scheme; the green curve is not visible in the graph as it coincides with the blue curve. Note that the red lines in Figure 96 (b) for minium and maximum average NP currents over a fundamental period correspond with an averaging of the functions in Figure 95 over θ.

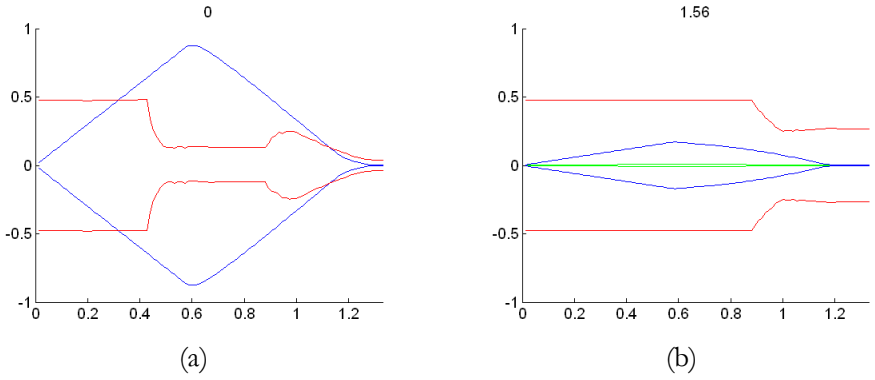
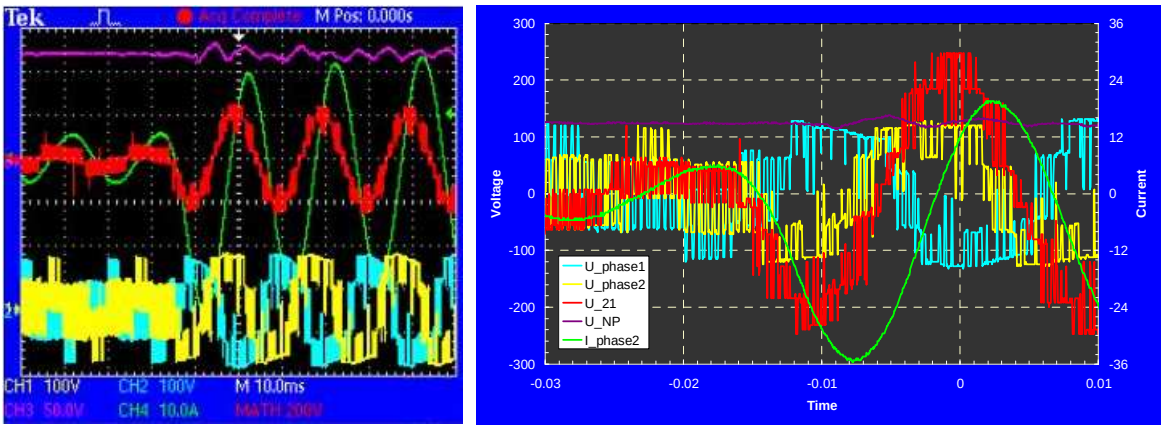


Figure 96, minimum and maximum average NP currents in function of load angle, modulation type and modulation depth. Red: modified and virtual vector scheme, Blue: real time NP current scheme, Green: unconstrained DC CM injection scheme. (a) φ = 0 (cos(φ) = 1), (b) φ = 1.56 (cos(φ) = 0.01)

A full set of graphs for different load angles φ is given in appendix 9.5.4.

6.1.6 Implementation of a virtual vector modulator and experimental verification

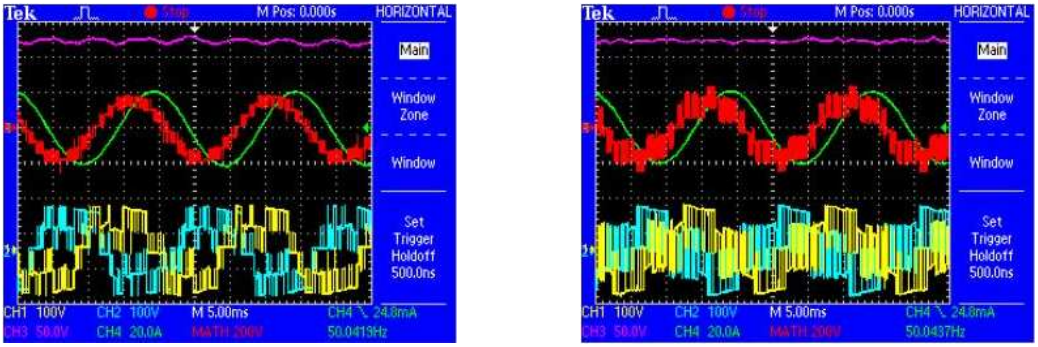
The virtual vector modulator has been implemented based on lookup tables for the first segment. All other vectors are transformed into that first segment to calculate states and application times. The calculations are done based on a non perpendicular coordinate system, very similar to the algorithm presented in [67]. A seamless integration of the different sequences is crucial, as there may be multiple changes in type of sequence within a fundamental period (see Figure 94). Also, the modulator needs to be compatible with standard modulators so that a smooth transition between the different operating modes is guaranteed. These features have been confirmed both by simulation and experiment.



CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2}

Figure 97, Virtual vector modulation at low modulation depth (m=0.2) and high modulation depth (m=0.9) in pure reactive power operation with zoom on transition period

Figure 97 shows a step in modulation depth from m=0.2 to m=0.9. This step includes a transition from virtual vector sequences type 1 to virtual vector sequences type 2, which seems to go very smooth. For low modulation depth, only virtual vector sequences type 1 are applied. They generate systematic 2 level steps in the phase voltages, but they are not visible in the phase to phase voltages (apart from glitches generated by commutation). Accordingly, there is no distortion in the current compared to any standard modulation scheme. The NP current can be kept zero in this operating mode and there is no low frequency ripple in the NP voltage. For high modulation depth, virtual vector sequences type 2 are applied. They also generate 2 level steps in the phase voltages, but these are not completely cancelled out and are partly visible also in the phase to phase voltages as expected from theory and simulation. For high modulation depth, the NP current cannot be cancelled out completely and a third harmonic appears.



(a) (b)

CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2}

Figure 98, NP current ripple for real time NP current scheme (a) and virtual vector scheme (b) at medium modulation depth (m=0.75)

Figure 98 shows the impact of the modulation scheme on the minimum NP voltage ripple. The virtual vector scheme can significantly reduce the NP voltage ripple at the cost of increased losses and increased output voltage distortion.

6.2 Online calculated optimal sequences by the use of optimal control schemes

When considering NP and FC control, all required quantities can be controlled separately, as has been done with previously proposed control schemes: Output voltage (for torque, flux, power or voltage control) can be set in open loop by the appropriate $\alpha\beta$ vector (and feed forward control taking into account actual DC voltages); flying capacitors can be controlled by the appropriate share of redundant states; the NP can be controlled with the application of a CM and suitable choice of redundant states.

Alternatively, all parameters can be controlled at the same time, applying an optimal control scheme. This chapter introduces an approach to optimized SVM by means of optimal control for the generation of sequences of converter states to be applied. This is related to the work by Geyer/Papafotiou/Morari [51, 52] or J. Rodriguez et al. [54, 57], who use MPC (model predictive control) to implement modulators integrating control of internal and external quantities. Those published concepts act directly on the individual switching states, resulting in a "next best vector" type of modulation (see 4.4.3) and variable frequency operation. In contrast, the method proposed in this chapter uses model based prediction and optimal control but applies those concepts on a number of generic sequences rather than next optimal vectors. As a result, the operation of the converter is much closer to classic CB PWM or SVM with constant switching frequency with the notable difference that multiple quantities are controlled at the same time.

Due to the large number of available states in ML converters, any sequence based on SVM can be generated in a large number of different ways. To start with, the length of a SVM sequence is not inherently given. A minimum of three discrete vectors is required to approximate any continuous space vector in $\alpha\beta 0$. However, more vectors are possible. It has been shown that CSPD PWM results in optimized harmonic performance for ML converters [35]. Such a modulator results in 7 states over one full period of the carrier. If there are two samples per carrier period, there are still 4 vectors to be applied per sampling period. Apart from the degree of freedom in choosing a certain type of sequence, there is also the degree of freedom in choosing redundant states within a given sequence frame. For the choice of redundant states there are many constraints and optimization criteria, which can be applied.

TABLE 53, CONSTRAINTS AND OPTIMIZATION CRITERIA FOR OPTIMAL SEQUENCE SVM

Constraints:
- DM voltages according to carrier based modulation, nearest three vector approach or any other alternate method for calculation of output level and application time
- NP and FC to be controlled within certain bounds
Optimization criteria may include:
- Switching losses minimization
- Output harmonics minimization
- CM voltage minimization

This list may be larger or smaller, but there are always multiple objectives and /or constraints, which makes the problem very suitable for an optimal control approach. Due to the discrete nature of the converter states, the problem to be solved is either a pure integer problem (if output levels and applications times are based totally on a separate nearest three vector scheme) or it is a mixed integer problem, if continuous variables for the timing are introduced (e.g. distribution of starting and end vector in a SVM scheme). Although the complexity of the problem seems to be moderate and intuitively comprehensible, the large number of possible states in a ML converter (512 in the ANPC1) leads to a very high number of physically possible sequences. This most probably leads to a demanding control problem, as there is only a short time available (~100 µs) to not introduce long delays in the control loop. This means that the development of any control algorithm needs to take into account implementation issues from the beginning and provide suitable simplifications to get an affordable complexity. Mixed integer problems of the given complexity are likely to be beyond today's control system capabilities, the concept proposed in this chapter therefore limits itself to a pure integer problem and determines all application times based on a standard NTV SVM.

6.2.1 Definition of an optimal sequence SVM scheme

In the first part of the chapter, multiple possibilities for tuning the algorithm are presented and backed up by simulation; in the second part of the chapter, an algorithm optimized for implementation with low calculation time is presented. This second algorithm has been verified experimentally.

TABLE 54, DEFINITION OF PREDICTIVE OPTIMAL SEQUENCE SVM

1. Vectors and application times for a given sampling period are determined based on standard modulation schemes (SVM or carrier based)
2. All suitable sequences based on chosen criteria are determined (subset of all physically possible sequences generating the desired output voltage vector)
3. Relevant quantities are predicted (calculation based on converter model, load modeled as current source)
4. Partial enumeration of all possible sequences is used to choose the best sequence to be applied to the converter

With this relatively simple and straight forward approach, the prediction horizon is always one. Even though multiple states are applied in the end, these are always calculated as one unit and they are not split; there is no update of the calculation after application of the first state. The scheme could be modified either by recalculation after the application of the first state or by prediction of the next sampling period. Both approaches are very demanding from a calculation point of view and neither of them would promise a leap in performance.

6.2.1.1 Determination of possible sequences

If multiple commutations are allowed between each state to be applied, the total number of possible sequences can be very high. If any redundant vectors for a sequence of 4 vectors could be

chosen, the total number of sequences possible would exceed 50'000 in the case of the ANPC 1 (for triangles with one vertex on the origin). However, a totally free application of states is not useful, as multiple commutations create high losses. Ideally, there should be only one single commutation between subsequent states, which guarantees low switching loss. On the other hand, such a restriction may limit the effectiveness of the optimal control approach. The algorithm may be trapped in a certain region and not be able to switch over to the globally optimal region. This may be the case especially for low cos(φ) and moderately low modulation depth, where the NP current function is non monotonic. The modulator may then operate on one side of the non-monotonic function, whereas the other side would have offered better performance. There are multiple possibilities to overcome that problem as will be shown later.

TABLE 55, SEQUENCE GENERATION FOR PREDICTIVE OPTIMAL SEQUENCE CONTROLLER

1. Choice of any starting vector on a vertex of the target triangle within a defined number of commutations from the last applied state.
a. If no vertex of the large triangle can be reached within the given number of commutations, the vector with the lowest number of commutations required is chosen
2. A set of second vectors on the triangle is determined by applying a defined maximum number of commutations (starting from the vectors obtained in step 1)
3. A third and fourth set of vectors are determined in the same way to complete the full sequence

All sequences possible form a tree structure and the total required calculation effort can be calculated from that tree. The total calculation effort depends highly on the complexity of the objective function but is proportional to the number of sequences considered in any case (full enumeration).

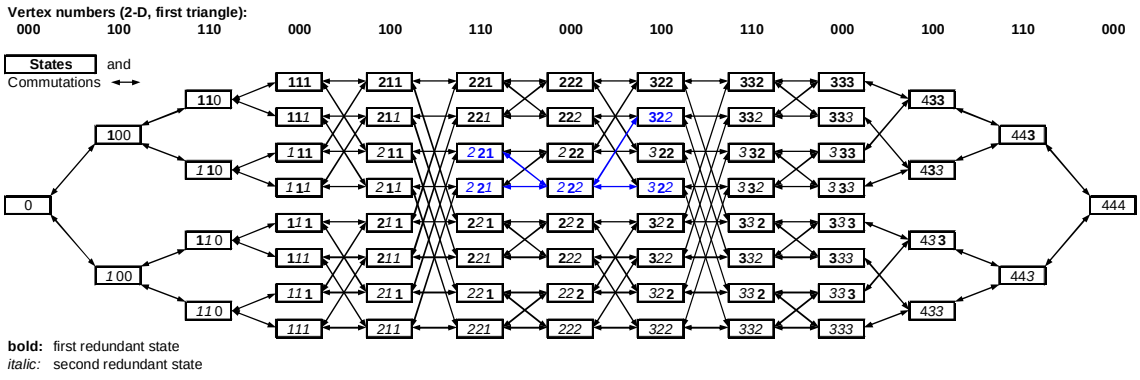


Figure 99, ANPC 1 state graph for the triangle {000 – 100 – 110}$_{2D}$, possible starting states according to step 1 (in TABLE 55) in blue (assuming *22* as last active state as an example)

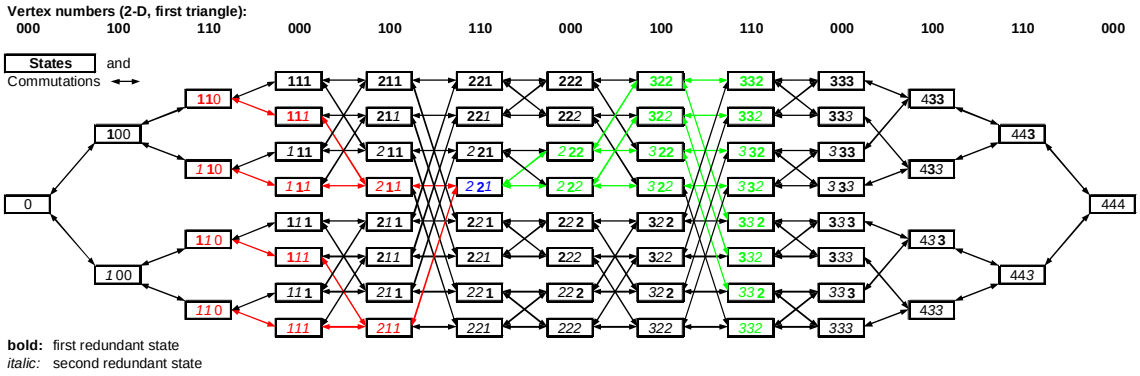


Figure 100, ANPC 1 state graph for the triangle {000 – 100 – 110}$_{2D}$, possible single commutation sequences (assuming *221* as starting state obtained in step 1 as an example)

Figure 99 and Figure 100 show sample cases of single commutation sequences based on a given last state. Figure 100 is one out of five graphs that can be drawn based on Figure 99. In Figure 100, red indicates decreasing CM voltage, green indicates increasing CM voltage. The largest number of sequences is obtained for any last state 221 or 322: 5 starting points result in 10 trees of sequences, 8 of those trees result in 8 sequences each, 2 of those trees result in 2 sequences each, resulting in the following maximum number of sequences (equation (83)) based on single commutations.

$$N_{seq\_\max} = 8 * 2^3 + 2 * 2^1 = 68 \tag{83}$$

Multiple sequences applied one after the other will describe a continuous path in abc. Depending on NP current requirements, the controller will automatically increase or decrease CM voltage by spiraling up or down the triangles (for example of a star shaped path with CM variation is given in Figure 50). The rate of change of the CM voltage is limited by the maximum number of commutation to be applied per transition.

6.2.1.2 Variations of basic scheme

A number of variations of this basic scheme are possible and have been tested in simulation. Multiple commutations for each state change can be applied to improve performance. Optimal states can be determined for each vertex independently of the number of commutations required. Such optimal states can be integrated in the predetermined sequences (e.g. single commutation sequences). This allows for CM jumps and generation of sequences similar to the virtual vector sequences presented in paragraph 6.1. Losses may increase due to the multiple commutations. However, the concept will enables reaching more optimal operating points very fast and reduces the risk of being trapped in a non global optimum. Optimal state will not be applied if not necessary, as they will generate a significant cost for the switching losses. The use of optimal states is an alternative to the multiple commutations approach resulting in similar performance with much less sequences to be calculated.

TABLE 56, PROPERTIES OF SCHEME ALLOWING MULTIPLE COMMUTATIONS

1. Discontinuous modulation (only 2 phases operating) is possible
2. Decoupling of CM from sequence orientation
3. Loss balancing between different phases
4. Higher common mode jump within one modulation cycle to improve NP control
5. The switching losses do not necessarily increase with double commutations. If the two phases with the lower currents are switched, the third current is the sum of the two lower currents and the resulting switching losses also roughly add up to the value of a single commutation of the highest current.
6. The complexity and calculation effort is significantly increased. Double commutations allow for up to 6 redundant states in each step of a sequence. As a result one individual tree of sequences may have 6^3 = 216 possible sequences. Also the maximum number of starting states is increased, so that significantly more than 1000 sequences are possible in the worst case (for the ANPC 1).

6.2.1.3 Definition of the objective function

The DM output voltage is a constraint which is satisfied by the nearest three vectors modulation. All considered sequences then result in the correct output voltage. Therefore, no converter output quantity needs to be integrated in the objective function. NP and FC voltages as well as losses can be predicted based on the converter model and the sequences of states determined.

TABLE 57, QUANTITIES TO BE USED IN OBJECTIVE FUNCTION

Quantity to be integrated in objective function	**Comment**
Switching losses	The switching loss cost is primarily proportional to the total losses, but can also include a term on loss distribution
Voltage deviation in flying capacitors	Square function to minimize total energy in flying capacitors or piecewise linear function to achieve quasi tolerance band behavior
Voltage deviation in NP	Square function to minimize total energy in NP or piecewise linear function to achieve quasi tolerance band behavior
Output quantity THD or WTHD	Approximation algorithms based on the output voltage can be used (e.g. harmonic flux trajectory, [107]) or load models can be used to determine current or torque ripple.
CM voltage optimization	CM voltage is relevant in motor applications because of the bearing current generation and isolation stress.
Apparent output switching frequency	A certain apparent output switching frequency may be required to optimally operate a filter or to avoid certain frequencies (mechanical resonances, signaling)

The performance of the optimal sequence modulator can be tuned depending on requirements by choosing an appropriate objective function.

6.2.2 Modulator implementation and simulation results

A modulator as described in the previous paragraphs has been implemented in Matlab/Simulink by use of an m-function. Several parameters of the modulator can be chosen flexibly, including the number of commutations per state change, the use of optimal states, THD minimization scheme, and CM optimization. A set of simulations has been done to demonstrate the performance and capabilities of the modulator. For comparison, standard carrier based modulators have also been used (CSPD PWM, 3rd harmonic injection PD PWM).

TABLE 58, OPERATING CONDITIONS FOR OPTIMAL SEQUENCE MODULATOR SIMULATIONS

PWM(X)	PD carrier based PWM modulation
X = 0	Continuous modulation with 3rd harmonic injection (1/6 of fundamental)
X = 1	Discontinuous modulation (highest absolute value output clamped to rail)
SVM(XY)	space vector modulation
X = 0	only single commutations (per state change) allowed
X = 1	double commutations (per state change) allowed
Y = 0	no THD minimization applied
Y = 1	THD minimization applied

TABLE 59, VARIOUS MODULATION TYPES WITH 500 HZ SWITCHING FREQUENCY, M = 0.8, COS(φ)=0.75, R_{LOAD} = 2 Ω, L_{LOAD} = 1mH

Modulation Type	f_{switch} Output	f_{switch} Internal	Switching Losses	THD U12	THD I1	THD I2	THD I3	THD avg.	Comments
SVM(00)	**500**	**585**	**100%**	**20.3**	**8.1**	**8.3**	**7.8**	**8.1**	**Reference operation**
SVM(01)	**503**	**520**	**98%**	**16.8**	**7.3**	**6.0**	**7.2**	**6.8**	**Reduction in THD**
SVM(10)	**497**	**561**	**97%**	**19.9**	**6.3**	**8.0**	**7.5**	**7.3**	**Lower THD than single commutation approach**
SVM(11)	**497**	**680**	**101%**	**14.2**	**4.8**	**5.5**	**5.1**	**5.1**	**Very significant reduction in THD (U and I)**
PWM(0)	**503**	**595**	**105%**	**17.2**	**8.2**	**7.6**	**7.5**	**7.8**	**Relatively high loss and high THD**
PWM(1)	**511**	**751**	**101%**	**21.0**	**8.6**	**8.9**	**9.1**	**8.9**	**Very high THD**

From TABLE 59 and TABLE 60, we can observe that carrier based PWM with 3rd harmonic injection has always the highest level of losses.

For a given loss level, the current THD behaves as follows:

- Double commutation SVM has by far the lowest THD
- Single commutation SVM has the second lowest THD
- Carrier based PWM has the highest THD

For a given THD, the losses behave as follows:

- SVM has significantly lower losses than carrier based PWM
- Double commutation based SVM has lower losses than single commutation based SVM

TABLE 60, VARIOUS MODULATION TYPES WITH 2000 HZ SWITCHING FREQUENCY, M = 0.8, COS(φ)=0.85, R_{LOAD} = 2.4 Ω, L_{LOAD} = 0.25mH

Modulation Type	f_{switch} Output	f_{switch} Internal	Switching Losses	THD U12	THD I1	THD I2	THD I3	THD avg.	Comments
SVM(00)	**1990**	**2144**	**307%**	**17.5**	**6.4**	**6.5**	**6.5**	**6.5**	**Very low switching loss (3 times the loss at 4 times f_{switch}). THD cannot be compared as a different load is used**
SVM(01)	**1987**	**2121**	**408%**	**16.7**	**5.7**	**5.8**	**5.7**	**5.7**	**Moderate THD reduction but large loss increase**
SVM(10)	**1990**	**2268**	**305%**	**17.5**	**6.8**	**6.6**	**6.7**	**6.7**	**Very similar to single commutation operation**
SVM(11)	**1990**	**2573**	**407%**	**16.3**	**5.1**	**5.1**	**5.2**	**5.1**	**Significant THD reduction but large loss increase**
PWM(0)	**1990**	**2087**	**421%**	**17.3**	**6.5**	**6.3**	**6.3**	**6.4**	**Moderate THD with very high loss**
PWM(1)	**2023**	**2284**	**324%**	**21.0**	**7.8**	**7.8**	**7.8**	**7.8**	**Reduced losses but significant increase of THD**

It can be concluded that optimal sequence SVM performs better than carrier based PD PWM with 3rd harmonic injection (regarding the stated criteria) and the double commutation generally outperforms the single commutation approach (for the chosen operating points). Note that a number of issues have not been considered in the simulations presented above. The current THD (which is proportional to the voltage WTHD) varies with modulation depth [35]. This function over m and the worst case operating points would need to be considered for a comprehensive comparison of the modulation schemes. CSPD PWM has not been used in above simulations, as 3rd harmonic injection has been considered to be almost equivalent. This may make a significant difference in the chosen operating point. Apart from that, there are implementation issues to be considered.

The algorithm takes time to compute; the resulting delay degrades performance and limits the control bandwidth. Comparing the different modulation types we can state:

- Standard carrier based PWM or a NTV SVM can be done with very little computational effort.
- Optimal sequence SVM required significant calculation time
  - Around 2500 floating point operations are required in each modulation cycle in the single commutation scheme
  - Around 50'000 floating point operations are required in each modulation cycle in the double commutation scheme.

The maximum calculation time allowed depends highly on the switching frequency and the control bandwidth required. A maximum calculation time of around 100μs is assumed to yield reasonable performance in standard applications. This seems possible for single commutation optimal sequence SVM (either in an optimized C routine or hard programmed in an FPGA). A fast enough implementation of the optimal sequence SVM with double commutations is a very big challenge with today's available control hardware, but it may be feasible in the not too distant future.

6.2.3 Implementation on control platform and experimental verification

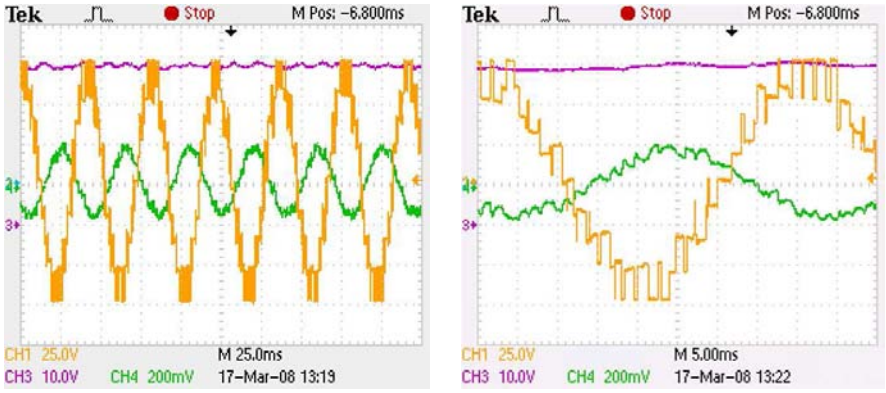
The predictive optimal sequence SVM has been implemented on a commercial control platform (OPCoDe by ABB), which allows implementation of control in Matlab / Simulink, simulation of the code in that environment and direct downloading of the same code to the target application. In order to allow implementation on the CPU rather than on the FPGA, the code has been optimized for fast execution.

6.2.3.1 Modulator adaptations for implementation on control platform

The sequence length has been reduced to 3 and only single commutations are allowed. This reduced the maximum number of sequences to be calculated to 40 (5 starting states with 2 trees each, each of the trees having 4 sequences). THD calculation has been excluded to further speed up calculation. No additional optimal states are considered.

6.2.3.2 Experimental results

The optimal sequence SVM algorithm has been verified on the 6kVA 5-L ANPC prototype. Figure 101 shows one specific operating point of m = 0.9. The DC-side of the converter is supplied by a constant DC source of V_{DC} = 80V and the AC-side terminals are connected to a three-phase RL load (10 Ω and 4.2 mH, cos(φ) = 0.966 at 25 Hz). The resulting current is 2.8 A.



CH1 (orange): U_{out1_2} CH3 (magenta): U_{NP} CH4 (green): I_{out3}

Figure 101, Predictive optimal sequence SVM scheme with single commutations

A 9-L waveform can be seen in the measured phase to phase voltages (given by the 5-L waveform in each phase) in Figure 101. The converter is balancing the NP as expected. A 3rd harmonic is clearly visible on the graph on the left side.

6.3 Executive summary for chapter 6

This chapter has introduced NP control methods for the 5-L ANPC based on SVM making use of optimized sequences. The first approach explores the possibility of combining specific states into modified and virtual vectors having different properties than the state combinations obtained with standard modulation schemes. The existence of such vectors is based on the fact that a flying capacitor cannot only be balanced by truly redundant states, but also by a combination of states with different output voltages. Namely a suitable combination of $+U_{DC}/4$ and $-U_{DC}/4$ states can generate either zero NP current or a large NP current while keeping the FC balanced. For small modulation depth, such states can be applied by CM jumps without impact on the DM voltage. If the states to be combined belong to the same $\alpha\beta$-vector, we call them modified vectors; if the states to be combined belong to adjacent $\alpha\beta$-vectors (one level apart), we call them virtual vectors type 1; if they are two levels apart, we call them virtual vectors type 2.

The availability of such vectors in the whole space vector hexagon has been analyzed. All vectors are available in star shaped regions of different size as shown in Figure 90. The impact of individual modified and virtual vectors has been investigated and is shown with TABLE 48 to TABLE 50. The new vectors could be applied directly for a NTV SVM, using those vectors on the vertices of new triangles. This approach is not as straight forward as it seems, as a large number of regular, modified and virtual vectors are available for the modulation. An online selection is computationally very demanding, as a very large number of sequences are possible.

An approach with an offline determination of optimal sequences has been chosen to be implemented. This approach allows for an optimization of the switching losses while providing large NP current control capacity. The predetermined sequences can be stored in a lookup table, which contains the true discrete state to be applied; the modified and virtual vectors are hidden in those states. The modulator can therefore use the standard discrete vertices for an NTV SVM rather than the virtual vectors with differing positions. This has the advantage that no new NTV algorithms need to be developed.

The modified and virtual vector sequence scheme is very powerful. The NP control capacity is highly increased for all modulation depths and all load angles. Minimum and maximum NP currents as a function of load angle and vector position are given in TABLE 87 in the appendix. Maximum and minimum average NP current over one fundamental period are given in TABLE 88.

An alternate method for the generation of optimized vector sequences is proposed in the second part of the chapter. The sequences are determined with a standard NTV SMV, but the choice of redundant states is done with an optimal control algorithm. This approach has the advantage that several objectives can be handled with one single controller. This may include, switching losses or harmonic distortion in addition to the capacitor balancing.

The theoretical number of possible sequences is very high. The evaluation of them has to be done by full enumeration, which is computationally very demanding. Therefore, only a subset of sequences can be considered. An obvious reduction of the number of sequences can be done by a limitation of the number of commutations allowed per transition to limit the switching losses. As an inherent feature of the concept, the state combinations according to modified and virtual vector definitions can be chosen automatically. However, this is only possible if a sufficiently large number of commutations per transition are allowed to enable the CM jumps required for the virtual vector application. In practice, this could not be realized. Several thousand sequences would need to be

considered in each modulation step. Different strategies to limit the number of sequences to be included in the evaluation are presented.

Simulations show promising performance regarding output voltage distortion and loss minimization trade off. Depending on the tuning of the control parameters, one of the two optimization criteria can be significantly improved compared to PD PWM. The modulator implemented for simulation is too complex for real time execution. A simplified version has been implemented for experimental verification. Basic functionality could be demonstrated, but the control performance was below expectations due to the simplifications applied. A significant effort is still required to implement a suitable algorithm on an FPGA rather than executing it on the CPU. This task has not been tackled in the frame of this thesis and could be the subject of future work.

7 APPLICATION AND VERIFICATION

This chapter relates the proposed modulation schemes to the different operating conditions regarding modulation depth and load angle as required by different applications (see also paragraph 2.2). A few specifc applications are discussed in the context of the suitablitiy of the modulation schemes proposed in this thesis.

Three ML topologies have high performance modulation schemes available and are suitable for all considered operating conditions. These are the ANPC 1, the ANPC 3, and the SMC. Hysteresis controllers making use of multiple modulation schemes had already been introduced for the ANPC3 and the SMC in chapter 1. This chapter introduces hysteresis controllers for the ANPC1. The experimental verification in this chapter includes a comparison of the NP control capacity for various modulation schemes and it demonstrates the performance of the proposed hysteresis controller.

7.1 General modulator capabilities

TABLE 61 to TABLE 63 state important features of the modulators considered in this thesis. They form a basis for the choice of a suitable modulation and control scheme for a given application.

The unconstrained DC CM injection control is very robust (except for reactive power operation) as it does not depend on current measurements and does not limit the CM. It can therefore provide always the highest NP current in case the NP current function is monotonic. All other schemes are sensitive to current measurement errors and delays in the control loop. Especially 6th harmonic injection an real time NP current function scheme require a low delay in the control loop to make sure the calculated limits for the CM do not reduce the range of controllable NP current. Modified and virtual vector sequence schemes are less sensitive as the current values are only required to determine the best choice of vector sequence to be applied. However, also the second best choice will lead to a very powerful control of the NP current. 6th harmonic injection and direct application of the real time NP current function are equivalent for pure reactive power and high modulation depth. They outperform the simple proportional feedback controller by far and are equivalent to optimized SVM schemes proposed in literature. The 6th harmonic scheme is to be favored whenever losses are important and CM voltage needs to be minimized. This scheme has much less CM jumps in steady state than the general schemes based on the real time NP current function.

The last proposed modulator calculating an optimal sequence with predictive methods relies very much on good real time values. Unfortunately, this is also the scheme requiring the longest calculation time. This can lead to a significant degradation of the control concept. It is therefore advisable to implement this scheme in hardware on a PLD (e.g. FPGA) to keep calculation times as low as possible.

TABLE 61, SUITABILITY OF THE DIFFERENT NP CONTROL SCHEMES FOR VARIOUS OPERATING POINTS

	m < 0.1		**0.1 < m < 0.9**		**m > 0.9**	
	cos(φ) < 0.15	**cos(φ) > 0.15**	**cos(φ) < 0.15**	**cos(φ) > 0.15**	**cos(φ) < 0.15**	**cos(φ) > 0.15**
Unconstrained DC CM injection, reference case	Very Poor	Medium	Poor	Good	Very Poor	Medium (Note 1)
Real time NP current function	Poor	Medium	Good	Good	Poor	Medium
6th harmonic	n.a.	n.a.	Good (for m > 0.5)	n.a.	Poor	n.a.
Modified vectors	Excellent	Excellent	Excellent (for m < 0.5)	Excellent (for m < 0.5)	n.a.	n.a.
Virtual vectors 1	n.a.	n.a.	Excellent (for m < 0.75)	Excellent (for m < 0.75)	n.a.	n.a.
Virtual vectors 2	n.a.	n.a.	Excellent	Excellent	Excellent (Note 2)	Excellent (Note 2)
Optimal sequence	Good	Good	Good	Good	Poor	Poor
ANPC 3 PWM	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent
SMC A / B / FC	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent

Note 1: The performance degrades in the very high modulation depth (including over modulation)

Note 2: Virtual vectors 2 can control the NP current up to very high modulation depths including pure trapezoidal modulation

TABLE 62, FEATURES OF THE DIFFERENT NP CONTROL SCHEMES (PART 1)

	CM / Impact on losses	**NP current range (I_{max} – I_{min}, measure for control-ability)**	**Harmonic performance in steady state (NP control not active)**	**Output voltage distortion when NP control active**	**DC link dimensioning (Note 1)**	**Implementation, Computational effort at runtime**
Unconstrained DC CM injection, reference case	no jumps / no impact on losses	below standard range for reactive power operation (Note 2)	According to base modulation scheme (e.g. PD PWM and /or CSVM)	No increase compared to steady state	standard value	simple, low computational effort
Real-time NP current function	occasional jumps / small loss increase	standard range	According to base modulation scheme	No increase compared to steady state	Reactive power: smaller DC link possible	simple, low computational effort
6th harmonic	no jumps / no impact on losses	almost standard range including for reactive power operation	According to base modulation scheme	No increase compared to steady state	Reactive power: smaller DC link possible	simple, low computational effort
Modified vectors	jumps in each cycle / medium loss increase	significantly above standard range at low modulation depth for all load angles	According to base modulation scheme	No increase compared to steady state	Low modulation depth: smaller DC link possible	off line calculation of suitable sequences, low computational effort (look up tables)
Virtual vectors 1	jumps in each cycle / medium loss increase	significantly above standard range at medium modulation depth for all load angles	According to base modulation scheme	No increase compared to steady state	Reactive power: significantly smaller DC link	off line calculation of suitable sequences, low computational effort (look up tables)
Virtual vectors 2	jumps each cycle / large loss increase	significantly above standard range at high modulation depth for all load angles	According to base modulation scheme	Significant increase of THD due to the 2 level steps	Reactive power: significantly smaller DC link	off line calculation of suitable sequences, low computational effort (look up tables)

Note 1: The comments on DC link dimensioning only refer to the constraints imposed by NP controllability for a specific modulation scheme. In reality, other constraints may be dominant (e.g. energy for ride through).

Note 2: standard range refers to the physical limitation of the NP current for a 3-L NPC in optimum modulation (without virtual vectors) as introduced in paragraph 4.7.1.2.

TABLE 63, FEATURES OF THE DIFFERENT NP CONTROL SCHEMES (PART 2)

	CM / Impact on losses	**NP current range ($I_{max} - I_{min}$, measure for control-ability)**	**Harmonic performance in stead state (NP control not active)**	**Output voltage distortion when NP control active**	**DC link dimensioning (Note 1)**	**Implementation, computational effort at runtime**
Optimal sequence	occasional jumps / medium loss increase	above standard range for all load angles (Note 2)	WTHD is slightly higher than for CSVM, but still better than many other modulation schemes	No increase compared to steady state	Depends highly on prediction horizon, theoretically smaller DC link possible	Complex algorithms (prediction and optimization), high computational effort
ANPC 3	smooth modulation, good switching loss distribution	above standard range for all load angles	According to base modulation scheme	No increase compared to steady state	Smaller DC link possible	simple, low computational effort
SMC A (Note 3)	smooth modulation, good switching loss distribution	above standard range for all load angles	According to base modulation scheme	No increase compared to steady state	Smaller DC link possible	simple, low computational effort
SMC B (Note 3)	Simultaneous commutations required, losses increase	above standard range for all load angles	According to base modulation scheme	No increase compared to steady state	Smaller DC link possible	simple, low computational effort
SMC FC (Note 3)	Pure FC operation with doubled commutation voltage and increased losses	NP current is zero	Significantly increased distortion	Significantly increased distortion	Smaller DC link possible	simple, low computational effort

Note 1: The comments on DC link dimensioning only refer to the constraints imposed by NP controllability for a specific modulation scheme. In reality, other constraints may be dominant (e.g. energy for ride through).

Note 2: standard range refers to the physical limitation of the NP current for a 3-L NPC in optimum modulation (without virtual vectors) as introduced in paragraph 4.7.1.2.

Note 3: SMC A, SMC B, and SMC FC have distinctive properties. Best overall performance can be achieved if all three are combined within a given modulation scheme. (See also implementation of hysteresis modulator in chapter 1.)

The choice of topology depends primarily on cost (bill of material and production), size, reliability and performance (availability, efficiency, dynamic performance etc.). However, NP controllability and robust operation are a must, so that the availability of a suitable modulator is crucial.

TABLE 64, APPLICABILITY OF MODULATION AND NP CONTROL SCHEMES

pure 3-L schemes	- all 3-L DC link topologies
FC + SMC schemes	- SMC only
ANPC 1 schemes	- ANPC 1 - backward half bridge ANPC variation, Figure 31 (a) - ANPC 3
ANPC 3 schemes	- ANPC 3 only

The ANPC 1, ANPC 3, and SMC feature very powerful NP controllability as introduced in this thesis. The ANPC 1 control schemes may also be applied to other ANPC variations with a flying capacitor connected directly to the last output half bridge, including the backward half bridge variation and the ANPC 3 as indicated in TABLE 64. The ANPC 2 and its related topologies, as well as all asymmetric topologies do not feature a sufficient level of redundancy to generate modified or virtual vectors, nor carrier based modulation schemes equivalent to those presented in chapter 1. Other schemes with significantly higher output voltage distortion would need to be considered to get the same level of capacitor controllability for those topologies. Such schemes could then also be applied to the topologies shown in Figure 31 (b), (c), (d), and (e) as they are functionally equivalent to the ANPC2.

7.2 Modulators and applications

7.2.1 Active front ends

AFE stands for any application connecting to the power system. The type of power flow may vary. The following are typical representatives of AFE applications.

- Active rectifiers power generation inverters with high modulation index and high cos(φ)
- Reactive power compensation
- Harmonic filtering

Generally, all of the presented modulation and control strategies can be applied. Output waveform harmonics are a key aspect. There are standards (e.g. IEEE 519 and IEC 68100) as well as country and application specific grid codes that define maximum permissible harmonic values for voltage and current. Modulation, control and filters must be designed accordingly. Selective harmonic elimination schemes are one approach to keep harmonics low. Such schemes can also be used in conjunction with the proposed modulation and NP control schemes in this thesis. The pre-calculated pattern serves as input for the subsequent calculation steps. The pattern needs to be split into multiple sections (equivalent to a modulation period, but with non constant time). Then the individual sections may be subjected to CM injection, either DC or 6^{th} harmonic. The injection is preferably with low amplitude to keep the generation of harmonics close the pre-calculated spectrum. A large CM injection can lead to a change of the mode and an alternate type of pattern may need to be applied if available. Online generated patterns (similar as presented by J. Wells [59]) are even more suitable for CM injection as the boundaries of the modulation period are clearly defined by the carriers. DC and 6^{th} harmonic injection can easily be applied.

Over modulation beyond sinusoidal phase to phase voltage is interesting for AFE applications. It will be avoided under normal circumstances to prevent the generation of low order harmonics. However, in exceptional overvoltage conditions on the line, over modulation may prevent tripping of the converter.

Optimal sequence modulators according to paragraph 6.2 are easier to be implemented for line applications, as the number of sequences to be considered is significantly lower for high modulation depth than for low modulation depth. A larger prediction horizon than for low modulation depth may be considered, leading to significantly improved performance.

Reactive power compensation requires reliable operation also in purely reactive operation. The proposed modulation and control schemes significantly improve the NP controllability in reactive power operation compared to standard schemes. Specifically, this is true for high modulation depth where the virtual vector scheme remains effective.

Harmonic filtering requires relatively high control bandwidth, which can be obtained with high switching frequency and suitable control loops for the individual harmonics. This can be done with all proposed concepts except for the optimal sequence modulator according to paragraph 6.2. The output current harmonics generated for compensation may lead DC NP current, which makes this application particularly demanding. Powerful schemes controlling the NP without introducing and DM distortion are required. A hysteresis based NP controller as proposed in paragraph 7.3 is a good approach to get a lot of NP control capacity while keeping good performance regarding DM distortion.

7.2.2 Motor drives

There are at least two fundamentally differing motor control approaches:

1. Direct control of motor quantities by direct application of suitable states. No classical pulse width modulation as such is used, but of course the resulting pulse pattern essentially also is PWM signal. DTC is ABB's preferred approach to motor control. None of the presented NP control schemes can be applied directly to DTC. However, DTC does automatically make use of the full physically controllable range based on the real time NP current function if a proper state selection for NP control is done. This is not true for the modified and virtual vectors. An application of such a combination of states would be pure coincidence. New NP control schemes for DTC can be defined by simply including modified and virtual vectors in the set of possible output vectors. The timing of the partner states of a virtual vector would be tricky as the overall application time of any vector is not known beforehand. DTC can also be tuned to have constant switching frequency (e.g. [108]). Yet other approaches would be required to make use of virtual vector in this case. There is also research work on the implementation of DTC based on MPC done (e.g. [52]). MPC will automatically make use of state combinations like the virtual vectors if the prediction horizon is long enough. However, this is computationally very demanding and has not been presented so far.
2. Vector control schemes or U/f control schemes make use of an approximated output voltage of the converter. Classical modulation schemes can be used for that purpose (SVM, carrier based). Consequently, all of the proposed modulation and NP control schemes are applicable to this kind of motor control.

Motor drives generally have less stringent requirements regarding output waveform harmonics. But in any case, a low distortion is beneficial to keep losses in the machine low, reduce torque ripple and avoid mechanical oscillations in the system.

Bearing degradation due to bearing currents is an important topic in drive systems. A lot can be done by proper bearing design. On the other hand it is clear that low average CM voltage and low CM transients are always beneficial for the drive system. Some of the proposed schemes (e.g. 6^{th} harmonic injection) perform better than others (e.g. virtual vector scheme) in that respects. A hysteresis based control approach can provide both a lot of NP control capacity and low CM voltage operation in steady state.

7.2.3 Back to back configurations

Back to back refers to the connection of two or more converters of the same type to the same DC link. This may be a drive system with active front end, a power generation system with line inverter, a power quality device with multiple connections (e.g. UPFC), a multi-drive system with several motor inverters on the same DC link, etc. NP control in all these systems can either be dedicated to one inverter or shared by several. In the case of sharing the control task, different concepts are possible: Master slave concepts can be use, where one controller is taking care of the task using multiple inverters. Multiple controllers can also work independently, but in this case care has to be taken with stability of the control loops, as multiple controllers may counteract. Regardless of the different possibilities of approaching the control problem, physical limitations do

not change do the back to back topology. The real time NP current function is still valid for the individual inverters and virtual vectors may still be generated on the level of individual converters. All concepts proposed in the frame of this thesis still may be applied. The sharing of the control task has not been investigated in the frame of this thesis. Lee proposes a coupled controller to improve performance [79]. Pou has mad an analysis of the limits of zero NP current operation for back to back system [109]. With a suitable choice of nominal and worst case AFE operating point, this range can be significantly increased even if the load inverter is operating at high modulation depth and large load angle. The analysis has been done for the 3-L NPC with a NTV SVM, but the concept could be extended to a higher number of levels and different modulator types, which could be the subject of future research.

7.2.4 Single phase applications

Single phase systems cannot make use of any of the proposed NP control schemes. However, NP control is relatively straight forward as shown in paragraph 4.7.1.1. The NP current can always be positive or negative independently of modulation depth or load angle.

Single phase applications include for example railway applications, which are usually DC or single phase AC supplied. A particularly important feature of such applications is that reactive power can not be circulated between phases like in multiphase systems and as a result, there is a second harmonic fluctuation in the DC link voltage. This has a significant impact on the dimensioning and control of the DC link capacitors. The required DC link capacitance is typically very large to ensure a maximum voltage ripple. An alternate DC link capacitor control approach has been investigated in the frame of this thesis (documented in [2]): In reactive power compensation applications, the DC link capacitor is allowed to discharge in every half cycle to a very low voltage. This reduces the required capacitive energy and has a positive impact on losses and output voltage THD.

The concept can also be extended to ML topologies. In spite of the inherently good capacitor controllability in single phase systems, the variable DC link operation in ML converters is not straight forward. There are conflicting targets regarding FC dimensioning and control. Flying capacitors should be relatively large to minimize the voltage ripple at the switching frequence; on the other hand they should be small to allow for a dynamic variation of the reference voltage. A in-depth investigation of this topic has not been done in the frame of this thesis. For more information on the proposed variable DC link approach, the reader is referred to [2, 3].

7.3 Hysteresis NP control

Modulators with hysteresis NP control have already been introduced for ANPC 3 and SMC in chapter 1. This paragraph focuses on a suitable controller for the ANPC 1. The hysteresis controllers for ANPC 3 and SMC can be extended accordingly.

TABLE 65, GENERAL REQUIREMENTS FOR HYSTERESIS NP CONTROL

1.	Output voltage distortion shall be determined by an underlying base modulation scheme in steady state (usually an optimum modulation scheme like PD-PWM, offline optimized, SVM etc.)
2.	Switching losses shall be minimized in steady state
3.	All operating points regarding modulation depth and load angle shall be covered
4.	The modulator shall have reasonable complexity to be applicable in an industrial environment
5.	The modulator shall have low computational requirements (online) to allow for high switching frequency and high control bandwidth
6.	The modulator shall be able to cope with different commutation schemes (e.g. hard commutated schemes vs. snubbered schemes
7.	The modulator shall be able to cope with load disturbances like distortion, sag, and unbalance and still keep the NP balanced
8.	For low deviations of the NP voltage, the NP controller shall produce no differential output voltage distortion, keep a low CM ripple and keep low switching losses
9.	For intermediate deviations of the NP voltage, the NP controller may increase the CM ripple, increase switching losses but keep the differential output voltage undistorted
10.	For high deviations of the NP voltage, the NP controller may generate output voltage distortion to keep the converter from tripping

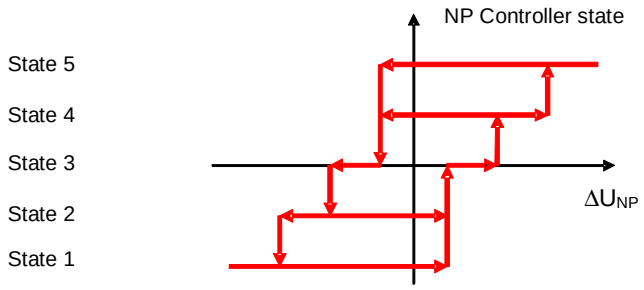


Figure 102, Hysteresis controller structure for NP voltage control

The hysteresis controller depicted in Figure 102 makes use of the controller states indicated in TABLE 66. Note that the boundaries indicated for the modulation depth in TABLE 66 have been determined heuristically. The formulas given are an approximation for a highly non-linear relationship. Fixed boundaries could be used instead, still providing good performance but not making full use of the physical capabilities of the converter.

TABLE 66, MODULATORS FOR HYSTERESIS NP CONTROL IN THE ANPC 1

Controller state	**cos(φ) < 0.15**		**cos(φ) > 0.15**		
	m < 0.5	**m > 0.5**	**m < 0.26 + abs(φ)**	**m > 0.26 + abs(φ) AND m < cos(φ)** (Note 1)	**m > cos(φ)**
State 3: all with low gain	6th harmonic injection	6th harmonic injection	real time NP current function	real time NP current function	real time NP current function
State 2 and 4: all with high gain	real time NP current function	6th harmonic injection	real time NP current function	real time NP current function	real time NP current function
State 1 and 5: with high gain	virtual vector sequences	virtual vector sequences	virtual vector sequences	real time NP current function	virtual vector sequences

Note 1: This condition is not determined analytically, but is just a random approximation of the relationship found by calculation of individual operating points as shown in TABLE 88 in appendix 9.5.4

There is a high degree of freedom for the implementation of the hysteresis controller. Any of the preferred controller configurations according to TABLE 29 and Table 30 or the like can be applied in case of use of the real time NP current function. To get best performance according to the chosen strategy, the control gain should be low in steady state (state 3). Alternatively, even a first tolerance band (state 3) could be defined where no NP control is active at all. The control gain should be high in state 2 and 4, so that maximum NP control capacity (controllers in saturation, CM limited by feasible operating range) is obtained before reaching the threshold for the next control mode.

7.3.1 Interaction of the modulators

All modulators determine switching patterns for a half modulation period at a time. Half periods with rising CM voltage (falling carrier in carrier based schemes) and with falling CM voltage (rising carrier in carrier based systems) alternate. This concept is also kept for the virtual vectors, so that they seamlessly fit with the other modulation schemes. The type of modulator to be used can be determined on a half switching period basis without problems. This results in very dynamic performance without sacrificing the output voltage waveform quality.

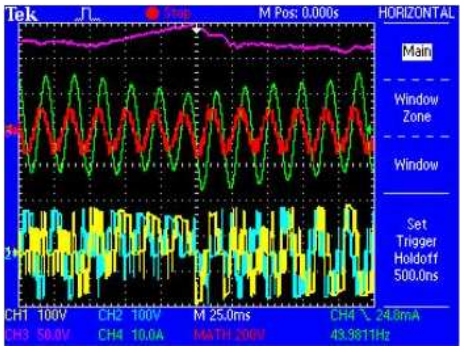
7.4 Experimental verification

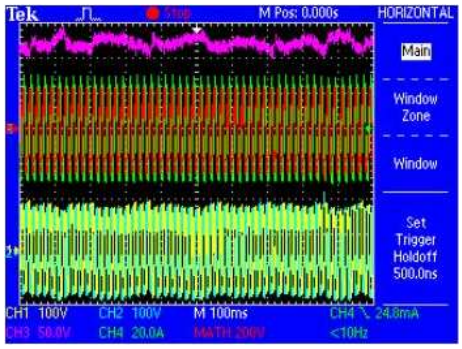
The proposed hysteresis controller has been implemented on the 5-L ANPC low power prototype and its performance has been experimentally verified. Two different operating points shall be shown. In both cases a simplified version of the hysteresis controller is applied. In steady state, a first NP control type is applied; when hitting the tolerance band, a second NP control type is applied until the NP voltage reaches the reference value again.

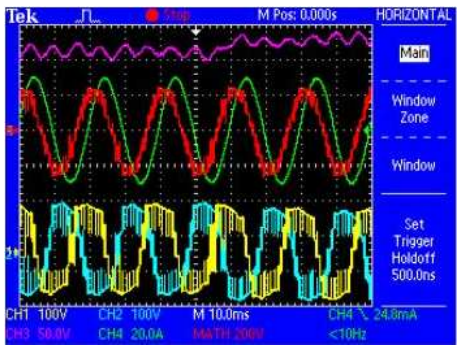
TABLE 67, COMMON PARAMETERS FOR THE EXPERIMENTAL VERIFICATION OF THE NP VOLTAGE HYSTERESIS CONTROLLER (TWO STATE OPERATION)

f_{load}	U_{DC}	U_{NP_ref}	Tolerance band	base modulation type	L_{load}	R_{load}
50Hz	240V	120V	+/-30V	CPDPWM	14.2 mH	0 Ω

TABLE 68, PERFORMANCE OF THE HYSTERESIS CONTROLLER FOR MEDIUM MODULATION DEPTH (M=0.5) AND OVER MODULATION FOR PURE REACTIVE POWER

m = 0.5, cos(φ) = 0
Hysteresis controller:
- NP control type 1:
  - unconstrained DC CM injection
- NP control type 2:
  - 6th harmonic injection
		CH1 (yellow): U_{out1}
		CH2 (cyan): U_{out2}
		CH3 (magenta): U_{NP}
		CH4 (green): I_{out2}
		MATH (red): U_{out1-2}
		Time/div: 25ms

m = 1.1 (over modulation), cos(φ) = 0
Hysteresis controller:
- NP control type 1:
  - real time NP current function
- NP control type 2:
  - virtual vectors
		CH1 (yellow): U_{out1}
		CH2 (cyan): U_{out2}
		CH3 (magenta): U_{NP}
		CH4 (green): I_{out2}
		MATH (red): U_{out1-2}
		Time/div: 100ms

m = 1.1 (over modulation), cos(φ) = 0
Hysteresis controller:
- NP control type 1:
  - real time NP current function
- NP control type 2:
  - virtual vectors
		CH1 (yellow): U_{out1}
		CH2 (cyan): U_{out2}
		CH3 (magenta): U_{NP}
		CH4 (green): I_{out2}
		MATH (red): U_{out1-2}
		Time/div: 10ms

The controller based on unconstrained DC injection cannot keep the NP voltage balanced even at m=0.5. The maximum DC CM injection is visible in the phase voltages while the NP voltage is diverging. When the tolerance band is hit (150V), the 6th harmonic injection scheme brings the voltage back to its set point in one fundamental cycle (TABLE 68, a). In over modulation (m=1.1), the NP voltage cannot be controlled by any of the standard controllers (real time current function used in this case). The NP voltage is drifting away until it hits the tolerance band, then virtual vector operation brings the NP voltage back to its reference. The zoom shows nicely how the NP voltage (purple) can be brought back to its set point within a fraction of a cycle. The virtual vectors type 2 can be recognized both in the line to neutral voltages (cyan and yellow) and in the line to line voltage (red) as double level steps. The distortion introduced is not very significant and hardly visible in the current (green). A significant 3rd harmonic is imposed on the NP voltage in this operating point.

7.4.1.1 Active power

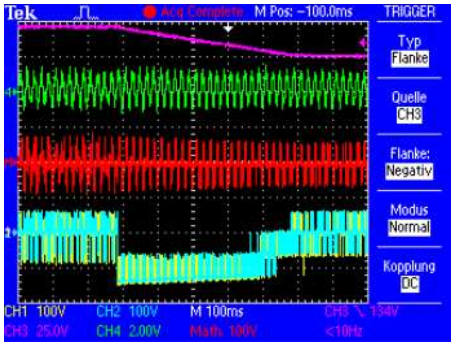
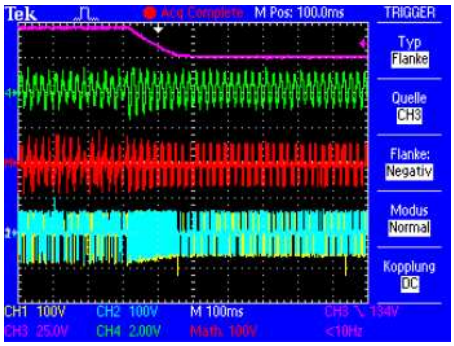
The unconstrained DC CM voltage injection works reliably throughout the linear operating range of the 5-L ANPC. However, its useful NP current range for control depends heavily on the modulation depth. The available current range start from zero for m=0, rises up to a maximum for m=0.5 and then is reduced again to zero for maximum over modulation. Improved NP control concepts are therefore of primary interest for the very high and very low modulation depth (see also TABLE 88 in appendix 9.5.4 and the resulting condition for the application of virtual vectors in TABLE 66). The following experimental results underline the usefulness of alternate schemes in those operating points.

TABLE 69, COMMON PARAMETERS FOR THE EXPERIMENTAL VERIFICATION OF A NP VOLTAGE REFERENCE STEP WITH ACTIVE POWER LOAD

f_{load}	U_{DC}	U_{NP_ref} initial	U_{NP_ref} end	base modulation type	L_{load}	R_{load}
100Hz	240V	140V	120V	CPDPWM	4.2 mH	12 Ω

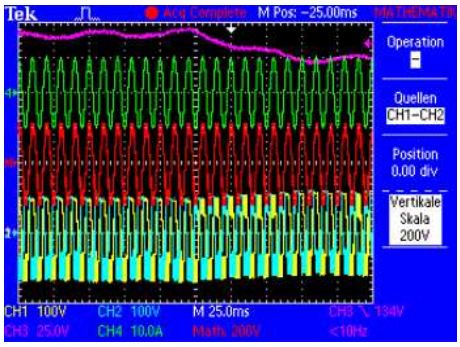
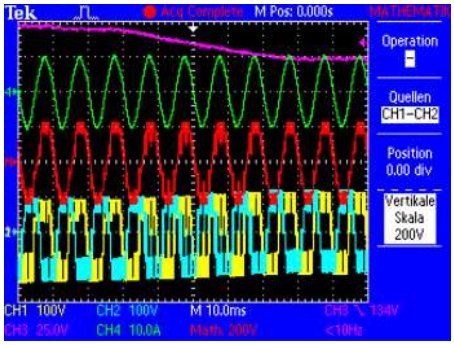
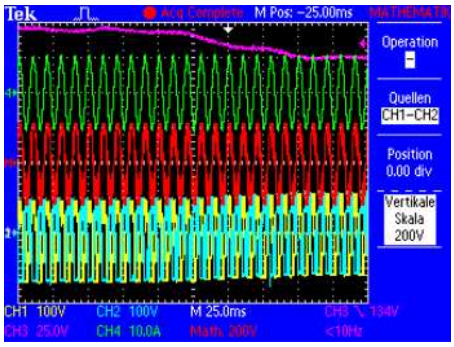
Unconstrained DC CM injection and use of the real time NP current function yield the same performance regarding NP control in active power operation. They both result in a dv/dt of 40V/s in the NP voltage. The corresponding NP current is 160 mA ($C_{effective}$ = 4 mF) which is equivalent to 14% of the peak phase current of 1.15A. The scheme applying modified vectors is significantly more powerful with a dv/dt of 160V/s and a NP current of 640mA (55% of the peak phase current). These values correspond with the calculated data; at even lower modulation depth, the modified vectors will still make use of 50% of the phase current, whereas in the other schemes, the percentage will go down to zero. Note the voltage waveforms in TABLE 70: Unconstrained DC CM injection makes use of a DC CM injection clearly visible in the phase voltages, whereas the modified vector scheme introduces 2 level commutations but no CM offset. In all schemes, the differential output voltage remains undistorted. The distortion seen in the graphs is based on the large NP unbalance and not on the pulse pattern. The same is true for the current transient, which is more prominent for the modified vector scheme, as the NP voltage transient is much faster (Note that the system is operating in open loop and does not actively control the output currents).

TABLE 70, PERFORMANCE OF THE INDIVIDUAL NP CONTROL SCHEMES AT ACTIVE POWER OPERATION AND LOW MODULATION DEPTH (m = 0.1)

Unconstrained DC CM injection - m = 0.1		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 100ms
Modified and virtual vectors - m = 0.1		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 100ms

The operating point of very high modulation depth is even more critical than the operation at low modulation depth. At high modulation depth, typically load currents are higher and distortion my produce significant NP bias currents that need to be compensated. This is especially true for line connected applications, where exceptional line conditions may be very demanding. TABLE 71 shows experimental results for very high modulation depth and different NP control schemes. Unconstrained DC CM injection is capable of controlling the NP voltage up to maximum sinusoidal line to line voltage. However, even without line distortion or any other source of NP bias current, there is a low frequency ripple apparent on the NP voltage, indicating that the controller is operating at its limits and cannot compensate the full NP current. The transient has a duration of ~80ms corresponding with an average dv/dt of 250V/s. The corresponding NP current is 1A or 8.5% of 11.5A peak phase current. With the modified and virtual vector scheme, the NP voltage is significantly more stable and the transient has a duration of 50ms (400V/s). This corresponds with 1.6A NP current or 14% of the peak phase current. The difference is significant, but it may not justify the use of the more complicated scheme, introducing distortion in the line to line voltage (nicely visible in TABLE 71 b, red waveform during transient). However, the unconstrained DC CM injection does not work anymore for maximum over modulation (NP voltage diverging in experimental verification), whereas the modified and virtual vector scheme keeps its properties also in this operating mode. TABLE 71 I shows maximum trapezoidal operation still yielding a NP voltage dv/dt of 250V/s or 1A NP current (8% of peak phase current). A hysteresis controller as introduced in the previous paragraph can make best use of that control power and the good performance regarding switching losses and output harmonics of the other modulators.

TABLE 71, PERFORMANCE OF THE INDIVIDUAL NP CONTROL SCHEMES AT ACTIVE POWER OPERATION AND HIGH MODULATION DEPTH (M = 1 AND OVER MODULATION)

Unconstrained DC CM injection - m = 1 (maximum sinusoidal line to line voltage		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 25ms
Modified and virtual vectors - m = 1 (maximum sinusoidal line to line voltage)		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 10ms
Modified and virtual vectors - maximum over modulation (trapezoidal line to line voltage)		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 10ms

It has also been experimentally verified that DC CM injection (constrained or unconstrained) yields better results than the modified and virtual vector scheme for medium modulation depth and pure active power. Therefore a flexible choice of modulation type according to TABLE 66 is required for best performance.

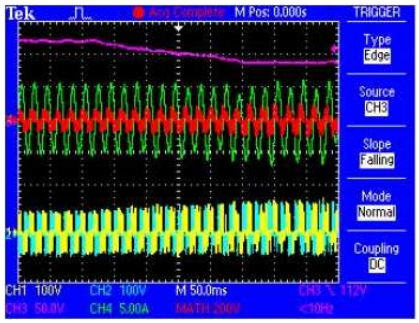
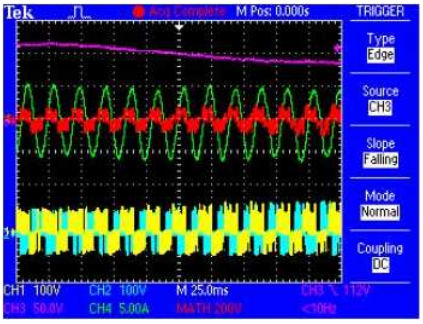
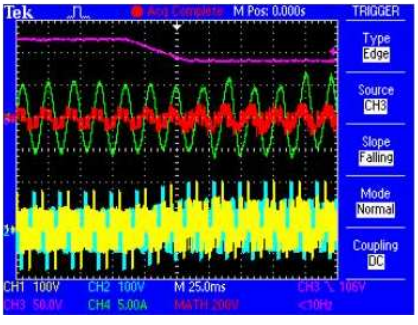
7.4.1.2 Reactive power

The performance of the different controllers has been compared at reactive power operation both for high and low modulation depth. Like in the case for active power, the performance is demonstrated by a step response for the NP voltage. In this case a step away from the balanced case is chosen, to have balanced operation in the beginning of the transient.

TABLE 72, COMMON PARAMETERS FOR THE EXPERIMENTAL VERIFICATION OF A NP VOLTAGE REFERENCE STEP WITH ACTIVE POWER LOAD

f_{load}	U_{DC}	U_{NP_ref} initial	U_{NP_ref} end	base modulation type	L_{load}	R_{load}
50Hz	240V	120V	90V	CPDPWM	14.2 mH	0 Ω

TABLE 73, PERFORMANCE OF THE INDIVIDUAL NP CONTROL SCHEMES AT REACTIVE POWER OPERATION AND LOW MODULATION DEPTH (M = 0.2)

Unconstrained DC CM injection (Note different time base in this recording)		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 50ms
Real time NP current function (constrained DC CM injection)		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 25ms
Modified and virtual vectors		CH1 (yellow): U_{out1} CH2 (cyan): U_{out2} CH3 (magenta): U_{NP} CH4 (green): I_{out2} MATH (red): U_{out1-2} Time/div: 25ms

The unconstrained DC CM injection achieves a dv/dt of 130V/s in the NP voltage. This corresponds with a current of 530 mA ($C_{effective}$ = 4 mF). This is 10% of the phase peak current of 5.3 A in this operating point. The unconstrained DC CM injection controller relies on a minimum of active current to operate, in the case of pure reactive power; it could not control the NP voltage at all. The stated value could be obtained by coincidence and cannot be relied on. Application of the real time NP current function on the other hand makes systematic use of the peak currents available for the NP, independently of the active part of the current. The result is a dv/dt of 200V/s. This corresponds with a current of 800mA or 15% of the phase peak current, which is above the values expected from simulation (~10%, see Figure 68). This mismatch can be attributed to the ohmic part of the load (copper and magnetic losses, forward voltage drop in semiconductors) in the setup, which helps increasing the peak NP current. Also the measurements with the oscilloscope are not very precise, so that the match can be considered sufficiently well.

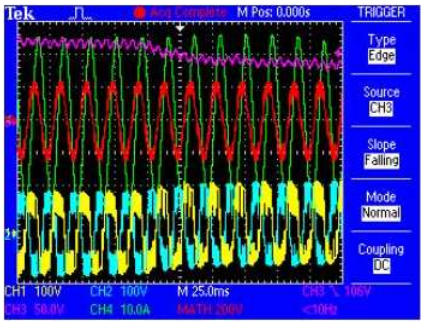
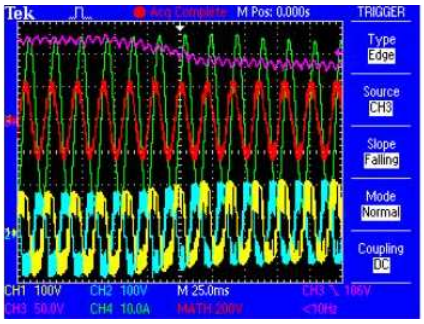
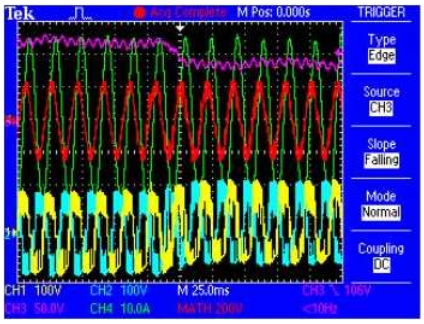
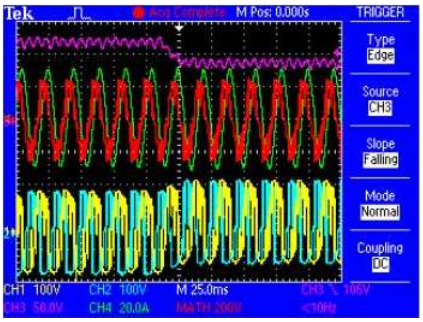
The use of modified vectors allows for 30V / 50ms equal to 600V / s. This corresponds with a current of 2.4A or 45% of the phase peak current. This is a value, which is not expected in reality and the controller can be considered very powerful and reliable. Note that the modified vectors applied at low modulation depth generate CM step visible in the individual line-neutral voltages (yellow, cyan) but do not generate any distortion in the line to line voltages. The current thus keeps the same THD as with the other NP controllers. The unbalance that can be observed in the current of the figure in TABLE 73 ([a] and [c], green) is caused by the NP voltage step (open loop operation).

TABLE 74 does not contain results with unconstrained DC CM injection, because this type of controller was not able to stabilize the NP in the experiment. This has been expected from theory and simulation and underlines that unconstrained DC CM injection should not be used in reactive power operation at any modulation depth. The real time NP current function and the 6th harmonic injection are very much equivalent, resulting in a dv/dt of 600V/s. The resulting 2.4A correspond with 8.5% of the 28A phase peak current. The calculated values shown in Figure 68 indicate a maximum NP current of around 7%, which is a good match.

The use of vector sequences with virtual vectors type 2 reduces the duration of the transient to 20ms. The resulting 6A of NP current are 21% of the phase peak current, which is less than at low modulation depth but significantly more powerful than any other control concept available. Note that the virtual vectors are only applied during the transient and the real time NP current scheme is used in steady state. This is also visible in TABLE 74 I both in line to neutral and line to line voltages. When going to over modulation (m>1), real time NP current scheme and 6th harmonic injection do not provide sufficient NP current range to keep the system stable due to the very small range of CM injection that can be used in this mode. The virtual vectors type 2 on the other hand are available even for full trapezoidal modulation. The virtual vector NP controller remains very powerful with an experimental maximum of 21% NP current injection as can be seen from TABLE 74 (d).

It can be concluded that the three proposed NP control schemes and modulators are very powerful, in fact even essential for the reliable operation of the 5-L ANPC type 1 in pure reactive power operation. Where 6th harmonic injection and the real time NP current scheme have equivalent performance as some SVM schemes proposed in literature, the virtual vectors extend the available NP current range significantly and allow for more robust operation.

TABLE 74, PERFORMANCE OF THE INDIVIDUAL NP CONTROL SCHEMES AT REACTIVE POWER OPERATION AND HIGH MODULATION DEPTH

<table>
<tr>
<td>Simulation (TABLE 40):
 
Measurement:
 
(a) Real time current function, m=0.9</td>
<td>Simulation (TABLE 40):
 
Measurement:
 
(b) 6th harmonic injection, m=0.9</td>
</tr>
<tr>
<td> 
(c) Virtual vectors, m=0.9</td>
<td> 
(d) Virtual vectors, m= 1.15 (full trapezoidal modulation)</td>
</tr>
</table>

Legend: CH1 (yellow): U_{out1}, CH2 (cyan): U_{out2}, CH3 (magenta): U_{NP}, CH4 (green): I_{out2}, MATH (red): U_{out1-2}, 25ms/div

7.4.1.3 Distorted load, harmonic compensation

An important aspect of distorted and unbalanced systems is the generation of DC NP currents and NP current harmonics. As can be seen from TABLE 27 and TABLE 28, the relationship between line currents, switching function, and resulting NP current is quite complex. It can be assumed that in heavily distorted system, the NP current is practically unpredictable and it possibly contains a significant DC component. A good NP control scheme is therefore required especially in such rough operating conditions.

The 6th harmonic injection scheme relies on relatively balanced currents. The concept does not work properly anymore if the currents are heavily unbalanced or contain a DC component. The real time NP current scheme does not make use of any three phase information like load angle, or transformed dq (direct-quadrature) values. It is using the instantaneous current values and applies a CM function totally independent from past and future of the load current. Therefore, the controller still operates reliably with unbalance or distorted load currents, provided the controller has a bandwidth high enough cope with the dynamics in the disturbed system. The same statements as for the real time NP current scheme apply to the virtual vector modulation schemes. The most

suitable sequence is chosen in every modulation cycle based on the instantaneous currents. The controller maintains its superior performance also for heavily unbalanced or distorted currents.

As a consequence, the 6th harmonic injection scheme is best applied within a hysteresis controller including also the real time NP current scheme or the virtual vector scheme, to make sure the system performs as it should also under unbalanced and distorted conditions.

7.5 Executive summary for chapter 7

The general capabilities of the modulators introduced in the previous chapters are summarized and suitable topologies fitting the modulator schemes are listed. There is no single modulation scheme providing best performance regarding all criteria and in all operating points. In fact some of the modulation schemes nicely complement each other. A hysteresis control approach is proposed to make best use of all the available modulation schemes.

The choice of modulators to be used within a hysteresis controller depends also on the application. Different basic applications are given and the suitability of the individual modulation schemes is evaluated.

Experimental results show the functionality of those controllers. The limitations of some modulation schemes are also demonstrated. In a given operating point (reactive power at high modulation depth), unconstrained DC CM injection cannot control the NP, the NP voltage drifts away to the next threshold, where 6^{th} harmonic injection is applied. The voltage is brought back to the set point. When going to trapezoidal over modulation, the real time NP current scheme does not work anymore, the NP voltage rise until it hits the threshold and the virtual vectors bring the NP voltage back to its set point.

The NP control performance is compared for the different modulation schemes in various operating points by applying a step function in the NP voltage reference. The resulting step response is a very good measure for the NP control capacity. The performance of all the modulators could be verified for the crucial operating points. The virtual vector sequences show best NP voltage control as expected for

- reactive power at any modulation depth
- low modulation depth at any load angle
- high modulation depth at any load angle

Seamless operation of all considered modulators is highly crucial for the application of a hysteresis controller. This is also demonstrated experimantelly and smooth transitions between different modulation schemes can be observed.

8 CONCLUSIONS AND OUTLOOK

8.1 Conclusions

Cost effective and solutions for MV ML converters with wide operating range and robust operation are required in industry. This asks for topologies with low requirements regarding total silicon area and passive components energy. Suitable control schemes need to be available to operate any converter in a robust way. This means that internal quantities like the capacitor voltages need to remain controllable in all operating points of the target application.

Control of converter capacitors is closely linked to converter modulation. Any converter topology needs to be evaluated regarding the availability of suitable modulation schemes making best use of the hardware. This thesis has addressed ML topologies and modulation schemes in order to provide good solutions for a wide range of applications. New topologies and new modulation schemes are proposed.

8.1.1 Topologies

A generic framework for the analysis and synthesis of ML converter topologies has been introduced. It has been shown that all major ML topologies used today fit in that generic framework. Based on the framework, a systematic approach for the invention of new topologies has been introduced. Two patent applications have been filed based on this approach. A few examples of new 5-L topologies are presented (Figure 31). Many more topologies are possible for higher level converter. The new topologies have been analyzed regarding controllability and they can be put in several categories referring to ANPC and SMC, so that not all need to be included in a comparison.

All major topologies (limited to single supply topologies) have been compared based on multiple criteria, focusing mainly on resource requirements (silicon area and passive components energy rating) and scalability.

- Some topologies have bad scaling properties and / or bad loss distribution based for example on the number of parallel paths (e.g. MLDC)
- Some topologies scale nicely but require a lot of resources (e.g. M²LC)
- The choice of topology is highly application dependent
    - The M²LC is of primary interest for HV constant frequency applications (power system applications), as it scales very good with increasing number of levels and increasing DC voltage.
    - The 3-L DC link family is very attractive for MV applications, as it offers a very good compromise between resource requirements and controllability

The 3-L DC link ML converter family has been chosen for more in-depth investigation in this thesis; this includes the 5-L ANPC 1, which is the primary topology of interest in this work.

8.1.2 Modulation and control

The two main degrees of freedom for NP and FC control are CM voltage and redundant states, which can be used to control capacitor currents. All considered topologies have redundant states generating opposite sign currents of the same amplitude in the flying capacitors. It is therefore possible to balance the flying capacitors within each modulation period purely by choice of redundant states. This standard approach splits the control problem. Once the simple FC control scheme acting on the flying capacitors, the remaining control problem is reduced to a pure NP balancing problem with a single quantity to be controlled. A thorough analysis of the NP characteristics is done in first step. The NP current is a time variant piecewise function of CM voltage. The key findings associated with the NP current as a function of CM voltage are:

1. The function is the same for all 3-L DC link topologies in case standard modulation schemes with decoupled flying capacitor control are used.
2. The function has a limited useful range; the outer pieces always have zero gradients and thus no impact on the NP current.
3. The function may be non monotonic in reactive power operation.
4. The standard NPC schemes can be used for any 3-L DC link topology
5. Most higher level 3-L DC link topologies offer a higher degree of freedom and are not constrained by the limitations that have been reported for the NPC regarding NP control.

This allows for the implementation of modulation and control schemes for any 3-L DC link topology according to the proven state of the art, while keeping the door open for better performance. For example a hysteresis controller can make use of multiple modulation schemes, which may include a standard NPC scheme, and a specific, more powerful ML modulation and control scheme of a new kind.

The higher level of redundancy of many 3-L DC link ML converters (5-L and above) allow for higher NP control capacity. This is important, as it indicates that the use of a higher level converter does not compromise the operational robustness of the converter, but in fact can improve the robustness from control point of view. (Robustness from a purely electrical point of view, e.g. sensitivity of components to over voltages, is a reliability issues and has not been discussed at all in this thesis.) Tripping of the converter due to deviations of DC link or FC voltages can be reduced.

TABLE 75, NP CONTROL SCHEMES PROPOSED IN THIS THESIS

	Carrier based PWM	**Optimized sequence SVM**
Applicable to any 3-L DC link topology	- Real-time NP current scheme - 6th harmonic injection	Online sequence optimization
Topology specific	ANPC 3 and SMC specific schemes	Virtual vectors for ANPC 1, can be adapted to other topologies

The specific NP control schemes introduced in this thesis all aim at keeping optimum modulation (no DM distortion) as far as possible. Some of the schemes allow going beyond to further increase NP current control capacity.

1. Carrier based real-time NP current scheme offer good performance with reduced CM excursions. 6th harmonic injection is an alternative with similar performance. Peak performance corresponds with other published schemes (due to the same physical limitations)
2. ANPC 3 and SMC schemes allow for NP current control capacity beyond the NPC limits throughout the whole operating range (modulation depth and load angle). This leads to significantly improved NP control capacity. The proposed schemes do not introduce DM distortion and The NP control can act largely independent from CM voltage. This has been demonstrated both in simulation and experiment.
3. Modified and virtual vectors make very systematic use of redundant states. A scheme using predetermined sequences is formulated for the ANPC 1. Similar schemes would be possible for other topologies with common flying capacitors. This scheme keeps optimum modulation up to medium modulation depth and introduces some DM distortion at high modulation depth. The NP current control capacity is significantly increased even up to over modulation region, including pure trapezoidal modulation. This is a very powerful scheme, which could be demonstrated in simulation and experiment
4. Online sequence optimization by optimal control schemes offers a lot of opportunities: control of multiple variables at the time, flexible tuning of objectives. However, high performance can only be reached, if the prediction horizon is large enough. This is computationally very demanding and the control problem is likely to be too complex for converters with many levels (around 5 levels and above). Only a simplified version with limited performance could be demonstrated experimentally. However, simulation with a more complex approach shows promising results.

A combination of the schemes under point 1 and point 3 within a hysteresis controller is proposed. The multiple schemes interact smoothly and the system can be tuned for good steady state performance as well as good dynamic response in transient operation. Such an approach is clearly delivering much higher NP control performance then what is possible with the NPC. At the same time, there are opportunities to optimize switching losses or output voltage harmonics. The schemes are applicable in an industrial environment, as has been demonstrated in the experimental verification, where an industrial PE control platform has been used. The results experimentally obtained correspond fully with the expectations from simulation.

All the proposed simulation and control schemes have a good performance throughout the full operating range regarding modulation depth and load angle. The 3-L DC link topologies are thus a good option for any kind of MV application. More specifically the ANPC 1, ANPC 3 and the SMC offer very good NP controllability, making them good candidates for industrial MV converters.

8.2 Outlook

None of the new topologies have been implemented in hardware, as the NP and FC control problems are the same as with the ANPC topologies and hardware implementation issues have not been in the focus of this thesis. However, if any of the new topologies should be chosen for implementation, PE design issues will need to be investigated. Namely the commutation properties differ a lot from any of the main topologies presented in this thesis. Different protection schemes would need to be developped.

All the proposed modulation schemes have been tested with passive loads on low power prototypes. This is regarded sufficient as proof of concept and qualitatively indicates that the schemes will also perform in real applications under severe operating conditions (unbalance, distortions). However, for quantitative statements on the performance under special operating conditions, the experiments would need to be continued under more realistic load conditions.

The last modulation scheme proposed optimizes PWM sequences online. This is clearly an area with a lot of potential. An MPC based optimal sequence approach can theoretically provide the same or even higher NP current control capacity than the virtual vectors. However, this is only possible if the prediction horizon is long enough and the suitable sequences are even considered. This could not be fully explored and demonstrated within the frame of this thesis. MPC is a logical candidate for the modulation and control of ML converters as there is a large number of redundant states and multiple quantities need to be controlled; ther is a lot of room for optimization. A powerful demonstration of MPC in PE has already been given in [52] where DTC has been improved for the NPC. However, the number of states in a ML converter scales essentially with a cubic function of the number of levels. Also the number of quantities to be controlled is rising with the number of levels. Therefore, the computational hurdles are high. Another hurdle may be the fact that ML converters allow generally for higher apparent output switching frequency than lower level converters, as more cells can be operated in interleaved mode. The calculation time at disposition gets shorter. However, with future control hardware platforms and sophisticated implementation of the control algorithm (e.g. on an FPGA), much more will be possible than today.

Other possible topics of continuation are:

1. Integration of findings regarding modified and virtual vectors directly in a 5-L MPDCT (model predictive direct torque control) scheme.
2. Integrate the proposed schemes with line current harmonic injection schemes for NP control [91]
3. Some operating points generate a minimum low frequency ripple in the NP based on physical constraints. A prediction of this minimum ripple and an accordingly modified NP voltage reference could improve overall performance
4. Back to back configurations offer additional opportunities for NP control. Not only can both converters contribute to the control task, they could even be linked such that new types of virtual vectors using both input and output converter could be defined.
5. The special application of harmonic filtering has special requirements as the harmonic currents may be dominant over the fundamental. The harmonic relationships presented in chapter 4 are not valid anymore. This questions at least the 6^{th} harmonic injection scheme.

A more thorough analysis of the NP current as a function of the line harmonics would be of high interest.

6. For the case of online optimized PWM sequences, the concept of the HFT (harmonic flux trajectory) could be applied to get a true online WTHD optimization. This is of interest specifically for very low switching frequencies (or converters with a high number of levels) where PD PWM does not yield best performance anymore and typically optimized pulse patterns would be applied.
7. CM injection schemes could be combined with the CB PWM schemes making use of redundant states according to chapter 5.3. All possible NP current functions can be pre-calculated, exploring all possible combinations of different modulation types. The choice of modulation type may be based on any desired criteria.

8.3 Summary of original contributions

- A generic framework for ML representation, analysis and synthesis has been introduced.
    - It has been shown that most converters according to the state of the art fit in that framework
    - New 3-L DC link topologies have been invented based on that framework.
- A large set of ML converters has been compared regarding a set of criteria including.
    - Switch requirements including scaling laws
    - Flying capacitor energy requirements including scaling laws
- Properties of 3-L DC link topologies have been investigated.
    - Exploration of redundant states and introduction of the virtual vectors of the 5-L ANPC
    - NP current representation as a function of CM voltage and θ, giving insight to the NP current characteristics and supporting the definition of new control schemes
- New modulation and control schemes have been introduced
    - Real-time NP current scheme and 6^{th} harmonic injection suitable for all 3-L DC link topologies including the NPC
    - Specific CB PWM schemes making use of redundant state for the ANPC 3 and the SMC with significant improvement of the NP current control capacity
    - Virtual vector sequence modulation for the ANPC 1 with significant improvement of the NP current control capacity
        - Exploration of the range of existence of modified and virtual vectors
    - Online optimal sequence modulation allowing for reduced switching losses coupled with good output harmonic performance
- Application of multiple schemes within hysteresis NP controllers
- Performance comparison of the different modulation and control schemes

9 APPENDIX

9.1 M²LC capacitor calculations

The steady state operation of the M²LC can be described with the following set of equations. Index 1 is referring to the lower arm, index 2 to the upper arm (Figure 27 a). Note that equations (84) to (103) use capital letters for short term average values (average per modulation period).

$$\alpha_1 = 0.5 + 0.5 * ref_{out} \tag{84}$$

$$U_1 = (\alpha_1 - 0.5) * U_{DC} \tag{85}$$

$$\alpha_2 = 0.5 - 0.5 * ref_{out} = 1 - \alpha_1 \tag{86}$$

$$U_2 = \frac{U_{DC}}{2} - \alpha_2 * U_{DC} = \frac{U_{DC}}{2} - (1 - \alpha_1) * U_{DC} = (\alpha_1 - 0.5) * U_{DC} \tag{87}$$

For a given output current (I_{out}), branch currents (I_1, I_2), capacitor currents (I_{C1}, I_{C2}) and bypass currents (I_{BP1}, I_{BP2}) can be calculated.

$$I_{C1} = \alpha_1 * I_1 \tag{88}$$

$$I_{BP1} = (1 - \alpha_1) * I_1 \tag{89}$$

$$I_{C2} = \alpha_2 * I_2 = (1 - \alpha_1) * I_2 \tag{90}$$

$$I_{BP2} = (1 - \alpha_2) * I_2 = \alpha_1 * I_2 \tag{91}$$

These equations can be rearranged and combined such that the branch currents and the average capacitor currents can be expressed with the output current directly.

$$I_{C1} = \alpha_1 * I_1 = I_{C2} = (1 - \alpha_1) * I_2 \tag{92}$$

$$I_2 = \frac{\alpha_1}{(1 - \alpha_1)} * I_1 \tag{93}$$

$$I_1 + I_2 = I_{out} \tag{94}$$

$$I_{out} - I_1 = \frac{\alpha_1}{(1 - \alpha_1)} * I_1 \tag{95}$$

Branch currents, average capacitor currents and average bypass currents in function of the output current:

$$I_1 = (1 - \alpha_1) I_{out} \tag{96}$$

$$I_2 = \alpha_1 I_{out} \tag{97}$$

$$I_{C1} = \alpha_1 (1 - \alpha_1) I_{out} \tag{98}$$

$$I_{C2} = \alpha_1(1-\alpha_1)I_{out} \tag{99}$$

$$I_{BP1} = (1-\alpha_1)^2 I_{out} \tag{100}$$

$$I_{BP2} = \alpha_1^{\,2} I_{out} \tag{101}$$

The average capacitor current is a function of the duty cycle α and I_{out}.

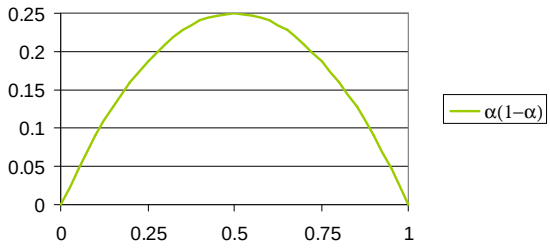


Figure 103, average capacitor current in function of duty cycle α

According to Figure 103 , the maximum average current in the flying capacitor is obtained with α=0.5. The worst case for the flying capacitor low frequency ripple is therefore given for zero output voltage (ref_{out} = 0 resulting in α=0.5) with maximum AC current. In this case, all capacitors see one fourth of the output current at fundamental frequency (Figure 104 a).

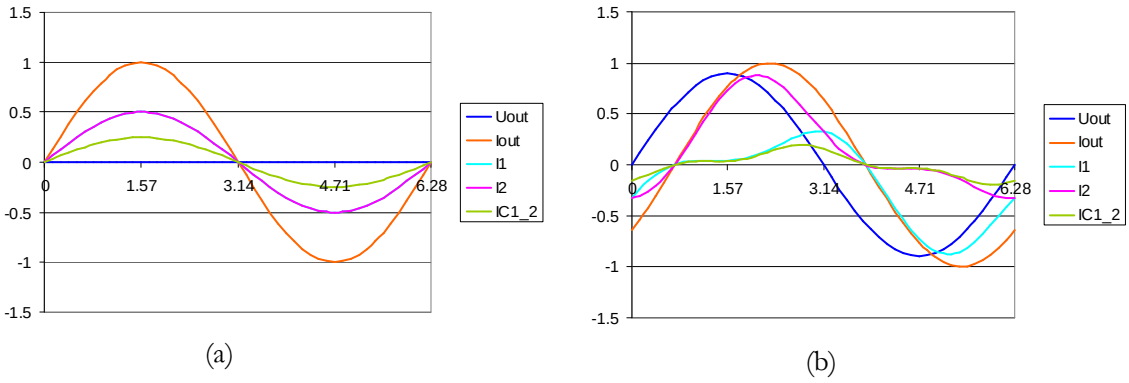


Figure 104, M2LC voltages and current in two operating points: m = 0, phi =0 and m = 0.9, phi = 0.7

The flying capacitor voltage can be calculated based on the given current characteristic. In the case of the sinusoidal current or U_{out} = 0 we get:

$$I_{cap} = \frac{I_{out}}{4} = \omega C U_{cap\_ac} \tag{102}$$

$$C = \frac{\hat{I}_{out}}{4\omega\hat{U}_{cap\_ac}} \tag{103}$$

These equations can directly be used for the dimensioning of the M²LC module capacitors (or flying capacitors) for a given maximum voltage ripple.

9.2 Flying capacitor energy tables

9.2.1 MC based topologies

TABLE 76, FLYING CAPACITOR ENERGY CONSTATNT WITH PEAK DEVICE SWITCHING FREQUENCY LIMITATION

	MC	**SMC**	**ANPC 1** **SCx+FCx**	**ANPC 2** **FCx+SCx**	**ANPC 3** **FCx+FCx**	**FSx+FCx**	**FC2 * x**
$\mathbf{k_{f\_sw}}$	1	1	1	1	1	1	1
$\mathbf{F_{sw\_out}}$	$N * f_{sw\_max}$	$N / 2 * f_{sw\_max}$	$N / 2 * f_{sw\_max}$	$N / 2 * f_{sw\_max}$	$N * f_{sw\_max}$	$N * f_{sw\_max}$	$N * f_{sw\_max}$
$\mathbf{K_{E\_cap}}$ **(N=2)**	0.25	0.00	0.00	0.00	0.00	0.00	0.25
$\mathbf{K_{E\_cap}}$ **(N=4)**	0.88	0.25	0.13	0.25	0.19	0.06	0.19
$\mathbf{K_{E\_cap}}$ **(N=6)**	1.53	0.56	0.28	0.56	0.42	0.14	0.17
$\mathbf{K_{E\_cap}}$ **(N=8)**	2.19	0.88	0.44	0.88	0.66	0.22	0.16
$\mathbf{K_{E\_cap}}$ **(N=10)**	2.85	1.20	0.60	1.20	0.90	0.30	0.15

TABLE 77, FLYING CAPACITOR ENERGY CONSTANT WITH AVERAGE DEVICE SWITCHING FREQUENCY LIMITATION

	MC	**SMC**	**ANPC 1** **SCx+FCx**	**ANPC 2** **FCx+SCx**	**ANPC 3** **FCx+FCx**	**FSx+FCx**	**FC2 * x**
$\mathbf{k_{f\_sw}}$	1	2	1	2	1	1	1
$\mathbf{F_{sw\_out}}$	$N * f_{sw\_avg}$	$N * f_{sw\_avg}$	$N / 2 * f_{sw\_avg}$	$N * f_{sw\_avg}$	$N * f_{sw\_avg}$	$N * f_{sw\_avg}$	$N * f_{sw\_avg}$
$\mathbf{K_{E\_cap}}$ **(N=2)**	0.25	0.00	0.00	0.00	0.00	0.00	0.25
$\mathbf{K_{E\_cap}}$ **(N=4)**	0.88	0.13	0.13	0.13	0.19	0.06	0.19
$\mathbf{K_{E\_cap}}$ **(N=6)**	1.53	0.28	0.28	0.28	0.42	0.14	0.17
$\mathbf{K_{E\_cap}}$ **(N=8)**	2.19	0.44	0.44	0.44	0.66	0.22	0.16
$\mathbf{K_{E\_cap}}$ **(N=10)**	2.85	0.60	0.60	0.60	0.90	0.30	0.15

TABLE 78, FLYING CAPACITOR ENERGY CONSTANT WITH APPARENT OUTPUT SWITCHING FREQUENCY LIMITATION (SCALING WITH N)

	MC	**SMC**	**ANPC 1** **SCx+FCx**	**ANPC 2** **FCx+SCx**	**ANPC 3** **FCx+FCx**	**FSx+FCx**	**FC2 * x**
$\mathbf{F_{sw\_out}}$	$F_{sw\_base} * N$	$F_{sw\_base} * N$	$F_{sw\_base} * N$	$F_{sw\_base} * N$	$F_{sw\_base} * N$	$F_{sw\_base} * N$	$F_{sw\_base} * N$
$\mathbf{K_{E\_cap}}$ **(N=2)**	0.25	0.00	0.00	0.00	0.00	0.00	0.25
$\mathbf{K_{E\_cap}}$ **(N=4)**	0.88	0.13	0.06	0.13	0.19	0.06	0.19
$\mathbf{K_{E\_cap}}$ **(N=6)**	1.53	0.28	0.14	0.28	0.42	0.14	0.17
$\mathbf{K_{E\_cap}}$ **(N=8)**	2.19	0.44	0.22	0.44	0.66	0.22	0.16
$\mathbf{K_{E\_cap}}$ **(N=10)**	2.85	0.60	0.30	0.60	0.90	0.30	0.15

TABLE 79, FLYING CAPACITOR ENERGY CONSTANT WITH APPARENT OUTPUT SWITCHING FREQUENCY LIMITATION (CONSTANT)

	MC	**SMC**	**ANPC 1** **SCx+FCx**	**ANPC 2** **FCx+SCx**	**ANPC 3** **FCx+FCx**	**FSx+FCx**	**FC2 * x**
$\mathbf{F_{sw\_out}}$	F_{sw_base}	F_{sw_base}	F_{sw_base}	F_{sw_base}	F_{sw_base}	F_{sw_base}	F_{sw_base}
$\mathbf{K_{E\_cap}}$ **(N=2)**	0.5	0	0	0	0	0	0.5
$\mathbf{K_{E\_cap}}$ **(N=4)**	3.5	0.5	0.25	0.5	0.75	0.25	0.75
$\mathbf{K_{E\_cap}}$ **(N=6)**	9.167	1.667	0.833	1.667	2.5	0.833	1
$\mathbf{K_{E\_cap}}$ **(N=8)**	17.5	3.5	1.75	3.5	5.25	1.75	1.25
$\mathbf{K_{E\_cap}}$ **(N=10)**	28.5	6	3	6	9	3	1.5

9.2.2 M²LC compared to MC topologies

TABLE 80, FLYING CAPACITOR ENERGY CONSTANT ($K_{2\_E\_cap}$ or K_{M2LC} scaled by 1000) WITH AVERAGE DEVICE SWITCHING FREQUENCY OF 250 HZ AND A FUNDAMENTAL FREQUENCY OF 50 HZ

	MC	SMC	ANPC 1 SCx+FCx	ANPC 2 FCx+SCx	ANPC 3 FCx+FCx	M²LC
K * 1000 (N=2)	1.00	**0.00**	**0.00**	**0.00**	0.00	1.59
K * 1000 (N=4)	3.50	**0.50**	**0.50**	**0.50**	0.75	1.59
K * 1000 (N=6)	6.11	**1.11**	**1.11**	**1.11**	1.67	1.59
K * 1000 (N=8)	8.75	1.75	1.75	1.75	2.63	**1.59**
K * 1000 (N=10)	11.40	2.40	2.40	2.40	3.60	**1.59**

TABLE 81, FLYING CAPACITOR ENERGY CONSTANT ($K_{2\_E\_cap}$ or K_{M2LC} scaled by 1000) WITH AVERAGE DEVICE SWITCHING FREQUENCY OF 2 KHZ AND A FUNDAMENTAL FREQUENCY OF 50 HZ

	MC	SMC	ANPC 1 SCx+FCx	ANPC 2 FCx+SCx	ANPC 3 FCx+FCx	M²LC
K * 1000 (N=4)	0.44	**0.06**	**0.06**	**0.06**	0.09	1.59
K * 1000 (N=8)	1.09	**0.22**	**0.22**	**0.22**	0.33	1.59
K * 1000 (N=12)	1.76	**0.38**	**0.38**	**0.38**	0.57	1.59
K * 1000 (N=16)	2.42	**0.55**	**0.55**	**0.55**	0.82	1.59
K * 1000 (N=20)	3.09	**0.71**	**0.71**	**0.71**	1.07	1.59
K * 1000 (N=24)	3.75	**0.88**	**0.88**	**0.88**	1.32	1.59
K * 1000 (N=28)	4.42	**1.04**	**1.04**	**1.04**	1.57	1.59
K * 1000 (N=32)	5.09	**1.21**	**1.21**	**1.21**	1.82	1.59
K * 1000 (N=36)	5.75	**1.38**	**1.38**	**1.38**	2.07	1.59
K * 1000 (N=40)	6.42	**1.54**	**1.54**	**1.54**	2.32	1.59
K * 1000 (N=44)	7.09	1.71	1.71	1.71	2.57	**1.59**
K * 1000 (N=48)	7.75	1.88	1.88	1.88	2.82	**1.59**

9.3 Single phase NP current functions

TABLE 82, MODULATION SCHEMES AND NP CURRENT FUNCTIONS FOR NPC AND ANPC

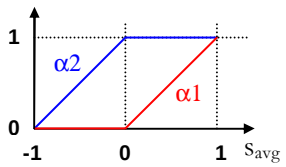
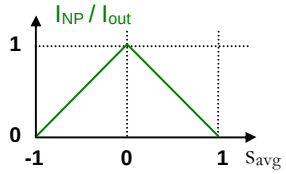
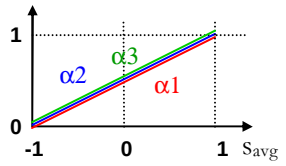
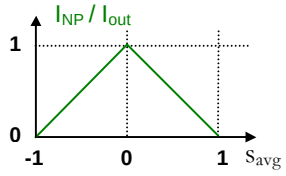
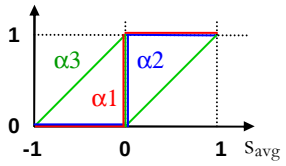
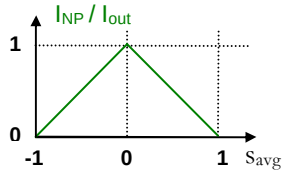
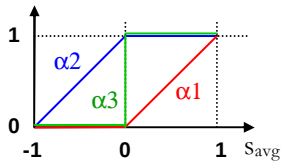
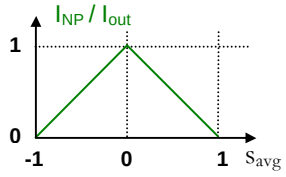
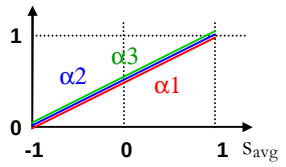
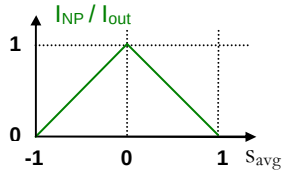
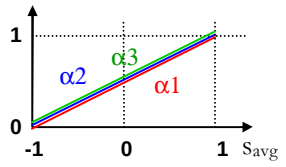
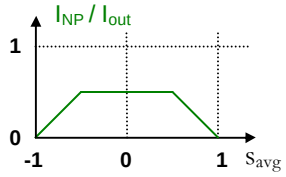
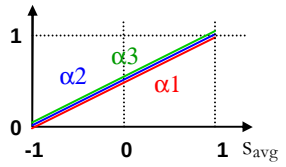
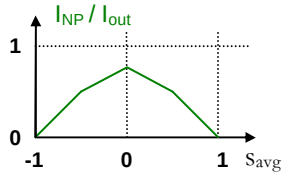
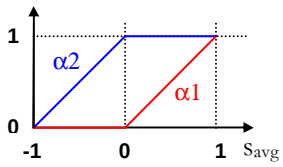
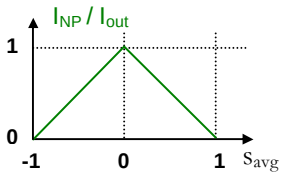
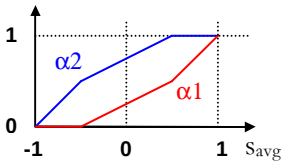
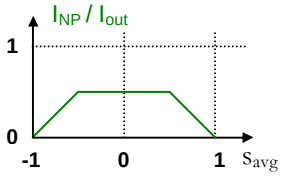
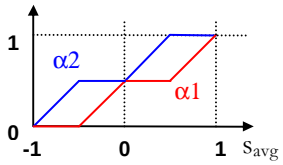
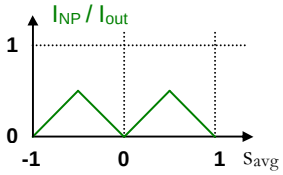
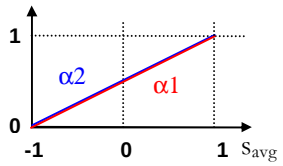
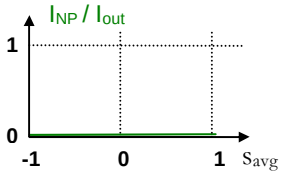
NPC		
ANPC 3-L		
ANPC Type 1 and Type 3 Type 1 modulation		
ANPC Type 2 and Type 3 Type 2 modulation		
ANPC Type 3 Type 1 and 2 NP states		
ANPC Type 3 Type 3 NP states		
ANPC Type 3 Mixed NP states		

TABLE 83, MODULATION SCHEMES AND NP CURRENT FUNCTIONS FOR THE SMC

SMC Standard modulation		
SMC Type A modulation		
SMC Type B modulation		
SMC pure FC modulation		

9.4 States of the ANPC 1 in the first 60° segment

TABLE 84, STATES OF THE ANPC 1 INT THE FIRST 60° SEGMENT

States				Levels			Currents			
Total	a	b	c	a	b	c	i-NP	i-FC-a	i-FC-b	i-FC-c
0	0	0	0	0	0	0	0	0	0	0
73	1	1	1	1	1	1	0	ia	ib	ic
74	2	1	1	1	1	1	ia	-ia	ib	ic
81	1	2	1	1	1	1	ib	ia	-ib	ic
82	2	2	1	1	1	1	-ic	-ia	-ib	ic
137	1	1	2	1	1	1	ic	ia	ib	-ic
138	2	1	2	1	1	1	-ib	-ia	ib	-ic
145	1	2	2	1	1	1	-ia	ia	-ib	-ic
146	2	2	2	1	1	1	0	-ia	-ib	-ic
219	3	3	3	2	2	2	0	0	0	0
365	5	5	5	3	3	3	0	ia	ib	ic
366	6	5	5	3	3	3	-ia	-ia	ib	ic
373	5	6	5	3	3	3	-ib	ia	-ib	ic
374	6	6	5	3	3	3	ic	-ia	-ib	ic
429	5	5	6	3	3	3	-ic	ia	ib	-ic
430	6	5	6	3	3	3	ib	-ia	ib	-ic
437	5	6	6	3	3	3	ia	ia	-ib	-ic
438	6	6	6	3	3	3	0	-ia	-ib	-ic
511	7	7	7	4	4	4	0	0	0	0
1	1	0	0	1	0	0	0	ia	0	0
2	2	0	0	1	0	0	ia	-ia	0	0
75	3	1	1	2	1	1	ia	0	ib	ic
83	3	2	1	2	1	1	-ic	0	-ib	ic
139	3	1	2	2	1	1	-ib	0	ib	-ic
147	3	2	2	2	1	1	0	0	-ib	-ic
221	5	3	3	3	2	2	0	ia	0	0
222	6	3	3	3	2	2	-ia	-ia	0	0
367	7	5	5	4	3	3	-ia	0	ib	ic
375	7	6	5	4	3	3	ic	0	-ib	ic
431	7	5	6	4	3	3	ib	0	ib	-ic
439	7	6	6	4	3	3	0	0	-ib	-ic
9	1	1	0	1	1	0	0	ia	ib	0
10	2	1	0	1	1	0	ia	-ia	ib	0
17	1	2	0	1	1	0	ib	ia	-ib	0
18	2	2	0	1	1	0	-ic	-ia	-ib	0
91	3	3	1	2	2	1	-ic	0	0	ic
155	3	3	2	2	2	1	0	0	0	-ic
237	5	5	3	3	3	2	0	ia	ib	0
238	6	5	3	3	3	2	-ia	-ia	ib	0
245	5	6	3	3	3	2	-ib	ia	-ib	0
246	6	6	3	3	3	2	ic	-ia	-ib	0
383	7	7	5	4	4	3	ic	0	0	ic
447	7	7	6	4	4	3	0	0	0	-ic
3	3	0	0	2	0	0	ia	0	0	0
77	5	1	1	3	1	1	ia	ia	ib	ic
78	6	1	1	3	1	1	0	-ia	ib	ic
85	5	2	1	3	1	1	-ic	ia	-ib	ic
86	6	2	1	3	1	1	ib	-ia	-ib	ic
141	5	1	2	3	1	1	-ib	ia	ib	-ic
142	6	1	2	3	1	1	ic	-ia	ib	-ic
149	5	2	2	3	1	1	0	ia	-ib	-ic
150	6	2	2	3	1	1	-ia	-ia	-ib	-ic
223	7	3	3	4	2	2	-ia	0	0	0
11	3	1	0	2	1	0	ia	0	ib	0
19	3	2	0	2	1	0	-ic	0	-ib	0
93	5	3	1	3	2	1	-ic	ia	0	ic
94	6	3	1	3	2	1	ib	-ia	0	ic
157	5	3	2	3	2	1	0	ia	0	-ic
158	6	3	2	3	2	1	-ia	-ia	0	-ic
239	7	5	3	4	3	2	-ia	0	ib	0
247	7	6	3	4	3	2	ic	0	-ib	0
27	3	3	0	2	2	0	-ic	0	0	0
109	5	5	1	3	3	1	-ic	ia	ib	ic
110	6	5	1	3	3	1	ib	-ia	ib	ic
117	5	6	1	3	3	1	ia	ia	-ib	ic
118	6	6	1	3	3	1	0	-ia	-ib	ic
173	5	5	2	3	3	1	0	ia	ib	-ic
174	6	5	2	3	3	1	-ia	-ia	ib	-ic
181	5	6	2	3	3	1	-ib	ia	-ib	-ic
182	6	6	2	3	3	1	ic	-ia	-ib	-ic
255	7	7	3	4	4	2	ic	0	0	0

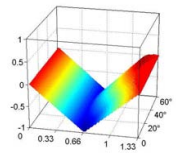
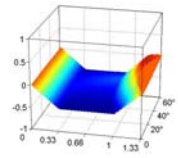
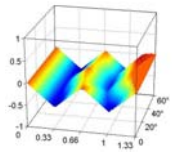
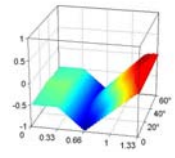
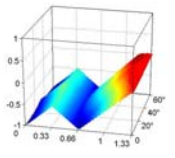
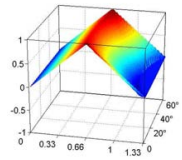
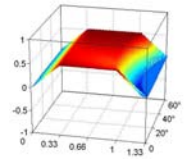
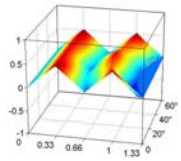
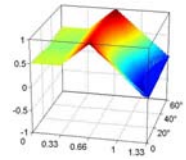
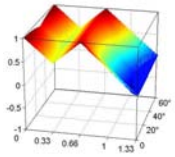
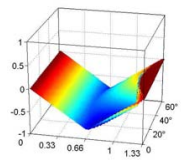
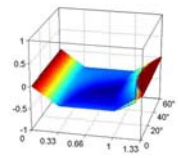
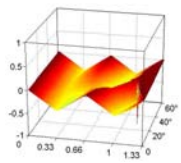
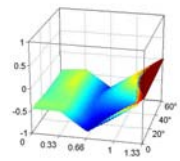
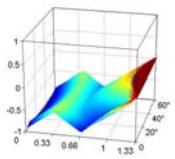
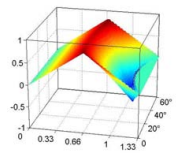
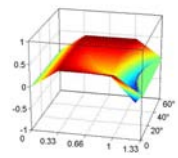
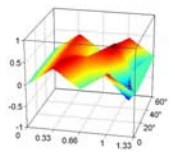
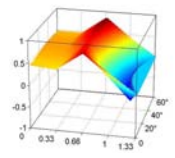
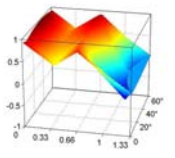
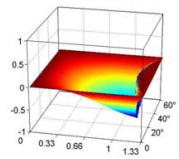
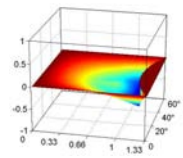
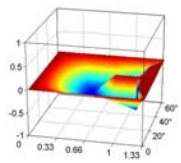
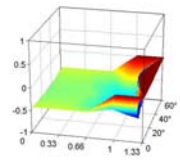
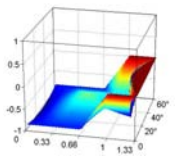
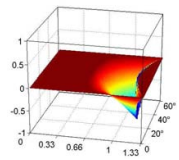
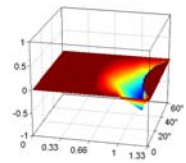
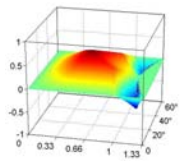
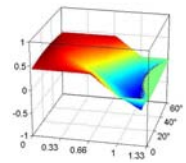
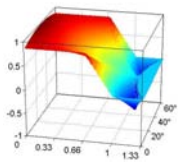
5	5	0	0	3	0	0	ia	ia	0	0
6	6	0	0	3	0	0	0	-ia	0	0
79	7	1	1	4	1	1	0	0	ib	ic
87	7	2	1	4	1	1	ib	0	-ib	ic
143	7	1	2	4	1	1	ic	0	ib	-ic
151	7	2	2	4	1	1	-ia	0	-ib	-ic
13	5	1	0	3	1	0	ia	ia	ib	0
14	6	1	0	3	1	0	0	-ia	ib	0
21	5	2	0	3	1	0	-ic	ia	-ib	0
22	6	2	0	3	1	0	ib	-ia	-ib	0
95	7	3	1	4	2	1	ib	0	0	ic
159	7	3	2	4	2	1	-ia	0	0	-ic
29	5	3	0	3	2	0	-ic	ia	0	0
30	6	3	0	3	2	0	ib	-ia	0	0
111	7	5	1	4	3	1	ib	0	ib	ic
119	7	6	1	4	3	1	0	0	-ib	ic
175	7	5	2	4	3	1	-ia	0	ib	-ic
183	7	6	2	4	3	1	ic	0	-ib	-ic
45	5	5	0	3	3	0	-ic	ia	ib	0
46	6	5	0	3	3	0	ib	-ia	ib	0
53	5	6	0	3	3	0	ia	ia	-ib	0
54	6	6	0	3	3	0	0	-ia	-ib	0
127	7	7	1	4	4	1	0	0	0	ic
191	7	7	2	4	4	1	ic	0	0	-ic
7	7	0	0	4	0	0	0	0	0	0
15	7	1	0	4	1	0	0	0	ib	0
23	7	2	0	4	1	0	ib	0	-ib	0
31	7	3	0	4	2	0	ib	0	0	0
47	7	5	0	4	3	0	ib	0	ib	0
55	7	6	0	4	3	0	0	0	-ib	0
63	7	7	0	4	4	0	0	0	0	0
States				Levels			Currents			
Total	a	b	c	a	b	c	i-NP	i-FC-a	i-FC-b	i-FC-c

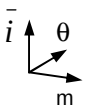
- States are defined as $\{c_1c_2c_3b_1b_2b_3a_1a_2a_3\}_{BS}$ (c_1 = MSB, a_3 = LSB).
- Output levels are numbered from 0 to 4.
- Currents are defined as positive when flowing out of the converter. Positive values indicate discharge of either NP and / or FC, negative currents are correspondingly charging NP or FC.

9.5 NP currents as a function of m, φ and θ

9.5.1 Maximum and minimum currents for SMC and ANPC3

TABLE 85, NP CURRENT LIMITS (MIN AND MAX) IN SYMMETRICAL 3 PHASE SYSTEMS MAKING USE OF DIFFERENT MODULATION TYPES AND CM VOLTAGE. THE ANGLE INDICATES POSITION OF THE VOLTAGE VECTOR IN THE FIRST 60° SEGMENT IN THE αβ-FRAME

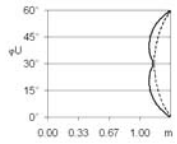
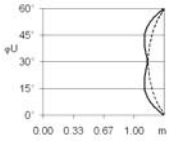
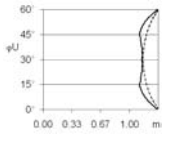
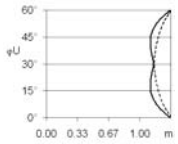
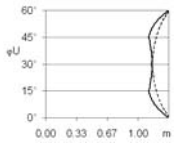
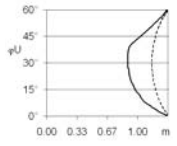
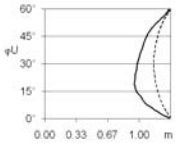
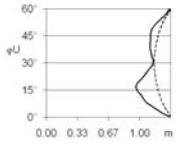
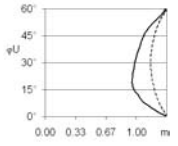
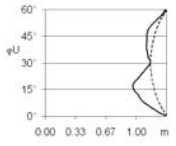
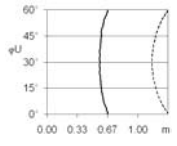
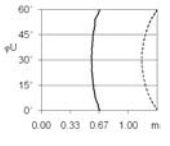
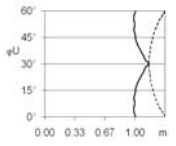
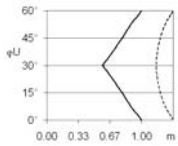
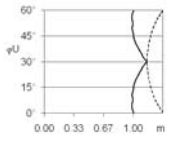
Condition	Standard modulation	SMC A modulation	SMC B modulation	Std. and A combined	All types combined
cos(φ)=1 **I_{NP}-min**					
cos(φ)=1 **I_{NP}-max**					
cos(φ)=0.81 **(inductive)** **I_{NP}-min**					
cos(φ)=0.81 **(inductive)** **I_{NP}-max**					
cos(φ)=0 **(inductive)** **I_{NP}-min**					
cos(φ)=0 **(inductive)** **I_{NP}-max**					



Axes definition applies to all of TABLE 85 and TABLE 87. m = 2/sqrt(3) for maximum sinusoidal phase to phase output voltage.

9.5.2 Zero average NP current areas for SMC and ANPC3

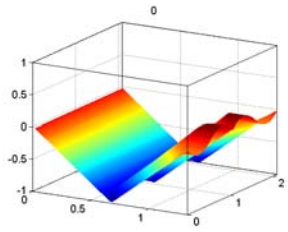
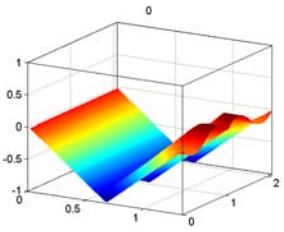
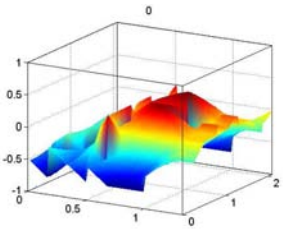
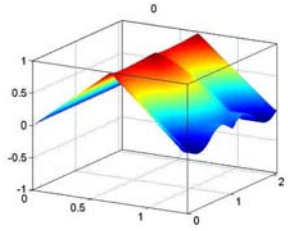
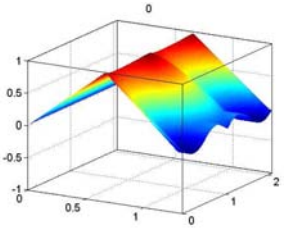
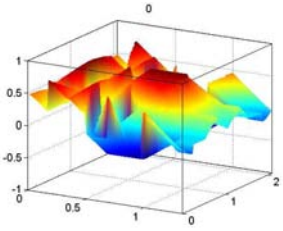
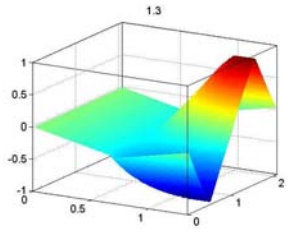
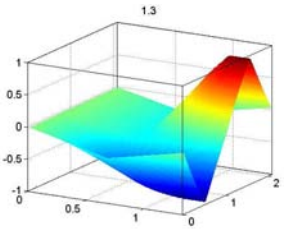
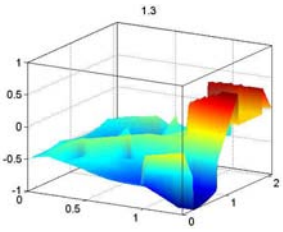
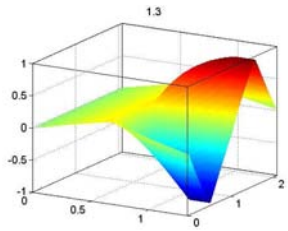
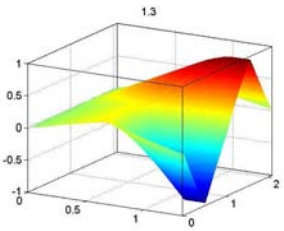
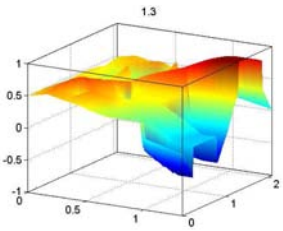
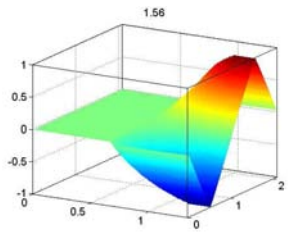
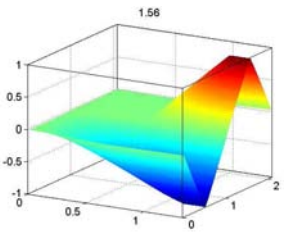
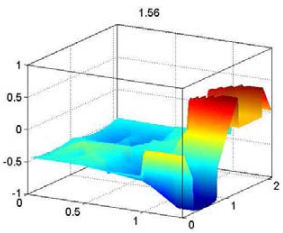
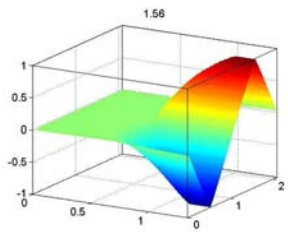
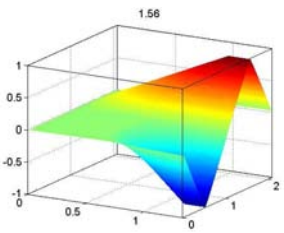
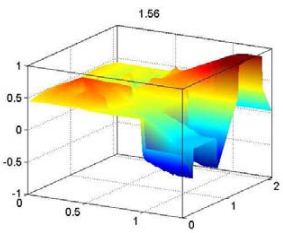
TABLE 86, ZERO AVERAGE NP CURRENT AREAS IN SYMMETRICAL 3 PHASE SYSTEMS MAKING USE OF DIFFERENT MODULATION TYPES AND CM VOLTAGE

Condition	Standard modulation	SMC A modulation	SMC B modulation	Std. and A combined	All types combined
cos(φ)=1					
cos(φ)=0.81 (inductive)					
cos(φ)=0 (inductive)					

- left of bold line: zero current possible
- right of bold line: zero NP current not possible
- dotted line: physical operation limit
- Axes definition applies to all of TABLE 85 and TABLE 87. m = 2/sqrt(3) for maximum sinusoidal phase to phase output voltage.

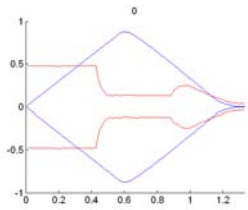
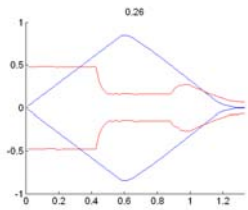
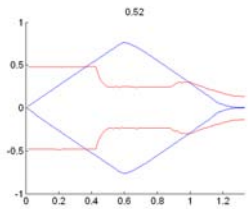
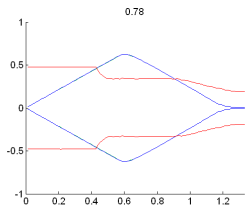
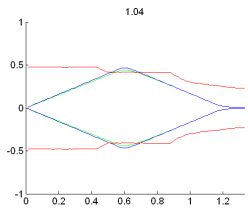
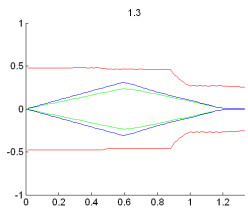
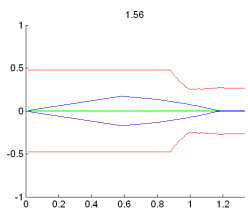
9.5.3 Maximum and minimum currents for the ANPC1

TABLE 87, NP CURRENT LIMITS (MIN AND MAX) IN SYMMETRICAL 3 PHASE SYSTEMS MAKING USE OF DIFFERENT MODULATION TYPES . THE ANGLE INDICATES POSITION OF THE VOLTAGE VECTOR IN THE FIRST TWO SEGMENTS IN THE αβ-FRAME (0 TO 2π/3)

Condition	Unconstrained DC CM injection	Real time NP current function	Modified and virtual vectors
cos(φ)=1 **I_{NP}-min** $\bar{i}$ θ m			
cos(φ)=1 **I_{NP}-max**			
φ = 1.3 **cos(φ)=0.27** **(inductive)** **I_{NP}-min**			
φ = 1.3 **cos(φ)=0.27** **(inductive)** **I_{NP}-max**			
φ = 1.56 **cos(φ)=0.01** **(inductive)** **I_{NP}-min**			
φ = 1.56 **cos(φ)=0.01** **(inductive)** **I_{NP}-max**			

9.5.4 Maximum and minimum average currents for the ANPC1

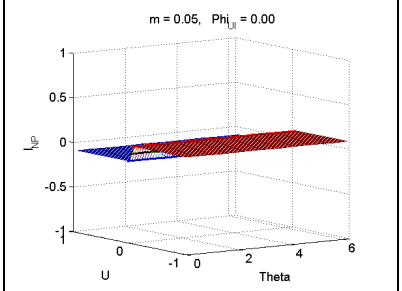
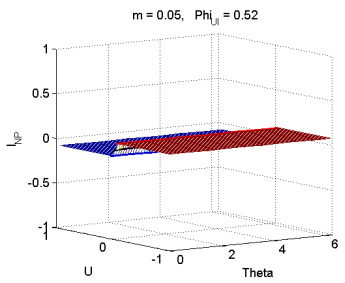
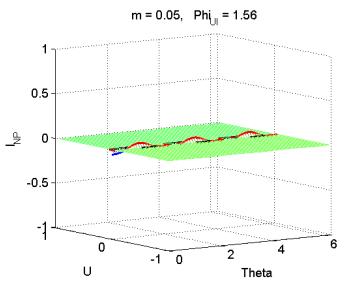
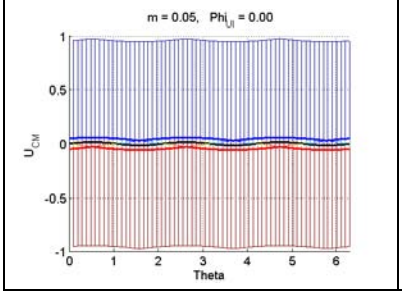
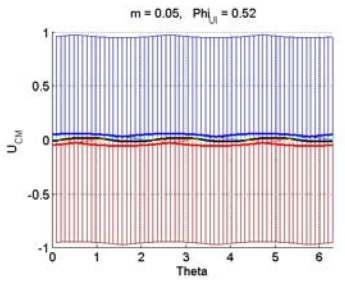
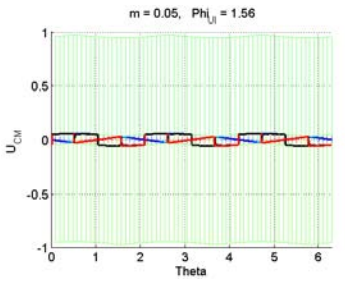
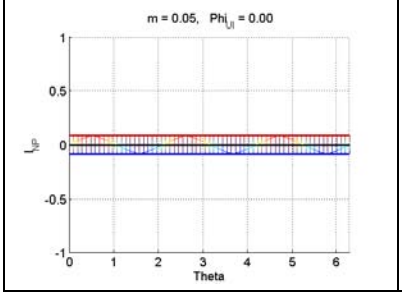
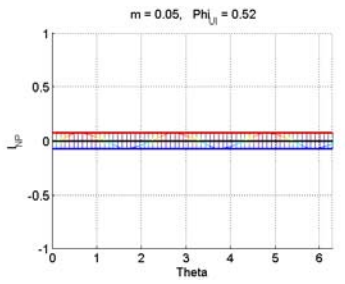
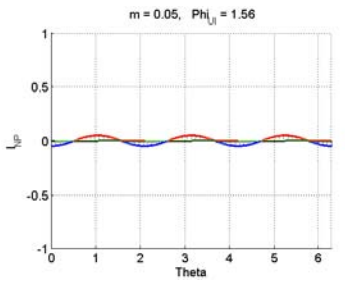
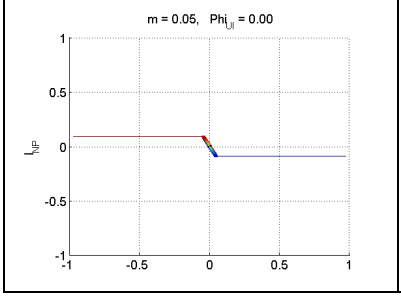
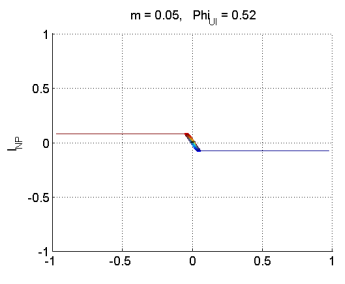
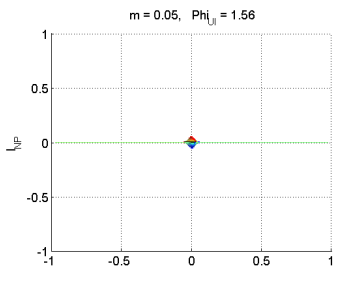
TABLE 88, MAXIMUM AND MINIMUM AVERAGE CURRENTS OVER ONE THIRD OF THE FUNDAMENTAL PERIOD FOR UNCONSTRAINED DC CM INJECTION (GREEN), REAL TIME NP CURRENT FUNCTION (BLUE, APPLIES ALSO TO 6TH HARMONIC INJECTION FOR HIGH LOAD ANGLES), AND MODIFIED AND VIRTUAL VECTOR SEQUENCES (RED)

Condition	Max. and min. average NP currents	Comment
φ = 0 i_{avg_fund} m		**Virtual vectors are highly effective in the low modulation depth region and allow for control in over modulation region**
φ = 0.26		**Increasing NP control capacity in over modulation region with virtual vectors.**
φ = 0.52		**Significant improvement of NP control capacity for high modulation depth (linear region) with virtual vectors**
φ = 0.78		
φ = 1.04		**Virtual vectors provide highest NP control capacity except for intermediate modulation depth**
φ = 1.3		**Virtual vectors provide by far highest NP control capacity for any modulation depth. Unconstrained DC CM injection gets less effective due to the non monotonic characteristic of the NP current function.**
φ = 1.56		**Unconstrained DC CM injection does not work at all. The real time NP function provides good controllability in the mid range. The blue curve also applies to 6th harmonic injection for this load angle.**

9.6 NP current functions for 3-L DC link converters

All of the following graphs are based on standard modulation schemes using optimum modulation and decoupled FC and NP control.

TABLE 89, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 0.05

m = 0.05, cos(φ) = 1 (φ = 0)	m = 0.05, cos(φ) = 0.86 (φ = 0.52)	m = 0.05, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

Legend (applies to TABLE 89 - TABLE 94) :

- red: maximum NP current trajectory
- blue: minimum NP current trajectors
- black: CM voltage trajectory generating the lowest possible NP current ripple
- the U-axis in the 1st row of graphs and the x-Axis in the 4th row of graphs refer all to U_{CM}

Note that the range of useful CM voltage for NP control is very small at low modulation depth (TABLE 89). Especially for pure reactive power operation, it is crucial to constrain the CM function.

TABLE 90, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 0.25

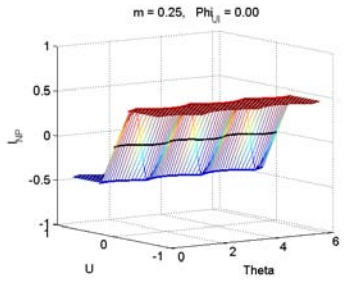
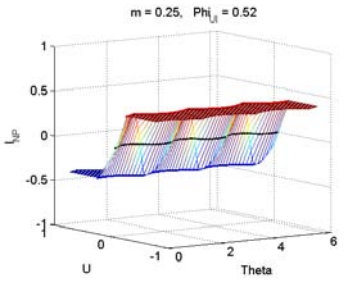
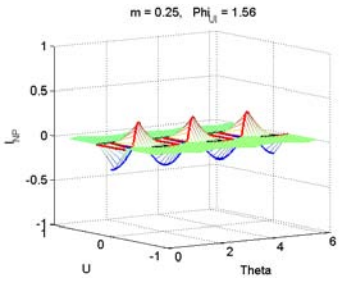
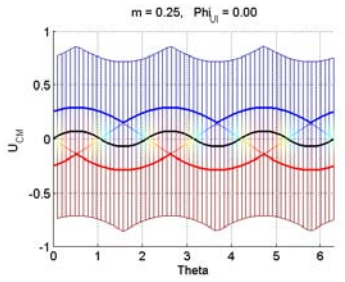
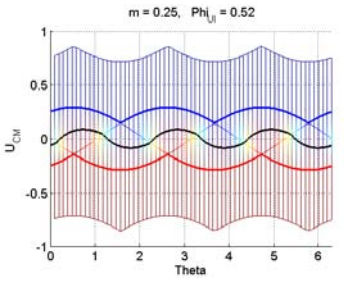
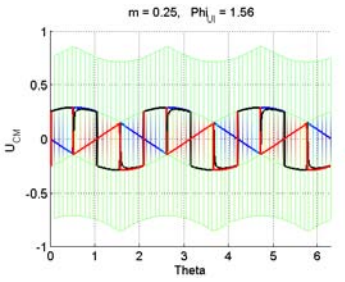
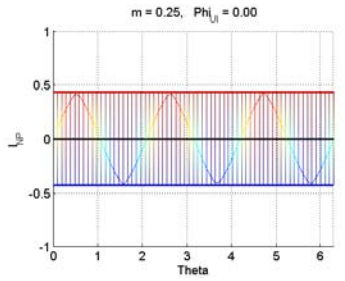
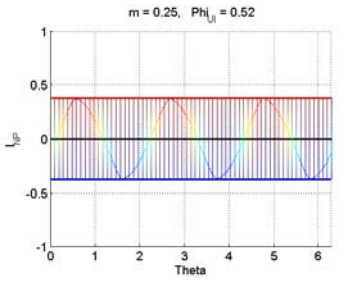
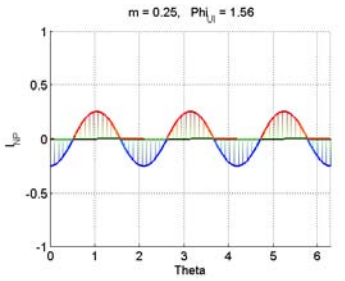
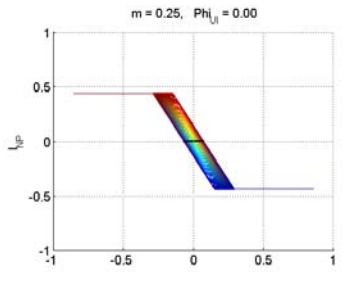
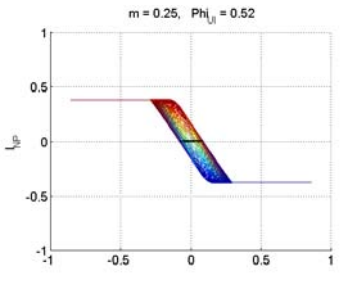
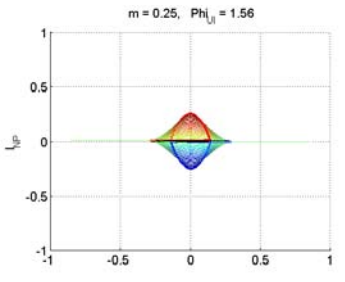
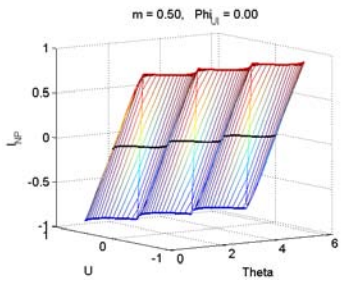
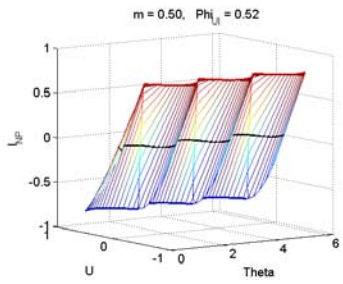
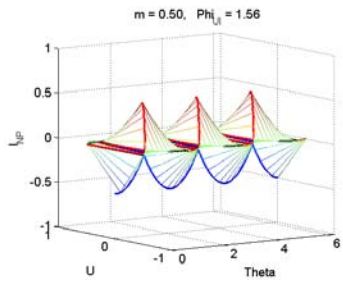
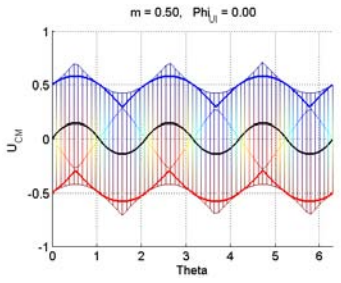
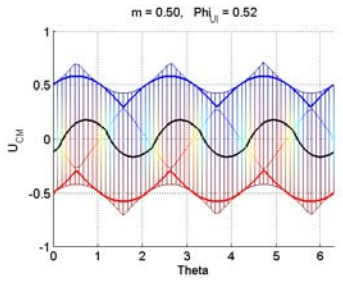
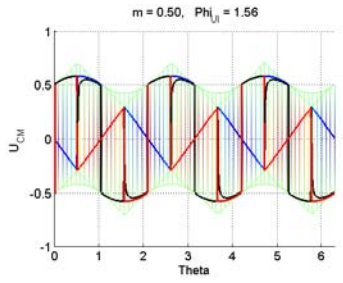
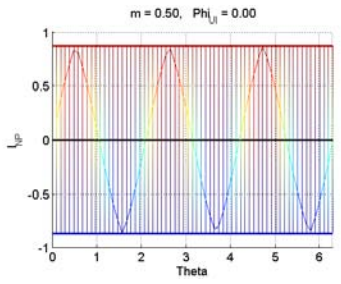
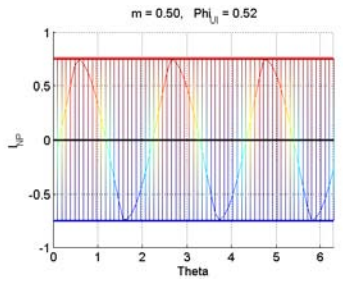
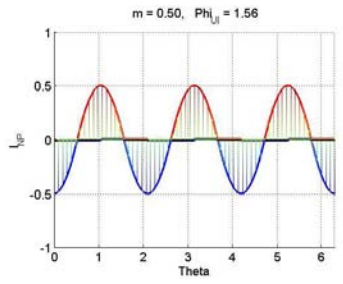
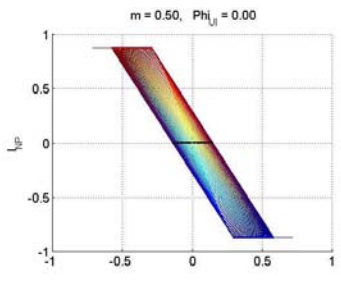
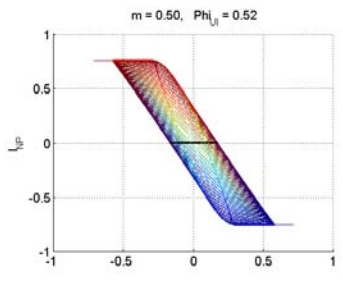
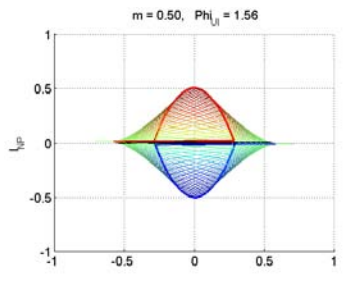
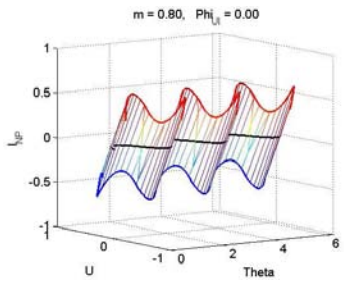
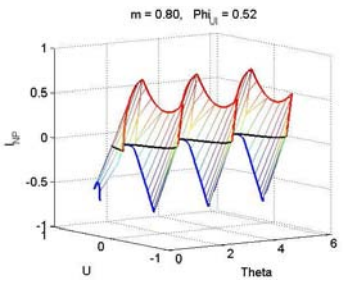
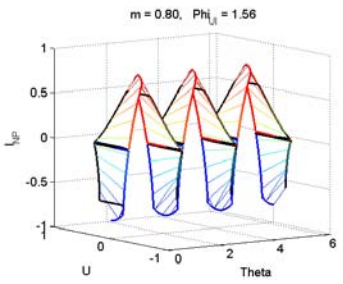
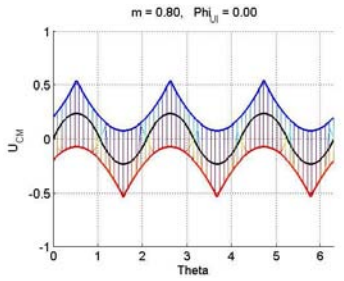
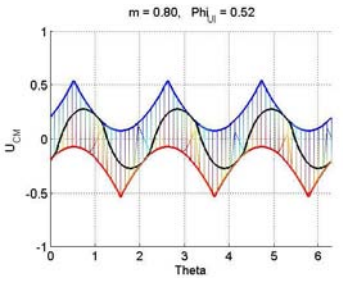
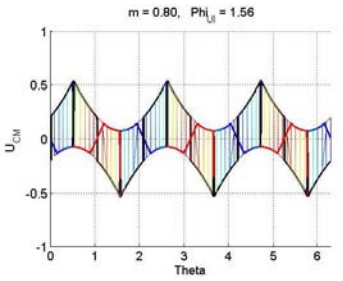
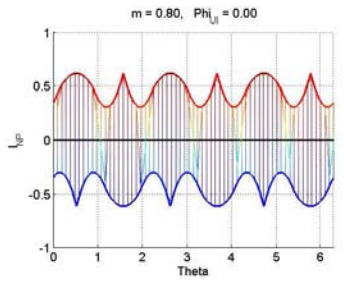
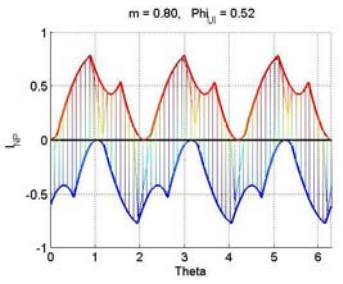
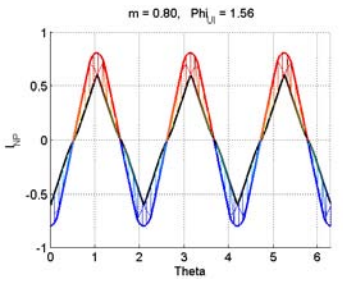
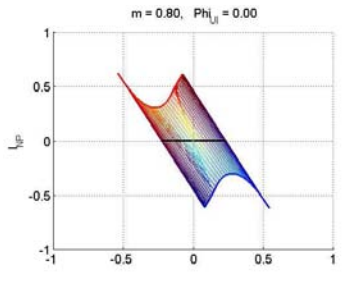
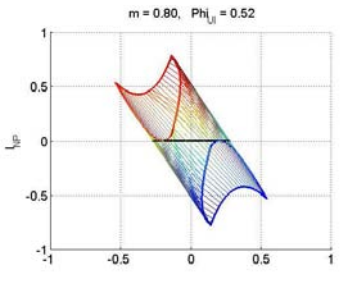
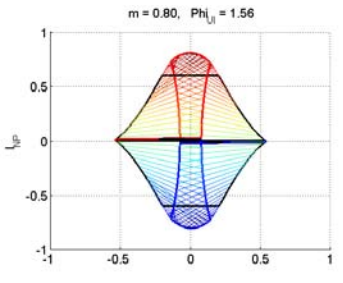
m = 0.25, cos(φ) = 1 (φ = 0)	m = 0.25, cos(φ) = 0.86 (φ = 0.52)	m = 0.25, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

TABLE 91, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 0.5

m = 0.5, cos(φ) = 1 (φ = 0)	m = 0.5, cos(φ) = 0.86 (φ = 0.52)	m = 0.5, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

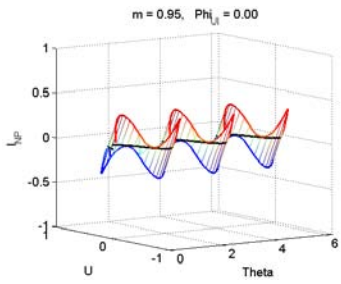
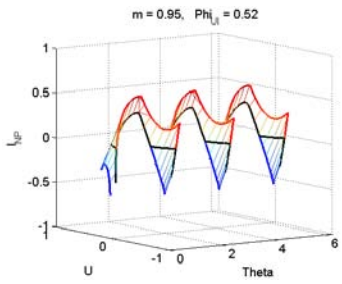
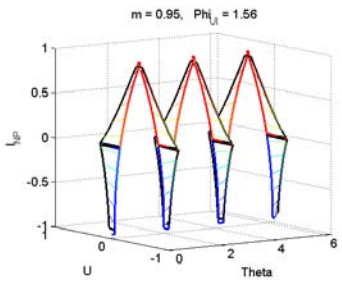
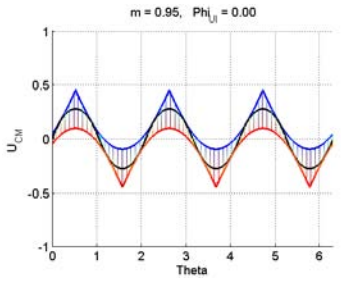
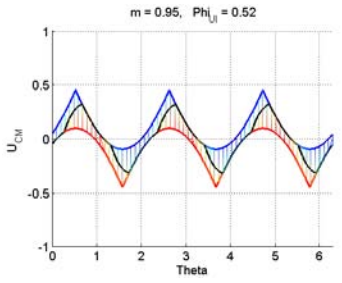
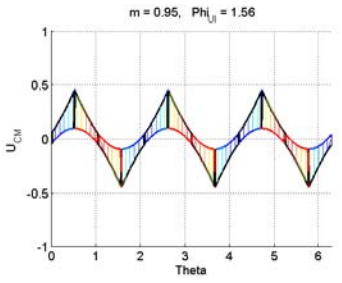
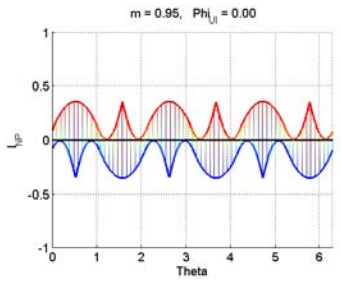
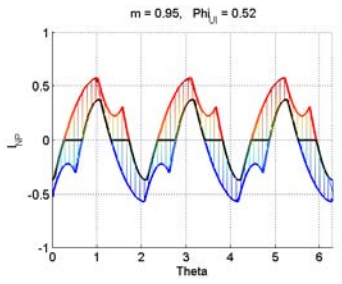
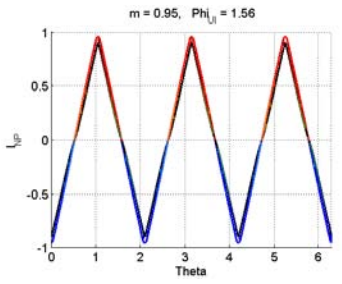
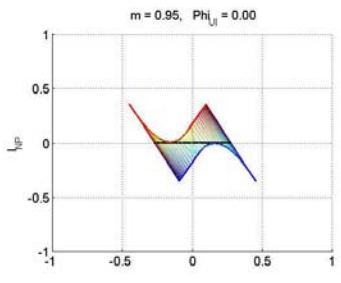
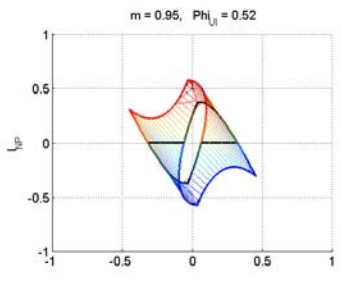
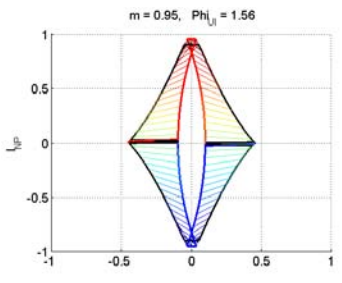
This operating point corresponds with the maximum modulation depth for zero NP current operation in pure reactive power operation (cos(φ) = 0, Figure 63).

TABLE 92, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 0.8

m = 0.8, cos(φ) = 1 (φ = 0)	m = 0.8, cos(φ) = 0.86 (φ = 0.52)	m = 0.8, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

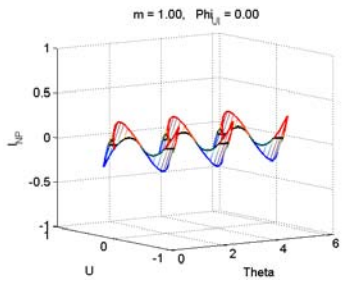
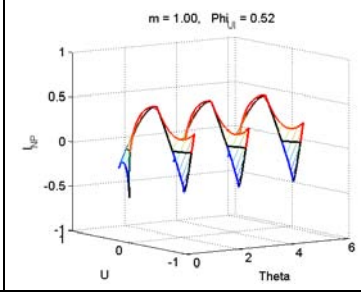
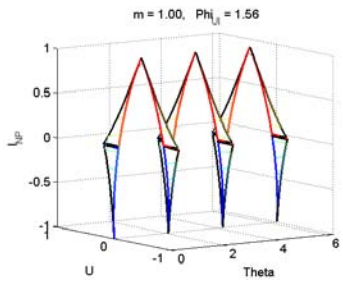
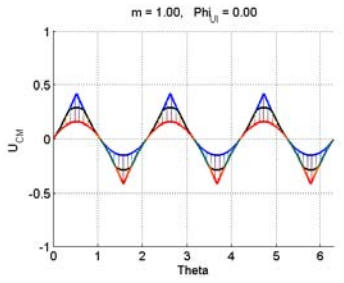
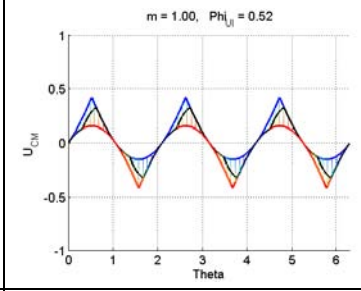
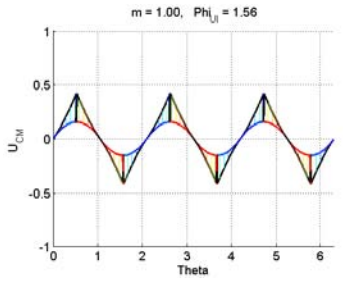
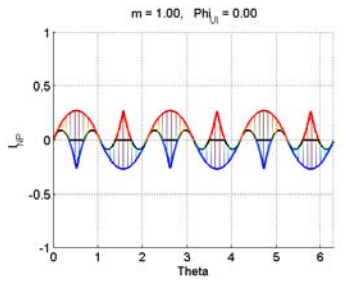
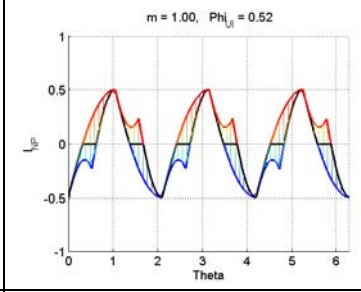
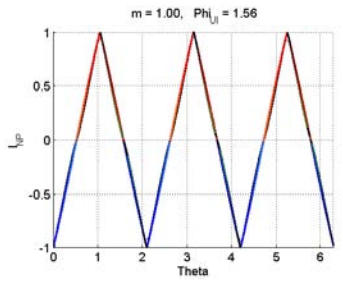
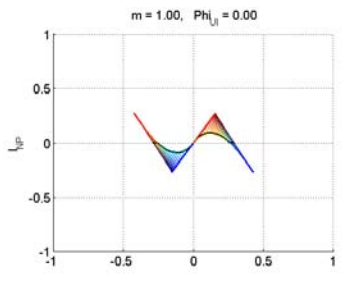
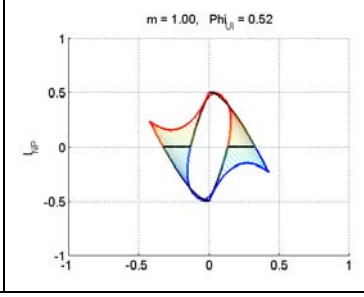
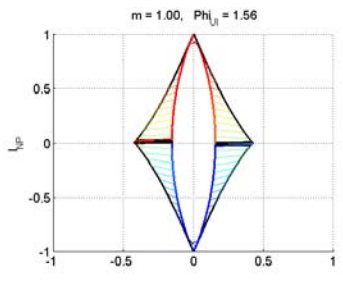
This operating point corresponds with the maximum modulation depth for zero NP current operation with cos(φ) = 0.86 (φ = 0.52, see also Figure 63).

TABLE 93, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 0.95

m = 0.95, cos(φ) = 1 (φ = 0)	m = 0.95, cos(φ) = 0.86 (φ = 0.52)	m = 0.95, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

This operating point corresponds with the maximum modulation depth for zero NP current operation pure active power operation (cos(φ) = 1, see also Figure 63).

TABLE 94, NP CURRENT IN FUNCTION OF CM VOLTAGE AND OUTPUT VOLTAGE ANGEL θ, MODULATION DEPTH m = 1

m = 1, cos(φ) = 1 (φ = 0)	m = 1, cos(φ) = 0.86 (φ = 0.52)	m = 1, cos(φ) = 0.01 (φ = 1.56)
		
		
		
		

This operating point provides maximum sinusoidal phase to phase values before going into over modulation. Note the shape of the minimum injected NP current. It contains a dominant 3rd harmonic for all load angles, but also relatively large higher harmonics (odd multiples of three).

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