EFFECTS OF ION BEAMS ON FLASH MEMORY CELLS

by

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This paper deals with the flash memory reliability in terms of the ionizing radiation effects. In fact, the reliability of flash memory depends on physico-chemical restrictions of electrostatic nature due to the effects of ionizing radiation. The presented results are actual as a high degree of integrated components miniaturization affects the memory sensitivity, while the role of memories in the solar cells management system for space flights is increasing, so that the effects of ionizing radiation may cause changes in the stored data or the physical destruction of the flash memory components.

Key words: flash memory, radiation hardness, Monte-Carlo simulation

INTRODUCTION

The miniaturization of electronic devices initiated with the appearance of the first semiconductor devices has to this day reached a considerable level of development in many areas of electrical engineering. At first it was attempted to implement semiconductor devices for lower frequencies, which did not achieve satisfactory results. One of the first semiconductor devices used at these frequencies was a tunnel diode, which is now completely suppressed by the elements of the TE-diode group, bipolar and MOSFET transistors, as it proved to be temperature unstable and sensitive to the effects of radiation. Microwave semiconductor devices began to develop in the early sixties. Since then many semiconductor devices have been developed for applications in microwave oscillators, amplifiers, mixers, detectors, *etc*. Semiconductor devices used in electronics are numerous and among them the special attention should be given to the flash memories.

Flash memory is the latest form of semiconductor memory that is named because of the speed with which can be reprogrammed. Flash memory first appeared in the mid-eighties and it was intermediate between EPROM and EEPROM memory according to the price and the functionality. Flash memory, the same as EEPROM, uses an electrical erasing technology. The entire flash memory can be erased in a matter of seconds. However, the flash memory can not be erased byte by byte, but only by blocks. Flash memory achieves the same packing density as well as EPROM (greater than EEPROM) because it uses only one transistor per bit of data. This is the most flexible type of ROM, and today it is often used to store the BIOS program. The use of flash memory to store the BIOS allows the user to always have the current version of BIOS on the computer.

Flash memory offers fast access to data besides the feature that it does not require power supply for data storage. Another very important feature of flash memory is that it has better kinetic shock resistance than hard disks. It is almost physically indestructible when packed in a memory card which is used by a digital device.

Due to its characteristics, flash memory plays an important role in the system for management of solar cells in space flights. For this reason, the stability characteristics of flash memory under the influence of light ions are of a particular interest (primary cosmic radiation), as well as the actual interaction with flash heavy ions (secondary cosmic radiation, and conditions of a particular risk). This aspect of the characteristics of flash memory has lately often been the subject of scientific interest. Hence, this paper is a continuation of work in the same field carried out at our project [1-5].

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THE PRINCIPLES OF THE FLASH MEMORY

Flash memory stores information in the rows of floating gate transistors (FTG) called "cells" and each cell stores one bit of information. Devices of newer generation which use flash memory can store more than one bit of information per cell, using more than two levels of electrical charge where each successive information is placed on the "floating" input of a cell [6, 7]. In flash memory, each cell looks similar to a standard metal oxide semiconductor field-effect transistor cell (MOSFET), except that it has two inputs instead of one. One input (gate), as in other MOS transistors, is the control input (CG), while the second input is "floating" (FG) and isolated with single oxide layer. Floating input is located between the control input and the substrate. Since the floating input is isolated with oxide layer, any electron that is found in it is trapped and in that way floating gate places the information. When electrons are on the floating input, they modify (halt) electric field that occurs from the control input, which modifies the voltage pulse of the cell. In this way, when a cell is "read" by setting certain voltage pulse on the control input, the current electric state will or will not flow, depending on the voltage pulse of the cell, controlled by the number of electrons on the floating input. The presence or absence of the current electrical condition is detected and translated into "zeros" and "ones", thus reproducing the stored data.

In the devices which store more than one bit of information per cell (multi-level cell device), the amount of current flow is detected in order to determine the number of electrons stored in the floating gate. Figure 1 shows the architecture of flash memory.

In order to program memory cell flash control leads short voltage pulse. Voltage pulse triggers the avalanche breakdown of the memory transistor that charges floating input (hot-electron injection). In this way, 1-Mbit chip of flash memory can be programmed in two seconds as opposed to the normal EEPROM. However, chip erase is performed simultaneously. During deletion, the flash memory control sends erasure impulses in the entire field of memory and in this way erases all memory cells. Erasure time for the whole flash memory is about one second. Figure 2 shows the block diagram of the flash memory.

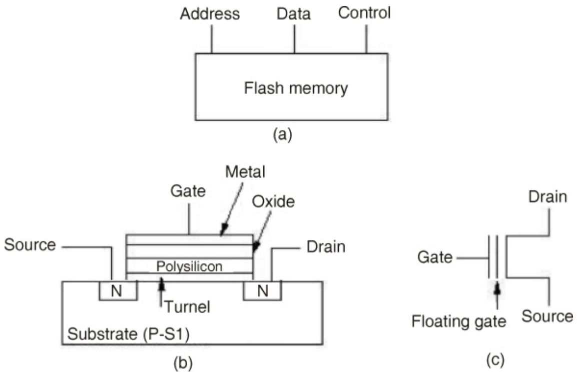

Figure 1. Architecture of the flash memory

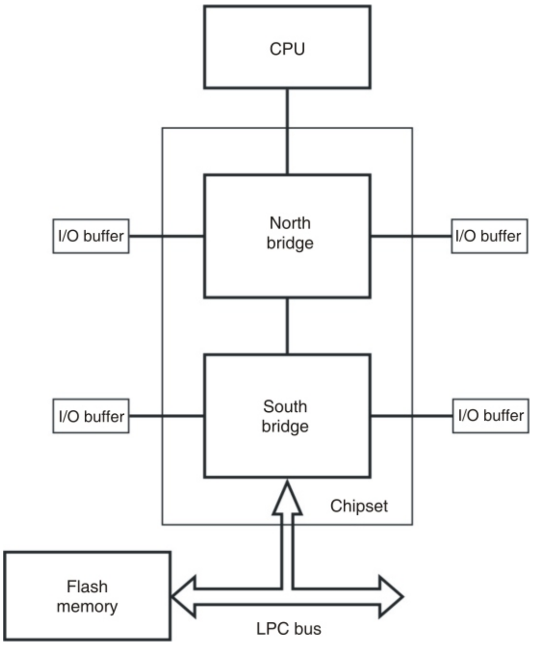

Figure 2. Block diagram of the flash memory

The central part of the flash memory is a matrix of memory cells. Cells are addressed by address buffer that alternately receives and transmits address signals to the sector of rows and columns. Row and column decoders select a word line and one or more pairs of bit-lines, as in the normal memory chip. The data is read by the I/O data buffer or is written in an addressed memory cell by the buffer through the I/O port.

The processes of reading, deleting, and programming are controlled by double-byte instructions that external microprocessor enters into the instruction register of flash control.

Depending on a circuit realized by each memory cell, flash chips are classified into two main categories: NOR and NAND.

NOR flash memory is suitable for use in microprocessor systems due to its ability to directly connect to the system. In addition, when it works in read-only mode, the memory is operating in a similar way as EPROM which characterizes simply designed interface.

The NOR structure, shown in fig. 3, provides direct access to individual cells. This simplifies the overall device architecture, but increases cell area because of the need for contacts at each drain and source. The NOR structure is used by Intel. It requires voltages of about 12 V for erasing and writing.

The second approach uses the NAND structure, as shown in fig. 4. The NAND cell is more compact because it does not provide contacts to individual source and drain regions. However, cells in the NAND structure require reading and writing through the other cells

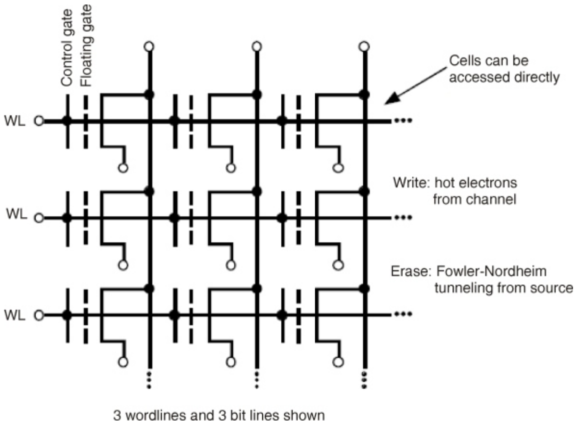

Figure 3. Cell architecture of a NOR flash memory

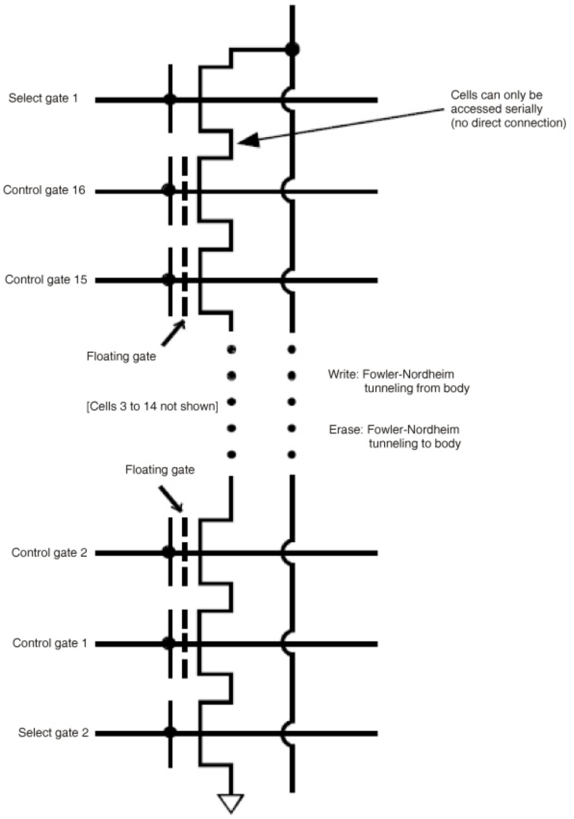

Figure 4. Cell architecture of a NAND flash memory organized in 16-bit stacks

in the stack, an architecture that results in inherently slower cell access. Cells in the NAND structure require higher voltages – typically 20 V for erasing and writing than the ~12 V of the NOR structure.

The overall architecture of either type of flash memory is very complex. Reading can be done relatively rapidly for either cell architecture using conventional circuitry for access and readout. However, erasing and writing are very slow operations (in the order of milliseconds) compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks, allowing erasing and writing to be done at the block level. Internal registers and buffers provide temporary storage for pages of data, allowing more transparent interface. A write state machine and a command state machine are used to control the complex sequences of operations that are needed. A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations.

Because of this complexity, flash memories can not be treated as simple memories. It is quite challenging to determine how they respond in radiation environments.

The main goal of research is to examine the theoretical and experimental radiation resistance of flash memories and the limits forecast of their applicability. Methods to protect these types of memory are the main tasks of the research.

NUMERICAL SIMULATION OF THE INTERACTION OF RADIATION AND MATERIALS APPLYING MONTE-CARLO METHOD

The development of computers and improvement of their performance and features have led to the extension of implementation of simulation techniques from radiation and nuclear physics to other fields of science and technology. Although the application field of Monte-Carlo methods extended to almost all areas, this technique remains a very important and very much applied in radiation physics [8, 9].

Implementation of Monte-Carlo methods in radiation physics is based on the fact that the interaction processes of radiation and material are stochastic. The particles emission process of ionizing radiation is random: the moment of nucleus transformation and particles emission as well as the direction of the emission can not be predicted. Types of atoms with which emitted particles interact, the type and intensity of interaction are also random processes. As the Monte-Carlo method is based on the random numbers use, it is convenient for the simulation of these random processes. It is especially suitable in the case of complex geometry, inhomogeneous materials, poly-energy radiation and these problems are commonly encountered in practice [10-12].

Ion beams in the simulations were chosen to correspond to the radiation fields in which electronic components are often located. For the implementation of the Monte-Carlo simulation SRIM software package was used whereby the simulation of the ions passage is derived by comparing the radiation damage caused by atoms displacing in the ONO dielectric and tunnel oxide [13-15]. Dimensions of layers used in the simulations are shown in fig. 5.

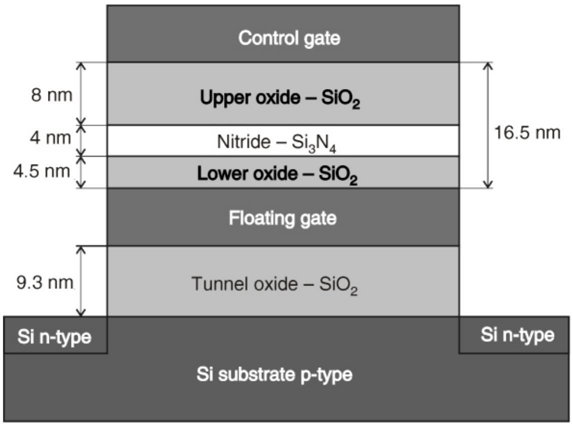

Figure 5. Model of flash memory cell used in the numerical simulation of the ions passage

Simulations were performed with the ion beam, which normally falls on the upper surface of the cell (control gate), where the ONO dielectric is represented by a 3-layer structure with upper and lower oxide (SiO_2) and Si_3N_4 layer between them.

RESULTS AND DISCUSSION

Energy losses of heavy ions regarding atoms displacement have been investigated in low and medium beam energy (~10 keV and ~100 keV, respectively). Figure 6 shows that the vacancy concentration generated by the incident beam and displaced atoms have a general trend of increase regarding the depth of flash memory cell. This can be explained by the preferential relocation of atoms forward (in the direction of the

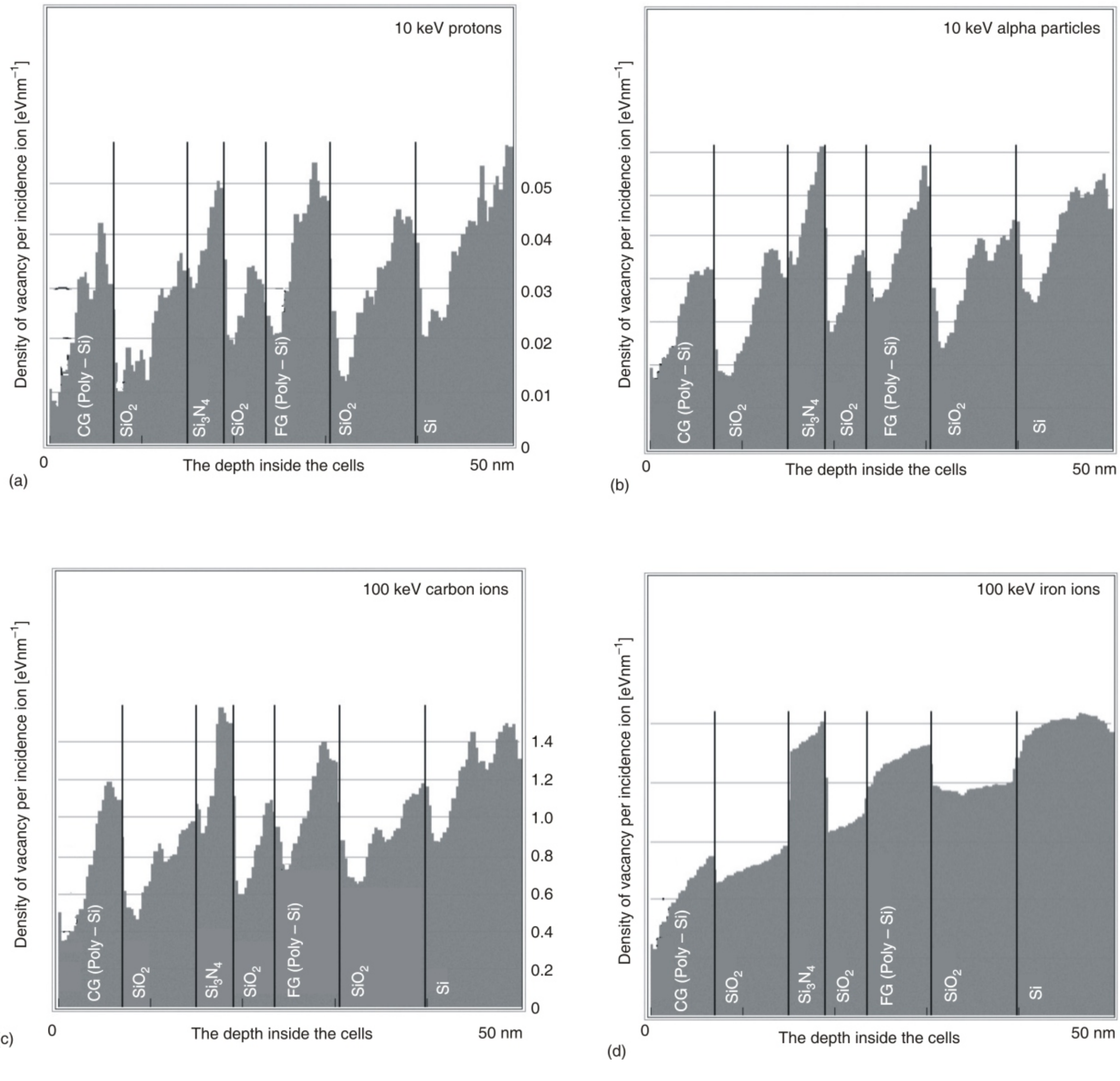

Figure 6. Vacancy distribution generated by displacing atoms (expressed per incident ion) for: 10 keV protons (a), 10 keV alpha particles (b), 100 keV carbon ions (c), and 100 keV iron ions (d)

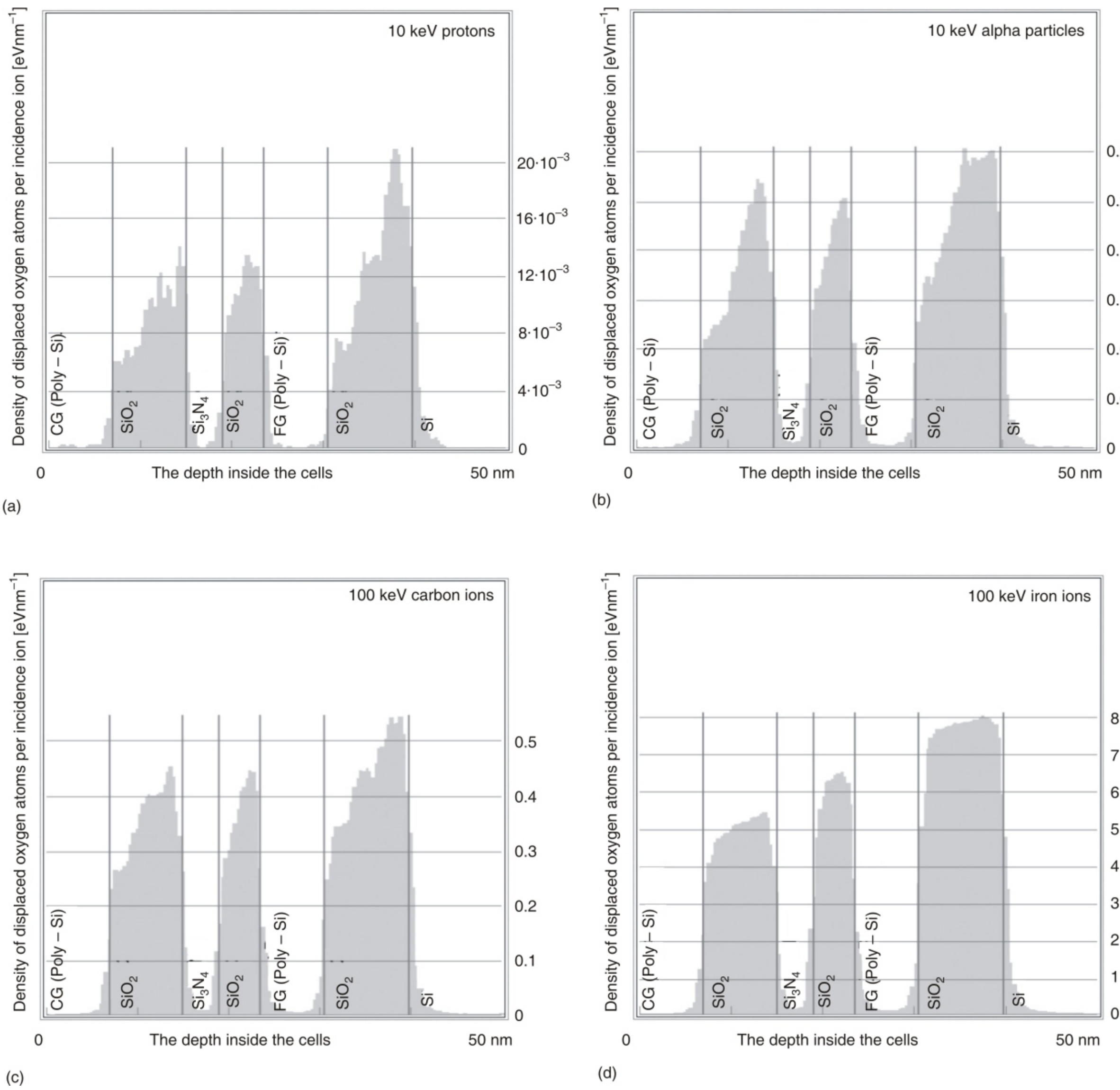

Figure 7. The distribution of the displaced oxygen atoms (expressed per incident ion) for: 10 keV protons (a), 10 keV alpha particles (b), 100 keV carbon ions (c), and 100 keV iron ions (d)

beam) and the fact that dislocation interactions dominate at the end of the path of displaced atoms. A striking increase of the vacancy concentration on the distinguish surface layers of cell is attributed to the existence of the energy barrier at the junction of two materials, which makes difficult vacancy transition from one material to another. For all four types of incident ions, the concentration of vacancies is particularly high in the nitride layer of the ONO dielectric which can cause the generation of the electrically active surface complexes on the distinguish surfaces of Si_3Ni_4 and surrounding oxides [16-18].

The concentration of displaced atoms of oxygen is highest in the tunnel oxide (fig. 7).

Displaced atoms and vacancies in the tunnel oxide may with impurities, present in this layer, form defects with the characteristics of electronic and cavity traps. The presence of defects in the tunnel oxide allows electrons to pass through the potential barrier between the floating gate and the substrate, creating a leakage current. At sufficiently high concentration of shallow traps in the oxide, the leakage current can become significant and leads to a change in the logical state of the cell, even in the case of stable permanent defects, it can prevent cell re-programming.

Migration of vacancies and displaced atoms through the tunnel oxide, which is described as the ionic conduction in solid material, arrive to the distinguish surface of the floating gate and the substrate. In this interfacial, displayed by a certain mechanical stress due to the discontinuity of crystal grid, surface states are formed that can affect electrons. In the case surface states act as deep electron traps, they can affect the threshold voltage of the flash cell and can lead to errors during the reading of the cell content. Surface complexes at interfacial oxide/surface represent the scattering centers for electrons in the channel and can reduce drain current, which decreases the access speed to flash arrays of cell.

CONCLUSIONS

An analysis of the effects due to the displacement of atoms was performed using a numerical simulation of the ions passage through the cell of the flash memory. Due to the low thickness, the layers of the flash memory cells are insensitive to ion energies greater than approximately 1 MeV. The simulation of radiation transport, however, shows that for a given type and energy of ions in some layers of the cells a considerable number of displaced atoms and vacancies occur. Damages caused by such displacement, which occur in the structure of flash cells, can affect the whole range of its parameters (threshold voltage, leakage current, access time and time of writing data), as well as prevent the re-programming of the cell. Some types of errors may occur even for devices that are not biased during the time that heavy ions strike occurs. Error detection and correction may be a viable way to recognize this type of failure mechanism, but it is also necessary to understand how and why the errors are generated within the device, as well as weather internal errors in the memory controller will affect their operation in the space.

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AUTHOR CONTRIBUTIONS

Theoretical analysis carried out by M. D. Obrenović and M. Lj. Vujisić. Simulations and calculations were carried out by M. D. Obrenović. All authors analyzed and discussed the results. The manuscript was written by M. D. Obrenović and M. Lj. Vujisić, and the figures were prepared by M. D. Obrenović.

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ЕФЕКТИ ЈОНСКОГ ЗРАЧЕЊА НА ФЛЕШ МЕМОРИЈЕ

У раду се излаже питање поузданости флеш меморија у условима дејства јонизујућег зрачења. На поузданост рада флеш меморије утичу физичко-хемијска ограничења електростатичке природе услед дејства јонизујућег зрачења. Приказани резултати су актуелни због осетљивости меморија на висок степен минијатуризације интегрисаних компонената и све већој улози меморија у системима за управљање соларним ћелијама у космичким летовима у којима ефекти јонизујућег зрачења могу бити такви да доведу до промене меморисаних података или до физичког уништења самих компонената флеш меморија.

Кључне речи: флеш меморија, радијациона отпорност, Монте Карло симулација