The Alternate Arm Converter: a New Hybrid Multi-level Converter with DC-fault Blocking Capability

Michaël M. C. Merlin, *Member, IEEE*, Tim C. Green, *Senior Member, IEEE*, Paul Mitcheson, *Member, IEEE*, David R. Trainer, Roger Critchley, Will Crookes, Fainan Hassan

***Abstract*—This paper explains the working principles, supported by simulation results, of a new converter topology intended for HVDC application, called the Alternate Arm Converter (AAC). It is hybrid between the modular multi-level converter, because of the presence of H-bridge cells, and the 2-level converter, in the form of director switches in each arm. This converter is able to generate a multi-level AC voltage and, since its stacks of cells consist of H-bridge cells instead of half-bridge cells, they are able to generate higher AC voltage than the DC terminal voltage. This allows the AAC to operate at an optimal point, called the "sweet spot", where the AC and DC energy flows equal. The director switches in the AAC are responsible for alternating the conduction period of each arm, leading to a significant reduction in the number of cells in the stacks. Furthermore, the AAC can keep control of the current in the phase reactor even in case of a DC-side fault and support the AC grid, through a STATCOM mode. Simulation results and loss calculations are presented in this paper in order to support the claimed features of the AAC.**

***Index Terms*—AC-DC power converters, emerging topologies, fault tolerance, HVDC transmission, multi-level converters, power system faults, STATCOM.**

I. Introduction

INCREASING attention is being paid to HVDC transmission systems, especially because most of the new schemes are intended to connect remote renewable sources to the grid and the most effective way to do it is to transmit the generated power using HVDC instead of HVAC [1]. For offshore HVDC applications, Voltage Source Converters (VSC) are more suitable than Current Source Converter (CSC) [2], thanks to their black-start capability and ability to operate in weak AC grids, such as a network of wind turbine generators. However, compared to CSC, their power ratings are limited and their efficiency somewhat poorer although recent developments in semi-conductor devices are closing the gap in both cases such that VSCs are becoming economically viable as technological solutions in large HVDC schemes; some of them [3], [4] to be commissioned in the next couple of years.

Since the 1990s, a great deal of research effort has been directed to improving converters primarily to make them more power efficient than the first generation of VSC [5]–[8]. The Modular Multi-level Converter (MMC), published in 1998 for STATCOM application [9], published in 2003 for HVDC Power Transmission [10] and followed up in [11]–[13], brought several new features to VSC. It replaced the series-connected IGBT in each arm of the 2-level converter by a stack of half-bridge cells which consist of a charged capacitor and a set of IGBTs. Given that the voltage of each cell is small compared to both the AC and DC voltages, a large number of cells are placed in series in each stack, resulting in the creation of a voltage waveform with numerous steps. This characteristic has two main consequences: (i) the generated AC current is very close to a sine wave and no longer requires any filtering, thus saving the implementation of bulky and costly AC filters and (ii) the converter does not rely on high-frequency PWM to syntheses voltage waveforms, thus greatly reducing the switching loss and thereby improving the overall efficiency of the converter.

Notwithstanding the advantages brought by this new generation of converter, there are some aspects that can still be improved. The avoidance of the AC filter means that the cells are now one of the bulkiest components of the converter station and cell format requires a physically large capacitor in addition to the set of IGBTs. Half-bridge cells are normally used in preference to H-bridge cells (both illustrated in Fig. 1) in order to reduce the number of devices in conduction at any time and therefore reduce the conduction power loss. Even if this choice is justified by the large cost associated with the power losses, it also means that the converter is vulnerable to a DC-side fault in a similar way to a 2-level converter whereas an H-bridge version would not be. The inability of half-bridge cells to produce a negative voltage results in the conduction of the anti-parallel diodes connected to the IGBTs, thus creating an uncontrollable current path in case of a collapse of the DC bus voltage. Given that DC breakers for high power applications are still under development [14], [15], the lack of other fast protective mechanisms [16] makes this loss of a means to control DC fault current problematic. In [17], the Double Clamped Submodule (DCS) was suggested as a new type of cell to deal with this issue. The DCS connects together two half-bridge cells together into one cell through one additional IGBT and two diodes. This configuration offers the possibility of switching in a reverse voltage, similar to the H-bridge cell, in order to respond to the need for negative stack voltage in case of DC-side fault. However the DCS does not fully

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solve the DC fault issue because (i) only half the available positive voltage can be translated into negative voltage, leaving a voltage deficit from that needed to fully control the current, and (ii) the power losses are increased by 50% compared to using two half-bridge cells during normal operation because of the additional IGBT in the conduction path.

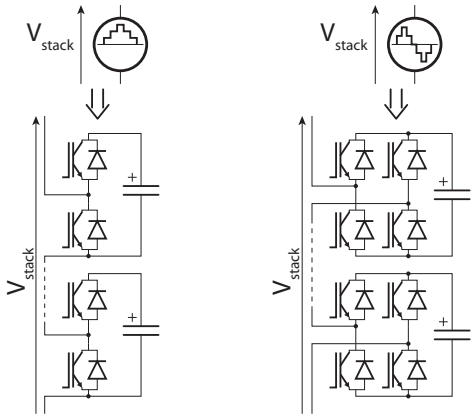

Fig. 1. Electrical schematic of half-bridge cells (left) and H-bridge cells (right).

This paper presents the analysis of a new converter topology, which is part of a new generation of VSCs [18], [19], based on the multi-level approach but also takes some characteristics from the 2-level VSC. As explained through this paper, one of the features of this topology lies in its ability to retain control of the phase current during the loss of the DC-bus voltage, thanks to the presence of H-bridge cells in the arms. The key advantage of this new topology lies in its reduced number of cells, thus it does not compromise on the efficiency of the converter, nor on the number of devices and even saves volume because of the reduced number of cells per arm. A component level simulation of a 20 MW converter is used confirm the claimed characteristics of this new topology.

II. Description of the Topology

A. Basic Operation

Briefly presented in [20], the Alternate Arm Converter (AAC) is an hybrid topology which combines features of the 2-level and multi-level converter topologies. As illustrated in Fig. 2, each phase of the converter consists of two arms, each with a stack of H-bridge cells, a director switch and a small arm inductor. The stack of cells are responsible for the multi-step voltage generation, as in a multi-level converter. Since H-bridge cells are used, the voltage produced by the stack can be either positive or negative, thus the converter is able to push its AC voltage higher than the DC terminal voltage if required. The director switch is composed of IGBTs connected in series in order to withstand the maximum voltage which could be applied across the director switch when it is in the open state. The main role of this director switch is to determine which arm is used to conduct the AC current. Indeed, the key feature of this topology is to use essentially one arm per half cycle to produce the AC voltage. By using the upper arm to construct the positive half-cycle of the AC sine wave, and the lower arm

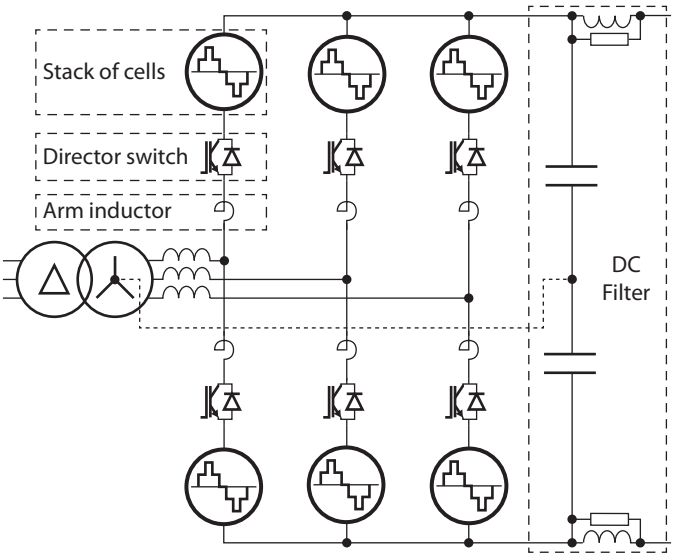

Fig. 2. Schematic of the Alternate Arm Converter, with the optional middle-point connection shown in dashed line.

for the negative part, the maximum voltage that each stack of cells has to produce is equal to half of the DC bus voltage, which is approximately half the rating of the arm of the MMC. The resulting voltage and current waveforms of the cells and reactor switches are illustrated in Fig. 3. The aim of the AAC is to reduce the number of cells, hence the volume and losses of the converter station.

The short period of time when one arm finishes its working period and hands over conduction of the phase current to the opposite arm is called the overlap period. Since each arm has an active stack of cells, it can fully control the arm current to zero before opening the director switch, hence achieving soft-switching of the director switch, further lowering the power losses. Although normally short, the overlap period can provide additional control features such as controlling the amount of energy stored in the stacks, as explained in section II-C.

B. DC Fault Management

One of the important characteristics of this converter is the ability of its arms to produce negative voltage. In fact, the AAC already uses this ability to produce a converter voltage higher than the DC terminal voltage without requiring the opposite arm to also produce a higher than normal positive voltage from its stack of cells, provided that the director switch is suitably rated. This ability is put to use in normal operation when the converter produces a voltage which is higher than the DC bus voltage. It can be extended to the case when the DC bus voltage collapses to a low level, e.g. a fault on the DC-side. Given that enough cells are present in the stacks to oppose the AC grid voltage, the converter is thus able to keep all its internal currents under control, in contrast to the 2-level converter or half-bridge version of the MMC. Furthermore, even if the absence of a DC bus voltage means that it is no longer possible to export active power to the DC-side, it does not prevent reactive power exchange with the AC side. Since

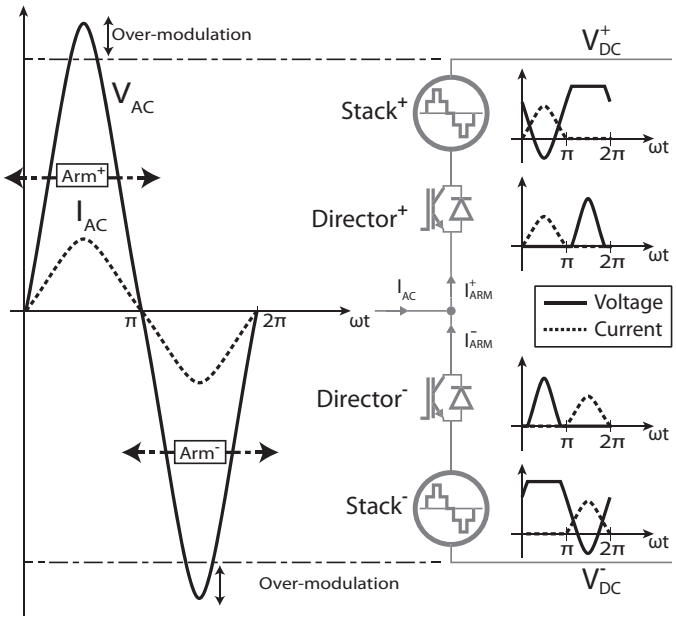

Fig. 3. Idealized voltage and current waveforms over one cycle in a phase converter of the AAC, showing the working period of each arm.

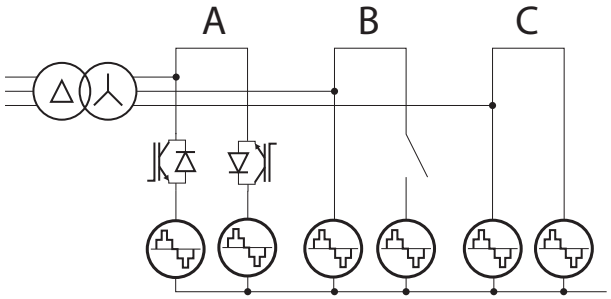

Fig. 4. STATCOM modes of the AAC during a DC-side fault: alternate arms (mode A), single working arm (mode B), dual working arms (mode C).

the arms of the AAC are still operational, the whole converter can now act as a STATCOM, similar to that in [9]. There are some choices over how the director switches are used in this mode, as illustrated in Fig. 4, which lead to different modes that can be achieved by the AAC during a DC-side fault: one arm conducts per half cycle similarly to normal operation, one arm works continuously or the two arms working together, potentially increasing the reactive power capability to 2.0 p.u. This STATCOM-mode of managing the converter during DC fault can help to support the AC grid during a DC outage, in contrast to the worsening effect that can be brought about by other topologies because of their inability to control DC-side fault current.

C. Energy balance

The ability of the converter to generate relatively fine voltage steps comes from its cells and, more specifically, from the charged capacitors inside. However, since the resultant AC current is flowing through them, the charge of these capacitors will fluctuate over time, depending on the direction of the current and the switching states of the cells. Due to the large number of cells, it is easier to look at the amount of energy which is stored by the stacks of cells as a whole. Assuming that this charge is evenly distributed among the various cells, thanks to some rotation mechanisms, the only requirement left to ensure satisfactory operation of the converter is to keep the energy of the stacks close to their nominal value. To achieve this, the converter has to be operated in such way that the net energy exchange for the stacks over each half cycle is strictly zero.

Based on the time functions (1) of $V_{AC}(t)$ and $I_{AC}(t)$:

$$\begin{aligned} V_{AC}(t) &= \hat{V}_{AC}\sin(\omega t) \\ I_{AC}(t) &= \hat{I}_{AC}\sin(\omega t + \phi_{AC}) \end{aligned} \tag{1}$$

The energy exchange corresponds to the difference between the amount of energy coming from the AC side (2) and going to the DC-side (3).

$$\begin{aligned} E_{AC} &= \int_0^{T/2} V_{AC}(t) I_{AC}(t) dt \\ &= \frac{\hat{V}_{AC}\hat{I}_{AC} cos(\phi_{AC}) T}{4} \end{aligned} \tag{2}$$

$$\begin{aligned} E_{DC} &= \int_0^{T/2} \frac{V_{DC}}{2} I_{AC}(t) dt \\ &= \frac{V_{DC}\hat{I}_{AC} cos(\phi_{AC}) T}{2\pi} \end{aligned} \tag{3}$$

By equating these two energies, an ideal operating point is identified as described in Equation 4. This operating point is called the 'sweet spot' and is defined by a ratio of the AC voltage magnitude to DC voltage magnitude.

$$\hat{V}_{AC} = \frac{2}{\pi} V_{DC} \iff V_{line} = \frac{2}{\pi}\sqrt{\frac{3}{2}} V_{DC} \tag{4}$$

It is important to remark that this sweet spot specifies an AC peak voltage higher than the DC terminal voltage, i.e. half the DC bus voltage. The converter is thus required to generate its AC voltage in over-modulation mode, at a level approximately 27 % higher than the DC terminal voltage ($\approx \frac{4}{\pi}\frac{V_{DC}}{2}$). The presence of H-bridge cells is thus fully justified since these cells are required to provide a negative voltage, thus pushing the voltage higher than the DC terminal voltage. By choosing the turns-ratio of the transformer between the converter and the AC grid in order to obtain the AC voltage of the sweet-spot, the converted energy will flow through the converter without a deficit or surplus being exchanged with the stacks.

In practice, discrepancies between the converter and its theoretical model (used to derived Equations (2) and (3) leading to Equation (4)) will lead to a small fraction of the converted energy being exchanged with the stack. To remedy this, the overlap period (i.e. the small period of time when one arm hands over conduction of the phase current to the other arm) can be used to run a small DC current through both arms to the DC-side. This will result in an exchange of energy between the stacks and the DC capacitor, which can be used to balance the energy in the stacks.

D. Number of Devices

The device count in the AAC can be obtained by following a series of steps, given the particular operating mechanism described above. The calculation presented below only gives the minimal requirement under normal operation. Additional margin has to be added to comply with the different operating conditions applying to each project. It is however important to note that the stacks of the AAC can generate as much negative voltage as positive voltage, thus the AAC is able to provide an AC voltage up to 200 % the DC terminal voltage without requiring extra cells.

First, the number of cells is obtained by calculating the maximum voltage that a stack has to produce. Since the two arms of a single phase converter have to support at least the total DC bus voltage, and assuming a symmetrical construction, this maximum voltage has to be at least half the DC bus voltage. Furthermore, given that this topology is intended to have DC-fault blocking capability, the arms should be able to produce at least the AC peak voltage in order to maintain control over the current in the phase reactor with the DC voltage reduced to zero. Therefore, the stacks should be rated to deliver the AC peak voltage. Since the sweet spot defines the AC peak voltage as 27% higher than half the DC bus voltage, the minimum requirement can then be increased up to the AC peak voltage. However, if DC-fault blocking is not a requirement, this voltage can remain at half the DC bus voltage. Furthermore, the maximum voltage of the stacks also defines for how long an arm can stay active beyond the zero-crossing point of the converter voltage in order to provide an overlap period. The longer the overlap period, the higher the voltage that the stack has to produce, hence the more cells are required. once the maximum voltage of the stack is set, the number of cells is directly obtained by dividing this voltage by the nominal voltage of a cell.

Second, the required number of series-IGBTs which form the director switch is determined based on the maximum voltage applied across the director switch, as illustrated in Fig. 3. This voltage is the difference between the converter voltage and the voltage at the other end of the director switch, which is connected to the (non-conducting) stack of cells. The non-conducting stack can be set to maximise its voltage so as to lower the voltage across the director switch, taking care not to reverse the voltage across the director switch. Equation (5) summarises all these arguments and presents the maximum voltage across the director switch. By implementing the sweet spot definition (4) into Equation (5), it yields Equation (6), a function of the DC bus voltage and the peak stack voltage.

$$\hat{V}_{Director} = \hat{V}_{AC} + \frac{V_{DC}}{2} - \hat{V}_{Stack} \quad (5)$$

$$= \frac{4+\pi}{2\pi} V_{DC} - \hat{V}_{Stack} \quad (6)$$

Table I summarises the voltage ratings required of the stack of cells and the director switch given three choices made over the need to block DC fault current and the extent of overlap. In defining these voltages, these choices will also determine the number of number of semiconductor devices in the AAC.

TABLE I
VOLTAGE RATINGS OF THE STACKS AND DIRECTOR SWITCHES

$\hat{V}_{Stack}$	$\hat{V}_{Director}$	Remarks
$\frac{V_{DC}}{2}$	$\hat{V}_{AC}$	No DC-fault blocking and no overlap
$\hat{V}_{AC}$	$\frac{V_{DC}}{2}$	DC-fault blocking and short overlap
$\hat{V}_{DC}$	$\hat{V}_{AC} - \frac{V_{DC}}{2}$	DC-fault blocking and full cycle overlap

The resulting number of cells per stack is given by Equation (7), where (V_{Cell}) the nominal voltage of a cell.

$$N_{Cell} = \frac{V_{Stack}}{V_{Cell}} \quad (7)$$

Equation (8) presents the total number of semiconductor devices (N_{IGBT}) in a 3-phase AAC, with $N_{Director}$ being the number series-IGBTs in the director switch obtained by dividing the maximum voltage of a director switch ($V_{Director}$) by the voltage applied to an IGBT, here assumed to be the same to the voltage of a cell (V_{Cell}).

$$N_{IGBT} = 6 \times (4 \times N_{Cell} + N_{Director}) \quad (8)$$

Using the DC-fault blocking case (given in Table I) and the definition of the sweet spot (4), the total number of semiconductor devices becomes the value in Equation (9).

$$N_{IGBT} = 6\frac{4\hat{V}_{AC} + \frac{V_{DC}}{2}}{V_{Cell}} \approx 18.28\frac{V_{DC}}{V_{Cell}} \quad (9)$$

III. Simulation Results

A. Model Characteristics

In order to confirm the operation of this new topology, a simulation model has been realised in Matlab/Simulink® using the SimPowerSystems toolbox. The characteristics of this model have been chosen in order to reflect a realistic power system, albeit at medium voltage, and key parameters are summarised in Table II. The transformer interfacing the AC grid and the converter has its turns-ratio defined such that the converter operates close to the sweet spot AC voltage, as defined in section II-C. The number of cells chosen for each stack follows the second case from Table II such that DC-side fault blocking is available. A small additional allowance was made so that the converter can still operate and block faults with an AC voltage of 1.05 p.u. The choice is therefore for 9 cells charged at 1.5 kV each per stack. The minimum number of cells for operation without overlap (sweet spot operation only) and without fault blocking would be 7 cells. The choice of 9 cells per stack allows the AAC to operate with a 1 ms overlap period which is sufficient to manage internally the energy storage within the current rating of the IGBTs (1.2 kA). Finally, a DC filter has been fitted to the AAC model, as illustrated in Fig. 2, and tuned to have both a critical damping and a cut-off frequency at 50 Hz; well below the first frequency component expected on the DC-side which is a 6-pulse ripple (i.e., 300 Hz in this model).

TABLE II
CHARACTERISTICS OF THE AAC MODEL

Characteristics	Values
Active power	±20 MW
Reactive power	±5 MVAr
DC bus voltage	20 kV
Grid-side AC voltage	11 kV
Converter-side AC voltage	15.56 kV
Phase reactor	3.9 mH
Arm inductor	0.5 mH
DC Filter inductors (x2)	6 mH
DC Filter inductors (x2)	6 mH
Quality factor of DC inductors	100
DC Filter capacitors (x2)	1.68 mF
Total energy in DC bus capacitors	168 kJ
DC Filter resistors (x2)	2.66 Ω
Overlap period	1.0 ms
Cell voltage	1.5 kV
Cell capacitor	4.0 mF
Stacks	9 cells
Director switches	7 IGBTs
Converter voltage waveform	**19 levels**
Total number of semiconductor devices	**258 IGBTs**

B. Performance under normal conditions

Based on this model, the behavior of the AAC was simulated under normal conditions in order to test its performance. In this section, the converter is running in rectifier mode, converting 20 MW and providing 5 MVAr capacitive reactive power. Figure 5 shows the waveforms generated by the AAC in this simulation.

First, the converter is very responsive. Second, the waveform of the phase current in the AC grid connection is high quality with only very low amplitude harmonics, as shown by the Fourier analysis in Fig. 6. Third, the DC current exhibits the characteristic 6-pulse ripple inherent in the rectification method of this converter, but attenuated by an inductor placed between the converter and the DC grid. Fourth, this rectification action of the current is particularly observable in the fourth graph which shows the arm currents in phase A, indicating when an arm is conducting. Finally, the fifth graph presents the average voltage of the cells in both stacks of phase A, with their off-state voltage being controlled to stay at the reference value of 1.5 kV.

The voltage and current waveforms have been post-processed together with the switching commands sent to the converter from the controller, in order to determine the generated power losses. For this example, all the semiconductor devices were based on the same IGBT device [21] from which the losses curves have been extracted to compute the energy lost through conduction and switching at every simulation time step (2 μs). A simulation of 1.5 s was used in which the first 0.5 s was ignored in order to focus only on the steady state

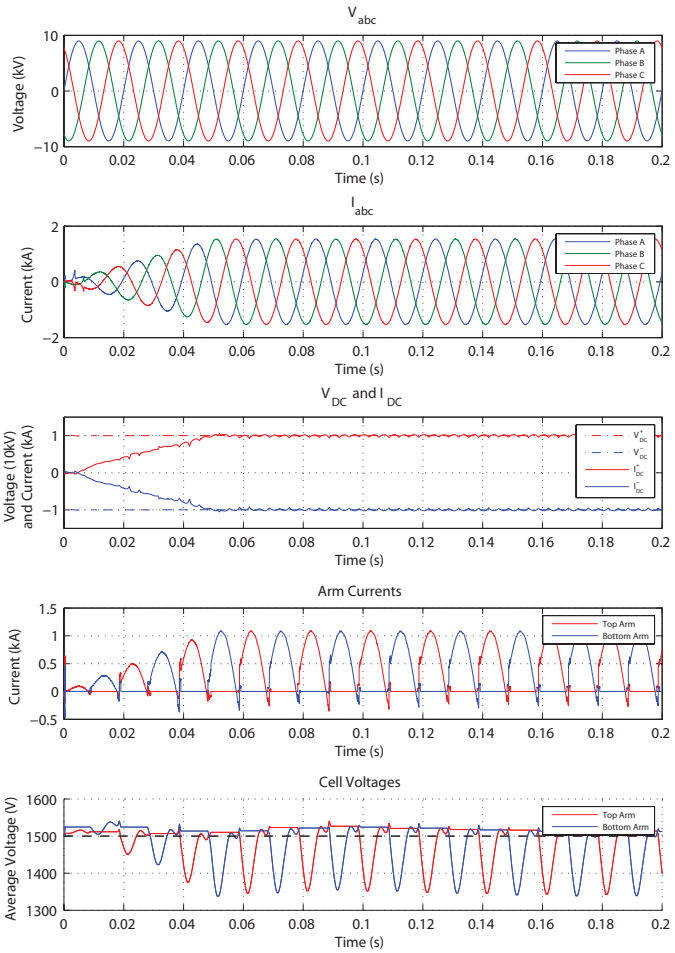

Fig. 5. Simulation results of a 20 MW AAC model running in rectifier mode under normal condition.

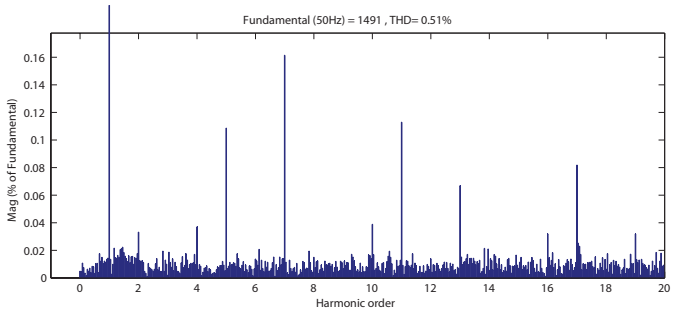

Fig. 6. Fourier transform of the grid-side AC current generated by the AAC.

portion. The results obtained are summarized in Table III.

As can be observed in Table III, the switching loss relative to the total power losses is low, as could be expected from a multi-level converter, meaning that the conduction loss is dominant. However, the conduction loss is kept small despite the use of H-bridge cells by the fact that the stacks do not have to be rated for the full DC bus voltage because of the presence of the director switches; the conduction loss of a director switch device being less than that of an H-bridge cell. The director switches do not incur any switching loss thanks to the soft-switching capability of the arms (through controlling

TABLE III
BREAKDOWN OF THE POWER LOSSES AT 20 MW

Stack power losses	**Value**
Conduction	103 kW
Switching	26 kW
Reverse Recovery	10 kW
Director switch power losses	**Value**
Conduction	36 kW
Switching	0 kW
Reverse Recovery	0 kW
DC-filter power losses	**Value**
Conduction	56 kW
Total Power Losses	**191 kW**
Efficiency	**98.85 %**

the arm current to zero before opening of the director switch). Finally, a large amount of the power losses comes from the DC inductor but is in fact exacerbated by the small scale of this model (e.g. 20 MW) which emphasises more the scalability in voltage (i.e. the number of devices in series) rather than in current (resistive losses in the DC inductor).

C. Robustness against AC faults

Since the AAC is a type of VSC, it does not rely on a strong AC voltage to operate. As a consequence, the AAC is able to cope with AC-side faults. Fig. 7 shows the results of the simulation where the AC voltage drops to 0.3 p.u. retained voltage between 0.20 s and 0.35 s, similar to a major fault on the AC grid. The converter switches into voltage control mode and supplies 1.0 p.u. current of capacitive reactive power. When the AC voltage returns to its nominal value, the converter switches back to normal operation and full power is reapplied with a ramp function over 50 ms.

Several observations can be made. First, the converter is able to react quickly to the fault and reduces the power as a consequence. Second, the quality of the AC current waveform deteriorates during the fault, mainly because fewer levels are needed to construct the reduced converter voltage waveform. Third, the cell capacitors display more voltage fluctuation during the fault because the converter is running far away from the sweet spot but does not prevent the AAC from generating the reactive power during the outage.

D. DC-fault blocking capability

The intended ability to block current during DC faults was tested by simulating the temporary reduction of the DC bus voltage to zero, equivalent to a DC-side fault. The graph in Fig. 8 show the waveforms generated during this simulation, where the DC bus voltage is lost between 0.20 s and 0.35 s followed by a ramp up back to normal operations.

When observing the sequence of events during this simulation, it can be seen that, when the DC voltage collapses to zero,

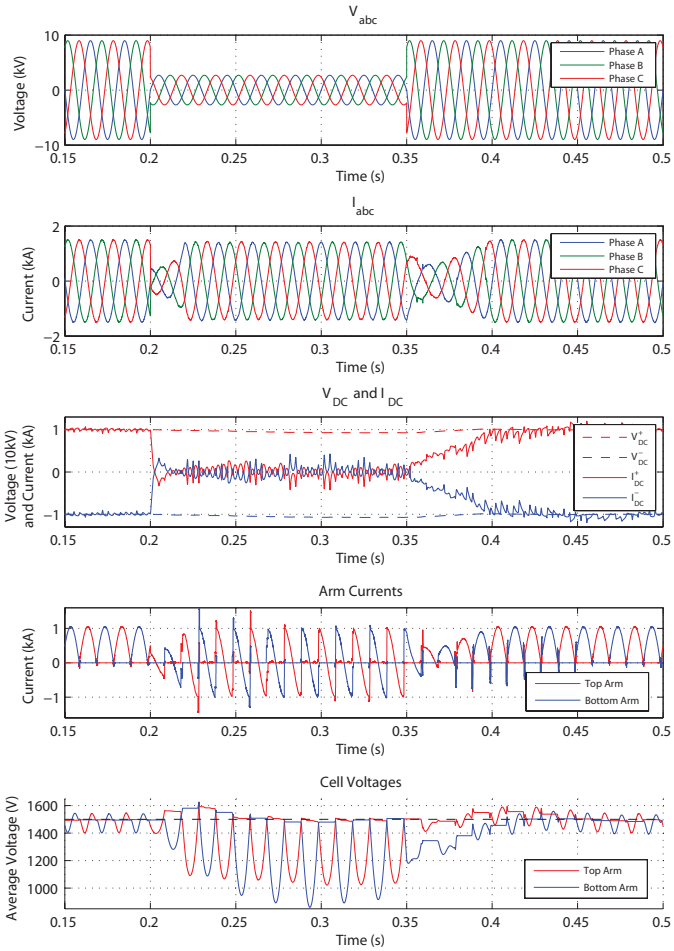

Fig. 7. Simulation results of a 20 MW AAC model running in rectifier mode when an AC-side fault occurs between 0.20 s and 0.35 s.

it leads to a rapid discharge of the DC bus capacitor which is outside the control of the converter in opposition to the cell capacitors. At the moment of the fault, the DC filter behaves similarly to an RLC circuit with a pre-charged capacitor (20 kV) and inductor (1 kA), resulting in a theoretical peak current of 5.1 kA which is close to the current spike observed in the third graph. However, the fourth graph shows that the converter is able to keep control of the AC reactor current and its arm currents such that no fault current flows from the AC-side to the DC-side, demonstrating the DC-fault blocking capability of the converter itself.

Since the converter is no longer able to exchange active power with its DC bus voltage at zero, the reference for active current is set to zero and effectively controls its current to zero. Then from 0.25 s, the AAC starts injecting 1.0 p.u. reactive power, thus acting as a STATCOM supporting the AC grid during the outage of the DC link. The stack in conduction at the instance of the fault sees its stored energy rise because it temporarily stores the still incoming energy (while the active current is being reduced), but converges back to its reference value over the period when the fault is present. Finally, when the DC voltage has returned (i.e. the fault is cleared, the converter is able to resume operation quickly. This simulation verifies the ability of the AAC to cope with DC-side fault and

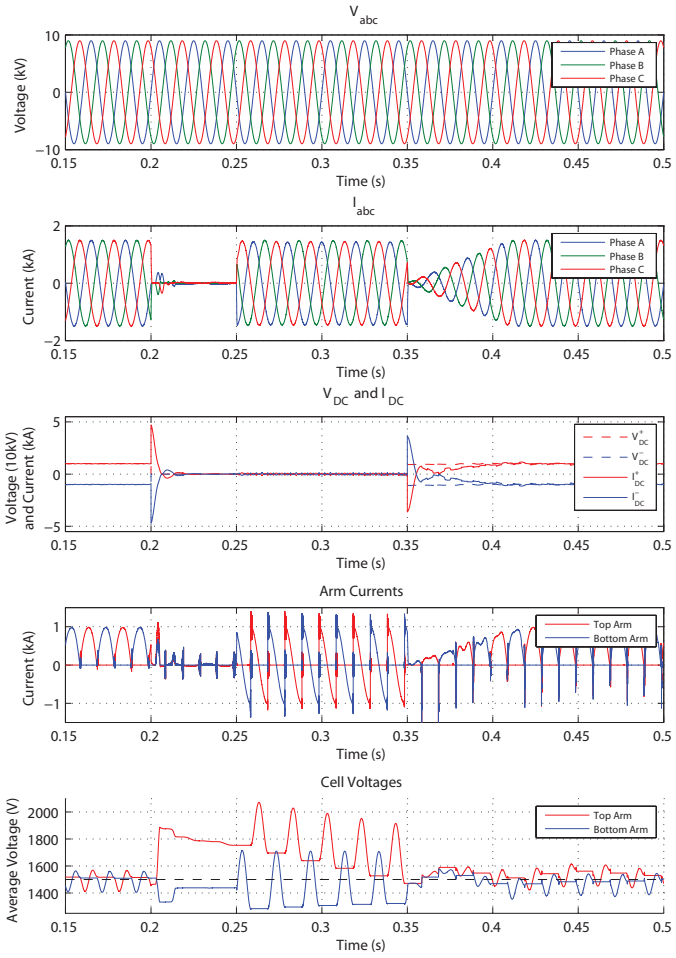

Fig. 8. Simulation results of a 20 MW AAC model running in rectifier mode when an DC-side fault occurs between 0.20 s and 0.35 s.

even run as a STATCOM to support the AC grid, in the absence of DC bus voltage. Furthermore, in the current simulation, the AAC keeps the same alternating mechanisms of its arms (mode A in Fig. 4) but, by activating both arms continuously (mode C in Fig. 4), the maximum reactive power could go up to 2.0 p.u. current.

IV. Conclusion

The Alternate Arm Converter is a hybrid topology between the 2-level converter and the modular multi-level converter. By combining stacks of H-bridge cells with director switches it is able to generate almost harmonic-free AC current, as does the modular multi-level approach, and by activating only one arm per half-cycle, like the 2-level converter, it can be built with fewer cells than the MMC.

Because this topology includes cells with capacitors which are switched into the current path, special attention needs to be paid to keeping their stored energy storage (equivalently, the cell capacitor voltage) from drifting away from their nominal value. By examining the equations which govern the exchange of energy between the AC and DC-sides, an ideal operating condition has been identified, called the "sweet spot". When the converter is running at this condition, the energy levels of the stacks return to their initial values at the end of each cycle without any additional action. In cases where this equilibrium is not attained, an overlap period can be used to run a small DC current in order to balance the stacks by sending the excess of energy back to the DC capacitors.

A discussion of the total number of devices required by this topology has also been presented. Providing DC-fault blocking and overlap both require more than the bare minimum number of cells and adding cells does lead to increased conduction power loss which gives rise to a design trade-off.

Simulations of a small scale model show that this converter is able to deliver both good performance under normal conditions, in terms of efficiency and current waveform quality, and also provide rapid responses in the case of AC- or DC-side faults. Its ability to keep control of the current even during DC faults is a significant advantage, especially in multi-terminal HVDC applications, and can be extended into STATCOM operation in order to support the AC grid during the outage, by providing potentially up to 2.0 p.u. reactive current.

Acknowledgment

The authors gratefully acknowledge the financial support provided by Supergen FlexNet Research Consortium (ESPRC grant EP/E04011X/1) and the opportunity to study and publish on this circuit provided by Alstom Grid.

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