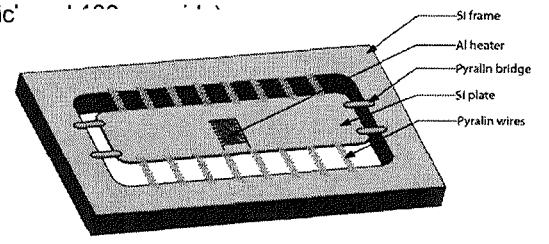
Fabrication of a thermally isolated and pre-amplified transistor module with polyimide micro-wires for cryogenic detectors

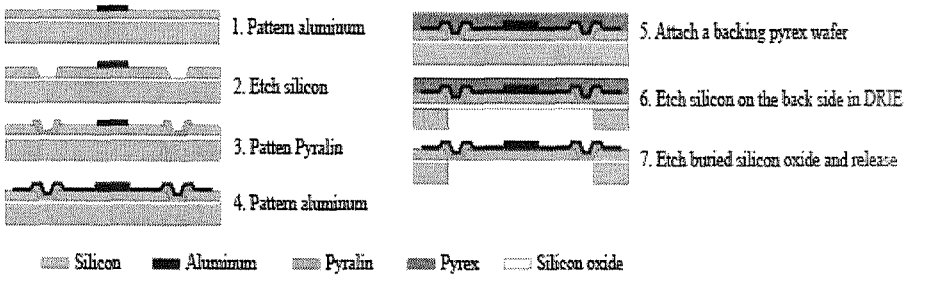
Lance Oh, Christine Allen, Richard Kelley

Objective: To develop a fabrication process to suspend a JFET mechanical module with polyimide micro-wires and bridges.

Design: The JFET module consists of a suspended silicon plate, a silicon frame, polymer bridges made of Pyralin, Pyralin micro-wires, and aluminum heaters as shown in Fig. 1. The JFETs are fabricated within the silicon plate (6 um thick) thus to isolate the heat from the heaters. The silicon frame is 350 um thick and used as a mechanical support and a substrate. The plate is suspended on the frame with four Pyralin bridges (2.5 um thic

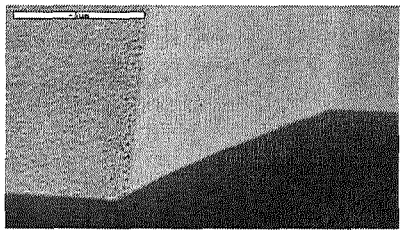


Process sequence:

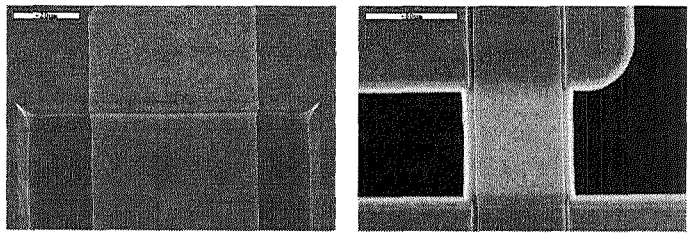


Discussion:

1. Anisotropic silicon etch: Due to subsequent processes of spin-coating of Pyralin film and deposition of aluminum, sloped side walls are desired for the continuity of the films. we developed a method to achieve this in a conventional RIE system using SF6 and O2 gases for etching silicon and photoresist, respectively.



2. Anisotropic polyimide etch: Pyralin is etched with an O2 gas in a RIE system.
3. Continuity of aluminum electrode:



4. Releasing of the chip: Final chips are glued to a Pyrex backing wafer with a transparent Crystalbond 509 wax, which dissolves in acetone. However, the Pyralin 2809 (HD Microsystems swells 10% in acetone and 3% in methanol. This creates a bad adhesion between Pyralin and aluminum films. Thus, the final chip is released in a wax stripper, Crystalbond 509-s, rinsed in isopropanol, and air-dried.

Fabrication of a thermally isolated and pre-amplified transistor module with polyimide micro-wires for cryogenic detectors

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Introduction

For use in cryogenic applications such as bolometer and x-ray microcalorimeter arrays, pre-amplifying Junction Field Effect Transistors (JFETs) are often required for the read-out electronics. The optimum operating temperature of the JFETs is 130 Kelvin while the cryogenic detectors operate in the milli-Kelvin range. Thus, the JFETs must be heated up but thermally isolated from the surrounding cryogenic instruments.

In the past, the thermal isolation was accomplished by suspending the JFETs with low conductance wires such as manganium or stainless steel on a Kevlar support platform [1]. This also achieved electrical connections. However, this assembly required manual soldering work, which could raise a reliability issue for the cryogenic applications.

In order to eliminate the manual work, polyimide micro-wires were developed [2]. The wires must be of sufficient length to decrease the heat load and in tension to prevent microphonic noise from vibration of the wires: the polyimide wires were patterned into "S"shaped curves over a thin metal wires such as aluminum, titanium, or niobium. The bilayer of the films were then suspended by etching silicon substrate thus to make freestanding air bridges (enough explanation?).

In this paper, we present a method to fabricate micromachined JFET mechanical modules suspended by polyimide Pyraline micro-wires and heated up with built-in aluminum micro-heaters.

Design

The JFET module consists of a suspended silicon plate, a silicon frame, polymer bridges made of Pyralin, Pyralin micro-wires, and aluminum heaters as shown in Fig. 1. The JFETs are fabricated within the silicon plate (6 um thick) thus to isolate the heat from the heaters. The silicon frame is 350 um thick and used as a mechanical support and a substrate. The plate is suspended on the frame with four Pyralin bridges (2.5 um thick and 100 um wide).

The aluminum electrodes are patterned over the Pyralin micro-wires. The aluminum etch also creates three micro-heaters on the suspended silicon plate. The aluminum heater wires are 10 um wide and 0.5 um thick.

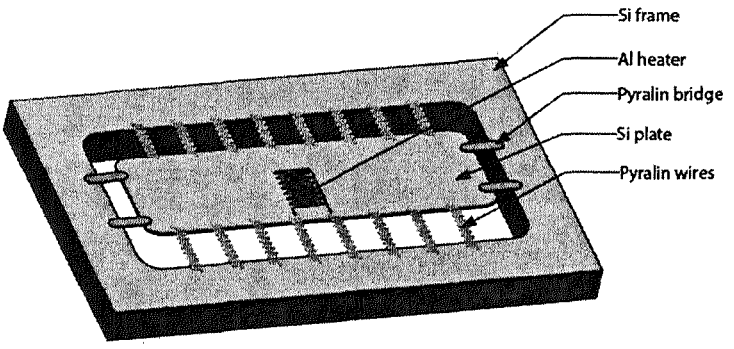

Figure 1. 3D drawing of the a simplified mechanical module that shows a silicon suspended plate, a silicon frame, polymer bridge, Pyralin micro-wires, and aluminum heaters.

Fabrication

The module is fabricated on silicon-on-insulator (SOI) wafers. The fabrication of JFET on the SOI wafer was well characterized and reported by ????? (reference). Thus, its fabrication steps are omitted here. Our process after the JFET fabrication begins with sputter depositing a 5000 Å thick layer of aluminum alloyed with 1% silicon. The aluminum is photolithographically patterned and etched to form the heater wires. The aluminum is then alloyed in a furnace to make an ohmic contact to the JFETs. Anisotropic silicon etching was then performed with sulfur hexafloride and oxygen gases in a reactive ion etching (RIE) system (March CS-1701). A 2.5 um thick layer of polyimide Pyralin 2809 (HD Microsystems) is spin-coated at 4000 rpm. The Pyralin is first baked at 150 °C for 25 min. Then, it is cured at 300 °C for 1 hour. The Pyralin film is etched with an oxygen gas in the RIE system using a thick resist, SPR 220-7 as a mask. Another 5000 Å thick layer of aluminum is deposited with an e-beam system and patterned to make electrical contacts to the JFETs. The SOI wafer is bonded to a backing Pyrex wafer using a transparent wax (Crystalbond 509). The back side of the wafer is patterned with a photoresist (AZ 4620) and then deep etched to a buried silicon oxide in a DRIE system. Finally, the mechanical module gets released in a wax stripper (Crystalbond 509-s), rinsed in isopropanol, and air-dried.

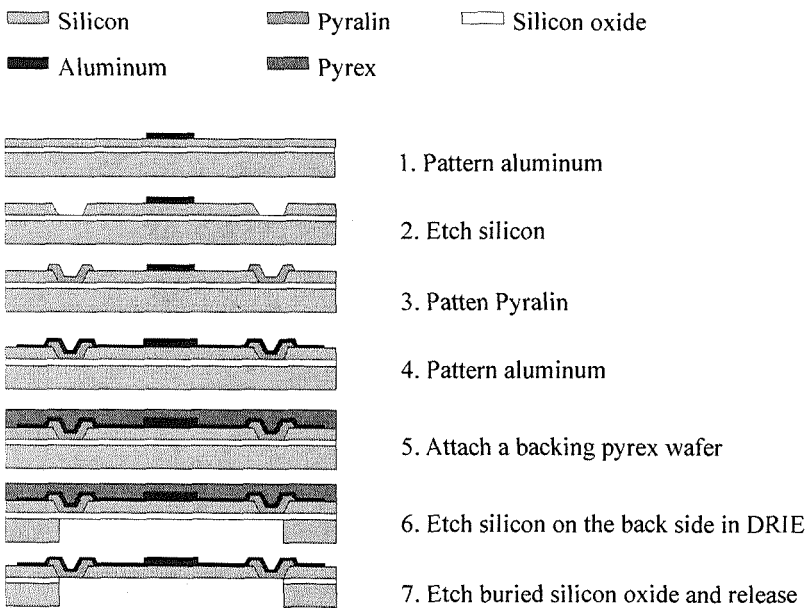

Figure 2. Process sequence of the JFET module.

Discussion

Anisotropic silicon etch:
Due to subsequent processes of spin-coating of the Pyralin film and e-beam deposition of aluminum, sloped side walls are desired for the continuity of the films. The silicon etch in aqueous potassium hydroxide is well known to achieved the sloped side wall. However, the solution attacks almost all the photoresists and aluminum, which are required prior to the silicon etch process. Thus, we developed a method to achieve this in a conventional RIE system using sulfur SF6 hexafloride and oxygen gases for etching silicon and photoresist, respectively.

For a masking layer, the SPR 220-7 was used. A smooth surface profile of the photoresist was obtained using the photoresist reflow technique; the photoresist was hard-baked at 110 °C on a hotplate for 8 min to melt the photoresist to form a hemispherical profile by surface tension. The sloped side wall was etched with the SF6 gas while the edges of the photoresist were gradually etched with an oxygen gas. In other words, the receding edges of the photoresist during the silicon etch make the sloped side walls.

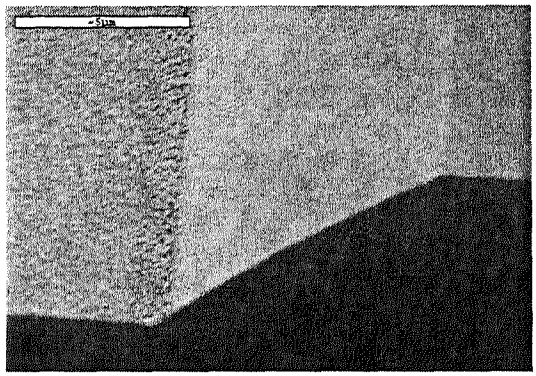

Figure 3. SEM picture of the sloped side walls of silicon

Anisotropic polyimide etch:
Similarly, the Pyralin is etched with an oxygen gas in the RIE system using the same technique above and the sloped side wall was fabricated.

Continuity of aluminum electrodes:
The aluminum film was deposited in an e-beam system while the wafer is tilted at 45 ^{o} and rotates 360 ^{o} at 10 rpm during the metal deposition; this setup is performed to have a uniform thickness of the film over the Pyralin and silicon patterns. Using a photoresist, Shipley 1811, the aluminum electrodes are patterned over the Pyralin wires. The photoresist is thicker at the corners and edges of the silicon side walls than that on a flat surface. Thus, the UV exposure at the corners and edges needs three times the exposure time of the flat surface. In order to achieve this, double exposure was only performed only at these areas with a separate chromium mask. After the etching the aluminum electrodes and stripping the photoresist, the continuity of the electrodes was confirmed with a multimeter and a SEM image as shown in Fig. 3.

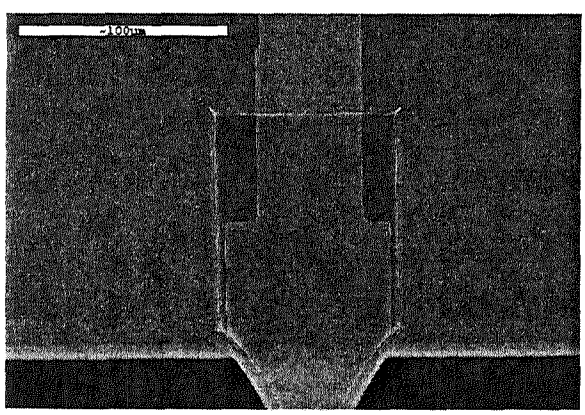

Figure 3. SEM picture of continuous aluminum electrodes over Pyralin wire.

Releasing of the chip:
The wax is known to dissolve in acetone. However, the Pyralin 2809 (HD Microsystems) swells ___% in acetone and ___% in methanol in ___ hours, which were measured with a profilometer by measuring thicknesses. The swelling results in a bad adhesion between the Pyralin and aluminum films. We learned that the film does not swell in the wax stripper, Crystalbond 509-s, and isopropanol. Thus, the Crystalbond 509-S was chosen to dissolve the wax and to release the chip, and isopropanol is used to rinse the chip.

Conclusion

We implemented the polimide micro-wires and bridges to thermally isolate the JFETs. The thermal isolation was achieved by suspending the silicon plate. For this suspension, we developed anisotropic silicon and polyimide etches using a conventional RIE system. We found out that the Pyralin manufactured by HD Microsystems swells its thickness and then result in bad adhesion with aluminum in acetone and methanol. Thus, the mechanical modules were released from a backing wafer bonded with the transparent wax (Crystalbon 509) in the wax stripper (Crystalbond 509-s), rised in isopropanol, and air-dried.

Future work

All these steps will be implemented with complete JFET fabrication processes.

Reference

[1] D.A. Harper et al, Proc. SPIE 4014, 43 (2000).

[2] C.A. Allen Compliant system of Polyimide microwires for cryogenic detector applications