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Fabrication of an Antenna-Coupled Bolometer for Cosmic Microwave Background Polarimetry

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Abstract. We describe the development of a detector for precise measurements of the cosmic microwave background polarization. The detector employs a waveguide to couple light between a pair of Mo/Au superconducting transition edge sensors (TES) and a feedhorn. Incorporation of an on-chip ortho-mode transducer (OMT) results in high isolation. The OMT is micromachined and bonded to the microstrip and TES circuits in a low temperature wafer bonding process. The wafer bonding process incorporates a buried superconducting niobium layer with a single crystal silicon layer which serves as the leg isolated TES membrane and as the microstrip dielectric. We describe the micromachining and wafer bonding process and report measurement results of the microwave circuitry operating in the 29-43GHz band along with Johnson noise measurements of the TES membrane structures and development of Mo/Au TES operating under 100mK.

Keywords: Cosmic Microwave Background Polarization, wafer bonding, polarimeter.
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INTRODUCTION

At Goddard Space Flight Center, we have been developing the technology for an innovative approach to measuring the cosmic microwave background polarization (CMB) in which the excellent beam control possible with feedhorns is combined with the sensitivity provided by transition edge sensor (TES) bolometers. We report the fabrication of the prototype polarimeter operating in the ~29-45 GHz band. The approach described can be extended up to 150 GHz. The design is optimized to meet the challenges of low systematic errors and scalability to large arrays necessary for a space mission to measure the polarization of the CMB to search for inflation.

To meet the requirements for such a mission, we employ a bonded wafer fabrication process, described here, that allows the use of 5 µm single crystal silicon as a dielectric for the superconducting microstrip circuitry. At cryogenic temperature single crystal silicon dielectric loss is much lower than other dielectric materials. Additionally, the same silicon layer is used as a low stress membrane for the antenna support and as a well characterized thermal link for the TES membranes. The final detector structure is integrated at the wafer level and consists of a conformally metalized three dimensional waveguide bonded to the planar microstrip circuitry and TES bolometers.

SYSTEM OVERVIEW

Incident radiation is collected using a feedhorn with integral circle to square waveguide transition. The feedhorn is designed to produce highly symmetric beams with low cross-polarization. The detector circuit is mounted in a metallic housing which is coupled to the feedhorn and the backshort with two photonic chokes. This configuration gives the equivalent of a direct metal connection between the housing and the feedhorn without the need for thermal contact thus allowing the feedhorns to be at a different temperature than the detector. A schematic of the system is shown in figure 1.

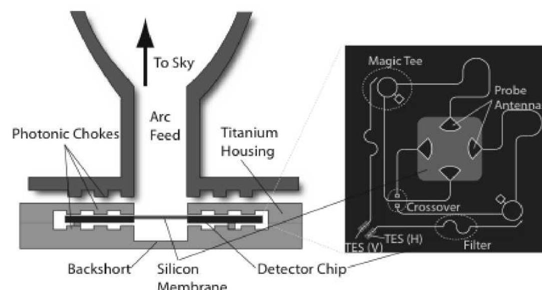

FIGURE 1. System configuration showing circular to square feedhorn, photonic chokes and detector chip layout. For further control of systematics, this approach also offers the advantage of being able to define the bandpass using on chip microstrip filters.

The detector chip consists of a metalized square waveguide bonded to a planar niobium (Nb) superconducting microstrip circuit on 5 μm silicon substrate. The circuit employs a thin silicon membrane that supports the probe antennas which couple the radiation from the waveguide into microstrip. Two orthogonal polarization modes are coupled into superconducting microstrip by a highly symmetric wide bandwidth planar orthomode transducer (OMT). A pair of antennas is used to couple each of the two linear polarizations into the circuit. For each polarization the signals from the two antennas are combined by a hybrid magic-T. An on-chip filter provides band definition[3]. A via-less crossover allows the microstrip lines containing the vertical and horizontal signals to cross in the plane of the detector chip using the existing microstrip layer and its ground layer.[2] Finally, each polarization signal is terminated in a resistor that is thermally coupled to a Mo/Au TES bolometer.

DETECTOR FABRICATION

Fabrication of the chip employs a hybrid two wafer approach which allows for process optimization of the planar microstrip and other associated structures. In particular it enables very low loss single crystal silicon dielectric layer for superconducting microstrip circuitry. A low temperature wafer level bonding process lends itself to scalability up to array level fabrication.

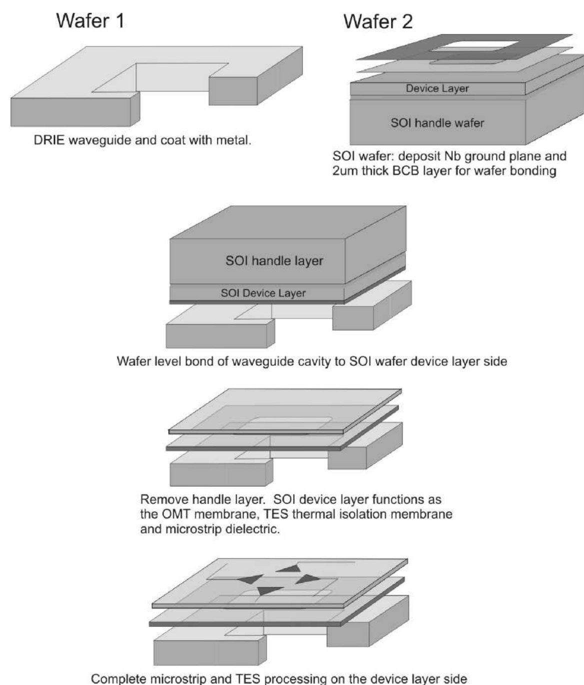

FIGURE 2. Detector chip fabrication

The detector chips are fabricated in the process shown in figure 2. The first wafer is a standard double side polished silicon that makes up the waveguide feature. Through holes in this wafer are etched using a standard deep reactive ion etching (DRIE) process. The through holes define the square waveguide, the antenna membrane, the magic-T membrane, the via-less crossover membrane, and the leg isolated TES bolometer membrane. The waveguide is aligned to the <100> crystalline plane. After DRIE a short etch in KOH chamfers the edge of the waveguide by selectively etching along the <111> plane. The front, back and sidewalls of the waveguide are metalized by gold in an angle deposition electron beam evaporation step.

The chamfer and angle evaporation enables conformal metal coating between the vertical sidewall of the waveguide and the horizontal front and back side of the chip. Figure 3 is a scanning electron micrograph of the metalized waveguide sidewall. It is important to stress that this approach guarantees the complete coverage of the waveguide wall with metal without the need to accurately control the deposition angle.. This would be very challenging if implemented in a standard DRIE step from the back side of the wafer.

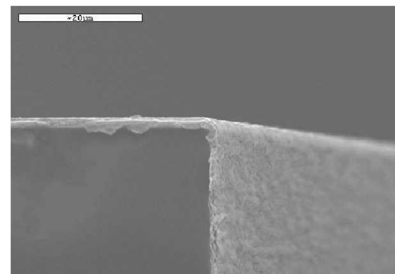

FIGURE 3. Waveguide wafer sidewall after chamfer etch and conformal metallization

The second wafer is a silicon on insulator (SOI) wafer with a 5μm thick device layer, 3000A buried oxide and a 350um thick handle layer. The silicon device layer serves two major functions in the circuit. First, it is a low stress mechanical support for the OMT antenna membrane and the thermally well isolated TES membrane structure. Second, it is the dielectric layer for the niobium microstrip circuitry with well characterized microwave properties. Single crystal silicon has been chosen for its low loss. Loss tangents less than 6×10^{-5} have been measured for similar materials at 40GHz and cryogenic temperatures. Fabrication of the second wafer starts with deposition and patterning of the niobium ground plane on the 5μm silicon device layer side. Next a polymer adhesive is applied to the niobium ground

plane and patterned. The waveguide wafer and the SOI wafer are then aligned and bonded.

Wafer Bonding

Wafer bonding is a critical step in the detector fabrication. The bonding must be done at low temperature < 250C in order to not degrade the niobium ground plane superconducting properties. The bonding material must be compatible with standard process chemistries and also definable by photolithography. For polymer materials, low out-gassing is also required and additionally, for high alignment tolerance, minimal flow during bonding is required. The final cured film must also have low stress. We have chosen Benzocyclobutene (BCB) from Dow Chemical Company as the intermediate polymer for adhesive wafer bonding. BCB has been successfully demonstrated to produce strong wafer bonding for three-dimensional integrated circuits. Its insensitivity to surface topography, low bonding temperature, and compatibility with fabrication processing are particularly applicable.[4]

To avoid particulates interfering with the bond quality, both wafers are cleaned in ultrasonic acetone and methanol. After cleaning, the wafers are dehydrated and subsequently an adhesion promoter AP3000 from Dow Chemical is applied onto the wafers. A 2.6 μm thick BCB film is spun on the SOI wafer and soft cured in an N_2 ambient. The soft cure process is critical to bonding performance. A slow ramp rate to the soft cure temperature is recommended for planarization[1]. During the soft cure process the BCB polymer is partially cross-linked. The degree of cross-linking will affect the final bond strength, the ability to dry etch the film, and the deformation of the patterned material after bonding. There is a narrow window for the soft cure time and temperature that provides the optimal polymer cross-linking. Too low a temperature and short a time and the film will be difficult to etch and will flow when bonding, causing alignment shift. If the soft cure time is too long or temperature too high then the bonding strength is degraded.

After cure the BCB is patterned using Shipley SPR220-7 resist and then reactive ion etched at 100W in an O_2:CF_4 gas mixture.

The SOI and waveguide wafers are aligned and bonded using a Karl Suss BA-6 aligner and Karl Suss SB6 bonder. We measure the alignment before and after bonding using a Karl Suss DSM-8. The wafers are bonded in vacuum at 250C with 3.5bar pressure for 1hr. The bond profile is shown in figure 4.

Our post bond alignment tolerance is set by the alignment of the buried Nb ground plane cut to the front side Nb microstrip. Figure 5 is a picture of the cross over component showing the ground plane cut and the microstrip layer. The cross over component converts microstrip to two slot lines driven out of phase on the ground plane to avoid having extra steps for making vias.

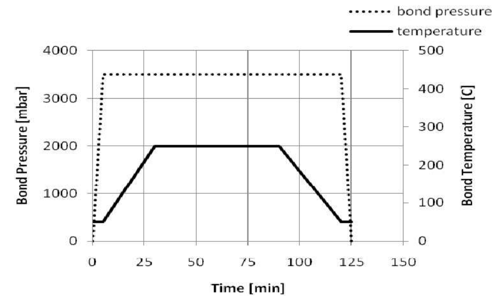

FIGURE 4. Bonding profile for BCB films

In figure 5 the buried ground plane cut can be seen because the 5μm silicon membrane is transmissive and the feature is illuminated from both the front and the back.

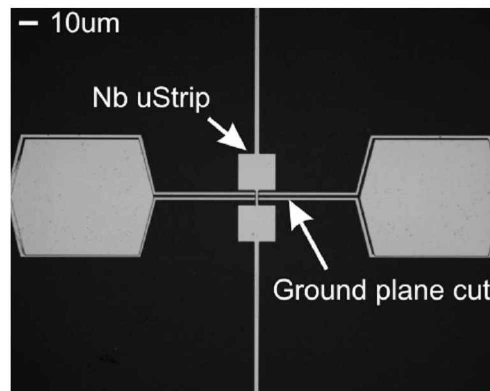

FIGURE 5. Image of cross over component showing alignment of the Nb groundplane cut and the Nb microstrip The misalignment is < 5um.

Microstrip Circuit and Detector Fabrication

After bonding the SOI handle wafer is removed by a combination of mechanical lapping and dry etching. The buried oxide is subsequently etched in HF solution. At this point in the process the niobium ground plane is buried under the single crystal silicon layer and separated from the metalized waveguide by the thickness of the BCB layer 2.6μm. It is critical to maintain alignment accuracy during the bonding process otherwise the waveguide will not be well aligned to the corresponding cutout in the chip, and it will be difficult to align the microstrip to the ground plane since lapping the handle wafer removes the

alignment mark and wafer to wafer alignment information is lost.

Processing of the rest of the circuit is completed on the opposite side of the SOI device layer after the handle layer and buried oxide layer is removed. On the freshly exposed side of the single crystal layer, Nb microstrip, load resistors, and TES bolometers are deposited and patterned. We are currently optimizing the process for Mo/Au bilayer TES with 100 mK transition temperature.

A 3000A thick Nb microstrip layer is magnetron sputter deposited and patterned. To produce Nb structure with sloped sidewall profile, plasma etching in an SF6:O2 atmosphere with resist erosion technique is used. A typical cross section view of Nb microstrip is shown in figure 6. The sloped sidewall is necessary to make ohmic contact to a subsequent Pd:Au alloy deposition. The Pd:Au serves as a load resistance in the microwave circuit and as the microwave power absorber at the TES detector.

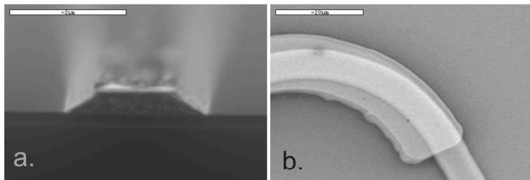

FIGURE 6. a.) Cross section view of Nb sloped sidewall profile. b.) 600A PdAu covering Nb microstrip line

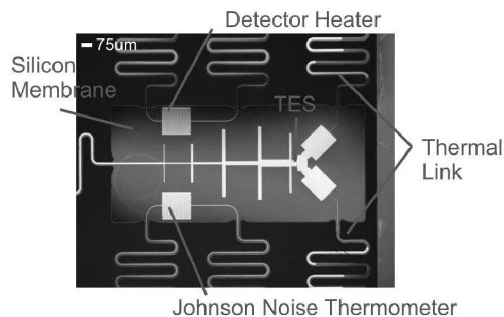

FIGURE 7. Leg isolated silicon membrane for TES thermal isolation. The test structure has a separate heater and Johnson noise thermometer.

The final step is a silicon etch that provides front side ground plane access and also cuts the TES membrane leg supports to provide additional thermal isolation. A picture of the leg isolated TES membrane is shown in figure 7. There are 7 leg supports that have a meander shape to provide desired thermal conductance. For testing purposes we have added PdAu heaters and a Johnson noise thermometer. Figure 8 is a photo of the full chip.

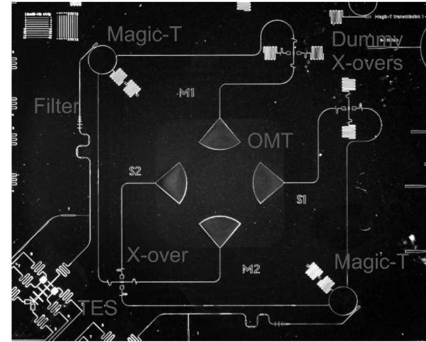

FIGURE 8. Photo of full chip after process completion.

RESULTS AND SUMMARY

We have measured the thermal properties of the leg isolated silicon membrane. From Johnson noise thermometry measurements of detector temperature as a function of input heater power we have extracted an equivalent conductance of 342pW/K for the suspended TES membrane. Heater pulses of 5pJ were applied to the PdAu heater and 8.9ms response time was measured.

We have completed fabrication of detector chips for CMBpol measurement using a hybrid process that incorporates a lithographically patterned polymer adhesive with high post bond alignment accuracy < 5μm. The bonding process enables the use of very low loss 5μm thick single crystal silicon as a dielectric layer for the superconducting microstrip circuitry The bonding process enables a complete conformal metalized waveguide that minimizes potential signal leaking from the waveguide to the front side microstrip circuits. Full system circuit measurement and characterization is currently in progress.

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