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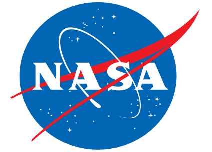

Yearlong 500 °C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits

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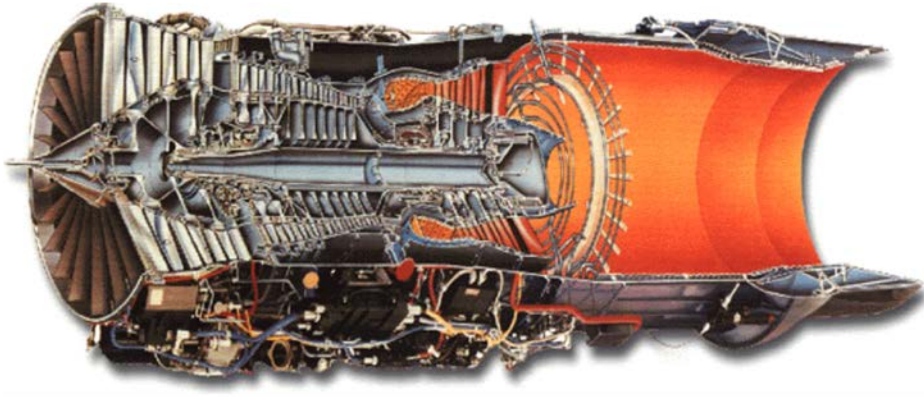
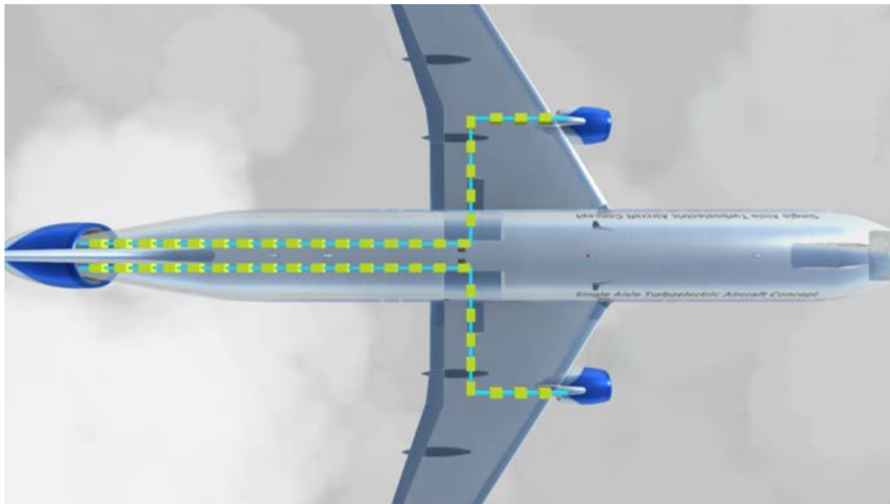
SiC Electronics Benefits to NASA Missions

Intelligent Propulsion Systems



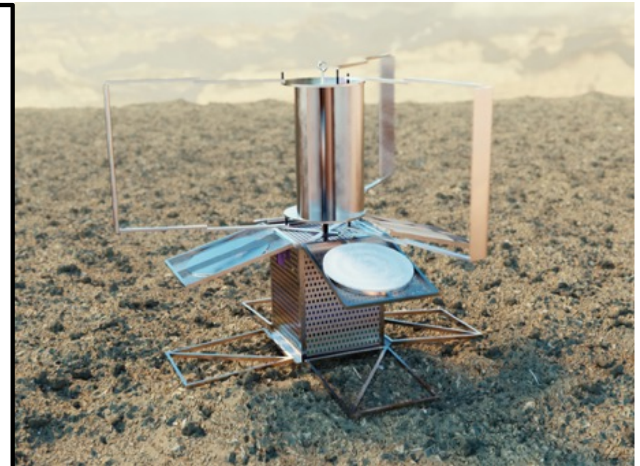
Hybrid Electric & Turbo Electric Aircraft



Venus Exploration

LLISSE = Long-Life In-Situ Solar System Explorer[1]

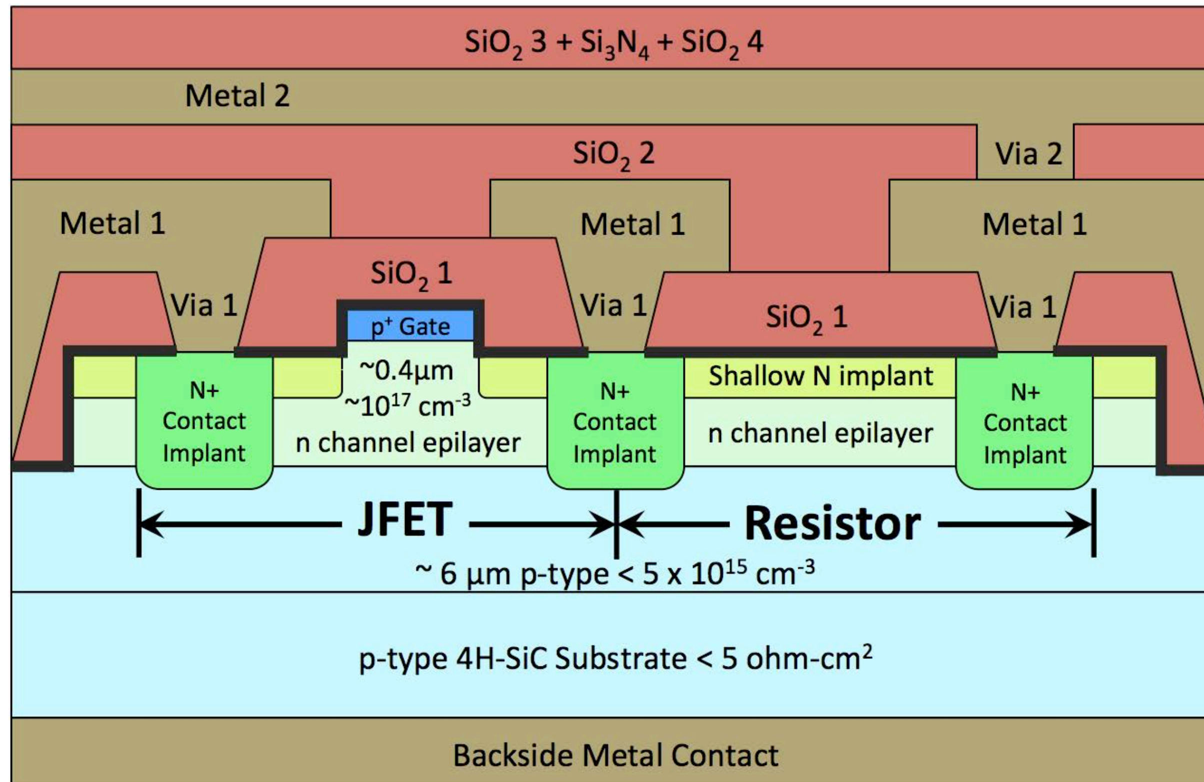
9.4 Mpa = 92.7X Earth pressure + 460 °C + chemical composition found at the surface of Venus (CO_2, N_2, SO_2, H_20, CO, OCS, HCl, HF, and H_2S)



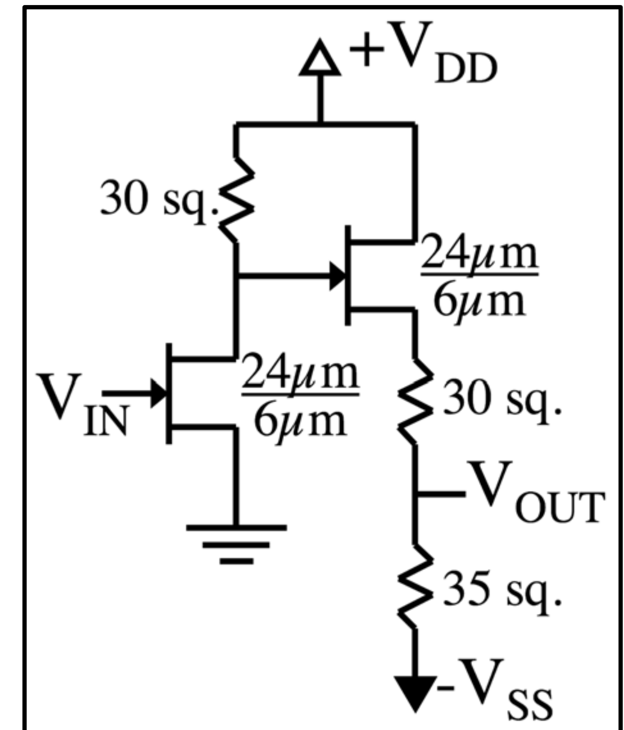
NASA GRC's internal research effort has been to focused on durable/stable integrated circuit operation at 500 ° C for > 1000 hrs.

[1]T. Kremic, et al., 48th Lunar and Planetary Science, 2017, 2986.

N-channel JFET design[1,2] "Version 10.1"



NOT Logic Gate Schematic

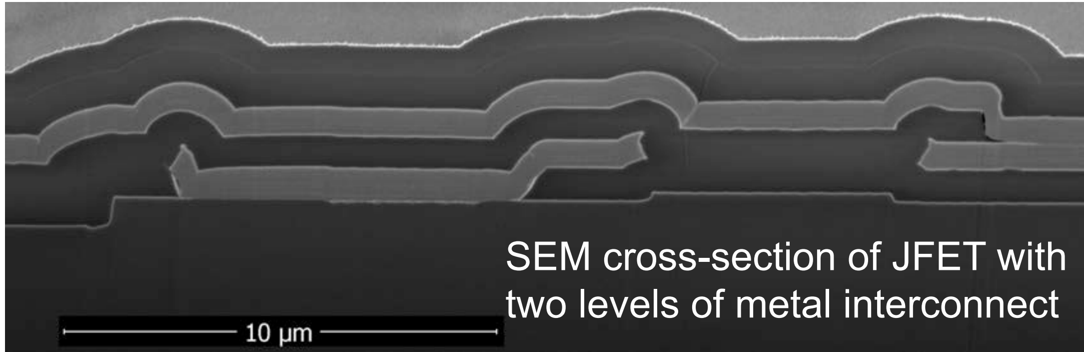


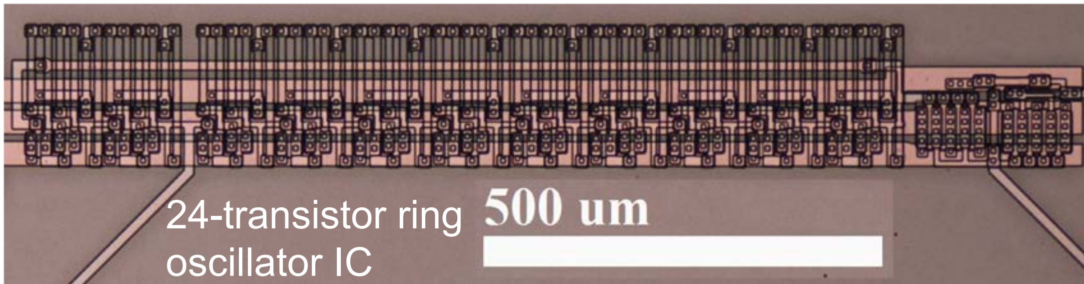
- Normally-on 4H-SiC JFET (fabricated at NASA Glenn)
- Resistors made with same epi as channel → matched T dependence
- Negative threshold voltage V_T → negative signal voltages (0 to -10V)
- 0 V = Binary 1 (high)   -10 V = Binary 0 (low)

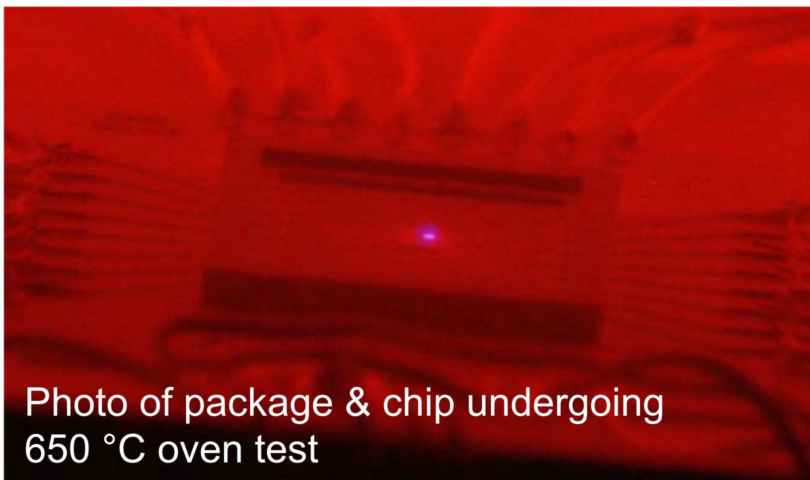
[1]M. J. Krasowski, US Patent 7,688,117 (2010).
[2]P. G. Neudeck, D. J. Spry, and L. Chen, Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

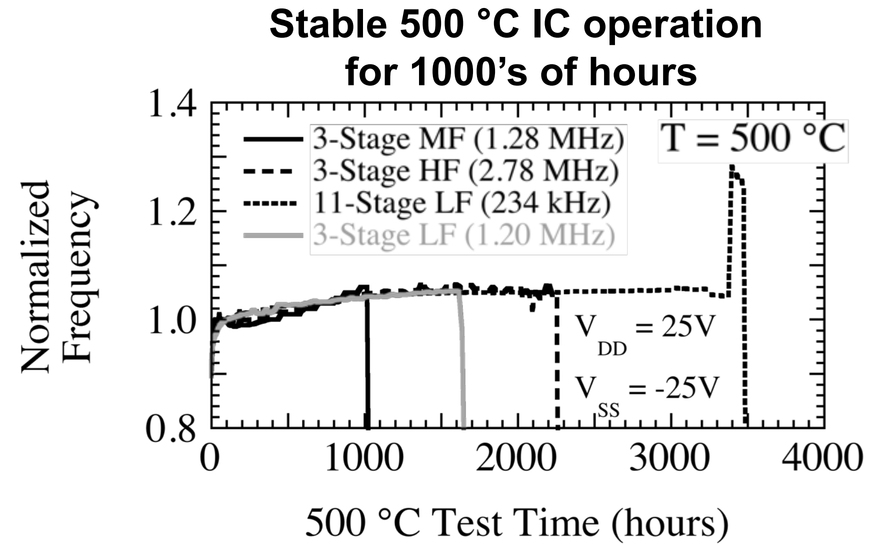
SiC JFET IC Results from HiTEC 2016

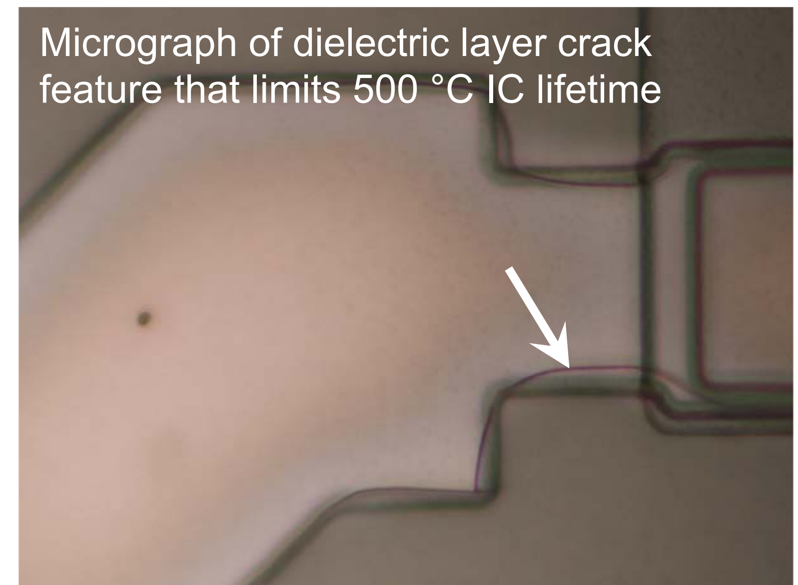
("IC Wafer/Version 9.2")









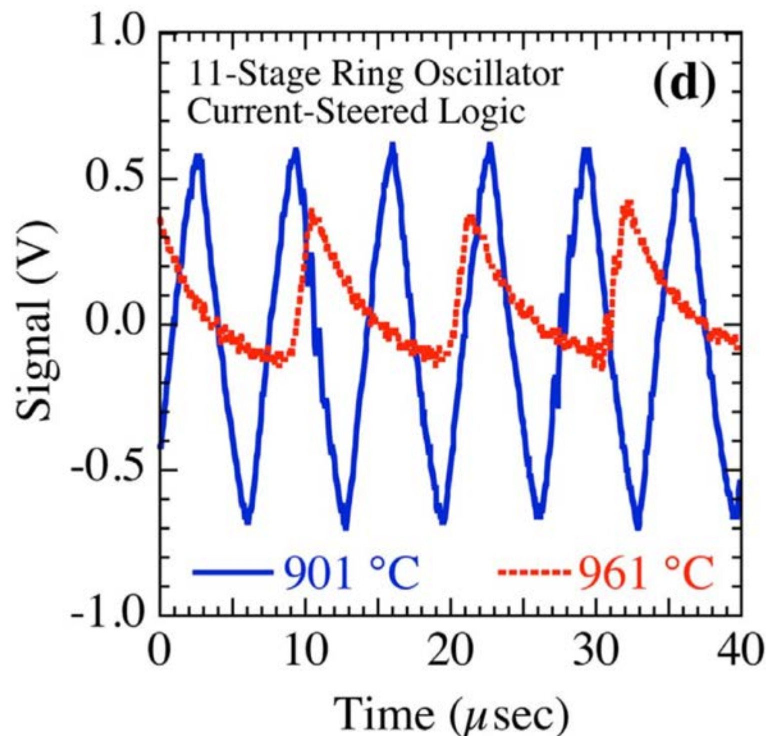


Primary design goal is extreme environment circuit durability.

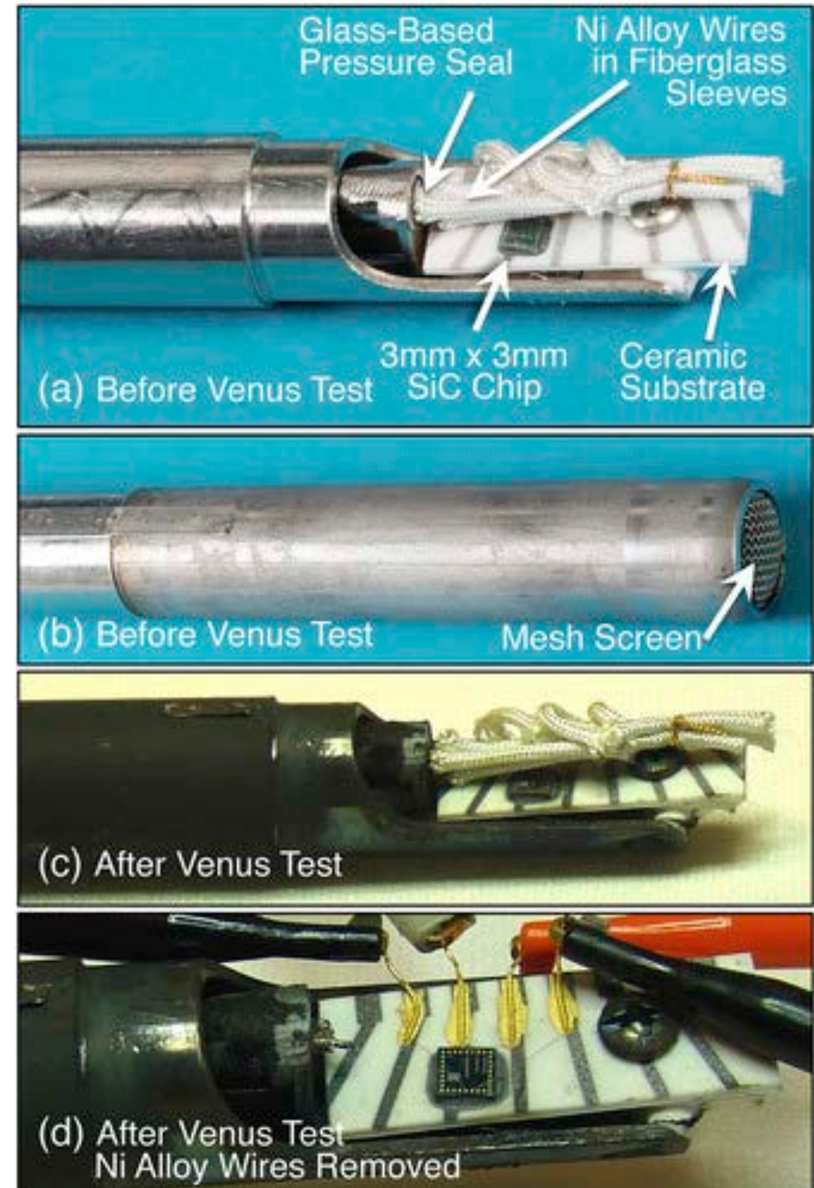
Recent Advances
(Since HiTEC 2016)

- Neudeck, et al., AIP Advances 6 (2016) 125119.
- Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

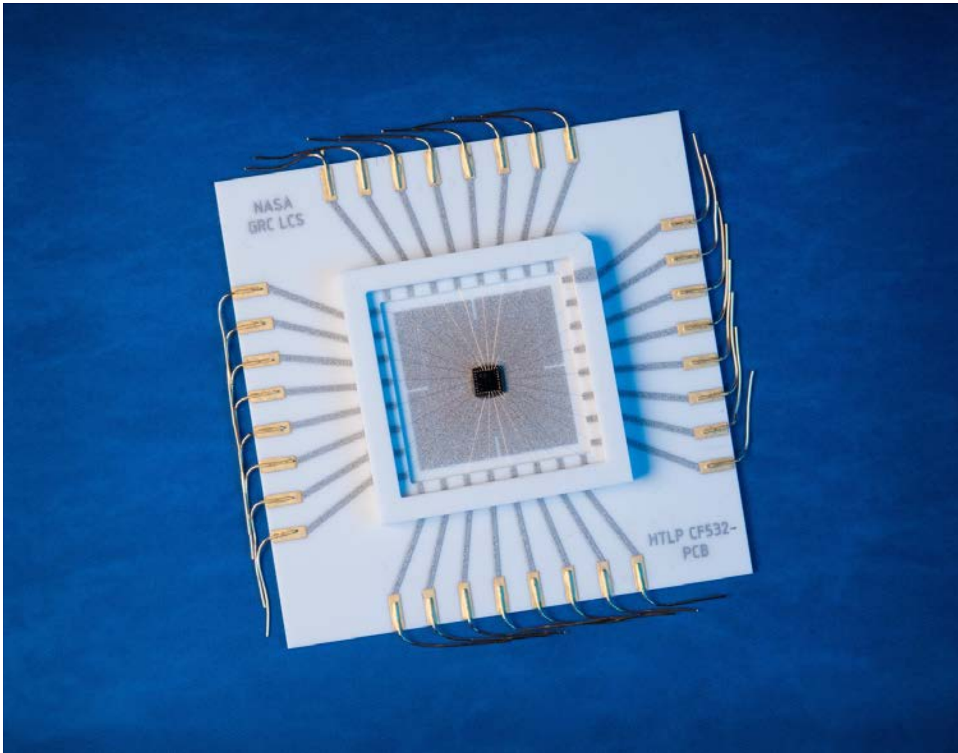
NASA SiC JFET IC operation at T > 900 °C

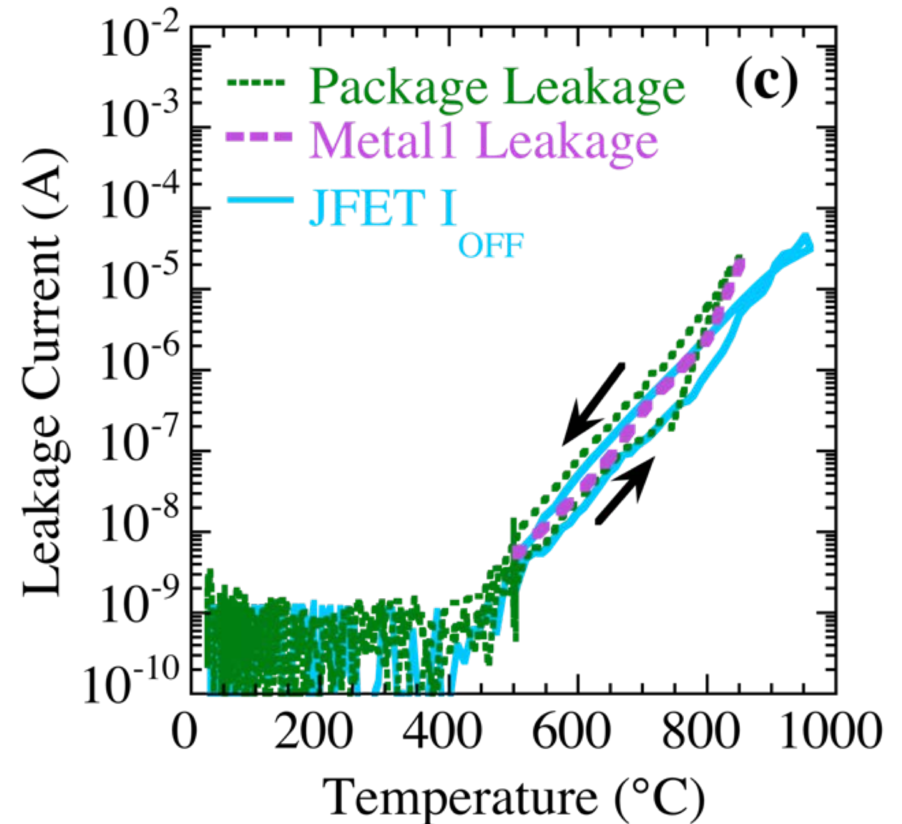


NASA SiC JFET IC operated **immersed in Venus surface conditions (460 °C, 9.4 MPa) for 3 weeks**, did not fail.



High-T packaging[1,2] (32 pins, HiTEC 2016)



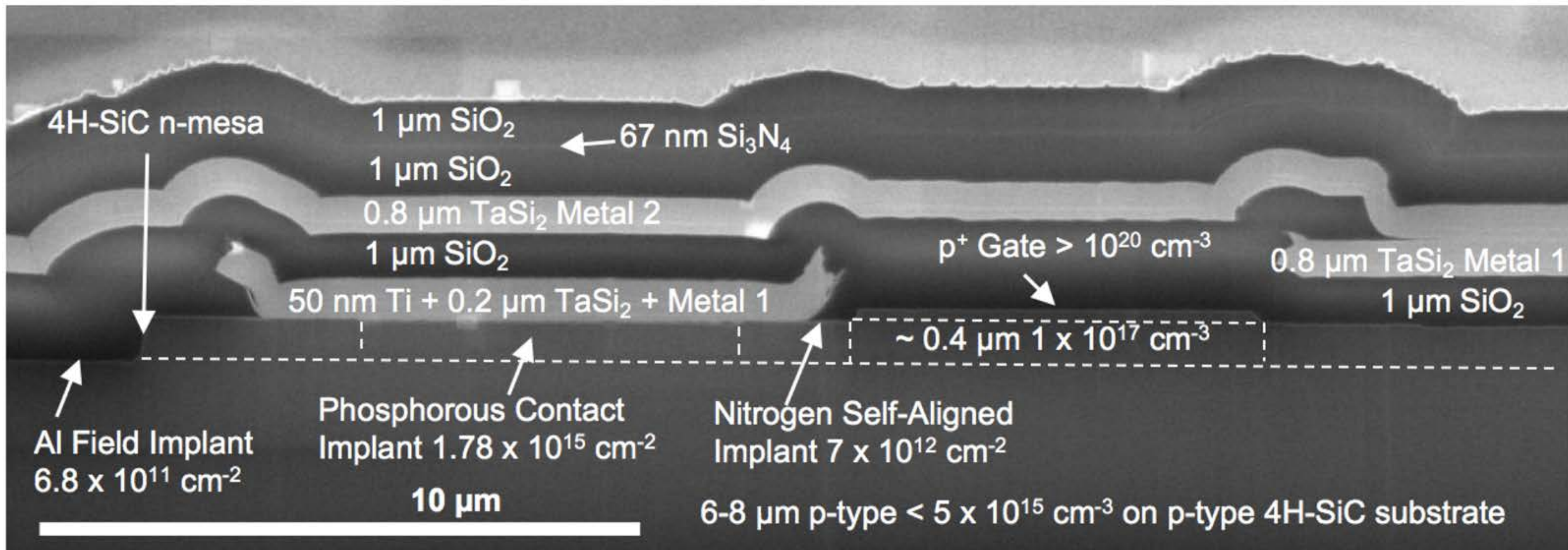


- Package durability and leakage characterized.

[1] L. Chen, et al., Proc. IMAPS High Temperature Electronics Conference, 2016, pp. 66-72.
[2] P. G. Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

JFET IC Wafer 10.1 vs past work[1-2]

- **Aluminum** Field Stop Implant to impede parasitic field MOSFETs.
- Heavily-implanted SiC contact regions were formed using **phosphorus** implant profile with slightly lower energy & dose.
- Contact was made using 50 nm sputtered **titanium** layer.



Primary design goal is extreme environment durability.

[1]D. J. Spry, et al., Mat. Sci. Forum 828 (2016) 908-912: “IC Wafer/Version 8.1”
[2]D. J. Spry, et al., IEEE Electron Device Lett. 37 (2016) 625-628: “IC Wafer/Version 9.2”

Wafer 10.1 IC Functional Yield at 25 °C[1]

Table I. 25 °C Probe Test Yield for 100+ JFET SiC ICs

Demonstration IC	IC JFET Count	# Good/# Tested $r \leq 25$ mm	% Yield $r \leq 25$ mm
16-bit RAM	195	19/27	70%
÷ 2/÷4 Clock	175	19/26	73%

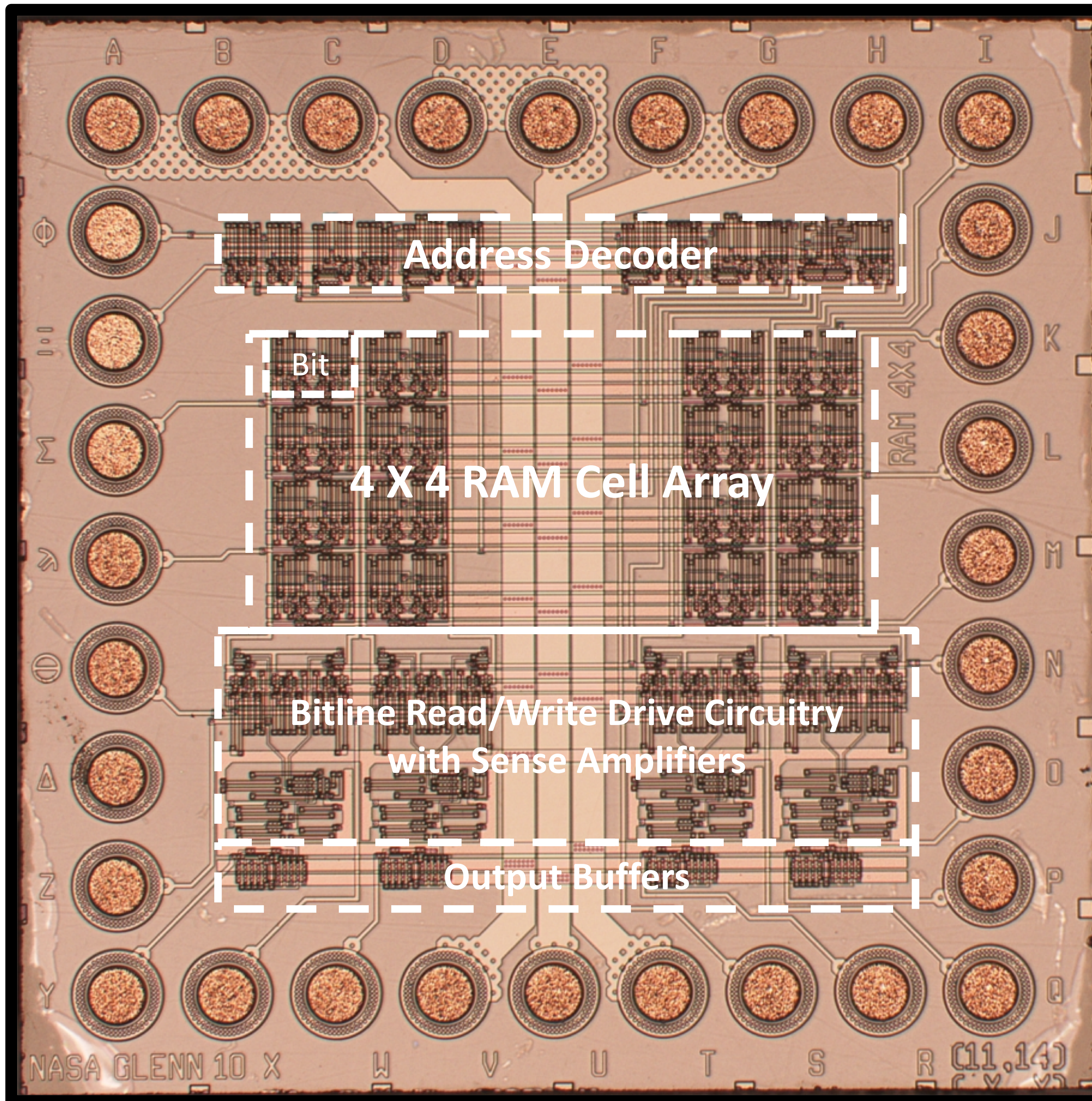
- JFET threshold voltage V_T on depends on distance from the center of the wafer *r*, due to as-purchased wafer epilayer variation (see Ref. 2).
- Table I is for *r* < 25mm (on 38 mm radius wafer), the wafer region where V_T falls within circuit design specifications of $|V_T| < 10$ V.

Despite > 7-fold increase in IC complexity from previous run (Wafer 9.2), functional probe yields in excess of 70% were obtained for Wafer 10.1.

[1]D. J. Spry, et al., presented at ICSCRM 2017, to appear in Materials Science Forum, Vol. 924 (2018).

[2]P. G. Neudeck, D. J. Spry, and L. Chen, Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

4X4 Random Access Memory (RAM) Demonstration Chip[1]

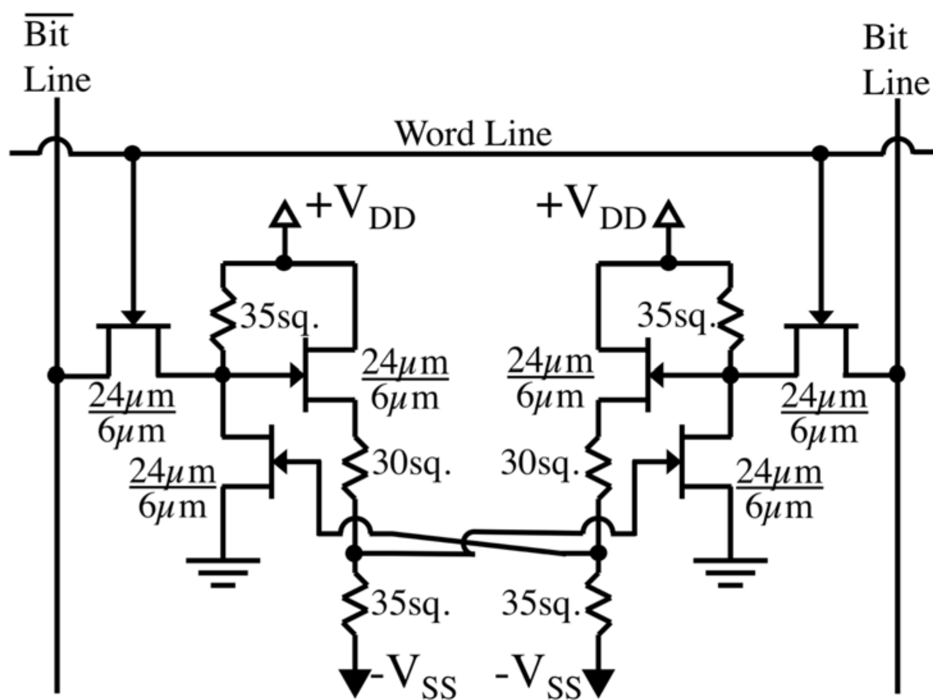


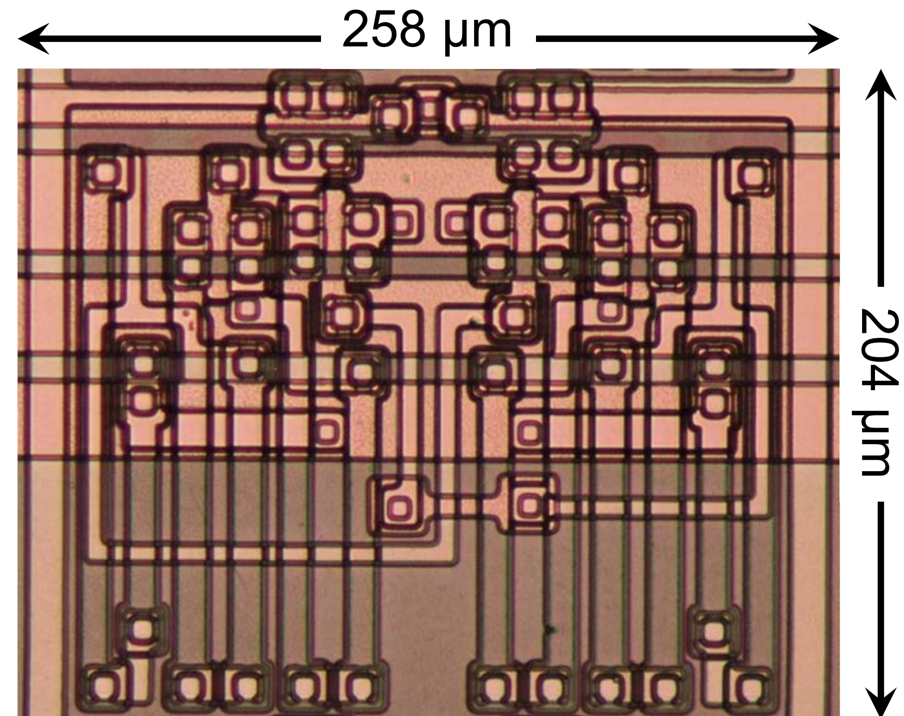
- 3mm x 3mm 4H-SiC JFET chip shown prior to packaging.
- 195 JFETs.
- 6-Transistor static RAM cell approach.
- Includes address decoders, read/ write bitline drive with sense amplifiers, output buffers.

[1]D. Spry et al., ICSCRM 2017

SiC JFET RAM Chip Circuit Design

RAM Cell





6-JFET cell mimics traditional "Static" RAM approach.

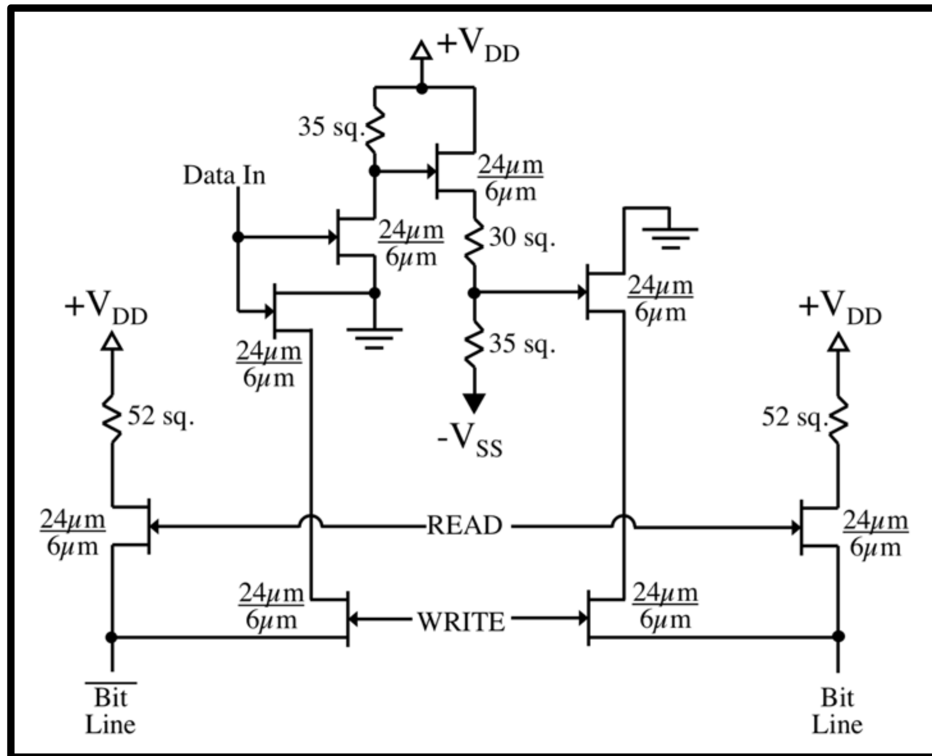
- Cross-coupled NOT gate latch connected to bit line pair by access FETs.

To enable "normally on" access JFETs function in "normally off" manner, latch is accessed at inverting amplifier stage and bit lines are internally driven/sensed using positive voltages.

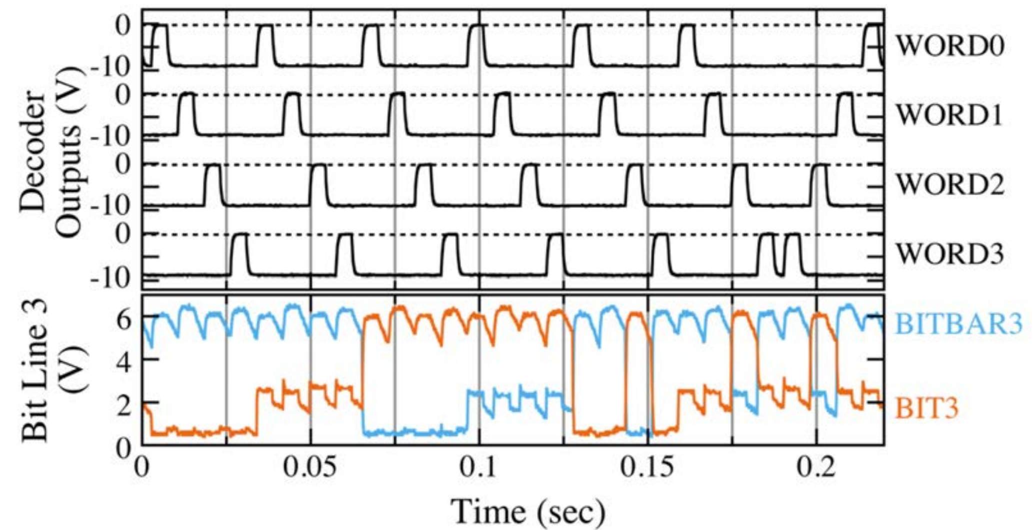
SiC JFET RAM Chip Circuit Design

RAM Array Support Circuitry

Bit line (Column) Driver Schematic



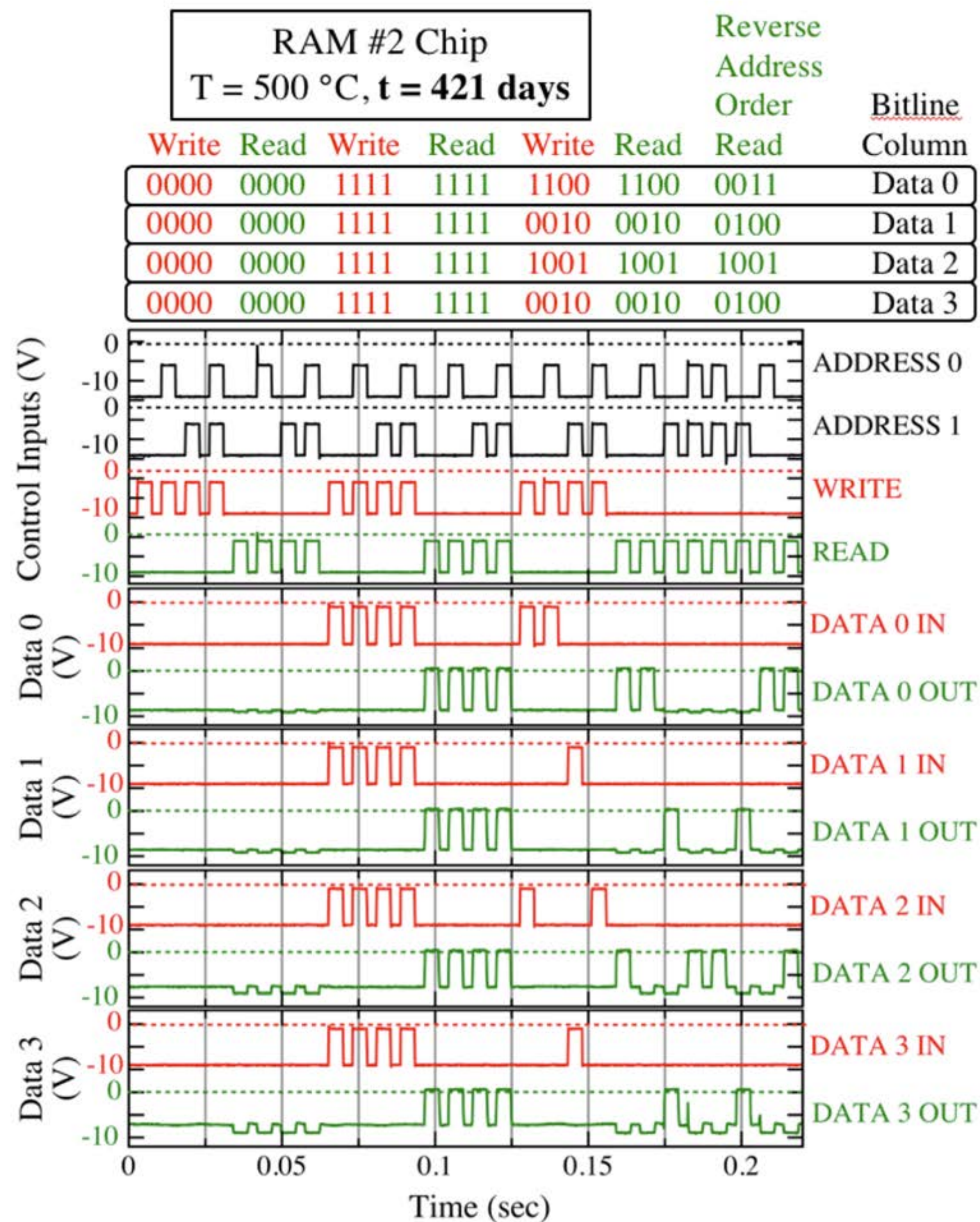
Internal chip word line (rows) and bit line (column) signals* at 500 °C



*Waveforms measured via diagnostic bond pads and oven wiring to 10 MΩ oscilloscope probes.

- Address decoder and word lines function at negative voltages of logic family.
- Bit lines and sense amplifiers function at positive voltages (per preceding slide).
- Design is "proof of feasibility" for 500 °C operation, not considered "optimized".

RAM #2



V_{DD} = +25 V

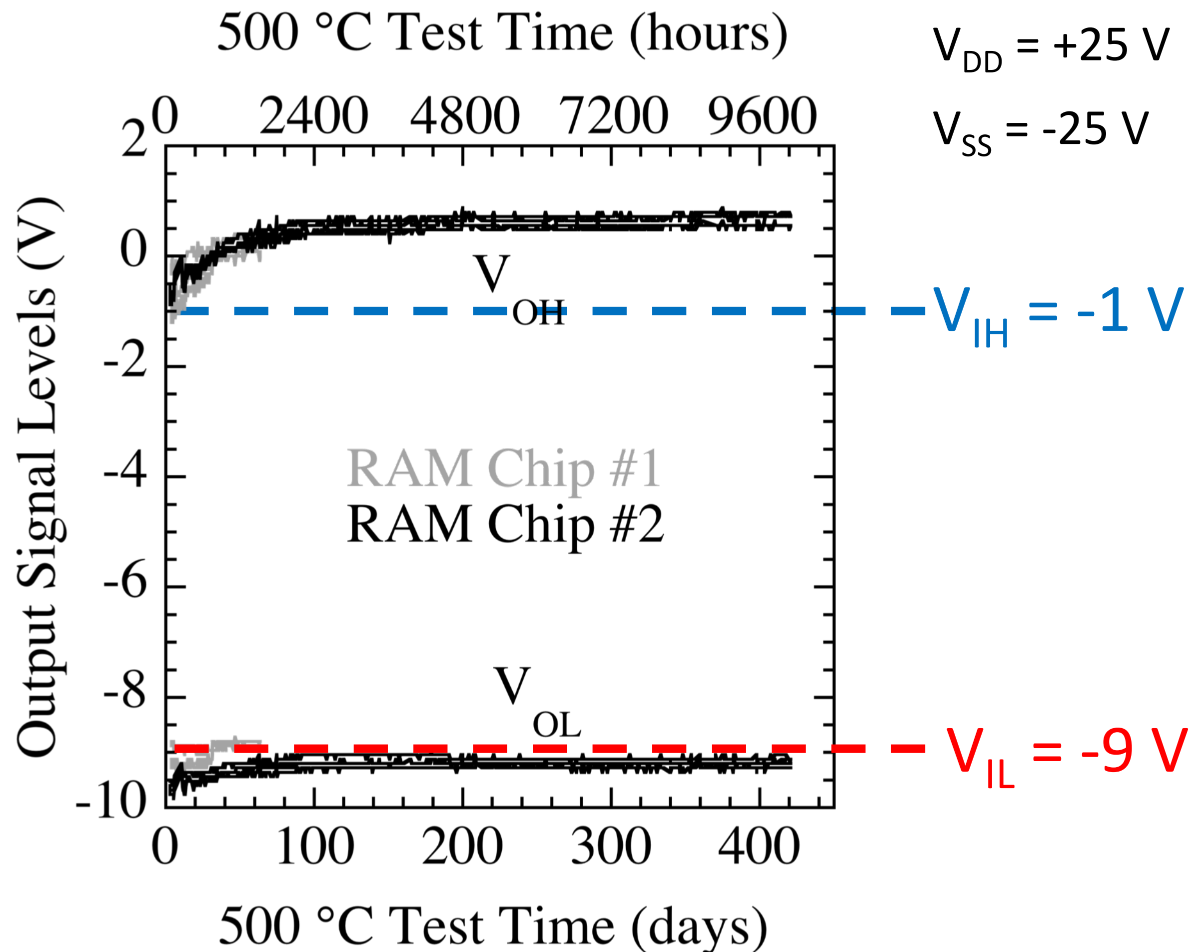
V_{SS} = -25 V

V_{IL} = -9 V

V_{IH} = -1 V

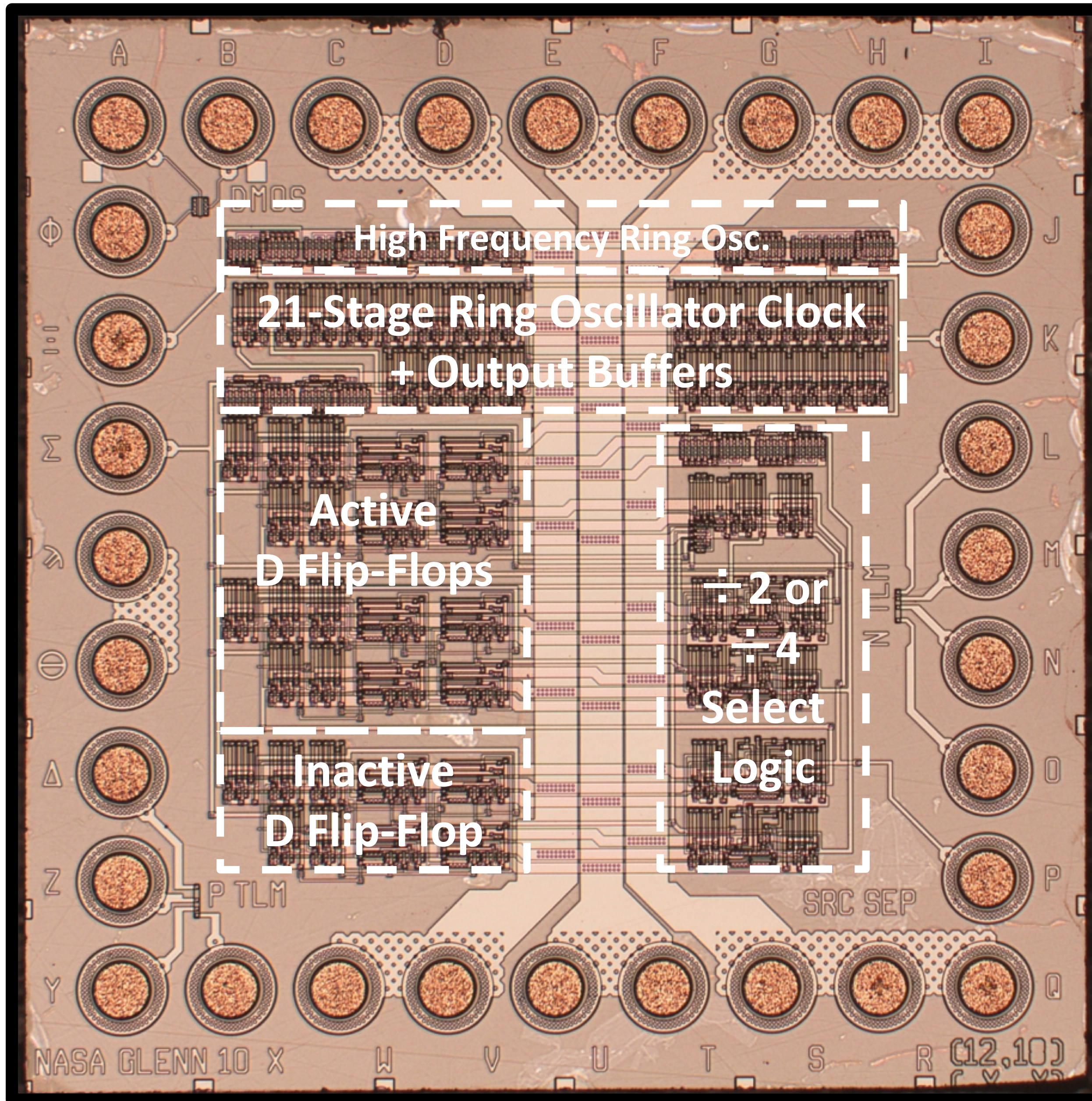
Measured 16-bit RAM waveforms showing read and write functionality of all bits at **421 days** (10,100 hours) of a 500 °C oven test.

RAM Chip Output Levels vs 500 °C Test Time



Following modest changes during early burn-in period, output high (V_{OH}) and output low (V_{OL}) voltage levels exhibit negligible change

÷2/÷4 Clock Demonstration Chip[1]

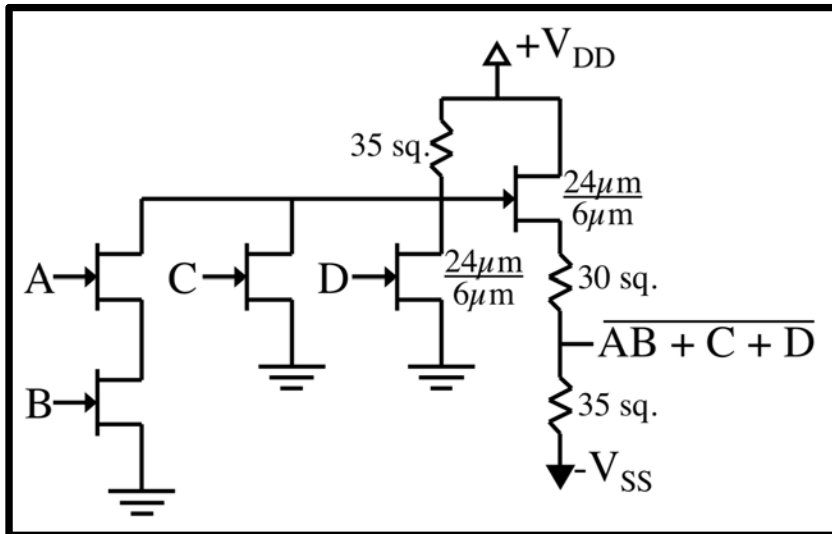


- 3mm x 3mm 4H-SiC JFET chip prior to packaging.
- 175 JFETs
- 21-Stage ring oscillator provides base frequency clock signal
- SELECT data line:
  - High (0 V) → ÷4 output
  - Low (-10 V) → ÷2 output
- Includes two D-type flip flops governed by select logic
  - 3rd flip flop is inactive due to layout error.
- Optional modulation of high-f ring oscillator signal

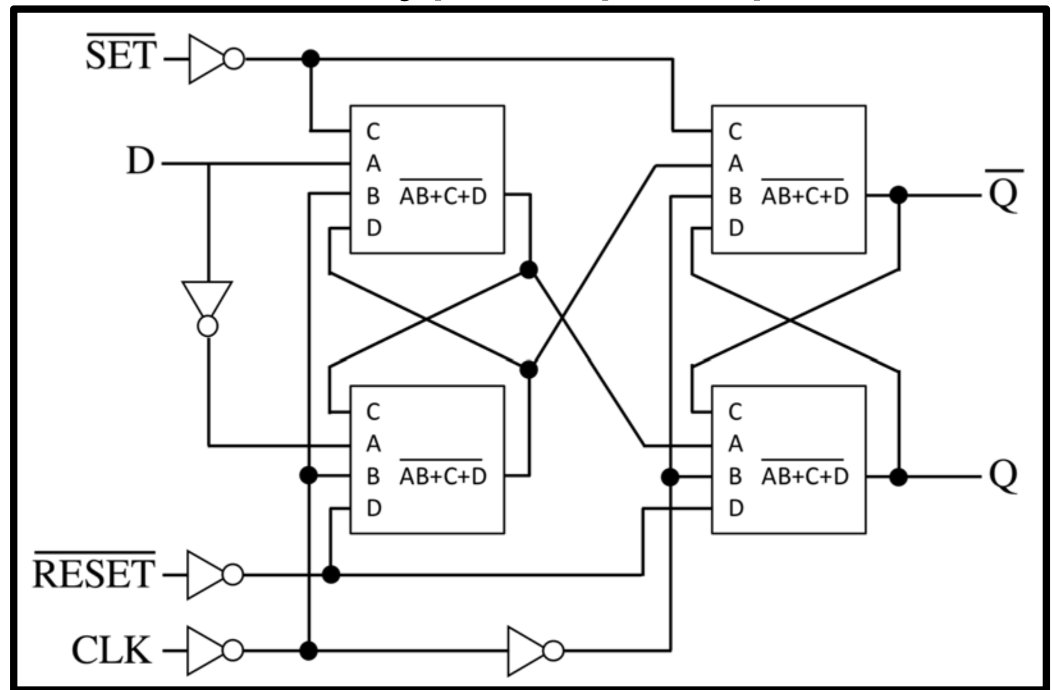
[1]D. Spry et al., ICSCRM 2017

SiC JFET Flip Flop Circuit Design

Combination Logic Gate

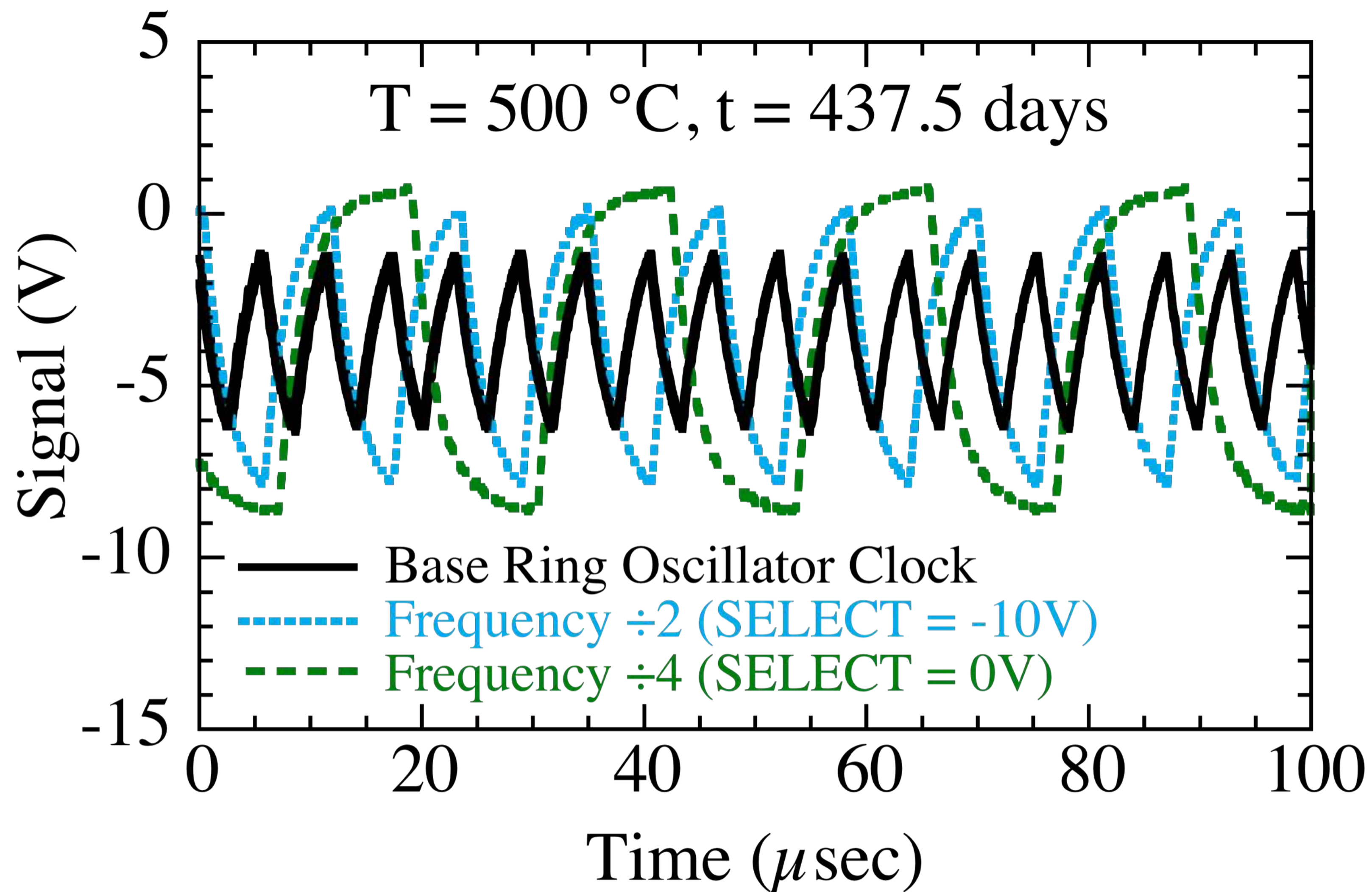


D-Type Flip Flop



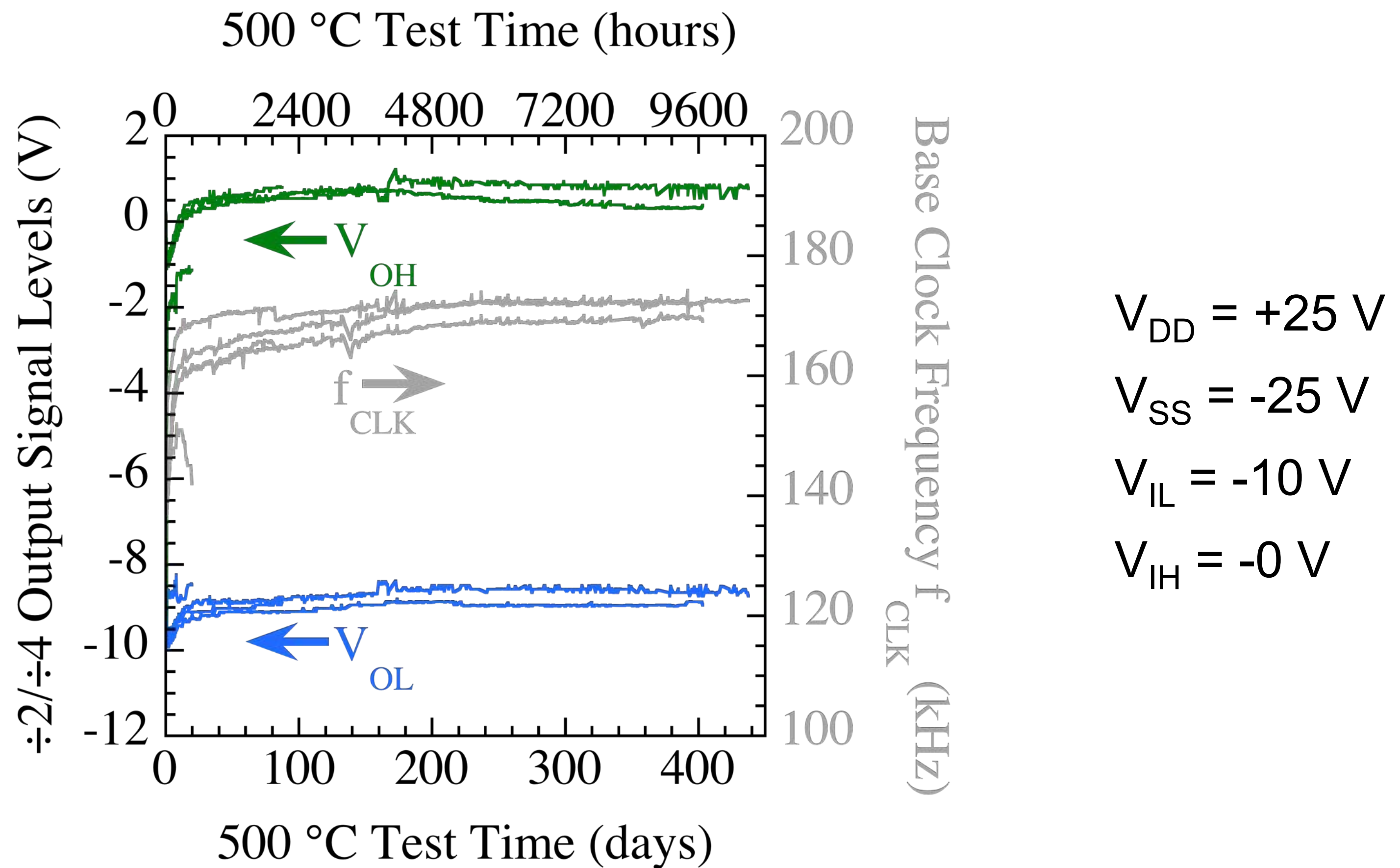
- Ring oscillator base clock is frequency divided using D-type flip-flops.
- Additional logic gates control signal propagation to realize ÷2 vs ÷4 base clock frequency based on SELECT input.

÷2/÷4 Clock Chip #2



Measured waveforms showing operation of ÷2/÷4 clock IC at **437.5 days** (10,500 hours) of 500 °C oven testing.

÷2/÷4 Clock Signals vs Time at 500 ° C



V_{DD} = +25 V

V_{SS} = -25 V

V_{IL} = -10 V

V_{IH} = -0 V

- Time evolution of ÷2/÷4 clock IC output voltages and frequency for all 5 packaged chips subjected to prolonged 500 °C testing.
- After initial burn-in, output characteristics change < 10%.
- 3 of 5 chips remain functioning under 500 °C test today.

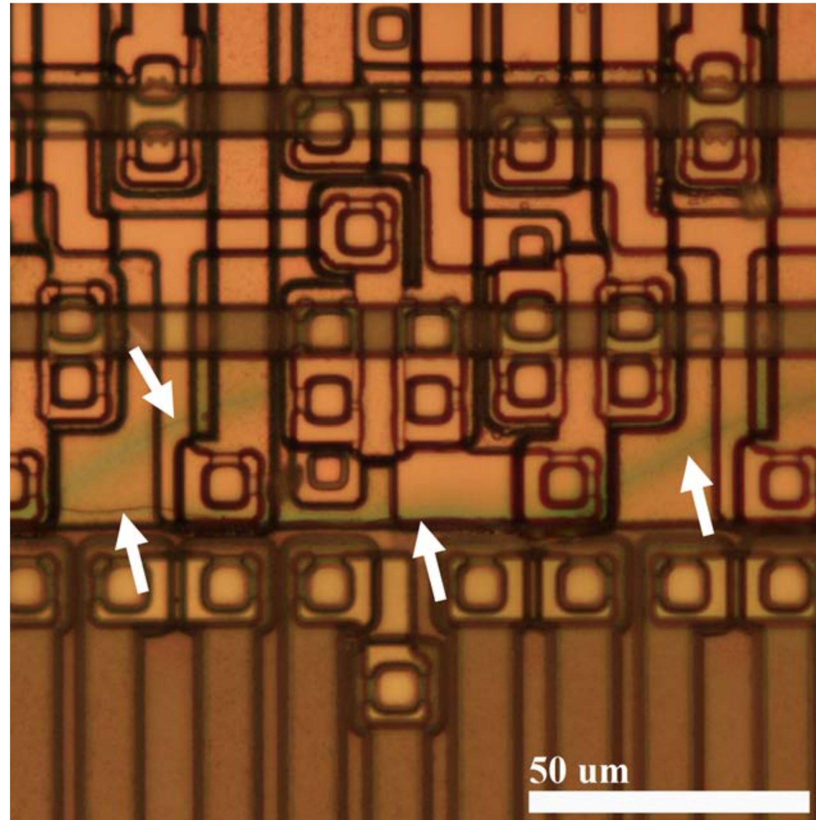
Wafer 10.1 500 °C Durability Results

Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	***r*** (mm)	500 °C Time	Test Status
RAM #1	13.4	1525 h	Suspended
RAM #2	6.7	10100 h	Running
Clock #1	24.2	470 h	Failed
Clock #2	15.3	10500 h	Running
Clock #3A	12.4	9677 h	Running
Clock #3B	12.4	9677 h	Running
Clock #3C	13.4	2090 h	Failed

First reported demonstrations of 1+ year (8766+ hours) 500 °C integrated circuit operation (in any semiconductor).

Clock #1 IC Failure Analysis



Electrical failure mode (at 470 hours): 21-stage ring oscillator ceased functioning.

White arrows denote examples of dielectric cracks and metal trace discoloration observed in the ring oscillator sub-circuit, symptoms of the primary 500 °C IC failure mechanism described previously[1].

[1]D. J. Spry, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 249-256.

Future Work

Continue development and demonstrations of increasingly capable 4H-SiC SiC JFET integrated circuits.

- Improve IC durability by reducing or eliminating dielectric crack formation.
- Improve IC capability by upscaling to higher chip complexity.
- Improve IC validation with larger statistical data sets, full flight environment electrical testing.
- Mature technology towards NASA mission insertion and commercialization.

Summary

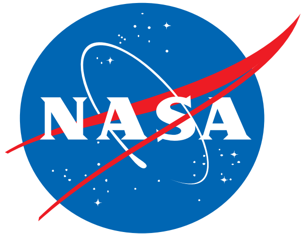
First demonstration of 1+ year of 500 °C ambient temperature integrated circuit operation.

- 4H-SiC JFET ICs up to 195 transistors/circuit.
- First 500 °C durable random access memory (RAM).

NASA Technology Access

Prototype IC designs meeting 4H-SiC JFET IC guidelines could potentially be fabricated by NASA Glenn, under negotiated collaborative Space Act Agreement:

- Contact: https://technology.grc.nasa.gov, Priscilla.S.Diem@nasa.gov.
- Tech guidelines: https://sic.grc.nasa.gov/files/HiTEC2016-NeudeckV1A.pdf


NASA