Power Amplifier Principles and Modern Design Techniques

Vladimir Prodanov and Mihai Banu

INTRODUCTION

Enabled by Lee de Forest's invention of the vacuum tube triode in 1906, power amplification of electrical signals has played a key function in electronic systems ever since. Mundane devices we take for granted such as the telephone, the radio, or the television would not exist without this capability. Given such a wide application space, it is not surprising that early on electrical engineers have worked out the details of designing good power amplifiers (PAs), first with vacuum tubes, and then with discrete transistors [1]. They did such a fine job that by the second part of the twentieth century, the art of designing PAs became a mature electrical engineering (EE) specialty, which seemed to have little room left for breakthroughs or major innovations. However, the late-century market explosion of mobile digital communication systems and devices, such as cellular phones and wireless local area networks (LANs), and the massive introduction of integrated circuit (IC) technology in everyday life have changed the electronic landscape dramatically, opening new challenges and opportunities for PAs.

In this chapter, the issues and appropriate techniques for modern PAs are discussed, focusing on IC implementations for wireless communication systems. To familiarize the reader with the general PA design approach, which is rather different from the regular analog circuit approach, a few important points are clarified, as a prerequisite for the following material. Then, the classical theory of PA design in the case of constant magnitude signals is reviewed and the trade-offs for different classes of transistor operation are pointed out. The important class AB case is discussed in more details. Next, the PA design problem from a unified, general point of view based on the internal PA signal harmonic content is revisited. This will give the reader a further insight into the PA design problem and high-level solution possibilities. The following section concerns the important topic of efficiency in the presence of back-off and briefly mentions other important design considerations. Finally, recent PA results are reviewed and conclusions drawn.

REVIEW OF PREREQUISITE KNOWLEDGE

Relative Signal Bandwidth for Most Modern PAs

The main motivation for the renewed interest in PA technology comes from the technical challenges and the economics of modern digital communication systems. The very high production volumes of consumer wireless mobile devices have created a large market for high-quality, low-cost PAs operating in the medium output power range (0–30 dBm). The allocated radio frequency (RF) bands for such typical applications are shown in Table 13.1. A simple calculation of the relative bandwidth compared to the average RF frequency for each system clearly shows that the signals at the RF front-end are narrow band-pass signals on the absolute frequency scale. This fact is not in conflict with the usual categorization of some of these systems as wideband because the latter refers to the base-band signal bandwidth and not to the RF relative bandwidth. More precisely, wideband signals carry a substantially larger amount of information than traditional voice-band signals, but when placed at a high RF carrier frequency, they become relatively narrow, as shown in Figure 13.1.

The relevance of the previous discussion is the realization that on a relatively short time span, that is, over a small number of carrier frequency cycles, the PA signals are practically sinusoidal. At the RF timescale, the magnitude and phase of this sinusoidal signal slowly change only over many carrier cycles. This justifies the common practice in the PA literature to analyze the circuit under

TABLE 13.1
Frequency Bands and Available Bandwidths for Common Wireless Systems

	Licensed Bands				
	US Cellular	**R-GSM**	**DCS**	**PCS**	**IMT2000**
Uplink (MHz)	824–849	876–915	1710–1785	1850–1910	1920–1980
Downlink (MHz)	869–894	921–960	1805–1880	1930–1990	2110–2170
Total BW (MHz)	25	39	75	60	60
Relative BW (%)	~3.0	~4.4	~4.3	~3.2	~3.1

	Unlicensed Bands		
	ISM-2.4 2400–2483.5	**UNII-5.2 5150–5350**	**UNII-5.8 5725–5825**
Total BW (MHz)	83.5	200	100
Relative BW (%)	~3.4	~3.8	~1.7

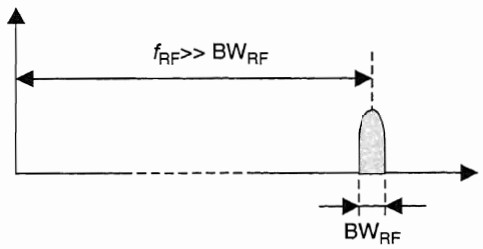


FIGURE 13.1 A typical frequency diagram illustrating that even wideband wireless systems (e.g., wideband code division multiple access [WCDMA]) have small signal bandwidths compared to the carrier frequency f_{RF}.

sinusoidal signal conditions. This adequately represents the PA behavior over short time durations, which is a necessary but not a sufficient criterion for a valid design. Later, in the section "PA Techniques for Power Back-Off Applications," the PA performance over long time spans is discussed in detail, but until then, assuming sinusoidal signals for the PA input and output will be sufficient to explain many important PA properties.

What Is a Power Amplifier?

Despite the deep-rooted terminology, PAs do not amplify power! Power is energy per unit of time, and as the first law of thermodynamics states, energy cannot be created. Then, what are PAs? And why are they given this name?

A defining property of a PA is that its output signal power delivered to a load is larger than the input signal power it absorbs from a driver. In this respect and outside any energy balance considerations, the PA produces the effect of a nonphysical power amplification device, hence the name. The way the PA accomplishes this effect is by converting the DC power supplied through the DC biasing lines into output signal power. Therefore, a PA is an energy conversion circuit very much like a DC-to-DC converter or an RF oscillator, which converts DC power into constant wave (CW) power. However, unlike DC-to-DC converters or oscillators, an ideal PA converts the DC power into output signal power under the linear control of an RF input. A wireless system PA is simply a DC-to-modulated-RF converter.

The simple observation regarding power conversion in PAs is crucial to understanding the design and operation of this type of circuits, as will be explained later. Here, it suffices to notice

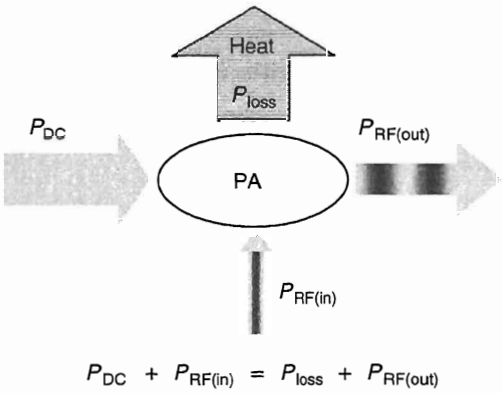


FIGURE 13.2 Power flow and balance diagram in a typical PA.

that the very PA concept implies a nonlinear operation since linear networks cannot shift power from one frequency to another.

As described so far, the PA concept is still nondistinguishable from a regular voltage or current amplifier since the latter may (or may not) generate a power-amplified output with respect to its input. What sets the PA apart is the matter of power conversion efficiency. Although the design of a regular voltage or current amplifier is not concerned with efficiency, this performance aspect is paramount in PA designs. In addition, very often the PAs are required to deliver much higher levels of power into the load than regular amplifiers do and may need the capability for power control.

Figure 13.2 illustrates the PA functionality in terms of a power flow diagram. The input power at DC is shown on the horizontal axis to emphasize the key role it plays in this circuit. The very purpose of the PA is to transfer most of this power to the modulated-RF output. The portion that is not transferred is lost through heat. The output modulation information is provided through a low-power RF input in a similar way as with regular analog amplifiers.

Related to the artificial power amplifier terminology are the concepts of power gains. Several output-power-to-input-power ratios are commonly defined under various operating and power-accounting conditions [2]. The PA power gains lack any deep physical meaning but are useful in practice for the purpose of specifying the driving requirements of the circuit in relation to matching and stability conditions.

PA Efficiency

Figure 13.3 shows the simplest classical nonswitched single-transistor PA configuration. DC bias is provided through a large inductor (choke) and the PA load is connected via an ideally lossless matching network. Two most important figures of merit of any PA are the following power efficiency ratios using the notation from Figure 13.2:

$$\text{PE} = \frac{P_{\text{out}}}{P_{\text{DC}}} \tag{13.1a}$$

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \tag{13.1b}$$

PE is the power conversion efficiency reflecting the percentage of the DC power drawn from the power supply, which has been converted into output signal power. This figure of merit is also called drain/collector efficiency. Power-added efficiency (PAE) is calculated by subtracting the input power from

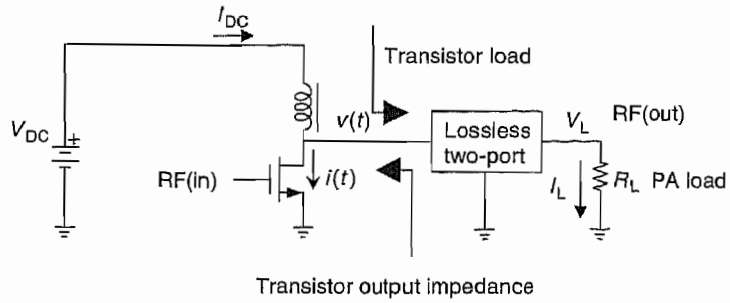


FIGURE 13.3 A classical single-transistor PA, often called linear PA or current PA.

the output power to include the effect of the PA driver in the efficiency metric. Obviously, for large power gains, PAE approaches power efficiency (PE).

The various power quantities can be calculated in the circuit from Figure 13.3 as follows:

$$P_{DC} = V_{DC} I_{DC} \tag{13.2a}$$

$$P_{out} = \frac{1}{2} V_L I_L \tag{13.2b}$$

$$P_{loss} = \frac{1}{T} \int_0^T i(t) v(t)\, dt \tag{13.2c}$$

These relations can be used in Equations 13.1a and 13.1b to calculate the PA efficiencies.

Matching for Maximum Output Power

On the basis of linear system theory hastily applied to the circuit shown in Figure 13.3, one would tend to believe that conjugate matching between the transistor output impedance and the transistor-load impedance ("seen" into the matching network input port) would transfer the maximum possible power to the PA load. This is not true because the transistor nonlinear behavior limits the voltage swing at the drain, shifting the maximum-power conditions far from the theoretical linear case. Laboratory experiments and theoretical investigations [2] show that constant-power closed curves exist on the transistor-load-impedance plane, usually shown as a Smith chart. These oval curves nest within each other like the classical constant-gain circles shrinking to a point of maximum power delivery under strong nonlinear operating conditions. The tuning of the transistor-load impedance performed with special equipment to identify the maximum-power case for various operating conditions is called load pulling. RF PA designers regularly use load-pulling laboratory data to guide their work since modeling is rarely accurate enough.

The Meaning of Linear PA

It was mentioned earlier that the PA is a nonlinear circuit by necessity. Nevertheless, though power conversion is a nonlinear process, it is possible to design an approximately linear modulation transfer characteristic from the RF input to the PA output. This is the second important design criterion in addition to getting high efficiency.

The usual implications of the previous requirements are illustrated in Figure 13.4. The RF input and the PA output are clean band-pass signals carrying the same modulation information. The internal PA voltage is a rather dirty wideband signal with rich and large harmonic content. It will

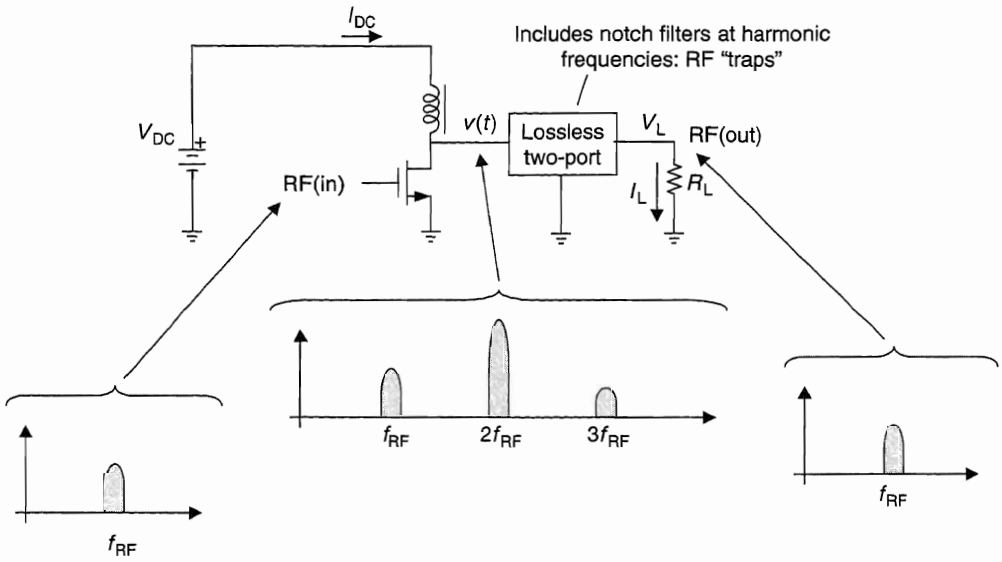


FIGURE 13.4 A highly nonlinear PA with linear RF-in/RF-out characteristic.

become clear later that it is precisely this internal harmonic content that is responsible for obtaining good efficiency. This indicates that the design strategy for a PA is quite different from that for a regular linear amplifier. In the latter, since there are no efficiency concerns, it is not necessary and undesirable to introduce high internal nonlinear behavior, which would have to be transparent to the output. Efficient PAs must be highly nonlinear internally and still be input/output linear in terms of the RF modulation transfer.

THE CLASSICAL APPROACH TO PA DESIGN

Types of PAs and the Concept of Conduction Angle

There are two main branches in the PA family tree shown in Figure 13.5. If the main PA transistor operates as a transconductance element converting the RF input signal into a current, the circuit is called a linear or current PA. If the main PA transistor is just a switch, the circuit is called a switching PA. This PA family branch will be discussed in the subsection "Switching PAs."

Current PAs, whose general structure is similar to that shown in Figure 13.3, are further divided into classes of operation on the basis of conduction angle [2]. Figure 13.6 illustrates this concept for the case of an ideal transistor with piecewise linear *I/V* characteristics. The conduction angle is a measure of the drain current generation process for a given biasing point and a given RF input signal magnitude. If the biasing point and the RF input signal magnitude are such that all input signal excursion is linearly converted into a drain current, the PA operates in class A with 2π conduction angle. Class B operation is defined for π conduction angle when exactly only one side of the RF input sinusoidal signal is converted into current. Lowering the conduction angle bellow π defines class C and increasing it toward 2π defines class AB, not shown in Figure 13.6. Next, the merits of these possibilities are discussed.

Class A, B, and C Operations

The maximum drain voltage and current waveforms for classes A, B, and C are shown in Figure 13.7. Notice that in all cases, the drain voltage is the same and consists of a full sinusoidal (see the subsection "Relative Signal Bandwidth for Most Modern PAs"). The difference comes from

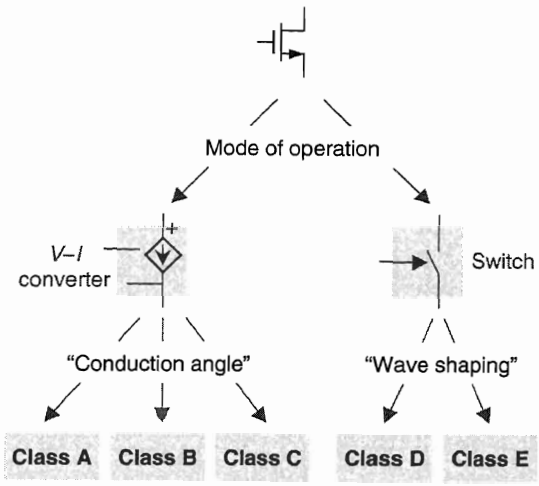


FIGURE 13.5 PA family tree.

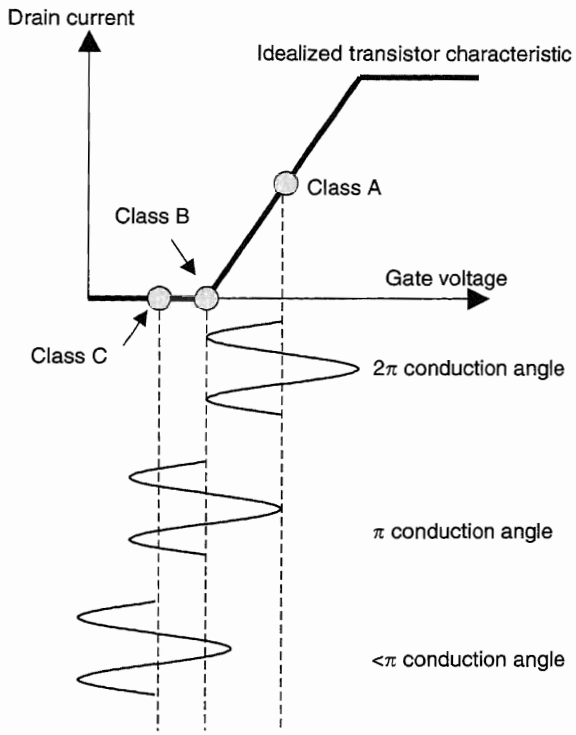


FIGURE 13.6 Conduction angle definition of class A, B, and C operations.

the transistor current, which varies from a full sinusoidal in class A to portions of a sinusoidal fc classes B and C. This determines major variations in PA efficiency calculated with Equations 13.1a through 13.2c and in other important performance parameters. Figures 13.8 through 13.10 illustrate these effects.

Theoretically, though class A is limited to 50% maximum efficiency, class B attains 78.5% effi ciency and class C tends toward 100% efficiency. A crucial aspect is the loss of efficiency as the PA

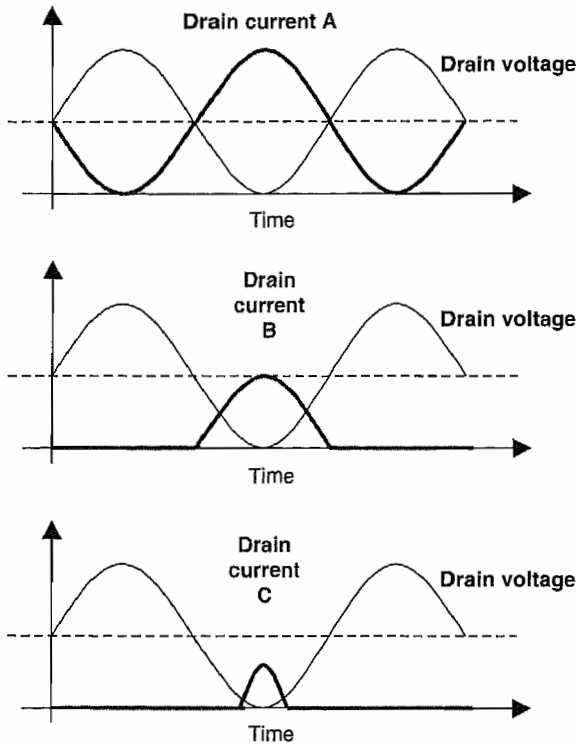


FIGURE 13.7 Drain voltage and current waveforms for class A, B, and C operations.

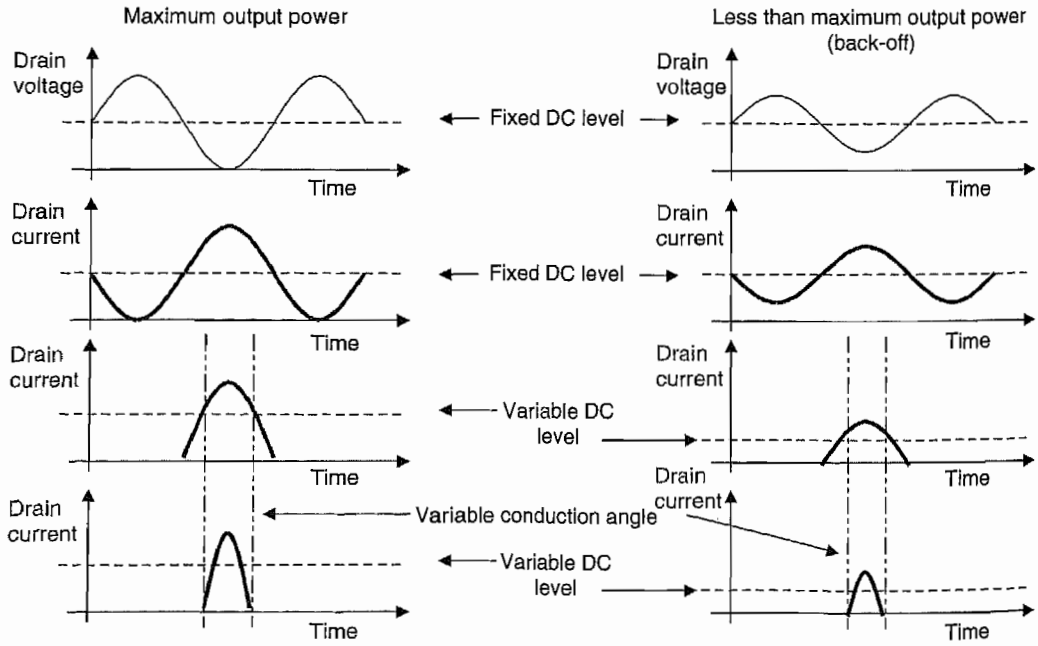


FIGURE 13.8 Drain voltage and current under power back-off conditions for class A, B, and C operations.

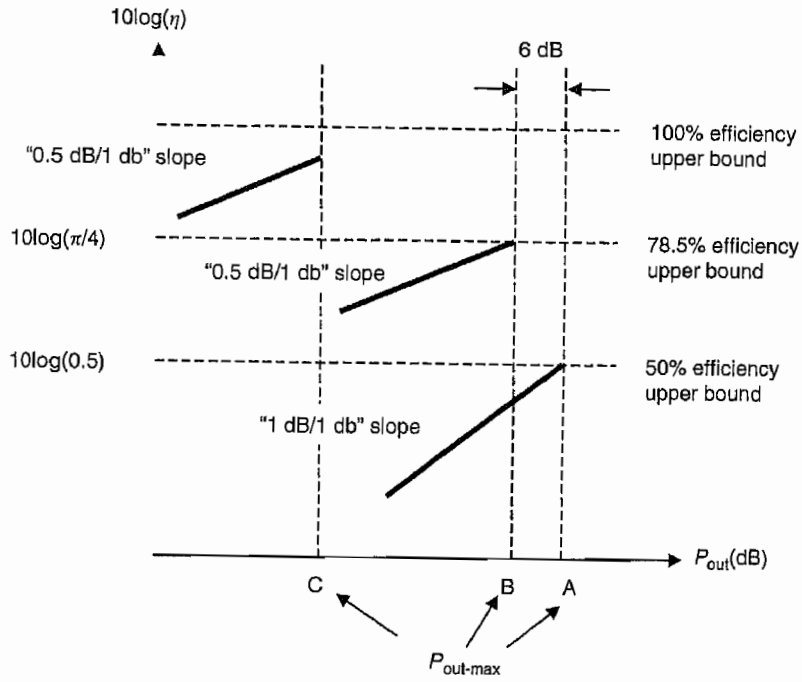


FIGURE 13.9 Power efficiency in decibels under power back-off conditions for class A, B, and C operations; same maximum input RF power is assumed.

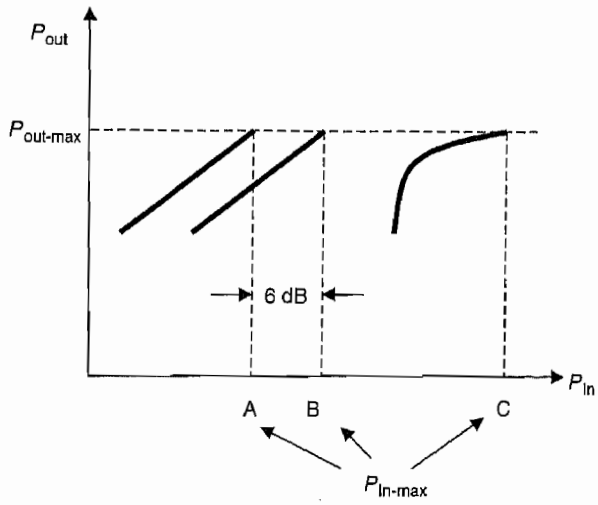


FIGURE 13.10 Output power versus RF input power for class A, B, and C operations.

output power is lowered or backed off from the peak value. Ideally, there should not be any re tion in efficiency but this is not the case. Figure 13.9 shows that class C is best in this res lowed by class B. This can be explained with the help of Figure 13.8. For class A operation value of the current signal does not change with the output power level, thus wasting effic back-off, which drops a full decibel for every decibel reduction in output power. Classes I feature a fundamentally different and valuable behavior: the DC current components decre

the output power. As a result, class B has only 0.5 dB loss in efficiency for every 1 dB reduction in output power, and so does class C.

The efficiency benefits of classes B and C compared to class A are not without penalties. An important property that only class A has is that its linearity performance is monotonic, that is, in back-off the linearity always improves [2]. This is not true in any other operation classes, including class AB, which will be discussed later.

Class C pays a particularly high price for excellent efficiency. Because of low conduction angle and low device utilization, the output power level is much reduced compared to that for classes A or B for the same input drive, as shown in Figures 13.9 and 13.10. In addition, the input/output signal characteristic changes rapidly with the output power level creating severe nonlinear effects in the output signal. For these reasons, class C operation is rarely used.

On the contrary, an ideal class B seems to be quite a good compromise between increased efficiency and a small 6 dB gain reduction compared to class A, with no loss in linearity. A simple analysis would convince the reader of this theoretical fact. Unfortunately, the ideal class B case is a poor approximation in practice since real transistors have smooth turn-on characteristics. A more appropriate model is class AB operation.

Class AB Operation

Class AB is the workhorse of linear high-efficiency RF PA applications; yet the reasons for its success cannot be explained from the idealized model shown in Figure 13.11a. According to this model, class AB is very similar to class C, as shown in Figure 13.12: good back-off efficiency due

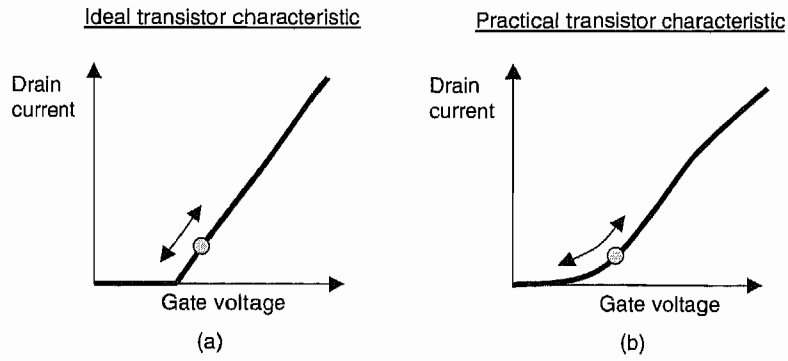


FIGURE 13.11 Class AB operation on (a) ideal transistor *I/V* characteristics and (b) real transistor *I/V* characteristics.

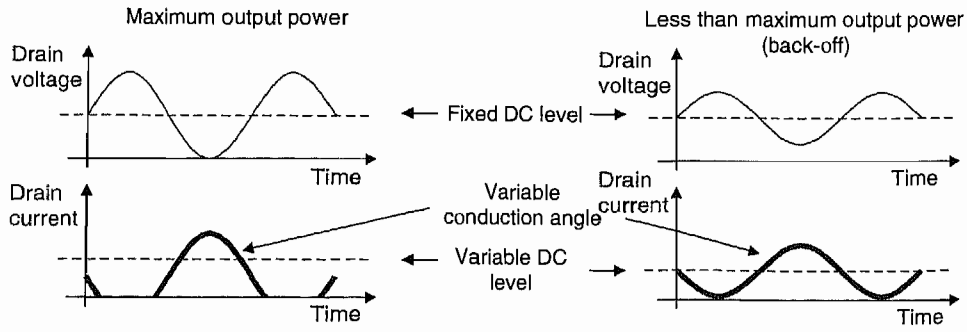


FIGURE 13.12 Drain voltage and current under peak power and back-off conditions for ideal class AB PA.

to variable current DC component but unacceptable nonlinear behavior in the output due to signal-dependent conduction angle.

The main reason class AB works well in practice is the fact that real transistor characteristics are smooth, as illustrated in Figure 13.11b. As a result, the intermodulation components of the drain current in the real transistor are quite different from those generated by the ideal curve shown in Figure 13.11a [3]. More important, these components vary with the biasing point in such a way that an optimum biasing condition exists in terms of odd-order intermodulation distortion (IMD). Care must be taken here to stress that the optimum biasing is very sensitive and difficult to find and maintain over fabrication process and temperature variations. In addition, unlike class A, the linearity performance of class AB is not monotonic and the odd IMD may get worse in back-off [2,3].

A circumstantial proof for the existence of the optimum biasing can be given with the help of Figures 13.13 and 13.14. Figure 13.13 shows the decomposition of a typical LDMOS RF-power FET *I/V* characteristics into even and odd components at the operating point. The g_m characteristic is decomposed as well and the focus is on the even g_m component, which is directly responsible for setting the IMD values. Figure 13.14 clearly shows how the even g_m component changes shape quite dramatically as a function of the biasing point. By inspection, notice that biasing at half the peak g_m value yields the minimum error ripple. In practice, the situation is complicated by many other practical factors such as transistor-parasitic capacitors, dynamic effects, etc., but the class AB nonlinear behavior remains qualitatively as described.

Starting from peak power level downwards, the back-off efficiency in class AB is practically identical to that of ideal class B, that is, the PE drops 0.5 dB for each decibel of output power reduction. Eventually, however, as the input signal gets small enough, the amplifier approaches a class A behavior due to the smooth transistor *I/V* characteristic (Figure 13.11b). As a result, the efficiency degradation gradually shifts to "1 dB per dB" roll-off. This is detrimental in applications with large back-off requirements such as code division multiple access (CDMA) PAs, which will be discussed later. A common method for mitigating this effect is to decrease the transistor bias gate voltage dynamically for low input signals and thus maintain class AB behavior. Naturally, this must be done without introducing PA linearity problems.

Switching PAs

The natural way in which a current PA becomes a switching PA is by overdriving the circuit shown in Figure 13.3 to the point of operating the transistor as a switch [2]. Figure 13.15a shows this possibility and Figure 13.15b expands this concept to a two-switch/transistor configuration by eliminating the biasing inductor. Now, the true nature of the PA as an energy converter comes in full view. The amplitude modulation can no longer be transmitted through the input port. Phase modulation is still transferred into the PA through the variable zero crossings defining the switching instances. Therefore, a first important observation about switching PAs is that they can process correctly only input signals that are phase/frequency modulated and have no amplitude modulation. However, it is still possible to pass amplitude modulation information into the PA through the power supply voltage since the output power is proportional to its value.

The main motivation for using a switching PA is the theoretical possibility of obtaining outstanding efficiency. To this end, the traditional approach is to satisfy two conditions: (a) arranging the circuit such that the transistor voltage and current overlap as little as possible, thus minimizing the loss through heat and (b) designing the lossless two-port networks shown in Figure 13.15 such that only the fundamental frequencies are allowed to pass into the output, thus avoiding harmonic power loss. As the two conditions must be met simultaneously and all signals inside the PA are strong interrelated, a high degree of design skill and knowledge is necessary to obtain a valid solu Three possibilities, which have been proposed, are known as classes D, E, and F PAs [1,2].

Figure 13.16 shows typical voltage and current waveforms for traditional switching PAs [1]. ' class D PA uses the two-transistor architecture and relies on very fast switching of the lossless two

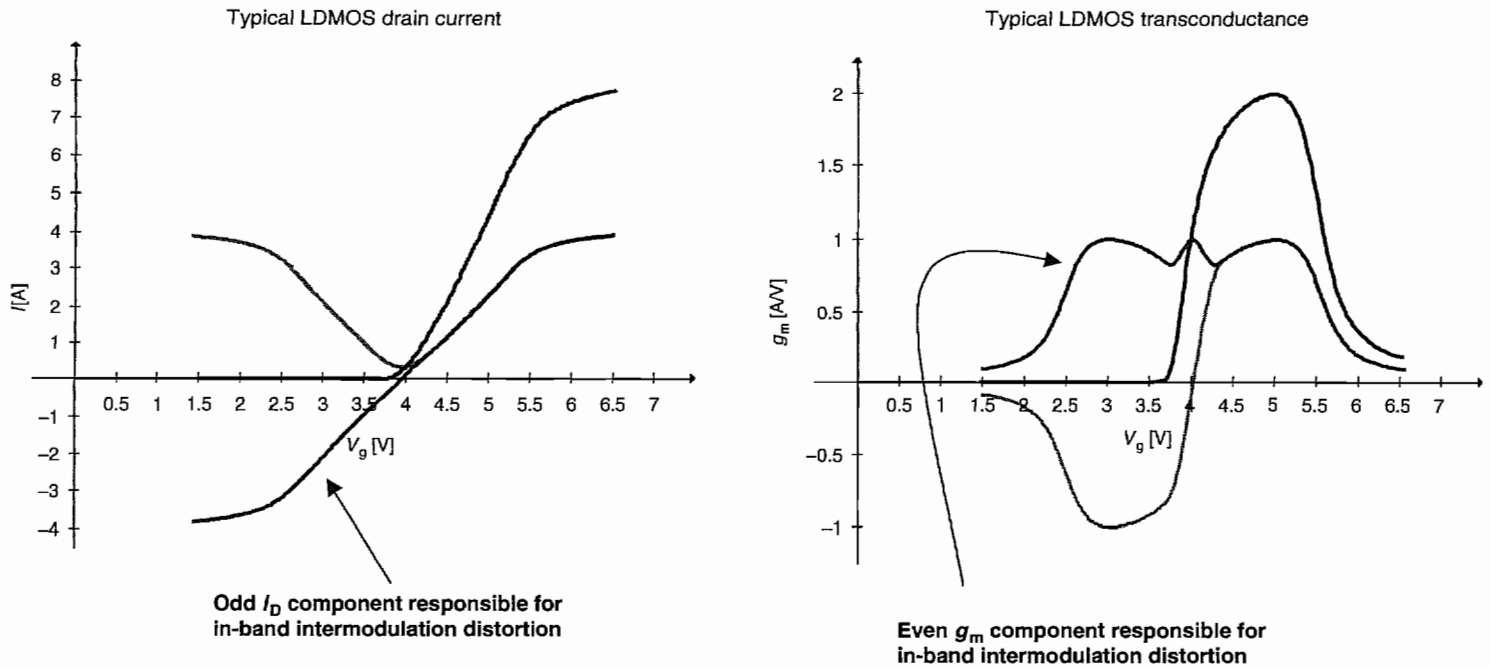


FIGURE 13.13 Decomposition of the *I*/*V* and g_m characteristics of a typical LDMOS RF power transistor into odd and even parts. (From Banu, M., Prodanov, V., and Smith, K., *Asia Pacific Microwave Conference*, 2004. With permission. © IEEE 2004.)

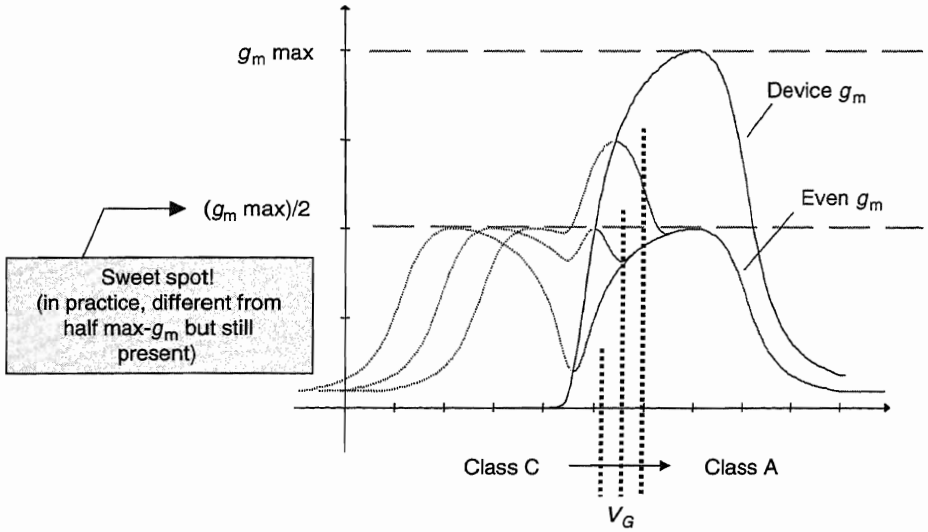


FIGURE 13.14 Simple demonstration of sweet spot biasing in real class AB operation. (From Banu, M., Prodanov, V., and Smith, K., *Asia Pacific Microwave Conference*, 2004. With permission. © IEEE 2004.)

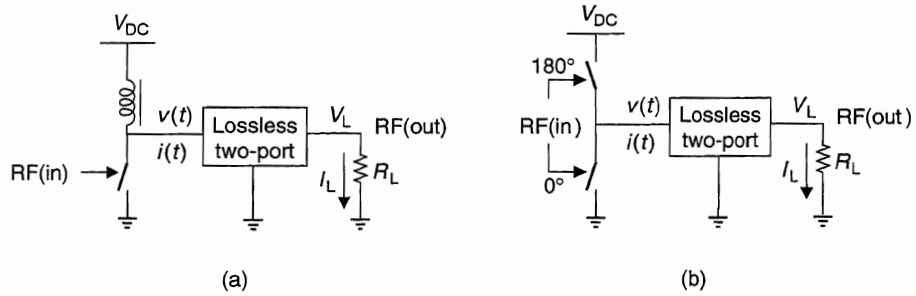


FIGURE 13.15 Switching PA architectures: (a) single-transistor architecture and (b) double-transistor architecture.

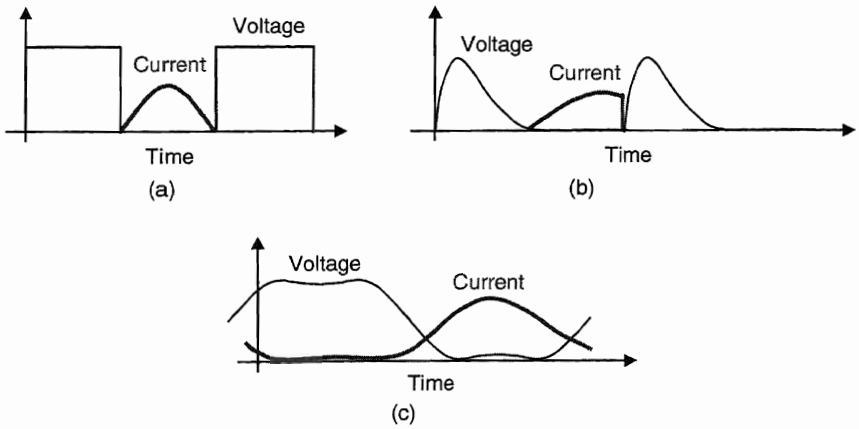


FIGURE 13.16 Typical voltage and current signals in (a) class D PA, (b) class E PA, and (c) class F PA.

input between the power supply line and ground. Figure 13.16a shows the resulting square drain voltage waveforms. For ideal switches, there is no power loss through heat, and assuming the lossless two-port is a band-pass filter rejecting all harmonics, 100% efficiency is obtained theoretically. In practice, the class D PA technology has been applied successfully at audio frequencies where switching can be realized fast enough compared to the signal bandwidth. Any reasonable application of this technique at RF has not been demonstrated yet and is plagued by unrealistically high demands on the transistor switching speeds. In addition, the losses due to drain-parasitic capacitance charging/discharging are difficult to avoid.

An RF switching PA approach that has been demonstrated in practice in the gigahertz range with better than 70% efficiency is based on class E operation [2–5]. This single-transistor PA switches the current ideally only when the voltage and its derivative are zero, thus avoiding heat losses. This is a promising approach, but it produces inherently large voltage swings, requiring transistors capable of handling such conditions [2,6]. Nevertheless, the voltage waveform shown in Figure 13.16b is substantially less abrupt than in the case of class D, hence the suitability of class E for RF applications.

The class F operation [7–10] employs a single-transistor architecture and voltage shaping improving the efficiency and the transistor utilization. Starting with class AB transistor biasing, the lossless two-port is designed to greatly enhance the third voltage harmonic to obtain an effective squaring of the voltage signal, as shown in Figure 13.16c. This increases the efficiency beyond class AB operation while maintaining the voltage swing within reasonable levels. Theoretically, fifth, seventh, and higher odd harmonics could be also enhanced for the benefit of even higher efficiency. Unfortunately, the design of the lossless two-port is quite challenging, and maintaining class F operation in back-off is problematic.

A UNIFIED GENERAL APPROACH TO PA ANALYSIS AND DESIGN

The Mathematics of Efficient DC-to-RF Conversion

An empirical observation clearly stands out from the discussion in the previous section: it seems that the only way to boost the efficiency from one PA scheme to another is by making its internal nonlinear behavior more pronounced. Mathematically this is indeed the case shown in Figure 13.3 by calculating the power flows at various frequencies in the PA and interpreting the results. The lossless two-port network is assumed AC coupled. Therefore, by construction, the DC voltage and current of the power supply are identical to those at the drain of the transistor.

In steady state, under a sinusoidal excitation of angular frequency ω_{RF} applied on the transistor gate, the drain voltage and current are periodic functions represented by the following Fourier series:

$$v(t) = V_{DC} + V_1 \cos(\omega_{RF} t + \varphi_{V_1}) + \sum_{k=2}^{\infty} V_k \cos(k\omega_{RF} t + \varphi_{V_k}) \tag{13.3a}$$

$$i(t) = I_{DC} + I_1 \cos(\omega_{RF} t + \varphi_{I_1}) + \sum_{k=2}^{\infty} I_k \cos(k\omega_{RF} t + \varphi_{I_k}) \tag{13.3b}$$

where V_k and I_k are the amplitudes and ϕ_{V_k} and ϕ_{I_k} the phases of respective harmonics. The total loss at the drain is calculated by multiplying Equations 13.3a and 13.3b and integrating over a period according to Equation 13.2c. Since all orthogonal products (i.e., voltage harmonic different from current harmonic) integrate to zero, we have

$$P_{loss} = V_{DC} I_{DC} + \frac{1}{2} V_1 I_1 \cos(\varphi_{V_1} - \varphi_{I_1}) + \frac{1}{2} \sum_{k=2}^{\infty} V_k I_k \cos(\varphi_{V_k} - \varphi_{I_k}) \tag{13.4}$$

Equation 13.4 gives important insights on how the PA converts energy from DC to RF. The total loss P_{loss} must be a positive quantity since the transistor considered as operating with full voltages and currents is a passive device (transistors do not generate power), unlike its customary model used for small-signal analysis. Furthermore, the transistor physics forces the DC drain current as defined in Figure 13.3 to be always positive, which makes the first term in the right-hand side of Equation 13.4 positive. This term is clearly identified as the power delivered into the PA by the DC power supply. The energy conservation law tells us that P_{loss} must be smaller than the DC power flowing into the PA; therefore, the second and third terms in the right-hand side of Equation 13.4 must add to a negative number. The right-hand side of Equation 13.4 can be interpreted as the superposition of the DC power flowing into the transistor from the DC power supply and a portion of it flowing out of the transistor at RF fundamental and harmonics. Since the biasing choke blocks the RF fundamental and harmonics, the only place the outgoing power can go is the PA load resistor through the lossless two-port. Thus, the PA accomplishes energy conversion: it extracts power at DC from the power supply and delivers a portion of it to the load at RF fundamental and harmonics. Next, the possibilities are analyzed to make this process power efficient, i.e., with as small P_{loss} as possible.

The second term in the right-hand side of Equation 13.4 is essential to the very function of the PA since it represents the fundamental RF power to be delivered to the PA load. This term should be negative with magnitude as large as possible. A necessary condition for this objective is to create fundamental voltage and current signals swinging in opposite directions (180° phase shift) to make the cosine factor equal to -1. This is automatically accomplished if the transistor pushes current into a real impedance. Therefore, the two-port lossless network terminated by the PA load resistor must be designed to have a real input impedance at the fundamental frequency. An equivalent way to state this is that the two-port lossless network terminated in the PA load resistor is a filter with a pass-band at the fundamental RF frequency. Naturally, the transistor-parasitic capacitances must be included in the network.

The generation of harmonic power represented by the last summing term in the right-hand side of Equation 13.4 must be eliminated for the following reasons. As discussed above in this section, any negative components in the sum would represent respective harmonic power flowing out of the transistor only to be dissipated in the PA load. This is not allowed by the PA linearity requirements (see Figure 13.4). On the contrary, any positive components in the sum would be dissipated in the transistor to the detriment of power efficiency. The only alternative left is to make the harmonic power summation zero.

Zero Harmonic Power

Ignoring the theoretical but exotic possibility of shifting power between harmonics for a zero net game, four ways of making the last summation term in Equation 13.4 null are illustrated in Figure 13.17. The two signals shown for each case in the frequency domain can be voltage or current signals interchangeably. They are members of a set of four generic signals, each containing DC and fundamental terms. In addition, the first generic signal contains no harmonics, the second generic signal contains only odd harmonics, the third generic signal contains only even harmonics, and the fourth generic signal contains all harmonics. These generic signals will be called, no-harmonic, odd-harmonic, even-harmonic, and all-harmonic, respectively. The four methods shown in Figure 13.17 combine pairs of generic signals such that the products in the summation of Equation 13.4 are only of orthogonal signals, integrating to zero over the RF input signal period.

Fundamental-to-DC Ratios

Assuming zero harmonic power as per the methods discussed in the previous subsection, the power efficiency from Equation 13.4 is calculated with the last term eliminated:

$$\mathrm{PE} = \frac{1}{2}\frac{V_1}{V_{DC}}\frac{I_1}{I_{DC}}$$

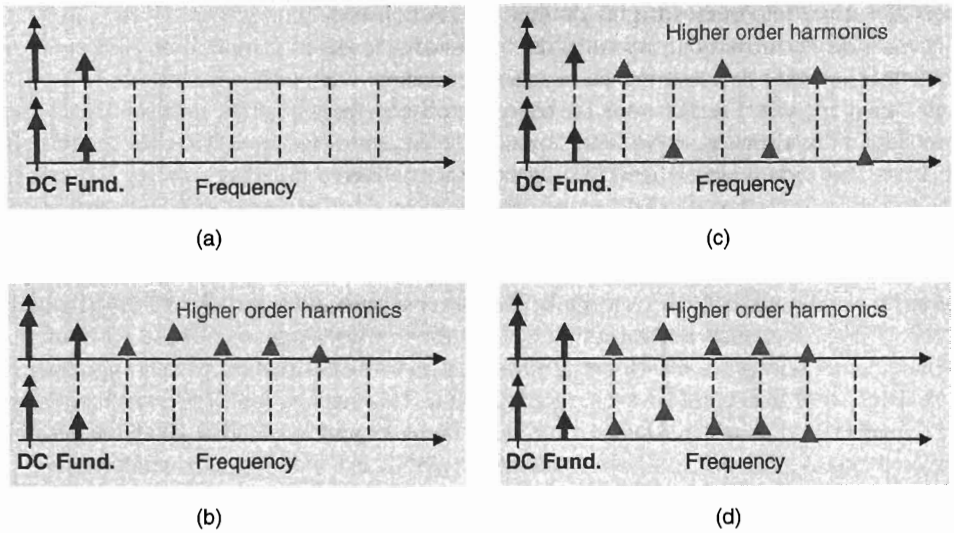


FIGURE 13.17 Pairs of internal PA signals with orthogonal harmonics: (a) two no-harmonic signals, (b) no-harmonic and all-harmonic signals, (c) odd-harmonic and even-harmonic signals, and (d) two quadrature all-harmonic signals.

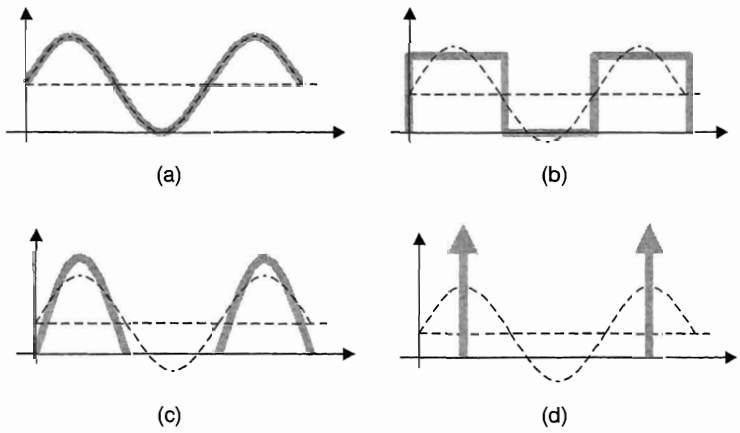


FIGURE 13.18 Signals with optimum FDC ratios: (a) no-harmonic shifted sinusoidal with FDC = 1, (b) odd-harmonic square wave with FDC = $4/\pi$, (c) even-harmonic half-wave rectified sinusoidal with FDC = $\pi/2$, and (d) all harmonic impulse with FDC = 2.

Notice that the overall PA efficiency is the product of two fundamental-component-to-DC-component (FDC) signal ratios. This gives a very important clue of what needs to be done for maximum efficiency, namely, maximizing the FDC ratios for the voltage and the current signals inside the PA. This is explicit evidence that the PA efficiency is directly linked to its internal signal harmonics, whose presence in proper amount and phasing can increase the FDC ratios. Next, this possibility under the condition of zero harmonic power is analyzed.

The transistor drain voltage and current signals as defined in Figure 13.3 must be positive on the basis of proper operation of the device. The question is, which positive functions have the maximum FDC ratio and are of the form of the generic functions discussed in the subsection "Zero Harmonic Power?" The answer is given in Figure 13.18. The positive no-harmonic function is unique and

TABLE 13.2
Efficiencies and Resulting Classes

(a) Maximum theoretical PA efficiency for different waveform pairing.

		voltage			
harmonics		none	odd	even	all
current	none	50.0 %	63.6 %	78.5 %	100 %
	odd	63.6 %		100 %	
	even	78.5 %	100 %		
	all	100 %			100 %

(b) PA operating classes corresponding to waveform pairing in (a).

		voltage			
harmonics		none	odd	even	all
current	none	A		"Inverse" B,C,D,F	
	odd				
	even	B	D/F		
	all	C			E

has an FDC ratio of 1. The odd-harmonic function with maximum FDC ratio of $4/\pi$ is a square wave, the even-harmonic function with a maximum FDC ratio of $\pi/2$ is a half-wave rectified sinusoidal, and the all-harmonic function with a maximum FDC ratio of 2 is an impulse train function. The iterative way in which these functions are constructed in the subsection " Finite Bandwidth Signals Internal to PA" ensures that they are optimum in terms of best FDC ratios for their respective class.

Pairing the Voltage and Current Signals Appropriately

Equipped with Equation 13.5 and the functions of Figure 13.18, the PA schemes discussed in the section "The Classical Approach to PA Design" can be analyzed from a unified and general point of view. For example, a class A PA uses only nonharmonic internal voltage and current functions. Equation 13.5 gives 50% efficiency, which of course is as calculated before. For ideal class B PA, the internal voltage is a no-harmonic signal, but the internal current is a half-wave rectified sinusoidal, the best even-harmonic signal. The efficiency increases to 78.5% in response to adding current harmonics. If proper odd harmonics are added to the voltage signal, e.g., use a square wave, the best even-harmonic signal, the efficiency reaches 100% and an ideal class D or F PA has been constructed. The same 100% efficiency may be obtained by using a no-harmonic signal for the internal voltage and an impulse train, the best all-harmonic signal for the internal current. This describes an ideal class C PA with infinitely small conduction angle (and infinitely large input signal or infinitely large transistor g_m).

Table 13.2a shows the efficiencies of all possible pairs of best FDC ratio signals, according to the schemes shown in Figure 13.17. Table 13.2b shows the resulting classes of PA operation. Notice that not all possible pairs have known PA configurations. Also, notice that class E operation requires voltage and current harmonics in quadrature to ensure orthogonal conditions.

Finite Bandwidth Signals Internal to PA

The previous analysis of ideal PAs assumed that internal signals with infinite bandwidths could be used. In reality, of course, this is not the case. For this reason, it is important to determine the effect of limited bandwidths inside the PA on efficiency. To be able to do this, the generic signals discussed

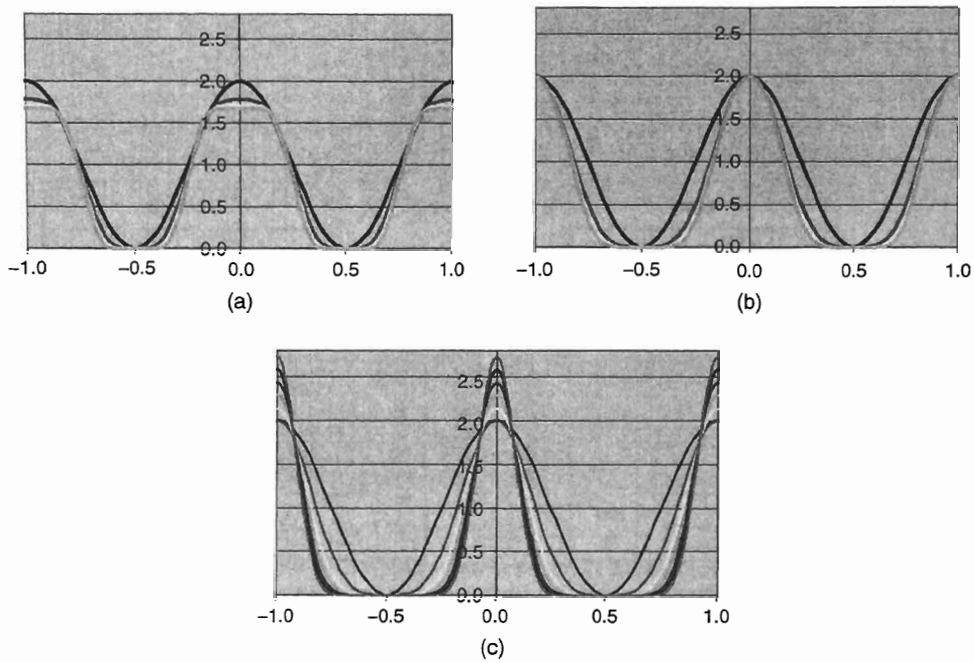


FIGURE 13.19 Series of functions with increasing number of harmonics and FDC ratios: (a) odd-harmonic functions converging to a square wave, (b) even-harmonic functions converging to a half-wave rectified sinusoidal, and (c) all-harmonic functions converging to an impulse.

in the subsection "Zero Harmonic Power" are first constructed not as infinite but rather as limited bandwidth signals, i.e., allowing only a limited number of harmonics [6,8–11].

Figure 13.19a shows graphically a series of odd-harmonic signals with increasingly larger number of harmonics. For each signal, the harmonic content is calculated so as to create zero derivatives at the midpoint in the fundamental cycle up to $(N-1)$th order derivative, where N is the number of harmonics. In this way, it is ensured that the function reaches a minimum at that point and it is as flat as possible. The fundamental component is increased to place the minimum point at zero value. As the number of harmonics increases, these functions resemble more and more a square wave, and in the limit (infinite number of harmonics), they become a square wave.

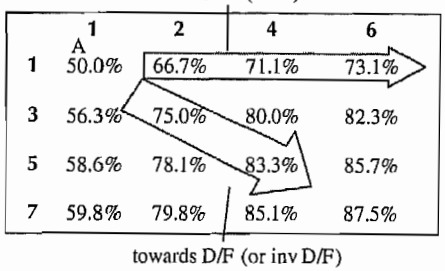
The same construction can be done for even-harmonic functions; the result is shown in Figure 13.19b. Here, in the limit, the half-wave rectified sinusoidal function is recovered. Finally, the all-harmonic functions shown in Figure 13.19c synthesized in a similar manner converge toward an impulse function. In all three series, the FDC ratio increases with the number of harmonics.

Efficiency in the Presence of Finite Bandwidth

On the basis of the functions from Figure 13.19 and the same signal pairing as in Figure 13.17, PA efficiencies can be calculated for various internal PA bandwidths. Table 13.3a summarizes the results for the pairing case in Figure 13.17c up to the seventh harmonic. The good news is that the efficiency increases rapidly, reaching respectable numbers without an excessive number of harmonics. For example, a class B PA (class AB practically the same) with up to sixth-order harmonics in the current has already 73.1% efficiency. Similarly, Table 13.3b representing the pairing from Figure 13.17b shows that a class C PA with only fourth-order harmonics reaches 80% efficiency. On the contrary, it is also clear that trying to push efficiency to even higher levels would be very challenging for RF PAs due to very high bandwidth demands.

TABLE 13.3
Efficiency Tables

(a) Harmonics in voltage and current waveforms.



(b) Harmonics only in voltage or current waveform.

Max. Harmonic	1	2	3	4	5	6	7
Efficiency	50.0%	66.7%	75.0%	80.0%	83.3%	85.7%	87.5%

A → toward C (invC)

A final observation is made by comparing the entries in Table 13.3a on a diagonal from top left to bottom right and those of Table 13.3b. The efficiency numbers are identical for identical number of total harmonics irrespective of which signals contain these harmonics. In other words, at this high-level explanation, the efficiency is independent of the actual PA configuration and depends only on the number of harmonics used internally. Given N internal PA harmonics, the following simple relation can be used to estimate efficiency:

$$\mathrm{PE} \leq \frac{N}{1+N} \tag{13.6}$$

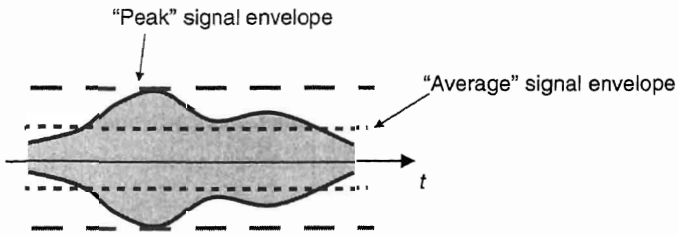
PA TECHNIQUES FOR POWER BACK-OFF APPLICATIONS

Reasons for Back-Off Requirements and Efficiency Penalties

The efficiency of PAs in back-off operation was considered previously. This aspect is crucial for RF applications using amplitude modulation. In the subsection "Relative Signal Bandwidth for Most Modern PAs," it is mentioned that the PA input RF signal looks sinusoidal for short durations. However, if amplitude modulation is present, the magnitude of this sinusoidal signal varies over long time, as shown in Figure 13.20. A traditional way to describe this magnitude variation is as the ratio between the peak power and the average power of the RF signal, known as peak-to-average ratio (PAR), usually expressed in decibels [1,2]. The typical statistics of real communication signals are such that peak power actually occurs infrequently.

The PAs must be designed and operated to handle the input signal correctly at all times without ever entering compression. The simplest way to accomplish this is by designing the PA for proper operation at expected peak power. Naturally, most of the time, the PA will be underutilized delivering only average power and thus be effectively backed off by the PAR value. The net result is that the PA average efficiency is not as given at peak power value but rather at some effective back-off value, depending on the signal statistics. The larger the signal PAR, the more backed-off the PA will be and the more severe the penalty in average efficiency.

The recent introduction of wideband digital wireless communication systems such as those based on CDMA or 802.11a/g standards has placed to center stage the PA efficiency problem in back-off operation. Nevertheless, this is not a new problem. The commercial amplitude modulation (AM)



- PAs must operate properly for worst-case signal conditions, i.e., peak power conditions.
- PA must be backed off from rated power by signal PAR (e.g., CDMA-2000: 4–9 dB, W-CDMA 3.5–7 dB, 802.11a/g: 6–17 dB).
- Efficiency suffers under back-off conditions.

FIGURE 13.20 Peak and average power levels in an amplitude-modulated RF signal.

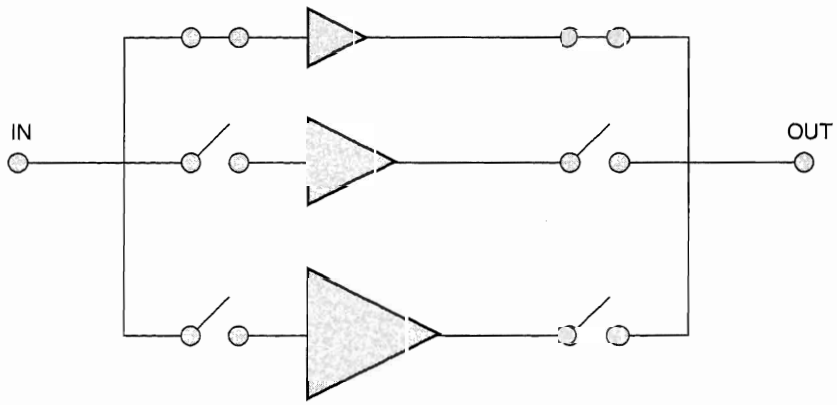


FIGURE 13.21 Conceptual PA subranging architecture.

broadcast industry has encountered and solved this issue for high-power PAs with system-level techniques, albeit using conventional RF technology, which is too expensive and bulky for modern portable devices [12–15]. Recently, there has been a considerable renewed interest in these system techniques [3,16,17] with a focus on trying to apply them to modern low- and medium-power PAs using integrated circuit (IC) technology. The most important system concepts for increased efficiency PAs in back-off is reviewed next.

PA Subranging

A brute-force solution to the back-off efficiency problem is shown conceptually in Figure 13.21. Several PA segments of increasing output power are placed in parallel and switched on and off appropriately by the transmitter system such that the RF output signal is always processed by a PA segment operating close to its peak power and efficiency. This is possible in theory because the transmitter system knows in advance the information to be transmitted and can bring on line the appropriate PA segment at the right time. This strategy increases substantially the average efficiency of the overall PA.

The challenge in implementing the scheme shown in Figure 13.21 comes from the input and output interfacing networks, which must provide "smooth" RF switching without major impedance changes and with low loss. A less demanding application of this architecture is power control, to be discussed in the section "Additional PA Considerations."

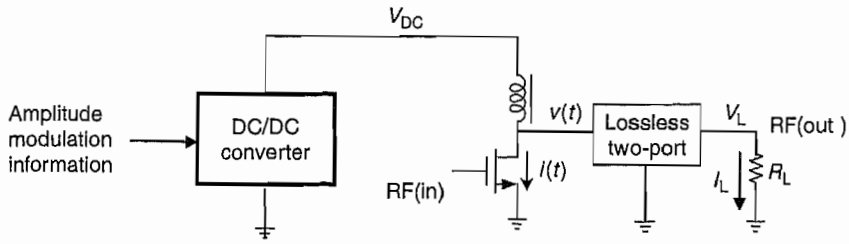


FIGURE 13.22 Envelope tracking and following PA concept.

Envelope Tracking

A more sophisticated technique is illustrated in Figure 13.22 and is based on the observation that the back-off efficiency of a class AB PA can be boosted by lowering the power supply voltage dynamically when the signal magnitude decreases. The core PA consists of the transistor, the inductor, and the lossless matching network. The DC power supply is an agile DC-to-DC converter capable of delivering the necessary PA current for a discrete set of output voltages under the control of an input terminal. The purpose of this converter is to change the supply voltage dynamically according to the RF amplitude modulation so as to operate the class AB PA at or close to its peak efficiency for all input signal levels between average and peak power. In effect, the transistor drain voltage always swings close to the full power supply voltage, which is dynamically changed. The voltage FDC ratio remains near unity independent of signal magnitude for close to peak efficiency in back-off.

Two conditions must be met for the proper operation of this scheme. First, the agility of the DC-to-DC converter must match or be better than the baseband signal bandwidth, which equals the amplitude modulation bandwidth. Second, the efficiency of the DC-to-DC converter must be good enough to make the overall system more efficient than a classical class AB PA. In the case of power control back-off, the bandwidth condition is relaxed.

Envelope Following

The envelope tracking concept requires that the power supply voltage generated by the DC-to-DC converter follows only roughly the signal magnitude for the sole purpose of increasing the average PA efficiency. Theoretically, one can imagine the power supply voltage following exactly the signal envelope, in which case the method is called envelope following [17].

When the circuit uses a current PA, the additional improvement in efficiency envelope following brings is minimal when compared to envelope tracking and does not justify the extra precision requirements for the DC-to-DC converter. Envelope following becomes an attractive option if instead of the current PA we use a switching design, such as a class E PA. In this case, the DC-to-DC converter provides the amplitude modulation information through the power supply line, and the switching PA generates the output power extremely efficiently [18].

Envelope Elimination and Reconstruction

A particular version of the envelope following concept, which was historically first proposed by Kahn, is envelope elimination and restoration (EER) [14]. Figure 13.23 illustrates this design, which predates baseband digital signal processors (DSPs). Here, the RF input is first processed by analog blocks, and the amplitude modulation information is separated from the RF signal and converted into a baseband signal. The remaining constant-envelope RF signal drives a switching RF PA with excellent efficiency and the amplitude modulation is reintroduced through the power supply voltage. The latter is driven by an efficient baseband PA. A critical and challenging issue in this technique is the correct synchronization between amplitude and phase.

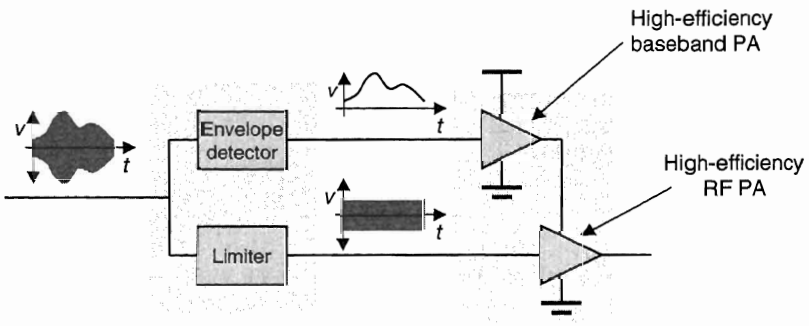


FIGURE 13.23 Envelope elimination and restoration PA concept.

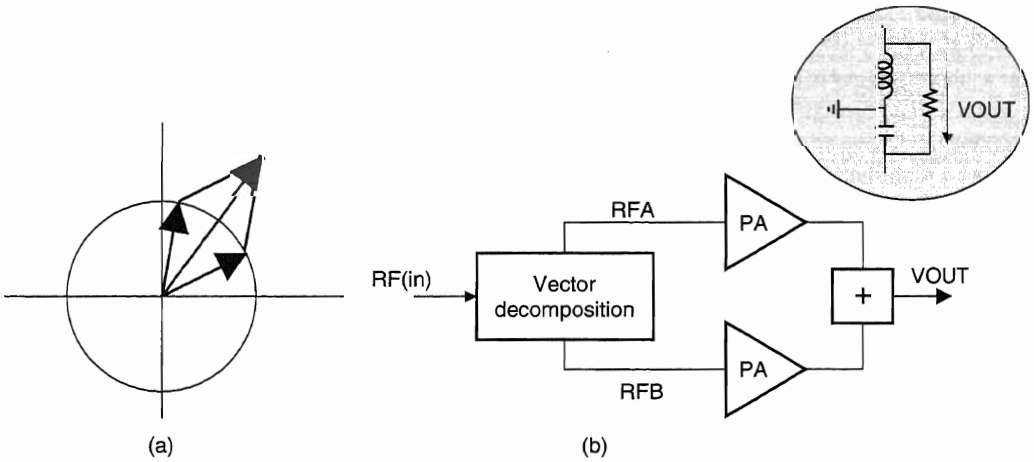


FIGURE 13.24 Out-phasing PA concept.

Kahn's EER scheme is less attractive when digital baseband processing is available. In this case, it makes more sense to generate the amplitude and phase signals directly from the DSP rather than decomposing an analog RF signal, whose phase and amplitude components were originally created by the DSP in the first place. The EER structure without the signal decomposition part is known as a polar transmitter [19].

The Out-Phasing PA

This concept is explained in Figure 13.24a where the RF signal is represented as a rotating vector with time-variable magnitude and angular velocity. From simple geometrical considerations, clearly it is possible to decompose this vector into two new rotating vectors with constant magnitudes, as shown in the figure. Therefore, all information contained in a modulated RF signal can be also represented in a pair of constant-envelope signals. This is a convenient representation for efficient power conversion of the two components based on switching PAs.

Figure 13.24b shows the Chireix first implementation of this concept [12], before the availability of DSPs. First, two constant-envelope components are derived from decomposition of the RF signal. Today, this would be done by the DSP [20] like in the polar transmitter case [19]. Then, these components are passed through two efficient switching PAs. Finally, an output power-combining network recreates the original RF vector. The design of the combining network is quite critical and is the potential Achilles' heel of this technique. This is discussed next.

A simple analysis would convince the reader that the process of combining two constant-envelope vectors through a simple vector addition, i.e., by conventional power combining, is fundamentally inefficient if the two signals are not in phase. Any vector components canceling each other dissipate

power. For example, in the worst case when the two constant-envelope vectors are in opposite phases, all their power gets dissipated and no power is produced at the output for 0% efficiency. Chireix recognized that traditional power combining is not an acceptable solution and proposed a fully differential load connection as shown in the Figure 13.24 inset. This configuration solves the efficiency problem but introduces a major PA-loading problem. The effective loads seen by each PA are not purely resistive as assumed in the standard design of the PAs but rather contain large reactive components. Even more troublesome is the fact that these reactive components depend on the angle separating the two vectors, which is constantly changing with the modulation. A compensation of these reactive components is possible, as shown in the figure inset, with the addition of a capacitor and an inductor, but this compensation is valid only around a unique separation angle. Chireix made this technique work with substantially better back-off efficiency than the class AB case for the AM broadcasting application.

The Doherty PA

The Doherty concept [13] is shown in Figure 13.25 and in some respects may be viewed as a very ingenious analog version of the PA subranging idea. It contains a main amplifier, which is always on, and a secondary or peaking amplifier, which turns on only when the input signal power exceeds a predetermined threshold, e.g., 6 dB below maximum PA power if the two transistors are identical. The classical implementation uses a class AB main amplifier and a class C peaking amplifier with identical transistors [2,3]. A single inductor is sufficient to bias the drain of both transistors at the power supply voltage.

The key Doherty innovation is combining the two transistor drain currents via a quarter-wave transformer, as shown in Figure 13.25. The quarter-wave transformer, which in practice is a piece of transmission line, converts the input current of one port into a voltage output at the other port. The same action is achieved using a symmetric LC π network. For input power levels, when only the main transistor is on, its drain current is converted linearly into a voltage applied to the load, just as in a regular PA. When the peaking transistor turns on and pushes RF current into the quarter-wave transformer, a differential RF voltage is generated at the drain of the main transistor. Phasing the drain RF current of the peaking transistor correctly, e.g., shifting the input RF signal by a quarter-wavelength before applying it to the peaking transistor gate, has the effect of lowering the RF voltage swing at the main transistor drain. This creates voltage headroom for the main transistor, which now can push higher RF currents before reaching current saturation. The system is adjusted such that the drain RF voltage swing of the main transistor remains constant after the input power increases beyond the triggering level of the peaking transistor. In this way, the main transistor keeps

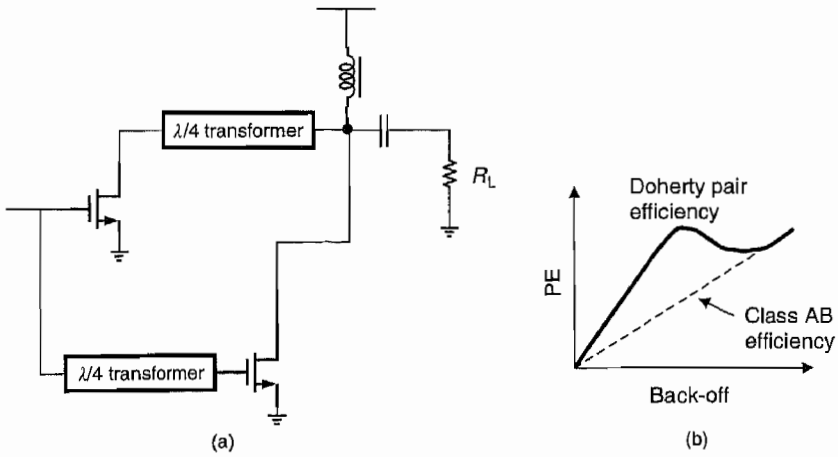


FIGURE 13.25 Doherty PA concept.

pumping higher power into the load but at lower rate since only its RF current increases. The peaking transistor naturally supplies exactly the amount of additional power necessary to have a linear power-in/power-out overall characteristic.

The advantage of the Doherty configuration is in terms of the PA efficiency. For low power levels, one quarter of the maximum power or less, when only the main transistor is on, the PA performance equals that of a class AB case. The maximum efficiency is reached when the drain voltage swings approximately as much as the power supply voltage for half of the total current the main transistor can deliver. This happens just before the peaking transistor turns on at a quarter of the PA total power capability, i.e., at 6 dB back-off. At this point, the drain of the peaking transistor, which is still off, swings approximately half the power supply voltage, driven by the main transistor. By increasing the input signal further, the peaking transistor turns on and starts delivering power with good efficiency from the start due to the presence of a substantial RF voltage at its drain. The peaking transistor efficiency increases with the input signal reaching the maximum value when the PA delivers maximum power. The overall PA efficiency is shown in Figure 13.23, a major improvement compared to conventional class AB.

ADDITIONAL PA CONSIDERATIONS

Power Control

An important practical issue related to the PA efficiency is power control. Typical wireless standards prescribe various transmitter output power levels for various operation modes and some require dynamic power changes. RF PAs are usually designed for specific applications and support appropriate power control capabilities. Naturally, having good efficiency in all power modes is highly desirable [16].

Many of the efficiency enhancement techniques discussed in the previous section inherently support power control, since the latter is a form of back-off operation from maximum possible PA power. Nevertheless, power control may require orders of magnitude higher range than in the usual signal-induced back-off operation, but the system response agility to power control changes is not particularly demanding. Some practical details of this PA aspect will be addressed via examples in the section "Current PA Technology and Recent Developments."

Linearity

The important topic of PA linearity and methods for improving it is a vast area of knowledge beyond the scope of this treatment (see, for example, Refs. 1–3). The discussion here is limited to the observation that two general wireless transmitter specifications address the PA linearity performance: (a) the output spectral mask and (b) the error vector magnitude (EVM) of the output signal.

The spectral mask specification is concerned with protecting the communication channels in the system from excessive noise generated by transmitting devices not using the respective channels. The EVM specification is concerned with the communication link signal-to-noise ratio (SNR) budget and allocates a maximum SNR loss in the transmitter including the PA. Depending on the wireless standard, the actual PA design is limited either by the spectral mask specifications as in the global system for mobile communication (GSM) or by the EVM specifications as in 802.11b/g. As a general rule, the higher the data rate supported by a communication system per unit of bandwidth, the more important EVM is since deeper modulation formats must be used with less room for errors.

CURRENT PA TECHNOLOGY AND RECENT DEVELOPMENTS

Wireless System PAs in the Real World

The theory presented thus far can be used to understand the commercially deployed RF PAs and the recent PA research results. Each real PA targets a specific wireless application among many wireless

TABLE 13.4
PAR, Bandwidth, and Power Control Specifications

	PAR (dB)	Signal Bandwidth (MHz)	Power Control (dB)
AMPS, GSM, GPRS, EDGE	Low (~0, ~3.2)	Small (≤0.2)	Moderate (≤30)
CDMA, CDMA2000, WCDMA	Moderate (3–5)	Large (1.23, 3.84)	Very large (70–80)
IEEE 802.11a, IEEE 802.11g	Large (>7)	Very large (~17)	N/A

systems and standards. Nevertheless, some systems have enough commonality in their specifications to prompt very similar PA solutions. The key specifications determining the PA design approach are the RF signal PAR and bandwidth, and the requirements for power control. Table 13.4 shows how popular wireless systems compare in terms of these specifications. The PAs we discuss next can be grouped into similar design and performance categories.

PAs FOR AMPS, GSM, AND GPRS

Advanced mobile phone system (AMPS) uses old-fashioned frequency modulation, whereas GSM and general packet radio service (GPRS) employ Gaussian minimum shift keying (GMSK) [18]. Since in all three cases, the RF signal PAR is near 0 dB, the PAs are operated in high-efficiency switching/saturation mode at high power levels. The power control strategies include lowering the drain DC voltage [21] or reducing the input RF signal allowing the PA to enter current mode operation at lower power levels.

Most present 824–849 MHz AMPS PAs are designed as dual-mode CDMA/AMPS solutions implemented with gallium arsenide (GaAs) or gallium indium phosphide (GaInP) transistors. These circuits support CDMA in optimized preferred mode as current PAs and are used for AMPS in legacy mode as switching PAs. The AMPS operation delivers respectable performance such as 31 dBm output power with 50% PAE from a 3.4 V power supply [22]. The 25 dB power control required by AMPS is a subset of the much tougher 73 dB of CDMA [18] to be discussed later.

The typical GSM/GPRS PAs are quad-band multichip modules (MCMs) containing two circuits, each covering adjacent bands: 824–849/880–915 MHz and 1710–1785/1850–1910 MHz. GaAs or InGaP transistors are used and the RF input/output are prematched to 50 Ω. At nominal 3.5 V battery voltage and 25°C, these amplifiers deliver 35 dBm power in the U.S. Cellular/enhanced GSM (EGSM) bands and 33 dBm power in the digital cellular communication system (DCS)/personal communication services (PCS) bands with average PAE (over different products) better than 55 and 52%, respectively [21].

The GSM/GPRS MCMs include a CMOS power control circuit accepting an analog voltage and producing PA internal control signals. The typical power control range is in excess of 50 dB [21], the system requirement being 30 dB [18].

In the last 10 years a substantial research effort has targeted the demonstration of class E CMOS PAs for GSM with 40% or better PAE, motivated by lowering the cost of present solutions [23–25]. Ref. 23 reports a 0.35 μm CMOS differential two-stage design delivering 1 W at 1.9 GHz with 48% PAE from a 2 V supply. A board microstrip balun is used for differential to single-ended conversion. The PAE including the balun is 41%.

The two-stage 0.25 μm CMOS PA reported in Ref. 24 has an output cascode transistor used to avoid the device voltage overstress. Powered from a 1.8 V DC supply, the circuit delivers 0.9 W of power at 900 MHz with 41% PAE. The output drain efficiency is larger than 45% and remains above 40% for supply voltages as low as 0.6 V, demonstrating the excellent power control capability of class E PAs.

Ref. 25 demonstrates a 0.13 μm CMOS class E PA for 1.4–2.0 GHz operation. Similar to the one used in Ref. 24, a cascode device is used in the output stage. The circuit operates from 1.3 V supply and delivers 23 dBm with 67% PAE at 1.7 GHz. The PAE is better than 60% over the entire band.

PAs for EDGE

Enhanced data for GSM evolution (EDGE), a GSM upgrade, uses the same 200 kHz channelization but introduces 8 phase shift keying (8PSK) modulation for a 3× increase in raw data rate. This comes at the expense of 3.2 dB signal PAR, which dictates a different approach to the PA design. To meet the spectral mask and EVM requirements, it is customary to use class AB current/linear PAs operated 2.5–3 dB below 1 dB compression. The resulting PAE penalty compared to GSM PAs is significant. Typically, an EDGE PA with 3.5 V supply providing 29 dBm power in the U.S. Cellular/EGSM bands and 28 dBm power in the DCS/PCS bands has only 25% PAE [26].

Because of moderate PAR and narrow signal bandwidth, EDGE is an excellent system candidate for polar PA application [18,19,27]. Research efforts in this direction [28,29] have focused on using supply-modulated class E PAs.

The 0.18 μm CMOS circuit discussed in Ref. 28 is a three-stage design, the last stage powered by a linear regulator for amplitude modulation insertion. In addition, the last stage and the linear regulator use tick-oxide transistors operating from 3.3 V supply unlike the rest of the circuit using 1.8 V supply. A peak CW output power of 27 dBm was measured at 34% PAE. The design met the EDGE EVM and spectral mask requirements in the DCS band at 23.8 dBm power with 22% PAE.

The class E PA discussed in Ref. 29 is integrated in 0.18 μm BiCMOS SiGe technology, has a single stage, and operates at 881 MHz. All necessary passive components except the choke coil are included on-chip. At the peak 22.5 dBm output power, the CW PE and PAE are 72.5 and 65.6%, respectively, operating from a 3.3 V supply. This PA does not contain the amplitude modulation driver, which is an external, discrete switching converter with 5 MHz bandwidth and 82.6% efficiency. The overall configuration meets the EVM and the spectral mask requirements for EDGE at 20.4 dBm power with better than 44% PAE.

PAs for CDMA and WCDMA

CDMA and WCDMA use MHz signal bandwidths and a coding scheme generating RF signals with high PAR. For example, the downlink signal composed of many superimposed CDMA channels addressing all active mobile units regularly exceeds 10 dB PAR [30]. This makes the design of efficient base station CDMA PAs extremely challenging. The PAR of the uplink signal containing a single channel is smaller and the handset PA design seems easier by comparison, but is no small feat in absolute terms. It is not surprising that the CDMA PA design problem has generated a large amount of activities and ideas [33–40]. The most successful CDMA PA approach to date is class AB with efficiency enhancements, but other techniques are also considered.

Table 13.5 shows typical specifications of commercial CDMA and WCDMA handset PAs. Somewhat surprisingly to a reader unfamiliar to the CDMA systems, the PA vendors quote PAE at 28 dBm and 16 dBm power. The 28 dBm figure is good but almost irrelevant since handsets rarely transmit at this level, the most likely transmit power being 5–6 dBm. The CDMA system's proper operation relies on very wide mobile unit power control, as shown in Table 13.4. This complicates the efficient handset PA design by a large degree.

TABLE 13.5
Typical Power/Gain/PAE Performance for Commercial CDMA and WCDMA PAs

	824–849 MHz	1850–1910 MHz	1920–1910 MHz
CDMA	28 dBm/28 dB/37% at 3.4 V	28 dBm/27 dB/39% at 3.4 V	
	16 dBm/25 dB/8% at 3.4 V	16 dBm/21 dB/8% at 3.4 V	
WCDMA	28 dBm/27 dB/43% at 3.4 V	28 dBm/27 dB/37% at 3.4 V	28 dBm/27 dB/42% at 3.4 V
	16 dBm/16 dB/19% at 3.4 V	16 dBm/25 dB/21% at 3.4 V	16 dBm/21 dB/15% at 3.4 V
	7 dBm/15 dB/14% at 1.5 V		7 dBm/24 dB/20 % at 1.5 V

A common method used in CDMA PAs to mitigate the efficiency problem due to large power control is quiescent operation adaptation [16] as discussed in the subsection "Class AB Operation." Another method is the power supply adaptation according to the envelope tracking technique [16,17]. Agile DC-to-DC converters with over 90% efficiency capable of adjusting the PA output power by 1 dB every 1.2 ms as required in CDMA are readily available [31,32]. Further activities are reported in stand-alone agile DC-to-DC converters [33–35] as well as DC-to-DC converters cointegrated with class AB PAs [36].

PA subranging is also effective for power control without excessive efficiency degradation as adopted in Refs. 37 and 38 using two PA segments. A three-segment PA is described in Ref. 39 and transformer-based subranging in Ref. 40. We also mention a 3-bit binary subranging PA reported in Ref. 41.

Finally, the CDMA efficiency problem has motivated a serious reconsideration of the classical Doherty and Chireix concepts [20,42–44]. In Ref. 42, a 0.5 W extended Doherty (peak efficiency at 12 dB back-off) has been implemented using discrete indium gallium phosphide (InGaP)/GaAs HBTs and microstrip quarter-wave transformers. The circuit operates at 950 MHz, delivering 27.5 dBm power at 1 dB compression with 46% PAE. PAE of better than 39% is maintained over the entire 0–12 dB back-off region and 15% is measured at 20 dB back-off. Design considerations and board-level implementations of three-stage WCDMA (1920–1980 MHz) Doherty amplifiers using 10 V GaAs field effect transistors (FETs) can be found in Ref. 43. The amplifier meets WCDMA linearity requirements up to 33 dBm with 48.5% PAE. The measured PAE at 27 dBm (6 dB back-off) and 21 dBm (12 dB back-off) are 42 and 27%, respectively. The 3 dB bandwidth of these amplifiers is broad enough to accommodate the WCDMA uplink reliably.

Similarly, a Chireix out-phasing PA for WCDMA 2110–2170 MHz downlink is discussed in Ref. 20. The circuit uses a pair of saturated class B amplifiers implemented with two 0.25 μm p-channel high electron mobility transistors (pHEMPTs), which are bare-die bonded on a printed circuit board (PCB). These circuits deliver 34.5 dBm from 5 V supply with PE and PAE of 75 and 54%, respectively. The Chireix combiner and matching circuits are implemented using on-board microstrip lines.

PAs for IEEE 802.11a/b/g

The typical performance of commercial IEEE 802.11 PAs operating from a 3.3 V power supply [45,46] is summarized in Table 13.6. The 6.5–8 dB difference between the 1 dB compression point P_{1dB} and the orthogonal frequency division multiplexing (OFDM) signal power $P_{OFDM(max)}$ is consistent with the large PAR of 64-QAM OFDM. Despite using identical signaling, the 802.11a PA efficiency is approximately 2× smaller than that of the 802.11g PA. This is a consequence of operation at much higher frequencies. The 802.11g parts support IEEE 802.11b CCK signaling with lower PAR. In CCK mode, the PAs can be operated with less back-off and much improved PAE. Typically, an 802.11b/g PA with 26.5 dBm P_{1dB} delivers approximately 23 dBm CCK power with 30% PAE [45].

Current research efforts target the implementation of 802.11 PAs with acceptable PAE in Si technologies [47], the development of methods for reducing EVM and improving efficiency by reduction of AM–PM distortion, and the introduction of previously discussed power-efficient PA schemes [48,49].

TABLE 13.6
Typical Performance for Commercial 802.11 PAs

	Gain (dB)	P_{1dB} (dBm)	$P_{OFDM(max)}$ (64 QAM with EVM ~3%) (dBm)	PAE@ $P_{OFDM(max)}$ (%)
IEEE 802.1g	25.5	26.5	19	25
IEEE 802.11a	21	26	18	3

Class AB g_m Ratio Biasing

This section is concluded with a description of a recent contribution on a promising new biasing technique for the class AB PA [50,51]. The class AB stage is one of the most important PA building blocks either as a stand-alone linear stage or as part of a more sophisticated scheme such as the Doherty PA. The motivation for this work is the fact that maintaining proper class AB biasing under all fabrication and temperature conditions is a challenging circuit design task due to the high sensitivity of the PA linearity to the biasing conditions. During the investigation on this matter, a new circuit design concept was discovered, which not only seems to solve the current PA biasing problem very efficiently but also gives a new insight into the transistor class AB operation.

The standard biasing technique for current/linear PAs is known as constant I_{DQ} biasing, where I_{DQ} is the transistor quiescent drain current. As the name suggests, the main objective of the biasing circuits is to maintain a constant I_{DQ} over all operating conditions. The types of practical circuits trying to accomplish this objective are either open-loop, developing the right quiescent gate voltage through an independent circuit, or closed-loop via an analog or digital control system measuring I_{DQ} and keeping it constant through negative feedback. Both types of techniques have important shortcomings. The open-loop methods are not precise enough for the high PA sensitivity and the closed-loop methods can guarantee the right I_{DQ} only when the RF signal is not present and are not able to correct for biasing drift during the PA operation. Regarding the open-loop methods, it is stressed that the use of a conventional current mirror is quite challenging due to RF coupling from the PA transistor into the mirror transistor, which can shift the quiescent gate voltage enough to create biasing errors.

The reasons why PA designers use constant I_{DQ} biasing are mostly pragmatic rather than based on any solid theoretical justification. Laboratory tests simply show that a good linearity compromise over temperature variations is obtained for constant I_{DQ}. It is also known that fabrication process variations require slightly different I_{DQ} values for different process corners for best linearity performance. For manufacturing cost reasons, I_{DQ} is rarely tuned for individual PA during production, so the actual shipped PA is usually not operating at its best.

The new principle called constant-g_m-ratio biasing is shown in Figure 13.26 and effectively implements a differential current mirror [50]. Instead of copying a current as in conventional current

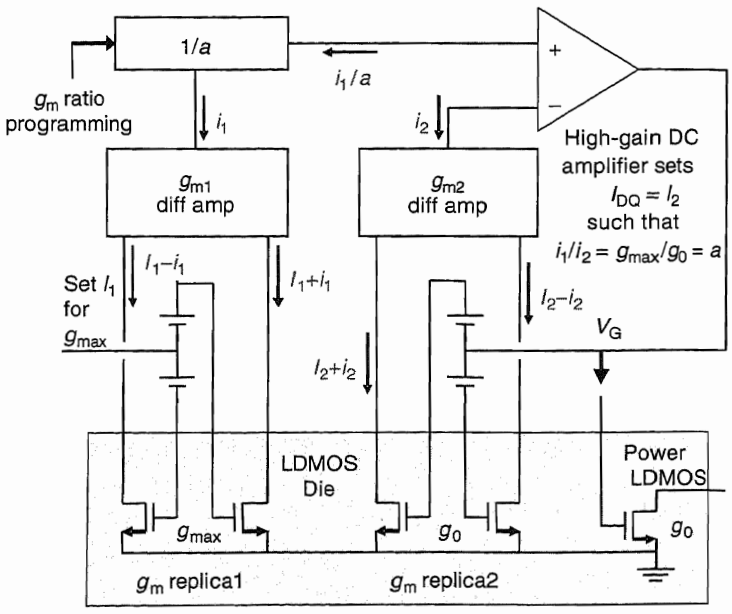


FIGURE 13.26 Circuit concept for g_m-ratio biasing.

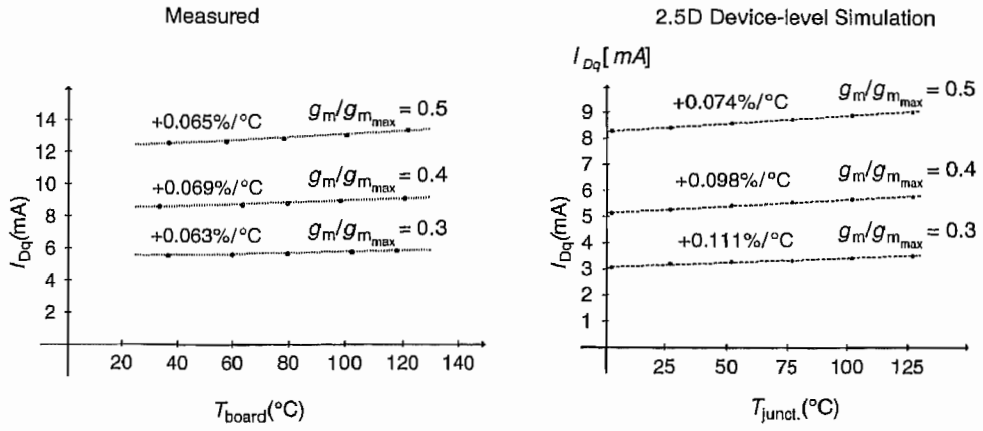


FIGURE 13.27 Simulated and measured drain current curves versus temperature under constant g_m-ratio conditions, demonstrating approximately constant I_{DQ} behavior. (From Banu, M., Prodanov, V., and Smith, K., *Asia Pacific Microwave Conference*, 2004. With permission. © IEEE 2004.)

mirrors, the difference between two slightly dissimilar currents is copied, which is a measure of the transistor transconductance g_m. The master g_m is set and tracks the peak transistor g_m value as shown in Figure 13.14. This is not difficult to accomplish even in open-loop fashion due to zero sensitivity of g_m as a function of the drain current at that point. The slave g_m is automatically set through high-gain negative feedback such that under all temperature and fabrication variations, the ratio between the peak g_m and the slave g_m is kept constant. The resulting gate voltage on the slave g_m transistors is used as the quiescent gate voltage of the PA main RF transistor. Naturally, the transistors realizing the two g_m values are assumed to be matched to the main PA transistor.

Constant-g_m-ratio biasing is justified mathematically by the fact that the maximum error in the transistor even g_m component compared to an ideally flat characteristic is determined by the g_m ratio to a high-order approximation [50]. In other words, the ripple magnitudes in the curves of Figure 13.14 are practically determined only by the g_m ratio at the operating point. Then, it is reasonable to expect that the constant-g_m-ratio strategy should maintain a consistent linearity performance over temperature and process variations.

Figure 13.27 shows simulated and measured I_{DQ} curves of an lateral double-diffused MOS (LDMOS) transistor under constant-g_m-ratio conditions. The resulting practically constant I_{DQ} curves agree with and for the first time explain the traditional PA biasing strategy. Figure 13.28 shows that a constant g_m ratio is substantially better than constant I_{DQ} biasing under fabrication process variations. In addition, this method is fully compatible with IC implementation requirements and the differential nature of the circuits makes them insensitive to RF coupling effects, as discussed for single-ended current mirrors.

A HISTORICAL PERSPECTIVE AND CONCLUSIONS

The PA has been an essential component since the dawn of electronics, and its history has been closely entangled with that of wireless information transmission technology, from the traditional analog radio to the sophisticated digital systems of today. Lee De Forest invented the triode tube in 1906 [52], the first electrical power-amplifying device, whose gain was boosted by Edwin H. Armstrong of Columbia University in 1915 through positive-feedback circuit techniques [53]. These advancements enabled the start of AM broadcasting in 1920. In 1926, Bernhard D. H. Tellegen of Philips Research Labs invented the pentode tube [54], the first voltage-controlled-current-source device, which opened the door for the development of amplifier circuit techniques known today as

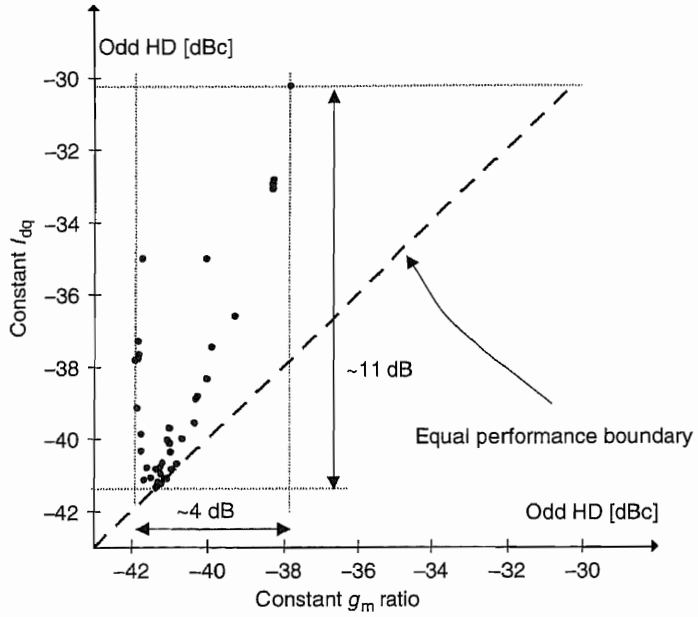


FIGURE 13.28 Simulated scatter plot showing the advantage of constant g_m-ratio biasing compared to conventional constant-I_{DQ} biasing for class AB PAs. (From Banu, M., Prodanov, V., and Smith, K., *Asia Pacific Microwave Conference*, 2004. With permission. © IEEE 2004.)

classes A, B, AB, and C. The effort to resolve linearity issues led to the discovery of feed-forward and negative-feedback principles in 1924 and 1927, respectively, both by Harold Black [55,56] of Bell Telephone Laboratories. All these early inventions consolidated the AM broadcasting industry, and even though the FM modulation was invented in 1933 by E. Armstrong and essentially modern FM transmitters were installed as early as 1940, AM remained the dominant method for RF broadcasting until 1978 when finally the FM exceeded AM in number of listeners.

During the golden years of AM radio broadcasting (1920–1960), much emphasis was put on power-efficient amplifiers, and in the mid-1930s, two important techniques were invented. In 1935, Henry Chireix described the out-phasing PA topology [12] and in 1936, William Doherty of Bell Telephone Laboratories invented a load modulation technique [13]. Today, these techniques bear the name of their inventors, the Doherty amplifier being sometimes called the crown jewel of RF power amplification. Both the Chireix and the Doherty architectures were successfully commercialized. Western Electric deployed Doherty-based AM transmitters in 1938, and RCA used the Chireix architecture in 1956 under the name ampliphase. Other notable accomplishments in efficient RF PAs are the concept of EER developed by Leonard Kahn in 1952 [14], the concept of odd-harmonic enhancement (class F) developed by V. J. Taylor in 1958 [7] and the zero-voltage-switching amplifier (class E) developed by Nathan Sokal and Alan Sokal in 1972 [4,5].

Since FM has fundamental advantages over AM in terms of higher quality audio signals and constant-envelope RF signals (0dB PAR) for easy and efficient PA implementation, it was selected as the preferred modulation format for the original cellular systems, AMPS in 1983 and GSM in 1992. Other wireless systems followed suit. The great consumer market opportunity opened by these applications focused most EE talent on designing PAs for constant-envelope modulation formats. The new circuit design technology available and appropriate for low-cost implementations was now based on ICs. There was no need for realizing efficient PAs under back-off conditions, so the respective generation of circuit designers could just ignore and forget most of the wealth of PA knowledge developed earlier. Class E switching PA is a perfect example of an appropriate architecture for constant-envelope

applications. The powerful Doherty, Chireix, and EER techniques, among others, had all but fallen into obscurity, but not for long.

In the last 10 years, the constant push for higher data rates has reintroduced AM modulation with a vengeance, as discussed in the subsection "Reasons for Back-Off Requirements and Efficiency Penalties." Reviewing their limited present options, PA designers have quickly realized that by looking into the past, they can see the future. We are witnessing a true renaissance in the PA field, and as was the case in the sixteenth-century art, we expect the rebirth of classical PA techniques such as class AB, Doherty, Chireix, etc., to surpass the originals in mastery.

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