PROCEEDINGS OF SPIE

SPIEDigitalLibrary.org/conference-proceedings-of-spie

A low-power CMOS readout IC with on-chip column-parallel SAR ADCs for microbolometer applications

Atia Shafique, Ömer Ceylan, Melik Yazici, Mehmet Kaynak, Yasar Gurbuz

Atia Shafique, Ömer Ceylan, Melik Yazici, Mehmet Kaynak, Yasar Gurbuz, "A low-power CMOS readout IC with on-chip column-parallel SAR ADCs for microbolometer applications," Proc. SPIE 10624, Infrared Technology and Applications XLIV, 1062422 (25 May 2018); doi: 10.1117/12.2304994

SPIE.

Event: SPIE Defense + Security, 2018, Orlando, Florida, United States

A low-power CMOS readout IC with on-chip column-parallel SAR ADCs for microbolometer applications

Atia Shafique[a], Ömer Ceylan[a], Melik Yazici[a], Mehmet Kaynak[a], Yasar Gurbuz[a]
[a]Sabanci University Faculty of Engineering and Natural Sciences, Tuzla, Istanbul 34956 Turkey
[b]IHP Microelectronics, 15236 Frankfurt (Oder) Germany

Abstract

A readout IC (ROIC) designed for high temperature coefficient of resistance (TCR) SiGe microbolometers is presented. The ROIC is designed for higher Ge content SiGe microbolometers which have higher detector resistance (~1M Ω) and higher TCR values (~%5.5/K). The ROIC includes column SAR ADCs for on-chip column-parallel analog to digital conversion. SAR ADC architecture is chosen to reduce the overall power consumption. The problem of resistance variation across the bolometers which introduce fixed pattern noise is addressed by setting a tunable reference resistor shared for each column which can be calibrated offline to set the common-mode level. Moreover, column non-uniformity has been reduced through comparator offset compensation in the SAR ADC. The column-wise architecture in this work reduces the number of integrators needed in the architecture and enables 17x17 μm2 pixel sizes. The prototype has been designed and fabricated in 0.25-μm CMOS process.

Keywords: microbolometer, infrared imaging, focal plane array (FPA), Si/SiGe quantum well, readout integrated circuit (ROIC), capacitive transimpedance amplifier (CTIA), column parallel.

1. INTRODUCTION

Infrared ray (IR) imaging systems find use in many commercial and military applications ranging from biomedical imaging, traffic monitoring, automotive applications, night vision and surveillance. Specifically, thermal infrared imaging and uncooled resistive type microbolometer thermal detectors has been the subject of heavy research in recent times. While the choice of the detector material is highly application specific, depending on a myriad of factors such as intended absorption bandwidth, detector noise, detector thermal time constant, pixel size, cooling requirements, and uniformity expectations. Uncooled microbolometers are receiving attention as they can be operated at room temperature and have lower cost, wider spectral response, compared to their cooled photon detector counterparts which add a significant cost in cooling requirements.

The operation of a microbolometer IR imager starts with the absorption of IR energy radiated on it which heats up the bolometer and causes a change in resistance in its thermistor material accordingly. As such, for higher performance imagers, the microbolometers should be kept thermally isolated from their surroundings, exhibit a larger resistance change with respect to temperature as well as efficient absorption of the incident IR radiation with low thermal capacity. The readout electronics of the imager are tasked with converting the resistance change to an electrical signal, such as a voltage or a current depending on the readout architecture. The signal from the detector is then amplified ready to be converted by an analog-to-digital converter for processing the digitized video information.

In this paper, a 4x4 ROIC infrared focal plane array (IRFPA) intended for high TCR Si/SiGe microbolometers with pixel pitch of 17μm and fabricated in 0.25-μm SiGe:C BiCMOS process is presented. In addition, a 10-bit SAR ADC desihn is also presented that incorporates a differential architecture with non-linearity calibration. The design is aimed towards high bolometer detector resistances intended for use in high TCR (≥ 4 %/K) MQW Si/SiGe microbolometers with 17μm pitch which is currently in development. The ROIC prototype is functionally tested with FETs emulating bolometer resistances and resistance changes.

Infrared Technology and Applications XLIV, edited by Bjørn F. Andresen, Gabor F. Fulop, Charles M. Hanson, John Lester Miller, Paul R. Norton, Proc. of SPIE Vol. 10624, 1062422

2. BOLOMETER EMULATION

The MQW Si/SiGe microbolometers have been shown to be superior in terms of TCR to conventional thin film materials used in bolometers such as vanadium oxide and amorphous silicon, with TCR increases thanks to higher Ge content in SiGe layers [1-5]. The on-wafer IV measurements of the triple stack bolometer devices for various Ge content were carried out in a probe station with thermal control with 5 K steps. The TCR is found to be increasing as the bolometer devices' Ge content increases. However, the detector resistance also increases considerably as the increase in Ge content causes more valence band offset [3][5]. While resistance increase results in lower Joule power dissipation for a constant voltage bias and consequently lower self-heating in the bolometers, high resistance is not ideal in terms of detector noise and responsivity. As the overall goal is in ultimately achieving a detector noise limited NETD (noise equivalent temperature difference) for the IR imager system, the bolometers are still currently in development.

In order to ensure and test for the functional correctness of the designed ROIC, n-channel and p-channel FETs are used instead of microbolometers which are biased to keep the same DC detector resistance with measured on wafer resistances (~1M Ω for the %40 Ge content case). These FETs are used to emulate the detector resistance change due to IR absorption and heating in the implemented IRFPA by changing bias during testing to test the sensitivity and dynamic range of the ROIC. The amount of resistance change emulated is taken as proportional to their measured and extracted TCR. This corresponds to approximately 4.5 %/K TCR and a resistance change of 45k Ω for a 1 K temperature change of the bolometer for the %40 Ge content case.

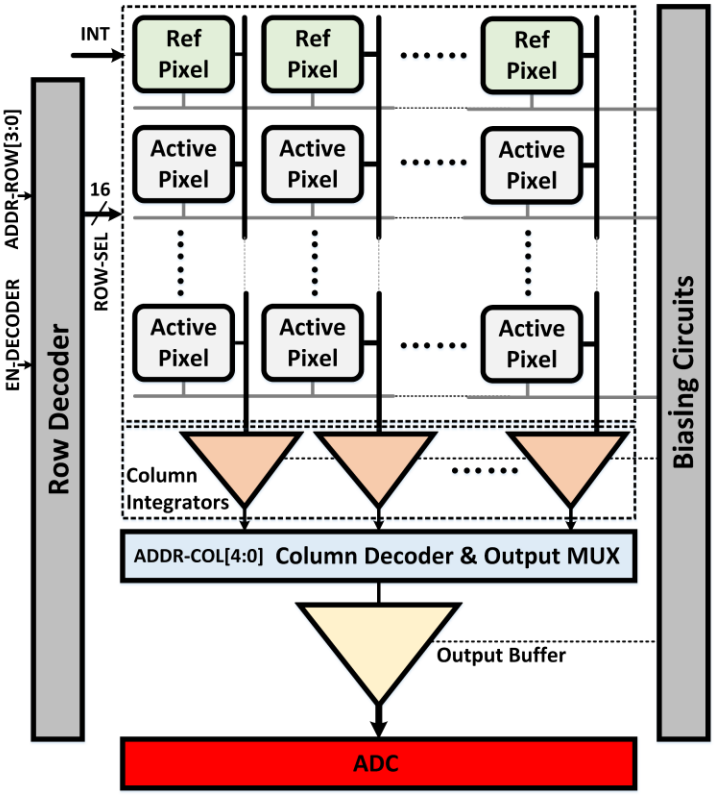

Figure 1. Readout architecture.

3. READOUT ARCHITECTURE

The IRFPA architecture is illustrated in Fig. 1. Every pixel in a column shares an optically isolated reference blind bolometer and an integrator to facilitate column parallel readout. The bolometer bias signals are shared in a row. Blind bolometer is used as a reference bolometer in bridge type readout pixel as shown in Fig. 2. The readout is implemented in a column parallel fashion which is a good compromise between pixel parallel and serial readout in terms of circuit

footprint and thermal imager operation speed. The columns are integrated in parallel and then serially readout in a rolling line manner using the column multiplexer.

The readout circuitry is based on the commonly used capacitive transimpedance amplifier where the detector is biased by constant voltage and the current difference between the active and blind bolometers is summed with an integrator. The CTIA configuration with bridged reference and active bolometers is suitable for highly resistive bolometer detectors because of the high output resistance of the direct injection biasing circuit. If we neglect the effect of bulk-to-source transconductance in the direct injection transistors, the output resistance of the direct injection biasing circuit is

$$r_{out} = \frac{1 + (g_m + g_d)R_{bolo}}{2g_d} \cong \frac{g_m R_{bolo}}{2g_d}$$

where, g_m and g_d are the input and output transconductance values of the p-channel and n-channel direct injection biasing transistors which are taken to be identical for simplicity and R_{bolo} is the nominal resistance of the identical active and reference detectors. The term $g_m R_{bolo}$ is much larger than unity; the output resistance of the direct injection biasing circuit is much higher than the detector resistance of the transistor. The high output resistance reduces the contribution of op-amp/integrator input noise current to the detector input noise current which makes CTIA favorable. However, the current responsivity of the detectors biased with the direct injection transistors is decreased as a result of negative feedback; a small decrease in the detector resistance upon incident radiation increases the detector current which, in turn, increases the gate overdrive voltage of the direct inject transistor and causing a small signal voltage drop in the actual detector bias voltage. This drop in detector bias tends to lessen the current increase, decreasing responsivity of the detector. It should be noted that maximum responsivity does not necessarily result in minimum NETD which is the hallmark of maximum detector performance.

The readout operation is controlled by INT and RS switches implemented as transmission gates enabling pulsed bias operation as seen in Fig. 2. The active and blind detector biases are set by the Vbias1 and Vbias2 signals using the direct injection transistors, respectively. The small signal current resulting from the resistance change of the active pixel due to IR heating is emulated by changing the Vbolo signal.

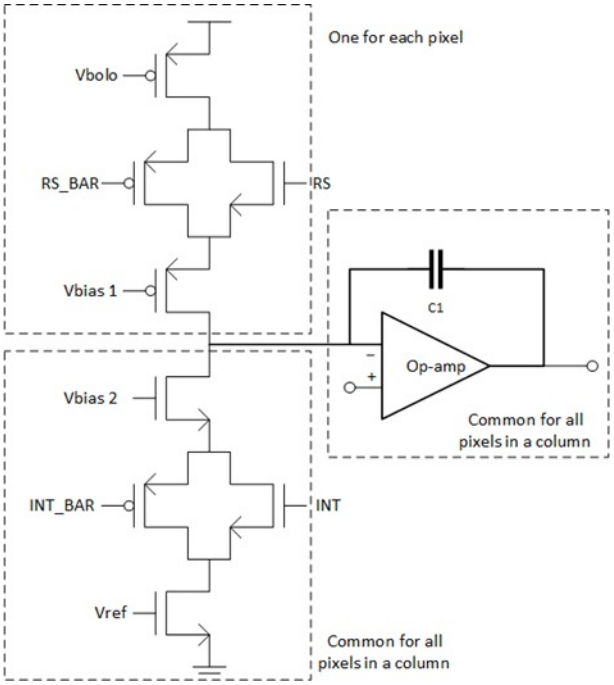

Figure 2. The readout circuit implementation.

3. ADC ARCHITECTURE

This requirement of low power consumption and moderate speed led to the choice of SAR architecture for the ADC. Fig. 3 depicts the ADC circuit. A binary weighted split capacitive DAC is used to save area. Moreover, VCM-based switching has been chosen for energy efficiency. A linearity calibration technique has been used improve the dynamic performabce of the ADC. A digital linearty controller along with two variable capacitors provide the necessary mechanism to correct the nonlinearity error caused by the series split capacitor C_B.

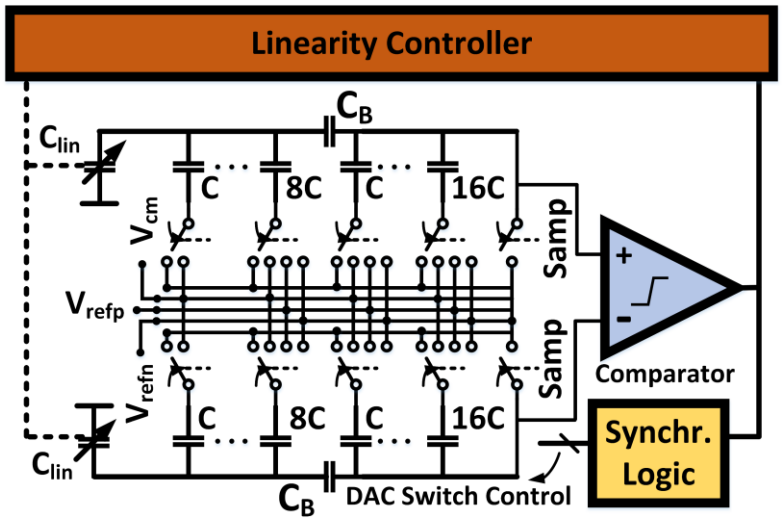

Figure 3. SAR ADC Architecture.

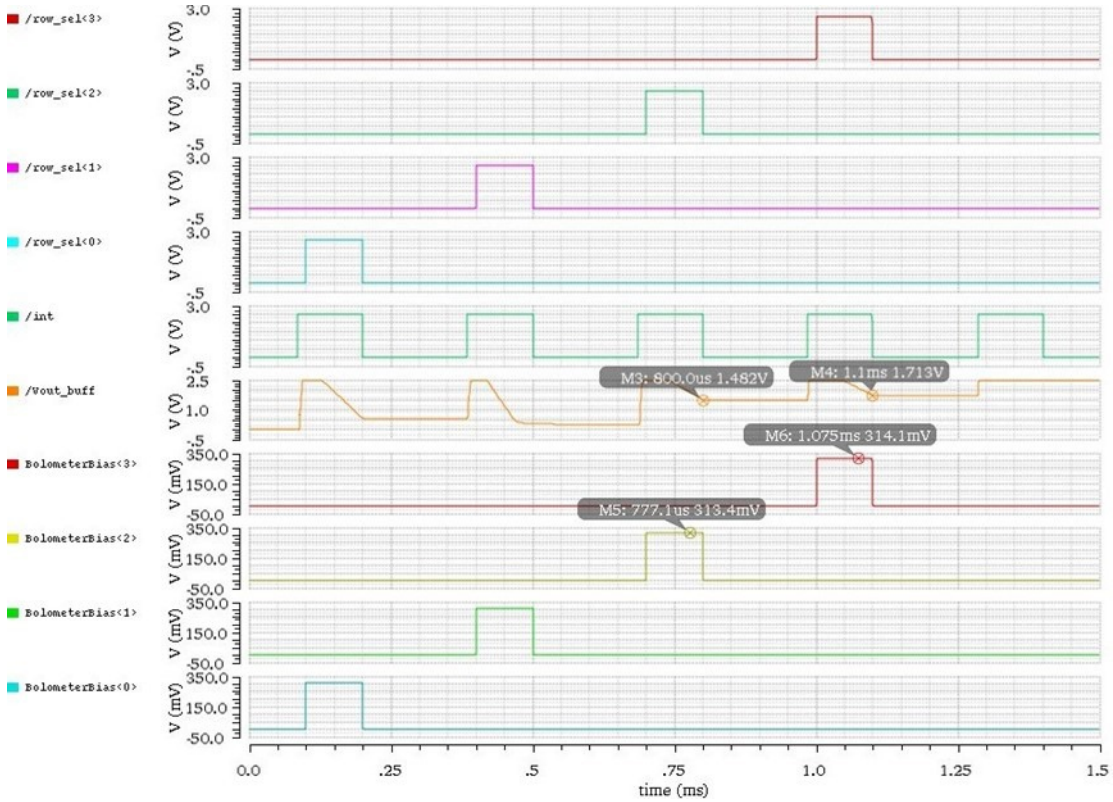

Figure 4. Simulation result of 4x4 prototype ROIC with row selecting and different Vbolo values.

4. SIMULATION AND MEASUREMENT RESULTS

In this section, simulation and measurement results of the 4x4 IRFPA porotype is presented. Simulation results for a fixed integration time of 100µs and different bolometer biases across the rows are shown in Fig. 4. The first four signals are row select signals and the fifth signal is the INT (shown in green) signal controlling the pulsed bias operation of the bolometers. The INT pulse biasing signal is set high before the row selection signal to reset the integration node back to Vdd. The integration results for four different bolometer biases are shown in the analog output signal, Vout_buff. The different bolometer biases are 310.6 mV, 306.7 mV, 313.4mV, and 314.1mV corresponding to pixels 0, 1, 2 and 3. A larger resistance decrease change corresponds to a lower bolometer bias and Vout_buff provided that the integration times are the same. The integration can go from 2.5V to 0V corresponding to a dynamic range of 2.5 V- 0 V.

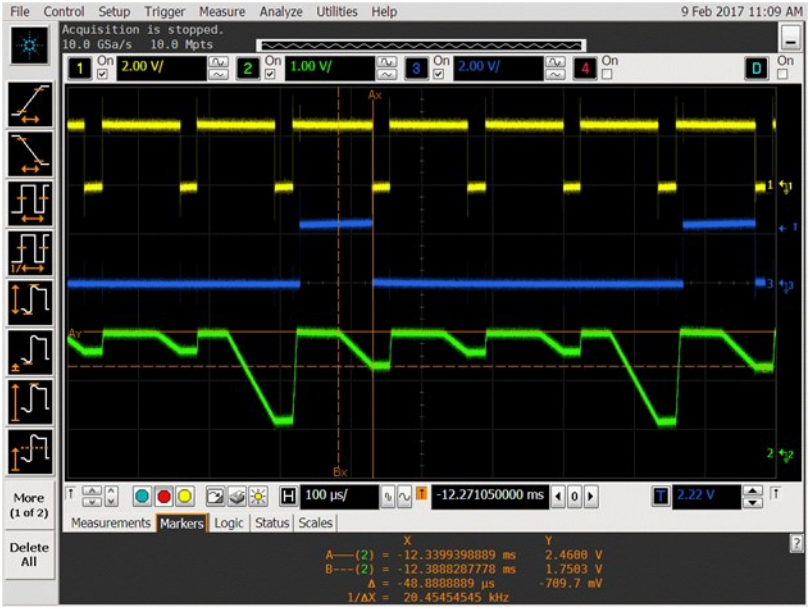

Figure 5. Measurement result of 4x4 prototype ROIC with row select and different Vbolo values.

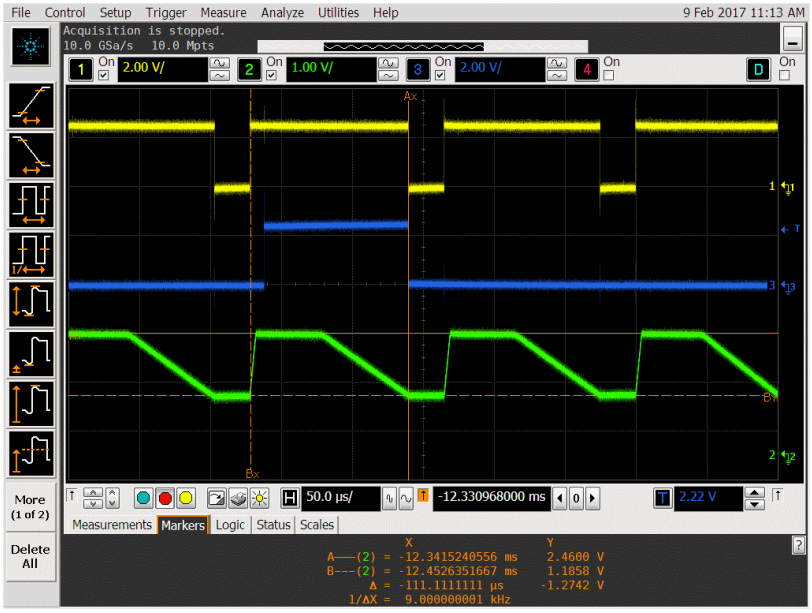

Figure 6. Measurement result of 4x4 prototype ROIC with same Vbolo biases across rows.

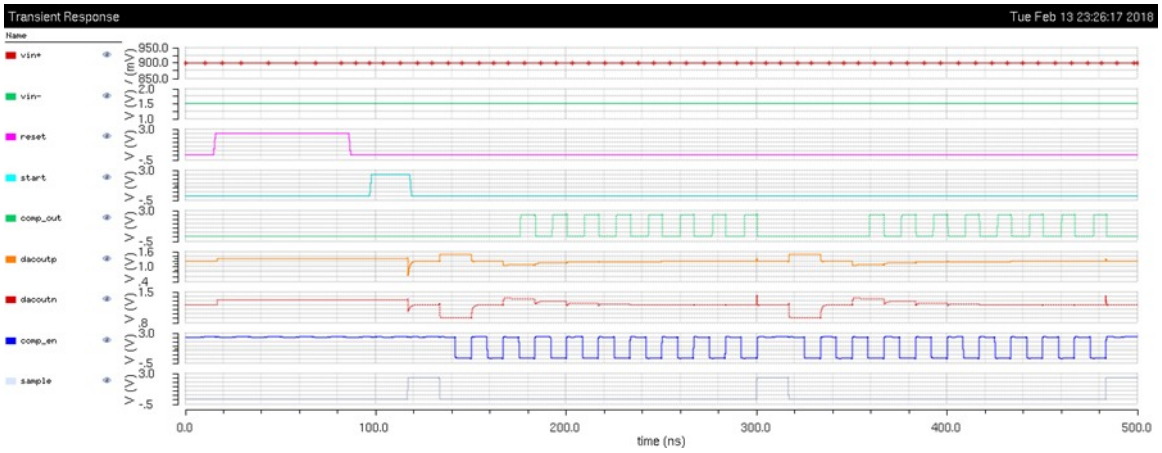

Figure 7. SAR ADC transient simulation plot.

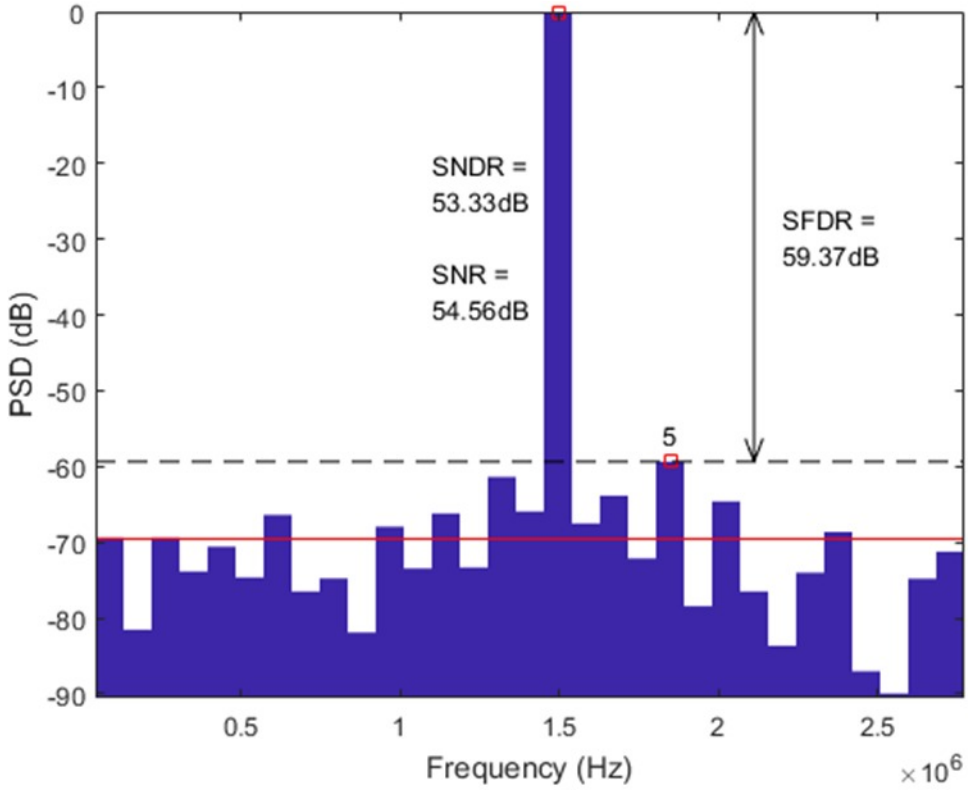

Figure 8. SAR ADC SNDR plot.

The measurement results for different Vbolo biases across rows for 111 µs integration time are shown in Fig. 5. The analog output signal corresponds to four different levels at the end of same integration periods for four different Vbolo biases, as expected. Measurement results for the same Vbolo biases applied across different rows for 111 µs integration time can be seen in Fig. 6. As expected, for the same bias, the integration ends at the same voltage level for a fixed integration time.

Furthermore, simulation results of the ADC are shown in Fig. 7 and Fig. 8. While Fig. 7 depicts the conversion sequence, the improved signal-o-noise-and-distortion ratio (SNDR) has been plotted in Fig. 8. Without the linearity calibraton indicated in Fig. 3, the SNDR drops to 39 dB.

5. CONCLUSION

A 4x4 ROIC prototype intended for highly resistive triple stack, %40 Ge content Si/SiGe MQW bolometers was designed and presented in this work. ROIC was functionally tested with bolometer structures emulated by FETs biased accordingly. Moreover, the design of the column SAR ADC is also presented alon with simulation results. Future work will target the development and optimization of reduced noise Si/SiGe MQW bolometers of various Ge content and suspension leg parameters and hybrid integration of ROIC to larger array formats of 80x60 and 320x240 for determining the NETD of the overall system.

ACKNOWLEDGEMENTS

The authors would like to thank TUBITAK, The Scientific and Technological Research Council of Turkey, for funding his project. The work was carried out under grant 115E098.

REFERENCES

[1] H. H. Radamson, M. Kolahdouz, S. Shayestehaminzadeh, A. Afshar Farniya, and S. Wissmar, “Carbon-doped single-crystalline SiGe/Si thermistor with high temperature coefficient of resistance and low noise level,” Appl. Phys. Lett., 97, no. 22, pp. 223507-1–223507-2, Nov. 2010.

[2] A. Roer, A. Lapadatu, E. Wolla, G. Kittilsland, “High-performance LWIR microbolometer with Si/SiGe quantum well thermistor and wafer level packaging,” Proc. SPIE 8704, Infrared Technology and Applications XXXIX, 87041B (June 11, 2013); doi:10.1117/12.2014914.

[3] A. Shafique, E. C. Durmaz, B. Cetindogan, M. Yazici, M. Kaynak, C. B. Kaynak, Y. Gurbuz,”Design of monocrystalline Si/SiGe multi-quantum well microbolometer detector for infrared imaging systems,” Proc. SPIE 9819, Infrared Technology and Applications XLII, 98191T (May 20, 2016); doi:10.1117/12.2224778.

[4] Jiang B., Gu D., Zhang Y., Su Y., He Y., and Dong T., “Modeling, Design, and Fabrication of Self-Doping Si1−xGex/Si Multiquantum Well Material for Infrared Sensing,” Journal of Sensors, vol. 2016, Article ID 6584650, 7 pages, 2016. doi:10.1155/2016/6584650

[5] S. G. E. Wissmar, H. H. Radamsson, Y. Yamamoto, B. Tillack, C. Vieider, and J. Y. Andersson, "SiGe quantum well thermistor materials," Thin Solid Films, 517, 337 (2008).