Pulse Frequency Modulated DROICs with Reduced Quantization Noise Employing Extended Counting Method

by

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ABSTRACT

Reducing the system size and weight is a very competitive advantage in today's IR market. A continuously growing effort has been shown to achieve digital output ROICs over the last decade with a primary concern to reduce the overall imaging system size and power by eliminating off chip ADCs and precise analog buffers as well as reducing the size of periphery boards.

There is an unnamed industry standard of 20mK NETD for military IR imaging applications. A lower value is always desired to improve image quality or for track and search systems higher correct decision probabilities. Photon noise is the primary noise source and follow shot noise behavior and ideal SNR is limited with the square root of the stored charges. The limiting issue for higher SNR is due the limited charge handling capacity in a small pixel area.

Recent works have shown DROICs with very high charge handling capacities on the order of giga electrons and SNR values as high as 90dB. The drawbacks of these works are the high quantization noise which makes their use limited to high flux scenes or low frame rate applications and high power dissipation which limits the use to small or moderate size array dimensions.

In order to overcome these issues, this thesis has proposed circuit architectures with quantization noise levels lower than 200 electrons with 22 bit representation for a charge handling capacity of 2.34Ge$^-$. The architecture relies on PFM pixel followed by a novel per pixel residue measurement method. A 32x32 prototype array has been fabricated and tested for verification of the proposed architecture. Design considerations have been followed for 256x256 array with a high frame rate of 400Hz and power dissipation of 22.21mW and a peak SNR of 71dB. Additionally low power operation of the proposed DROIC architecture with respect to ordinary PFM DROICs has been analyzed.

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ÖZET

Günümüz kızılötesi görüntüleme pazarında sistem ağırlık ve ölçütlerinin küçültülmesi rekabet üstünlüğü sağlayan önemli bir avantajdır. Son on yılda, çevre kartlardaki ADC ve tampon devrelerinin kaldırılmasıyla güç tüketiminin ve sistem ölçülerinin azaltılması amacıyla, sayısal okuma devrelerinin geliştirilmesinde sürekli artan bir çaba gösterilmektedir.

Askeri uygulamalarda, kızılötesi görüntüleme sistemleri için 20mK NETD değeri bir standart oluşturmaktadır. Daha yüksek görüntü kalitesi, ve arama takip sistemleri için daha yüksek doğru tespit olasılığı için daha düşük NETD değerleri her zaman arzu edilmektedir. Bununla birlikte bir kaynaktan çıkan fotonlar saçma gürültüsü davranışı sergilerler. Saçma gürültüsü nedeniyle ideal SNR, biriktirilen yükün kare köküyle doğru orantılı olarak artar. Burada sınırlayıcı unsur, okuma devrelerinin sınırlı yük depolama kapasitesidir.

Yakın zamanda yapılan çalışmalarda giga electron seviyesinde yük depolama kapasiteesi olan sayısal okuma devreleri ile 90dB SNR seviyeleri gösterilmiştir. Bu çalışmaların eksik yönü ise yüksek niceleme gürültüsüdür. Bu nedenle, bu okuma devrelerinin kullanım alanları, düşük resim hızlı uygulamalar ya da yüksek akı manzaralar ile sınırlı kalmaktadır. Bununla birlikte bu okuma devrelerinin yüksek güç tüketimi de kullanım alanlarını küçük ya da orta ölçekli diziler ile sınırlamaktadır.

Bahsedilen eksiklikleri gidermek için, bu tez ile 200 elektronun altına niceleme gürültüsü ile 2.34Ge^- yük depolama kapasitesi elde edebilen devre mimarileri önerilmiştir. Önerilen mimari PFM piksel yapısı üzerine, her piksel bazında kalan yük miktarını ölçmek üzerine kuruludur. 32x32 dizi formatında bir prototip dizisi üretilmiş ve test edilmiştir. Tasarım 256x256 diziler için yapılmıştır ve bu boyutta 400Hz gibi yüksek bir resim hızını 22.21mW güç tüketimi ve 72dB SNR ile desteklemektedir. Bununla birlikte önerilen mimarinin standart PFM yapılarına gore düşük güç tüketiminde çalıştırılması ile ilgili analizler yapılmıştır.

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LIST of ABBREVIATIONS

BDI ……..Buffered Direct Injection

CCD ……..…….Charge Coupled Device

CDS ……Correlated Double Sampling

CGA ……...Color Graphics Adapter

CTIA ……...Capacitive Transimpedance Amplifier

DI ……Direct Injection

DPS ……..... Digital Pixel Sensor

DROIC ……..….Digital ReadOut Integrated Circuit

FLIR ……Forward Looking Infra Red

IR……... InfraRed

IRST ……..InfraRed Search and Track

ITR ……..Integrate Then Read

IWR ……...Integrate While Write

HFI ……...Hostile Fire Indication

LWIR ……Long Wave InfraRed

MAW ……Missile Approach warning

MSO ……..Mixed Signal Oscilloscope

MTF ……Modulation Transfer Function

MWIR ……..Mid Wave InfraRed

NEC ……Noise Equivalent Charge

NETD ……Noise Equivalent Temperature Difference

NIR ……Near InfraRed

ROIC ……ReadOut Integrated Circuit

SCA ……Sensor Chip Assembly

SL ……Super Lattice

SNR ……Signal to Noise Ratio

SXVGA ……..Super Extended Video Graphics Array

SWaP ……..…..Size Weight and Power reduction trend

SWIR …….Short Wave InfraRed

TDI …….Time Delay Integration

TRL ……Technology Readiness Level

QDIP …… Quantum Dot Infrared Photodetector

QWIP ……...Quantum Well Infrared Photodetector

UAV ……Unmanned Air Vehicle

1. INTRODUCTION

1.1 A History of Sensing the Invisible

We define what is visible with respect to what can be observed through our eyes which are sensitive to light between 390nm-700nm wavelengths only. Technology has not yet shifted the spectrum of seeing, but for about a century, has made quite a progress on devices that make very good use of the electromagnetic spectrum to make the invisible observable.

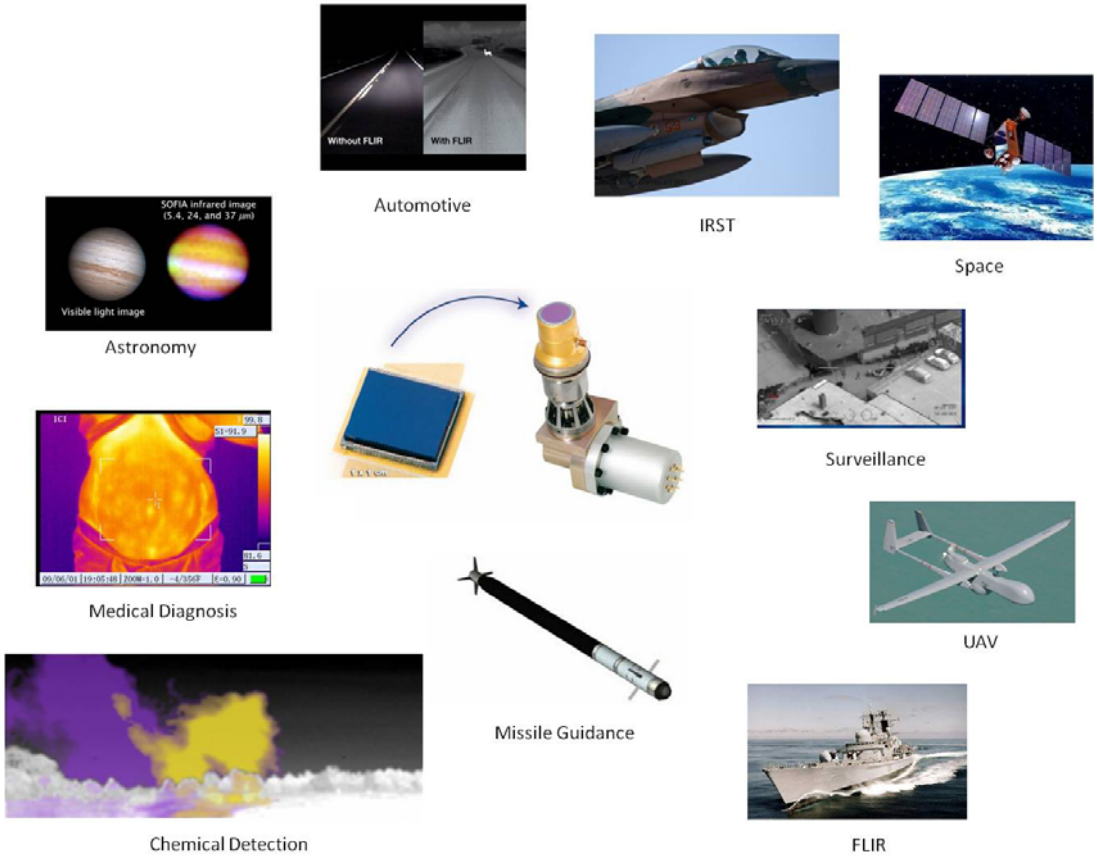

Figure 1 IR imaging applications

Various applications; both military and civilian, benefit from infrared imaging today though most of the technological developments were due to military demands. A passive IR system is impossible to be detected by the enemy, and since it sees the heat difference, it is hard to be camouflaged from, aside from the superior imaging performance through haze and fog, with respect to visible cameras. Unmanned air vehicles, (UAVs), navy navigation and forward looking IR (FLIR) systems, missile guidance systems and IR search and track systems (IRST)

of airborne platforms such as F16 and F34 all benefit from IR imaging. Today, IR cameras are even on satellites for military surveillance. Civilian applications include medical diagnosis (such as detection of breast cancer), chemical detection of gases and agricultural monitoring by airborne systems through hyperspectral imaging, astronomical cameras and automotive industry FLIR systems for night vision. The list is being populated everyday with the continuous cost reduction of IR imaging systems.

All these fascinating devices have a past of about 60 years of rapid innovation, while mankind's awareness of the infrared is about two centuries old. It has been more than 200 years since Herschel put his thermometer to conduct his famous experiment and measure the temperature difference between the different colors of the dispersed light passing from a prism. Having noticed the highest temperature reading at the dark area just after the red color, Herschel had discovered the "invisible light", which shall wait for about 80 more years to be called as infrared [1]

Until the 20th century; there has not been a tremendous effort to develop infrared sensors. Most of the research was done on thermal detection. In 1821 Seeback has discovered the thermoelectric effect. His work was followed by thermocouples made by Nobili in 1829 and finally by Melloni in 1833, a thermopile that can detect the heat of a person from 30ft had been implemented [2]. The first bolometer appeared in 1880 by Langley by use of a Wheatstone bridge [3].

By the late 19th century photoconductive effect was discovered by Smith and the photon effect had been started to be investigated on the selenium as the material. In 1917 Case discovered photoconductivity in thallium sulphur. As in many technological achievements of mankind, efforts for warfare have significantly accelerated the researches on infrared detectors. Kutzcher discovered the photoconductivity of lead sulphide. Lead sulphide was the first practical infrared detector deployed in a variety of applications during the World War II with its results unknown till the end of war. By the end of the war, researches held at Germany constituted the basis for future directions of detector development in USSR, Britain and USA.

Many of the early sensors were developed by the low cost PbS and PbSe materials, especially operating between 3-5μm range. In 1960 discovery of extrinsic Ge:Hg has led to development of IR systems operating in the LWIR region with scanning arrays. In 1959 a breakthrough was about to happen. Lawson and co-workers has developed HgCdTe alloys, with variable bandgaps, that can be tailored to operate at different wavelengths up to 12μm. However due

to difficulties of manufacturing such as high vapor pressure of Hg lead to focus on development of PbSnTe with easier grow and good quality[4]. By the 1970s the situation was again in favor of HgCdTe due its better thermal expansion coefficient with silicon, which enables better hybridization with readout integrated circuits [2].

The variable bandgap and both photoconductive and photovoltaic operations of the HgCdTe material has enabled a breakthrough to achieve modern FPA's. For about forty years research towards military IR applications has been held with the HgCdTe material. The first generation scanning systems, the second generation 2D staring systems and the third generation dual-color dual-band systems incorporated HgCdTe technology. Today, still the high performance of HgCdTe material dominates the market for military applications. The only promising rival against HgCdTe is the type-II superlattices.

Table 1 Comparison of LWIR existing state of the art devices and technology readiness levels [2]

	Bolometer	HgCdTe	Type-II SLs	QWIP	QDIP
	TRL 9	TRL 9	TRL 2-3	TRL 8	TRL 1-2
Status	Material choice for application requiring medium to low performance	Material choice for application requiring medium high performance	Research and development	Commercial	Research and development
Military system examples	Weapon sight, night vision goggles, missile seekers, small UAVs, unattended ground sensors	Missile intercept, tactical ground and air born imaging, hyper spectral, missile seeker, missile tracking, space based sensing	Being developed in university and evaluated in industry research environment	Being evaluated for some military applications	Very early stages of development at universities
Limitations	Low sensitivity and long time constants	Performance susceptible to manufacturing variations. Difficult to extend to >14μ cutoff	Requires a significant >$100M, investment and fundamental material breakthrough to mature	Narrow bandwidth and low sensitivity	Narrow bandwidth and low sensitivity
Advantages	Low cost and requires no active cooling, leverages standard Si manufacturing equipment	Near theoretical performance, will remain material of choice for minimum of the next 10-15 years	Theoretically better than HgCdTe at >14μ cutoff, leverages III-V fabrication techniques	Low cost applications. Leverages commercial manufacturing processes. Very uniform material	Not sufficient to characterize material advantages

Type II-superlattices have shown to have high quantum efficiency and attractive manufacturability as well as HgCdTe like tunable bandgap and band edge properties [5-7]. In recent years, multicolor and large format 640x512 InAs GaSb arrays have already been demonstrated [5] and type-II superlattices are benefitting from an ever increasing attention. Still, today the state of the art IR systems use HgCdTe detectors as the primary sensors despite the challenging type II superlattices, due being at a higher level of technological readiness.

The HgCdTe era through good hybridization to silicon has enabled a boost on ROIC design. The first generation of readouts was of scanning types consisting of a single column of detector elements. In order to decrease the sensitivity to non-uniformity of the pixels and to increase the effective integration time, hence the SNR of the FPA, TDI cameras were soon introduced to the market with multiple columns. Today, IR market has formats for scanning type of FPAs as 288x4 of SOFRADIR and 576x7 of AIM. A scanning system can also have a large spatial resolution with a single column of pixels since the scanner can span a wide coverage area, with a frame rate trade-off. A scanning system is shown in Figure 2 with its position in the dewar as well. Typically a mechanical scanner, scans the scene that is focused by the optics over the array and each readout event generates a raw data of a column image. All columns are combined to generate a 2D image by the off dewar uncooled periphery electronics.

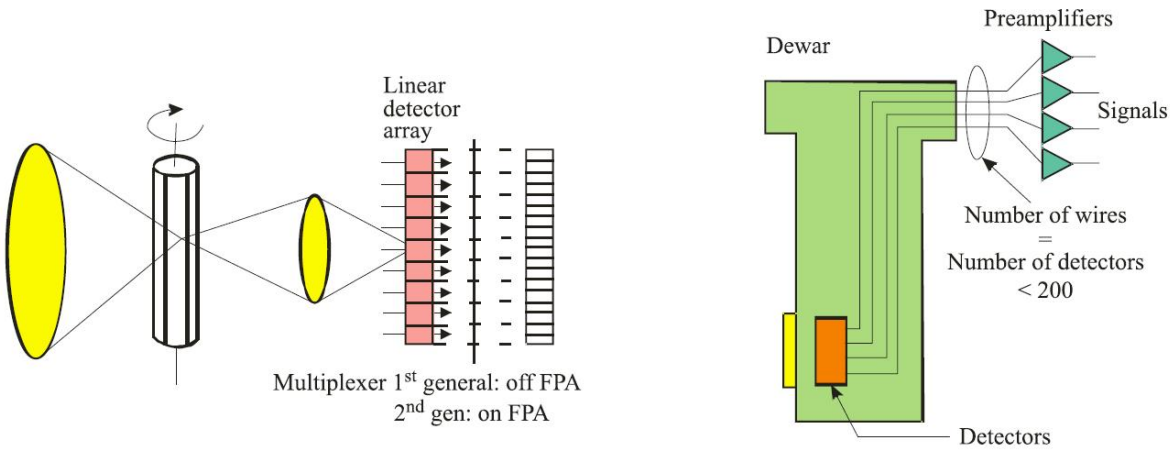

Figure 2 Scanning type IR imaging system [2]

The second generation FPAs of Figure 3 is in 2D structure and called staring arrays. Various formats have been introduced to the market with different video formats. Early arrays, due to the uniformity and manufacturability issues, were of smaller sizes, CGA format of 320x240

such as Goodrich's [8], followed by the 640x512 PAL [9] and 640x480 NTSC formats (bolometer) [10]. Even larger arrays of sizes 1024x1024 for space applications as of Raytheon's [11] or 1280x1024 SXVGA [12], [13] have been on the market for many years. Finally, larger arrays that are used in the astronomy applications have been produced in 4096x4096 formats, as of Teledyne's [14] in mosaic form using 1024x1024 pixel arrays.

The third generation FPAs consists of larger arrays with higher frame rates, more on-chip functionalities, digital outputs and more importantly dual-band or dual-color operations [15]. Some of these expectations have been met as commercial products and some of them are still being under research and development stage. Dual band and dual color detectors have been shown with good NETD results [16-18] as well as digital output FPAs [19, 20] and high frame rate FPAs for hostile fire indication systems (HFI) [21, 22].

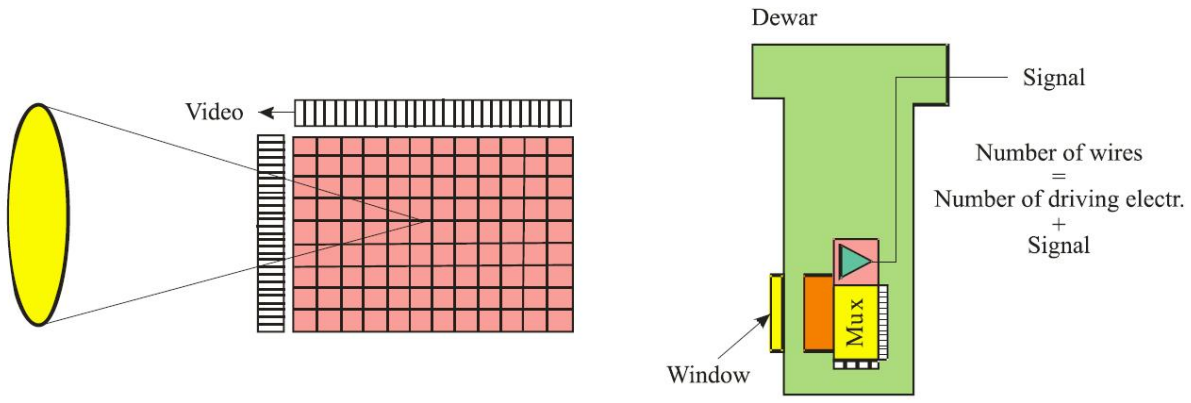

Figure 3 Staring type IR imaging system [2]

Today the trend for the FPAs is to reduce the pixel sizes while increasing the array sizes, reducing the weight, and power of the dewar and FPA as a whole and the total cost. Industry has named these objectives as SWaP in reference to size, weight and power [9, 23-28]. These objectives are met as a whole at system level; power of FPA should be reduced and operation temperature should be increased for low weight, low power cooler assembly, digital output FPAs are required for smaller periphery cards without analog buffers and ADCs.

1.2 Readout Integrated Circuits ROIC

"Detectors are only a part of usable sensor systems which include optics, coolers, pointing and tracking systems, electronics, communication, processing together with information extraction sub−systems and displays. So, the process of developing sensor system is significantly more challenging than fabricating a detector array" [2]. One of the mentioned

challenges is the design of ROICs and packaging it with the sensor array to build the sensor chip assembly (SCA).

The SCA can be monolithic or hybrid. The monolithic approach is mainly inherited from the visible CCD arrays and today, ROICs are sometimes still referred as multiplexers due to the CCD heritage [29]. In the IR spectrum, a hybrid approach is usually followed since the invention of flip chip bonding in late 1970s. The hybrid approach incorporates indium bumps between the sensor array and the ROIC. Hybridization usually takes place by heating and pressure. As shown in Figure 4 hybrid approach has the advantage of near %100 fill factor, and using different substrates for FPA and ROIC can optimize the performance of SCA. Additionally, silicon ROICs offers significant reliability and much more on-chip signal processing.

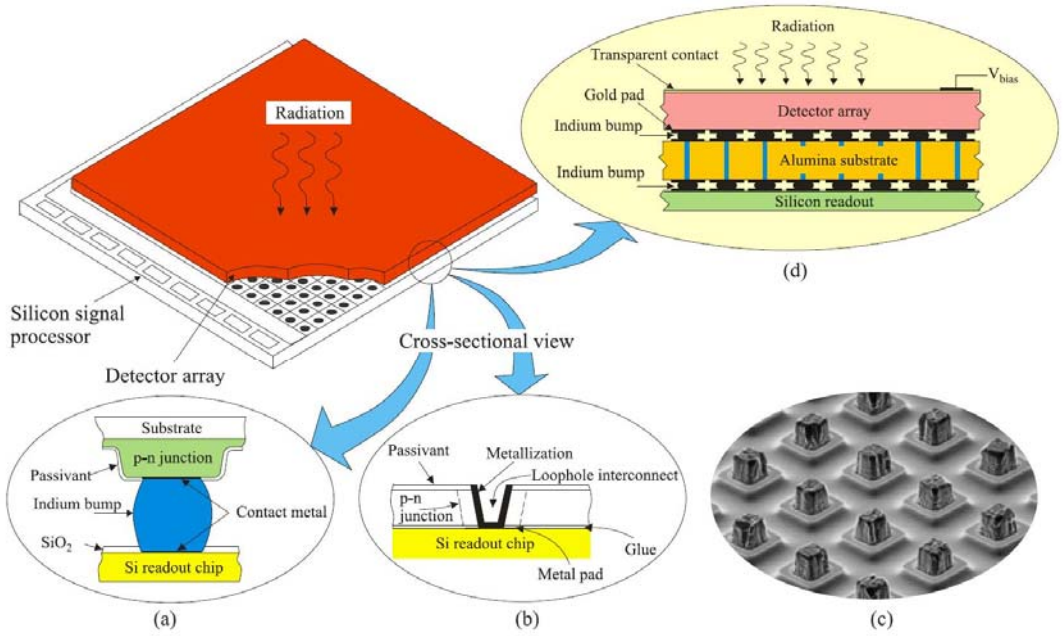

Fig. 29. Hybrid IR FPA interconnect techniques between a detector array and silicon multiplexer: (a) indium bump technique, (b) loophole technique, (c) SEM photo shows mesa photodiode array with indium bumps, and (d) layered-hybrid design suitable for large format far IR and sub-mm arrays.

Figure 4 Flip chip bonding methods [2]

ROICs can be considered as the front-end of all the imaging system electronics, and hence, has a key importance on the system parameters. The quality of the raw image data relies on the ROIC parameters such as charge handling capacity, input referred noise, dynamic range linearity etc. Key ROIC performance parameters and their related system parameters are summarized in Table 2 [29]. These performance parameters are further discussed in the next sections.

Table 2 Relationship between key ROIC requirements and system performance parameters [29]

Major ROIC Parameter	Related System Parameter	Comments
NEC (noise equivalent charge)	Sensitivity	Minimized to enhance SNR
Power dissipation	Cool down time, life, weight	Limited cooler life, cooler weight and size
Dynamic range	Maximum saturation signal	Loss of signal
Crosstalk	System MTF, blooming of saturated elements	Element to element
Frequency response	System MTF, latent images	Often related to crosstalk
Input impedance	Signal linearity, noise	Detector bias change with signal, loss of optimum bias
Linearity reliability	Calibration, instrument life	Proper identification, confidence of success
Gain	Sensitivity	Signal amplified above system noise floor
Output driver impedance	Sensitivity, MTF	EMI from environment crosstalk between multiplexed elements

1.2.1 ROIC Performance Parameters

A ROIC is a custom IC, built for specific detector requirements. There are some off-the-shelf ROICs that can be applied to different size FPAs such as former INDIGO's (now FLIR) ROICs. However at product stage most FPAs include a custom made ROIC. The most important parameter of the FPA as a whole is the SNR. For ROICs this parameter is linked through the input referred noise in electrons or noise equivalent charge (NEC) and the charge handling capacity. Aside, parameters such as power consumption, frame rate, injection efficiency and pixel size impose stringent design considerations and challenging trade-offs.

1.2.1.1 Charge Handling Capacity

Photons emitted from a source follow the Poisson's statistics and inhibit shot noise behavior. In a ROIC, photo-generated charges are stored at an integration capacitance as well as the noise charge. Due to the shot noise, the stored noise charge is the square root of the stored signal charge. Hence SNR is directly proportional to the charge handling capacity of the readout. Usually pixel area is limited with the detector array's pitch and in order to handle the

highest possible charge, high voltage semiconductor processes are chosen. In MWIR and SWIR applications, in order to obtain high SNR long integration times are used due to the lower amount of photon emittance from the objects. However in LWIR band, less than 0.5 ms integration times are used in order not to saturate the integration capacitor, whereas with a longer integration time more and more charges can be stored if permitted by the capacity of the ROIC.

1.2.1.2 Input Referred Noise Electrons

Charge handling capacity defines the maximum SNR that the imaging system can operate at. Input referred noise in electrons, also referred as the noise equivalent charge (NEC) gives the noise floor that is due not to the detection mechanism, rather the readout itself. Various stages affect this performance parameter. KTC noise of the integration capacitor, input preamplifier noise, buffer and multiplexer noises are square summed at the output node and then, by being divided to the transfer function of the ROIC, this value is referred to the input. Typical values differ for different operation wavelengths. An LWIR ROIC can have 1000 electron noise whereas an MWIR ROIC can have 300-500 electrons and an SWIR ROIC can have even lower value of 10 electrons [30]. This is also due to the larger shot noise of the LWIR and MWIR bands; higher readout noises can be tolerated in addition to being unavoidable due to higher kTC noise of larger integration capacitances.

1.2.1.3 Power Dissipation

Power dissipation is an important parameter especially for the cooled systems. It is desired that these systems operate at low power levels not because they are integrated to portable systems, rather to decrease the system cost by increasing the coolers lifetime. As the power consumption increases so does the heat, and the lifetime of the dewars are reduced, larger dewars are required and longer cool down times are required at start-up. All these are contradictory to the reducing the size weight and power of IR imaging systems (SWaP trend) for cooled IR imaging systems.

1.2.1.4 Input Impedance

Input impedance is directly related to the injection efficiency and the biasing conditions of the detector. A stable bias is required during the operation of the detector. Additionally low input

impedance of the pre-amplifier of ROIC ensures high injection efficiency, which is a measure of the generated photo-current to the integrated photo-current. Various input pre-amplifiers have been proposed to optimally combine to different detectors of different wavelengths. For example a direct injection (DI) pre-amplifier is a good choice for LWIR applications with high photocurrents, while a capacitive transimpedance amplifier (CTIA) is a better choice even with its larger area, due to the low photocurrents at MWIR wavelengths results a high impedance node for the DI pre-amplifier.

1.2.1.5 Gain

Almost all ROICs include multiple gain functionality. This is due to the fact that different irradiances require different sensitivities. Aside, a low flux scene should be observed by use of a small capacitor to reduce the kTC noise, whereas a high irradiance scene should be observed by a large capacitance in order to prevent saturation and data loss. Multiple set of capacitors that can be programmed to the desired value by the user is implemented at the integration node for variable gain functionality.

1.2.1.6 Frame Rate

For a staring array, frame rate is the frequency of the raw data transfer out of the ROIC for the whole pixel array. Human eye realizes images over 30Hz as video. Usually readouts are operated at 50Hz for low speed applications. However this parameter is application specific and faster operation speeds such as 200Hz and 400Hz are required for hostile fire indication (HFI) systems and missile approach warning (MAW) systems. This starts to be problematic as the array sizes becomes larger. As in any IC, higher speed comes with the power cost.

1.2.1.7 Uniformity

FPAs are generally corrected for uniformity by a two-point correction method in order to suppress the non-uniformity of the detectors. Still even after the correction, fixed-pattern noise can be the dominant noise source [31]. Careful layout design is required in order to sustain reliability and matching of ROIC's individual pixels.

1.2.2 ROIC Architectures

"Third generation sensors will place special demands on the Read Out Integrated Circuit (ROIC) design. For the cooled detector, the ROIC will need to support the collection of 10^9 electrons per color per 30 Hz frame, provide 14 bits of linearity, a 14 bit signal-to-noise ratio, and a spatial non-uniformity of less than one half of a least significant bit. To simplify the overall system design, the ROIC will also need to support on-FPA A/D conversion, simultaneous dual color operation, high frame rates (up to 480 Hz), possibly some level of on-FPA non-uniformity correction, and an optical dewar data link. Even though commercially driven miniaturization of Si-based IC's continues to make tremendous progress, it is doubtful that a traditional ROIC design will support these requirements in an l8um unit cell."[32]

Some of these prospects such as 14 bit SNR, on chip A/D conversion and dual color operation have been met. It is still a challenging task to obtain 14 bit linearity (for wide dynamic range applications at least) and 480 Hz operation with state of the art SWaP trends. Additionally aside from some DPS arrays (digital-storage, digital-output readouts), no ROIC has come up with giga electron storage capacity.

In the last decade, analog to digital conversion have been added to ROICs. Traditionally, ROICs are analog circuits. Today the main approach to digital ROICs is still an analog chain followed by an on-chip ADC. Another approach has been proposed to make digital pixels and carrying the analog to digital conversion at pixel level. This massive parallelism has immense charge handling capacity compared to the analog counterparts, making it a desirable methodology especially for the LWIR band, where the irradiance is already high.

An analog ROIC signal chain starts with an input pre-amplifier coupled to the photo-detector on one side and the integration capacitor on the other side. The function of the pre-amplifier is to create a stable detector bias and to pass the photocurrent to the integration capacitor with high injection efficiency. The stored charge is then transferred to the sample and hold stage for integrate while read (IWR) functionality, or is held until it is read out as in integrate then read (ITR) functionality. To transfer the voltage to the output, usually a source follower type buffer is included at the pixel level. Time delay integration (TDI) for linear arrays and correlated double sampling (CDS) for staring arrays are common noise reduction techniques applied on-chip.

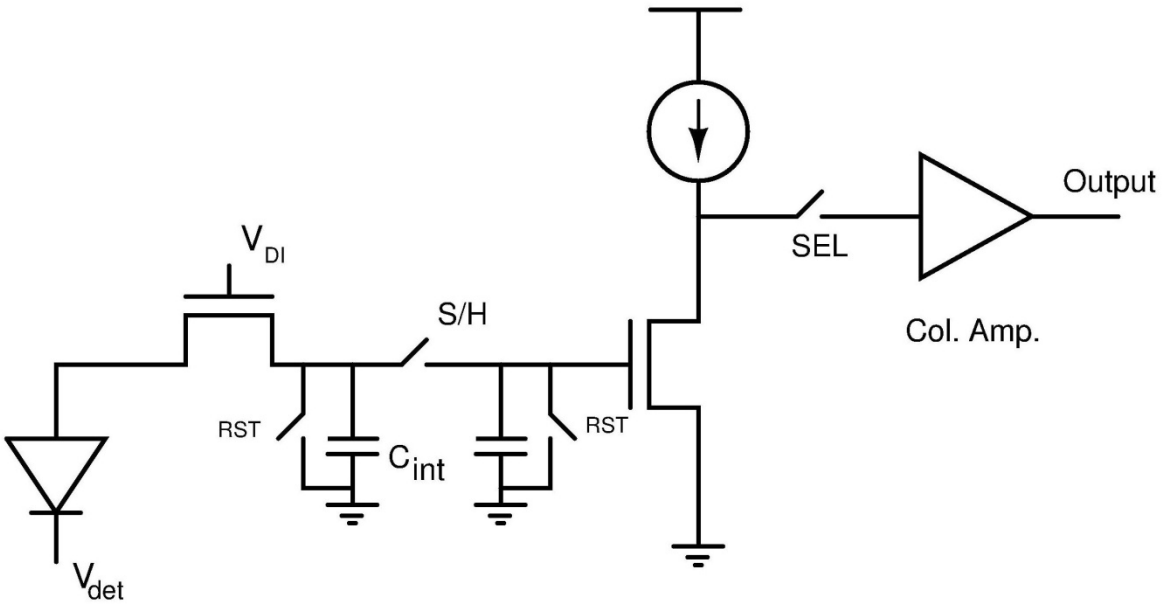

Figure 5 Analog ROIC signal chain

DROICs have been on the market for the last decade. Commercially available ones have same signal chain with the analog counterparts with A/D conversion implemented on-chip. These A/D convertors can be implemented per channel or per a fixed block in order to operate at moderate speeds and not to dissipate much power while whole FPA is read out at video frame rates. These DROICs suffer similar limited charge handling capacity as the analog ROICs since integration capacitor at the limited pixel area is of the same size. However, bringing the on-chip conversion at the ROIC level enables digital outputs, which eases the peripheral card design. More importantly without the need of an ADC; card size, weight and power of the whole IR system can be reduced which is very desirable.

Finally, there are DROIC architectures with digital pixels which can store the charge in the digital domain, instead of analog domain. This task is accomplished by using a small integration capacitor at the pixel area, and leaving the remaining area for digital cells such as counters and memory. A small capacitor can store low amount of charge and as soon as its voltage passes certain storage, it is reset and the number of resets are count as representation of the incoming signal. Effectively, this allows the integration capacitance to increase exponentially with respect to pixel area. These ROICs can achieve 30dB higher SNR than analog counterparts.

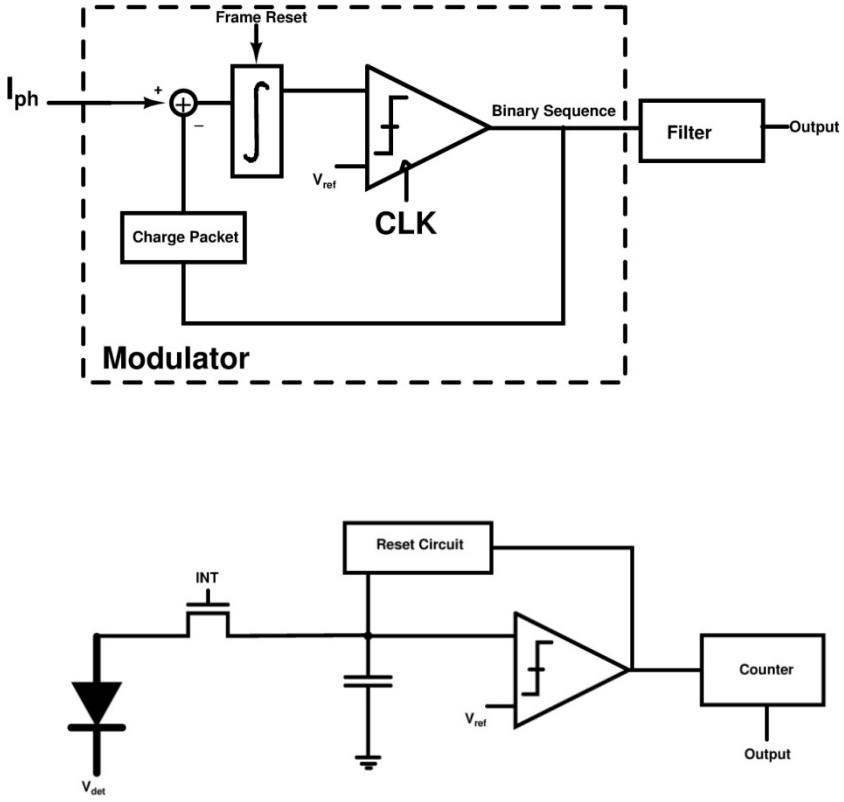

Figure 6 Digital pixels a) ΔΣ ROIC pixel (synchronous) b) PFM ROIC pixel (asynchronous)

Two architectures have been known in the literature for DROICs with digital storage. The first one is based on Delta-Sigma Modulator approach [33-39] as shown in Figure 6.a and the second one is based on a pulse frequency modulation approach of Figure 6.b [40-44]. Two methods differ by the capacitor threshold control mechanisms. In delta-sigma method, the resetting is controlled by the clock; at each clock cycle voltage on the integration capacitor is compared with the reference value. If the value is higher than the threshold level, integration capacitor is reset. In a PFM ROIC threshold crossing is monitored continuously. As the voltage on integration capacitor reaches the threshold value, capacitor is reset immediately. Both architectures count the number of resets as the representation of the input signal.

1.3 Drawbacks of Current ROICs

Analog ROICs are limited with charge handling capacity. Especially in LWIR systems, this limits the integration time to less than 0.5ms and stored charges are less than 50Me$^-$. Due to the shot noise being square root of the collected charge, analog readouts are operating with lower SNR than that can be achieved with video frame rates.

There are two types of digital ROICs (DROICs) that have been demonstrated. The first approach is to use an on-chip ADC to do the conversion and transferring data to the peripheral circuits in digital form. This reduces the noise coupling due to the peripheral cards and buffers thanks to digital operation; however the charge handling capacity remains still the same as analog counterparts due to the same signal chain. Additionally for large arrays such as 1024x1024 pixels, fast ADC architectures are required and as the number of bits is increasing, building an accurate ADC cost a lot of power dissipation.

The second type of DROICs has pure digital pixels, where the conversion takes place right under the pixel area. Since the conversion takes place under the pixel area, and the digital storage capacity increases exponentially with respect to area as opposed to linear increase of an analog pixel, very high charge handling capacities can be achieved. High charge handling capacity results very high SNR at high flux applications. However at low irradiance levels, SNR is reduced significantly due to the quantization noise. In order to decrease the quantization noise, the conversion step size must be reduced which can be achieved by either reducing the capacitance or the threshold voltage. This has physical limitations, as well as additional problems with SNR and power dissipations. Also, it is not practical to reduce the integration capacitance to less than 1.5fF in a 90nm CMOS technology due to the comparator input capacitance. Secondly voltage swing on the integration node should be high for better SNR. Finally, reducing the capacitance increases the switching activity, which increases the power consumption.

In order to overcome these design challenges and reduce quantization noise in a power and area efficient architecture, new techniques must be implemented.

1.4 Thesis Objectives

Up to now, DROICs have aimed to have only A/D conversion on chip to ease proximity cards or achieving high charge handling capacities to increase the dynamic range. Primary objective of this thesis is to create DROIC architectures that have very high charge handling capacity advantage to the analog counterparts, as well as very low quantization noise levels. With this capability, IR systems that can cover a wide dynamic range of applications can be implemented. Lowest quantization noise levels for giga electron charge handling capacity DROICs are aimed in order to achieve very high dynamic range.

This objective is to be implemented in a limited pixel area with low noise, high frame rate operation. Obviously, DROICs should be compatible to the common of-shelf FPAs, while operating with modest power consumption.

Another objective of the proposed techniques is to investigate DROICs with low power dissipation with respect to analog and digital counterparts, while having high charge handling capacity and moderate quantization noise.

1.5 Thesis Overview

This thesis is organized as five chapters. Following a brief history of IR imaging and ROICs, chapter 2 focuses on the ROIC architectures starting with a brief discussion about the necessity for DROICs. For completeness, analog ROIC architectures are discussed first with its noise performance. Next, DROICs with analog signal chain and on-chip ADCs are discussed with circuit topologies, drawbacks and design examples. More focus is given on ΔΣ DROICs and PFM DROICs with their SNR analysis. Finally, the proposed DROIC architecture is introduced with its sub blocks and practical design considerations. Design specifications for prototype implementation are also discussed in this chapter.

Third chapter of this thesis is dedicated to the implementation of the prototype for empirical verification of the proposed architecture. This chapter starts with the architecture of the prototype and the pixel. Next, each sub block is investigated in detail; design specifications, circuit topologies, physical design and simulation results. Following a brief discussion on test blocks that have been implemented, physical design of the prototype is given. Simulation results for different scenarios are represented followed by measurement results. Detailed discussion on measurement set-up and methodology is given in this chapter for every proposed system specification.

Fourth chapter is dedicated for power analysis of the proposed DROIC. It starts with power dissipation analysis of each block with corner simulations. Next with a closer look to the SNR analysis, a low power operation mode of the proposed architecture is introduced. Finally a figure of merit for power efficiency is introduced and using measured power consumption values, the proposed work is compared with the state of the art in the literature.

The last chapter summarizes the need for DROICs and drawbacks of current DROICs. It also gives a final complete comparison of this work with the referenced works. Finally future design perspectives are given, concluding the last chapter.

2. ROIC ARCHITECTURES

This chapter starts with the necessity for digital readouts followed by ROIC architectures with special focus on digital storage DROICs. For completeness of a comparative study, analog readout architectures are discussed as well. Detailed noise analysis of ROICs is evaluated and the advantage of a DROIC with low quantization noise is identified. Finally a new DROIC pixel is proposed employing extended counting method with reduced quantization noise.

2.1 Why Digital Readouts?

As most of the readouts commercially available on the market for infrared detector arrays are analog readouts, this is a very fair question to ask. Fortunately, it has many convincing answers.

Traditional signal processing for image sensors are held on the analog domain. This includes quite simple steps of photon to charge conversion (only monolithic readouts), charge to voltage conversion, amplification and read out. Some noise reduction techniques such as correlated double sampling or time delay integration may take place in between the charge to voltage conversion and amplification steps [45-47]. In any case, a voltage output in the analog domain per pixel for representing an incident photon amount (representing observed scene) is read out and transmitted to the analog to digital conversion block, ADC. Following the A/D conversion, raw image data is ready, which can be processed by any image processing algorithm, can be corrected for non-uniformities or can simply be displayed on a monitor. Well the whole system described here requires an ADC already; so one reason for digital readouts is this requirement. An on-chip ADC reduces the external noise added before the conversion and additionally, reduces the cost. Actually this is the many case for consumer electronic readouts operating in the visible region, the sensors are monolithic p/n diodes, the readout is analog, and finally an ADC per column does the necessary conversion. In the end, there has to be an analog to digital conversion to process and monitor the readout data, hence why not have digital outputs at the first place?

There is more to it than that. All imaging applications are limited by the shot noise. That is the best that can be achieved in any photon measurement system. Shot noise is due to the discreteness of photons being emitted from a source (just as the shells leaving a shotgun,

hence the name shot noise). The mean irradiance is known, yet photons leave the source in discrete quantities in time, that follow Bose-Einstein distribution for blackbody sources and Poisson distribution for laser sources [48]. In both distributions variance is the same. Assume that, over a time interval of τ, "n" photons are incident on a detector which has a quantum efficiency of one. Pixel current will be measured as in (2.1) with a mean current of (2.2)

$$i = \frac{nq}{\tau} \tag{2.1}$$

$$I = \bar{i} = \frac{\bar{n}q}{\tau} \tag{2.2}$$

The noise current, i_N^2 can be calculated through the variance of the detector current and is as in (2.3)

$$\overline{i_N^2} = \overline{(i-\bar{i})^2} = \frac{q^2}{\tau^2}\overline{(n-\bar{n})^2} = \frac{q^2}{\tau^2}\bar{n} \tag{2.3}$$

$$\overline{i_N^2} = \frac{q^2}{\tau^2}\bar{n} = \frac{q^2}{\tau^2}\frac{I\tau}{q} = \frac{qI}{\tau} \tag{2.4}$$

Noise current is integrated over the same time interval of τ, which results the SNR of:

$$SNR = \frac{I\tau/q}{\sqrt{qI\tau/q^2}} = \frac{\bar{n}}{\sqrt{\bar{n}}} = \sqrt{\bar{n}} \tag{2.5}$$

Total noise of $\bar{n}$ photons being measured has $\sqrt{\bar{n}}$ noise photons; hence the SNR is $\sqrt{\bar{n}}$ as well. Clearly, best possible image/video quality is desired at the user end, resulting the requirement of the highest possible SNR. Hence any imaging sensor should collect as many photons as it can (as long as they are available from the source) in order to operate at its best performance.

Figure 7 is a visual example to the relationship between collected number of signal electrons and SNR. In Figure 7.b. photon per pixel is reduced by 1000 times and in Figure 7.c. photon per pixel is reduced by 100,000 times. The quality of the images (of the probe station in our test and measurement design lab) increase as the measured photon numbers is increased.

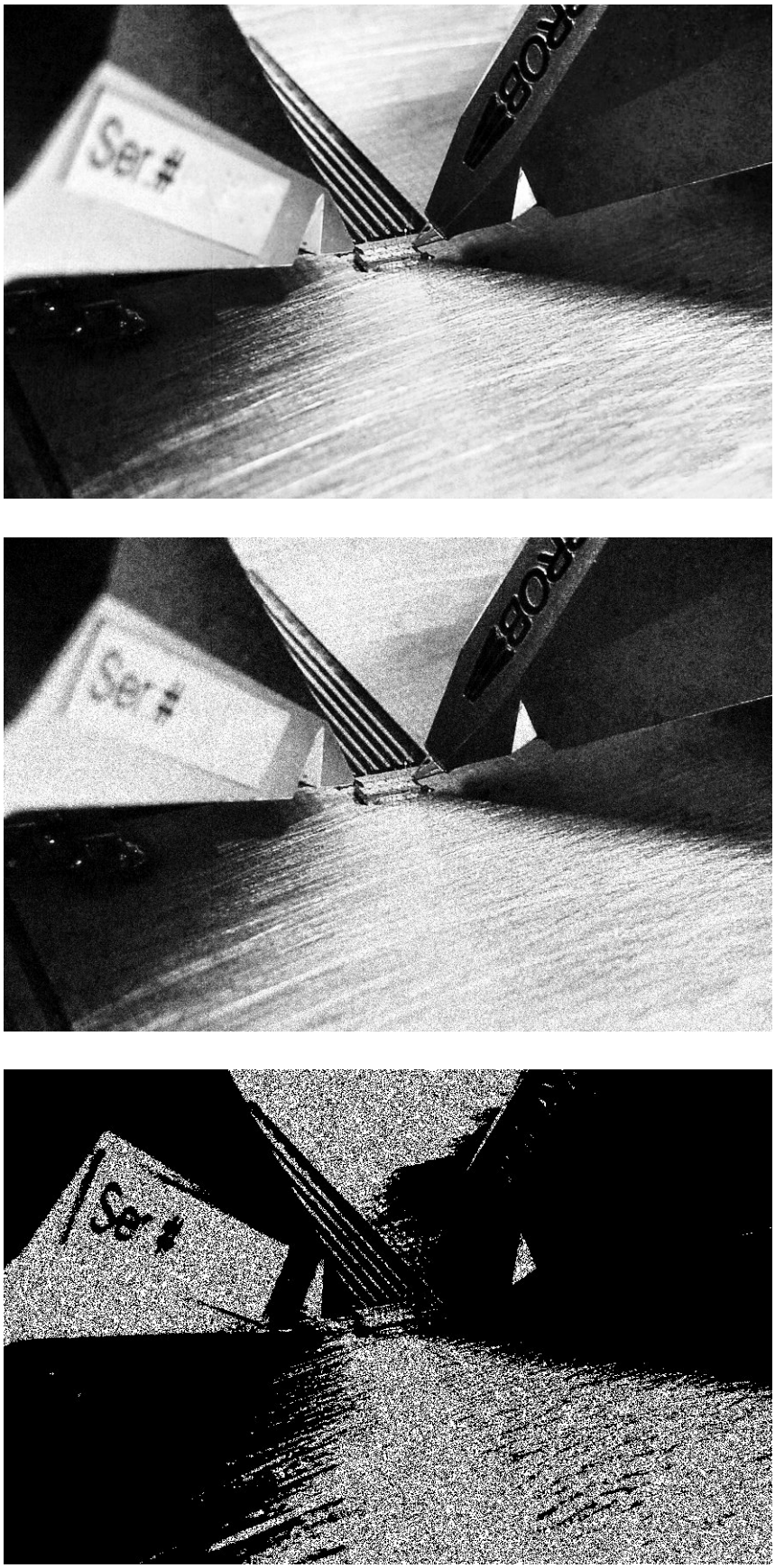

Figure 7 Image quality with respect to collected charges (a) photo with k photons per pixel , (b) photo with k/1000 photon per pixel, (c) photo with k/10,000 photon per pixel

High SNR is not desirable only for better image quality but also for highest confidence of decision in IR search systems. Search systems operate at point source basis; target source is far away and can be considered as a point source. In such systems it is not important to visualize the target but to know whether it is there or not with a high probability of a correct decision. The principal concern is to assess the maximum SNR required for specified values of the probability of correct detection to minimize false-alarm rate [49].

All image sensor arrays are physically limited to their charge storage capacity by their limited pixel sizes. A very limited pixel area sets the upper limit for the amount of charge that can be stored. In most cases for the infrared arrays, this limit is around 20 million electrons. For example in an LWIR sensor array, integration time is held around 100 μs in order to prevent saturation of the limited storage capacitance. In a video application this time can be allowed up to 33msec (30 Hz frame rate). Hence the system is operating at lower SNR than possible. While maintaining the video frequency an increase of $\sqrt{330}$x SNR is possible (25dB).

In a digital storage readout, storage is done on a digital memory cell rather than an analog memory; capacitor. Hence, storage capacity increases exponentially for digital readouts. For example, in order to increase storage capacity 8x, only three additional bits are required. In an analog readout this would require 8 times the area, since the capacitance area is linearly proportional to the charge handling capacity. Already digital readouts achieving 3 Ge^- have been reported [40] with 89dB SNR and 2mK NETD values with a pixel area of 25 μm x 25 μm, which is the best NETD values reported up to date.

Aside, digital readouts with PFM show interesting kTC noise behavior. SNR of digital readouts is independent of the capacitance value for kTC noise contribution when multiple count values are being measured by a pixel. This allows single readout architecture to be deployed for dual band applications, since the need for very small or large capacitances for kTC noise is not a significant issue.

Furthermore a digital storage readout can operate at lower power consumption than analog readouts due to the absence of power hungry analog output drivers. Additionally digital readouts are scalable with technology and can follow Moore's law. The scalability with process and low power operation is in line with the SWaP trend of the IR imaging industry. Finally, with DROICs, non-uniformity can be implemented on-chip, a prospect for the third generation ROICs that has not yet met [32].

2.2 ROIC Architectures

2.2.1 Analog ROICs

An analog ROIC for a staring type FPA is shown in Figure 8.

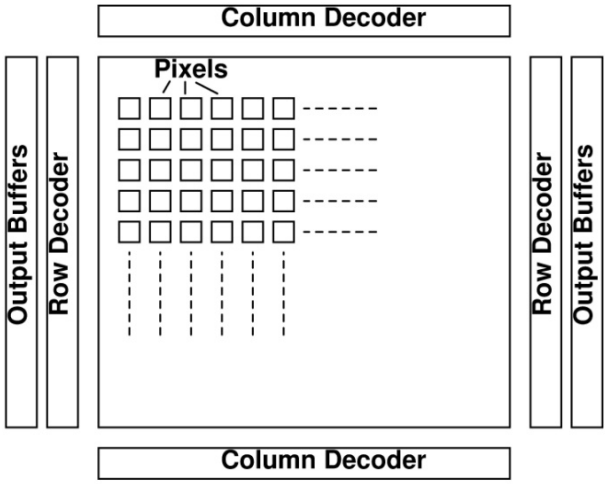

Figure 8 An analog staring ROIC

Here the first and perhaps the most important stage is the input preamplifier. Input preamplifiers main function is to pass the photo-generated electrons to the integration capacitor. While doing this, it should maintain a stable bias at the detector and it should also have low input impedance, so that the injection efficiency is high. Among various preamplifiers direct injection (DI), buffered direct injection (BDI) and capacitive transimpedance amplifier (CTIA) circuits are the most common ones due complying with the requirements of many detector arrays. Signal chain of an analog ROIC pixel is represented in Figure 9 with various noise sources.

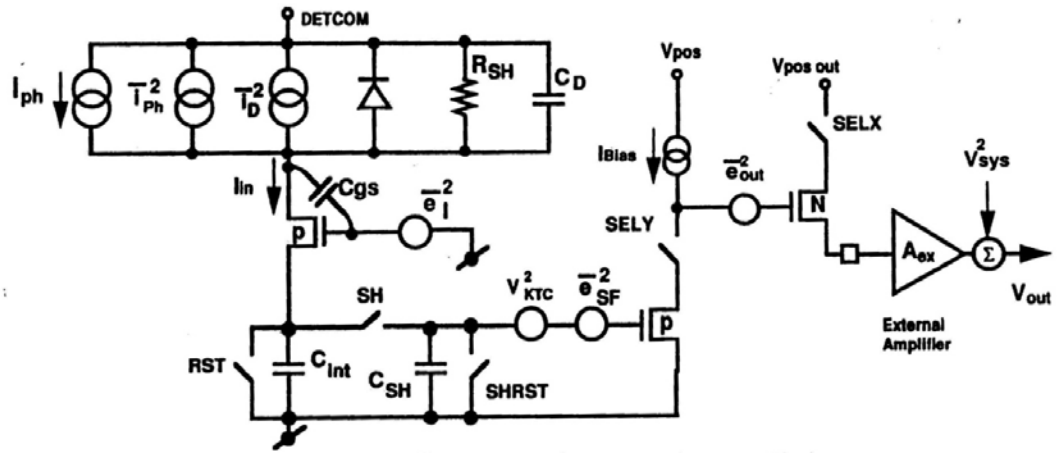

Figure 9 Analog readout signal chain and noise sources [31]

Following the preamplifier a unit cell buffer, possibly a sample and hold followed by a source follower is incorporated to get the data out of the pixel array. According to the type of the system, time delay integration (TDI) or correlated double sampling (CDS) is applied. For both methods, at least an additional storage capacitor is required.

The stored signals then multiplexed and read-out through an output buffer. Usually this buffer is the highest power consuming part of the readout. The power consumption is strongly dependent to the output load and settling time requirements.

Noise Analysis of Analog Readouts

As mentioned previously, the most critical parameter of a ROIC is its SNR. An analysis for the readout of Figure 9, (without TDI or CDS) is presented at this section [31]. First component of noise is at the integration capacitor due to the detector noise, input pre-amplifier noise and the reset noise.

$$V_{RMS1} = \left[\int_0^\infty i_t^2 |\eta(f)|^2 \left(\frac{T_{int}}{C_{int}}\right)^2 \frac{sin^2(\pi f T_{int})}{(\pi f T_{int})^2} df + V_{KTC}^2\right]^{1/2} \tag{2.6}$$

Where i_t^2 is the sum of detector noise with shot noise (i_{Ph}^2), detector thermal and 1/f noise (i_D^2) and input pre-amplifier noise (e_i^2), $\eta(f)$ is the injection efficiency, T_{int} is the integration time, C_{int} is the integration capacitor and V_{KTC}^2 is the reset noise.

$$i_t^2 = i_{Ph}^2 + i_D^2 + \frac{e_i^2}{|Z_D|^2} \tag{2.7}$$

Two other variables, input preamplifier transfer function and the injection efficiency are given as;

$$|Z_D|^2 = \frac{R_D^2}{1+(2\pi f R_D C_D)^2} \tag{2.8}$$

$$|\eta(f)|^2 = \frac{(g_m R_D)^2}{(1+g_m R_D)^2 + \left[2\pi f R_D (C_D + C_{gs})\right]^2} \tag{2.9}$$

where R_D is the detector dynamic resistance, C_D is the detector capacitance, C_{gs} is the input preamplifier gate-source capacitance and g_m is input preamplifier transconductance.

Following the input preamplifier we have the source follower output amplifier and the external amplifier. Their contribution to FPA noise can be calculated as;

$$V_{RMS2} = \left[\int_0^\infty e_{sf}^2 \, |A_{sf}(f)|^2 |A_{OUT}(f)|^2 |A_{EX}(f)|^2 df + \int_0^\infty e_{OUT}^2 \, |A_{OUT}(f)|^2 |A_{EX}(f)|^2 df\right]^{1/2} \tag{2.10}$$

where e_{sf}^2 is the input referred source follower noise power spectral density, e_{OUT}^2 is the output amplifier input referred noise power spectral density, $A_{sf}(f)$ is the source follower transfer function, $A_{OUT}(f)$ is the output amplifier transfer function and $A_{EX}(f)$ is the transfer function of the external amplifier. The transfer functions are assumed to be single pole as given in the equations below with their respected f_{3dB}.

$$|A_{sf}(f)|^2 = \frac{{A_{sf}}^2}{1+\left({f}/{f_{3dBsf}}\right)^2} \tag{2.11}$$

$$|A_{EX}(f)|^2 = \frac{{A_{EX}}^2}{1+\left({f}/{f_{3dBEX}}\right)^2} \tag{2.12}$$

$$|A_{OUT}(f)|^2 = \frac{{A_{OUT}}^2}{1+\left({f}/{f_{3dBOUT}}\right)^2} \tag{2.13}$$

Finally, the output noise is the square sum of the all noise components and is evaluated as;

$$V_{RMS,TOTAL} = \left[\left(V_{RMS1} A_{sf} A_{OUT} A_{EX}\right)^2 + (V_{RMS2})^2 + (V_{SYS})^2\right]^{1/2} \tag{2.14}$$

where V_{SYS} is the system noise. An example of noise analysis of an analog ROIC is represented in [31], results of which are shown in the bar diagram of Figure 10.

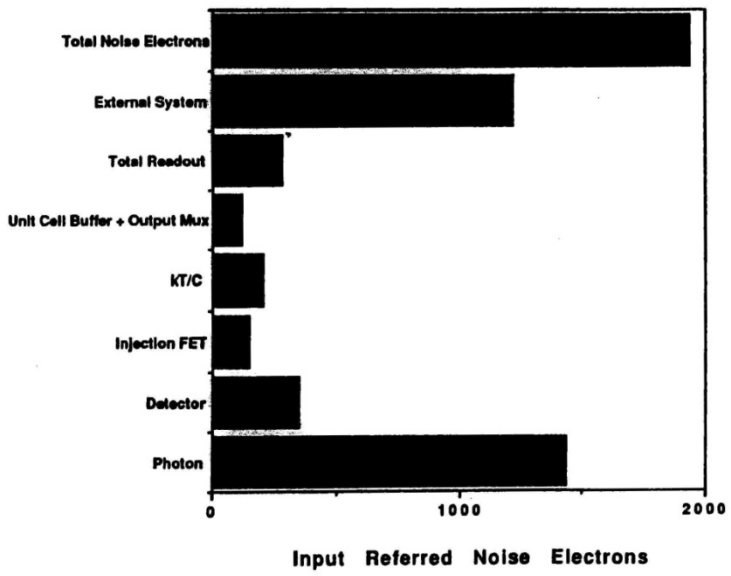

Figure 10 Input referred noise of an analog ROIC in number of electrons

As seen from the bar diagram, the photon noise (shot noise) is the dominant and inevitable noise source. The limitation of the analog readouts in terms of SNR also lies in the photon noise. Typical analog readouts have maximum of $20Me^-$ charge handling capacity for some high pitch detectors. Even if the only noise source is the photon noise, maximum achievable SNR is limited to 73dB in this case.

2.2.2 Digital ROICs

The most important impact of the digital readouts is their ability to handle larger amount of charges. Historically, this was not the main aim; rather what has been done previously was to put the ADC on chip, to reduce system cost, decrease quantization noise and additive external noise and also add more functionality on the digital domain. Not until recent years, readouts capable of holding a $3Ge^-$ were shown. Clearly the limit can be even higher, as long as the application requires it and sustains the required photon flux. The downside is actually at the low photon flux levels.

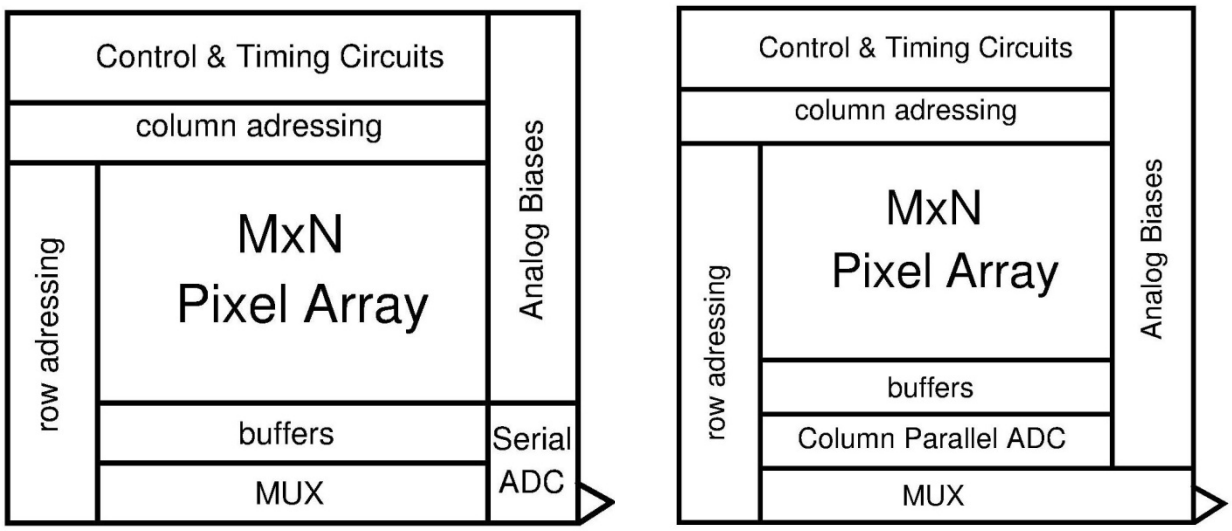

Figure 11 Serial ADC and Column parallel ADC DROICs [50]

There are two approaches to digital readouts. In the first one analog data is converted to digital data before being transferred to the output. In the second approach the data is stored digitally on a digital pixel. Of these two methods the latter one has the advantage to increase system SNR through increasing the charge handling capacity and is the subject to this thesis. Two circuit approaches of this type of readouts will be represented in this section and their SNR will be derived after a brief discussion of analog ROICS with A/D conversion on chip.

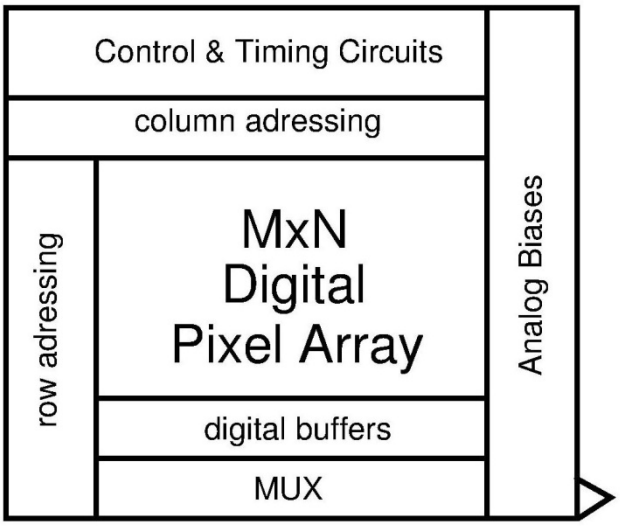

Figure 12 DROIC with digital pixel array[50]

2.2.2.1 DROICs with Analog Signal Chain

Various ADC topologies have been implemented in imaging applications in the past driven by the needs of visible imaging (commercial) applications market. Primary challenge is to implement a high resolution, low power yet high speed ADC. Industry has been focusing on column parallel architectures in order to accomplish this task.

One of the easiest ADCs that can achieve reasonable resolution and speed for imaging applications is the single-ramp single slope ADC architecture of Figure 13. In this architecture a global ramp signal is received by the in-pixel comparator and time to trigger is measured by a counter. Least significant bit (LSB) is measured by change of the ramp voltage over one clock period whereas the number of bits is determined by the counter bits. The conversion takes approximately 2^N cycles conversion time for N bit resolution. The slow operation, limits the use of this type of ADCs in large format arrays. A 10 bit example of this topology has been reported in [51] with 160x240 pixel format.

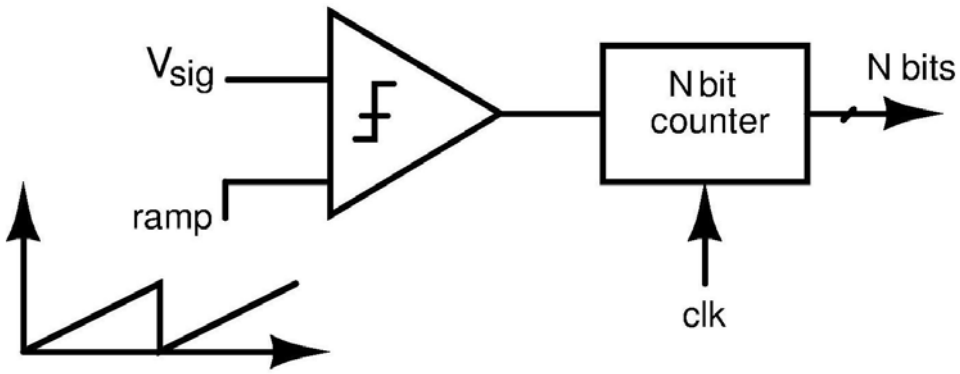

Figure 13 Single-ramp single-slope ADC

A very high speed example of single slope ADC has been reported by El Gamal's group with 10000 frames/s operation [52]. High speed operation has been achieved through pixel parallel implementation. However resolution is limited to 8 bits.

SCD has implemented dual-ramp single slope (DRSS) ADCs splitting the MSB and LSB conversion to two steps, which reduces the conversion time to $2^{N/2}$ cycles for N bit resolution. This commercial product of [53, 54] is designed for InSb detector arrays for IR detection, achieves 15 bit conversion with 640x512 array format for a power consumption of 130mW (at 120Hz).

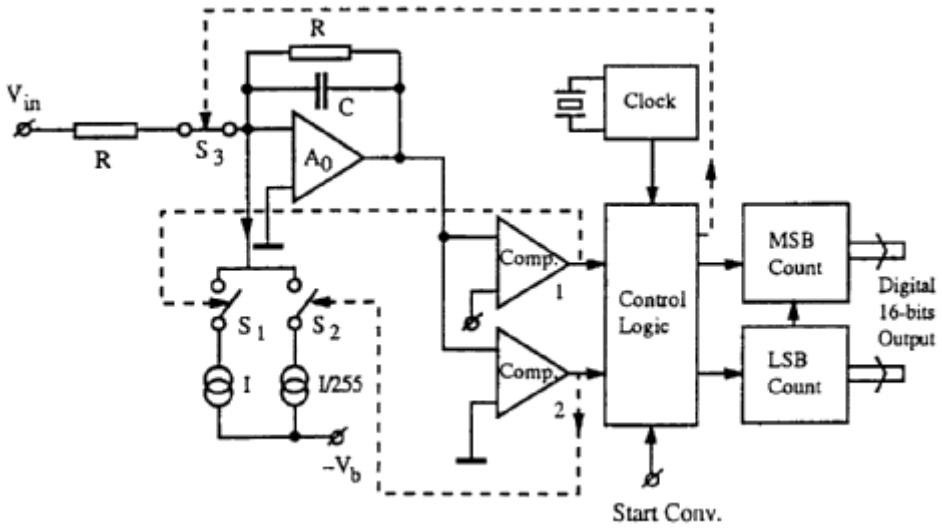

Figure 14 Dual ramp single slope ADC [53]

Successive approximation (SA) ADCs of Figure 15 has been applied in various APS arrays. A successive approximation ADC requires N clock cycles per conversion making it attractive for large arrays. The penalty is the power consumption for high resolution due to the DAC at the feedback.

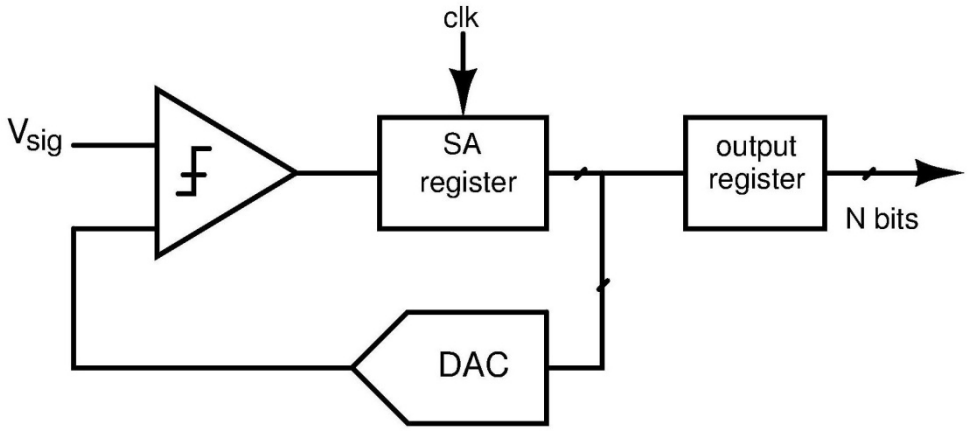

Figure 15 Successive approximation ADC

A 5000 frame/s CMOS APS array has been reported in [55] using a successive-approximation ADC with 8 bit resolution. Colum parallel approach has been used for 512x512 array format. A much more attractive implementation of SA ADCs is found in [56] with only 1.9μW power consumption for 10 bit resolution.

Over two-thirds of commercial ADCs in the industry are pipeline ADCs and due to their complexity, they are used as serial converters in imaging applications [57]. A pipeline ADC

consists of sub-converter stages with residue being transferred from one stage to another until the last one. Resolution requirements are reduced past the MSB stage making pipeline ADCs attractive [57].

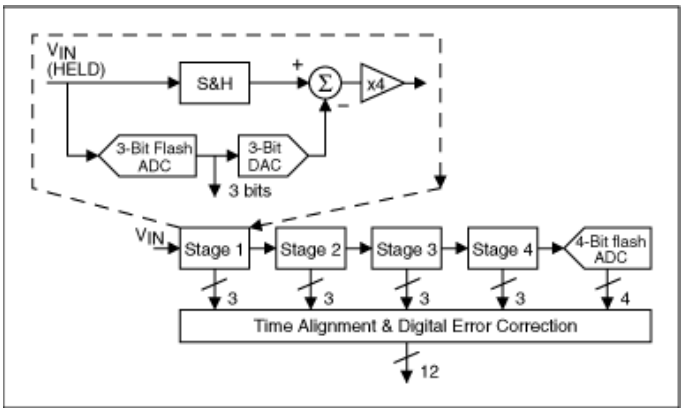

Figure 16 Pipeline ADC with 2 bit per stage conversion [58]

Many imaging applications have benefitted from pipeline ADCs. 12 bit HD TV format array of 1920x1080 has been reported in 2006 [59] 13 and 14 bit pipeline ADCs for bolometer arrays have been reported in [60, 61]. Raytheon [50] has patented pipeline ADC architectures on image sensors [57]. Teledyne (former Rockwell Scientific) has published on an ASIC called SIDECAR [62, 63] reducing the camera system to two chips; sensor array and the peripheral chip including all biasing, ADC conversion and image processing, that incorporates 16 bit pipeline ADCs.

The list can be enhanced with DROICs utilizing ADC topologies such as cyclic ADCs or time to digital type convertors. However either serial or column based parallel or with the exemptional example of [55] parallel architecture, all digital ROICs represented in this section are limited with the charge handling capacity of an analog ROIC. Only oversampling ADCs such as sigma delta ADCs or pulse frequency modulated (PFM) ADCs can achieve extreme charge handling capacities.

2.2.2.2 Delta Sigma ROICs

Delta Sigma ROICs are examples of digital pixel sensors (DPS). The use of ΔΣ in ROICs dates back to 15 years. Back then due to the pitch size of the CMOS technology, a per pixel ADC was not feasible in size. Rather the integrator part was implemented under each pixel and the comparator as well as the filter was shared [33-36]. Later works showed column parallel ADCs [64, 65] or split ADCs in which part of the ADC is placed in pixel [66-68].

With the ever decreasing pitch sizes of CMOS technology today, it is possible to fit the entire ADC under pixel area. The first approach is the conventional first order incremental ΣΔ as shown in Figure 17.

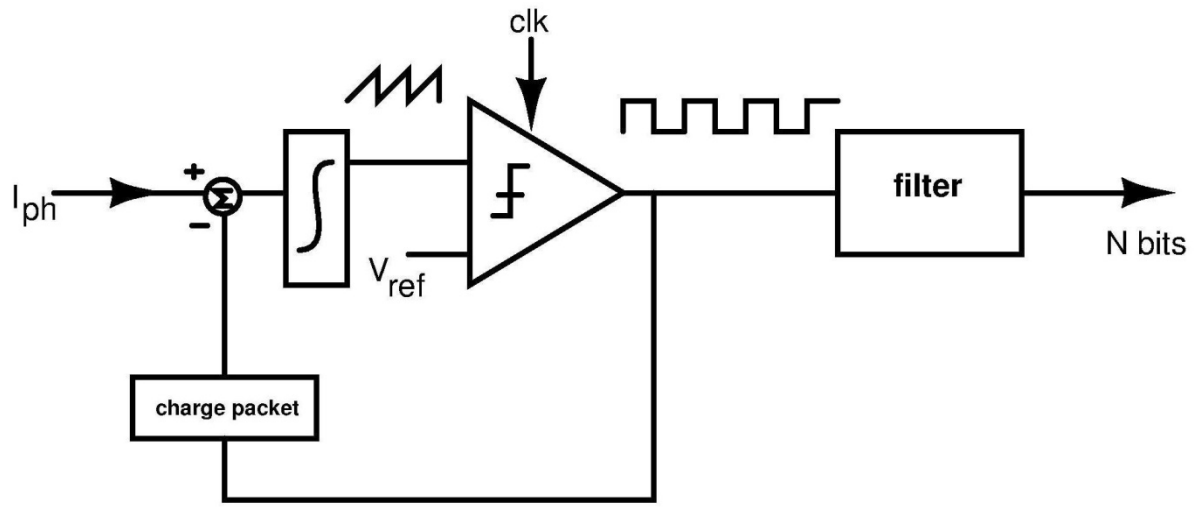

Figure 17 Block diagram of incremental ΣΔ ROIC pixel

Photocurrent, I_{ph} is integrated continuously and at every clock edge, integrated voltage is compared with the reference voltage V_{ref}. When the clocked comparator reference voltage level is reached, a fixed charge packet is removed from the integration capacitor. Comparator is monitored for threshold crossing at every clock cycle. The integrator at the input is one of the ordinary pre-amplifiers used in analog readouts such as DI, CTIA or BDI stage and the integration capacitor. At the comparator output binary sequence is filtered. The decimation filter used here can be a simple counter giving the digital representation of the accumulated photo generated charge. The counter value in this architecture is given as:

$$n_{counter}(i_{ph}) = {i_{ph}t_{int}}/{C_{int}V_{ref}} \tag{2.15}$$

where t_{int} is the integration time, C_{int} is the integration capacitance and V_{ref} is the comparator's threshold voltage. In this architecture output noise is the sum of quantization noise, the switching noise due to charge subtraction and the reset noise is evaluated as [37]

$$\sigma_{readout-eff} = \sqrt{\frac{(C_{int}V_{ref})^2}{12q^2} + n_{counter}(i_{ph})\sigma_{switch}^2 + \sigma_{reset}^2} \tag{2.16}$$

where σ^2_{switch} is the total noise per switching event and σ^2_{reset} is the kTC noise. Here shot noise or detector noise is not evaluated, and the quantization noise is limited with the step size $\Delta^2/_{12}$ with $\Delta = V_{ref} * C_{int}$ [69]. Hence in order to decrease the quantization noise, either integration capacitance should be reduced or comparator reference voltage should be decreased. The problem is then, the fixed pattern noise, the residual non-uniformity introduced by device mismatches. Almost all IR ROICs pass through an off-chip non-uniformity correction (NUC), yet there is a limit that the NUC can correct before the CMOS technology limit is achieved and the comparator is not making false transitions or no transitions at all. This limitation has lead to search for solutions to reduce quantization noise while not reducing the integration capacitance or the comparator reference voltage. One proposed solution is using an extended counting method to count the residue on the integration capacitor. This is effectively same as reducing the step size, without pushing the limits of the integration capacitance or the threshold voltage. A circuit solution is represented in Figure 18.

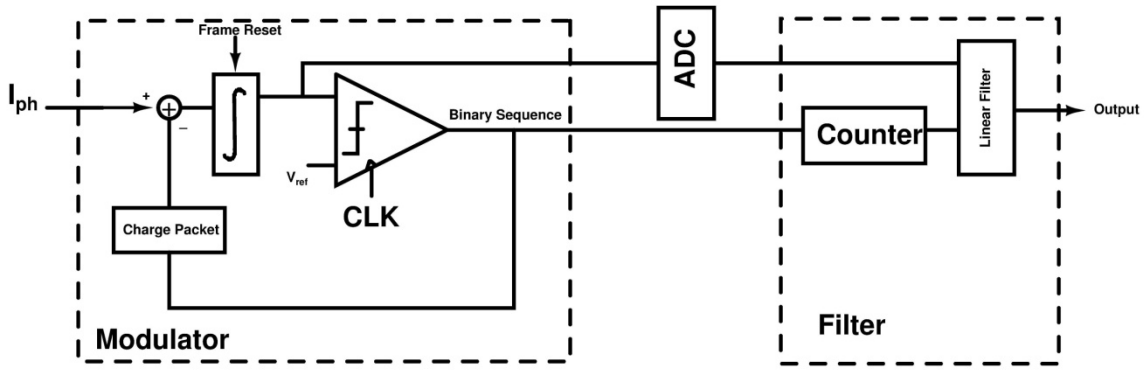

Figure 18 Block diagram of incremental ΔΣ ROIC pixel with extended counting [39]

The circuit is same except that there is an additional ADC to resolve the residue. In this case the step size is limited with the ADC's step size and quantization noise can be reduced without changing the integration capacitor or the reference voltage. In [38] Jansson shows a 16 bit readout with 8 bit coarse quantization from the counter and 8 bit precision with a successive approximation ADC. Output noise for this approach is given as in (2.17);

$$\sigma_{readout-eff} = \sqrt{\sigma^2_{ADC-readout} + n_{counter}(i_{ph})\sigma^2_{switch} + \sigma^2_{reset}} \tag{2.17}$$

The use of the second ADC is a very common practice [70, 71]. The issues associated with it are similar to those discussed about the DROICs with analog flows. These ADCs are shared and for large arrays and high frame rate operations power dissipation and circuit complexity become problematic.

The drawback of delta sigma DROICs is that in order to increase the dynamic range, one need to use a higher frequency clock, so that the integration capacitor is not saturated between two clock periods. So, higher dynamic range requires higher clock speeds (higher oversampling ratios) and higher power dissipation [68]. The charge packet subtraction can be realized through a CTIA circuit as shown in Figure 19.

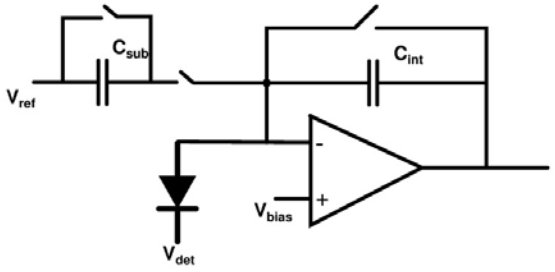

Figure 19 Capacitive Transimpedance Amplifier

Increasing the clock frequency means increasing the bandwidth of the CTIA amplifier, since the settling time of the subtraction circuit dictates the required gain-bandwidth product. Summing up, amplifier power increases as the square of the factor of increase in the dynamic range [39] which is not in line with the power reduction trend of ROICs.

2.2.2.3 PFM ROICs

Recent DROICs, [40-44] incorporate pulse frequency modulation (also called asynchronous self-reset). Excellent imaging results have been shown by MIT Lincoln Laboratory as well as SOFRADIR using this method. SOFRADIR has reported the largest charge handling capacity of $3Ge^-$ as well as the lowest NEDT of 2mK with their DROICs for LWIR detector arrays.

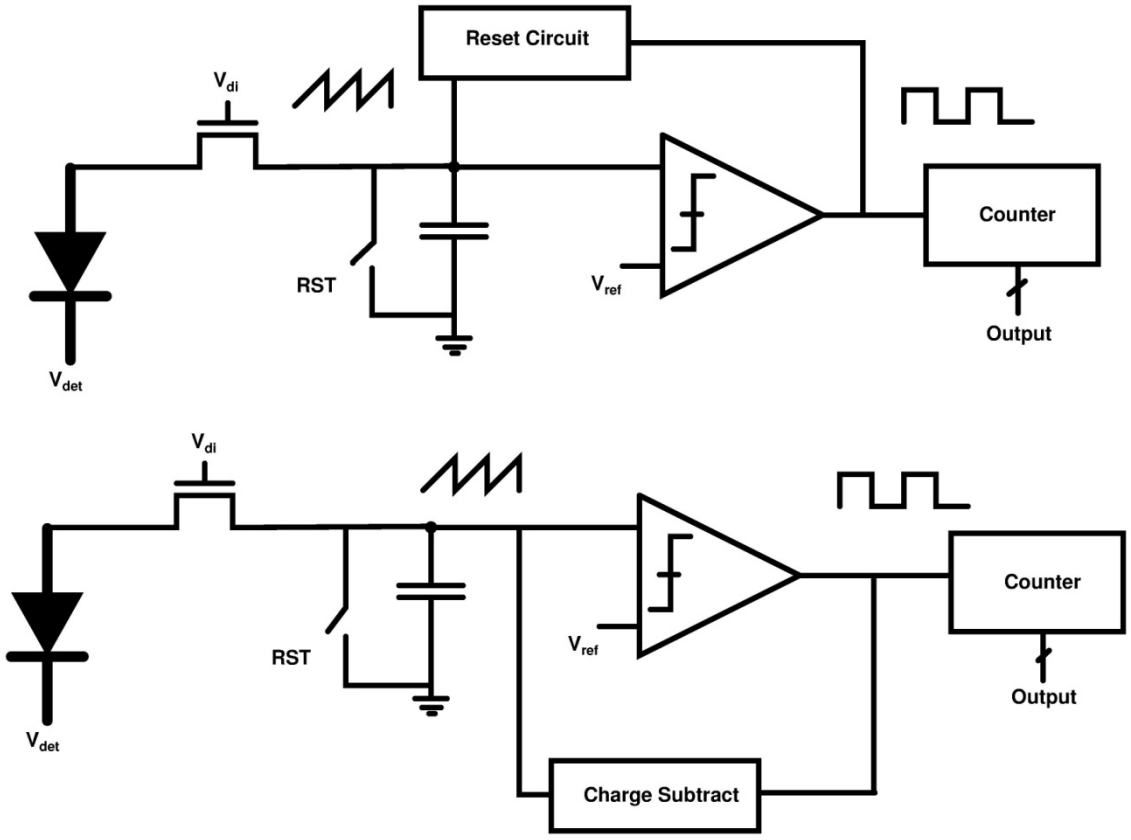

Figure 20 Pulse Frequency Modulate DROIC pixel circuits a) reset to voltage b) charge subtract methods

In pulse frequency modulated systems, photocurrent is again integrated on a capacitor and when the threshold voltage of comparator is exceeded, the comparator is triggered and the counter value is incremented. Note that when the comparator is triggered the integration capacitor is reset asynchronously. Counter value is incremented at every reset operation and at the end of the integration time, is read out or transferred to a memory for being transferred to output at its required timing. In this way significant power savings with respect to Delta-Sigma architecture can be achieved. In Figure 20.b, a second approach is represented which, as in the ΣΔ uses a charge subtraction method. In [43] it is discussed that the method is more prone to non-uniformity, with the use of a 12-b SRAM for programmability against mismatch.

Having described the basic operation principle of the pulse frequency modulation readout, noise analysis and SNR can be calculated. White noise contribution of sub-blocks is evaluated first together with the shot noise, followed by low frequency noise analysis.

$$n_{e-T} = \sqrt{\frac{C_{int}V_{mr}}{q} + \frac{kTC_{int}}{q^2} + \frac{e^2_{pa-white}\tau}{2q^2{R_d}^2} + \frac{8kTC_{int}{}^2}{3q^2 g_m \tau}} \tag{2.18}$$

where $V_{mr} = V_m - V_{reset}$, $e_{pa-white}$ is the white noise component of the preamplifier noise, R_d is the dynamic impedance of the detector, τ is the average time per count, g_m is the transconductance of the comparator, k is Boltzmann's constant, and T is the temperature. The four terms correspond to the shot noise, reset (kTC) noise, preamplifier noise, and comparator noise. This is the number of noise electrons in single count. In N_{counts} this becomes

$$n_{e-E-N} = n_{e-T}\sqrt{N_{counts}} \tag{2.19}$$

The 1/f noise contribution of the circuit components and the detector is:

$$n_{e-LF} = \sqrt{\left[i_T^2\left(\alpha_{1/f}^2 + \alpha_{comp@1Hz}^2\right) + \frac{e^2_{DI_n@1Hz}}{{R_d}^2}\right]\left(\frac{t^2}{q^2}\right) ln\left(\frac{t_{samp}}{t_{int}}\right)} \tag{2.20}$$

where, $i_T{}^2$ is the detector current and $\alpha_{1/f}$, α_{comp}, e_{DIn} correspond to the detector, comparator and injection pre-amplifier 1/f noise contribution factors. Finally, the quantization noise is given as:

$$n_{e-Q} = \frac{C_{int}V_{mr}}{q\sqrt{12}} \tag{2.21}$$

The total noise in electrons in N_{counts} is given as:

$$n_{e-T-N} = \left\{\left[\left(\frac{C_{int}V_{mr}}{q} + \frac{kTC_{int}}{q^2} + \frac{e^2_{pa-white}t_{int}}{2q^2{R_d}^2N_{counts}} + \frac{8kTC_{int}{}^2N_{counts}}{3q^2 g_m t_{int}}\right)N_{counts}\right] + \left[i_T^2\left(\alpha_{1/f}^2 + \alpha_{gain_n@1Hz}^2\right) + \frac{e^2_{DI_n@1Hz}}{{R_d}^2}\right]\left(\frac{t^2}{q^2}\right) ln\left(\frac{t_{samp}}{t_{int}}\right) + \frac{C_{int}{}^2V_{mr}{}^2}{12q^2}\right\}^{0.5} \tag{2.22}$$

At this point to get further insight from the above complicated equation, it is assumed that the detector is ideal and produces an electron for an incident photon (quantum efficiency is one). In this case the total number of photo-generated charge is equal to

$$q \times ph = i_{ph}t_{int} = NC_{int}V_{mr} \tag{2.23}$$

$$\mathrm{N} = \frac{\mathrm{ph}\times\mathrm{q}}{\mathrm{C_{int}V_{mr}}} \tag{2.24}$$

Using equation 19, and knowing that the signal in N_{counts} is equal to $N_{counts} \times C_{int} \times V_{mr}$ SNR can be written as;

$$SNR = \frac{1}{\left(\sqrt{\frac{1}{ph}+\frac{kT}{V_{mr}\times ph\times q}+\frac{e_{pa-white}^2 t_{int}}{2q^2 {R_d}^2 ph^2}+\frac{8kT}{3{V_{mr}}^2 g_m t_{int}}+\left[i_T^2\left(\alpha_{1/f}^2+\alpha_{gain_{n@1Hz}}^2\right)+\frac{e_{DIn@1Hz}^2}{{R_d}^2}\right]\left(\frac{t^2}{q^2 ph^2}\right)ln\left(\frac{t_{samp}}{t_{int}}\right)+\frac{{C_{int}}^2{V_{mr}}^2}{12q^2 ph^2}}\right)} \quad (2.25)$$

From this equation, it is seen that as the number of photons increases, SNR is improved as expected with square root dependence. Second, in terms of SNR it is required that V_{mr} is to be kept high while $C_{int} \times V_{mr}$ should be reduced. This is also interesting to note since this shows that step size cannot be reduced to lower the quantization noise without an additional SNR penalty.

SNR of the PFM DROIC can easily go up to 80dB as shown in Figure 21 [43]. However there is a limitation at the bottom end of collected signal charges which is due to the quantization noise limit. This is due to the integrated charge packet step of around 7500e^-, which results quantization noise floor of 2200 e^- is reported. The contribution of various noise sources are represented in Figure 21. As seen from the graph at low photon flux levels, readout is quantization noise limited.

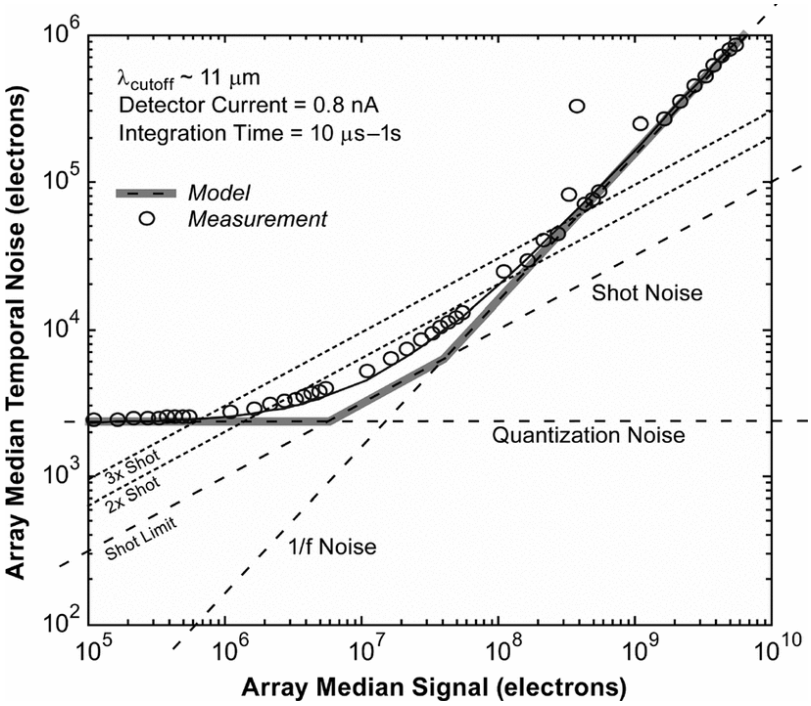

Figure 21 Noise in electrons vs the collected signal electrons [43]

Another example of a pulse modulated DROIC has been shown by SOFRADIR in 2010 showing that the FPA's with digital readouts employing per-pixel ADCs will be on the market soon. The key properties of this readout are that it can handle a charge up to $3Ge^-$ and achieve an NETD of 2mK; both parameters are the best values reported up to date. The ADC resolution is also 15 bits.

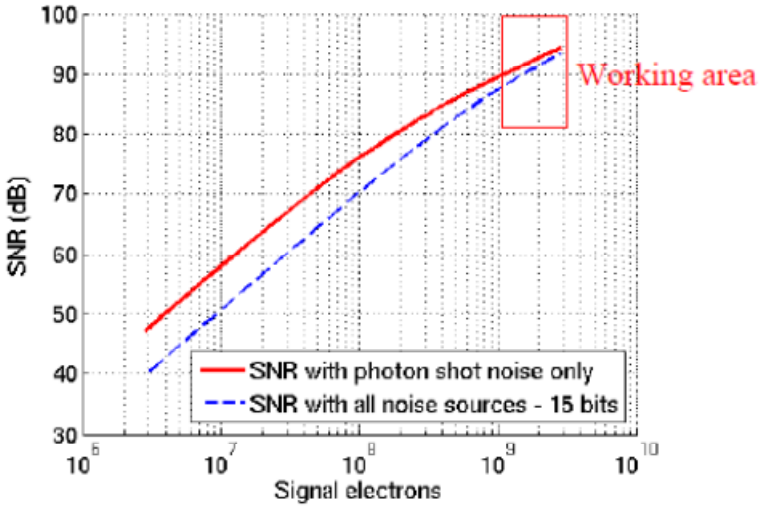

Figure 22 SNR with respect to signal electrons [40]

SOFRADIR's example shows significantly higher quantization noise primarily due the operation region has already been defined for signal electrons higher than $1.1Ge^-$. SNR is reduced around 50dB for flux levels corresponding to 10^7 signal electrons. This is due to the very coarse quantization of 91.000 electrons on a 14fF integration capacitor with 1V comparator threshold. The quantization noise is 26.300 electrons. However if the reported ROICs are to be used for a MAW system of HFI system then, readout would have a high frame rate of 800Hz, so that the imaging will be fast; this will reduce the integration time and the integrated charge would be much less than $1.1Ge^-$; integrated charge would be $68Me^-$. Corresponding SNR would be around 55dB for this ROIC. This shows that, if the flux levels are low, or the frame rate requirements are high, it is required to come up with a solution to reduce the quantization noise in order to operate closer to the shot noise limit.

2.3 Proposed Circuit Architecture – Extended Counting

As described in the previous sections, in order to maximize the frame rate while operating the large format ROICs with low power operation, it is the most feasible approach to put A/D

conversion to the pixel area. This massive parallelism is realized by PFM type DSP architecture. However quantization noise limits the use of DROICs with low flux scenarios, especially at high frame rate applications. In order to reduce the quantization noise PFM DROICs with extended counting method of Figure 23 is proposed.

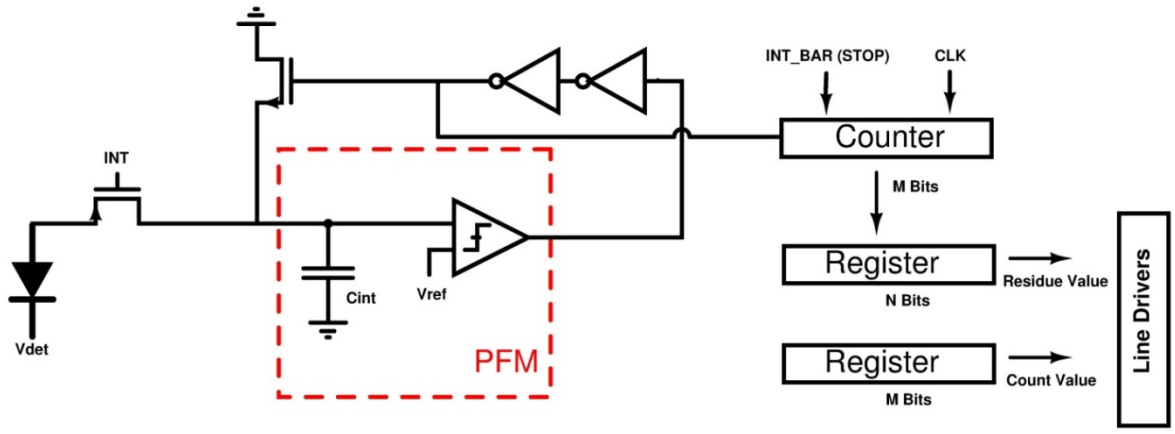

Figure 23 Proposed pixel architecture

As in a two stage ADC, operation of the proposed pixel circuit consists of two phases: a coarse quantization phase and a fine quantization case. The first phase is where the incoming photon flux is measured in terms of the number of resets on the integration node. During this phase the operation of the proposed circuit is as an ordinary PFM pixel circuit. At the beginning of a frame all the counters and integration capacitors are reset to zero. As the charges accumulate on the integration capacitor, its voltage increases and finally approaches to the comparator threshold voltage. At this instance comparator output makes a transition to the high level which is sensed by a pos-edge counter. The count is incremented by one while the inverters at the top delays the comparator output pulse for few hundred picoseconds before the reset switch is activated and sets the capacitor voltage to zero again. This procedure is repeated until the end of the integration time. At the end of the integration time, value at the counter is immediately transferred to the storage register.

At the second phase, residue is to be measured. For this objective, the same counter is operated as a clocked counter in order to measure the time that is required to re-trigger the comparator one more time. Integration of the photocurrent on to the integration capacitor is allowed to continue at this phase. In a sense, residue measurement is handled as in a single slope ADC with multiple ramps. In fact the number of ramps is equal to the number of pixels. As soon as the counter is trigged one more time, count operation is halted. And the value at

the counter, which is a representation of the time elapsed to fill the integration capacitor to the comparator threshold voltage, is transferred to its storage register. Finally there is still a residue left at the integration capacitor due to the discrete time operation of the counter. This value is quite smaller than the residue left in an ordinary PFM pixel. This will be discussed in detail in the following sections.

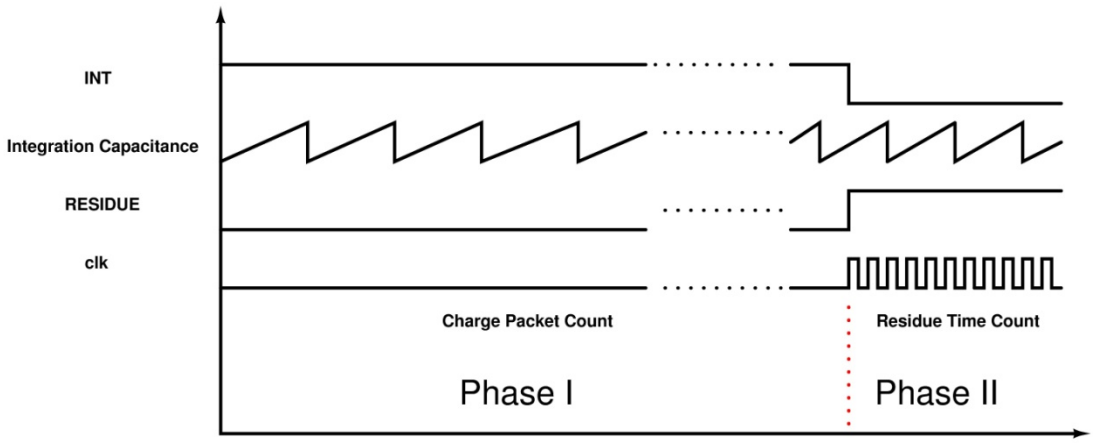

Figure 24 Operation phases of proposed pixel

As soon as the residue time data is transferred to its register, a new integration can be started. Each pixel holding the data for the count value and the residue time, can integrate a new frame's data while the previous frame's data can be transferred to the output. In this way DROIC is capable of doing an integrate-while-read (IWR) operation. The two data is used to calculate the correct output value for the given integration time. The count data is incremented by one, and the residue time is added to the integration time which is measured by a global counter that is incremented at every clock cycle during the programmed integration. This is done for each pixel serially at the peripheral circuitry. So, at this point each pixel has a count value and a unique integration time. Peripheral circuitry normalizes the count value to the global integration time as in (2.26).

$$Output = \frac{INT\_TIME \times Count}{(\text{Residue Time} + INT\_TIME)} \tag{2.26}$$

An example can make the operation more clear. Suppose for an integration time of 300 clock cycles the counter value is 29. ROIC pixel continues to integrate until the comparator triggers one more time and let this duration be 7 cycles. The result for this pixel is then 30 counts for 307 clock cycles. Since it is desired to know the value for 300 cycles (integration time) for all pixels on the array, peripheral circuits calculate the digital representation of the integrated

charge as $30 \times 300/307$. The quantization error in this case will be signal dependent with a step size of the integrated charge in a single clock cycle. The quantization noise again will be lowered, as well as the quantization noise being smaller for lower signal levels than higher ones.

With the proposed circuit, lower quantization noise can be achieved while still having large charge handling capacities. This has the potential of more than 130dB dynamic range, with improved SNR at the lower flux regime.

As provided in the previous sections, increasing charge handling capacity improves the SNR. Very high SNR values up to 89 dB have been achieved by DROICs [40]. However the trade of is now with the SNR performance of pixels that have lower amount of photo-generated charges. The quantization noise at the lower end reduces the SNR performance. In other words, DROICs, while achieving high dynamic range and high SNR at high photon fluxes, suffer from poor SNR at low photon flux levels. The same discussion is also true for high frame rates. For high frame rates, due to reduced integration times the integrated charge decreases, even if the irradiance is high, increasing the significance of the quantization noise.

In Table 3 a comparison of the state of the art on DROICs with extreme charge handling capabilities are given together with the proposed architecture. The proposed method can decrease the quantization noise to a level of 200 electrons, an order of magnitude improvement with respect to state of the art, while keeping the high charge handling capacity of 2.335Ge^-. Aside, the proposed ROIC can operate at a lower power consumption mode than the state of the art.

Table 3 Comparison of state of the art with the proposed DROIC

	Pixel pitch (µm)	**Integration Capacitance (fF)**	**Integration voltage (V)**	**Capacity (Ge-)**	**Quantization Noise Floor (e-)**	**Number of Bits**
SOFRADIR	25	14	1	3	26,000	15
MIT	30	1.38	0.565	10	2,200	15
Proposed Method	30	12	0.475	2.335	161 (Function of input current)	22

With the proposed method, achievable quantization noise is a function of input current and the residue counting clock period. As described previously, when the integration is stopped by the master integration clock, the proposed DROIC continues to integrate until another toggle of the comparator is achieved. The operation can be summarized as below:

1. Integration starts with the high assert on integration master clock
2. During the integration, every time the reference voltage of the comparator is exceeded, the comparator is reset and the counter is incremented
3. At the end of integration time the value at the counter is passed to a memory for storage of the count value
4. Residue measurement starts and counter is reset for initialization
5. Counter receives a clock (residue clock) to measure the residue on the integration capacitor. At every clock cycle the counter is incremented to measure the time
6. As the comparator threshold voltage is exceeded one more time, the counter stops, having the digital representation of the time value spent to measure the residue
7. The value of the counter is transferred to a memory to be transferred to the periphery and a new integration cycle can be started at this point
8. Using the time value and the count value, and having measured the integration time globally, peripheral circuit scales the output of the measured pixel to the real integration time.
9. Scaled pixel value is read

As described above, the remaining residue can be measured in time, with only additional circuit of digital memory used to store the residue measurement time and additional, minor control logic. The method proves very useful at the lower end of the stored charges. In order to analytically evaluate the performance of the proposed circuit some assumptions for the additional memory and the residue clock period should be made. These are:

1. A residue clock frequency of 100MHz (10ns period), which can easily be achieved in submicron CMOS technologies, and can be tuned to any other frequency according to operational needs.
2. 14 bit memory to keep the residue count. This can be scaled according to the detector requirements. Specifically the minimum detector current, photocurrent and the dark current, sets the amount of extra memory.

As seen from Table 3 a 12fF integration capacitor and a 0.475V comparator reference voltage is selected for validating the proposed method. These two correspond to a charge packet of 35,625 electrons. Without applying any further means to decrease the quantization noise, designed DROIC would have a quantization noise of 10,284 electrons. With the proposed method, at the low photo-currents (low photon flux levels) the quantization noise can be, theoretically, as low as 3 electrons.

First the lowest current that can be detected with improved quantization noise performance is to be calculated. Given 14 bits of memory for residue time count and a residue clock of 10ns, makes the longest residue measurement (extended integration) time as 163.84µs. Comparator should be trigged once at the end of 163.84µs. From this and equation (2.27),

$$Q = C \times V = i \times t \tag{2.27}$$

$$12f \times 0.475 = i \times 163.84 \tag{2.28}$$

$$i = 0.035nA \tag{2.29}$$

The minimum current that will cause a triggering of the comparator at the extended integration time is found to be 35pA. Considering dark currents on the order of hundred pico-amperes for LWIR detectors, this is a practical value. Any current lower than this, will have a quantization noise of 10,284 electrons.

Having stated the minimum resolvable current, minimum quantization noise that can be achieved with the proposed circuit can be calculated. The uncertainty of the measurement or the unmeasured residue in the proposed method is the integrated charge within a residue clock period. For the 10ns residue period, the step size is given by (2.31) as 2.18 electrons, corresponding to a quantization noise of 0.62 electrons.

$$\Delta = i \times t_{residue\ clock} \tag{2.30}$$

$$\Delta = \frac{0.035n \times 10n}{1.6 \times 10^{-19}} = 2.18 \text{ electrons} \tag{2.31}$$

$$QN = \frac{\Delta}{\sqrt{12}} = 0.62 \text{ electrons} \tag{2.32}$$

Of course, these are theoretical values and the sensitivity of the comparator to achieve this low level signal swing and the required bit depth to represent 0.62 electrons are challenging issues.

Having defined the minimum achievable quantization noise with the above defined assumptions, it is beneficial to state some current range for the detectors that are to be bonded to these DROICs and analyze the corresponding quantization noise levels. For this purpose, a current range of 1-100nA is assumed for analyses. As an example, SOFRADIR assumes a range of 8nA to 24nA of input current[40]. Also in [44] power consumption values are reported for input currents of 1-2 nA.

All step sizes and corresponding quantization noise levels can be calculated by (2.30) and can be seen from Table 4. Additional number of bits is the bit size required to reduce the step size of 35,625 electrons to the step sizes described in the table.

Table 4 Quantization noise as a function of input currents

	Δ (e^-)	**QN (e^-)**	**Additional number of bits**
1nA	62.5	18.04	10
10nA	625	180.4	6
100nA	6250	1804	3

In theory, shown quantization noise levels of Table 4 can be achieved with the cost of increased word size. This is in well agreement with increasing the dynamic range of any digital representation.

2.3.1 Realization: What is practical?

There is an ever increasing trend on number of pixels of staring focal plane arrays. 1024x1024 focal plane arrays have been introduced into the market for years. This in return brings the difficulty of processing huge amount of data out of the pixel while achieving video frame rates. In a DROIC the amount of data to be processed is also scaled by the bit length of the digital representation. 15 bit [40, 41] and 16 bit [42, 43] solutions have been shown in literature. This section shows that a 6 bit additional conversion on a 16 bit coarse quantization can be implemented practically.

16 bit coarse quantization with a step size of 35,625 electrons can represent a charge handling capacity of 2.33Ge$^-$. As proposed, to reduce the quantization noise to less than 200e$^-$, 6 additional bits are required. This in sum, results a digital representation of 22 bits.

The proposed method allows to measure even smaller step sizes, with lower quantization noise levels of 18 electrons. However then the pixel data is to be represented by 26 bits, assuming the same charge handling capacity, 2.33Ge$^-$, is required. If the charge handling capacity is to be reduced by sixteen times, then the representation is again 22 bits. Scalability of the digital representation is another advantage of DROICs. It is beneficial to restate some important remarks at this point, and announce additional assumptions for the pixel circuit.

Remarks:

1. Achievable dynamic range is related to the bit size of the digital representation. As the bit sizes are increased, dynamic range increases as well.
2. SNR at the lower end is driven by the quantization noise. As the quantization noise is reduced, the low illuminated pixels will have better SNR. Bit depth is irrelevant for SNR for low level illuminations.
3. Bit depth of a DROIC can be scaled (by end user) depending on the emittance from the scene

Assumptions:

1. A residue clock frequency of 100MHz (10ns period),
2. A 16 bit memory to store the count value during integration time,
3. 14 bit memory to keep the residue count,
4. Pixel size of 30µm x 30µm.
5. Array size of 256 x 256 elements

While investigating the practicality of achieving a 200e$^-$ quantization noise with the proposed method, the first thing is to look if the required circuits will fit in the pixel area. Using a 90nm CMOS technology and 30 bit memory in a pixel area of 30µm x 30µm is feasible, allowing plenty of area for the remaining circuits. All parameters will be calculated for 256x256 array so that a fair comparison can be made with the state of the art PFM DROICs [40, 41, 43, 44].

How is 22 bit output achieved with a quantization noise less than 200e$^-$ from the 30 bit in-pixel data? The 16 bit pixel data stores the count data during the integration time. The 14 bit memory stores the residue time required for one additional comparator toggle. Then the 22 bit output is evaluated according to (2.33)

$$Output = \frac{INT\_TIME \times (Count + 1)}{(\text{Residue Time} + INT\_TIME)} \tag{2.33}$$

where, INT_TIME is the integration time, count is the value stored in the pixel counter and Residue Time is the time value stored in the 14 bit memory. INT_TIME is the digital representation of 22 bits for the integration time. It is output from a counter that operates with a 10ns residue clock. INT_TIME can measure up to 41,94ms, which is more than enough for 50Hz video operation. Count is represented with 16 bits. Residue count is represented with 14 bits with same least significant bit size of INT, and is added to the integration time. From the above equation (14) a 22 bit output is given.

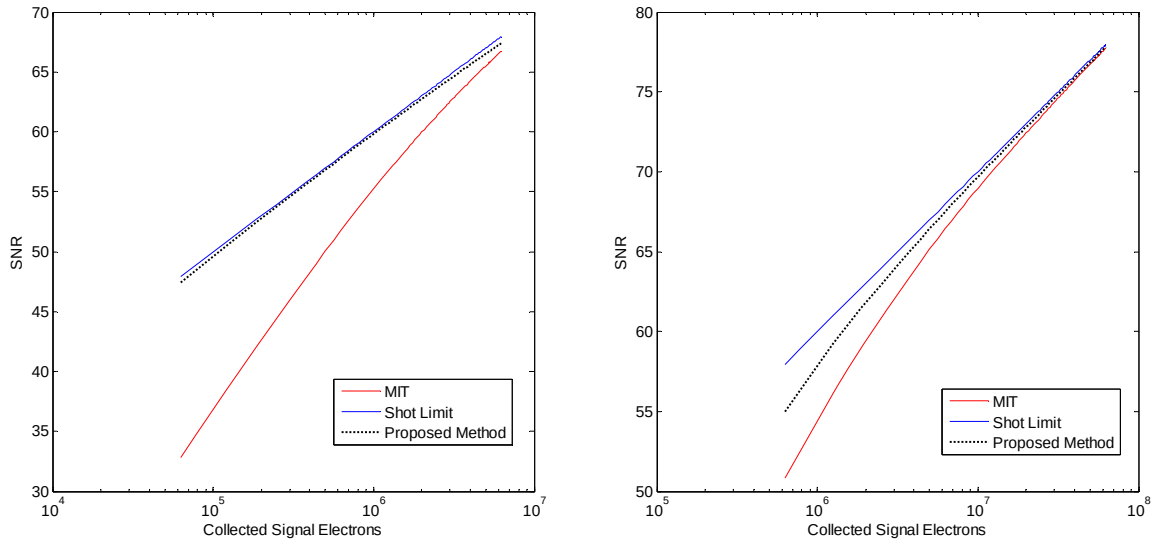

Figure 25 Comparison of the SNR performance of the proposed method with the SNR performance of the readouts of MIT Lincoln laboratory for two different integration times. Left : 10nA with integration time 10us, Right: 10nA with integration time 10ms.

Then, the quantization noise is less than 200e$^-$. Of course different bit sizes for each representation can be selected, or can be left as user programmable during the design of DROIC. The numbers used are merely to provide more insight on the practical application of the proposed method.

SNR performance of the proposed method with 22 bit accuracy is compared with the performances of readouts of SOFRADIR and MIT Lincoln Laboratory as shown in Figure 25 and Figure 26. The comparison metrics are the same except for the quantization noise. Clearly proposed method proves very effective especially at improving the SNR at low levels of illuminations.

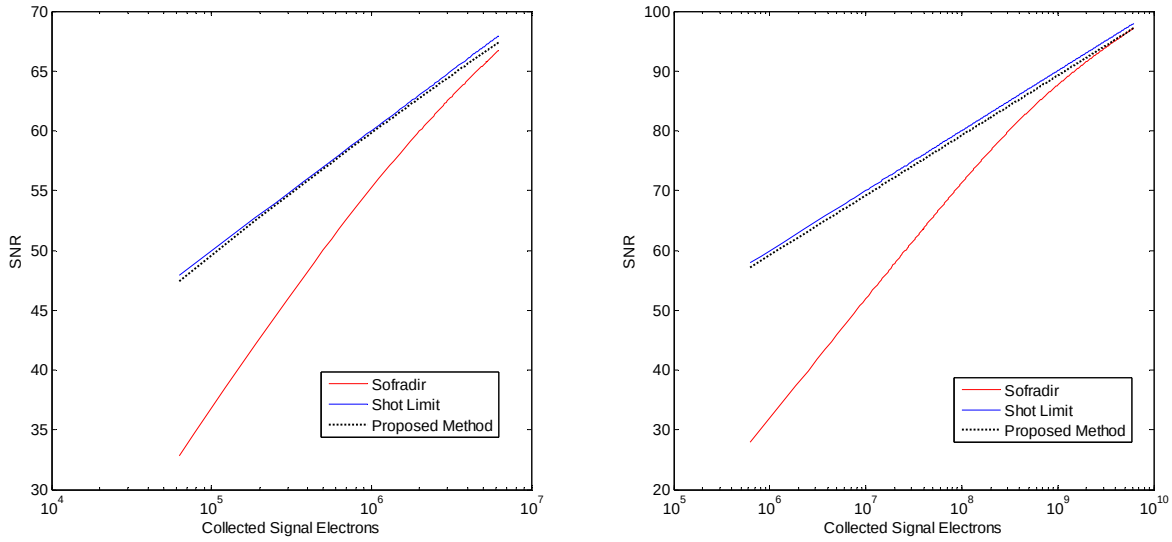

Figure 26 Comparison of the SNR performance of the proposed method with the SNR performance of the readouts of SOFRADIR for two different integration times. Left : 10nA with integration time 10us, Right: 10nA with integration time 10ms.

Another important aspect to be analyzed is to calculate the bit rate out of the pixel core and out of the chip. For a 256x256 array with 30 bits of data per pixel and 50Hz operation the bit rate out of the core is:

$$30 \times 256 \times 256 \times 50 = 98.3\text{Mb/s} \tag{2.34}$$

In order to reduce the data rate, data from the core is transferred to periphery in 30 bit parallel. 9 metal layers of the 90nm process allow this to be practical. Without any drivers, 400Hz frame rate is achievable with 2 output configuration for a 256x256 array. For 50Hz with parallel transfer scheme, data rate is 3.27Mb/s and for 400Hz frame rate, data rate is 26.2Mb/s.

Data is processed at the peripheral circuitry to be represented as 22 bits. Assuming a single output configuration, the bit rate for each output can be calculated as:

$$22 \times 256 \times 128 \times 50 = 36\text{Mb/s} \tag{2.35}$$

If 400Hz frame rate is required, then the bit rate per pixel will be 288Mb/s. This speed can be achieved by an LVDS output bus easily. With CMOS logic levels, it is better to use multiple outputs for fast frame rate operation. If 4 parallel output buses are used, than the speed of a single bus will be 144Mb/s at 400Hz frame rate. Hence, both the clock speed required to transfer data from the core to periphery, and from periphery to output can be achieved easily in sub-micron CMOS technologies.

In conclusion, the proposed method promises low quantization noise and extreme charge handling capacity with manageable circuit constraints such as area, data throughput and process technology. It is left to chapter 4 to discuss that these prospects can be met in a low power operation with the proposed technique.

3. IMPLEMENTATION

This chapter gives details about the designed prototype that is used for empirical verification of the proposed method. First an overall view of the chip is given followed by the pixel architecture and pixel sub-blocks. Design details of each sub-block with alternative and chosen topologies are reported. Simulation results are given to show functionality and finally test methodology and measurement results are reported.

3.1 Prototype Architecture

A staring array of 256x256 is shown in Figure 27. DROIC consists of pixel circuit matrix of 256x256, column and row decoders (digital control circuits), peripheral circuits that set the desired bit size and digital output buffers (I/O pads).

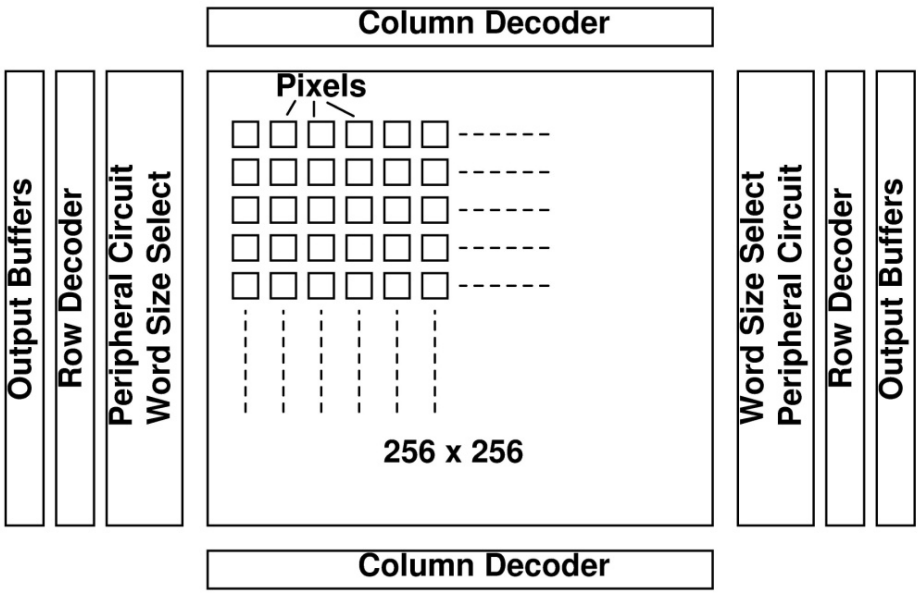

Figure 27 Block diagram of the prototype staring type DROIC

Each pixel has its own pixel circuit according to the proposed method block diagram of which is given in Figure 28. The first stage is a direct injection unit cell, which is followed by the integration capacitor and the comparator circuit. The two inverters at the output node of the comparator are used for pulse shaping so that the comparator output rises to the power supply level and counter can be triggered. Whenever the comparator output is one, the reset NMOS transistor is activated and resets the integration capacitor, and the counter is incremented. At

the end of the integration period, M (16) bit value at the counter is transferred to the M bit register. The counter operates as a clocked counter until the comparator threshold is exceeded once more. At this instant, the value of the counter is passed to N (14) bit register to be transferred to the ALU. A new integration can be started immediately. Whenever 30 bit pixel data (16 bit count, 14 bit residue) is transferred to the output, it is scaled to 22 bits and read out.

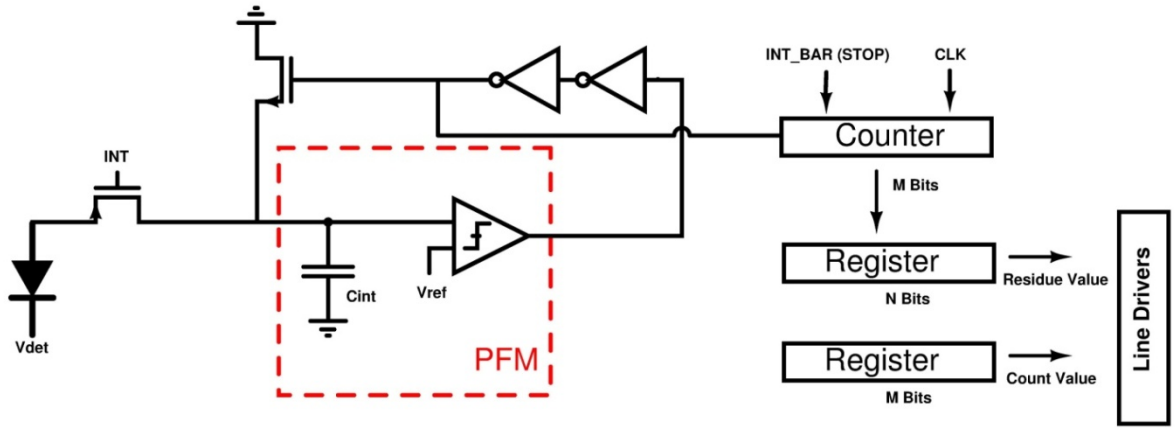

Figure 28 Block diagram of the proposed pixel circuit

Although all design parameters are evaluated towards a large scale staring array, implemented prototype is in a 32x32 array format. 32x32 array is selected in order to reduce manufacturing cost, while being able to submit the largest design for fabrication with an affordable cost.

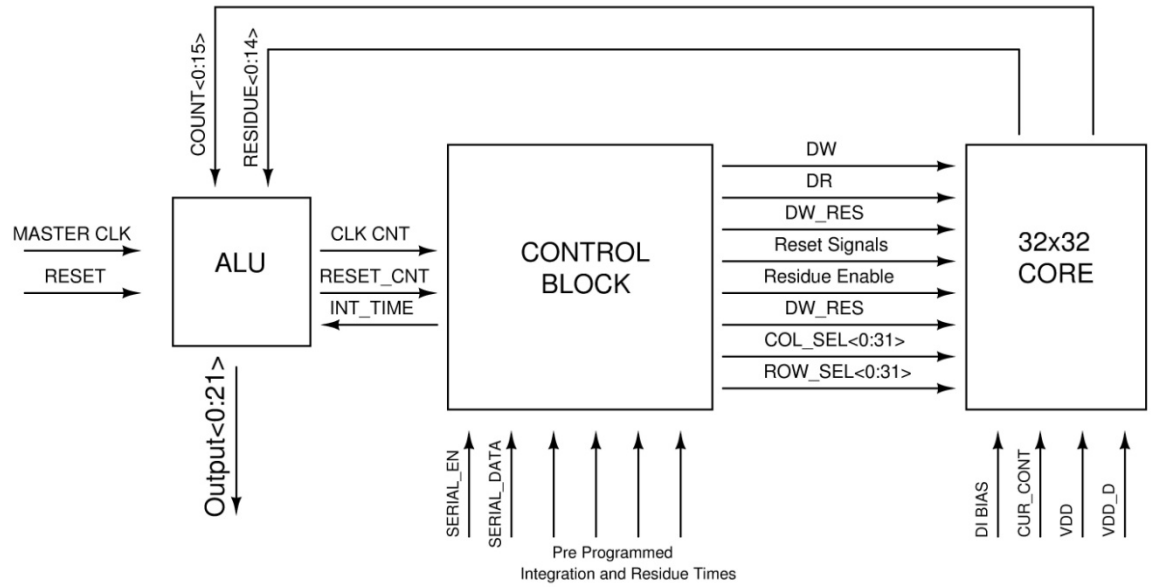

Figure 29 Block diagram of the prototype

Additionally, pitch size is 30µm, making a 32x32 array large enough prototype for TSMC miniasic run with 1,920 µm x 1,920 µm minimum area, including various standalone test blocks. A block diagram of the designed 32x32 array is represented in Figure 29.

In a quick look, prototype has three core blocks, the arithmetic logic unit; ALU, the control unit and the 32x32 pixel core. Master clock is received by the ALU, and the 22 bit output data is synchronized to the master clock. A slower clock, generated by the master clock, is supplied to the control unit. ALU receives the data from the 32x32 core, by the command of the control unit. Control unit supplies the digital code of the integration time as well. Using the data from the core (16 bit count, 14 bit residue time, 30 bit total), and integration time from the control unit (20 bit), ALU calculates the 22 bit output data. With this 22 bit information, the readout is capable of handling 2.33 Ge^- with a step size of 557 e^- and quantization noise of 161 e^-. Clearly, as proposed, readout is capable of handling two order higher charge handling capacity than analog readouts and one order lower quantization noise than digital readouts. Additionally, design technique can be focused on the higher end or lower end's favor easily.

In order to operate functionally, control unit needs to be programmed first. Programming is done via a serial interface through the serial enable and serial data ports. Serial data should be synchronized to the control unit clock, which is 26 times slower than the master clock. Residue clock period is generated from the master clock as well. This eases the design of the whole system requiring operating from a single clock. In case there are issues with serial interface, a parallel pre-programmed integration time and residue time setting is available through control block input pins.

The core block is completely controlled by the control unit. It receives reset, data write, data read, residue write, residue enable signals, and column and row decoder signals from the control unit. Aside from it there are only 2 control voltages required; DI bias and the current control voltage. DI bias is integral part of the DROIC. The current control bias is for testing purposes only and sets the input current value for the array. Additionally there are six separate power supplies to operate the prototype. Supplies are separated in order to monitor power consumption of different blocks, and in fact one supply for all pure digital and one supply for digital parts would be enough.

Process technology to design the prototype is chosen as 90nm TSMC mixed-signal / RF option. 90nm node is selected due it is much more affordable than the 65 nm or 40 nm

options. However, larger charge handling capabilities can be offered by use of a smaller technology node, or for a lower charge handling capacity, a higher, hence cheaper, technology node can be selected. Since the primary concern of the proposed DROIC is to offer a wide dynamic range ROIC with reduced quantization noise, 90nm node is the most convenient choice.

3.2 Pixel Architecture

The physical organization of sub-blocks in a 30x30 µm pixel is shown in Figure 30, schematic representation of which is given in Figure 28. Most of the area is consumed by pure digital circuits such as counters and memories, making the DROIC scalable with the technology.

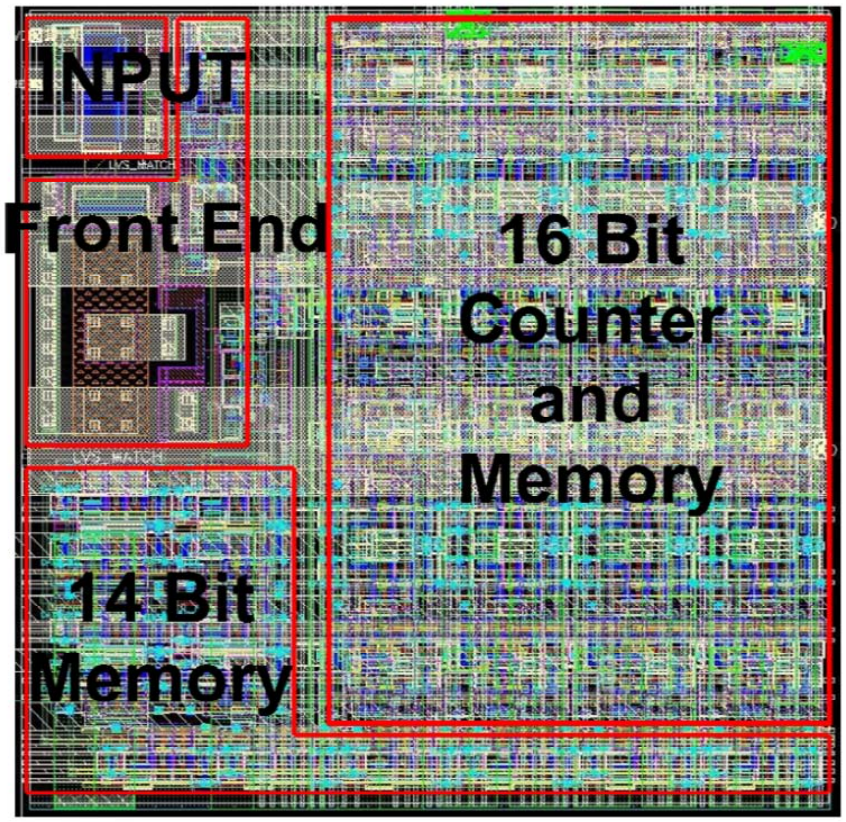

Figure 30 Layout of the prototype single pixel, 30 µm x30 µm (650 devices)

Input circuit is a PMOS transistor to supply input current instead of photo-current. Front end consist of integration capacitor and comparator. There is a small control logic used to stop the counter while measuring the residue and it is not highlighted in the image. Finally 16 bit

counter is implemented with 16 bit memory dumped in, in order to ease the routing. 14 bit memory is distributed to the bottom and bottom left corner of the pixel.

3.3 Pixel Sub-blocks

3.3.1 Comparator and Reset Circuits

Comparator design is critical in many ways at the design of DROICs. Comparator should be fast in order to preserve good linearity. It should be low power and it should be insensitive to process variations, or should show variations that could be corrected easily by two point correction. In a sense, all linear variations are acceptable, since for IR detectors NUC is mandatory and linear errors such as offset and gain variations can be corrected easily.

Two types of comparators have been designed and investigated. The first one is based on an operational amplifier and is shown in Figure 31. An operational amplifier without the feedback is essentially a comparator. Additionally, observe that even if the amplifier is two stage, no compensation capacitor is required due to the lack of feedback during operation.

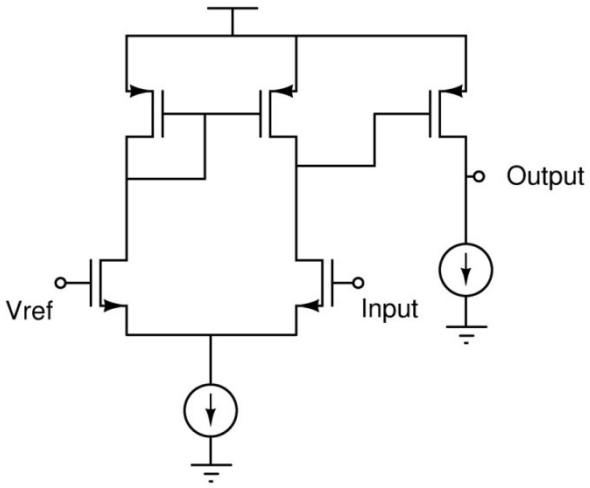

Figure 31 Operational amplifier based comparator

The drawback of an op-amp based comparator lies in its power consumption. In order to have a fast transition, the tail current should be high. Additionally, if used without an additional reset circuit, comparator's transition time will cause significant non-linearity. Assuming a finite reset time of t_{reset}, count value with respect to the input current can be calculated as:

$$\left(\frac{V_{ref}\times C_{\text{int}}}{i}+t_{reset}\right)\times Count = T_{INT} \tag{3.1}$$

$$\left(Q_{packet}+i\times t_{reset}\right)\times Count = i\times T_{INT} \tag{3.2}$$

$$Count = \frac{i\times T_{INT}}{Q_{packet}+i\times t_{reset}} \tag{3.3}$$

where V_{ref} is the comparator reference voltage, C_{int} is the integration capacitance and T_{INT} is the integration time. Clearly, for a linear relationship between the current and the Count value, $i\times t_{reset}$ must be zero. This limits the use of op-amp comparator, due its response being slow for low power operation.

A circuit solution to overcome the non-linearity due to comparator transition time is also proposed [72] and shown in Figure 32. In this approach $i\times t_{reset}$ product is saved at the temporary node. Whenever the integration capacitor is reset, a secondary PMOS switch is opened preventing the loss of charge during the finite reset time by preserving the charge at its source node capacitance.

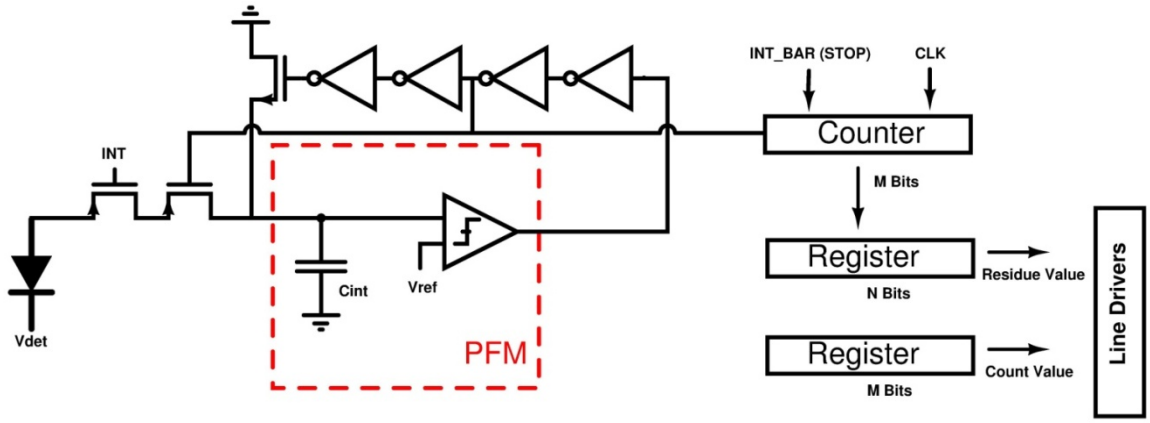

Figure 32 Modified pixel circuit to improve linearity

Another circuit approach for the comparator circuit is inverter based as shown in Figure 33. The transition from low to high is controlled by the threshold voltage of the inverter. The advantage of this type of comparator is that the response is fast, so good linearity can be achieved by the pixel circuit with no static power consumption.

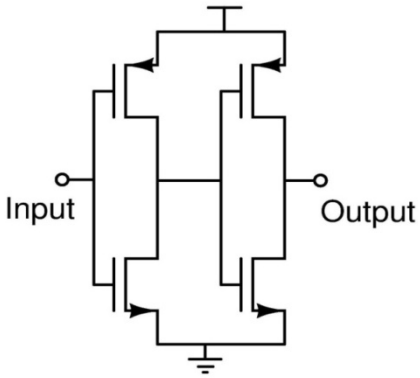

Figure 33 Inverter based comparator circuit

Reset circuit is formed by two inverters and an NMOS transistor. The two inverters are used for pulse shaping. The designed inverter based comparator has 200ps rise/fall times and the linearity performance is excellent. For an input current sweep of 1nA-100nA, the output linearity has an R^2 fit of 0.99996. The simulated graph is represented in Figure 34.

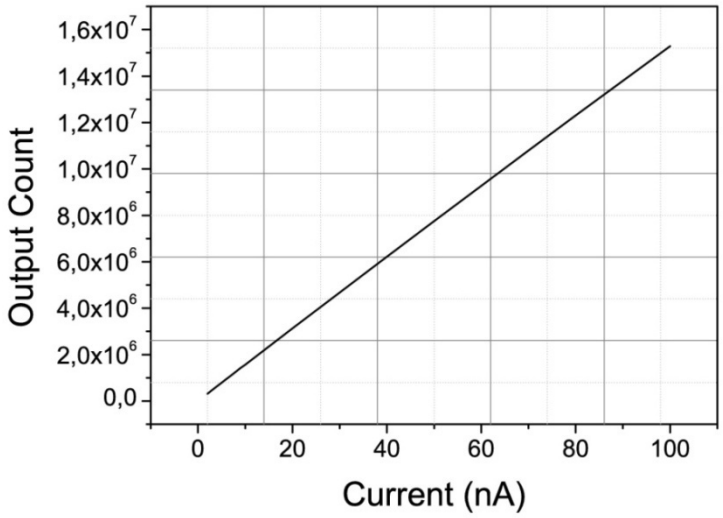

Figure 34 Output count vs input current

The comparator and the reset circuits, together have a device count of only 9 transistors.

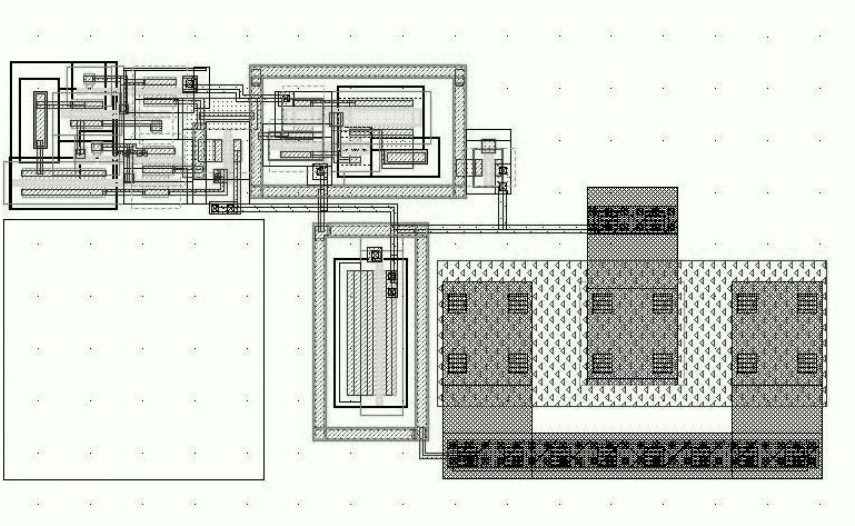

Figure 35 Front end of the pixel circuit. Area is 8.10 µm x15.8 µm including 5 µm x 5 µm bond opening at bottom left corner.

3.3.2 Binary Ripple Counter

Due to the limited pixel area, it is required to use the smallest possible counter. Also with the packet size of 35,625 electrons and maximum current of 100nA, the speed requirement of the counter is relaxed. In fact, the speed specification depends on the period of the residue clock, which is 10ns. It is still a relaxed parameter and the smallest counter can achieve nearly 2 GHz of operation frequency.

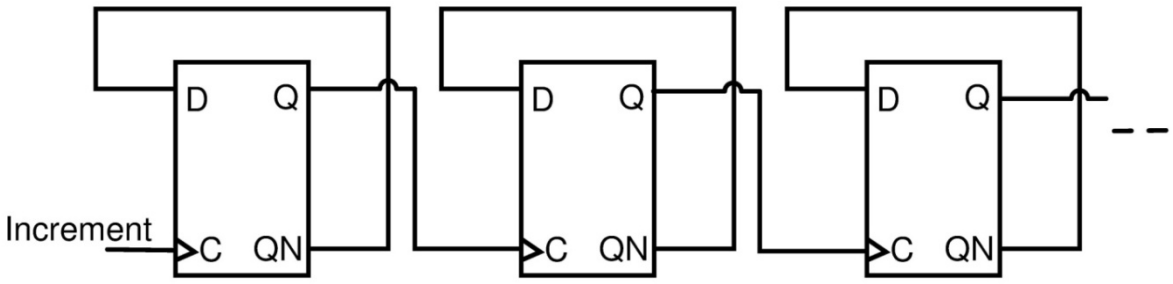

Figure 36 Block diagram of binary ripple counter

Since the speed is not an issue, smallest possible counter, which is a binary ripple counter, is implemented. A gray coded counter would do less transitions and consume less static power, however, the area requirements dictates the use of binary ripple counter. As seen from Figure 36, binary ripple counter consists of D flip flops (DFF). Each DFF is static and has two stage master and slave latch architecture with 20 devices, making it 360 devices per pixel for the

counter circuit. Additionally, 16 bit memory is also implemented in the counter to ease the routing.

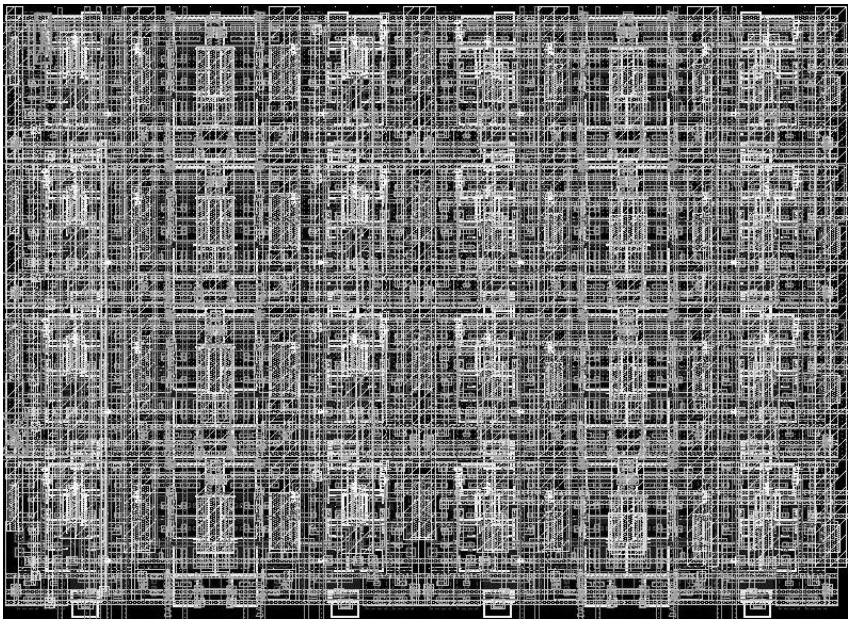

Figure 37 Binary ripple counter and 16 bit memory layout. Area is 26.7 μm x 19 μm including the 16 bit memory

3.3.3 Memory and Line Drivers

Static memories are preferred as the in-pixel memory for their robustness and due to the lack of necessity for refresh operation of a dynamic random access memory (DRAM). An SRAM cell with an additional inverter at the input as shown in Figure 38 has been implemented. The inverter at the input is required to overcome the low drive capability of the binary ripple counter. Each memory cell has 10 devices per cell. A 30 bit memory is required in-pixel with the proposed method, 16 bit for the count and 14 bit for the residue time, making up to 300 devices per pixel for the memory. Single memory cell layout occupies an area of 7 μm^2. Total memory area occupies 200μm^2.

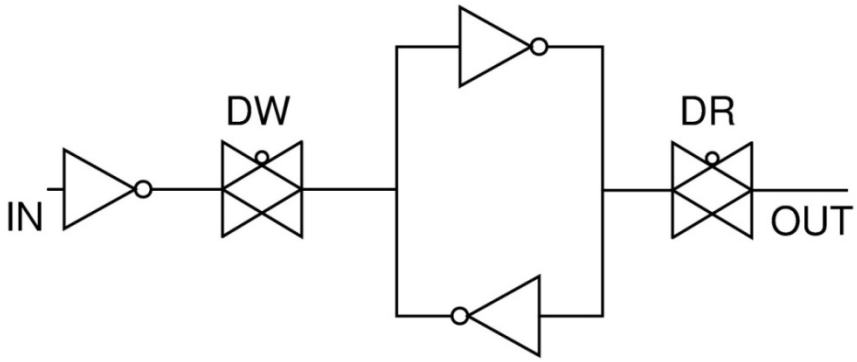

Figure 38 Block diagram of memory cell

Due to area requirements, no additional buffers are used under the pixel area. Instead all the data of a pixel, are output in parallel. Hence low speed of driving strength of a single SRAM cell is not an issue due to massive parallelism. In fact, simulations show that the pixels driving the bus for 1 pF load capacitance can drive ALU in 70 ns, resulting in a maximum frame rate of 400Hz for a 256x256 array. Faster operation is possible if drivers following the row select switches are inserted. Figure 39 represents the layout of 14 bit additional memory used to hold the residue time data.

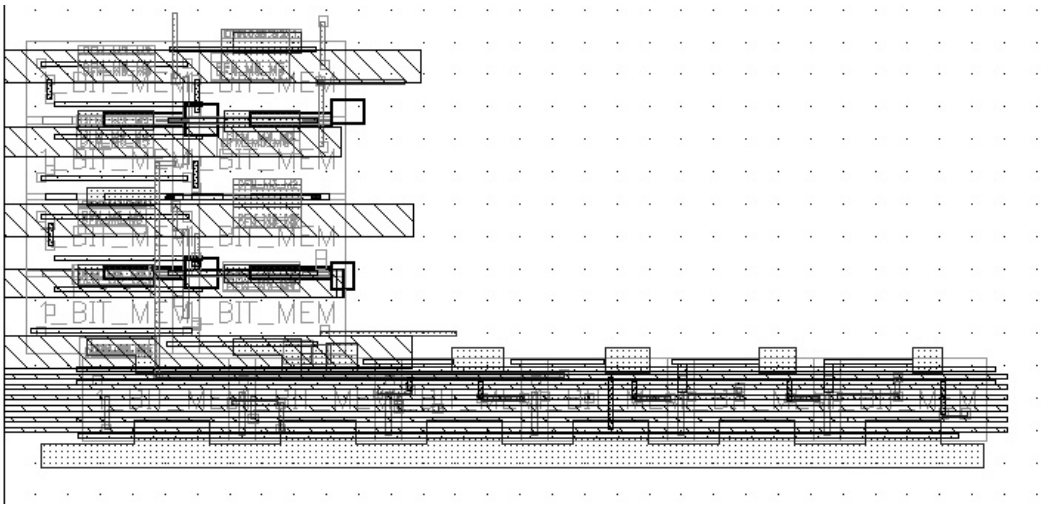

Figure 39 Layout of the 14 bit memory, 202.8 µm x µm (13.2 µm x 10.2 µm + 19.5 µm x 3.5 µm)

3.3.4 Counter Control Logic

There is additional control logic of Figure 40 implemented in-pixel to stop the counter whenever the final toggle of the comparator happens during the residue measurement.

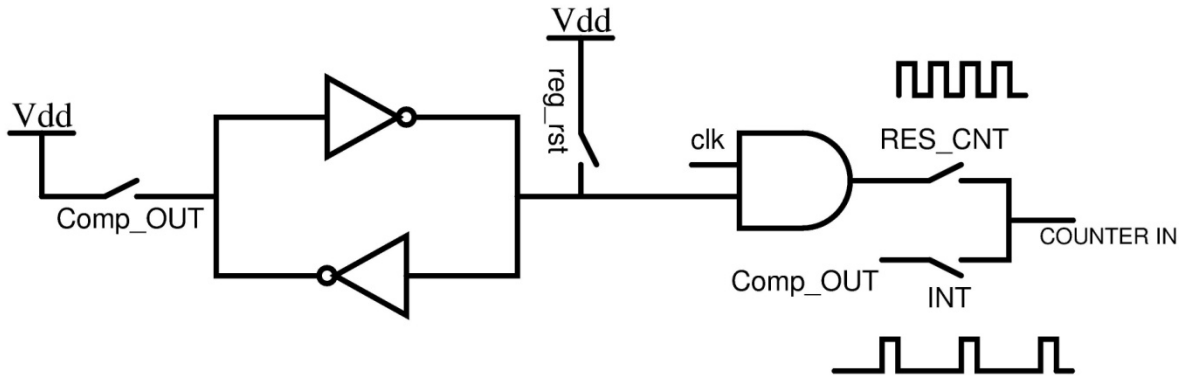

Figure 40 In-pixel counter control logic

At the beginning of the residue measurement, SRAM at the input is reset, allowing the AND gate to be active for count operation. When the comparator output is high again (the last toggle), SRAM output is set to low level and AND gate output is set to low, disabling the counter. During the integration period, through the switch controlled by the INT signal, comparator output pulses are connected directly to the counter.

3.3.5 Input Test Circuit

A PMOS transistor with 4 μm length and 1 μm width has been used to supply the input test current. Input current is controlled through the gate voltage of the PMOS transistor and the current is varied between 1 nA and 100 nA. Three control voltages are available at the chip I/O. Each row's current can be set to desired level through one of the three voltage levels.

3.3.6 Control Unit and the Arithmetic Logic Unit (ALU)

Control logic and arithmetic logic unit are implemented using verilog language. For synthesis, Synopsys Design Compiler has been used. Encounter has been used for physical design and behavioral model has been mapped to 90nm TSMC standard cell library.

From TSMC, only verilog models and standard delay files for the standard cells are available. Other views, such as schematics or layout views are not supplied by the foundry. As a result, no layout views are presented; rather circuit area of each block is reported. The black box area of the ALU is 270 μm x 86 μm and the control unit area is 113 μm x 1000 μm.

Control block is responsible for generating all the required control signals of Figure 41, where the uses of each are represented in Table 5 and Table 6.

Table 5 Control block signals

	Signal Name	Direction	**Functionality**
CONTROL UNIT	CLK_CNT	INPUT	Master clock from ALU
	RESET_CNT	INPUT	Initialization reset
	SERIAL_EN	INPUT	Serial programming enable
	SERIAL_DATA	INPUT	Serial data for programming
	PARALLEL<0:2>	INPUT	Parallel mode pre-programmed operation
	DW	OUTPUT	Data write from counter to count memory
	DW_RES	OUTPUT	Data write from counter to residue memory
	RESET_COUNTER	OUTPUT	Counter initialization
	RESET_INPUT	OUTPUT	Integration capacitor initialization
	COL_SEL<0:31>	OUTPUT	Colum select during read operation
	ROW_SEL<0:31>	OUTPUT	Row select during read operation

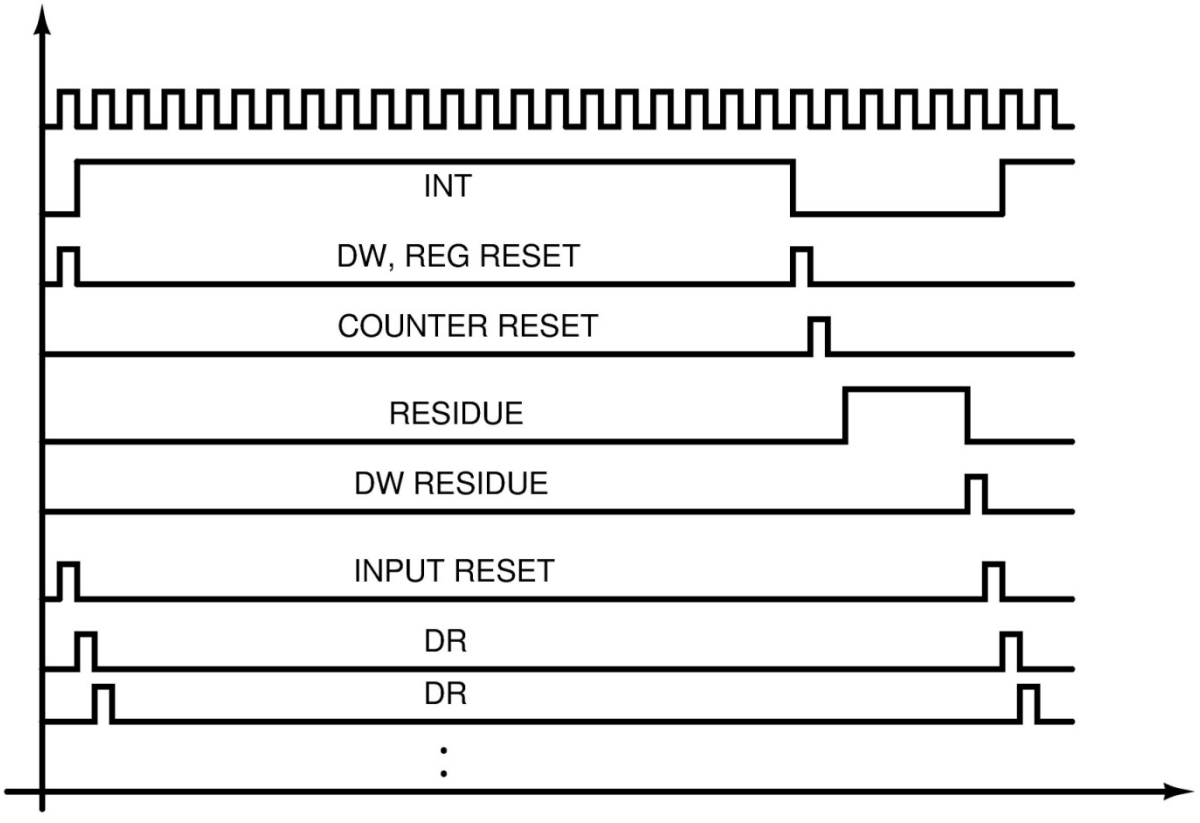

Figure 41 Control Signal Timings

Table 6 ALU signals

	Signal Name	Direction	Functionality
ALU	MASTER CLK	INPUT	Master clock
	RESET	INPUT	Initialization reset
	COUNT<0:15>	INPUT	Count data
	RESIDUE<0:13>	INPUT	Residue time data
	INT_TIME	INPUT	Global integration time
	OUTPUT<0:21>	OUTPUT	Pixel output data

ALU is responsible for calculating the output data from the input count, residue time and integration time data. ALU operates by command of the control unit and processes each pixels data in 26 clock cycles. Each pixel is processed by the ALU serially.

3.4 Test Blocks

There are various separate test blocks implemented in this prototype. Four standalone pixels, 2 DACs, various transistors with different sizes, four operational amplifiers and three ring oscillators are implemented in this prototype. It is important to mention that the prototype is pad limited, rather than area limited, due many I/O pads are required.

Four pixels are placed at the bottom left corner with 6 bit count and 6 bit residue output and a single buffered output, showing the integration capacitor value. From this setup, various design parameters can be analyzed; power consumption of a pixel, input current to frequency conversion and also jitter. Control signals of these pixels are supplied completely from external sources.

Various transistors have also been implemented in order to monitor the process and also, aside from the thesis work, in order to measure the cryogenic behavior of the 90nm TSMC process. If these transistors prove operable, and models seem to be within corner analysis limits when simulation temperature is set to 77K, this process will be used to build cryogenic readouts in the near future.

There are also four operational amplifiers to be tested separately. These op-amps are used in the design of the DAC as well. These op-amps are used in order to observe their behavior in cryogenic temperatures, as they are key elements of analog design.

Finally, to have more information of the digital domain operations at cryogenic temperatures, three ring oscillators have been laid out.

3.5 Layout of the Prototype

The designed prototype is shown in Figure 42, occupying an area of 1920 µm x 1920 µm (miniasic area of 90nm TSMC process). Prototype is I/O limited due to various test structures and there is some empty space due to this reason. In fact a lot of the outputs are switched in between different blocks. This set up is enough to measure the key parameters of charge handling capacity, quantization noise and power consumption of different blocks, gives empirical support to the thesis as well as showing the practicality of the proposed idea.

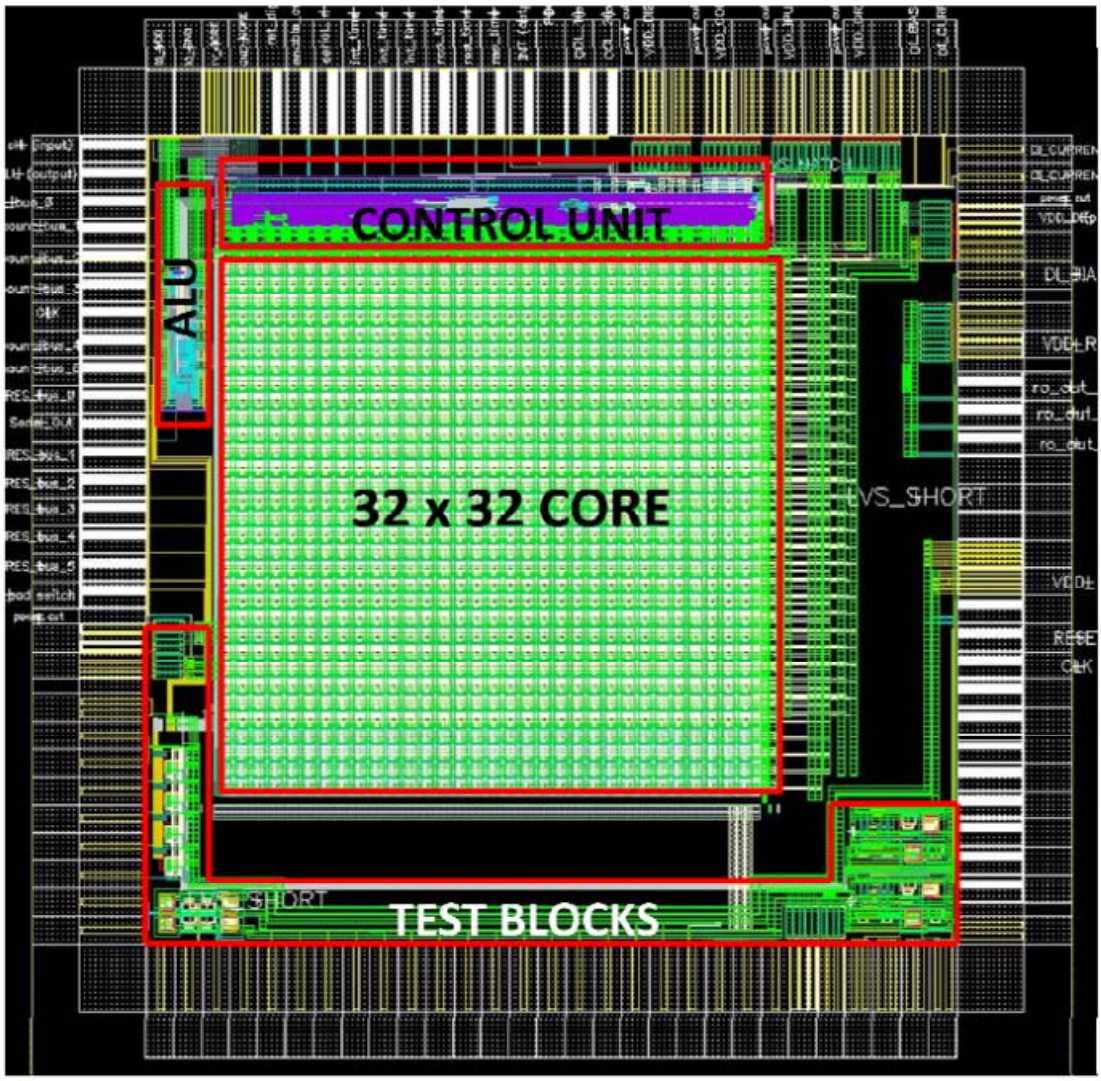

Figure 42 Layout of the complete prototype including the test circuits, 1920 µm x 1920 µm

3.6 Simulation Results

Verification of the prototype has been done on different levels of simulation. First each sub-block of pixel is verified and then pixel level simulations carried out. At the highest level, whole array is to be simulated. However with each pixel containing 650 elements, 32x32 prototype contains more than 665,000 devices. Considering the clocked operation of the array, simulation time of the array increases to extremely long values. In order to overcome this difficulty, arrays are laid out, but simulated with a few pixels.

As mentioned in the previous sections, only available models for the standard cells are verilog models and a mixed mode simulation approach is hence mandatory. Control circuit and ALU were simulated through Spectre-Verilog on RTL level, while conservative settings for high accuracy are used for front-end circuits.

In the following scenarios, various parameters are varied such as control voltage, input current and integration time. The essence of these simulations is to represent the effectiveness of the method in various scenes and frame rate scenarios by achieving a very low quantization noise. Control voltage sets the input current and is used to mimic flux level whereas integration time is varied in order to mimic different frame rates. Mean operation frequency of the counter and residue time values are reported as well in order for completeness. However the outputs of these simulations are the count values: primary count at the output and the actual scaled count value that is evaluated by the ALU.

3.6.1 Case I – Very Low Amount of Incoming Flux

In the first simulation case integration time is set to 72 cycles. The master clock period is set to 4 nsec, this sets the control unit clock, as well as the residue clock period to 104 nsec. Total integration time in this case is 7.5 μsec. Current source bias is set to 900 mV, with an input current of 1.07 nA. With the given integration time, this results a total count of only 1. The residue time is measured to be 31 cycles. This means the integration capacitor voltage crosses the comparator threshold twice, in total. ALU calculates the result for the output value of this pixel is 1.3750 as opposed to the ideal 1.3846. The decimal part here represents the fine quantization done by the method without which the output would be 1.

ALU operation is simple arithmetic. It receives the Integration time from the control unit in binary as 0000 0000 0000 0100 1000 (72). It then adds the residue time to this value; 00 0000

0001 1111 (31), to find the accurate integration time specific to this pixel as 0000 0000 0000 0110 0111 (103). The count for this pixel was already measured to be 0000 0000 0000 0001 (1). Well the whole array is scaled to the integration time. Hence an arithmetic operation of;

$$\frac{(Integration\ Time) \times (Count+1)}{(Integration\ time+1+Residue\ Time)} = \frac{72\times2}{104} = 1.3846 \quad (3.1)$$

results in the actual count for this pixel. The operation is done in digital domain with binary representation of 22 bit depth, the result is 0000 0000 0000 0001. 011000 (1.3750)

Table 7 Simulation results for case I

	Decimal Value	**Binary Value**
Current Control Voltage	900 mV	-
Input Current	1.07 nA	-
Mean operation frequency of Counter	189 kHz	-
Integration Time	72 cycles	0000 0000 0000 0100 1000
Residue Time	31 cycles	00 0000 0001 1111
Counter Value (primary count)	1	0000 0000 0000 0001
Count Value at the Output	1.375	**0000 0000 0000 0001. 011000**

Figure 43 represents the signal timings for count, data write and residue count operations for Case I. At the beginning of the frame, counter is reset by setting high to the counter reset signal. Integration capacitor is reset at the beginning of the frame as well. The separation between the first two reset signals is the integration time. The time difference between the second and third reset operations is the residue time. As seen from the Figure, there is only one resetting operation and counter counts to 1 at time 10.25 µsec, during the whole integration time.

Just before the counter is reset a second time, DW signal gets high and writes the counter data to the in pixel memory. Counter is reset again at time 12.25 µsec, and starts to count for the residue time in cycles. As seen, between 12.25 µsec and 15.475 µsec, counter increments by one at every clock cycle, until it crosses the threshold one more time and the counting stops.

Counter value at this instance is 31. Just before the reset counter is activated the third time, data write residue signal gets high, and the data at the counter is written to the in-pixel memory. Data read signals are not shown here, but at this point pixel is ready for measuring a new exposure. Whenever the column and row read signals are activated (pixel is selected) the residue time data and count data are passed to the ALU and the output is calculated as in (3.1)

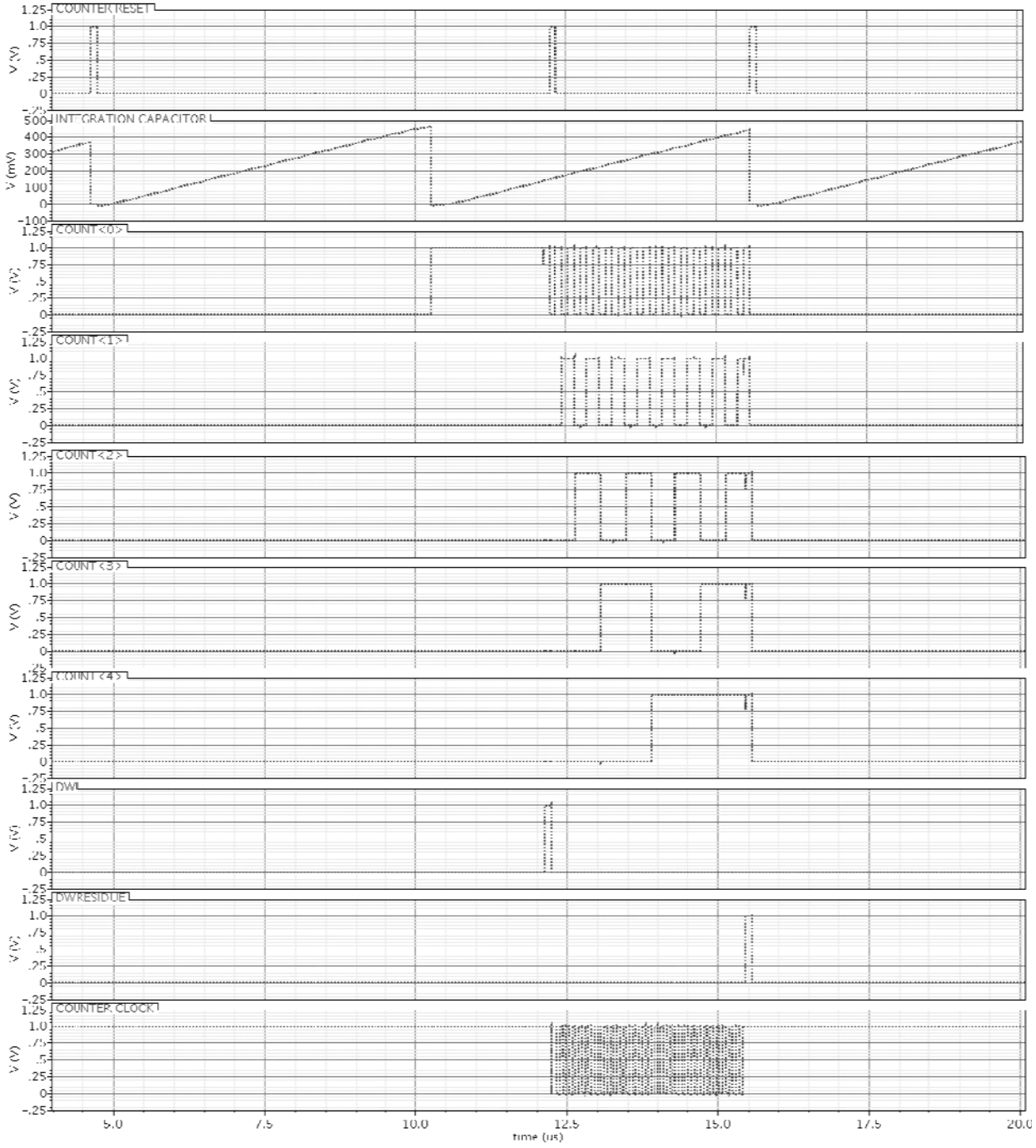

Figure 43 Transient response of the pixel and timing of control signals

3.6.2 Case II – Moderate Amount of Incoming Flux

In the second simulation case integration time is again set to 72 cycles. The master clock period is set to 4 nsec, this sets the control unit clock, as well as the residue clock period to 104 nsec. The total integration time in this case is 7.5 µsec. Current source bias is set to 800 mV, with an input current of 17.3 nA. With the given integration time, this results a total count of 21. The residue time is measured to be 2 cycles. This means the integration capacitor voltage crosses the comparator threshold in 2 additional clock cycles. ALU result for the output value of this pixel is 21.1094 as opposed to the ideal 21.12. The decimal part here represents the fine quantization done by the method without which the output will be 21.

ALU operation is simple arithmetic. It receives the Integration time from the control unit in binary as 0000 0000 0000 0100 1000 (72). It then adds the residue time to this value; 00 0000 0000 0010 (2), to find the accurate integration time specific to this pixel as 0000 0000 0000 0100 1010 (74). The count for this pixel was already measured to be 0000 0000 0001 0101 (21). The whole array is scaled to the integration time. Hence an arithmetic operation of;

$$\frac{(Integration\ Time) \times (Count+1)}{(Integration\ time+1+Residue\ Time)} = \frac{72 \times 22}{75} = 21.12 \tag{3.2}$$

results the actual count for this pixel. The operation is done in digital domain with binary representation of 22 bit depth, the result is 0000 0000 0001 0101. 000111 (21.109375)

Table 8 Simulation results for case II

	Decimal Value	**Binary Value**
Current Control Voltage	800 mV	-
Input Current	17.3 nA	-
Mean operation frequency of Counter	2.87 MHz	-
Integration Time	72 cycles	0000 0000 0000 0100 1000
Residue Time	2 cycles	00 0000 0000 0010
Counter Value (primary count)	21	0000 0000 0001 0101
Count Value at the Output	21.09375	**0000 0000 0001 0101. 000111**

3.6.3 Case III– High Amount of Incoming Flux

For the third case, simulations are done entirely on the Modelsim on RTL level. In this case a very long simulation time is aimed. This would take very long simulation time and very long time to process the output data. Hence the count data and residue time have been set manually. Integration time is set as 131,072 cycle (0010 0000 0000 0000 0000) which is one of the pre-defined (can be set by switches, and requires no programming) integration times of the prototype. With the control unit clock of 104nsec, integration time is 13.631 msec. A current of 1nA on the average will cause a count value of 2478 (0000 1001 1010 1110) for this integration time. For this count values, arbitrarily set residue value is 48. ALU once again follow the formula;

$$\frac{(Integration\ Time) \times (Count+1)}{(Integration\ time+1+Residue\ Time)} = \frac{131072 \times 2479}{131121} = 2478.2437 \qquad (3.3)$$

The finite representation of 22 bits, this value is quantized to 0000 1001 1010 1110. 000100 (2478.23475).

Table 9 Simulation results for case III

	Decimal Value	**Binary Value**
Current Control Voltage	-	-
Input Current	1 nA	-
Mean operation frequency of Counter	177 kHz	-
Integration Time	131,072 cycles	0010 0000 0000 0000 0000
Residue Time	48 cycles	00 0000 0011 0000
Counter Value (primary count)	2478	0000 1001 1010 1110
Count Value at the Output	2478.2437	**0000 1001 1010 1110. 001111**

3.7 Measurements

3.7.1 Measurement Setup

Measurement setup includes various analog biases as well as digital signals such as clock, serial enable, reset, and serial data. Analog power signals are supplied through DC power supplies. Programming signals are supplied from the logic analyzer. Logic analyzer clock is also used for lower clock frequencies such as 100 MHz. After the programming function generator clock is used for high speed operation up to 250MHz clock speeds. Data is obtained from the serial output of the DROIC. Only one output for 32x32 array is available and in order to monitor correct functionality and timing, few column select signals were also supplied as outputs.

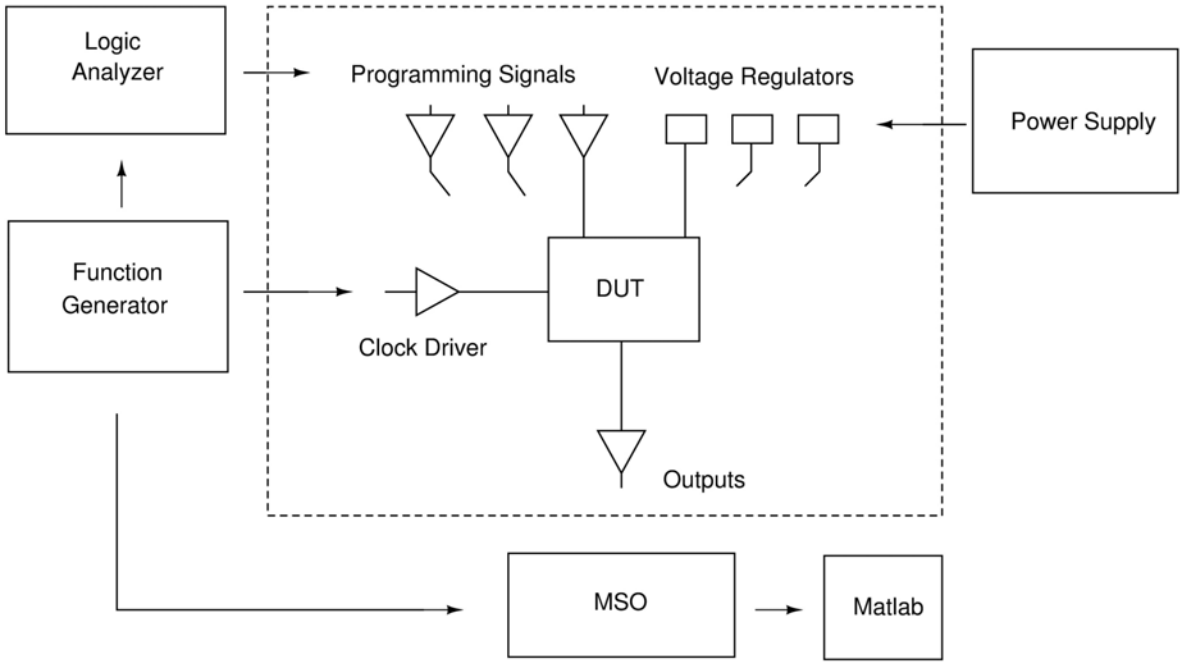

Figure 44 Measurement setup diagram

Data from the serial output is synchronized with the master clock and is read by the mixed signal oscilloscope. Mixed signal oscilloscope (MSO) has data storage capacity and stored data is transferred and processed on MATLAB. For noise measurements multiple capture of the same pixel is essential. For this reason, thirty two frames are stored in the MSO in segmented mode and all frame data is processed on MATLAB for average signal levels and noise. A photo of the measurement set-up is shown in Figure 45.

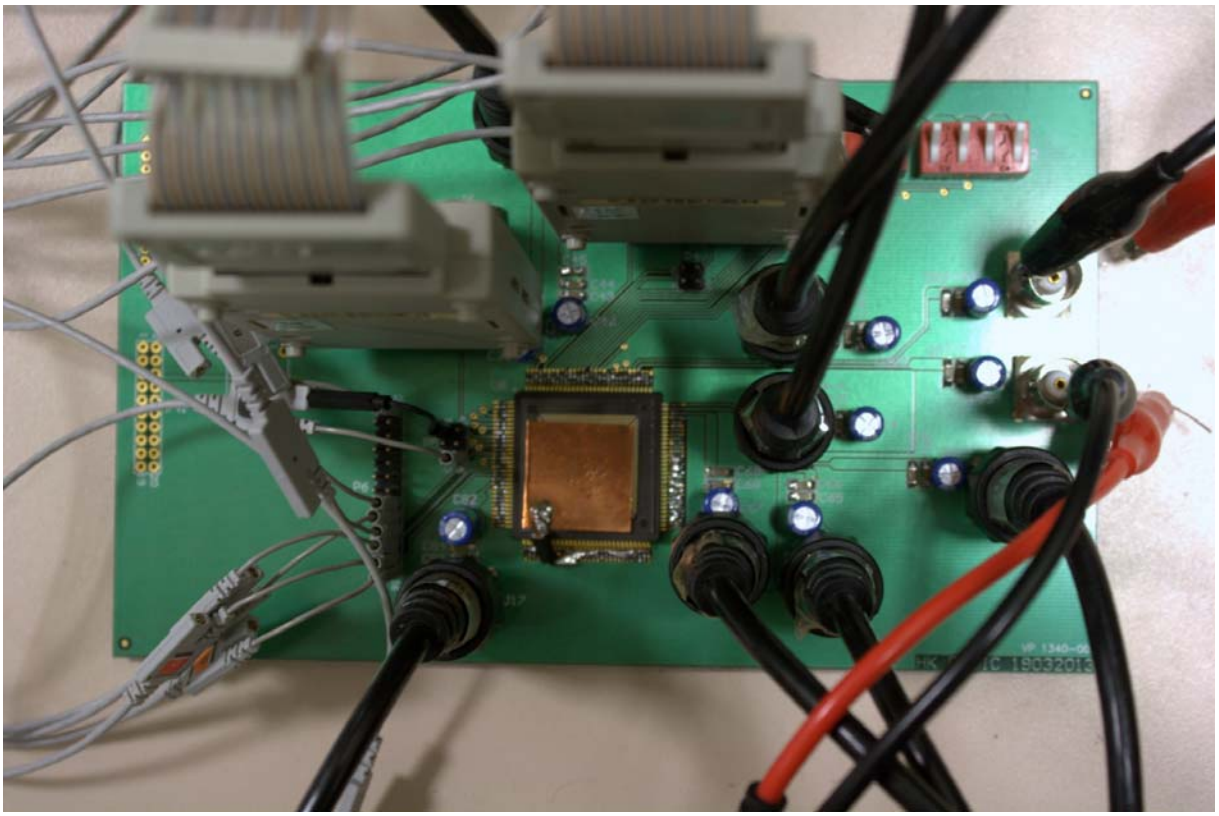

Figure 45 Photo of the measurement set up

3.7.2 Measurement Methodology and Results

3.7.2.1 Quantization Noise (QN)

Quantization noise lower than 200 electrons has been proposed. Using a 557 electrons measurement packet through extended counting method, quantization noise level of 161 electrons has been achieved.

Methodology: Measurements for quantization noise is done with zero input current setting. In this case, during the residue measurement counter operates indefinitely since there is no threshold crossing at the comparator. Using the integration time value and residue time value (2.33) is calculated by ALU for a count of 1. Different integration times with zero current results in correct division showing the minimum step size is 557 electrons. Once the step size is known, quantization noise is also known [69].

Additionally, 6 bits of the residue count have been supplied to output as a test node. Proper scaling of the residue counts have been observed with varying input currents. Figure 46 presents residue time counts with varying input currents.

Figure 46 Residue count vs input current measurement a) Residue count for 8nA (top) b) Residue count for 0.35nA (bottom)

3.7.2.2 Charge Handling Capacity

Charge handling capacity higher than $2.2Ge^-$ has been proposed. Minimum packet size is 557 electrons and data is represented with 22 bits, which results a charge handling capacity of $2.336Ge^-$.

Methodology: Input transistor has been biased with a high overdrive voltage to supply a current of 24nA. This current is integrated for 16ms and output from the serial output pin has been measured to represent 2.336Ge^-.

3.7.2.3 Power consumption

Various power supplies have been used separately so that empirically power levels on each block can be measured. The first supply is the comparator power supply and for nominal current of 20nA, has an average current consumption of 140nA. Reset circuits, memory and counter circuits share a common supply and for the nominal current, has an average consumption of 114nA. This value also includes the residue measurement value. Due residue time is 50µs; residue power is negligible compared to the remaining circuits. Digital control circuit and ALU have a separate supply with 43µA average current. Measurements are done for 400Hz frame rate as opposed to 50Hz and 100Hz state of the art.

As a summary for 400 Hz frame rate, single pixel dissipates a power of 276nW. When compared to state of the art, [40], 3x lower power consumption has been measured. Total power consumption is projected to be 22.21mW for 256x256 array.

Methodology: Small resistors of values 20Ω and 200Ω are used over the supply voltages and measured the voltage drop so as to measure the average power consumption. Results are in agreement with the simulations.

Table 10 Power consumption of the array and projected values for 256x256 arrays

Block	**Average Current (nA)**	**Supply Voltage (V)**	**32x32 Power (uW)**	**Projected 256x256 Power (mW)**
Comparator	140n	1	143.4	9.18
Reset circ., memory, counters	114n	1.2	140	8.96
Control circ., ALU, drivers	43u	1.2	51.6	3.3
I/O pads	100u	2.5	250	0.25
I/O pads	400u	1.2	480	0.48
I/O pads	41u	1	41	0.04
		TOTAL	**1.106mW**	**22.21mW**

3.7.2.4 Temporal Noise

Switching noise is the bottleneck and the dominant noise source. Similar issues have been reported by SOFRADIR's work with lower impact [41]. In SOFRADIR's work a 20% increase in noise has been reported in IWR mode than ITR.

Noise is measured per switching event. The lowest noise per switching event has been measured to be 560 electrons. This is still higher than the shot noise limit which is 189 electrons per switching. Additionally 380 electrons of noise are due to the biasing transistor and in an actual implementation with photodiodes, will be reduced due to the higher dynamic resistance of the detectors. Noise is paramount in imaging systems and is to be reduced in following tape-outs. A sample measured noise table is represented in Table 11. Noise is represented in number of electrons with respect to varying input currents and integration times. As seen from the table, noise per switching event is increased with increased integration times or with increased current values. This is due to the increased switching activity during data transfer.

Table 11 Noise in electrons per switching event

Integration Time (ms)	**Test Transistor Bias-V (Input Current)**				
	0.9 (60nA)	**0.95 (24.7nA)**	**1.00 (7.88nA)**	**1.05 (1.77nA)**	**1.10 (0.35nA)**
0.8	1485	1130	560	617	1095
3.2	2270	1509	1036	904	764
12.8	--	2328	1646	1344	635

Table 12 Output count

Integration Time (ms)	**Test Transistor Bias-V (Input Current)**				
	0.9 (60nA)	**0.95 (24.7nA)**	**1.00 (7.88nA)**	**1.05 (1.77nA)**	**1.10 (0.35nA)**
0.8	8262	3341	1023	247	51
3.2	33.901	13894	4426	991	197
12.8	--	55868	16960	4605	799

Table 13 Stored electrons (x1000)

Integration Time (ms)	Test Transistor Bias-V (Input Current)				
	0.9 (60nA)	**0.95 (24.7nA)**	**1.00 (7.88nA)**	**1.05 (1.77nA)**	**1.10 (0.35nA)**
0.8	297,710	120,400	36,850	8,916	1,844
3.2	1,221,500	500,630	159,470	35,699	7,098
12.8	--	2,013,000	611,110	165,920	28,805

Table 14 SNR (dB)

Integration Time (ms)	Test Transistor Bias-V (Input Current)				
	0.9 (60nA)	**0.95 (24.7nA)**	**1.00 (7.88nA)**	**1.05 (1.77nA)**	**1.10 (0.35nA)**
0.8	66.87	65.3	66.2	59.2	47.2
3.2	69.2	68.9	67.27	62	56.4
12.8	--	71.25	69.09	65.18	64.1

Additionally, Table 12, Table 13, Table 14 shows the output count at different input currents, stored charges and SNR respectively. It is observed that SNR is increased with increased input current and increased integration times. Highest SNR at 50Hz is 71.25 dB, while measured highest SNR at 400Hz operation is measured to be 71dB.

Methodology: Multiple measurements have been done, through the oscilloscopes segmented mode. In this mode data of 32 frames have been taken and their standard deviation has been calculated using MATLAB. Corrections for the 1/f noise of the supply voltages have been implemented when an offset change behavior was observed between the frames. The procedure does not apply to 1/f noise of the pixels, hence keeping the measured data valid. From the table it is seen that increasing the integration time leads to higher noise values at every bias but low currents. This behavior can be either due to 1/f noise or increased switching activity. This amount of 1/f noise is not observed through the simulations. Hence it is thought it could be due to the switching noise. In order to verify this, keeping the integration time low, 1ms, and the residue time high, 16ms, additional measurements have been done with the resulting 1/f noise spectrum being the same, but the digital activity being lower. This leads to significantly lower noise in any of the above cases. This concludes that increased noise is due to the switching activity.

3.7.2.5 Programming and Operation Frequency

Serial programming has been implemented in order to reduce the I/O amount which is important to reduce the heat transfer between the dewar and periphery in cooled IR systems. Programming can be done up to 250 MHz through serial data and serial enable pins. Additionally a built in parallel test has been implemented with pre-defined integration and residue times. Both the programming and parallel modes with 250MHz clock speed have been verified during the measurements.

Methodology: The DUT has been programmed through the serial, control port using the logic analyzer for lower clock speeds as well as the main clock. For higher clock speeds function generator clock has been used. Additionally during the experiments, slightly lower noise has been observed when the function generator clock was used to operate the DUT.

4. POWER DISSIPATION

This chapter covers the power analysis of each sub circuit with corner analyses. Additionally, DROICs utilizing the extended counting method can be used for low power operation when a moderate quantization noise is acceptable. This possibility to achieve low power operation with the proposed DROICs is discussed. Finally, a comparison with the state of the art in terms of power dissipation is also given.

4.1 Power Dissipation Simulations

4.1.1 Comparator Power Consumption

At low or moderate input currents, the major power consumer is the comparator circuit, even if it is a simple inverter. This is due to the input being a slow ramp; inverter is simply operating in a mode where both devices are on and conducting current, which results significant power dissipation. Power consumed is also a function of the input current, since input current determines the frequency of resetting, hence the dynamic power consumption. Analysis is held on three different current values of 1nA, 10nA and 100nA pixel currents at three different corners, results of which are represented in Table 15.

Table 15 Comparator power consumption with respect to process corners.

Detector Current	**Power (nW)**		
	Fast Corner	**Typical Corner**	**Slow Corner**
1nA	159	94	57
10nA	168	**101**	65
100nA	238	164	121

It is assumed that the nominal power consumption is at 10nA, and nominal power consumption of the comparator is 101nW per pixel. Lower power consumption can be achieved with a cost of reduced linearity or higher noise. If the sizes of the transistors at the input stage of the comparator are reduced, a lower static leakage current is achieved. However this also slows down the resetting operation and as seen from (3.3), this introduces non-

linearity. Additionally, supply voltages can be reduced down to 0.8V and inverter based comparators can still operate. However as described in (2.25), this increases the temporal noise. Due to these reasons, relatively large transistors at the comparator input are preferred. The operation voltage is kept at 1.0V as well.

4.1.2 Reset Circuit Power Consumption

Reset circuit power is also scaled with respect to varying input currents. Reset circuits are 'true' inverters. Following the comparator stage, slow ramp behavior of the pulse disappears. Hence reset circuit power consumption is mostly dynamic and is scaled proportional to the frequency. The frequency is linearly dependent to the input current and this behavior can be seen from the power consumption results of Table 16.

Table 16 Reset circuit power consumption with respect to process corners

Detector Current	**Power (nW)**		
	Fast Corner	**Typical Corner**	**Slow Corner**
1nA	14.4	9.6	6.84
10nA	66	**45.6**	33.6
100nA	430	330	256

It is assumed that the nominal power consumption is at 10nA, and nominal power consumption is 45.6nW per pixel.

4.1.3 Counter Circuit Power Consumption

Counter circuit power consumption is, similar to reset circuit power consumption, and is mostly dynamic. Again the operation frequency is linearly dependent to the input current. Hence the dynamic power is linearly dependent to the input current as well. This behavior can be seen from the power consumption results of Table 17.

Table 17 Counter circuit power consumption with respect to process corners.

Detector Current	Power (nW)		
	Fast Corner	**Typical Corner**	**Slow Corner**
1nA	38.4	21.6	18
10nA	67.2	**45.6**	38.4
100nA	342	264	224.4

It is assumed that the nominal power consumption is at 10nA, and is 45.6nW per pixel.

4.1.4 Memory Circuit Power Consumption

Memory circuits have static leakage current and accordingly static power consumption and also dynamic power consumption for read and write operations. The static power is independent of the input current and is 4nW at typical process corner, 7.5nW at fast process corner and 2.9nW at slow process corner.

The dynamic power consumption of the memory circuits are negligible due single read operation energy being 9.3fJ/bit and write operation power being 7fJ/bit.

4.1.5 Residue Measurement Power Consumption

During the residue measurement, counter is clocked at every cycle (until a threshold crossing is achieved) and power consumption of the counter supply may increase dramatically. Transient simulation result of counter supply is shown in Figure 47. Between 6.0 µs and 6.5 µs residue measurement takes place and the current spikes are occurring at a very high rate. During this period average current is 1.23 µA. A 1024x1024 array would have a power consumption of 1.289 W, luckily, this high activity is observed only a very short fraction of the frame time. For example, for a 50 Hz operation and 100 µsec residue measurement, average power consumption for residue measurement drops down to 6.5mW, due the residue measurement takes place only by $1/200^{th}$ of the whole frame time. Additionally, this power consumption is a worst case estimate for the whole FPA being illuminated with extremely low irradiance levels, resulting in the counter to be active for the whole residue time.

It is also important to report power consumption for a 256x256 array. 1.23 µA average current during residue measurement is equivalent to 6.15 nA average current consumption per pixel for 50Hz operation. This is negligible when compared to power dissipations of different blocks of Table 18.

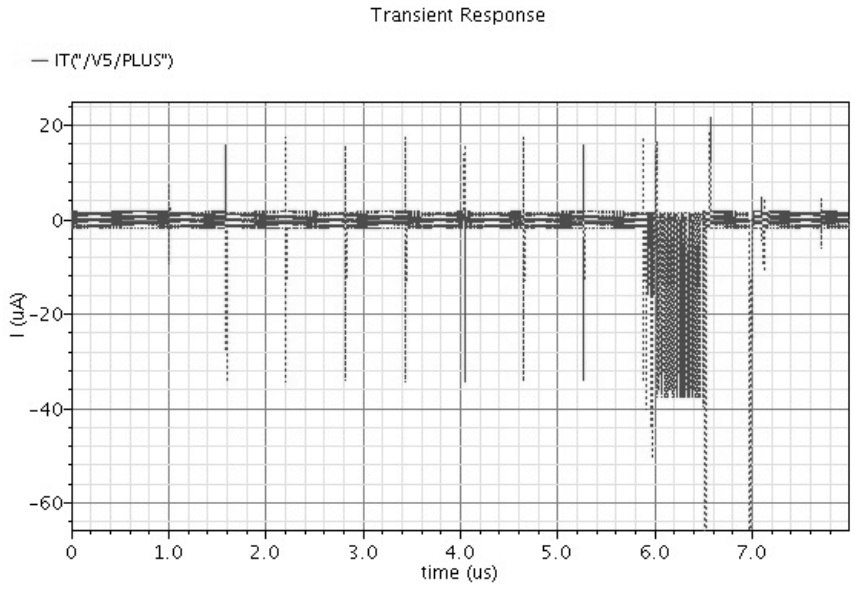

Figure 47 Transient response of the current for the counter.

4.1.6 Total Power Consumption

In order to make the evaluation of total power easily, power consumption of all blocks with three different process corners and input currents are given at this section in tabular form. Dominant power consumer is the comparator at the front-end at low-medium current levels. Hence its design for linearity, noise, circuit area power consumption has critical importance. It is also important to note that total power consumption increases with increased input currents. For nominal current of 10nA (which is still a high current value even for the LWIR detectors) a 256x256 array core consumes 12.84mW of power. If array size is increased to 1024x1024 power consumption increases to 205.52mW, which is a low value compared to analog ROICs, while having the advantages of PFM DROICs.

Table 18 Total power consumption for a single pixel of 1nA with respect to process corners.

	Power (nW)		
	Fast Corner	**Typical**	**Slow Corner**
Comparator	159	94	57
Reset Circ.	14.4	9.6	6.84
Counter	38.4	21.6	18
Memory	7.5	4	2.9
TOTAL	219.3	**129.2**	87.74

Total power consumption of a 256x256 array is 8.46mW and for an1024x1024 array it is 135.47mW

Table 19 Total power consumption for a single pixel of 10nA with respect to process corners.

	Power (nW)		
	Fast Corner	**Typical**	**Slow Corner**
Comparator	168	101	65
Reset Circ.	66	45.6	33.6
Counter	67.2	45.6	38.4
Memory	7.5	4	2.9
TOTAL	308.7	**196.2**	139.9

Total power consumption of a 256x256 array is 12.84mW and for an1024x1024 array it is 205.52mW

Table 20 Total power consumption for a single pixel of 100nA with respect to process corners.

	Power (nW)		
	Fast Corner	**Typical**	**Slow Corner**
Comparator	238	164	121
Reset Circ.	430	330	256
Counter	342	264	224.4
Memory	7.5	4	2.9
TOTAL	1017.5	**762**	602.3

Total power consumption of a 256x256 array is 49.93mW and for an1024x1024 array it is 799mW

4.2 A closer look to SNR

It is beneficial to restate the white noise behavior of the proposed DROIC is important as it reveals one unanticipated property: kTC noise contribution to SNR is dependent on the reset voltage level, V_{mr} rather than the integration capacitance. White noise of a single pixel at single count is:

$$n_{e-T} = \sqrt{\frac{C_{int}V_{mr}}{q} + \frac{kTC_{int}}{q^2} + \frac{e^2_{pa-white}\tau}{2q^2{R_d}^2} + \frac{8kTC_{int}{}^2}{3q^2 g_m \tau}} \tag{4.1}$$

where $V_{mr} = V_m - V_{reset}$, $e_{pa-white}$ is the white noise component of the preamplifier noise, R_d is the dynamic impedance of the detector, τ is the average time per count, g_m is the transconductance of the comparator, k is Boltzmann's constant, and T is the temperature. The four terms correspond to the shot noise, reset (kT/C) noise, preamplifier noise, and comparator noise. This is the number of noise electrons in one count. In N counts SNR can be written as:

$$n_{e-E-N} = n_{e-T}\sqrt{N} \tag{4.2}$$

$$SNR = \frac{{NC_{int}V_{mr}}/{q}}{\sqrt{N\left(\frac{C_{int}V_{mr}}{q} + \frac{kTC_{int}}{q^2} + \frac{e^2_{pa-white}\tau}{2q^2{R_d}^2} + \frac{8kTC_{int}{}^2}{3q^2 g_m \tau}\right)}} \tag{4.3}$$

$$N = \frac{T_{int} I_{ph}}{C_{int} V_{mr}} \tag{4.4}$$

$$\tau = \frac{C_{int} V_{mr}}{I_{ph}} \tag{4.5}$$

$$SNR = \frac{\sqrt{T_{int} I_{ph}}}{\sqrt{q + \frac{kT}{V_{mr}} + \frac{e^2_{pa-white}}{R_d{}^2} \frac{1}{2I_{ph}} + \frac{8kT}{3 g_m V_{mr}{}^2} I_{ph}}} \tag{4.6}$$

which is in agreement with SNR result achieved in (2.25) but is represented with different metrics.

Well, quite interestingly, SNR is not affected by the change of the integration capacitance, contrary to the analog readouts. The kTC component of the noise is a parameter of V_{mr}. If we look at the analytics, $q = 1.6 \times 10^{-19}$,

$$\frac{kT}{V_{mr}} = \frac{0.0414 \times 10^{-19}}{V_{mr}} \tag{4.7}$$

If kTC noise is to be an order of magnitude lower than shot noise (desired dominant noise) than V_{mr} should be set around 250mV. Assuming an input stray capacitance of the comparator to be 1.5fF (no additional integration capacitor), with 250mV V_{mr}, measured packet size is 2343 electrons, and has a quantization noise of 676 electrons.

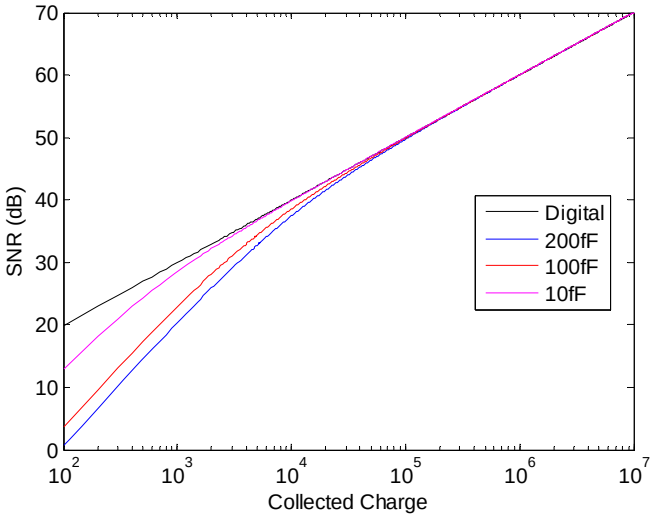

Figure 48 SNR plot with respect to collected charges for different integration capacitors

In the proposed method, without reducing V_{mr}, low quantization levels of 200 electrons can be achieved. Figure 48 represents SNR plots with varying integration capacitances under the assumption of the noises sources are the kTC noise and the shot noise. Figure 48 shows the

well known behavior of better SNR with reduced capacitance size for analog readouts, while showing the indifference for PFM DROICs.

SNR is not mentioned here to show the effectiveness of the method for low noise operation. Rather it is shown, because it gives a flexibility to circuit designer to change integration capacitor values without effecting SNR. Since noise is independent to the integration capacitance, low power operation can be achieved with the use of larger integration capacitances.

4.3 Low Power Operation

Since the capacitance is not playing a critical role on kTC noise performance, how should one decide on appropriate capacitor sizes? The answer to this question lies along the power consumption. Qualitatively, for a given photon irradiance, a small capacitance will fill up quickly and a lot of resetting event together with a high frequency counting operation will take place. On the other hand a large capacitance will fill up very slowly and few resetting events followed by a low frequency counting operation will take place. In order to reduce the dynamic power, choosing the largest capacitance that would fit in the pixel area will be the wise choice.

In order to understand this quantitatively results from section 3.4 is re-organized in Table 21. It is seen that power consumption of a single pixel increases as the input current increases. This is mainly due to the increased digital activity. It is possible to use a higher integration capacitance to achieve the same charge handling capacity with reduced digital activity and moderate quantization noise. In a sense, leaving the very low quantization noise achievement aside low power operation can be achieved. Additionally, varying integration capacitors can be implemented which would allow user to select between two operational modes; low power or low noise.

Table 21 Simulated power dissipation with respect to varying input currents

	Fast Corner	**Typical**	**Slow Corner**
1nA	219.3	**129.2**	87.74
10nA	308.7	**196.2**	139.9
100nA	1017.5	**762**	602.3

As seen from Table 21, as the input current increases from 1nA to 100nA power consumption of a single pixel increases from 129.2nW to 762nW. The behavior of power consumption with respect to input current is also represented graphically in Figure 49. It is important to note that power consumption of all sub-blocks are linearly dependent to the input current, showing the dynamic power consumption behavior of digital circuits. If this circuit uses 100 times larger integration capacitor, then power consumption of a pixel with a detector current of 100nA will dissipate a power of 196.2nW instead of 762nW. A significant improvement of 2.8 times is observed.

In order to show the practicality of this scenario, Lincoln Laboratories' DROIC [43] is used as an example. In this array, a 15 bit representation is used with an integration capacitance off 1.38fF and voltage swing of 0.565V. This makes a packet size of 4873 electrons. If the capacitance is increased by 64 times, then, counter can count 6 bits less to count for the same charge amount. Required input capacitance for same charge handling capacity would be 88.32fF. Let's assume a 12 bit residue counter with an objective to detect 0.1nA with the previous design specifications, i.e. quantization step of 5000 electrons. For this to hold, during the residue time, we have to make sure a pixel with a current of 0.1nA will cross the comparator threshold level. Hence;

$$88.32f \times 0.565 = 0.1n \times ResidueTime \tag{4.8}$$

This corresponds to a residue time of 500 μsec, for a 12 bit counter, this would require a clock period of;

$$T_{Residue} = 122nsec \tag{4.9}$$

Finally, 12 bit residue time value will be received by the ALU together with the 9 bit count data. ALU will then output 15 bit value scaled to the integration time as in (3.1). A DROIC with the same charge handling capacity and quantization noise can be implemented using the proposed method which will have significantly reduced power consumption.

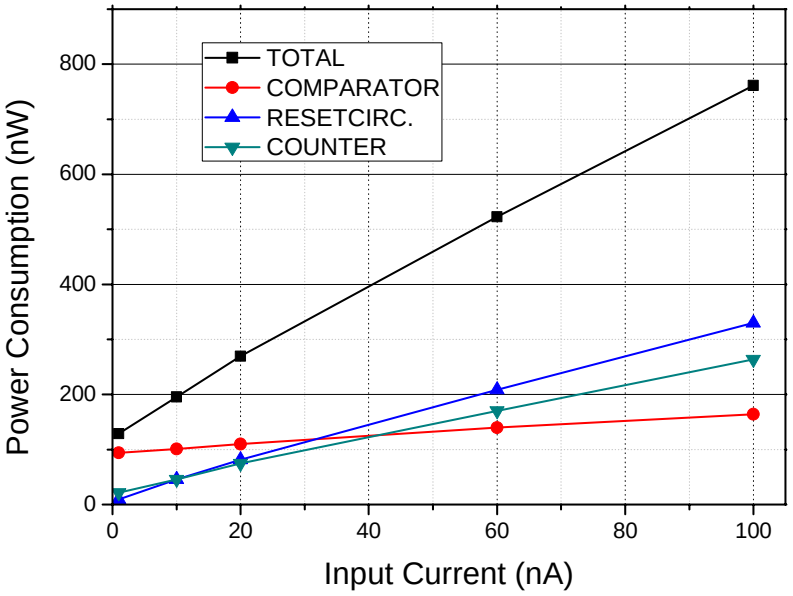

Figure 49 Power consumption with respect to varying input currents

It follows that, for the same quantization noise level, one can use a 12 bit counter and 88.32fF, all being practical, together with the proposed method to achieve lower power consumption. As seen from Figure 49 using an integration capacitance of 8x will reduce the power consumption from 640nW per pixel to 196.2nW while changing the operation from 80nA to 10nA respectively. This corresponds to a power saving of 200%, 29mW for a 256x256 array, and 465mW for 1024x1024 array. It is seen that, for wide dynamic range imaging, only power efficient way is to use a large integration capacitor and then reducing the quantization noise by residue measurement as shown in this work.

It is also important to mention that the new pixel that operates at low power mode can easily fit to the 30µm x 30µm pixel area. This design includes a 12 bit counter and 21 bit memory freeing a space of 162µm^2 for the additional capacitance of 56fF. Only 50µm^2 additional area is required thanks to very dense mim capacitors of the process. Hence even higher charge handling capacity or lower quantization noise is still achievable.

At system level, the novel architecture, proposes an adoptable solution to the implementation of DROICs. Users can select between different modes of operation: low quantization noise or low power. Additionally user can easily select a fixed amount of bits in favor of the most significant bits or least significant bits. For example, in a high flux scene with low contrast

between different objects of the observed scene, higher 16 bit can be used since quantization noise is insignificant for high flux operation.

4.4 Comparison of designed DROIC with the state of the art in terms of power dissipation

Although the proposed DROIC is of 32x32 array format, power consumption for a 256x256 array has been projected to be 22.21mW as shown in Table 10. The projection has been made under the assumption that the measured digital control circuit and ALU power consumption increases linearly with the array size. This is actually an overestimate since the static power dissipation will not increase linearly with the array size, in terms of control circuits. However, since the array is not in actual 256x256 size, an overestimate is a fair penalty. Additionally, during the design, all line capacitances are assumed for 256x256 array size, so that there is actually no change required on the pixel design for driving the load of a larger array. Therefore no additional assumptions are made on the pixel circuit. Measured pixel power is scaled with respect to array size linearly. Finally it is already shown in Table 21 that power dissipation varies with varying input currents. 22.21mW power consumption has been calculated for input current of 20nA. For reference, SOFRADIR's work in 2011 has been designed for an MCT array with currents 8nA- 24nA range [40]. It will be shown that proposed architecture can have significantly lower power dissipation even with high input current of 20nA.

4.4.1 Figure of merit for power dissipation for ADCs

Before comparing the proposed DROIC with other DROICs with DPS arrays it is important to clarify a figure of merit for power comparison. It is hard to compare various ROICs due to different array sizes, accuracies, and frame rates. A figure of merit named power effectiveness is a good method that gives insight for power consumption accuracy and speed parameters at once. FoM_{PE} is the figure of merit that is used to assess how much power is needed to complete the task of sampling at a particular resolution [57] and usually is given in joule per least significant bit (J/LSB).

$$FoM_{PE} = \frac{P_{TOT}}{2 * f_{BW} * 2^{ENOB}} = \frac{P_{TOT}}{f_s * 2^{ENOB}} \tag{4.10}$$

where P_{TOT} is the total power dissipation, f_{BW} is the circuit bandwidth and f_s is the sample rate for Nyquist ADCs and ENOB is the effective number of bits; binary representation of the SNR of an ADC and is calculated through the SNR by [57]:

$$ENOB_{\sin} = \frac{SNR_{\sin} - 1.76}{6.02} \tag{4.11}$$

SNR of the PFM DROICs are increased with increased charge handling capacity. Therefore for fair comparison with the state of the art, highest measured SNR is used to evaluate the ENOB of various DROICs.

In MIT's Lincoln Labs work in 2009 [43], a DROIC with 50mW power consumption for 100Hz operation and 16 bit resolution have been reported. SNR of this ROIC is around 80dB and ENOB is in this case around 13 bits. Measured power consumption values are reported for 20nA input current. A later work in 2010 from the same group reports a 30mW DROIC with 16 bit resolution [44] while operating at 1-2nA input currents. For comparison power consumption reported in [43], 20nA input current, is used to calculate FoM_{PE}. Following (4.10);

$$FoM_{PE} = \frac{50mW}{256 \times 256 \times 100 \times 2^{13}} = 930\,fJ / LSB \tag{4.12}$$

The second state of the art is SOFRADIR's work with 90dB measured peak SNR [40, 41]. Operation frequency is less than 50 Hz with 17.7nA input current. Power dissipation is 150mW due to the static power consumption of a pixel being around 1μW at 180nm process and 1.8V supply voltage. The resolution of the ADC is 15 bits. With SNR being 90dB, ENOB is found to be 14.6 bits. Following (4.10);

$$FoM_{PE} = \frac{150mW}{320 \times 256 \times 50 \times 2^{14.6}} = 1.47\,pJ / LSB \tag{4.13}$$

The projected power consumption of this work is 22.21mW. Design can operate up to 400Hz frame rate with two output configuration. The peak SNR is 71.5dB. However at reduced integration time of 2.5ms (400Hz frame rate), this value drops to 67dB and ENOB is found to be 10.83. Following (4.10);

$$FoM_{PE} = \frac{22.21mW}{256 \times 256 \times 400 \times 2^{10.83}} = 465\,fJ / LSB \tag{4.13}$$

As seen, this work is in terms of performance, this work is superior, when considering FoM_{PE}. If only frame rates and power consumption values are to be evaluated, this work has higher frame rate and lower power consumption than works of both groups. However a fair comparison can only be made with including accuracy in the analysis. It is also important to note that right now designed prototype is limited with the switching noise. Designed DROIC still maintaining 72dB SNR, will not be shot noise limited when bonded to detector arrays. This will be overcome in the second prototype. If as in the case of SOFRADIR's shot noise limited performance is met, 90dB SNR can be achieved. This would result in an ENOB of 14.6 and FoM_{PE} will drop to 34.1fJ/LSB, a significantly lower value than the state of the art.

Table 22 Comparison of this work with state of the art in terms of FoM_{PE}

	Array Size	**Power (mW)**	**Frame rate (Hz)**	**Resolution (bits)**	**ENOB (bits)**	**FoM_{PE} (fJ/LSB)**
SOFRADIR	320x256	**150**	50Hz	15	14.6	**1470**
MIT Lincoln Labs	256x256	**50**	100Hz	16	13	**930**
This Work	256x256	**19.17**	400Hz	22	10.83	**465**

Finally, all these results are evaluated for a DROIC with very low quantization noise levels. If low power operation discussed in section 4.2 is applied even lower power dissipation levels can be achieved with moderate quantization noise levels. Comparison of measured results of this work with state of the art is given in Table 22.

5. CONCLUSION

Over the last decade, a continuously growing effort has been shown to achieve digital output ROICs. Primary concern is to carry the analog to digital conversion on chip to reduce the overall imaging system size and power by eliminating off-chip ADCs and precise analog buffers and periphery cards. Reducing the system size and weight is a very competitive advantage in today's IR market. However reducing the system size and weight comes with an additional cost of increased on-chip power consumption, even though the total system power is reduced. Increased on-chip power consumption is a very harsh drawback especially for cooled IR systems, since it reduces the lifetime of the dewar, as well as increasing the cool down time and size of dewar. All these are direct impacts for increased system cost and reduced product lifetime. The situation is even worse for higher frame rate applications such as MAW and HFI systems, since these applications require a high speed ADC with higher power dissipation. Hence, a lot of effort has been put on low power ADC architectures to be applied to ROICs.

Aside from the low power ADC efforts, increasing the SNR of IR imaging systems has always been the primary design objective. Today's military IR systems have an unnamed standard of 20mK NETD specification. A lower NETD is always desired, since it results for better image quality and for search and track systems, longer range or higher correct decision probabilities. The limiting factor for NETD is the limited charge handling capacity of ROICs. Photon systems are limited with shot noise of photons themselves. Ideal SNR is the square root of the stored photo generated charges (measured photons). In a limited pixel area, integration capacitor size is limited making it difficult to have NETD values lower than 20mK.

PFM DROICs and ΔΣ DROICs are strong candidates to overcome the current NETD limits. A 2mK DROIC has been shown by the SOFRADIR group in 2010 with PFM architecture following the works of MIT Lincoln labs started in 2005. Dramatic SNR increase is achieved by per pixel PFM ADCs, allowing the charge to be stored in digital memory. Storage capacity increases exponentially with respect to circuit area contrary to linear increase of analog ROICs. More than $3Ge^-$ charge handling capacity has been achieved using PFM DROICs.

The drawback of current state of the art DROICs with per pixel ADCs (DPS arrays) is the high quantization noise. Moderate power consumption for small arrays and high power consumption for large arrays is another drawback that has to be overcome for PFM DROICs to find a decent market share. This thesis has proposed circuit architectures that can overcome these difficulties. The primary objective has been designing circuit architectures that achieve very low quantization noise levels along with practical power dissipation levels and high frame rate operability while maintaining the high charge handling capability of PFM DROICs. Additionally design approaches for low power operability of proposed architectures have been analyzed.

A new pixel design has been proposed for PFM DROIC to reduce the quantization noise without further increasing the power consumption or pixel sizes. The method relies on a coarse quantization on charge domain which is followed by a fine quantization on time domain. Input preamplifier, integration capacitor, comparator and counter blocks of an ordinary PFM circuit is still used in the proposed method. In the first phase circuit operates as an ordinary PFM pixel and measures the stored charge by counting the number of resets. The remaining value, residue, is to be further measured for reduced quantization noise. This measurement is done on time domain in the proposed pixel. Counter is operated as a clocked counter while allowing the integration to continue until a final threshold crossing. Using a high speed clock enables very low quantization noise levels.

The proposed method has been proven with experimental results. A prototype has been designed, manufactured and tested in 32x32 array format. Pixel size has been selected as 30µm x 30µm in order to reduce manufacturing cost of the DROIC, since 90nm process is feasible for this pixel size eliminating the need for a smaller pitch technology such as 65nm or lower. Target quantization noise has been identified as lower than 200 electrons while maintaining a charge handling capacity of more than $2Ge^-$. Although no power specifications has been defined at the beginning a low power dissipation DROIC is aimed. Low quantization noise is especially important for high frame rate applications where the stored charge and shot noise is reduced. A fast frame rate of 400Hz with two output configuration has been aimed.

While operating as ordinary PFM, measured packet size is 35,625 electrons at each count. Following the residue measurement period and ALU operation, measured packet size is further reduced by 64 times to 557 electrons. This results a quantization noise level of 161 electrons. With per pixel counters of 16 bits, charge handling capacity is 2.336G electrons.

Measurement results verify the low quantization noise behavior as well as charge handling capacity.

Total power consumption of the 32x32 prototype is found to be 1.106mW while the whole array is being operated with an input current of 20nA. Power dissipation is a very strong function of the input current, and lower power dissipation is observed at lower input currents. Results for 20nA are reported in order to fairly compare the power consumption of this work with state of the art as the compared works report 20nA and 17nA input currents. Furthermore, power dissipation is projected to be 22.21mW for 256x256 arrays.

The operation frequency of the DROIC for 256x256 array with two outputs, can be as high as 400Hz which is adequate for MAW systems or HFI systems. At 400Hz operation SNR is measured to be 67dB. FoM_{PE} is found to be 465fJ/LSB and is one third of SOFRADIR's DROIC and half of MIT Lincoln Laboratory's DROICs. The power dissipation is significantly lower than both of the state of the art, however SNR being lower, results a reduced advantage in FoM_{PE}. Highest measured SNR is found to be 72dB and DROIC is limited with the switching noise of the digital circuits.

Additionally, for scenarios where low quantization noise requirements are relaxed such as low frame rate imaging or high flux scenarios the proposed architecture can be used with low power dissipation and moderate quantization noise. A larger integration capacitor can be used for measuring a higher charge packet at each reset event. This can significantly reduce the power consumption due reduced digital activity. The residue will be even larger in this case, however using the proposed method; quantization noise can be lowered to a desired value.

It is important to note that this work has been designed for and tested at room temperature. PFM ROICs are especially advantageous for very high SNR for LWIR applications where the sensor chip assembly is operated at a cooler, usually at 77K. Lack of models at 77K let the design to be optimized for room temperatures. However, there is no specific issue on operating CMOS circuits at cryogenic temperatures aside from modeling activities which the foundries usually supply for -40ºC – 80ºC range.

A comparison of this work and the state of the art is given in Table 23 . It is seen that the proposed work is advantageous in terms of quantization noise, FoM_{PE} and frame rate. SNR is theoretically comparable to the compared work, while at this point limited due to high switching noise.

Table 23 Comparison of this work with state of the art

	Array Size	Pixel pitch (µm)	Capacity (Ge^-)	Quantization Noise Floor (e^-)	FoM_{PE} (fJ/LSB)	Frame Rate (Hz)	Number of Bits
SOFRADIR	256x320	25	3	26,000	1470	50	15
MIT	256x256	30	10[1]	2,200[2]	930	100[3]	15
Proposed Method	256x256	30	2.335	161	465	400	22

[1] Physical capacity is lower, achieved by up/down counting [2] 5000 and 700 electrons packet sizes has been reported at later works, results are not discussed, QN values 1443 and 202 electrons respectively [3] 10kHz maximum, results reported at 100Hz.

Low NETD is paramount in IR imaging applications. Hence it is important to reduce the switching noise. Therefore, this design at the physical level will be optimized for reducing the switching noise. Measurements at cryogenic temperatures will be held for optimizing a second design for cryogenic temperatures. There are various test circuits, including transistors that can be used to monitor process parameters at 77K.

Moreover, industry's SWaP trend is being followed strongly. Proposed architecture is a strong candidate for very low power consumption / moderate quantization noise applications. As part of the future works, aside from the cryogenic operation, a very low power PFM DROIC is planned to be manufactured. Combined with the proposed low-power operation scheme and improved SNR, proposed DROICs will have significantly lower FoM_{PE}.

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