National Aeronautics and Space Administration

Printed Wiring Board Technology Infusion and Supplier Capability Overview

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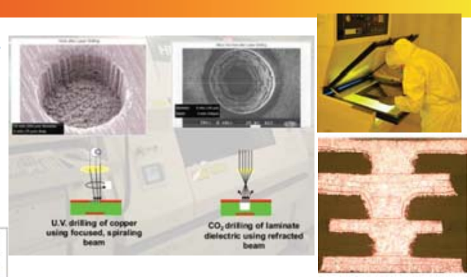
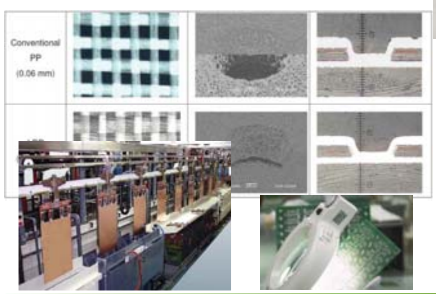
Outline

- Printed circuit board [...]nology
- PCB quality assuran[...]
- Supplier capability s[...]
- New technology inser[...]/TRL
- Risk based methods
- Closure

Introduction

- In today's compressed development cycles where rapid and cost-effective testing and analysis are key, a properly designed and executed quality assurance function (with appropriate reliability analysis) can enable products with robust design margins.



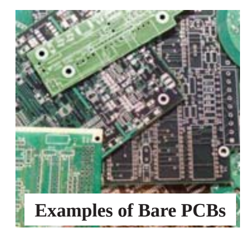


- If the mission conditions are not well understood or the reliability analysis and accelerated testing are not conducted right, cost and schedule impacts, along with unexpected failures will add risk to a Project development cycle.

SOURCE: Industrial Laser Solutions. PCBShop.org

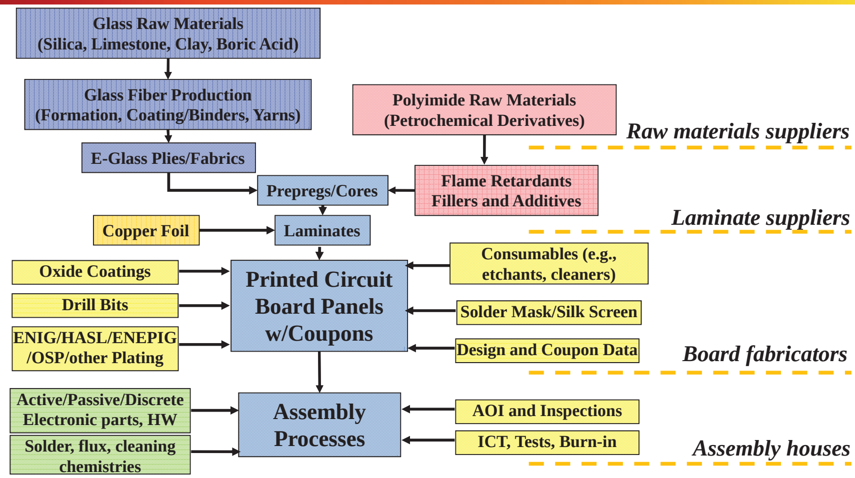
Printed Circuit Boar[...]nd Classification

- Printed circuit boards are the baseline in e[...] packaging – they are the interconnection medium up[...] electronic components are formed into electronic sys[...]
  – PCB materials are generally glass reinf[...]ganic polyimide (epoxy, BT, ceramic are also[...]
- Classified on the basis of
  – Dielectrics used
  – Reinforcement
  – Circuit type
  – Component types
  – Board construction
  – Design complexity


Examples of Bare PCBs


Populated PCBA

Polyimide PCBA Supply Chain*



* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).

Major Constituents of Laminates*

Constituent	Major function (s)	Example material (s)
Reinforcement	Provides mechanical strength and electrical properties	Woven glass (E-grade) fiber
Coupling agent	Bonds inorganic glass with organic resin and transfers stresses across the structure	Organosilanes
Matrix	Acts as a binder and load transferring agent	Polyimide
Curing agent	Enhances linear/cross polymerization in the resin	Dicyandiamide (DICY), Phenol novolac (phenolic)
Flame retardant	Reduces flammability of the laminate	Halogenated (TBBPA), Halogen-free (Phosphorous compounds)
Fillers	Reduces dissipation (high frequency), thermal expansion and cost of the laminate	Silica, Aluminum hydroxide
Accelerators	Increases reaction rate, reduces curing temperature, controls cross-link density	Imidazole, Organophosphine

* - Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).

Example: Glass Fabric Treatment*

Glass Weave Style

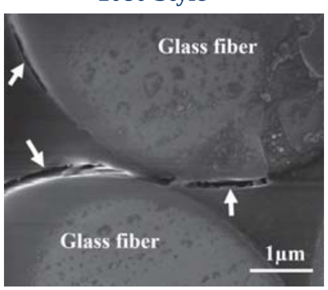
1080 Style

Glass Weave Style

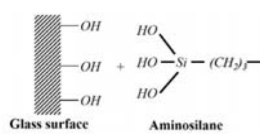
2116 Style

Glass Weave Style

7628 Style



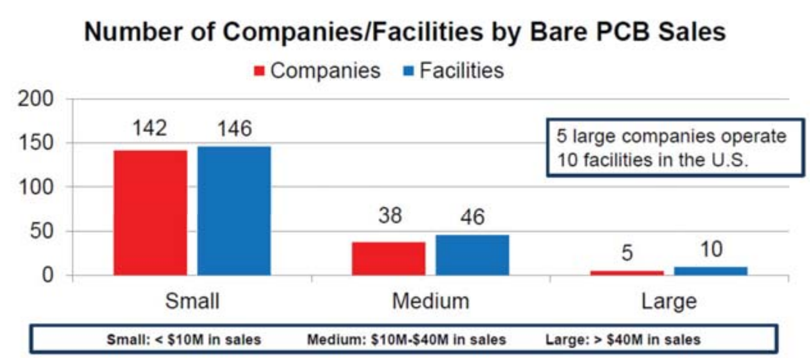
Fiber/resin interphase delamination occurs due poor glass treatment.



* - Sood, Bhanu, and Michael Pecht. "The effect of epoxy/glass interfaces on CAF failures in printed circuit boards." *Microelectronics Reliability* (2017).

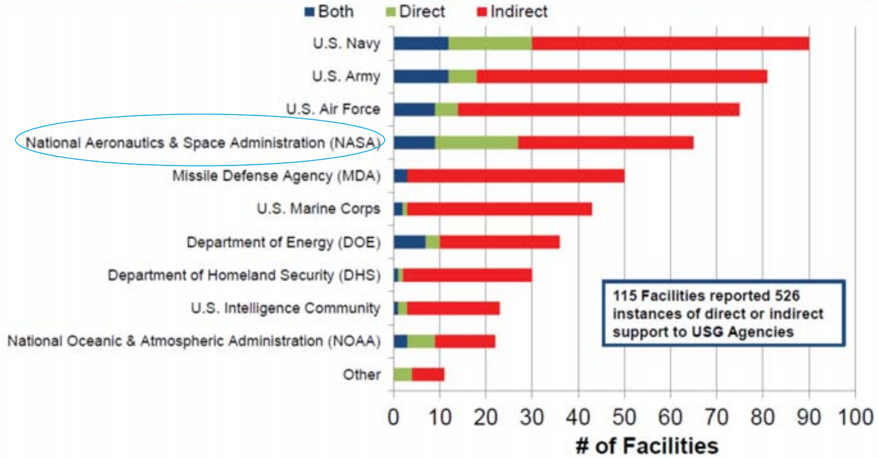
Bare PCB Suppliers*

185 companies operate 202 bare printed circuit board manufacturing facilities in the U.S. - 2015



* - "Challenges and Opportunities: State of the U.S. Bare Printed Circuit Board Industry" Crawford M. and Botwin B., IPC APEX Expo, February 11-16, 2017, San Diego CA. Reproduced with permission.

Support to U.S. Government Agencies*



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Bare PCB Supplier Capabilities*

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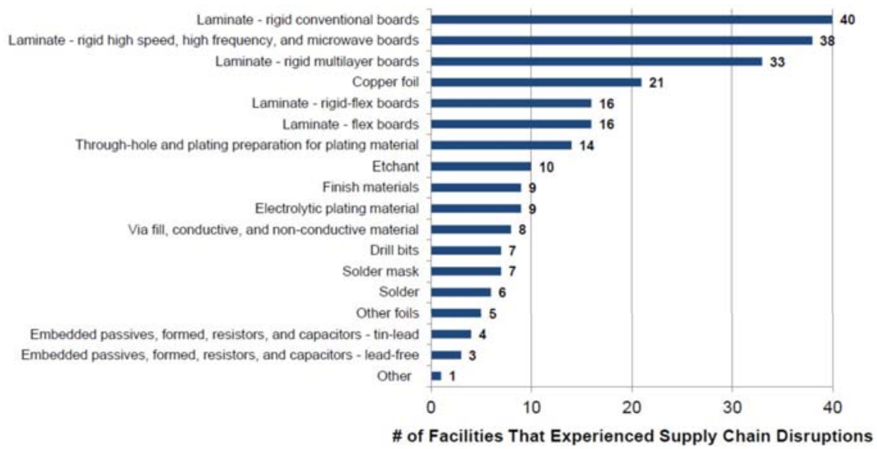
Material Supply Chain Disruptions*



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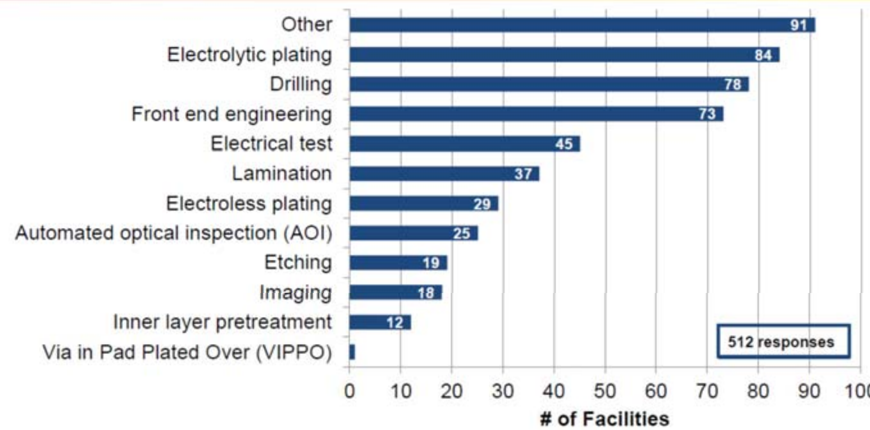
Factors Causing PCB Production Bottlenecks*



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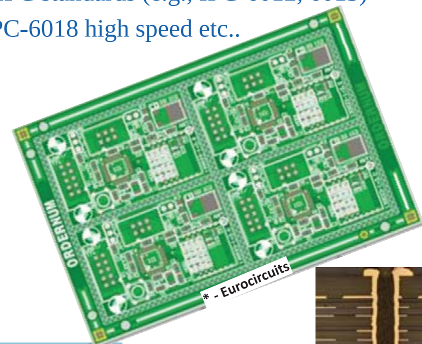
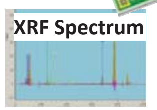
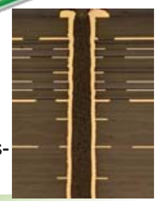
PCB Quality

- In a vast majority of cases, NASA uses IPC standards (e.g., IPC-6012, 6013)
  - IPC-6012 for rigid, IPC-6013 flex, IPC-6018 high speed etc..
- Inspection include:
  - Microsection evaluation (coupons)
  - Surface finish evaluation (coupons)
- Test include:
  - External visual examination
  - Electrical continuity and isolation
  - Solderability (not 100% cases)
  - Cleanliness
- In some cases MIL, ESA or "in-house" standards are applied.





PTH in Cross-section



Significance of Board Requirements

- The requirements and coupons are a "front door".
- Examples:
  - Internal Annular Ring:
    - Egregious violations indicate there may have been a serious problem in development of the board (layup or lamination).
    - Other NCs don't indicate any risk at all (example: application of IPC-6012 Rev B. v/s IPC-6012 Rev. D)
  - Negative etchback v/s positive etchback:
    - Modern cleaning processes and flight experience result in equal reliability with both etchback conditions or no etchback.
  - Wicking of copper:
    - Requirements are conservative based on broad statistics.
    - A basic analysis of the board layout can indicate directly if there is risk or not, regardless of requirements violations.

PCB Supplier Evaluation Study

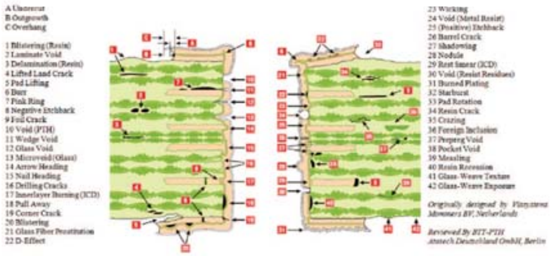
Study Objective

- Evaluate a subset of GSFC PCB suppliers (direct or indirect) and corresponding PCB coupon microsection testing data.
- Develop a methodology for data generation and collection to provide trend analysis
  - Identifies/predicts violation of a process limit criteria (in case of an egregious NC).
- Provide analysis for severity categories of the nonconformance.
- Provide recommendations to the suppliers (i.e. supplier quality engineering, continuous process monitoring, quality metrics definition).

Microsectioning

- Suppliers perform microsectioning and inspect per specifications.
- Secondary GSFC independent microsection analysis yielded 20-30% inspection rejects, caused by:
  - – Screening escapes:
    - Test sample quality not consistent
    - Supplier microsection process, inadequate coupons
  - – Requirement interpretations
  - – Requirements flow-down issues
    - Alternative specifications (MIL, ECSS)
    - Buying heritage and off-the-shelf designs

IPC - PCB Multi-Issue Microsection Wall Poster*



* - https://blog.ipc.org/2010/11/22/pcb-multi-issue-microsection-wall-poster/

Requirements, Nonconformance, Data Generation and Collection

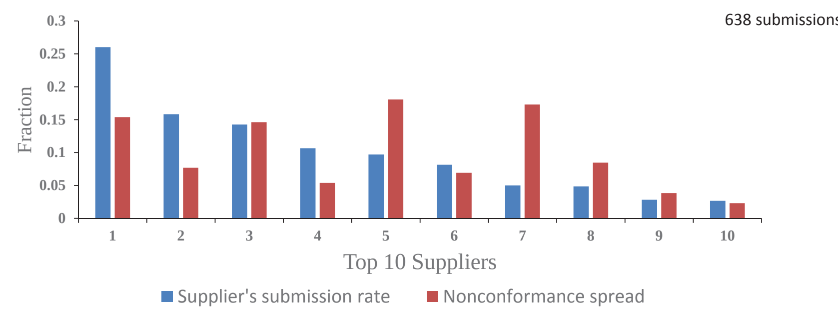
- Present study evaluates only the microsections performed by GSFC.
  - – PCB coupon microsection evaluation in accordance to IPC Standard (IPC-6018B Class 3, IPC-6012C Class 3/A).
  - – Coupon evaluation reports were generated, identified non-conformances.
- All PCB coupon testing results from all GSFC suppliers were recorded for the past 3 years (from 2015 – present)
  - – Data include nonconformance and conformances in accordance with IPC Standards.
  - – Total number of data points are approximately 882 jobs.
  - – Each job has number of nonconformance with different severity.

Study Methodology

- Since 2015, received and analyzed 882 PCB coupon submissions from PCB suppliers.
- Top ten suppliers sent 638 submissions.
- Total nonconformance observed: 260

- For each supplier, analyzed nonconformance (s)
  - – Identify severity trend across top 10 GSFC suppliers by analyzing submission rate and nonconformance spread.
  - – Classifying and analyzing top 5 severity categories.

Data Analysis –Submission and Nonconformance for Supplier



$$\textit{Supplier submission rate} = \frac{\textit{total submission by individual supplier}}{\textit{total submission by all suppliers}}$$

$$\textit{Nonconformance spread} = \frac{\textit{total nonconformance by individual supplier}}{\textit{total nonconformance by all suppliers}}$$

Classification and Analysis - Top 5 Nonconformances

Twenty one distinct conformances observed among the ten suppliers

NC	Nonconformance	Standard
A	Inner layer separations/inclusions	IPC 6012B Class 3/A
B	Electroless Ni less than 118 microinches	IPC 6012B Class 3/A
C	Plating voids	IPC 6012DS
D	Separation/inclusions between plating layers	IPC 6012B Class 3/A
E	Copper wicking in excess of 2.0 mil	IPC 6012B Class 3/A
F	Internal annular ring less than 2.0 mil	IPC 6012B Class 3/A
G	Internal annular ring less than 5.0 mil (drwg. note)	IPC 6012B Class 3/A
H	External annular ring less than 5.0 mil	IPC 6012B Class 3/A
I	Immersion gold less than 3.0 micro inches	IPC 6012DS
J	Electroless nickel and immersion gold plating thickness < 118 micro-inches (Ni) and 2 micro-	IPC 6012B Class 3/A
K	Blind via plating thickness less than 0.8 mil	IPC 6012B Class 3/A
L	Resin recession greather than 3 mil	IPC 6012B Class 3/A
M	Solid copper micro via voids in excess of 33%	8252313C
N	Laminate delamination	IPC 6012B Class 3/A
O	laminate cracks	IPC 6012C Class 3/A
P	Etchback less than 0.2 mil	IPC 6012B Class 3/A
Q	Immersion gold plating thickness in excess of 6 mil	IPC 6012C Class 3/A
R	Copper plating thickness less than 1.0 mil	IPC 6012B Class 3/A
S	Laminate crack greater than 3.0 mil	IPC 6012B Class 3/A
T	Dielectric thickness less than 3.0 mil min	IPC 6012B Class 3/A
U	Laminate void greater than 3.0 mil	IPC 6012B Class 3/A

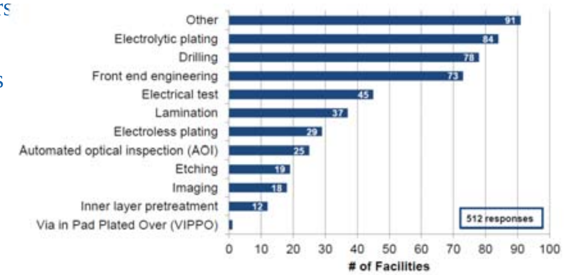
Common Nonconformances from suppliers

← PCB Suppliers →									
1	2	3	4	5	6	7	8	9	10
A	F	E	K	A	N	E	E	A	E
B	G	D	F	F	O	P	A	F	F
C	H	B	L	D	F	C	D	S	T
D	A	I	J	J	E	D	F	D	U
E	D	J	A	M	P	Q	R	P	R

Analyzing Top 5 Severities of Supplier's Nonconformance

- Observations show the nonconformances with the most occurrences (7 out of 10 Suppliers) are D and F.
- Investigated the contributors to implement techniques which may eliminate theses nonconformances from at least 7 suppliers.

(A) Inner layer separations/inclusions
(D) Separation/inclusions between plating layers
(E) Copper wicking in excess of 2.0 mil
(F) Internal annular ring less than 2.0 mil
(J) ENIG is less than the minimum requirements



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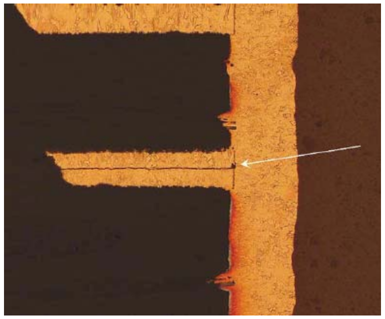
Inner Layer Separations or Inclusions

- Separation of inner-layer foil and the plated through hole barrel.
- Inclusion - contaminant material that is present in an area where it is not expected.

Risk: intermittent electrical open or complete open after board is subjected to thermal excursions (reflow, wave soldering or rework)



1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Swirbel, Tom, Adolph Naujoks, and Mike Watkins. "Electrical design and simulation of high density printed circuit boards." IEEE transactions on advanced packaging 22.3 (1999): 416-423.

Inner Layer Separations or Inclusions

Contributors

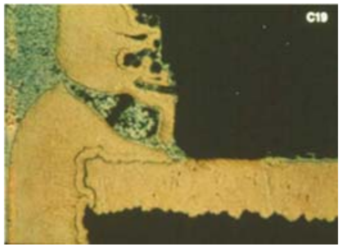
- Improper lamination press or cure cycles whether it be pressure, time, temperature.
- Others include inadequate coverage of inner layer oxide, moisture not completely removed in pre-lamination bake cycle.
- Bad batch of prepreg and or laminate.
- Post-electroless copper cleaning residues, contaminated pretreatment prior to electrolytic plating, or an out-of-control electrolytic copper process.

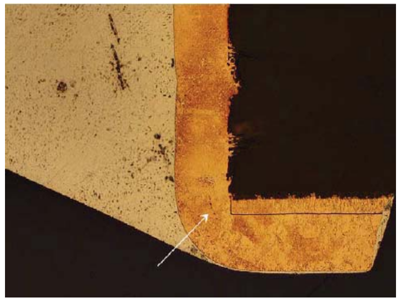
Resolution

- Consistency in drilling processes.
- Reduce the resin content in the stack up.
- Good desmear, with adequate texture.
- Provide adequate copper border for support and resin venting

Separation or Inclusions Between Plating Layers

Plating separation -The separation between a plating layer and foil.





Risk: intermittent electrical open or complete opens due to mechanical or thermal stresses.

1. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.
2. Yung, Edward K., Lubomyr T. Romankiw, and Richard C. Alkire. "Plating of Copper into Through-Holes and Vias." Journal of the Electrochemical Society 136.1 (1989): 206-215.

Separation or Inclusions Between Plating Layers

Contributors

- Incomplete wrap plating
- Overly-aggressive cleaning process
- Insufficient cleaning

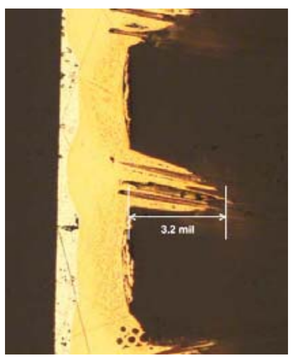
Resolution

- Adjust plating parameters
- Optimize cleaning processes

Copper Wicking in Excess of 2.0 mil

The extension of copper from a PTH along the glass fiber fabric.

Risk: intermittent electrical shorts or complete shorts due to bias driven migration of copper towards non-common conductors.



1. Sood, Bhanu, and Michael Pecht. "Printed Circuit Board Laminates." Wiley Encyclopedia of Composites (2011).
2. Tummala, Rao R., Eugene J. Rymaszewski, and Y. C. Lee. "Microelectronics packaging handbook." (1989): 241-242.
3. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Copper Wicking in Excess of 2.0 mil

Contributors

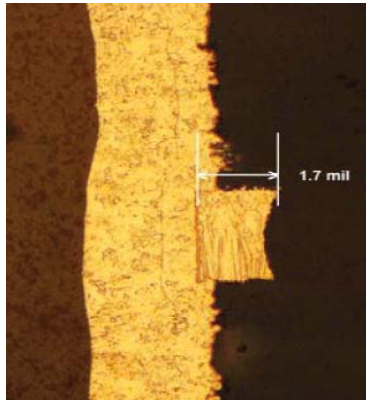
- Dull drill bits or broken drill bits that causes a crack in the laminate.
- Incompatible laminate material
- Insufficient glass etch.
- Poor glass to organic adhesion.

Resolution

- Optimize desmear parameters
- Improve drilling operation (feed and speed).
- Ensure sufficient resin wet-out of glass fibers (siloxane treatment).

Internal Annular Ring Less Than 2.0 mil

This occurs, when the inner layer copper pad (measured from the hole wall plating to its outer most length) is less than 2 mils.



Risk: inner layer breakouts after the board is subjected to thermal excursions (reflow, wave soldering or rework) leading to intermittent electrical or complete open behavior.

1. Sood, Bhanu, and Sindjui, N. "A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards", Proceedings, IPC APEX Expo (2018).
2. IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards.

Internal Annular Ring Less Than 2.0 mil

Contributors

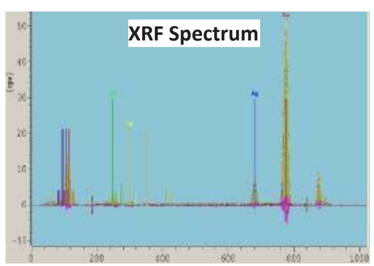
- Drilled-hole pattern not matching the lands on the internal layers (Misregistration).
- Lamination process.
- Prelamination treatments that involve scrubbing or bending may stretch the thin laminate, which will then shrink after it is etched and baked dry.
- Application of specification or drawing notes.

Resolution

- Better material selection of laminate, improved cleanliness, and reduction in the amount of volatiles.
- Confirm whether or not it is operator error.
- Update drawing notes to bring the notes in line with current industry maturity levels.

ENIG (Au or Ni) Less than the Minimum

Electroless nickel and/or immersion gold plating thickness (ENIG) is less than the minimum requirements (118 micro-inches for Ni and 2 micro-inches for Au).



Risk: (1) solderability and, (2) excessive dissolution of copper into the bulk solder (forming brittle intermetallic) when nickel is thin.

1. Johal, Kuldip, and Jerry Brewer. "Are you in control of your electroless nickel/immersion gold process?." Proc. Of IPC Works. No. S03-3. 2000.
2. Meng, Chong Kam, Tamil Selvy Selvamuniandy, and Charan Gurumurthy. "Discoloration related failure mechanism and its root cause in Electroless Nickel Immersion Gold (ENIG) Pad metallurgical surface finish." Physical and Failure Analysis of Integrated Circuits, 2004. IPFA 2004. Proceedings of the 11th International Symposium on the. IEEE, 2004.
3. IPC-4552 – Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

ENIG Less than Minimum

Contributors

- Improper cleaning of surfaces.
- Improper or inadequate rinsing.
- Bath parameters not being followed (pH and chemical).
- Bath temperature too low.
- Copper surface not clean of oil or inhibiting film.

Resolution

- Re-clean copper using chemical cleaners or mechanical
- scrubbing Institute micro-etch step to improve cleaning
- Improve rinsing(Check flow, agitation and water quality)
- Raise temperature per supplier specifications
- Readjust to supplier operational parameters

Summary of Supplier Study

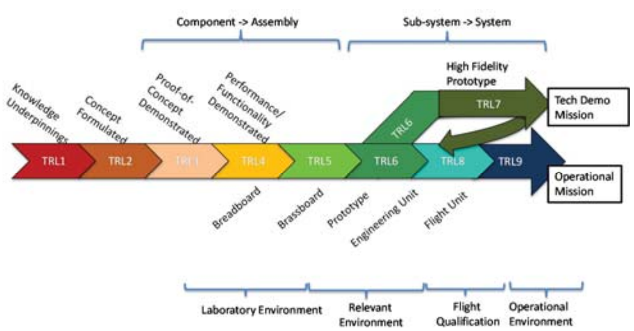
- The test data is analyzed using statistical method to provide trend analysis for all suppliers.
  - Root cause(s) and key contributors are identified.
  - Mitigation plan is included for the root cause of nonconformance.
- Provide recommendations to the supplier's process, identification and prediction of nonconforming process limit criterion, and to improve test standards.
- New technologies (example: smaller annular rings, via-in-pads, thinner laminates or newer plating) are implemented on the basis of supplier maturity and reported NCs.

New technology Implementation: Technology Readiness Levels

Technology Readiness Levels

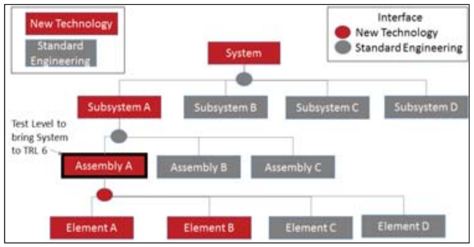
"TRLs are a set of metrics that enable the assessment of the maturity of a particular technology and the consistent comparison of the maturity between different types of technology in the context of a specific application, implementation, and operational environment."

Once TLR6 is demonstrated, the risk associated with the new technology is roughly equivalent to the risk of a new design that employs standard engineering practice and is bounded by previously implemented ground-based systems.



TRL Implementation – Considerations

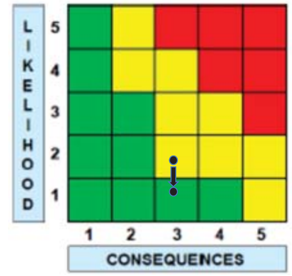
- A new technology can be at a different TRL depending on the requirements.
- Not all new designs are new technology
  - Some may be considered "standard engineering" (e.g., a new primary structure based on existing design and fabrication processes)



- The configuration for TRL verification occurs at the lowest level of integration that exhibits the new performance/functionality.
- The "weakest link" approach is used to determine the TRL of a subsystem
  - There can be cases where a subsystem's TRL is lower than that of all of its elements (e.g., a new architecture that is used to provide new performance, but employs all "heritage parts").

Risk Based Technology Evaluation and Insertion

Risk



Risk is an expectation of loss in statistical terms.

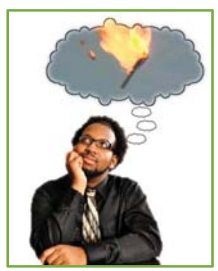
Definition: the combination of

a) the probability (qualitative or quantitative) that an undesired event will occur, and
b) the consequence or impact of the undesired event

- Flavors of risk (consequences)
  - Technical (failure or performance degradation on-orbit)
  - Cost ($ it will take to fix the problem)
  - Schedule (time to fix the problem)
  - Safety (injury, death, or collateral damage)

Communicating risk is key to portraying the status of a new technology and project in development.

Risk vs. Possibility



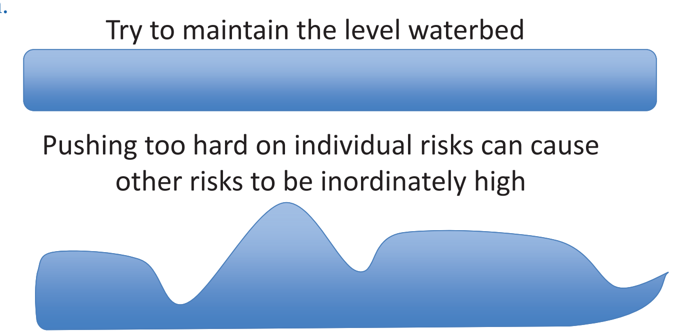
- Failure modes and mechanisms can appear through
  - Analysis and simulation
  - Observation
  - Prior experiences
  - Brainstorming "what if" scenarios
  - Speculation
- These all constitute ***possibilities***

- There is a tendency to take action to eliminate severe consequences regardless of the probability of occurrence
- **When a possibility is combined with an environment, an operating regime, and supporting data, a risk can be established—this is core to the engineering process.**

- Lack of careful and reasoned analysis of each possibility in terms of the conditions that results in the consequence and the probability of occurrence **will** result in excessive cost and **may** increase the overall risk.

Balanced Risk - Maintaining a Level Waterbed*

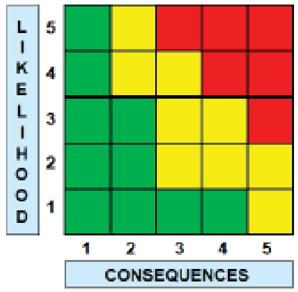
A systems approach of looking across all options to ensure that mitigating or eliminating a particular risk does not cause much greater risk somewhere in the system.



** - Leitner, J., Sood, B., Isaac, E., Shue, J., Lindsey, N., & Plante, J. (2018). Risk-Based Safety and Mission Assurance: Approach and Experiences in Practice. Quality Engineering, (just-accepted), 1-40.*

Impact of Non-conformances

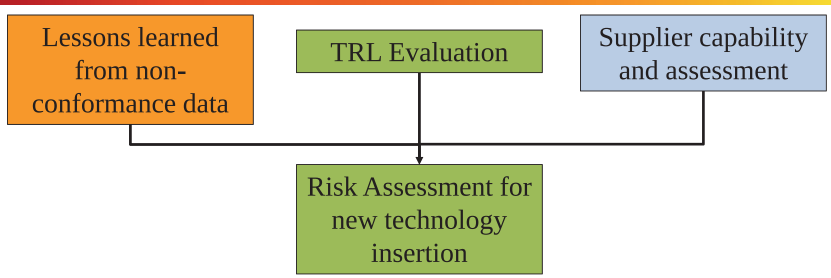
- Bare boards cost $$ and build schedules – expensive!!
- But failures are even more expensive!
- Test sample nonconformance is not the same as PCB failure.
- Risk-based decisions are used for disposition of non-conformances.
- Non-conformances may have little to no impact per application.
- Began to explore origins and merit of requirements (more later).



Risk Assessment

- Traceable PCB test coupons (designed per specs. such as IPC-2221B) are submitted to GSFC or to a GSFC-assessed laboratory.
- Reports that indicate nonconformance are dispositioned by risk assessment performed prior to refabricating or populating the PCB.
  – If risk assessment indicates elevated risk due to the nonconformance, then use is dispositioned by MRB.
- Risk assessment process eliminates waste and saves money and schedule, lowers overall risk for the project.
- The process reduces the need for repeated attempts to refabricate.

Summary



- Risk-based new technology assessment centered around understanding all sides of risk.
- Lessons learned are at the core of the methodology
- This approach is effective at saving cost and schedule resources.
- Enables any project to operate at the lowest possible risk posture given its particular resource constraints.

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Backup Slides

TRL Definition and Decomposition by Factor*

TRL	Definition from NPR 7123.1e	Completion Criteria from NPR 7123.1e	Mission Req.	Performance/ Function	Fidelity of Analysis	Fidelity of Build	Level of Integration	Environment Verification
4	Component and/or bread-board validated in laboratory environment	Documented test performance demonstrating agreement with analytical predictions. Documented definition of relevant environment.	Generic class of missions	Basic functionality/ performance demonstrated	Medium fidelity: to predict key performance parameters and life limiting factors as a function of relevant environments	Low fidelity: bread-board	Component/Assembly	Tested in laboratory for critical environments Relevant environments identified. Life-limiting mechanisms identified.
5	Component and/or brass-board validated in relevant environment	Documented test performance demonstrating agreement with analytical predictions. Documented definition of scaling requirements.	Generic or specific class of missions	Basic functionality/ performance maintained	Medium fidelity: to predict key performance parameters and life limiting factors as a function of relevant environments	Medium fidelity: brass-board with realistic support elements	Component/ Assembly	Tested in relevant environments Characterize physics of life-limiting mechanisms and failure modes.
6	System/ subsystem model or prototype demonstrated in a relevant environment	Documented test performance demonstrating agreement with analytical predictions	Specific mission	Required functionality/ performance demonstrated	Medium fidelity: to predict key performance parameters and life limiting factors as a function of operational environments	High fidelity: prototype that addresses all critical scaling issues	Subsystem/ System	Tested in relevant environments. Verify by test that the technology is resilient to the effects of life-limiting mechanisms
7	System prototype demonstration in an operational environment	Documented test performance demonstrating agreement with analytical predictions	Tech-nology demon-stration mission	Required functionality/ performance demonstrated	High fidelity: to predict key performance parameters and life limiting factors as a function of operational environments	High Fidelity: prototype or engineering unit that addresses all critical scaling issues	Subsystem/System	Tested in actual operational environment
8	Actual system completed and "flight qualified" through test and demonstration	Documented test performance verifying requirements and analytical predictions	Specific mission	Required functionality/ performance demonstrated	High fidelity: to predict key performance parameters and life limiting factors as a function of operational environments	Final product: Flight unit; Life test unit for life limited items*	System	Tested in project environmental verification program. Completed life tests.
9	Actual system flight proven through successful mission operations	Documented mission operational results verifying requirements	Specific mission	Required functionality/ performance demonstrated	High fidelity: to predict key performance parameters and life limiting factors as a function of operational environments	Final product: Flight unit	System	Operated in actual operational environment

NASA Systems Engineering Processes and Requirements (NPR) 7123.1B (Table 3.1.3-1)

Fidelity of Build

Table 3.1.6-1: Fidelity of Build

	Unit	Purpose	Performance/ Function	Form and Fit/ Scaling	Environmental Requirements	Pedigree
New Technology Development	Breadboard	Proof-of-concept for a potential design	Demonstrate performance/ function	Not required, e.g. laid out flat on lab table	Tested in a laboratory environment	NA
	Brassboard	Demonstrate feasibility of form and fit, environments	Demonstrate performance/ function	Approximate (not flat) with scaling factors understood	Designed to meet relevant environmental requirements	NA
	Prototype	Representative design; pathfinder; demonstrator	Tested to meet performance/ function requirements	Representative with scaling factors understood	Tested to meet relevant environmental requirements	NA, but may be partial or full
Engineering Development	Engineering Unit	Finalize detailed design	Tested to meet performance/ function requirements	Exact as known at time of build	Tested to meet relevant environmental requirements	NA, but may be partial or full
	Qualification Unit	Qualify design	Tested to meet performance/ function requirements	Exact as known at time of build	Tested to meet flight qualification environmental requirements	Full
	Flight Unit	Final Product	Tested to meet performance/ function requirements	Exact	Tested to meet flight qualification environmental requirements	Full
	Flight Spare	Final Product	Tested to meet performance/ function requirements	Exact	Tested to meet flight qualification environmental requirements	Full

TRL 6

At the Subsystem level

- Specific mission (and specific mission risk class)
- Required functionality/ performance demonstrated
- Medium fidelity: to predict key performance parameters and life limiting factors as a function of operational environments
- High fidelity: prototype that addresses all critical scaling issues
- Subsystem tested in relevant environments.
  - Verify by test that the technology is resilient to the effects of life-limiting mechanisms
  - Note, “relevant environment” is a subset of the operational environment and specifically focuses on “stressing” the new technology

Risk Classification (NPR 7120.5 Projects)

- **Class A: Lowest risk posture by design**
  - Failure would have extreme consequences to public safety or high priority national science objectives.
  - In some cases, the extreme complexity and magnitude of development will result in a system launching with many low to medium risks based on problems and anomalies that could not be completely resolved under cost and schedule constraints.
  - Examples: HST and JWST
- **Class B: Low risk posture**
  - Represents a high priority National asset whose loss would constitute a high impact to public safety or national science objectives
  - Examples: GOES-R, TDRS-K/L/M, MAVEN, JPSS, and OSIRIS-REX
- **Class C: Moderate risk posture**
  - Represents an instrument or spacecraft whose loss would result in a loss or delay of some key national science objectives.
  - Examples: LRO, MMS, TESS, and ICON
- **Class D: Cost/schedule are equal or greater considerations compared to mission success risks**
  - Technical risk is medium by design (may be dominated by yellow risks).
  - Many credible mission failure mechanisms may exist. A failure to meet Level 1 requirements prior to minimum lifetime would be treated as a mishap.
  - Examples: LADEE, IRIS, NICER, and DSCOVR